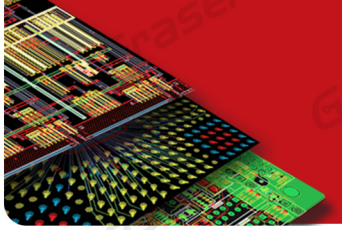
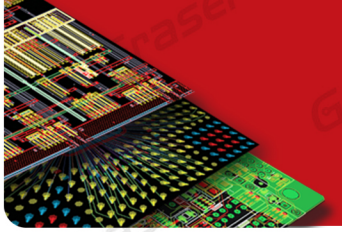


Cadence SiP Design Feature Summary

	SiP Layout*	SiP Layout and Chip Integration Option	SiP Digital Architect	SiP Digital SI**	SiP RF Architect
Front-End Design Creation					
System Connectivity Manager with logical co-design objects			XL/GXL		
Full SiP LVS (substrate and ICs)			XL/GXL		o
Virtuoso Analog Design Environment, schematic/layout integration and flow					o
Substrate-level embedded RF passive synthesis					o
Parasitic backannotation into system-level testbenches					o
Signal Integrity					
SigXplorer topology editor and simulator (pre-route)			GXL	o	
SigXplorer topology editor and simulator (pre- and post-route)				o	
S-Parameter interconnect modeling and SI simulation			GXL	o	
Source synch and serial interface simulation			GXL	o	
3D PCB full-package simulation model creation			GXL	o	
Embedded integration with a (third-party-supplied) 3D field solver			GXL	o	
Co-planar coupling extraction			GXL	o	
Spectre transistor-level simulation engine			GXL	o	
Channel analysis for high-capacity SI simulation			GXL	o	
Power delivery network (PDN) optimization and verification				o	
Etch back stub effects simulation			GXL	o	
Package/pin delay length report			GXL	o	
Substrate Design					
Constraint Manager (electrical/physical and DRC)	o	o	XL/GXL	o	
Import/export Allegro Package Designer (.mcm) database	o	o	GXL	o	
Interactive (i/a) and automatic component (packaged and bare die) placement	o	o	GXL	i/a only	
Auto/interactive wirebonding including rapid autobond	o	o	GXL		
User-definable wirebond model profiles including XML import	o	o	GXL		



	SiP Layout*	SiP Layout and Chip Integration Option	SiP Digital Architect	SiP Digital SI**	SiP RF Architect
Full and partial design connectivity assignment and optimization (router based, closest match, inter-active, and constraint-based)	o	o	GXL		
Interactive and automatic interconnect routing (free angle and multi-layer orthogonal)	o	o	GXL		
On-line soldermask checking	o	o			
Recursive breakout pattern creator (flip-chip and wirebond)	o	o			
Static-style screen rulers		o			
Advanced Design					
Distributed co-design with die editor (using die abstract)	o	o	GXL		
Concurrent co-design with I/O planning co-design editor (using LEF/DEF and OA 2.2)		Unix/Linux only	GXL (Unix/Linux only)		
Hierarchical GDSII output	o	o			
Team-based design (design partitioning)	o	o			
Embedded RF passive creation and editing		o			
3D Design Viewer and 3D wirebond DRC	o	o	GXL	o	
3D die stack editor	o	o	GXL	o	
Support for multiple die stacks	o	o	GXL	o	
Interconnect cline spreading	o	o			
BGA editor	o	o	GXL	o	
Constraint-driven HDI design	o	o	GXL	o	
DFM Preparation/Output					
Die/BGA footprint compare using DEF/OA/.TXT	o	o			
Filled shapes (metal) creation and editing	o	o			
Design documentation (dimensioning, annotation)	o	o			
Assembly rule checking (ARC) system	o	o			
Etch back of plating traces	o	o			
Plating bar generation	o	o			
Manufacturing /documentation export/import capabilities (stream, dxf, AIF)	o	o			
Substrate mask output (Gerber, GDSII)	o	o			
Full design-status reporting capabilities	o	o			
Waived DRCs (creation and reporting)	o	o			
Degassing of filled metal shapes	o	o			
Thieving (metal area balancing)	o	o			

** Note that license for this product also authorizes use of Allegro Package Designer at the XL level (see Allegro Package Designer datasheet)*
*** Note that license for this product also authorizes use of Allegro Package SI at the XL level (see Allegro Package Designer datasheet)*