

OrCAD^x AutoCAD

電路與機構零距離
2016 SPB SEMINAR TAINAN



訊號阻抗耦合驗證 – Sigrity ERC

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Topic



- What's OrCAD Sigrity ERC?
- OrCAD Sigrity ERC
 - Trace Reference Check
 - Trace Coupling Check
 - Trace Impedance Check
- OrCAD Sigrity SRC
- Summary

What's OrCAD Sigrity ERC?

- OrCAD[®] Sigrity[™] Electrical Rules Check (ERC) 可使 PCB 設計師快速篩選 PCB 設計的信號品質，而無需給予任何模擬模型，或者是一個完整信號。
 - 超越 DRC 檢查規範
 - 為 PCB 設計找出阻抗不連續
 - 進行 layout 走線串擾評估

OrCAD Sigrity ERC 可以不須依賴的 SI 工程師，在 PCB 佈局階段即可以發現信號質量問題，進而提升產品設計效率以達到縮短整體設計時間。



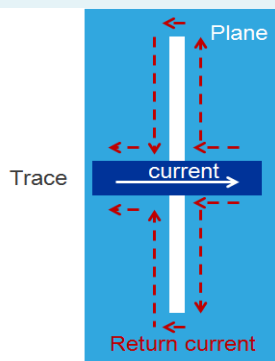
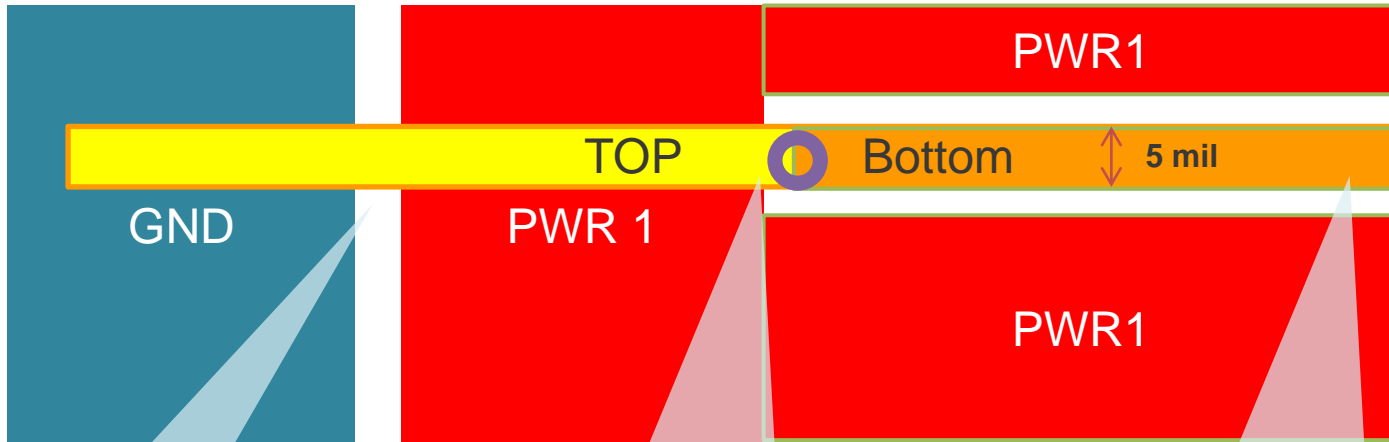
OrCAD Sigrity ERC

Signal integrity electrical checks for PCB designers

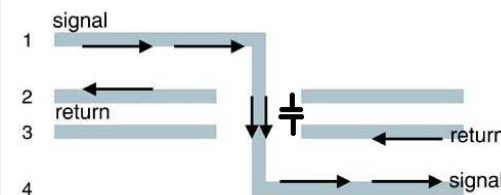
OrCAD Sigrity ERC

Layout 阻抗與串擾問題

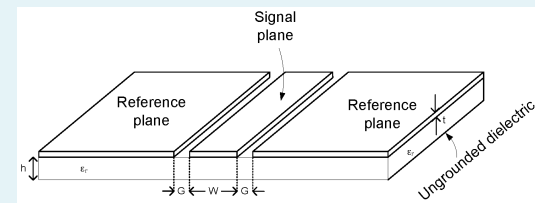
- Talk about impedance Z_0 , let's see the following case:
 - After simulation, you set the trace width to be 5 mil in the constraint system to achieve the impedance you want. Of course, the following picture will show **no DRC** violation. **But if this is a 2-layers design and...**



1. Reference change
2. Cross plane split



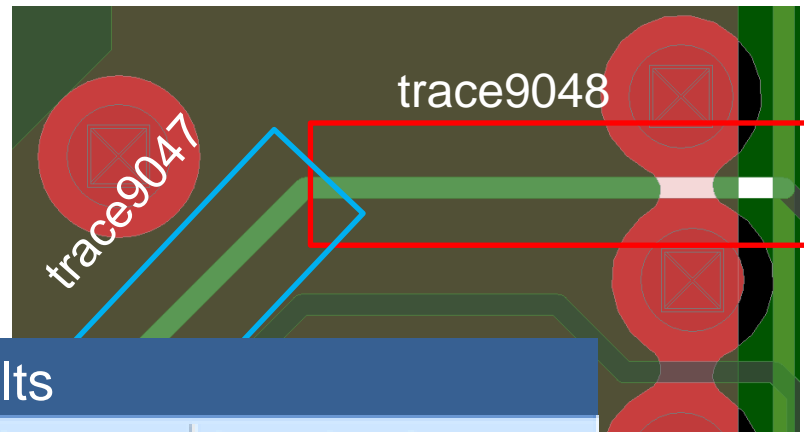
1. Layer Transition



1. Coplanar reference

ERC – 走線上 / 下層面的 參考電源層

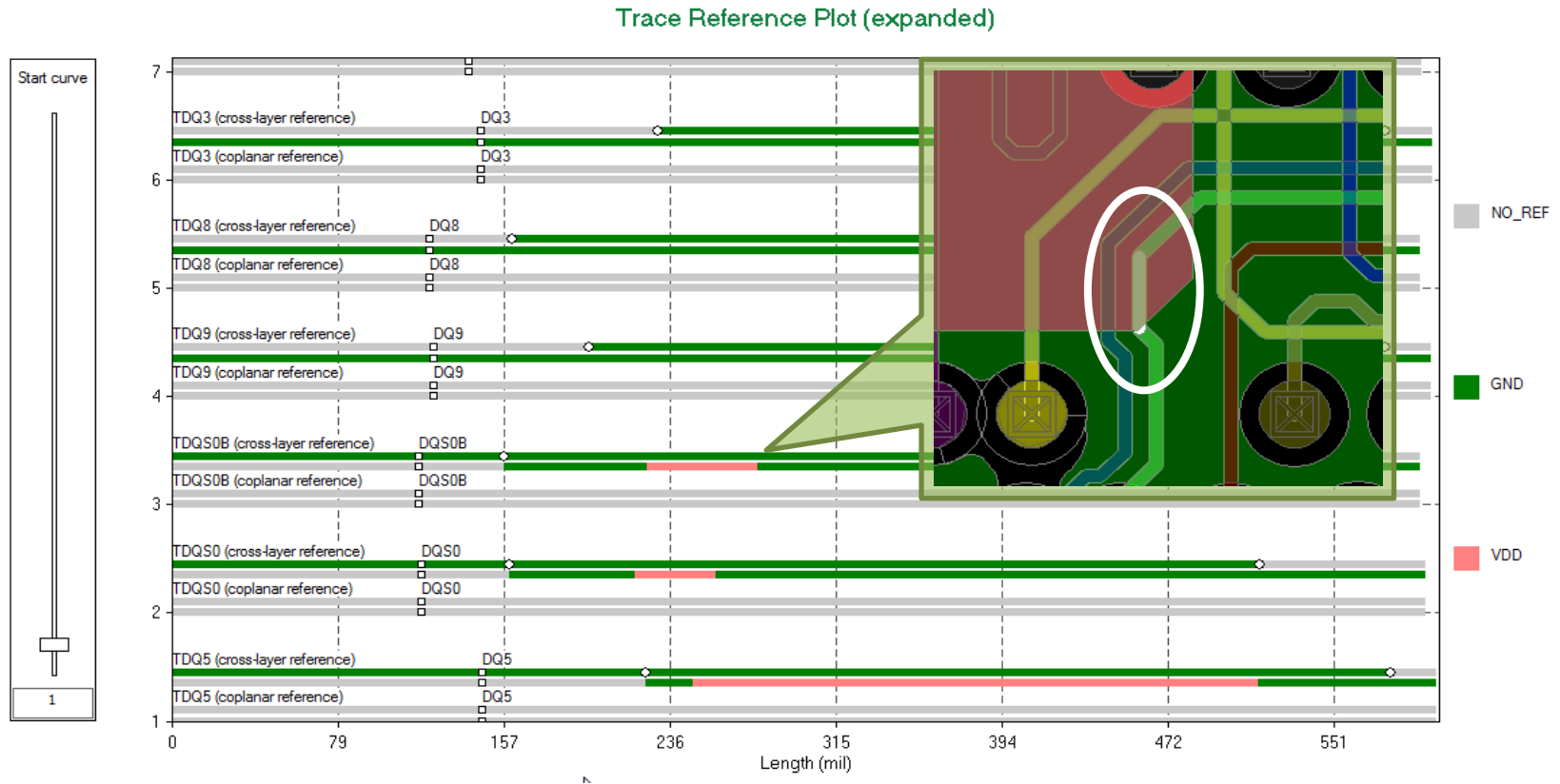
- Based on upper / lower layer references
 - Trace9047 → one section
 - Trace9048 → 5 sections



ERC results			
Trace Name	Length (%)	Upper-lyr ref net name	Lower-lyr ref net name
Trace9047::DQ0	11.58	GND	VDD
Trace9048::DQ0	12.74	GND	VDD
Trace9048::DQ0	1.78	VDD	VDD
Trace9048::DQ0	0.11	-	VDD
Trace9048::DQ0	0.89	GND	VDD
Trace9048::DQ0	1.66	GND	GND

*Note:
This is the reason why
there are 5
impedance sections.*

走線參考電源層檢查



- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

走線耦合計算

- Trace9047 is one uniform impedance section
- Trace9047 broken into 5 sections based on trace coupling
 - two no coupling sections (1 & 5)
 - two 2-line coupling sections (2 & 4)
 - one 3-line coupling section (3)

ERC results			
Trace Name	Aggressor Trace Names	Coupling Coefficient (%)	Length (%)
Trace9047::DQ0	-	-	← 1 1.82
Trace9047::DQ0	Trace9024::DQ1	5.3	← 2 1.46
Trace9047::DQ0	Trace9024_Auto_190::DQ1	5.3	← 3 1.16
	Trace8280::DQ4	0.6	
Trace9047::DQ0	Trace9024_Auto_191::DQ1	5.3	← 4 4.10
Trace9047::DQ0	-	-	← 5 3.04



走線阻抗檢查

<input checked="" type="checkbox"/>	P3E_SLOT2_TX_C_DP0
<input checked="" type="checkbox"/>	P3E_SLOT2_TX_C_DP1
<input checked="" type="checkbox"/>	P3E_SLOT2_TX_C_DP2
<input checked="" type="checkbox"/>	P3E_SLOT2_TX_C_DP3
<input checked="" type="checkbox"/>	P3E_SLOT2_TX_C_DP4

Impedance (Ohm)

220

140

120

80

0

197

394

591

787

984

1181

1378

1575

3

2

1

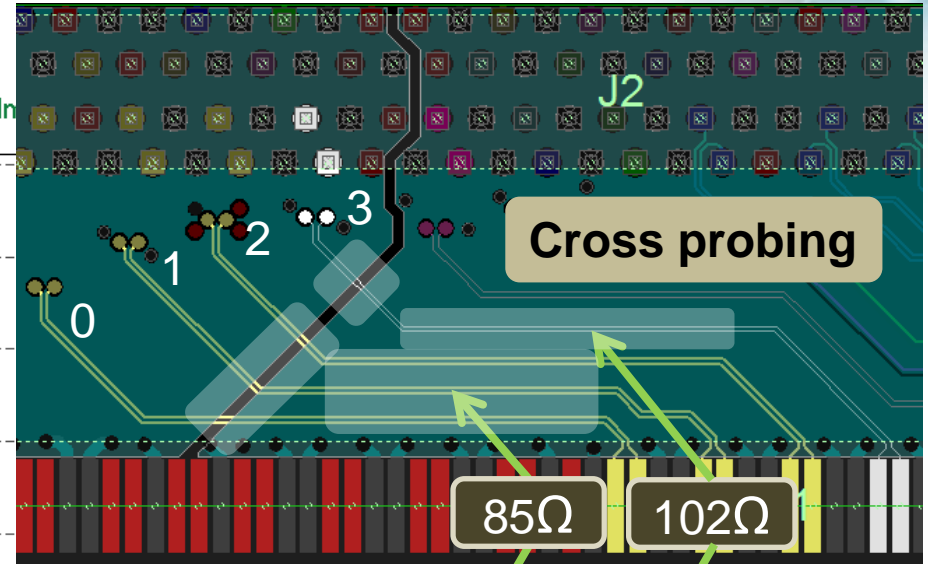
0

85Ω

102Ω

Cross probing

- This check helps you to identify,
 - Wrong trace width spacing (diff. pair)
 - Cross moat
 - Highly trace impedance



- Visually or tabular result for trace impedance check that shows trace segments mismatch with target impedance.

走線阻抗檢查

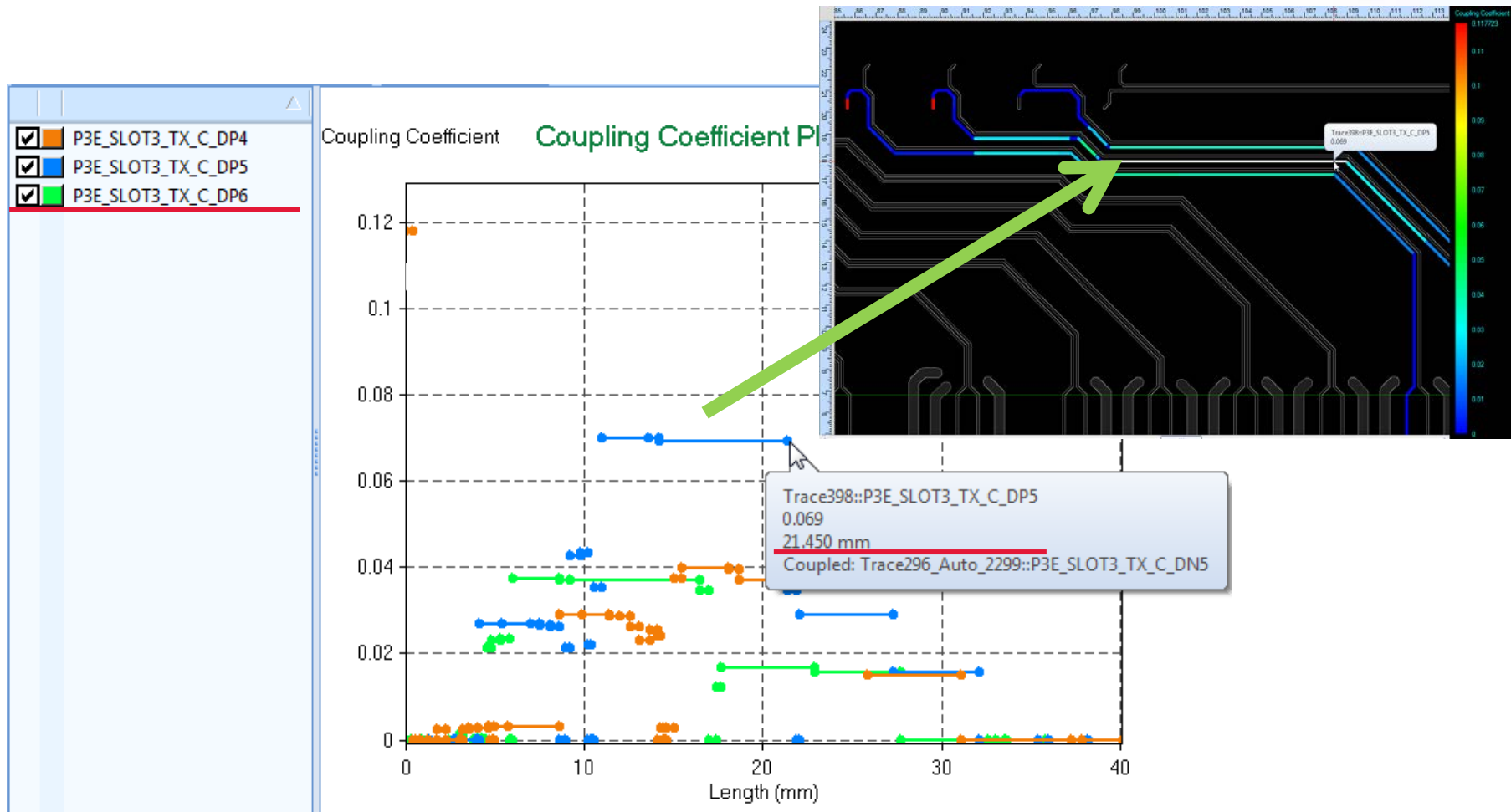
Cross Probing

- Auto-Zoom in board.

The screenshot displays two software windows side-by-side. The left window is 'Allegro Sigrity SI (PCB): DDR3_LRDIMM166.brd' showing a PCB layout with a blue selection box around a component. The right window is 'SPEED2000 Generator - [DDR3_LRDIMM166 Layer View]' showing an impedance plot of the selected net. The plot features a color scale for impedance in Ohms, ranging from 32.9703 (blue) to 81.0385 (red). The plot shows several traces with varying impedance values. The right window also includes a 'Layer S...' panel with a list of signal layers (Signal\$T0F to Signal\$B0T) and an 'Output' panel with 'Miscellaneous' and 'Output Folder Browser' options. The status bar at the bottom indicates 'Mouse(mm): X: 64.814, Y: 6.154'.

走線耦合檢查

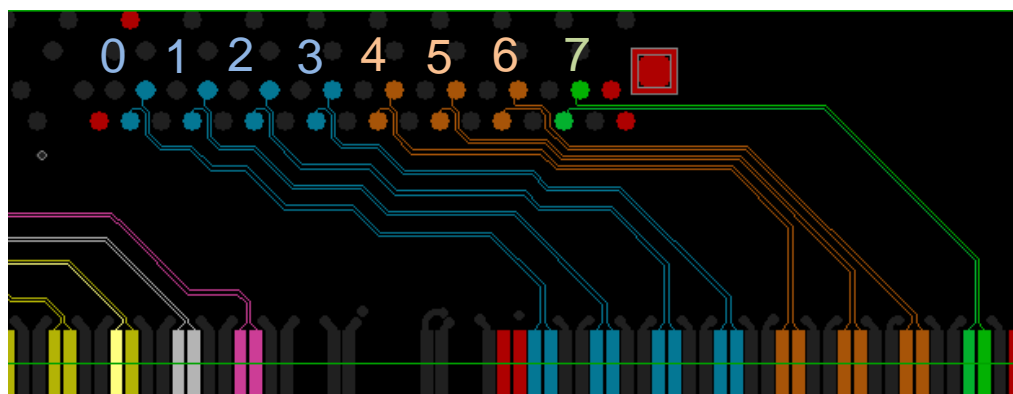
- Cross probing helps to resolve issue intuitively



走線耦合檢查

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
1	P3E_SLOT2_TX_C_DP0-P3E_SLOT2_TX_C_DN0	P3E_SLOT2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
2	P3E_SLOT2_TX_C_DP1-P3E_SLOT2_TX_C_DN1	P3E_SLOT2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
3	P3E_SLOT2_TX_C_DP2-P3E_SLOT2_TX_C_DN2	P3E_SLOT2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
4	P3E_SLOT2_TX_C_DP3-P3E_SLOT2_TX_C_DN3	P3E_SLOT2_TX_C_DN2	0.135%	36.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.135%	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

18X

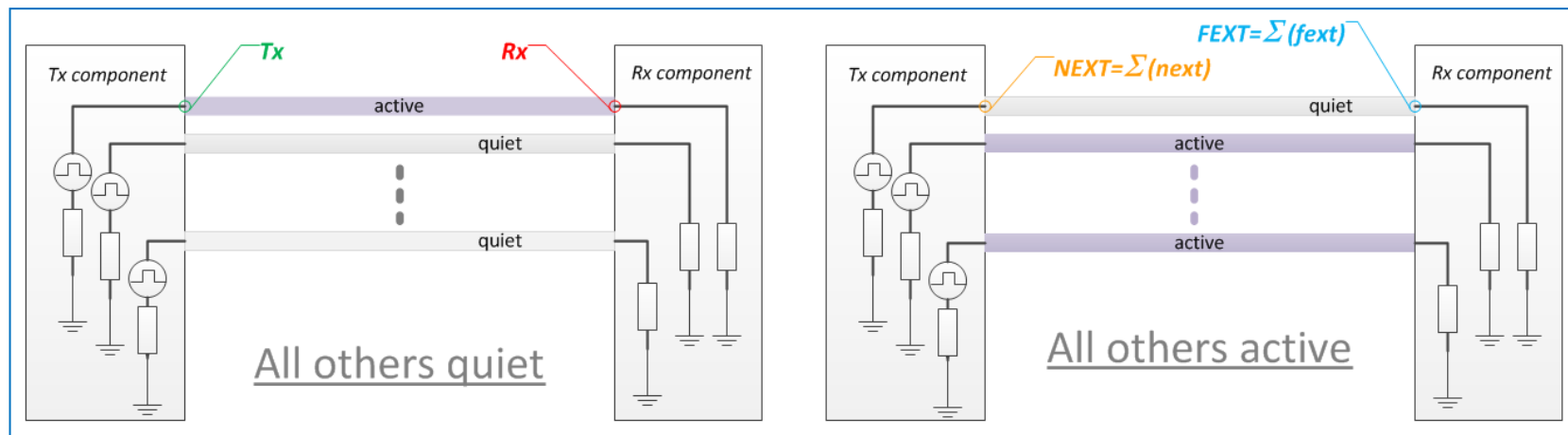


Through this test, you will see,

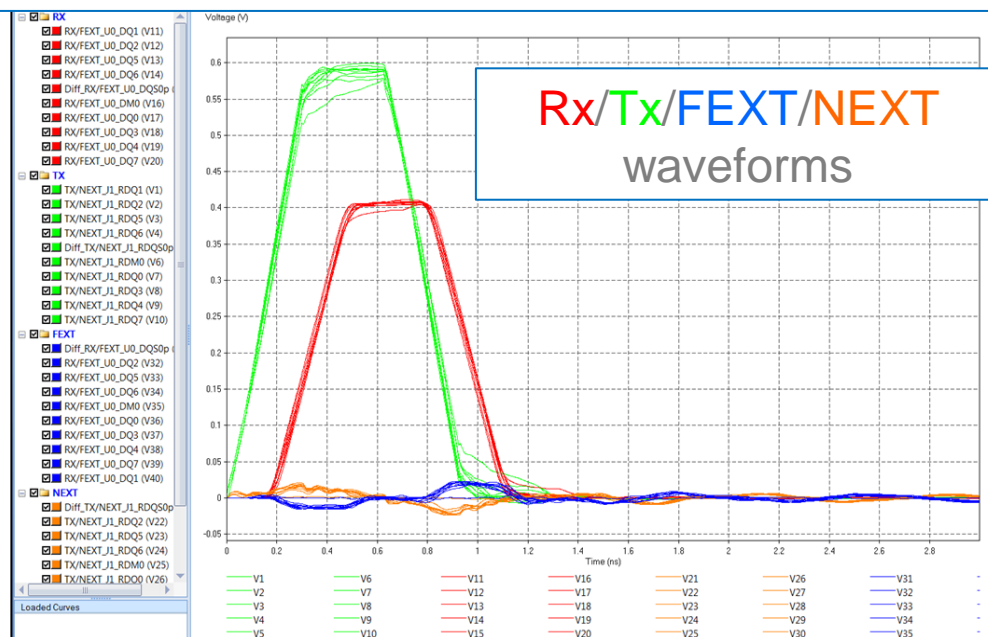
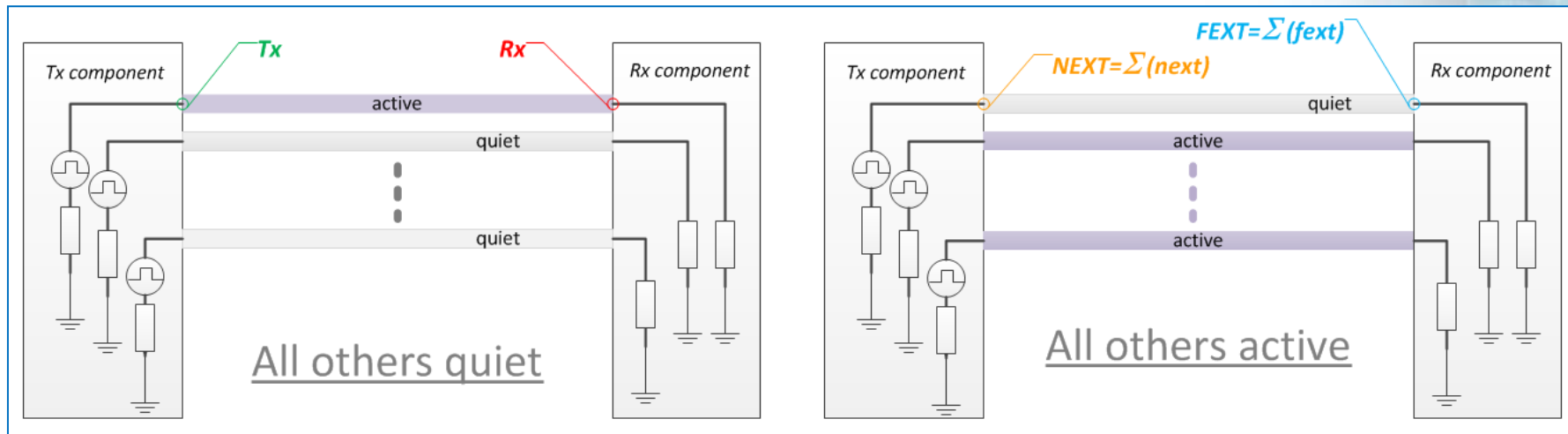
- Tight coupling pairs
- Max coupling aggressor
- Dangerous vs. safe coupling
→ **18X** (= 2.81% / 0.156%)

What is Sigrity SRC?

- Sigrity SRC is Macro, combined, net-level view in time-domain of impact due to ERC violations measured in mv&ps (no device model needed)
 - Setup considering termination impedance, data rate (pulse width, rise/fall time), and amplitude
 - Results with Tx/Rx/NEXT/FEXT waveforms, SI performance metrics
 - Organized to easy SI performance interpretation along with ER
- Practical for board level check (setup, simulation, report)



Time-domain Waveforms



Summary

- Sigrity ERC / SRC fills the gap between layout designers and SI engineers
 - Expanded expertise
 - Using same tools
 - Measured by same units



Layout/Board designer -----> *SI engineer*

Layout tools -----> *Simulation tools*

Geometry domain (mil/mm) -----> *Electrical domain (mv, ps)*