

# OrCAD<sup>x</sup> AutoCAD

電路與機構零距離

2016 SPB SEMINAR TAINAN



## 輕鬆面對 PCB Layout 挑戰 – OrCAD PCB Designer

Mika Ho / Graser

2 / Sep / 2016

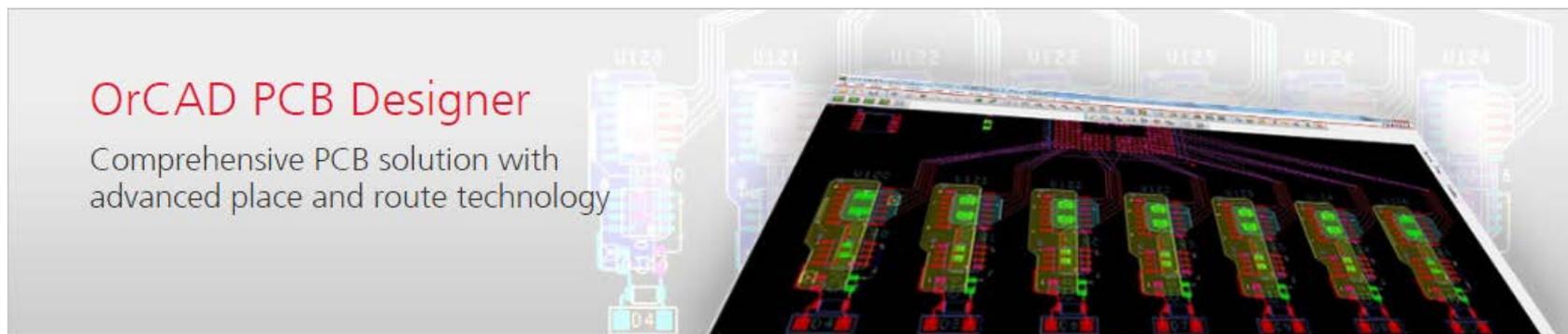
# Topic



- What's OrCAD PCB Designer?
- OrCAD Capture CIS Support
- OrCAD PCB Designer
  - The Integration of Capture and OrCAD PCB
  - Library
  - Placement
  - Routing
  - Shape
  - Constraint Manager
    - Spacing
    - Physical
    - Differential Pair
    - Min/Max Propagation Delay
    - Relative Propagation Delay
  - Support XNet
  - Segments Over Voids
  - Flex and Rigid Flex Technologies
- GraserWARE EnhancePack

# What's OrCAD PCB Designer?

- OrCAD<sup>®</sup> PCB Designer 是款強大又有高度整合性的 PCB 設計軟體，讓您從電路原理的線路圖設計進展到最終底片等工程資料的輸出
  - 包含 Capture CIS 線路圖設計及零件庫管理
  - 完善的 Constraint Manager 定義 PCB Layout 規範
  - PCB 佈局及佈線功能

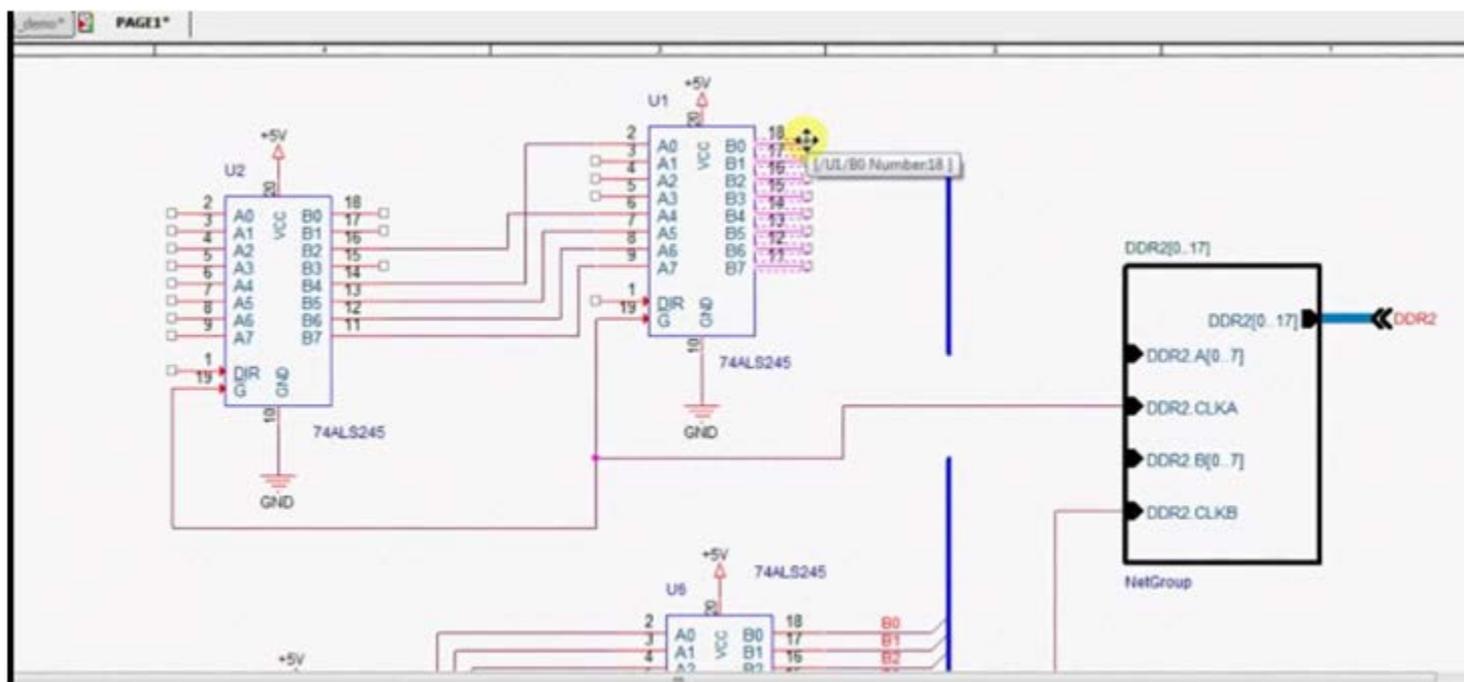


# OrCAD Capture CIS Support

# OrCAD Capture CIS Support

- Powerful Schematic Entry

- 可透過階層式電路及 Variant 方式來簡化複雜的線路設計以達縮短設計時間

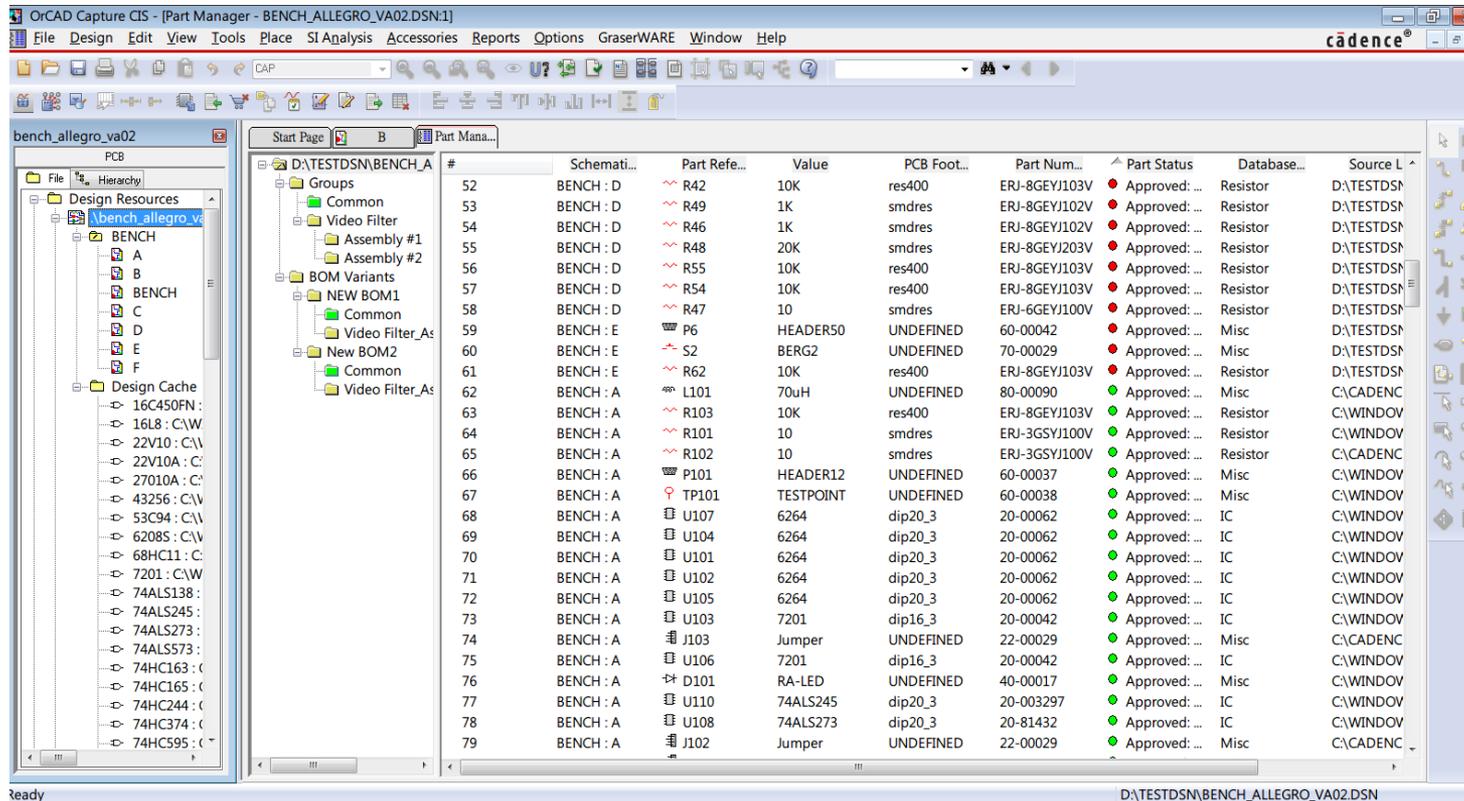


# OrCAD Capture CIS Support



- Powerful Schematic Entry

- OrCAD® Capture CIS (Component Information System) 讓您能夠輕鬆的管理並存取公司的零件庫

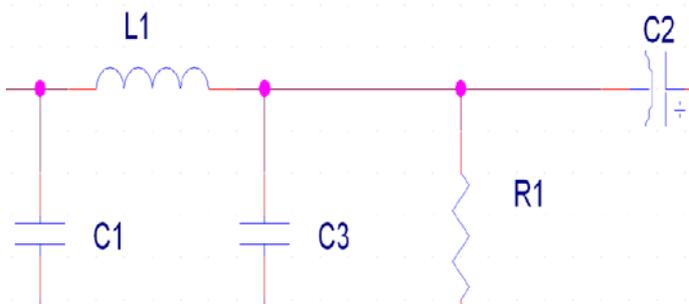


# OrCAD PCB Designer

# The Integration of Capture and OrCAD PCB

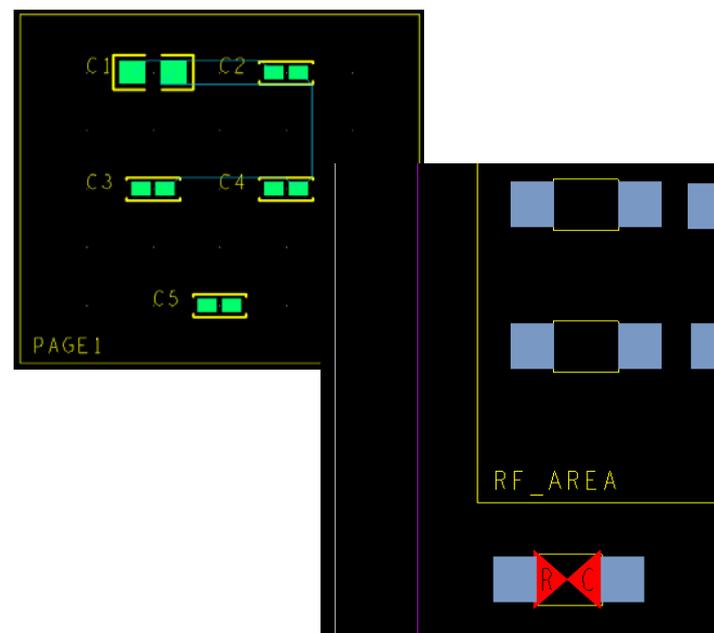
- Properties from Capture to OrCAD PCB
  - 可將線路圖中的訊號及零件帶上相關的屬性再轉入 PCB

## Capture



REFERENCE	C1	C2	C3	L1	R1
REUSE_INSTANCE					
TOL					
REUSE_MODULE					
ROOM	RF_AREA	RF_AREA	RF_AREA	RF_AREA	RF_AREA
SIGNAL_MODEL					
Source Library	D:\ORCAD\WIN98\CAP	C:\WINDOWS\TEMPX	D:\ORCAD\WIN98\CAP	C:\WINDOWS\TEMPX	C:\WINDOWS\TEMPX
SWAP_GROUP					
T_TEMPERATURE					
VALUE	390PF	10UF	820PF	282u	75
VOLTAGE	50V	50V	50V		

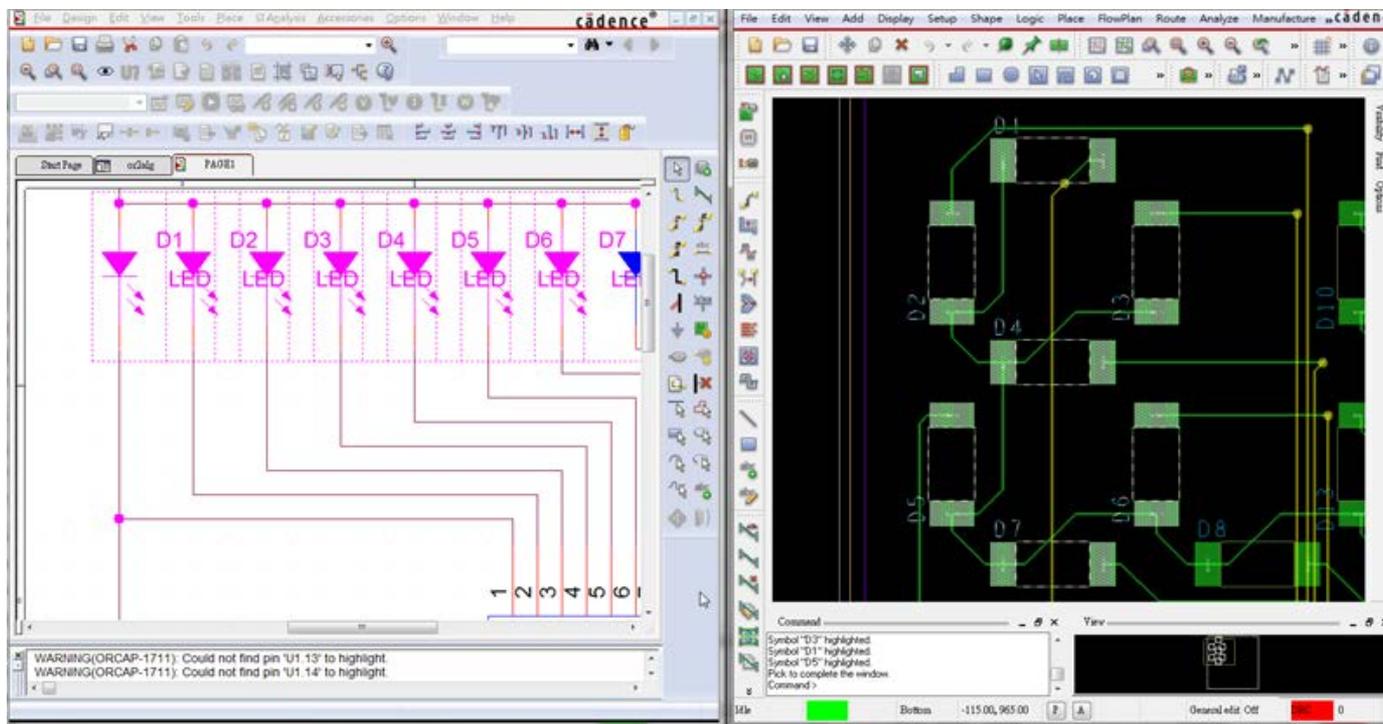
## PCB



# The Integration of Capture and OrCAD PCB

- Cross Probe

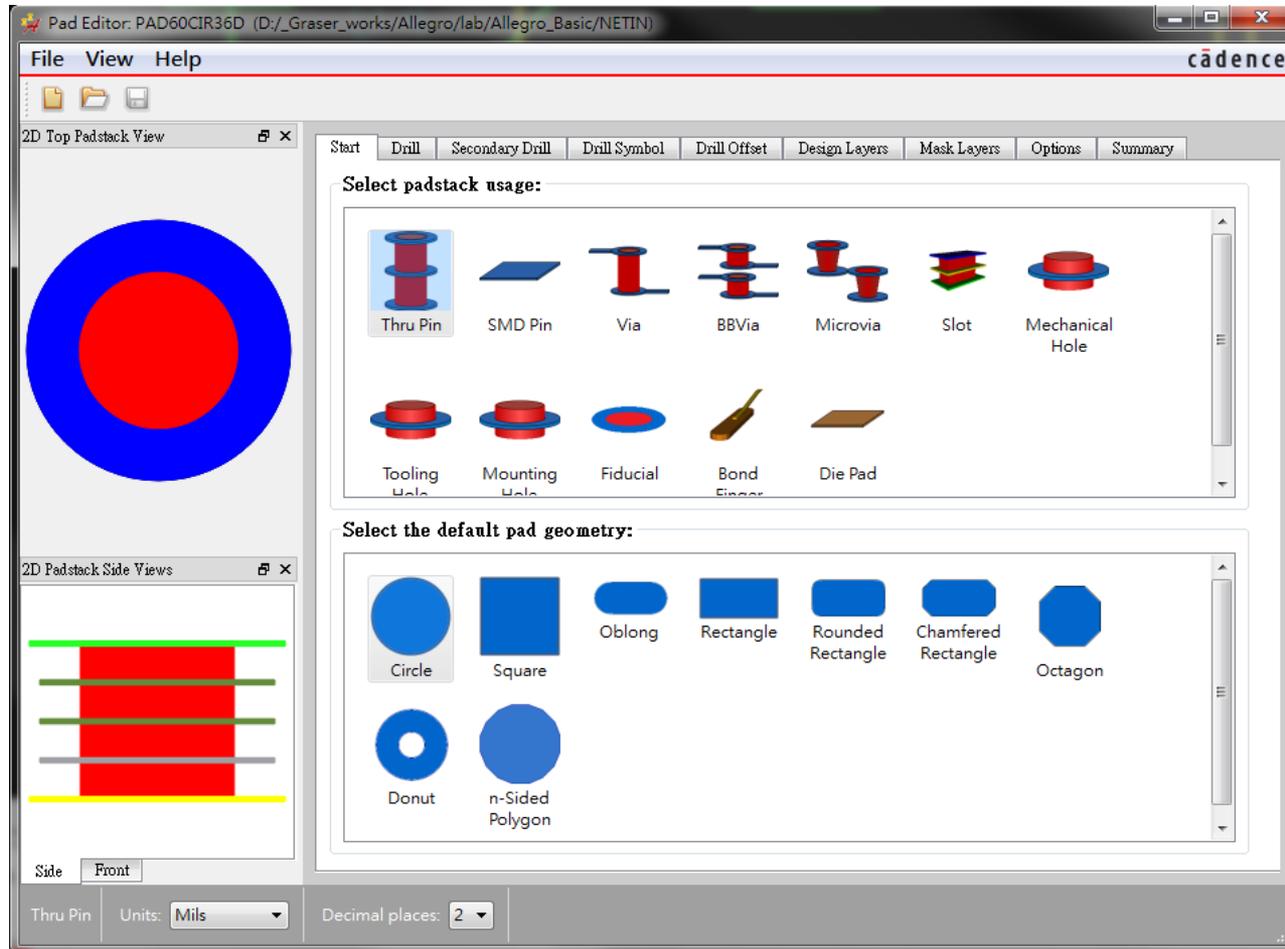
- 雙向 Highlight 能讓使用者即時的了解到相關的訊號、零件及走線位置；而搭配 PCB 擺放零件也能透過此功能快速選取相關零件放置，提高工作效率



# OrCAD PCB / Library

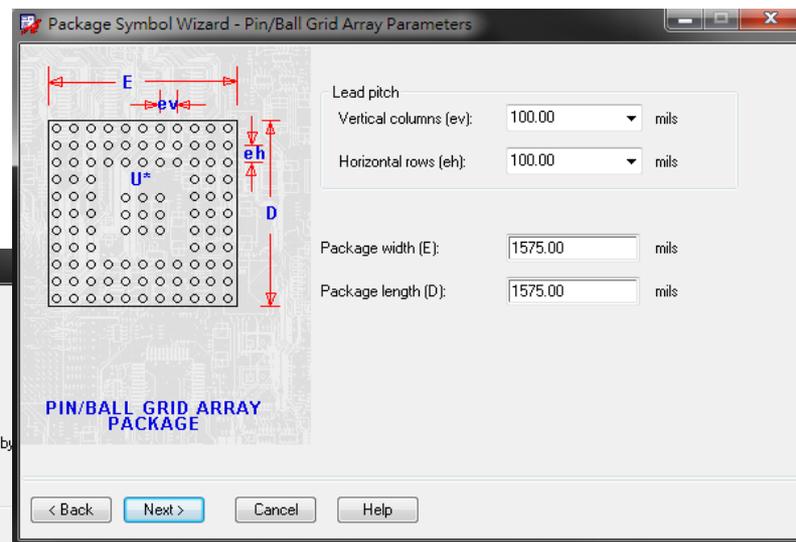
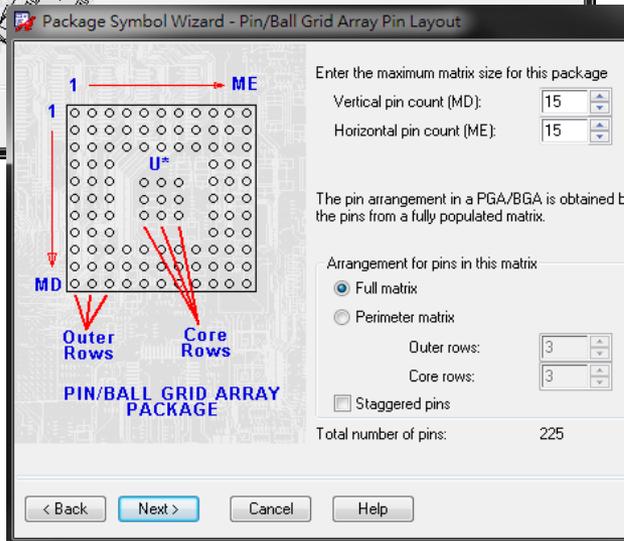
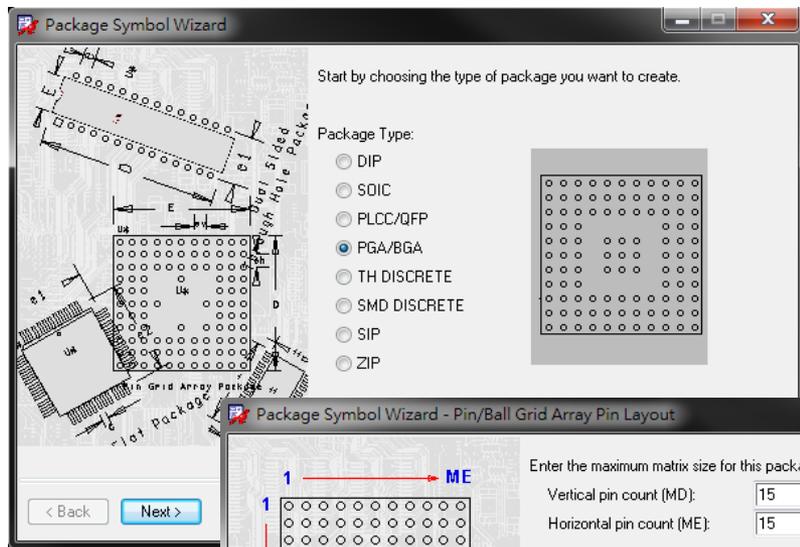


- Pad stack Editor



# OrCAD PCB / Library

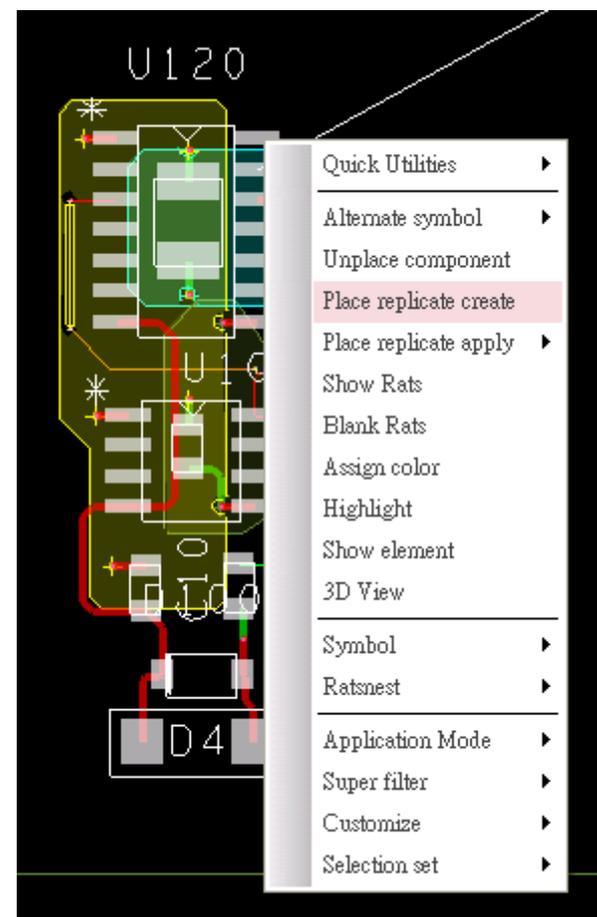
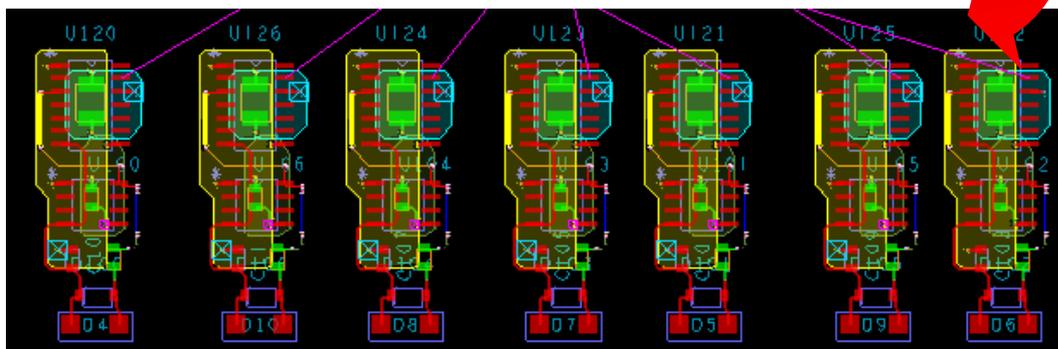
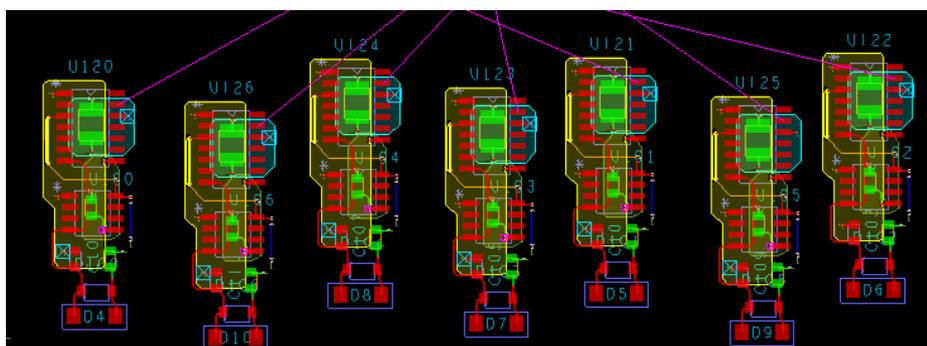
- Component : 零件精靈



# OrCAD PCB / Placement

- Placement Replication

- 藉由 Module reuse 方式將設計中同樣連線架構的部分做快速的套用

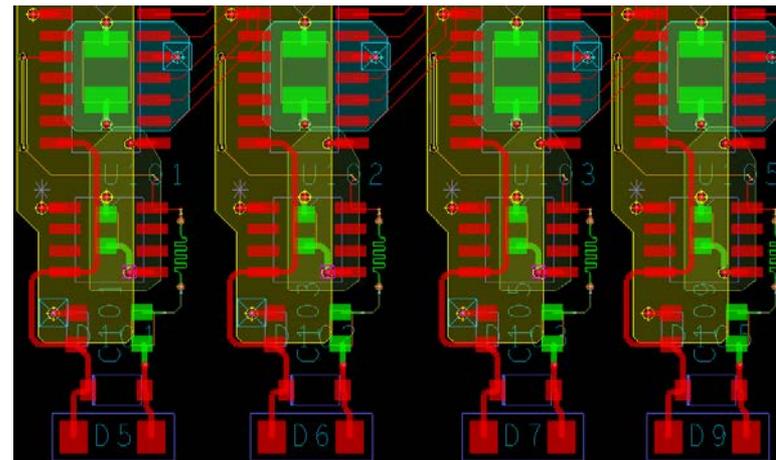
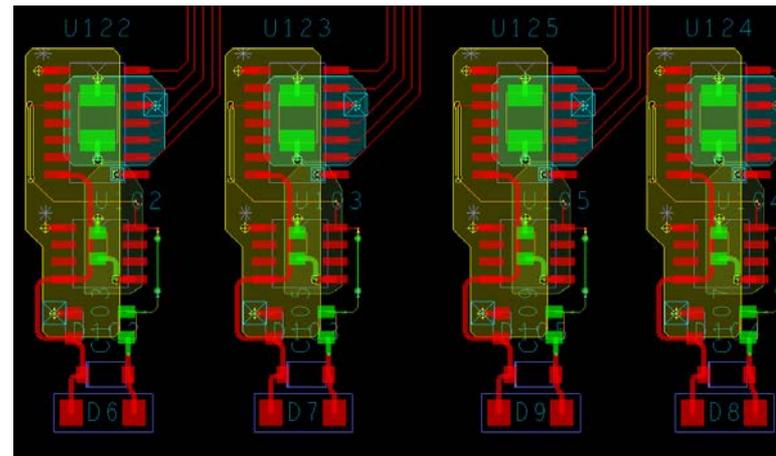
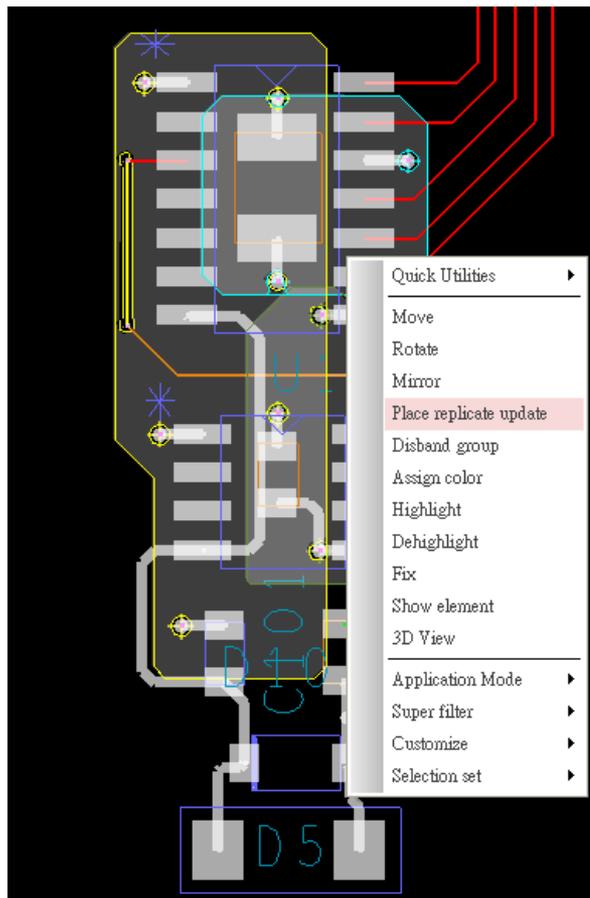


# OrCAD PCB / Placement



- Placement Replication

- Module 若有修改變更可透過 update 快速套用到其他模組



# OrCAD PCB / Routing



- Manual Route – Hug, Shove & Scribble Mode



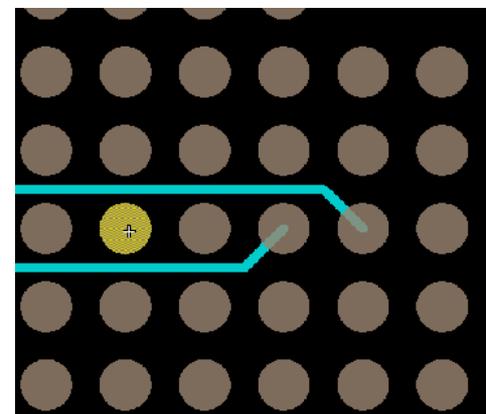
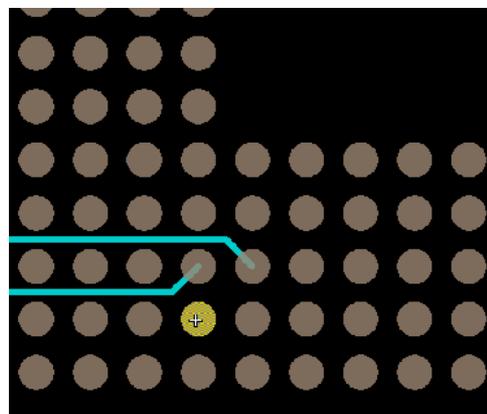
Hug



Hug preferred



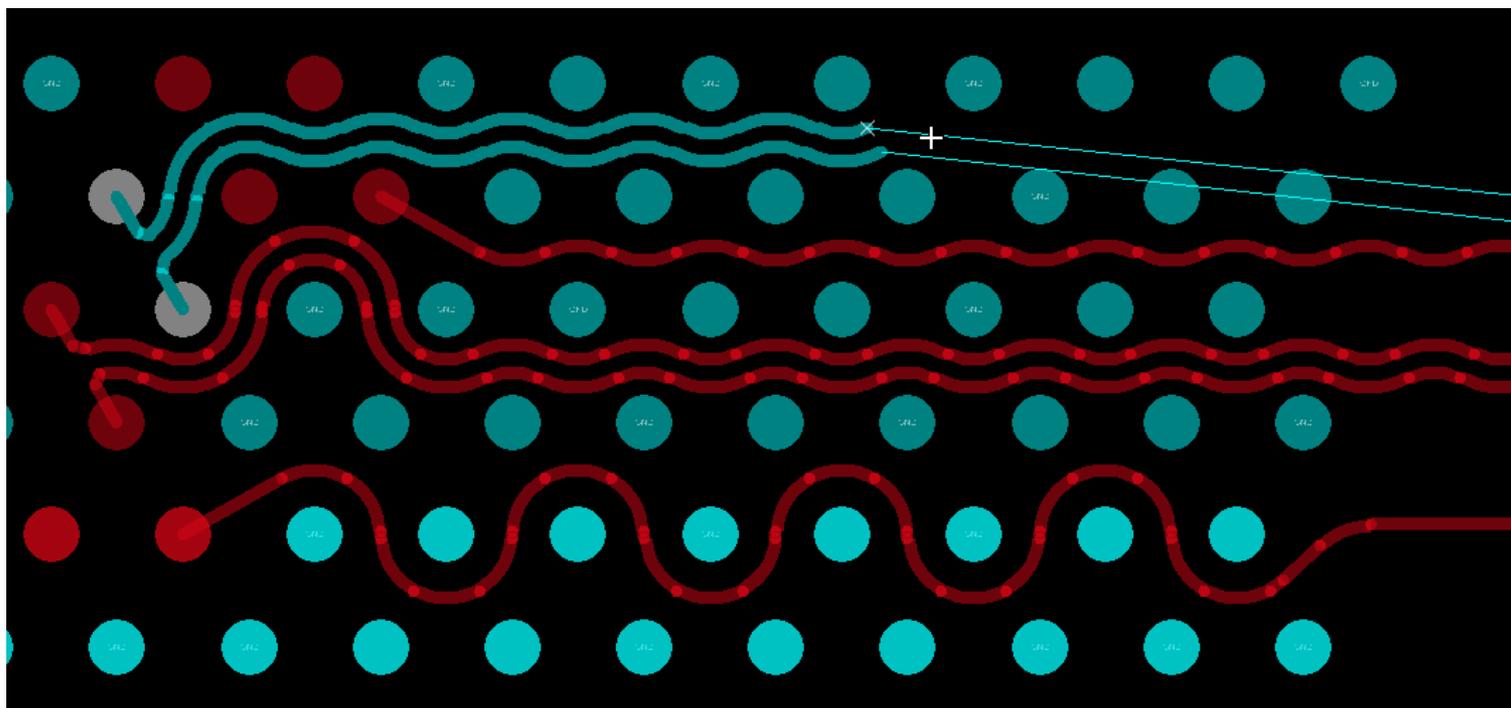
Shove preferred



Scribble Mode

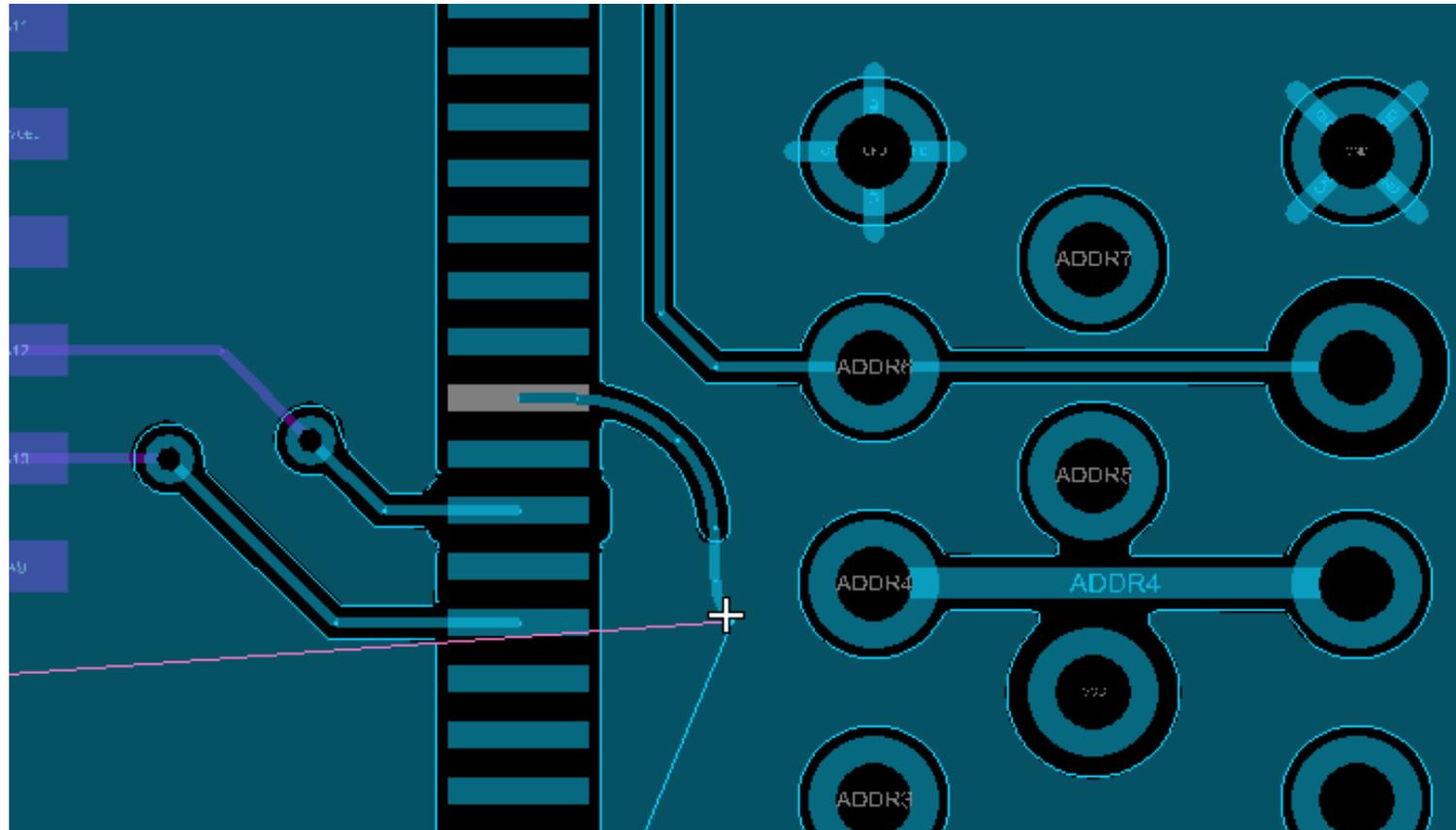
# OrCAD PCB / Routing

- Snake Route
  - 對於 BGA 內交錯的 Pad 排列方式，可透過蛇行走線模式快速 Breakout



# OrCAD PCB / Shape

- 智慧型鋪銅 – 動態避開和導接



# OrCAD PCB / Constraint Manager



- PCB Layout 設計規範定義

Object column

ECSet reference

Constraint values

Type	Objects	Referenced Electrical CSet	Pin Pairs	Pin Delay		Prop Delay			Prop Delay			
				Pin 1	Pin 2	Min	Actual	Margin	Max	Actual	Margin	
				mil	mil	mil			mil			
Bus	XPAK_PRTAD (5)											
Bus	XPAK_VEND (4)	PARALLEL4	All Drivers/All Receivers			500 mil	4361.23 ...	9853.9 mil	5000 mil	-5353.9 mil		
Net	XPAK_VEND<0>	PARALLEL4	All Drivers/All Receivers			500 mil	10353.9 MIL	9853.9 mil	5000 mil	-5353.9 mil		
PPr	U7.AJ28:R334.1											
Net	XPAK_VEND<1>	PARALLEL4	All Drivers/All Receivers			500 mil	4396.92 ...	4396.92 ...	5000 mil	103.08 mil		
PPr	U7.AF24:R335.1											
Net	XPAK_VEND<2>	PARALLEL4	All Drivers/All Receivers			500 mil	4896.92 MIL	4396.92 ...	5000 mil	4896.92 MIL	103.08 mil	
PPr	U7.AC22:R336.1											
Net	XPAK_VEND<3>	PARALLEL4	All Drivers/All Receivers			500 mil	4361.23 ...	4361.23 ...	5000 mil	4861.23 MIL	138.77 mil	
PPr	U7.AD22:R337.1											
DPr	BRIDGE_RXCLK_	UPREVED_DEF...	All Drivers/All Receivers			1000 mil	4948.11 MIL	4448.11 ...	5000 mil	4948.11 MIL	51.89 mil	
Net	BRIDGE_RXCLK_I	UPREVED_DEF...	All Drivers/All Receivers			1000 mil	7779.73 ...	7779.73 ...	8900 mil	7779.73 ...	120.27 mil	
PPr	U15.L6:U7.T32											
Net	BRIDGE_RXCLK_P	UPREVED_DEF...	All Drivers/All Receivers			1000 mil	8779.73 MIL	7779.73 ...	8900 mil	8779.73 MIL	120.27 mil	
PPr	U15.L7:U7.T31											
DPr	BRIDGE_RX_0											
Net	BRIDGE_RX_I<0>											
Net	BRIDGE_RX_P<0>											
DPr	BRIDGE_RX_1											
DPr	BRIDGE_RX_2											
DPr	BRIDGE_RX_3											
DPr	BRIDGE_RX_4											
DPr	BRIDGE_RX_5											
DPr	BRIDGE_RX_6											
DPr	BRIDGE_RX_7											
DPr	BRIDGE_RX_8											
DPr	BRIDGE_RX_9											
DPr	BRIDGE_RX_10											
DPr	BRIDGE_RX_11											
DPr	BRIDGE_RX_12											
DPr	BRIDGE_RX_13											

# OrCAD PCB / CM - Spacing



- 物件間之間距控制 (Line, Via, Shape, Pad, Hole...等)

The screenshot displays the Allegro Constraint Manager interface, showing various constraint sets and their parameters. The main table lists constraint sets for different object types and their associated spacing rules.

Objects	Referenced Spacing CSet	All mil	Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil	Test Via mil	Shape mil	Hole mil	Thru Pin To mil	SMD Pin To mil	Test Pin To mil	Thru Via To mil	BB Via To mil
Bsn	Delay	***	5.00	5.00	5.00	5.00	5.00	5.00	10.00	5.00	***	***	***	***	***	***
SCS	BGA	***	5.00	5.00	5.00	5.00	5.00	5.00	10.00	5.00	***	***	***	***	***	***
LTyp	Conductor	***	5.00	5.00	5.00	5.00	5.00	5.00	10.00	5.00	***	***	***	***	***	***

The PCB layout shows several DRC errors related to spacing constraints:

- DRC error "DiffPair Minimum Gap":** L3\_Sigx, Constraint value: 3.5 MIL, Actual value: 2.5 MIL
- DRC error "Line to Thru Via Spacing":** L3\_Sigx, Constraint value: 3.5 MIL, Actual value: 2.25 MIL

# OrCAD PCB / CM - Physical



- 實體走線之線寬控制及 Via List 設定

The image shows the Allegro Constraint Manager interface. The top window displays the 'Physical Constraint Set' for 'All Layers' with various parameters for Line Width, Neck, and Differential Pair. The bottom window shows the 'Edit Via List' dialog, which allows users to select vias from a library or database. The 'Via List' table includes columns for Name, Start, End, and various physical parameters.

Objects	Referenced Physical C Set	Line Width	Neck	Uncoupled Length	Static Phase Tolerance	Differential Pair						
Type	Name	Min mil	Max mil	Min Width mil	Max Length mil	Gather Control	Max mil	Min Line Spaci mil	Primary gap mil	Neck Gap mil	(+)Tolerance mil	(-)Tolerance mil
Bsn	uvia_stacking	5.00	0.00	0.00	0.00			0.00	0.00	0.00	0.00	0.00
OTyp	Net Classes											
NCls	DP_CLASS_PS (12)	5.00	0.00	0.00	0.00			0.00	0.00	0.00	0.00	0.00
	DP_DR	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_DR1	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_NEX1	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_BIT1	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_NECK1	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_REG1	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_1	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_2	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_3	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_4	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_5	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10
	DP_6	6.00	0.00	3.40	1000.00	Ignore	300.00	5 mil	3.80	6.00	3.90	0.10

The 'Edit Via List' dialog shows a list of vias with columns for Name, Start, and End. The 'Filter' section includes options to show vias from the library or database. The 'Filter by name' field is empty. The 'Add' button is highlighted.

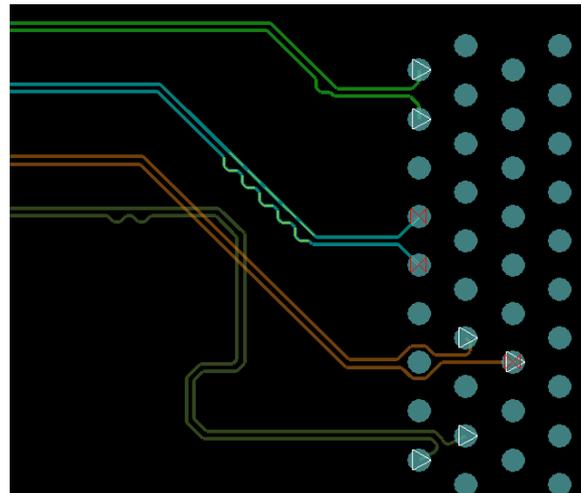
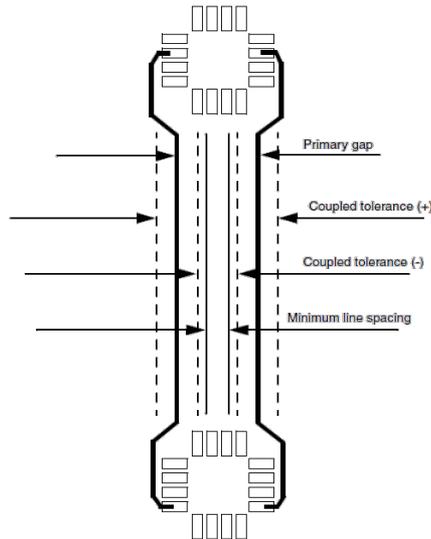
The bottom right image shows a PCB layout with a via and a constraint error message: "DRC error 'Minimum Neck Width' L3\_Sixp Constraint value: 3.5 MIL Actual value: 3 MIL". The error is highlighted with a red box and a white text box.

# OrCAD PCB / CM - Differential Pair



- 差動訊號線控制

Gather Control	Uncoupled Length				Static Phase			Min Line Spacing mil	Coupling Parameters					
	Length Ignored mil	Max mil	Actual mil	Margin	Tolerance mil	Actual	Margin		Prim. Gap mil	Prim. Width mil	Neck Gap mil	Neck Width mil	(+)Tol.	(-)Tol.
													mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*	*	
							-60.71	0.00	0.00	5.00	0.00	0.00	0.00	0.00
Ignore		300.00			5 mil		-60.71	0.00	0.00	5.00	0.00	0.00	0.00	0.00
Ignore		300.00			5 mil		-36.98	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-5.220	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-40.32	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil			3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-22.16	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-12.36	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-60.71	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-12.51	3.80	6.00	6.00	3.90	3.40	0.10	0.10



# OrCAD PCB / CM

## - Min/Max Propagation Delay

- 點對點 (Pin pair) 的長度控制

The screenshot displays the OrCAD PCB Editor interface with the 'Min/Max Propagation Delays' constraint set. The 'cdn\_design1match\_routed' constraint is selected, showing a list of objects and their associated pin pairs, minimum, and maximum propagation delays.

Type	Objects	Pin Pairs	Min Delay	Max Delay
Dsn	cdn_design1match_routed			
ECS	DGP			
ECS	DP_75			
ECS	DP_90			
ECS	LAMP_BUS			
ECSP	NET.T.1:U23.9		500 mil	1500 mil
ECSP	NET.T.1:U24.9		500 mil	1500 mil
ECSP	NET.T.2:U39.9		500 mil	1500 mil
ECSP	NET.T.2:U52.9		500 mil	1500 mil
ECSP	U20.31:NET.T.1		8000 mil	11000 mil
ECSP	U20.31:NET.T.2		8000 mil	11000 mil

Min	Prop Delay			Max	Prop Delay		
	Actual	Margin	Actual		Margin		
0 mil	-420.5 MIL		275.36 MIL				
0 MIL			633.5 MIL				
500.00 MIL	851.49 MIL	351.49 MIL	1500.00 MIL	851.49 MIL	648.51 MIL		
500.00 MIL	500.01 MIL	0.01 MIL	1500.00 MIL	500.01 MIL	999.99 MIL		
500.00 MIL	866.50 MIL	366.5 MIL	1500.00 MIL	866.50 MIL	633.5 MIL		
500.00 MIL	0 MIL	0 MIL	1500.00 MIL	500.00 MIL	1000 MIL		
8000.00 MIL	9152.45 MIL	1152.45 ...	11000.00 MIL	9152.45 MIL	1847.55 MIL		
8000.00 MIL	9432.44 MIL	1432.44 ...	11000.00 MIL	9432.44 MIL	1567.56 MIL		
0 MIL				662 MIL			
500.00 MIL	824.49 MIL	324.49 MIL	1500.00 MIL	824.49 MIL	675.51 MIL		
500.00 MIL	500.01 MIL	0.01 MIL	1500.00 MIL	500.01 MIL	999.99 MIL		
500.00 MIL	838.00 MIL	338 MIL	1500.00 MIL	838.00 MIL	662 MIL		
500.00 MIL	500.00 MIL	0 MIL	1500.00 MIL	500.00 MIL	1000 MIL		
8000.00 MIL	9647.18 MIL	1647.18 ...	11000.00 MIL	9647.18 MIL	1352.82 MIL		
8000.00 MIL	9632.65 MIL	1632.65 ...	11000.00 MIL	9632.65 MIL	1367.35 MIL		

The bottom right shows a PCB layout with a DRC error callout: "DRC error 'Propagation Delay' All Constraint value: 60 mil; 6500 mil; 7000 mil. Actual value: 6435.29 MIL".

# OrCAD PCB / CM

## - Relative Propagation Delay

- 群組等長控制 (BUS 等長)

The screenshot displays the OrCAD PCB Editor interface for a Relative Propagation Delay analysis. The 'Worksheet selector' on the left shows the 'Electrical' constraint set, with 'Relative Propagation Delay' selected. The central table, titled 'cdn\_design1match\_routed', lists various constraint types and objects, including 'LAMP\_BUS\_M1 (2)' with a Delta/Tolerance of 1000 mil. The right-hand table provides a detailed view of the 'Relative Delay' for various objects, including 'BRIDGE\_RX\_MATCH (32)', 'LAMP\_BUS\_M1 (16)', and 'XCVR\_RX\_MATCH (40)'. The table columns include Objects, Pin Pairs, Scope, Delta/Tolerance, Actual, Margin, Length, and Delay. A DRC error dialog is overlaid on the PCB layout, indicating a 'Relative Propagation Delay' error with a constraint value of 400 mil and an actual value of 538.02 mil.

Objects	Pin Pairs	Scope	Delta/Tolerance mil	Relative Delay			Length mil	Delay ns
				Actual	Margin	+/-		
cdn_design1match_routed				0 MIL				
BRIDGE_RX_MATCH (32)	All Drivers/All Receive...	Global	:500.00 MIL	29.47 MIL				
LAMP_BUS_M1 (16)				0 MIL				
U20.31:LAMP7.T.1 [LAMP7]		Local	:1000.00 MIL	1000.00 MIL	0 MIL		9724.64	1.783
U20.31:LAMP7.T.2 [LAMP7]		Local	:1000.00 MIL	1000.00 MIL	0 MIL		10724.64	1.967
U20.32:LAMP6.T.1 [LAMP6]		Local	:1000.00 MIL	379.01 MIL	620.99 MIL		10476.74	1.917
U20.32:LAMP6.T.2 [LAMP6]		Local	:1000.00 MIL	379.01 MIL	620.99 MIL		10097.73	1.847
U20.33:LAMP5.T.1 [LAMP5]		Local	:1000.00 MIL	97.99 MIL	902.01 MIL		9609.40	1.760
U20.33:LAMP5.T.2 [LAMP5]		Local	:1000.00 MIL	97.99 MIL	902.01 MIL		9511.41	1.742
U20.34:LAMP4.T.1 [LAMP4]		Local	:1000.00 MIL	224.01 MIL	775.99 MIL		9552.31	1.749
U20.34:LAMP4.T.2 [LAMP4]		Local	:1000.00 MIL	224.01 MIL	775.99 MIL		9328.30	1.708
U20.35:LAMP3.T.1 [LAMP3]		Local	:1000.00 MIL	737.00 MIL	263 MIL		9955.78	1.767
U20.35:LAMP3.T.2 [LAMP3]		Local	:1000.00 MIL	737.00 MIL	263 MIL		10692.78	1.952
U20.36:LAMP2.T.1 [LAMP2]		Local	:1000.00 MIL	521.49 MIL	478.51 MIL		9196.54	1.684
U20.36:LAMP2.T.2 [LAMP2]		Local	:1000.00 MIL	521.49 MIL	478.51 MIL		9717.03	1.779
U20.37:LAMP1.T.1 [LAMP1]		Local	:1000.00 MIL	14.53 MIL	985.47 MIL		9647.18	1.765
U20.37:LAMP1.T.2 [LAMP1]		Local	:1000.00 MIL	14.53 MIL	985.47 MIL		9632.65	1.762
U20.38:LAMP0.T.1 [LAMP0]		Local	:1000.00 MIL	279.99 MIL	720.01 MIL		9152.45	1.677
U20.38:LAMP0.T.2 [LAMP0]		Local	:1000.00 MIL	279.99 MIL	720.01 MIL		9432.44	1.728
XCVR_RX_MATCH (40)	All Drivers/All Receive...	Global	:300.00 MIL	6.47 MIL				
XCVR_RX_N<0>	All Drivers/All Receivers	Global	:300.00 MIL	15.99 MIL				
XCVR_RX_N<1>	All Drivers/All Receivers	Global	:300.00 MIL	104.54 MIL				
XCVR_RX_N<2>	All Drivers/All Receivers	Global	:300.00 MIL	6.5 MIL				
XCVR_RX_N<3>	All Drivers/All Receivers	Global	:300.00 MIL	34.89 MIL				
XCVR_RX_N<4>	All Drivers/All Receivers	Global	:300.00 MIL	6.47 MIL				
XCVR_RX_N<5>	All Drivers/All Receivers	Global	:300.00 MIL	8.23 MIL				
XCVR_RX_N<6>	All Drivers/All Receivers	Global	:300.00 MIL	7.76 MIL				
XCVR_RX_N<7>	All Drivers/All Receivers	Global	:300.00 MIL	47.71 MIL				
XCVR_RX_N<8>	All Drivers/All Receivers	Global	:300.00 MIL	109.11 MIL				
XCVR_RX_N<9>	All Drivers/All Receivers	Global	:300.00 MIL	36.13 MIL				
XCVR_RX_N<10>	All Drivers/All Receivers	Global	:300.00 MIL	67.15 MIL				
XCVR_RX_N<11>	All Drivers/All Receivers	Global	:300.00 MIL	126.24 MIL				

# Support XNet



- eXtend Net

The screenshot displays the OrCAD PCB Designer interface. The main workspace shows a PCB layout with two ICs, U100 and U101, connected via a resistor component RN1. Yellow arrows labeled 'Net A' and 'Net B' indicate the signal paths. A red arrow labeled 'XNet A' spans the entire connection path between the two ICs. Below the PCB layout, a schematic diagram shows the electrical model of the connection, including the resistor RN1 and two transmission line components (TL1 and TL2) with propagation delays of 0.2588212 ns and 0.0495409 ns respectively. To the right, the Allegro Constraint Manager is open, showing a table of constraints for the project 'cde\_routed\_Rat\_XNET\_172'.

Objects	Pin Pairs	Scope	Delta: Tolerance
Dsn			
OType			
MGrp			
PPr			
OType			
OType			
XNet			
PPr			
Net			
XNet			
PPr			
Net			

# Segments Over Voids

- SOV 檢查能將訊號走線與相鄰電源層間跨 Moat 的問題找出來

The screenshot shows the OrCAD PCB Editor interface. The 'Display' menu is open, and the 'Segments Over Voids' option is highlighted. The main workspace displays a PCB layout with green signal traces and white circular voids. Two red arrows point to specific signal segments that overlap with the voids. A 'View of file: highlight\_Lsovlog' window is open in the bottom right, displaying a list of violations.

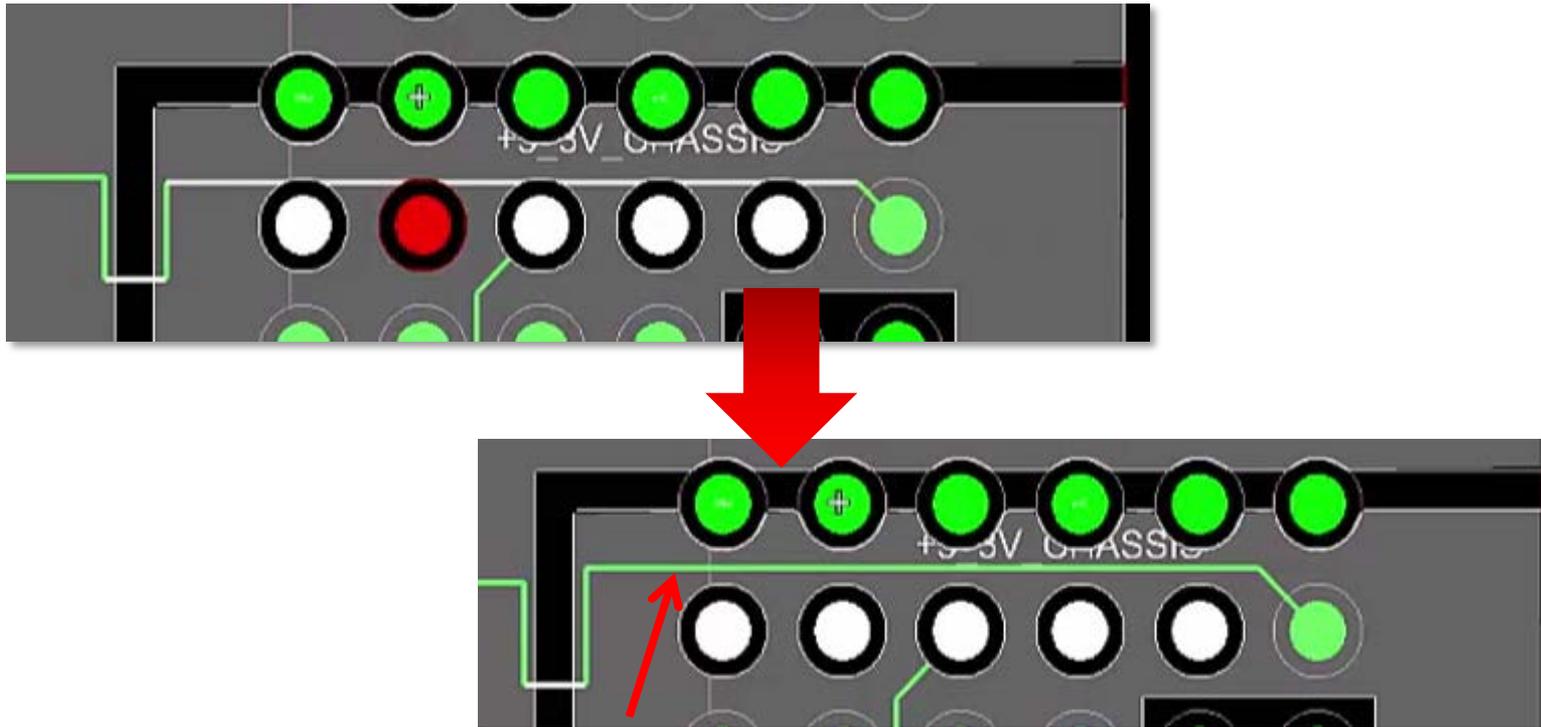
Layer	Location	Net Name
SIG_2V	12292.10 1222.291	H_PCL_INTA_L
SIG_2V	12511.72 1124.861	H_PCL_RST_L
SIG_2V	12432.04 924.261	H_PCL_RST_L
SIG_2V	12652.02 1222.291	H_PCL_REQ_L
SIG_2V	12444.62 1214.051	H_PCL_REQ_L
SIG_2V	12671.62 755.021	H_PCL_REQ_L
SIG_2V	12578.52 1159.021	H_PCL_REQ_L
SIG_2V	12521.62 1437.321	H_PCL_AD<15>
SIG_2V	12521.62 1437.321	H_PCL_AD<15>
SIG_2V	12572.72 1116.021	H_PCL_AD<15>
SIG_2V	12432.04 1437.321	H_PCL_AD<15>
SIG_2V	12622.02 1419.521	H_PCL_AD<15>
SIG_2V	12511.72 1124.861	H_PCL_REQ_L
SIG_2V	12432.04 1113.221	H_PCL_REQ_L
SIG_2V	12567.32 117.421	H_PCL_INTA_L
SIG_2V	12712.02 1238.521	H_PCL_CLK
SIG_2V	12731.22 1122.291	H_PCL_CLK
SIG_2V	12737.62 1134.021	H_PCL_CLK
SIG_2V	12737.62 1264.021	H_PCL_CLK
SIG_2V	12737.62 1214.021	H_PCL_CLK
SIG_2V	12644.02 6779.521	I_LED_RST_L
BO7T04		

Layer	Location	Net Name
SIG_4V	12537.62 6719.521	I_LED_RST_L
SIG_4V	12527.02 6762.521	I_LED_D<2>
SIG_4V	12537.62 6229.521	I_LED_D<1>
SIG_2V	12222.02 1113.021	H_PCL_INTA_L
SIG_2V	12227.62 1113.021	H_PCL_INTA_L
SIG_2V	12671.62 125.261	UNNAMED_12_CPC110000_112_020

# Segments Over Voids

- SOV 檢查能將訊號走線與相鄰電源層間跨 Moat 的問題找出來

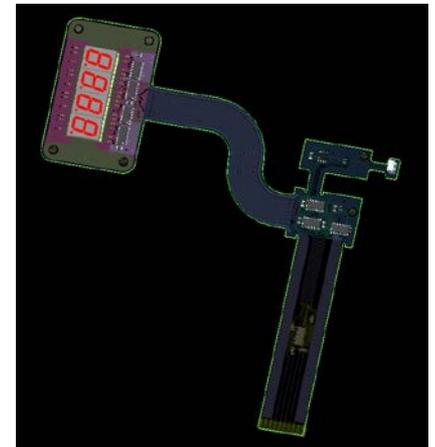
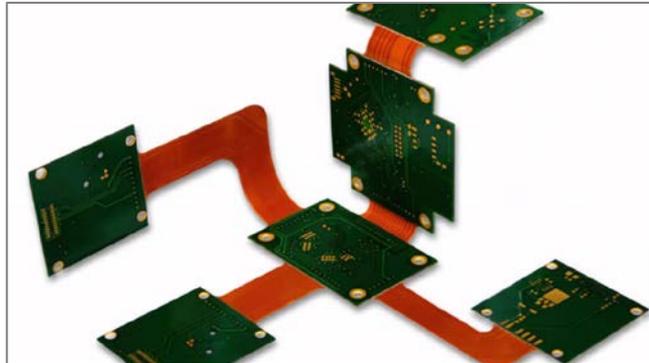
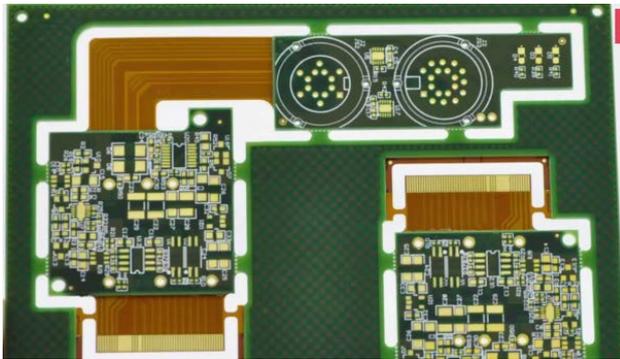


# Flex and Rigid Flex Technologies



- 支援軟板、軟硬結合板設計應用

- 對應不同板材間的板層疊構可清楚定義並輕鬆劃分區域
- 藉由 Inter-layer checks (ILC) 來進行相關的檢查設定
- 方便的 Contour 及 Arc-aware 佈線指令



# Flex and Rigid Flex Technologies

- Layer Setting
  - 支援多重疊構設定 PCB 板層架構

The screenshot displays the OrCAD PCB Editor interface with the Cross Section Editor (Multi Stackups mode) open. The main window shows a table of layer properties for a PCB design. The table includes columns for Name, Layer, Types, Thickness (mil), Material, Primary, Flex-1, Flex-2, and Flex-3. The layers are listed from TOP to BOTTOM, including STIFFENER\_FLEX\_1, TIN\_PLATE\_TOP, ADHESIVE\_STIFFENER\_FLEX\_1, COVERLAY\_FLEX\_1, ADHESIVE\_FLEX\_1, PASTEMASK\_FLEX\_1, GOLD\_SOFT\_FLEX\_1, PASTEMASK\_TOP, SOLDERMASK\_TOP, SOLDERMASK\_INT1, PASTEMASK\_INT1, TOP, INT\_1, FLEX\_1, FLEX\_2, INT\_4, BOTTOM, PASTEMASK\_BOTTOM, SOLDERMASK\_BOTTOM, and PASTEMASK\_INT\_4.

The Cross Section Editor (Multi Stackups mode) window is also visible, showing a 3D cross-section of the PCB layers. The stackup is detailed in the following table:

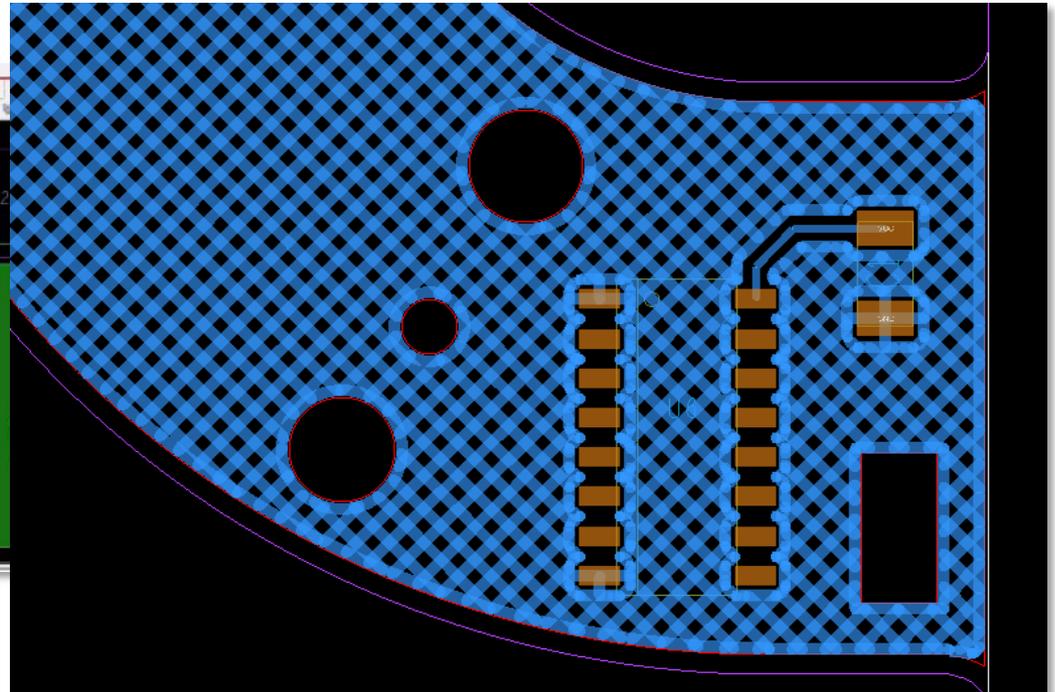
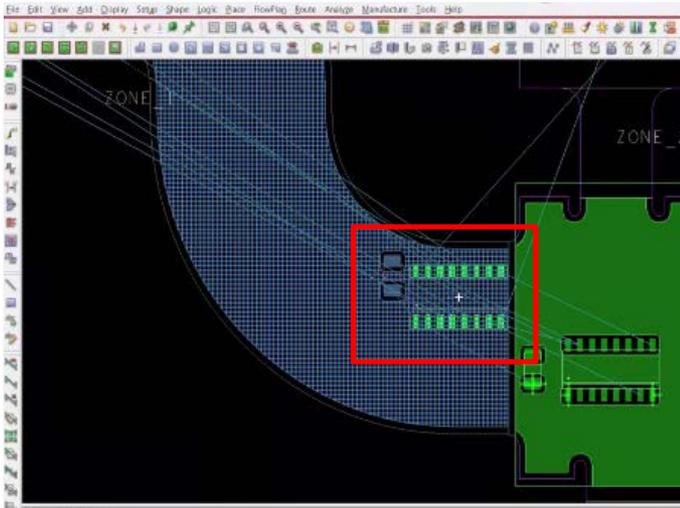
#	Name	Layer	Layer Function	Manufacture	Constraint	Value	Layer
1	TIN_PLATE_TOP	Surface	Coating Conductive			0.5	
2	PASTEMASK_TOP	Mask	Solder Paste			3	
3	SOLDERMASK_TOP	Mask	Solder Mask	0.590551		1	
4	TOP	Conductor	Conductor			1.2	1
5	INT_1	Conductor	Dielectric			1.2	2
6	FLEX_1	Dielectric	Dielectric Adhesive			5	
7	FLEX_2	Conductor	Dielectric Base			1.2	3
8	FLEX_2	Conductor	Dielectric Core			1.2	4
9	INT_4	Dielectric	Dielectric Prepreg			5	
10	INT_4	Conductor	Conductor			1.2	5
11	INT_4	Dielectric	Dielectric			8	
12	BOTTOM	Conductor	Conductor			1.2	6
13	PASTEMASK_BOTTOM	Mask	Solder Paste			3	
14	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.590551		1	
15	SURFACE	Surface					

The interface also shows a 3D cross-section view of the PCB layers, with a legend on the right side. The legend lists the layers and their corresponding colors: Surface (green), TIN\_PLATE\_TOP Mask (orange), PASTEMASK\_TOP Mask (red), SOLDERMASK\_TOP Mask (yellow), TOP Conductor (blue), Dielectric (purple), INT\_1 Conductor (brown), Dielectric (purple), FLEX\_1 Conductor (blue), Dielectric (purple), FLEX\_2 Conductor (blue), Dielectric (purple), INT\_4 Conductor (blue), Dielectric (purple), BOTTOM Conductor (blue), PASTEMASK\_BOTTOM Mask (red), SOLDERMASK\_BOTTOM Mask (yellow), and Surface (green).

# Flex and Rigid Flex Technologies

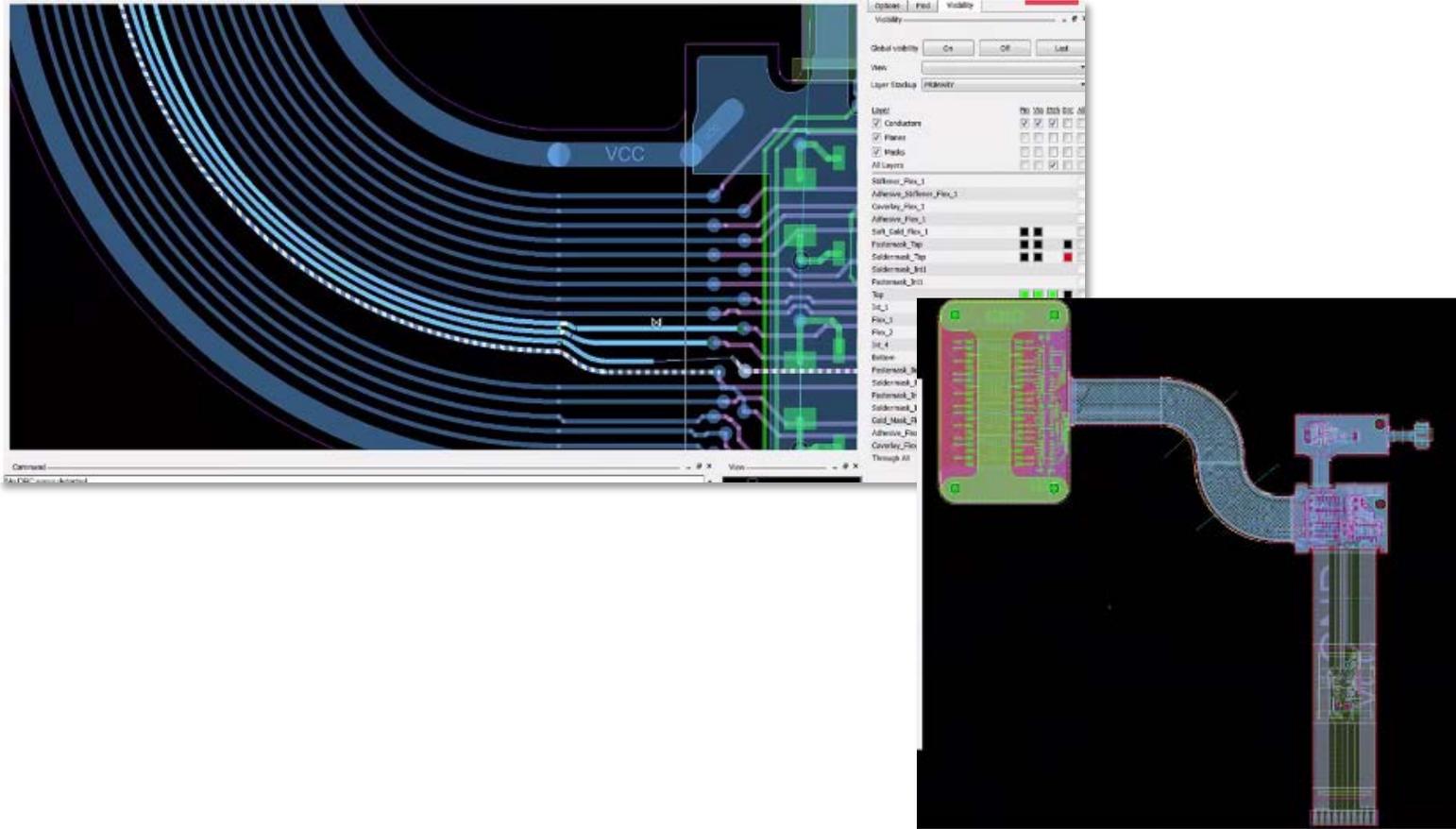


- Component place on Rigid Flex
  - 擺放零件可依板層關係自動切換擺放層面
- Dynamic Xhatch
  - 動態鋪銅支援網狀型態，即時的導接與隔離可減少編輯動作



# Flex and Rigid Flex Technologies

- Routing on Rigid Flex
  - 對應特殊弧度之軟板，可透過 Arc 及 Contour 指令完成佈線工作

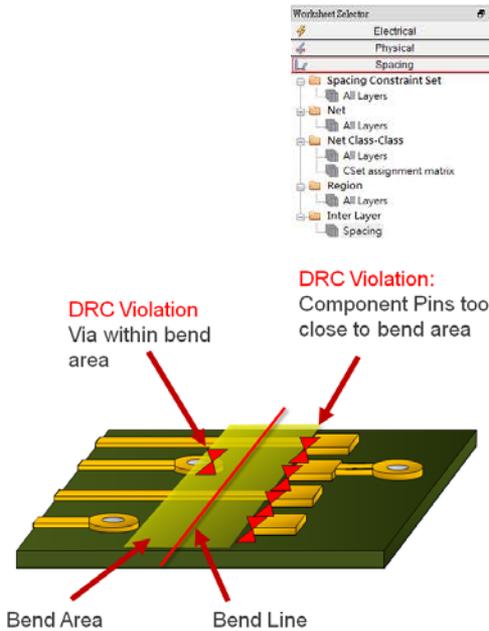


# Flex and Rigid Flex Technologies



- Inter Layer Checks (ILC)

- 層面與層面間的檢查

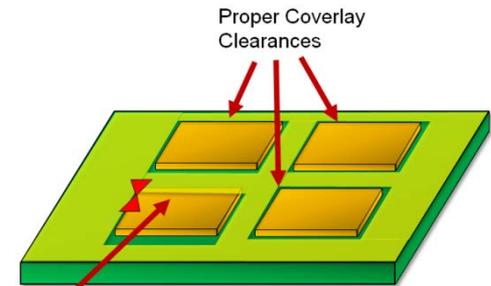
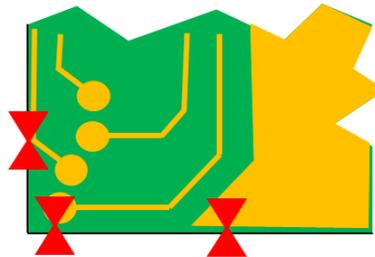


Worksheet Selector

Layer 1: Geometries, Layer 1 Filter

Layer 2: Geometries, Layer 2 Filter

Layer 1	Layer 2	Type	Value	Enabled	DRC label	DRC subclass	Description	Delete
Transition_Zone	Tin_Plate_Bottom	Overlap	25.000	✓	O	INTER_LAYER	Prevent Tin Plate Peeling	✗
Adhesive_Stiffener_Flex_1	Stiffener_Flex_1	1 inside 2	45.000	✓	A	INTER_LAYER	Adhesive compression spacing to prevent excessive leakage	✗
Via (and Pin)/FLEX_1	Transition_Zone	Gap	12.000	✓	t	FLEX_1	Via and pin to transition area to prevent cracking and splitting of holes and flex	✗
Etch_Int_1	Design_Outline	1 inside 2	45.000	✓	B	INT_1	Copper to Design Edge Clearance	✗
Bend_Area	Transition_Zone	Overlap	15.000	✓	O	INTER_LAYER	Proper transition area clearance	✗
Coverlay_Flex_2	Gold_Hard_Flex_2	1 inside 1	15.000	✓	G	INTER_LAYER	Ensure Proper Gold Plating	✗
Gold_Soft_Flex_1	Coverlay_Flex_1	1 inside 2	0.000	✓	M	INTER_LAYER	Ensure Proper Gold Plating	✗
Bend_Area	Stiffener_Flex_1	Gap	20.000	✓	S	INTER_LAYER	Prevent Stiffener Peel and Bend interference	✗



# Flex and Rigid Flex Technologies

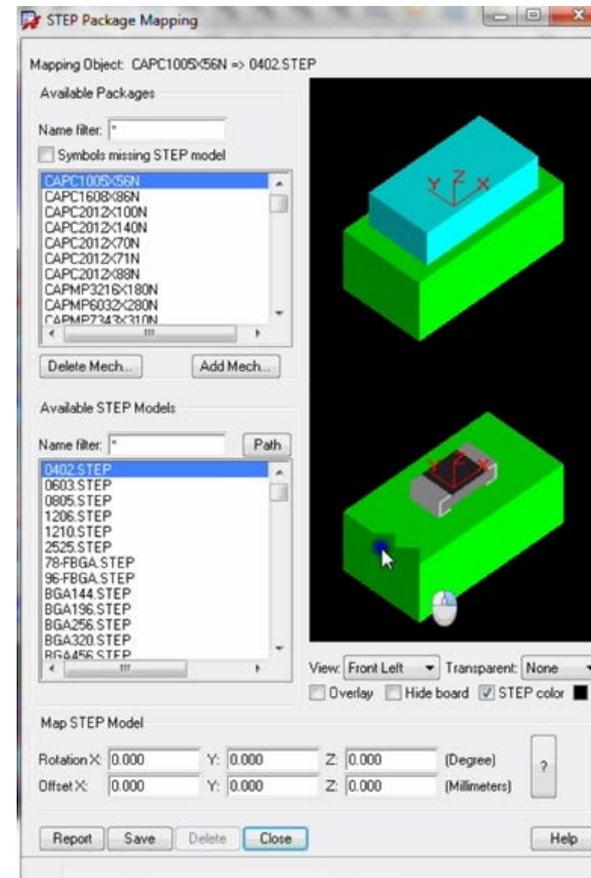
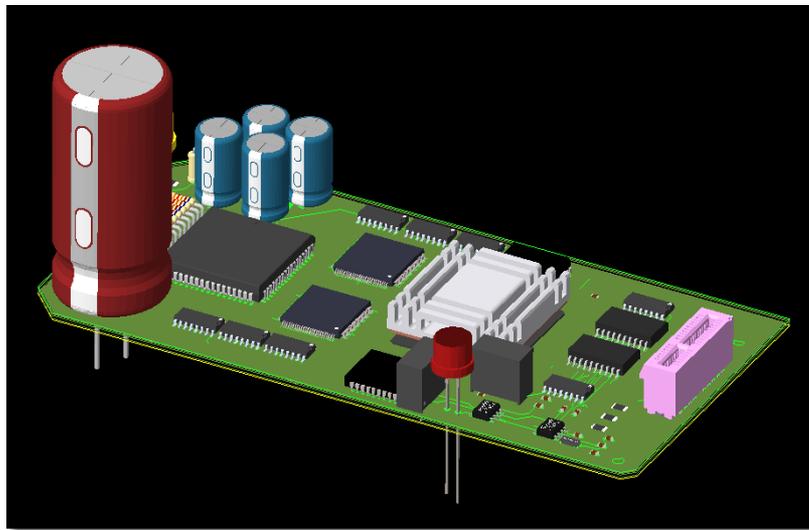


- Multiple Stackup Table
  - 輸出相關的工程資料

MULTIPLE STACKUP TABLE								
Unit : mils								
#	NAME	TYPE	MATERIAL	TOLERANCE	FLEX1	FLEX2	PRIMARY	FLEX3
		SURFACE	AIR	+0/-0	0.000	0.000	0.000	0.000
	STIFFENER TOP	MASK	FR-4	+0/-0		2.000		
	COVERLAY TOP	MASK	POLYIMIDE FILM 1MIL	+0/-0	2.000	2.000		2.000
	ADHESIVE TOP	MASK	ADHESIVE ACRYLIC	+0/-0	0.500	0.500		0.500
	SOLDERMASK TOP	MASK	SOLDERMASK	+0/-0			2.000	
1	TOP	CONDUCTOR	COPPER	+0/-0			1.200	
		DIELECTRIC	FR-4	+0/-0			8.000	
2	INT 1	CONDUCTOR	COPPER	+0/-0			1.200	
		DIELECTRIC	POLYIMIDE RIGID 5MIL	+0/-0			5.000	
3	FLEX 1	CONDUCTOR	COPPER	+0/-0	1.200	1.200	1.200	1.200
		DIELECTRIC	POLYIMIDE FILM	+0/-0	3.000	3.000	3.000	3.000
4	FLEX 2	CONDUCTOR	COPPER	+0/-0	1.200	1.200	1.200	1.200
		DIELECTRIC	POLYIMIDE RIGID 5MIL	+0/-0			5.000	
5	INT 4	CONDUCTOR	COPPER	+0/-0			1.200	
		DIELECTRIC	FR-4	+0/-0			8.000	
6	BOTTOM	CONDUCTOR	COPPER	+0/-0			1.200	
	SOLDERMASK BOTTOM	MASK	SOLDERMASK	+0/-0	2.000	2.000	2.000	2.000
	ADHESIVE BOTTOM	MASK	ADHESIVE ACRYLIC	+0/-0	0.500	0.500		0.500
	COVERLAY BOTTOM	MASK	POLYIMIDE FILM 1MIL	+0/-0	2.000	2.000		2.000
	GOLD SOFT BOTTOM	MASK	GOLD	+0/-0				1.000
		SURFACE	AIR	+0/-0	0.000	0.000	0.000	0.000
TOTAL THICKNESS					12.400	14.400	40.200	13.400
ZONE NAME					ZONE_1	ZONE_3		ZONE_4
					ZONE_2			

# STEP Support - Mapping 3D Models

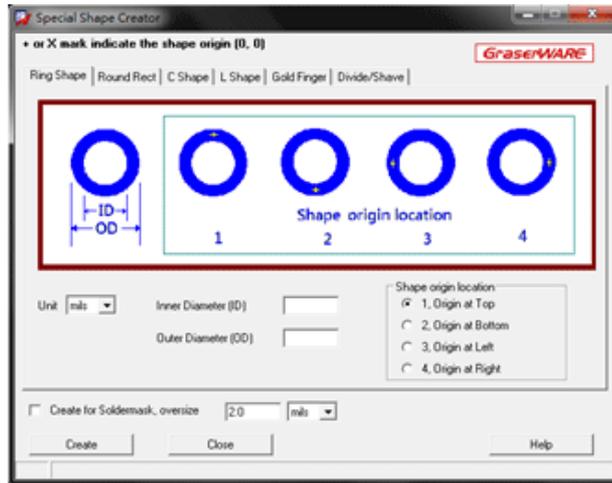
- 支援 3D STEP Model 掛載，能讓零件外觀更趨近於真實樣貌



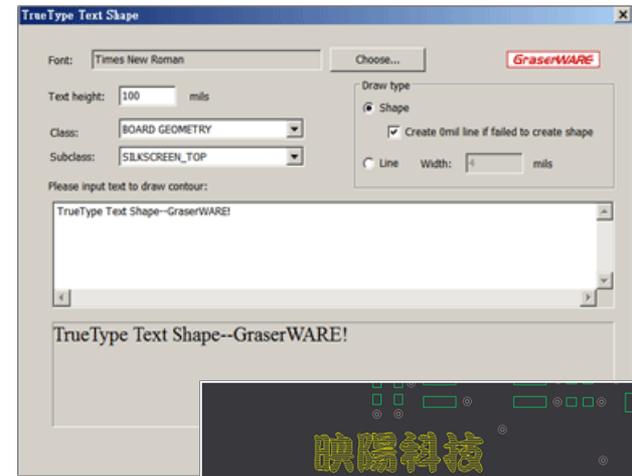
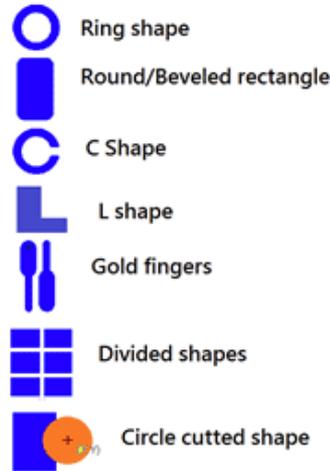
# GraserWARE EnhancePack

# GraserWARE EnhancePack

- 針對 PCB 設計工程師設計佈線時的需求，應用在 Cadence<sup>®</sup> Allegro<sup>®</sup> / OrCAD<sup>®</sup> PCB 程式上，主要含括整個 PCB Layout 流程的前、中、後三階段



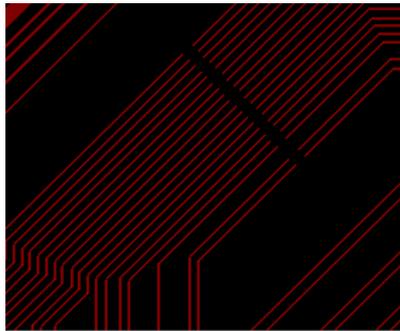
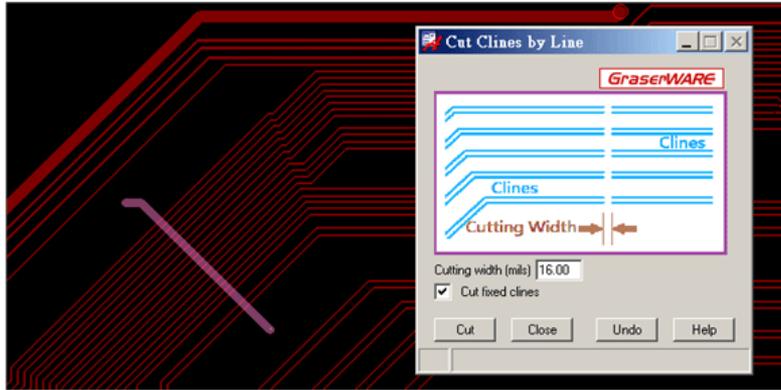
Create Special Pad Shape



TrueType Text Shape



# GraserWARE EnhancePack



Cline Cut

**Pin Pair Length Report**

	A	B	C	D
1	<b>Pin Pair Length Report</b>			
2				
3	Board name	tms799		
4	Date	Apr 11 10:31:32 2013		
5	Design unit	Mils		
6				
7	Net	Pin pair		Length
8	MDA18	J6.27 - Via1 - CPU1.AV5		1961.66
9				
10	Net	Pin pair		Length
11	MDA19	J6.28 - Via1 - CPU1.AW5		1927.02
12				
13	Net	Pin pair		Length
14	MDA20	J6.140 - Via1 - CPU1.AU2		1884.36

**Cline Segment Length Report**

	A	B	C	D	E	F
1	<b>Cline Segment Length Report</b>					
2						
3	Board name	tms799				
4	Date	Apr 11 10:31:32 2013				
5	Design unit	Mils				
6						
7	Net	From	To	Layer	Length	(width length)
8	MDA18	CPU1.AV5	Via1	TOP	193.02	(4.00 193.02)
9	MDA18	J6.27	Via1	BOTTOM	1768.64	(7.00 1768.64)
10				Summary	1961.66	(7.00 1768.64)(4.00 193.02)
11						
12	Net	From	To	Layer	Length	(width length)
13	MDA19	CPU1.AW5	Via1	TOP	125.4	(4.00 125.40)
14	MDA19	J6.28	Via1	BOTTOM	1801.82	(7.00 1801.82)
15				Summary	1927.02	(7.00 1801.82)(4.00 125.40)
16						

Pin/Pin Length Report