

OrCAD^x AutoCAD

電路與機構零距離
2016 SPB SEMINAR TAINAN



全面強化電路設計與模擬驗證

Addi Lin / Graser
2 / Sep / 2016

Agenda

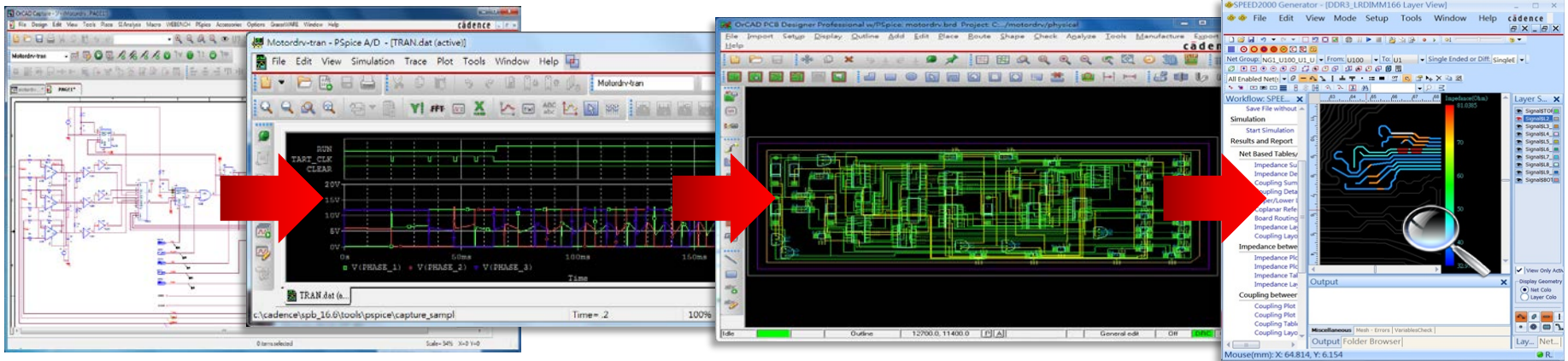


- OrCAD Design Solution
- OrCAD Capture 功能應用
- OrCAD Capture CIS 介紹
- OrCAD PSpice 模擬與驗證

OrCAD Design Solution



- Powerful and Widely Used Design Solution
 - Front-to-Back Integration
 - Fast and intuitive schematic design entry, OrCAD® Capture
 - Mixed-signal simulator, OrCAD® PSpice®
 - Comprehensive PCB solution, OrCAD® PCB Designer
 - Signal integrity electrical checks, OrCAD® Sigrity™ ERC



Schematic
OrCAD Capture

Simulation
OrCAD PSpice

Layout
OrCAD PCB Designer

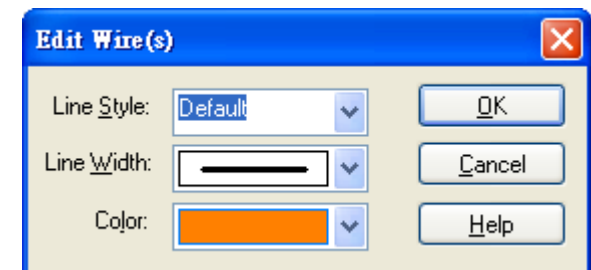
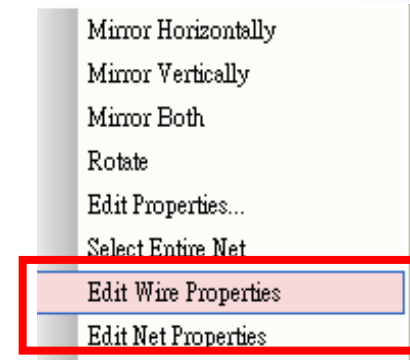
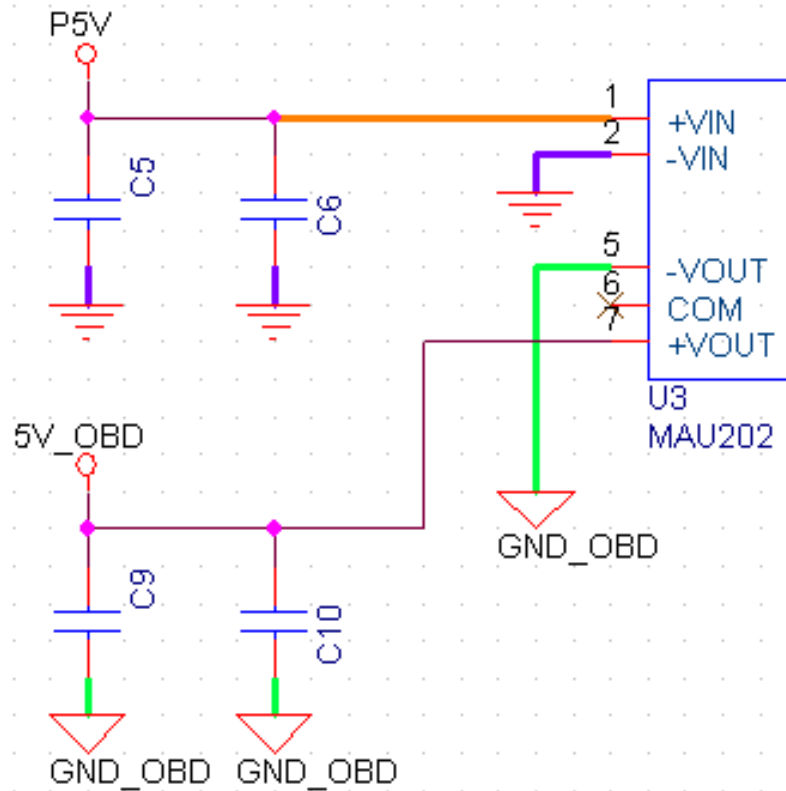
Signal integrity electrical checks
OrCAD Sigrity ERC

OrCAD Capture / CIS V17.2 - 2016 Release



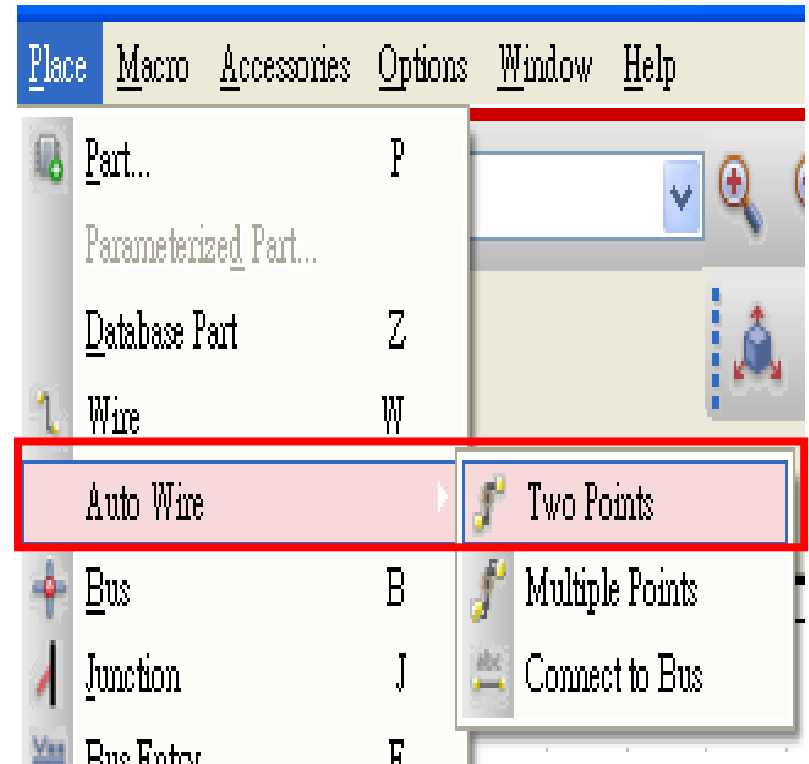
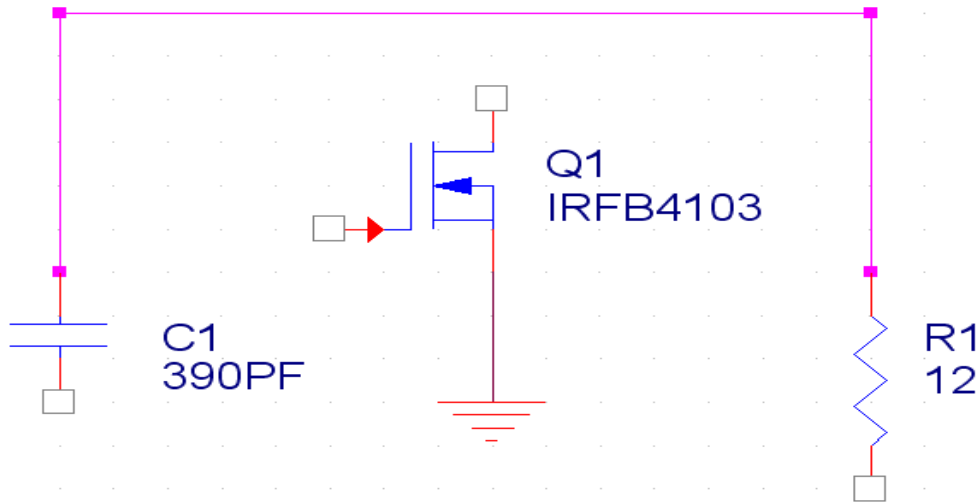
- Color Wire
- Auto Wire
- Advanced Annotate
- Design Difference Viewer
- Demo Design
- Export PDF
- OrCAD® Marketplace Support

Color Wire



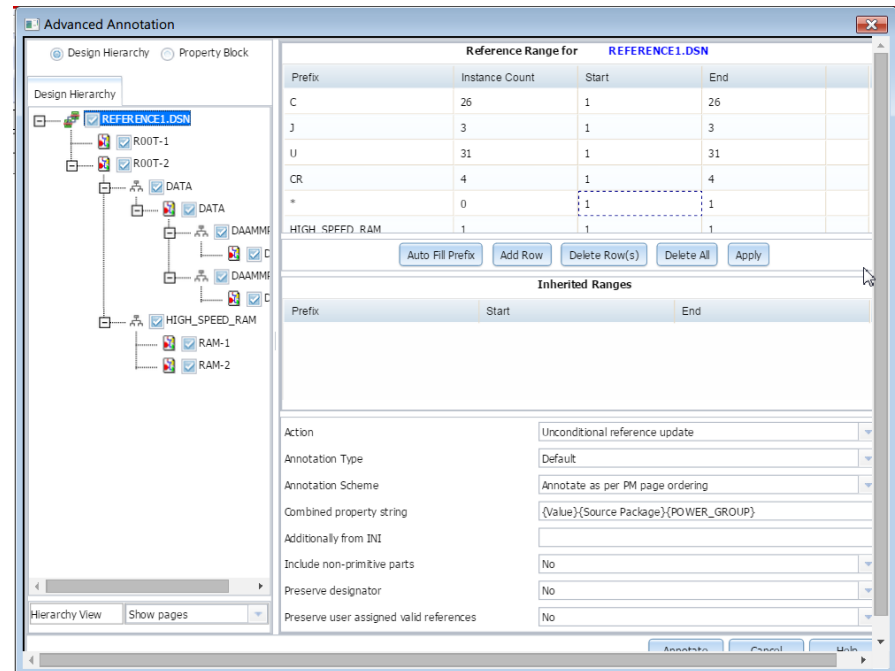
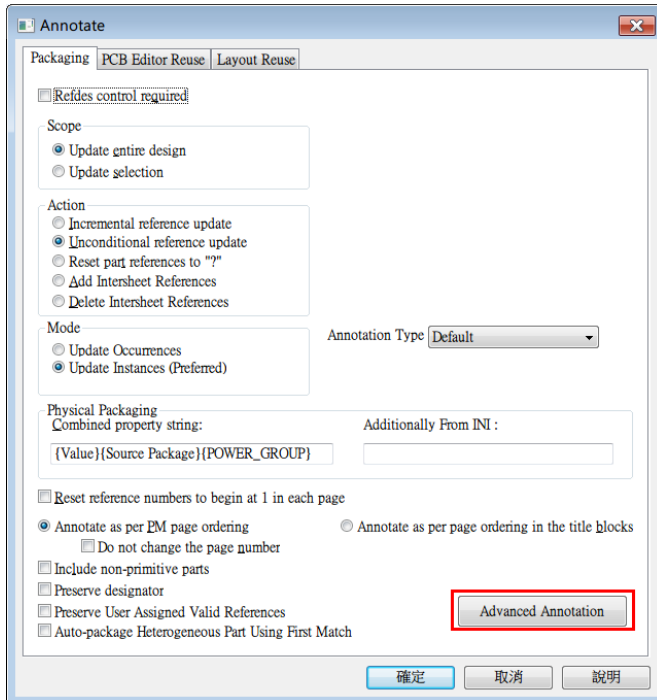
Auto Wire

- Tow Points



Advanced Annotation

- You can annotate multiple schematic pages at a time.



Advanced Annotation

- Design / Hierarchical Block / Page / Property Block level REFDES control
- REFDES Control –
 - Prefix based (R ,U..)
 - Generic (support of *)
- Hierarchical support of specified Ranges
 - Inherited from the Parent
 - Closest assigned range wins
- Auto Instance count support
 - To help in deciding range span
- Auto reference follows the specified range for Blocks / Pages
 - Place part
 - Copy – Paste part

The screenshot displays the 'Reference Range for REFERENCE1.DSN' dialog box. The table below shows the reference ranges for various prefixes:

Prefix	Instance Count	Start	End
C	26	1	26
J	3	1	3
U	31	1	31
CR	4	1	4
*	0	1	1
HIGH_SPEED_RAM	1	1	1

Below the table are buttons: Auto Fill Prefix, Add Row, Delete Row(s), Delete All, and Apply. A dropdown menu is open, showing a list of hierarchical blocks with checkboxes:

- ROOM=HIGH_SPEED_RAM
- DAAMM...
- HIGH_SPEED_RAM
- RAM-1
- RAM-2
- (HIGH_SPEED_RAM)
- RAM-1
- RAM-2

Graphical Design Difference Viewer



- You can view logical and graphical differences between two designs, schematic folders, or schematic pages.

Design Difference Summary

Differences generated using **Object ID**. Regenerate using [Object Name / Part Reference](#).

Logical Differences		All Differences	
Show Details		Show Details	
Object	Number of Differences	Object	Number of Differences
Components	3	Schematic	1
Pin Net Connectivity	0	Page	1
FlatNet	6	Components(Logical Differences)	3
		Components(All Differences On Matching Pages Only)	3
		Pin Net Connectivity	0
		FlatNet	6
		Wire	0
		OffPage	0
		Hierarchical Port	0
		TitleBlock	1

General Information		
Selected Options	Design1	Design2
	D:\WorkData\Capture\17.2\OrCA	D:\WorkData\Capture\17.2\OrCA
	D:\Capture\17.2\Tutorial\DPD	D:\Capture\17.2\Tutorial\DPD

file:///F:/capture_automation/172_diff_viewer/demo/ALL_CAT/abc_vs_abc_mod.html

ABC.DSN

ABC_MOD.DSN

S.No.	ABC.DSN	ABC_MOD.DSN	Information
	Components Difference		Number of differences: 16
	Pin Net Connectivity Difference		Number of differences: 4
	FlatNets Difference		Number of differences: 12

- Supported Browser
 - Chrome (v45 +)
 - recommended
 - IE (11 & above)

Graphical Design Difference Viewer



Difference Categories

- Detailed Mode

- Schematic Difference

- PAGE differences

- ▶ Components Difference

- ◆ Property Difference
 - ◆ Pin Difference
 - ✓ Property Difference
 - ◆ Occurrence Difference
 - ✓ Property Difference

- ▶ Wire Differences

- ◆ Property Difference
 - ▶ Port Differences
 - ◆ Property Difference
 - ▶ Off-Page Differences
 - ◆ Property Difference
 - ▶ Title block/Buses Differences

S.No.	design_v1.dsn	design_v2.DSN	Information
Schematic Difference			
1	SCHEMATIC1	SCHEMATIC1	Number of differences: 1
Page Difference			
1-1	PAGE1	PAGE1	Number of differences: 1
Components Difference			
1-1-1	U2	U2	Property Difference(2)
1-1-2	U3A	U33A	Property Difference(3)
Property Difference			
1-1-2-1	Location Y-Coordinate	110	90
1-1-2-2	Part Reference	U3A	U33A
1-1-2-3	Reference	U3	U33
1-1-3	U3B	U33B	Property Difference(2)
Wires Difference			
			Number of differences: 3

Demo Design



- The Cadence® hierarchy contains more than 150 demo designs to help you understand OrCAD® Capture, Capture CIS, and the Capture – PSpice® flow.

Name	Capture	CIS	PSpice	PSpiceAA	Allegro	Lite	Info
3-to-8 line decoder	Y	N	Y	N	Y	Y	?
8-bit Analog to Digital converter	Y	N	Y	N	N	Y	?
8-bit BCD counter using Actel devices	Y	N	N	N	N	Y	?
8-bit BCD counter using Altera devices	Y	N	N	N	N	Y	?
8-bit BCD counter using Xilinx devices	Y	N	N	N	N	Y	?
8-bit Digital to Analog converter	Y	N	Y	N	N	Y	?
80C51 Board Schematic	Y	N	N	N	N	N	?
AC Analysis of RC circuit	Y	N	Y	N	N	N	?
ADC parameterizing circuit	Y	N	Y	N	N	Y	?
Amplitude and Balanced Modulation	Y	N	Y	N	N	Y	?
Analyzing Amplifier's Settling time	Y	N	Y	N	N	Y	?
BJT as a switch	Y	N	Y	N	N	N	?
BJT common base configuration circuit	Y	N	Y	N	N	N	?
BJT common emitter configuration circuit	Y	N	Y	N	N	N	?
BJT emitter follower circuit	Y	N	Y	N	N	N	?

Open Cancel

Open Demo Design: low pass filter

Mixed Simulation Designs

PSpice hierarchical design

A 4th Order Chebyshev Filter circuit that demonstrates frequency domain (AC) analysis and Monte Carlo analysis. This design example shows the following:

- Using a hierarchical schematic for PSpice Simulation.
- Using a single circuit block to create a cascading design; connecting two 2nd order filter block in series to build a 4th order filter.
- Passing a parameter (component value) to lower level design blocks.
- Setting up tolerances on a discreties, such as resistors and capacitors.
- Setting up statistical analysis such as Monte Carlo in PSpice.

Phase-shift oscillator

A phase-shift oscillator design. In this design, the PSpice option *RELTOL* has been tightened to 0.00001 to improve the accuracy of the transient response. This design cannot be simulated using the OrCAD® Lite version.

3-to-8 line decoder

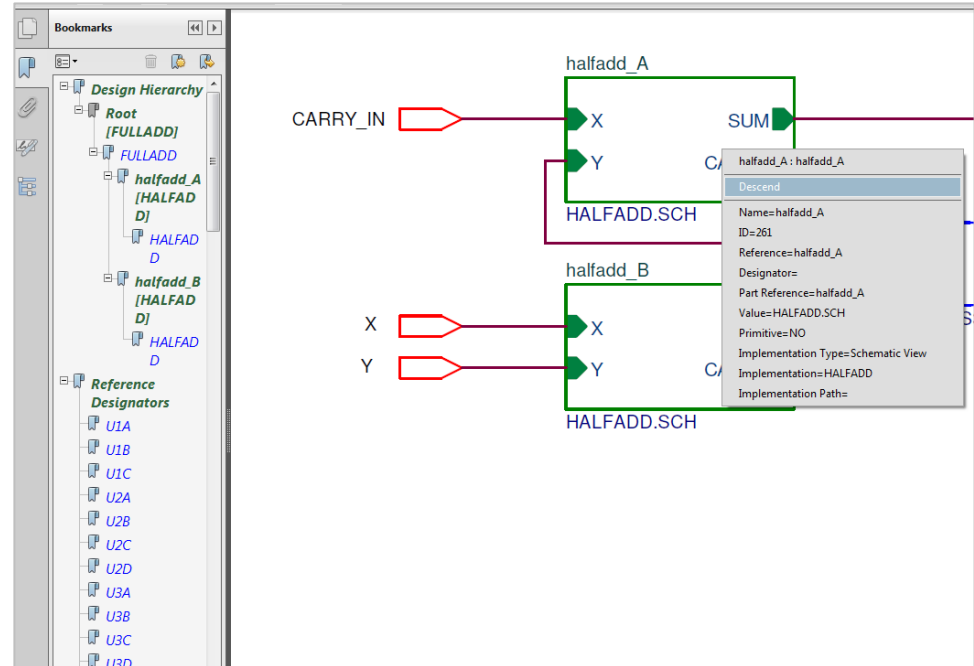
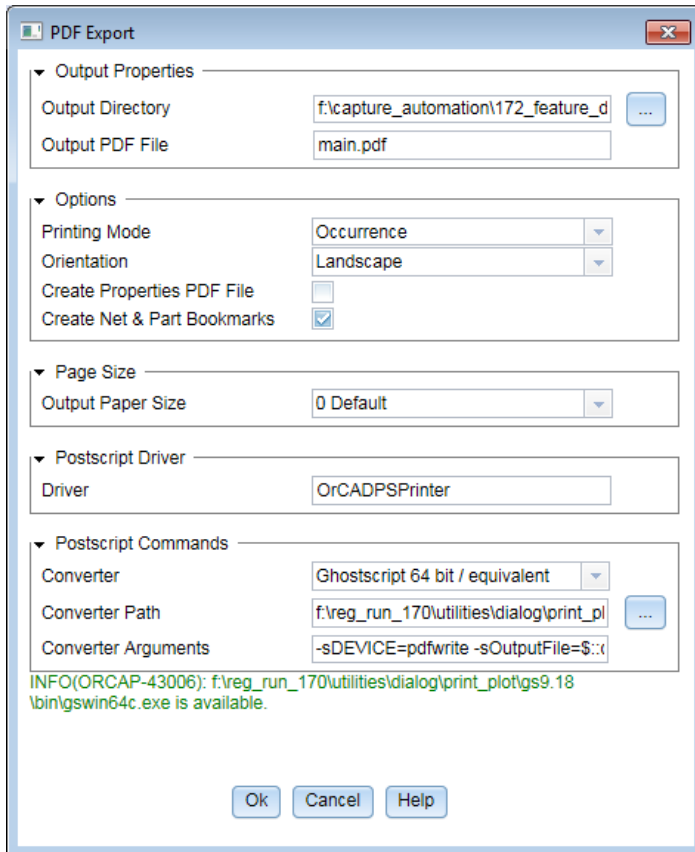
A simple decoder circuit that demonstrates digital event-driven simulation capability of PSpice. It uses stimulus sources as input source.

Digital frequency-comparator

This design example demonstrates digital simulation capability of PSpiceAD simulator. This design uses data bus for establishing connectivity between the devices as against bit wise connection.

Export PDF

- Export a Capture design as a PDF file.
 - Capture Design PDF
 - Capture Design Object Properties PDF



OrCAD TcI/Tk Support



OrCAD Capture Marketplace

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Log In | Register

Online Store





Browse for custom or enhanced features, functions, and design capabilities

Store Home **Products** My Apps My Account

Plug-In Type: All Free/Paid: All Added: All Reset Filters: Clear All

Products

Sort by: Name

 CDN Capture Cached Object Reporting Reports out-of-date cached objects in the active Capture design ☆☆☆☆☆ Free Download 0 Ratings	 Capture INI Manager Framework for manipulating the Capture INI file ☆☆☆☆☆ Free Download 0 Ratings
 CIPinCIS Instant access to search and download component data for millions of parts without having to leave OrCAD Capture ☆☆☆☆☆	 CircuitFit Perform early fit studies at the schematic level before you commit to placement ☆☆☆☆☆

Cart

0 Items US \$0.00

Related Documents

- Tcl/Tk Extensions in OrCAD Capture
- OrCAD Capture Marketplace FAQs
- Capture Intelligent PDF Generation App Movie

Recommended Products

- Find in Design ★★★★★
- Intelligent PDF ★★★★★
- Locked Object Reporter ★★★★★
- CIPinCIS ★★★★★
- Extended Preferences Dialog ★★★★★
- Show Open Libraries and Designs ★★★★★
- Customize Page on Creation ★★★★★

Export PDF

- 電路圖手動輸入零件資訊與 BOM 表操作人工確認。



1/8W

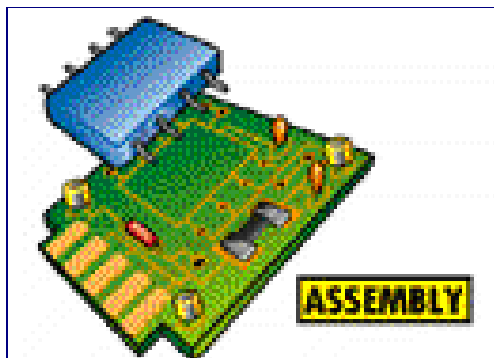
1K

ERJ-8GEYJ102V

5%

1206

(Footprint)



Problems:

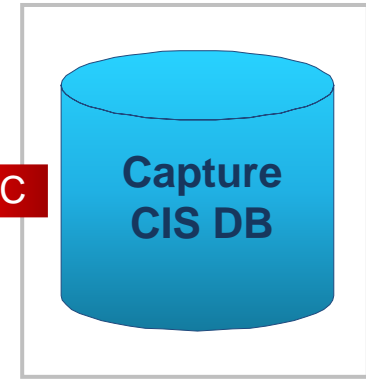
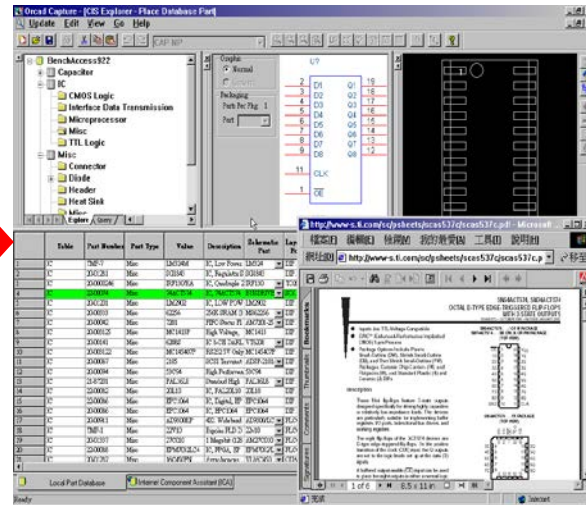
- 耗費時間
- 人爲輸入錯誤的錯誤

OrCAD Capture CIS System

- 設計資料之完整性的文件輸出
 - 零件物料清單 (Bill of Materials)
 - 零件網路表 (NetList)

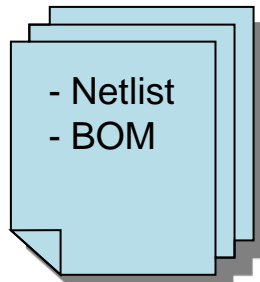
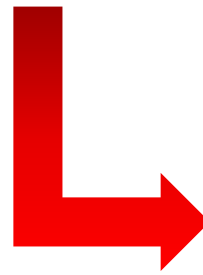


Engineers



ODBC

OrCAD[®] Capture CIS



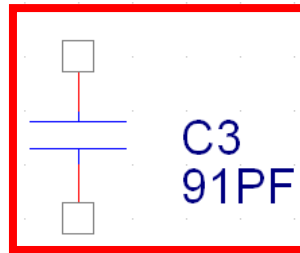
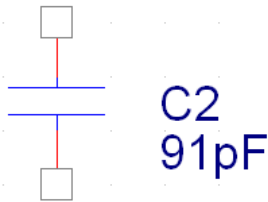
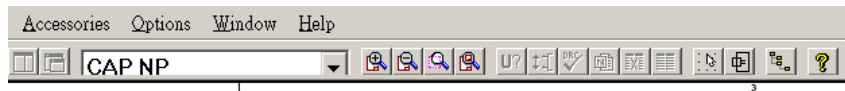
- Netlist
 - BOM

- OrCAD Capture CIS 是一套可以在繪製電路圖時，電路圖零件符號從公司或企業內所建立的 CIS 零件資料庫中，**直接取得**零件的相關資訊 (Part_Number、Footprint)，且可將資料輸出到 BOM 表中。

OrCAD Capture CIS System



- Auto-add schematic part properties from CIS database.



	A	B
	SCHEMATIC1 : PA	SCHEMATIC1 : PA
Color	Default	Default
Description		CAP 91PF 50V CERA
Designator		
Graphic	CAP NP.Normal	CAP NP.Normal
ICA_MFR_NAME		
ICA_PARTNUM		
ID		
Implementation		
Implementation Path		
Implementation Type	<none>	<none>
Location X-Coordinate	370	430
Location Y-Coordinate	170	170
Name	INS137	INS164
Part Number		PCC910CQTR-ND
Part Reference	C2	C3
PCB Footprint		smdcap
Power Pins Visible	<input type="checkbox"/>	<input type="checkbox"/>
Primitive	DEFAULT	DEFAULT
Reference	C2	C3
Source Library	C:\ORCAD\ORCAD	C:\ORCAD\ORCAD
Source Package	CAP NP	CAP NP
Source Part	CAP NP.Normal	CAP NP.Normal
Value	91pF	91PF
Voltage		50V

OrCAD Capture CIS System



- Row Coloring & Row Filtering

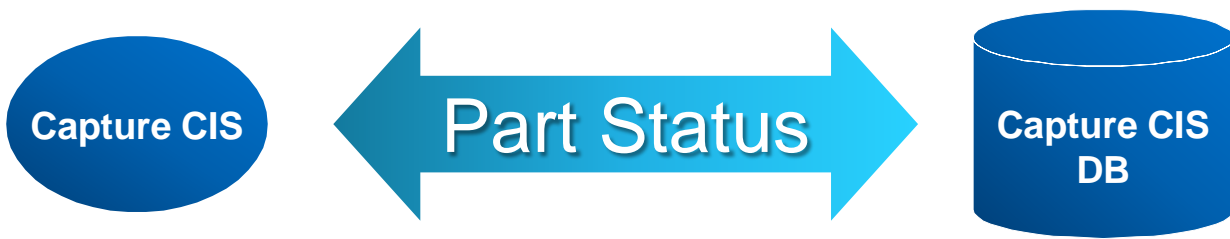
	Table	Part Number	Part Type	Value	Description	Voltage	Tolerance	Schematic Part	PCB Footprint	Layout PCB Footprint	Implementation	Manufacturer Part Number	Manufacturer	Approved	Distributor Part Number	Distributor	Price	Availability	Datasheet	Activeparts ID
120	Capacitor	PCC180C	Ceramic	18PF	18PF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic		PCC180C	Digi-Key	0.025	In Stock	capcerm.pdf	
121	Capacitor	PCC153BG	Ceramic	0.015UF	015UF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	EOL	PCC153BG	Digi-Key	0.036	In Stock		
122	Capacitor	PCC152BN	Ceramic	0.0015UF	0015UF 50	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	EOL	PCC152BN	Digi-Key	0.025	In Stock		
123	Capacitor	PCC151C	Ceramic	150PF	150PF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	EOL	PCC151C	Digi-Key	0.027	In Stock	capcerm.pdf	
124	Capacitor	PCC150C	Ceramic	15PF	15PF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	EOL	PCC150C	Digi-Key	0.025	In Stock	capcerm.pdf	
125	Capacitor	PCC123BG	Ceramic	0.012UF	012UF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC123BG	Digi-Key	0.033	In Stock		
126	Capacitor	PCC122BN	Ceramic	0.0012UF	0012UF 50	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC122BN	Digi-Key	0.025	In Stock		
127	Capacitor	PCC121C	Ceramic	120PF	120PF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC121C	Digi-Key	0.027	In Stock	capcerm.pdf	
128	Capacitor	PCC120C	Ceramic	12PF	12PF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC120C	Digi-Key	0.025	In Stock	capcerm.pdf	
129	Capacitor	PCC103BN	Ceramic	0.01UF	01UF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC103BN	Digi-Key	0.031	In Stock		
130	Capacitor	PCC102BN	Ceramic	1000PF	1000PF 50	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC102BN	Digi-Key	0.025	In Stock		
131	Capacitor	PCC102C	Ceramic	1000PF	1000PF 50	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC102C	Digi-Key	0.044	In Stock		
132	Capacitor	PCC101C	Ceramic	100PF	100PF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC101C	Digi-Key	0.027	In Stock		
133	Capacitor	PCC100C	Ceramic	10PF	10PF 50V	50V		discrete1	smdcap	SMC_0805	C	ECU-V1H1	Panasonic	NO	PCC100C	Digi-Key	0.022	In Stock		

	Table	Part Number	Part Type	Value	Description	Voltage	Tolerance	Schematic Part	PCB Footprint	Layout PCB Footprint	Implementation	Manufacturer Part Number	Manufacturer	Approved	Distributor Part Number	Distributor	Price	Availability	Datasheet	Activeparts ID
26	Capacitor	PCC121C	Ceramic	120PF	CAP 120PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H1	Panasonic	NO	PCC121C	Digi-Key	0.087	In Stock	capcerm.pdf	
27	Capacitor	PCC120C	Ceramic	12PF	CAP 12PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H1	Panasonic	NO	PCC120C	Digi-Key	0.079	In Stock	capcerm.pdf	
28	Capacitor	PCC111C	Ceramic	110PF	CAP 110PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H1	Panasonic	NO	PCC111C	Digi-Key	0.087	In Stock	capcerm.pdf	
29	Capacitor	PCC110C	Ceramic	11PF	CAP 11PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H1	Panasonic	NO	PCC110C	Digi-Key	0.079	In Stock	capcerm.pdf	
30	Capacitor	PCC101C	Ceramic	100PF	CAP 100PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H1	Panasonic	NO	PCC101C	Digi-Key	0.083	In Stock		
31	Capacitor	PCC100C	Ceramic	10PF	CAP 10PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H1	Panasonic	NO	PCC100C	Digi-Key	0.079	In Stock		
32	Capacitor	PCC0R5C	Ceramic	0.5PF	CAP 0.5PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	NO	PCC0R5C	Digi-Key	0.079	0 week(s)		
33	Capacitor	PCC090C	Ceramic	9.0PF	CAP 9.0PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	YES	PCC090C	Digi-Key	0.079	In Stock	capcerm.pdf	
34	Capacitor	PCC080C	Ceramic	8.0PF	CAP 8.0PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	YES	PCC080C	Digi-Key	0.079	0 week(s)	capcerm.pdf	
35	Capacitor	PCC070C	Ceramic	7.0PF	CAP 7.0PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	YES	PCC070C	Digi-Key	0.079	In Stock	capcerm.pdf	
36	Capacitor	PCC060C	Ceramic	6.0PF	CAP 6.0PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	YES	PCC060C	Digi-Key	0.079	In Stock	capcerm.pdf	
37	Capacitor	PCC050C	Ceramic	5.0PF	CAP 5.0PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	YES	PCC050C	Digi-Key	0.079	In Stock	capcerm.pdf	
38	Capacitor	PCC040C	Ceramic	4.0PF	CAP 4.0PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	YES	PCC040C	Digi-Key	0.079	In Stock	capcerm.pdf	
39	Capacitor	PCC030C	Ceramic	3.0PF	CAP 3.0PF	50V		discrete1	smdcap	SMC_0402	C	ECU-E1H0	Panasonic	YES	PCC030C	Digi-Key	0.079	In Stock	capcerm.pdf	

OrCAD Capture CIS System



- Part Manager - 零件資訊的查核驗證，可驗證電路圖零件資訊是否與資料庫相符，減低人爲的錯誤。



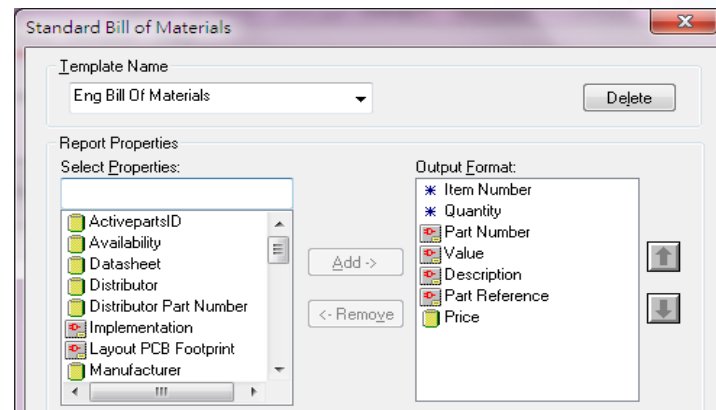
Part Reference	Value	Part Number	Part Status	Source Library	Source Pack
Y201	10MHz	20-00442	Approved: Current	C:\WINDOWSTE...	CRYSTAL
C722	0.1UF	EC6-V1H8R1SR	Approved: Current	C:\WINDOWSTE...	CAP
S201	BER02	70-00029	Approved: Current	C:\WINDOWSTE...	2W PWRHEUIT
C723	0.1UF	EC6-V1HA0R1SR	Approved: Current	C:\WINDOWSTE...	CAP
TP202	TESTPOINT	60-00030	Approved: Current	C:\WINDOWSTE...	TP-105-01-00
C724	0.1UF	EC6-V1HA0R1SR	Approved: Current	C:\WINDOWSTE...	CAP
Y201	HEADER8	60-00039	Approved: Current	C:\WINDOWSTE...	8 HEADER
C725	0.1UF	EC6-V1HA0R1R	Approved: Current	C:\WINDOWSTE...	CAP
TP201	TESTPOINT	60-00038	Approved: Current	C:\WINDOWSTE...	TP-105-01-00
C726	0.1UF	EC6-B1H0B0R1	Approved: Current	C:\WINDOWSTE...	CAP
C201	222F	PCC220CNR-ND	Approved: Current	C:\WINDOWSTE...	SMALL CAP
C403	222F	PCC220CNR-ND	Approved: Current	D:\ORCAD\WINV...	CAP NP
C727	0.1UF	EC6-A1HKK0R1	Approved: Current	C:\WINDOWSTE...	CAP
C202	222F	PCC220CNR-ND	Approved: Current	C:\WINDOWSTE...	SMALL CAP
C728	0.1UF	EC6-A1HKK0R1	Approved: Current	C:\WINDOWSTE...	CAP
U301	2105	20-00067	Approved: Current	C:\WINDOWSTE...	ADSP-2101KP-5
C729	0.1UF	EC6-V1HA0R1R	Approved: Current	C:\WINDOWSTE...	CAP
S201	75	ERJ-05EV750V	Approved: Current	C:\WINDOWSTE...	R
C204	150pF	PCC150CTR-ND	Approved: Not Current	C:\WINDOWSTE...	C
U603	74LS138	TMP-3	Temporary: Not Current	C:\WINDOWSTE...	74LS138
U410	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10A
U111	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10
U109	74ALS138	TMP-2	Temporary: Current	C:\WINDOWSTE...	74ALS138
U412	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10A
U509	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10A
U303	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10A
U322	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10
U318	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10
U320	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10
U411	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10A
U602	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10
U402	22V10	TMP-1	Temporary: Current	C:\WINDOWSTE...	22V10A
R306	2.7K	UNDEFINED	Undefined	C:\WINDOWSTE...	RESISTOR
C207	0.1UF	UNDEFINED	Undefined	C:\WINDOWSTE...	CAP

OrCAD Capture CIS System

- 值得信賴的設計資料之完整性的文件輸出
 - 零件物料清單 (Bill of Materials)
 - 零件網路表 (NetList)

```

e:\user_file\wistron\alle\gro\psb\prt.dat
1: FILE_TYPE = EXPANDEDPARTLIST;
2: ( Using PSTWRITER 15.7.0 p001Aug-07-2006 at 14:24:05 )
3: DIRECTIVES
4: PST_VERSION='PST_HDL_CENTRIC_VERSION_0';
5: ROOT_DRAWING='DESIGN5';
6: POST_TIME='May 28 2006 22:05:31';
7: SOURCE_TOOL='CAPTURE_WRITER';
8: END_DIRECTIVES;
9:
10: PART_NAME
11: C1 'CAPACITOR NON-POL_0_SMDCAP_B90P';
12: VOLTAGE='50V';
13: ROOM='RF_AREA';
14:
15:
16: NET_NAME
17: 'RESET'
18: '@DESIGN70-1.SCHEMATIC1(SCH_1):RESET';
19: C_SIGNAL='@\design70-1\schematic1(sch_1):reset',
20: MAX_VIA_COUNT='3',
21: MIN_LINE_WIDTH='8mil';
    
```

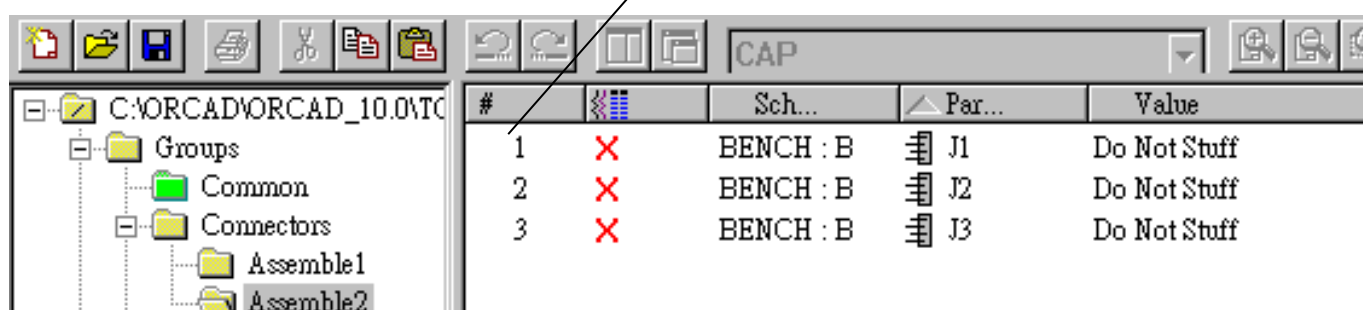


	A	B	C	D	E	F	G
1	Item Num	Quantity	Part Num	Value	Description	Part Refere	Price
17	16	1	40-00018	MV209	Diode	D501	0.15
18	17	1	70-00022	BERG5	Connector, E401		0
19	18	10	70-00029	BERG2	Connector, E402,E403		0
20	19	3	70-00037	BNC	Connector, J?		0
21	20	1	60-00047	HEADER5	Header, 2 r JP401		0
22	21	2	60-00042	HEADER5	Header, 2 r JP502,P602		0
23	22	3	80-00043	282u	282u Induct L?		0.17
24	23	3	80-00089	12.8m	12.8m Induct L?		0.17
25	24	1	60-00037	HEADER1	Header, 2 r P101		0
26	25	1	70-00048	ECON62	Connector, P401		0
27	26	1	70-00049	DB25P	Connector, P501		0.89
28	27	1	70-00052	DIN96	Connector, P601		0
29	28	1	60-00044	HEADER1	Header, 2 r P603		0
30	29	1	60-00043	HEADER9	Header, A1P604		0

OrCAD Capture CIS System

- CIS Variant BOM :
按**需求(或規格)**，設定不同的零件資訊，產生**多樣化 BOM** 表。

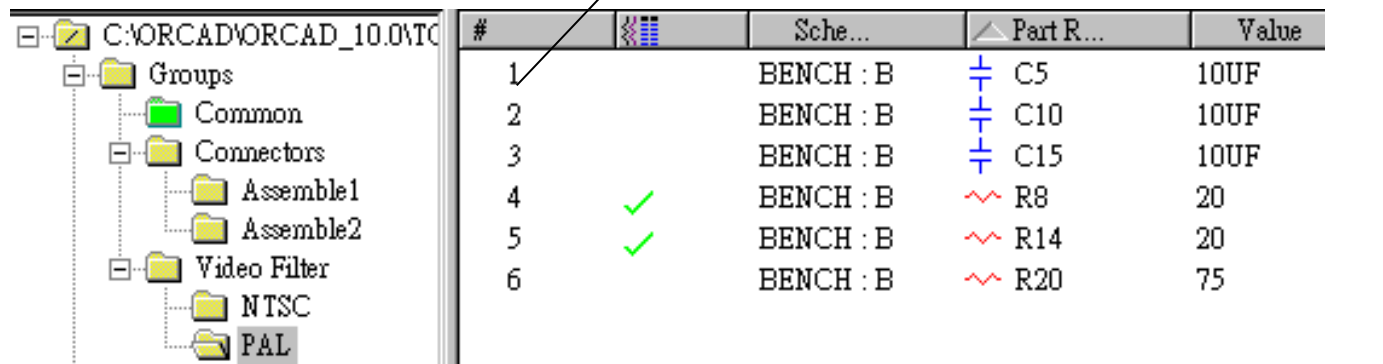
Set NC Parts before report BOM



The screenshot shows the OrCAD Capture CIS interface. The left pane displays a project tree with folders: Groups, Common, Connectors, Assemble1, and Assemble2. The main window shows a BOM table with the following data:

#		Sch...	△ Par...	Value
1	✗	BENCH : B	J1	Do Not Stuff
2	✗	BENCH : B	J2	Do Not Stuff
3	✗	BENCH : B	J3	Do Not Stuff

Set change parts before report BOM

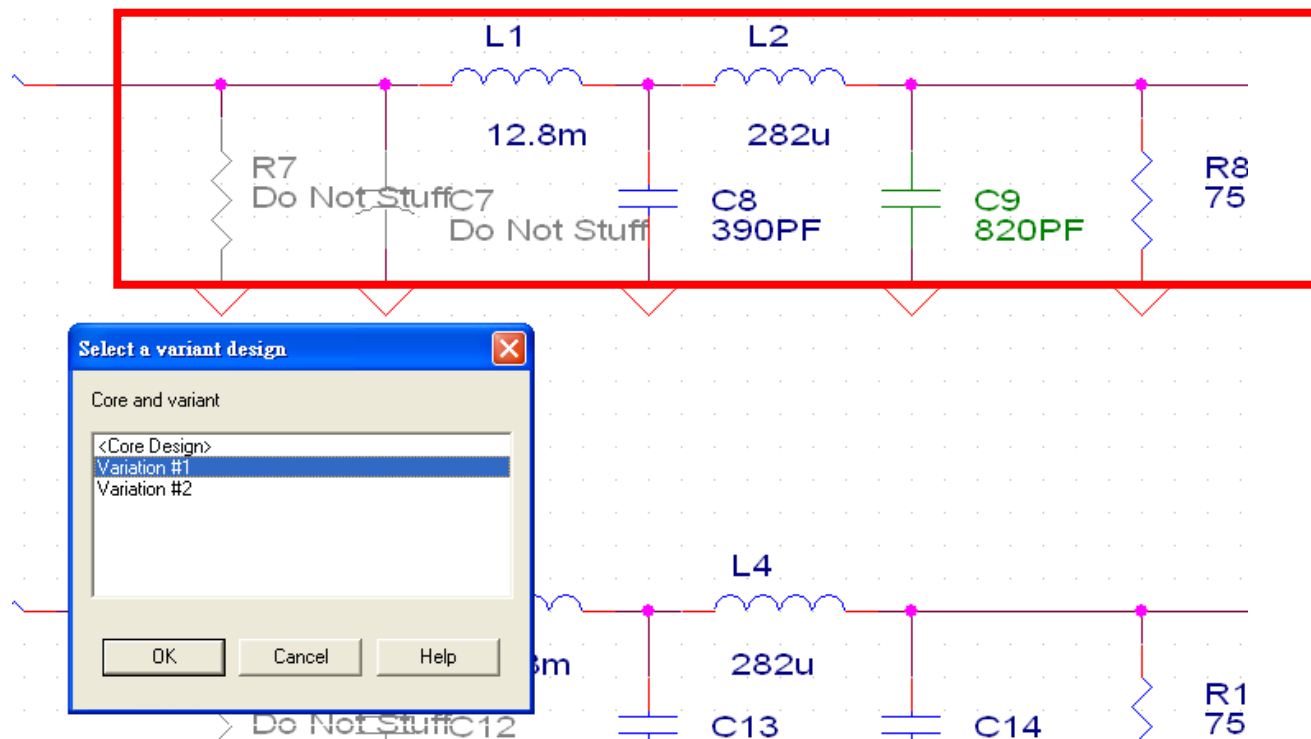


The screenshot shows the OrCAD Capture CIS interface. The left pane displays a project tree with folders: Groups, Common, Connectors, Assemble1, Assemble2, Video Filter, NTSC, and PAL. The main window shows a BOM table with the following data:

#		Sche...	△ Part R...	Value
1		BENCH : B	C5	10UF
2		BENCH : B	C10	10UF
3		BENCH : B	C15	10UF
4	✓	BENCH : B	R8	20
5	✓	BENCH : B	R14	20
6		BENCH : B	R20	75

OrCAD Capture CIS System

- 電路圖查看多樣化 BOM 表設計結果。



GraserWare FrontEnd PACK Application



- Schematic Edit Application
 - Replace BUS Alias
 - Export-Import Properties
 - Reference Edit
 - NC-Part Setting
- Verify & Report
 - Capture Design Compare
 - Part Check Utility

Replace BUS Alias

- How to change BUS signal Name by page?
 - Manually change
 - Delete and reconnect the net
 - Global Replace for string

The diagram illustrates a bus signal list on the left and a 'Find And Replace' dialog box on the right. The bus signals are listed as follows:

PMS	37	PMS-
DMS	38	DMS-
BMS	39	BMS-
RD	45	DSP_RD-
WR	44	DSP_WR-
A0	21	DSP_A0
A1	22	DSP_A1
A2	23	DSP_A2
A3	24	DSP_A3
A4	25	DSP_A4
A5	27	DSP_A5
A6	28	DSP_A6
A7	30	DSP_A7
A8	31	DSP_A8
A9	32	DSP_A9
A10	33	DSP_A10
A11	34	DSP_A11
A12	35	DSP_A12
A13	36	DSP_A13

The 'Find And Replace' dialog box is configured as follows:

- Find what: DSP_A0
- Replace with: DSP_D0
- Match Case:
- Scope: Entire Design, Current Page Only
- Object Type: Hierarchical Ports, Hierarchical Pins, Net Aliases, OffPage Connector

2105

Replace BUS Alias

- [GraserWARE FrontEnd PACK] - Replace Bus alias
 - By Selection
 - By Page
 - By Design

The screenshot shows a circuit diagram on the left with bus aliases being replaced. The bus aliases are listed as follows:

Bus Alias	Pin Number	Signal Name
BMS_RD	45	BMS-DSP_RD-
BMS_WR	44	DSP_WR-
A0	21	DSP_D0
A1	22	DSP_D1
A2	23	DSP_D2
A3	24	DSP_D3
A4	25	DSP_D4
A5	27	DSP_D5
A6	28	DSP_D6
A7	30	DSP_D7
A8	31	DSP_D8
A9	32	DSP_D9
A10	33	DSP_D10
A11	34	DSP_D11
A12	35	DSP_D12
A13	36	DSP_D13

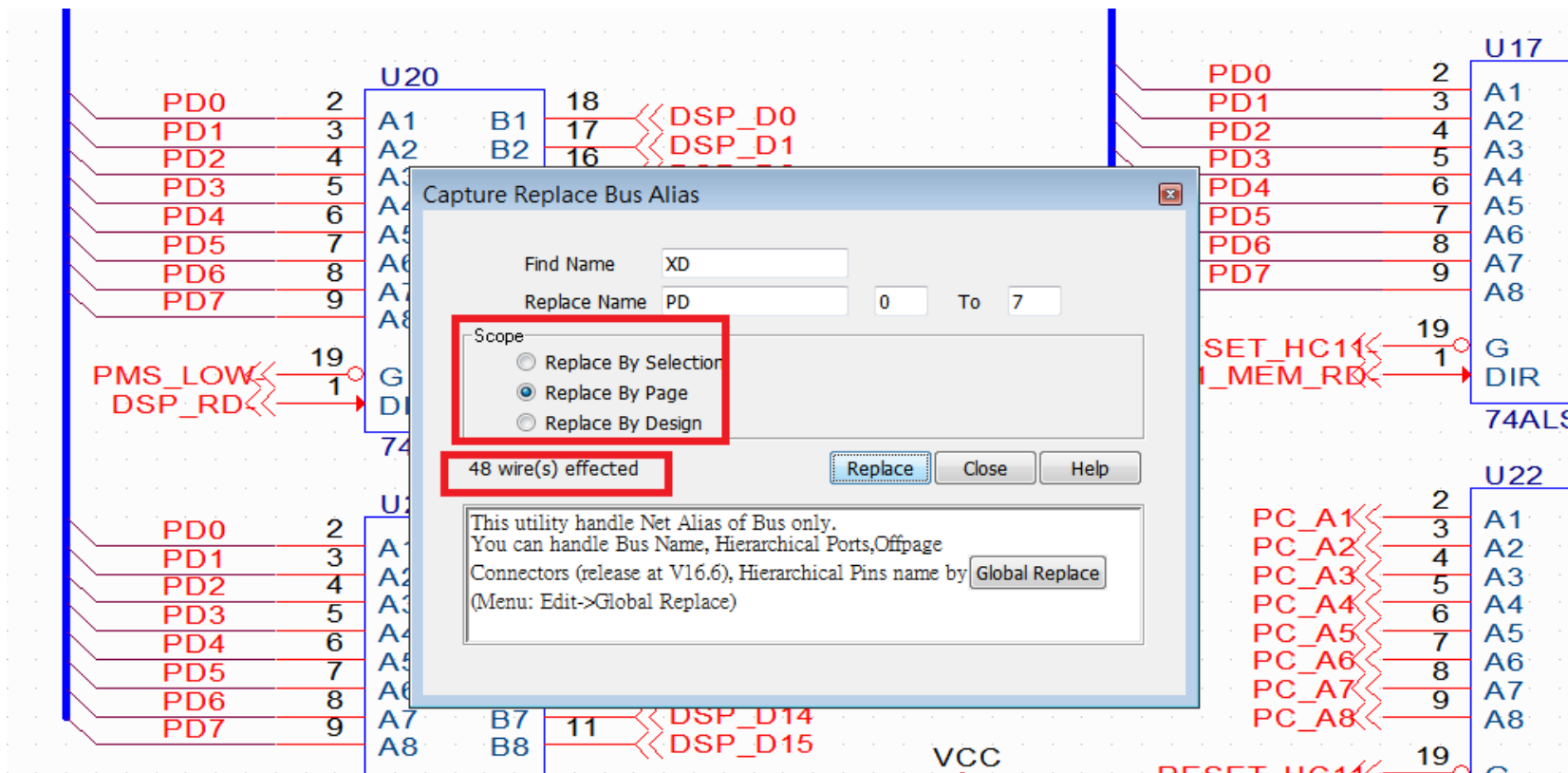
The 'Capture Replace Bus Alias' dialog box is shown with the following settings:

- Find Name: DSP_A
- Replace Name: DSP_D
- Scope:
 - Replace By Selection
 - Replace By Page
 - Replace By Design
- 14 wire(s) effected
- Buttons: Replace, Close, Help

The background diagram shows a bus alias 'DSP_D[0..13]' being replaced. The bus alias is shown as a blue line connecting to a bus symbol 'DSP_D[0..13]'.

Replace BUS Alias

- [GraserWARE FrontEnd PACK] - Replace Bus alias
 - RESULT



Design Properties Editor



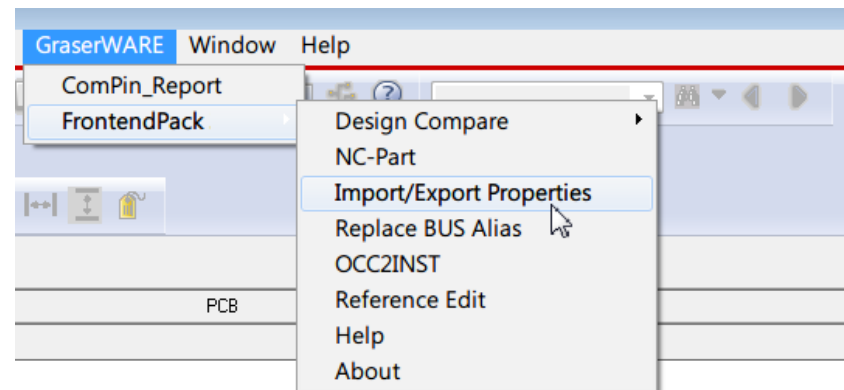
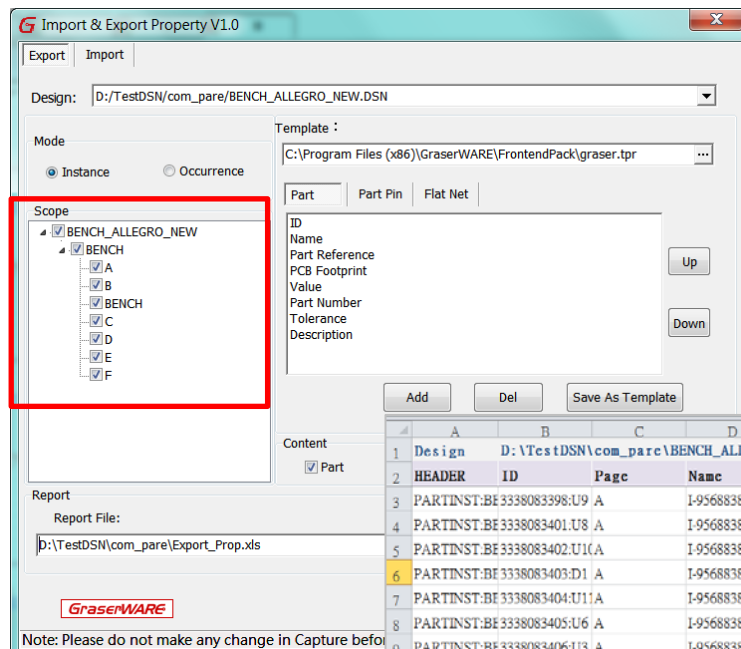
- Traditional edit properties solution - Property Editor
 - Hard to find which properties you want

The screenshot shows the OrCAD Capture CIS interface. The main window displays a circuit schematic with three LM2902 comparators (U14A, U14B, U14C) and various passive components (resistors R4-R18 and capacitors C6, C11, C16). The Property Editor window is open on the right, showing a table of properties for selected components.

	A	B	C	D
Tag	BENCH : B : C3	BENCH : B : C4	BENCH : B : C5	BENCH : B :
Color	Default	Default	Default	Default
Description	22PF 50V CERAMI	22PF 50V CERAMI	CAP 10UF 50V VS	
Designator				
Graphic	SMALL CAP Normal	SMALL CAP Normal	CP Normal	CAP Norma
ID				
Implementation Path				
Implementation Type	<none>	<none>	<none>	<none>
Location X-Coordinate	260	260	1340	550
Location Y-Coordinate	130	170	650	680
Name	I-956883785	I-956883784	I-956883704	I-95688370
Part Number	PCC220CNTR-ND	PCC220CNTR-ND	ECE-V1HA100SP	
Part Reference	C3	C4	C5	C6
PCB Footprint	smdcap	smdcap		
Power				
Power Pins Visible	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Primitive	YES	YES	YES	YES
PSpice	C	C	C	
Rating				
Reference	C3	C4	C5	C6
Source Library	C:\WINDOWS\SI...	C:\WINDOWS\SI...	C:\WINDOWS\SI...	C:\WINDOWS\SI...
Source Package	SMALL CAP	SMALL CAP	CP	CAP
Source Part	SMALL CAP Norma	SMALL CAP Norma	CP Normal	CAP Norma
Tolerance				
Value	22PF	22PF	10UF	0.1UF
Voltage	50V	50V	50V	

Design Properties Editor

- [GraserWARE FrontEnd PACK] - Export Properties
 - Export Design Properties to Excel file



	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Design	D:\TestDSN\com_pare\BENCH_ALLEGRO_NEW.DSN											
2	HEADER	ID	Page	Name	Part Reference	PCB Footprint	Value	Part Number	Tolerance	Description			
3		PARTINST.BE3338083398:U9	A	I-956883898	U9	dip16_3	74ALS138	TMP-2		IC, 74ALS138, multiplexer, Standard input, Inverted, totem output			
4		PARTINST.BE3338083401:U8	A	I-956883895	U8	dip20_3	74ALS273	20-81432		IC, 74ALS273 OCTAL D POS EDGE TRIGG 20 DIP			
5		PARTINST.BE3338083402:U1(A		I-956883894	U10	dip20_3	74ALS245	20-003297		IC, 74ALS245 (N)OCTL TRI-ST TRANSCVR 20DIP			
6		PARTINST.BE3338083403:D1	A	I-956883893	D1		RA-LED	40-00017		LED Red			
7		PARTINST.BE3338083404:U11	A	I-956883892	U11	plcc28	22V10			Bipolar PLD Device			
8		PARTINST.BE3338083405:U6	A	I-956883891	U6	dip16_3	7201	20-00042		FIFO Status Flag Expandable 512x9			
9		PARTINST.BE3338083406:U3	A	I-956883890	U3	dip16_3	7201	20-00042		FIFO Status Flag Expandable 512x9			
10		PARTINST.BE3338083407:U5	A	I-956883889	U5	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
11		PARTINST.BE3338083408:U2	A	I-956883888	U2	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
12		PARTINST.BE3338083409:U1	A	I-956883887	U1	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
13		PARTINST.BE3338083410:U4	A	I-956883886	U4	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
14		PARTINST.BE3338083411:U7	A	I-956883885	U7	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
15		PARTINST.BE3338083412:TP1	A	I-956883884	TP1		TESTPOINT	60-00038		Header, 1 row, 1 pin			
16		PARTINST.BE3338083413:P1	A	I-956883883	P1		HEADER12	60-00037		Header, 2 row x 6 pin			
17		PARTINST.BE3338083414:R2	A	I-956883882	R2	smdres	100	ERJ-2GEJ101X	5%	Carbon Film Resistor 100 OHM 1/16W 5% 0402 SMD			
18		PARTINST.BE3338083415:R1	A	I-956883881	R1	smdres	100	ERJ-2GEJ101X	5%	Carbon Film Resistor 100 OHM 1/16W 5% 0402 SMD			
19		PARTINST.BE3338083416:R3	A	I-956883880	R3	res400	10K	ERJ-8GEY1103	5%	Carbon Film Resistor 10K OHM 1/8W 5% 1206 SMD			

Design Properties Editor

- [GraserWARE FrontEnd PACK] - Import Properties
 - Import part properties from Excel into Capture schematic design

	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Design	D:\TestDSN\com_pare\BENCH_ALLEGRO_NEW.DSN											
2	HEADER	ID	Page	Name	Part Reference	PCB Footprint	Value	Part Number	Tolerance	Description			
3	PARTINST:BE	3338083398	U9	A	I-956883898	U9	dip16_3	74ALS138	20-00045		IC, 74ALS138, multiplexer, Standard input, Inverted, totem ouput		
4	PARTINST:BE	3338083401	U8	A	I-956883895	U8	dip20_3	74ALS273	20-81432		IC, 74ALS273 OCTAL D POS EDGE TRIGG 20 DIP		
5	PARTINST:BE	3338083402	U1	A	I-956883894	U10	dip20_3	74ALS245	20-003297		IC, 74ALS245 (N)OCTL TRI-ST TRANSCVR 20DIP		
6	PARTINST:BE	3338083403	D1	A	I-956883893	D1	SMDLED	RA-LED	40-00017		LED Red		
7	PARTINST:BE	3338083404	U11	A	I-956883892	U11	plcc28	22V10	20-00033		Bipolar PLD Device		
8	PARTINST:BE	3338083405	U6	A	I-956883891	U6	dip16_3	7201	20-00042		FIFO Status Flag Expandable 512x9		
9	PARTINST:BE	3338083406	U3	A	I-956883890	U3	dip16_3	7201	20-00042		FIFO Status Flag Expandable 512x9		
10	PARTINST:BE	3338083407	U5	A	I-956883889	U5	dip20_3	6264	20-00042		FIFO Status Flag Expandable 512x9		
11	PARTINST:BE	3338083408	U2	A	I-956883888	U2	dip20_3	6264	20-00042		FIFO Status Flag Expandable 512x9		
12	PARTINST:BE	3338083409	U1	A	I-956883887	U1	dip20_3	6264	20-00042		FIFO Status Flag Expandable 512x9		
13	PARTINST:BE	3338083410	U4	A	I-956883886	U4	dip20_3	6264	20-00042		FIFO Status Flag Expandable 512x9		
14	PARTINST:BE	3338083411	U7	A	I-956883885	U7	dip20_3	6264	20-00042		FIFO Status Flag Expandable 512x9		
15	PARTINST:BE	3338083412	TP1	A	I-956883884	TP1	TP20	TESTPOINT	60-00012		TESTPOINT		
16	PARTINST:BE	3338083413	P1	A	I-956883883	P1	headx12x45	HEADER12	60-00012		TESTPOINT		
17	PARTINST:BE	3338083414	R2	A	I-956883882	R2	smdres	100	ERJ		RES 100 OHMS		
18	PARTINST:BE	3338083415	R1	A	I-956883881	R1	smdres	100	ERJ		RES 100 OHMS		
19	PARTINST:BE	3338083416	R3	A	I-956883880	R3	res400	10K	ERJ		RES 10K OHMS		

Import & Export Property V1.0

Export | Import

Import File: D:\TestDSN\com_pare\Export_Prop.xls

Get mapping sheet from import file

Part mapping sheet:

Source design: D:\TestDSN\com_pare\BENCH_ALLEGRO_NEW.DSN

PartPin mapping sheet:

Source design:

FlatNet mapping sheet:

Source design:

GraserWARE

Note: Please do not make any change in Capture before closing this dialog.

Design Properties Editor

- [GraserWARE FrontEnd PACK] - Export / Import Properties
 - Import part properties from Excel into Capture schematic design

The screenshot shows the Design Properties Editor window. On the left, a schematic diagram displays two components: U9 (74ALS138) and U11 (22V10). U9 is a 3-to-8 decoder with inputs DSP_A0, DSP_A1, DSP_A2, DSP_IO, DSP_A11, and DSP_A12, and outputs Y0 through Y7. U11 is a 22V10 PLD with various inputs and outputs including CLKOUT, PMS-, BMS-, DSP_RD, DSP_WR, BG-, DSP_A13, DSP_A14, DSP_A15, PC_RESET, and DSP_A11.

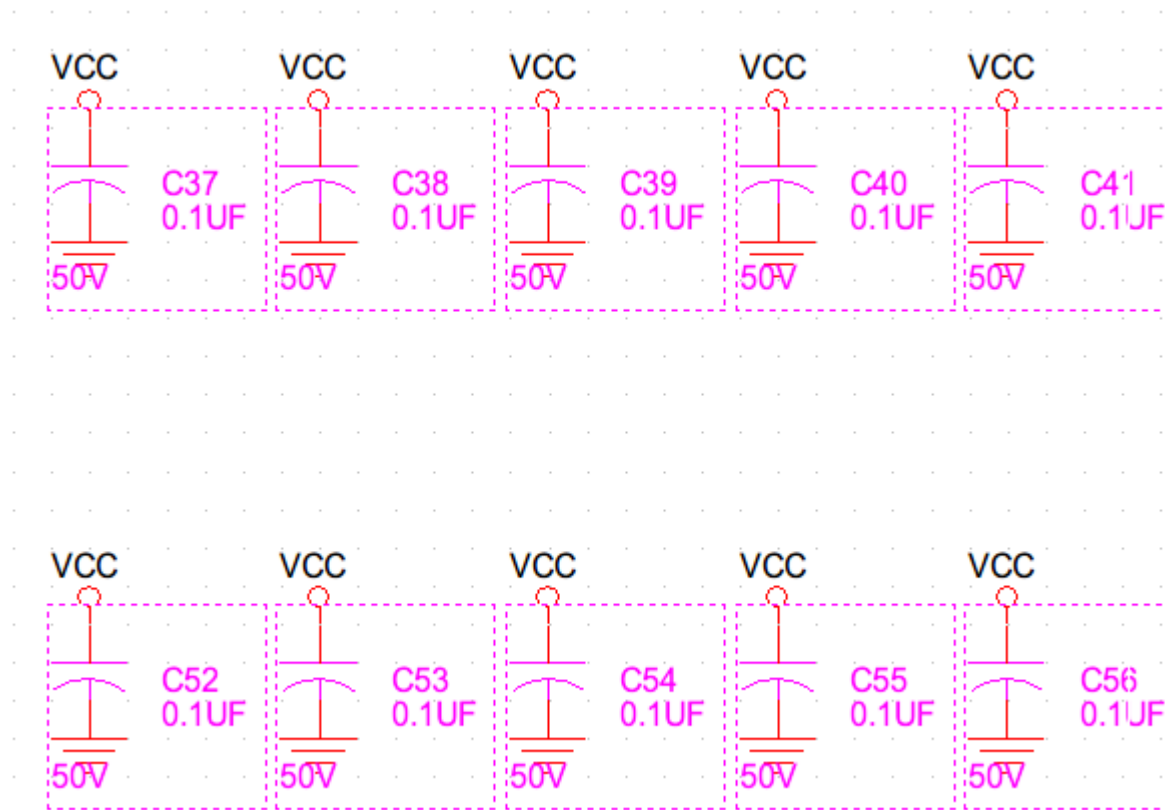
On the right, the Property Editor table shows properties for three instances: BENCH : A : D1, BENCH : A : U9, and BENCH : A : U11. The table includes columns for Tag, Color, Description, Designator, Graphic, ID, Implementation, Implementation Path, Implementation Type, Location X-Coordinate, Location Y-Coordinate, Name, Part Number, Part Reference, PCB Footprint, Power Pins Visible, Primitive, PSpice, Rating, Reference, Source Library, Source Package, Source Part, Tolerance, and Value.

	A	B	C
	BENCH : A : D1	BENCH : A : U9	BENCH : A : U11
Tag			
Color	Default	Default	Default
Description	LED Red	IC, 74ALS138, multi	Bipolar PLD Device
Designator			
Graphic	LED1.Normal	74ALS138.Normal	22V10.Normal
ID			
Implementation	D	74ALS138	
Implementation Path			
Implementation Type	Schematic View	Schematic View	<none>
Location X-Coordinate	1540	710	510
Location Y-Coordinate	850	850	1000
Name	I-956883893	I-956883898	I-956883892
Part Number	40-00017	20-00045	20-00033
Part Reference		U9	U11
PCB Footprint	SMDLED	dip16_3	plcc28
Power Pins Visible		<input type="checkbox"/>	<input type="checkbox"/>
Primitive	YES	YES	YES
PSpice	D	74ALS138	
Rating	2.0V		
Reference	D1	U9	U11
Source Library	C:\WINDOWS\IT	C:\WINDOWS\IT	C:\WINDOWS\IT
Source Package	LED1	74ALS138	22V10
Source Part	LED1.Normal	74ALS138.Normal	22V10.Normal
Tolerance			
Value	RA-LED	74ALS138	22V10

Reference Edit

How to control part reference prefix?

- Traditional
 - Change Part Reference Prefix manually



Reference Edit

[GraserWARE FrontEnd PACK] - Reference Edit

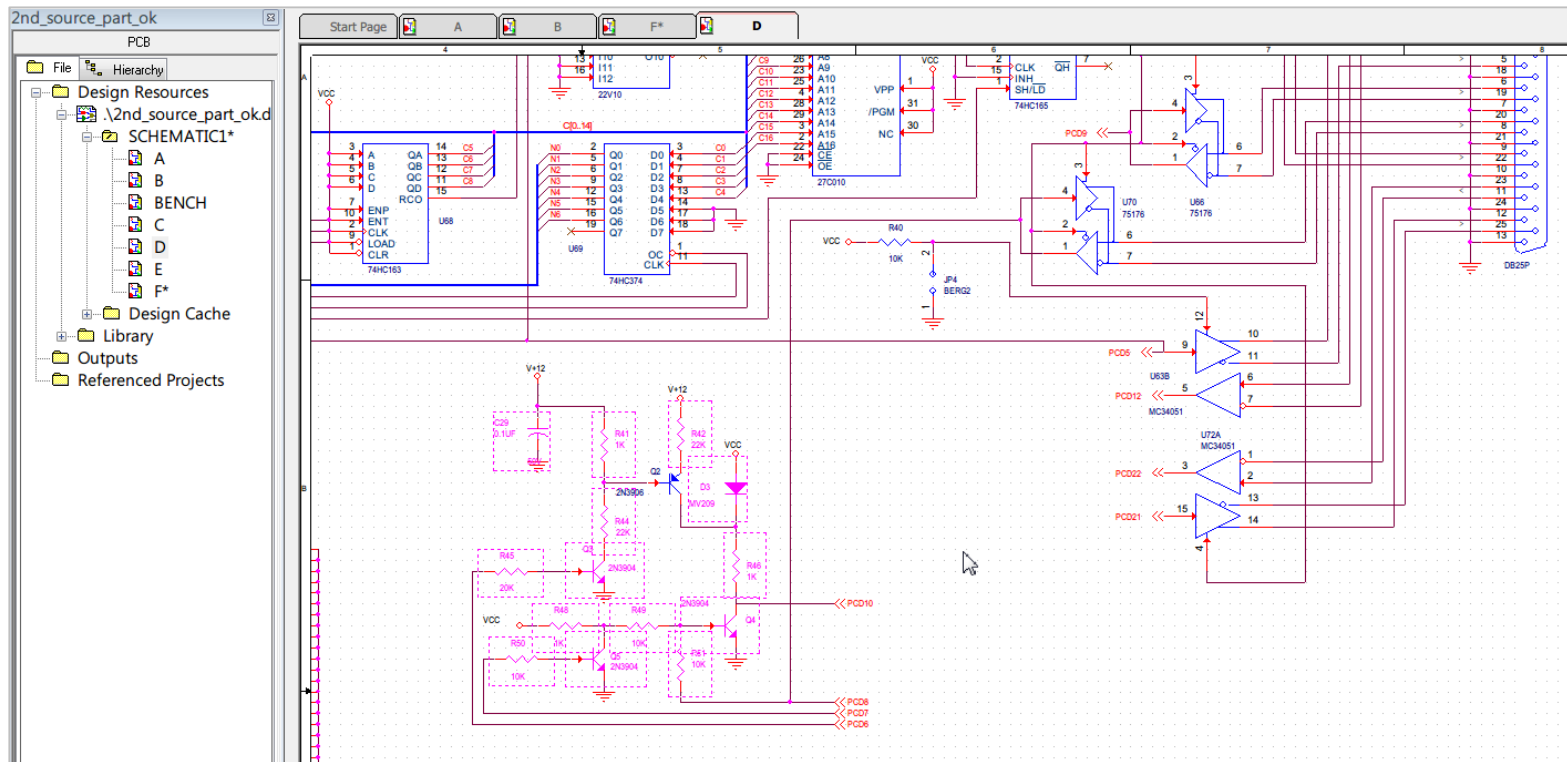
- Scope
 - By Selection, Page and Design
- Modify RefDes
 - Insert, Delete and Modify the Part Reference Prefix

The image shows a PCB layout with two rows of capacitors. Each capacitor is connected to a VCC net and a 50V net. The capacitors are labeled CP37, CP38, CP39, CP40, CP41 in the top row and CP52, CP53, CP54, CP55, CP56 in the bottom row. All capacitors are 0.1UF. The Reference Edit V1.0 dialog box is open, showing the 'Modify RefDes' tab. The 'Scope' section has 'By Selection' selected. The 'Mode' section has 'Update Instance' selected. The 'Action' section has 'Position' set to 'Middle'. The 'RefDes Prefix reset to default' button is visible. The 'Operation' section has 'Insert' selected, and a text box contains the letter 'P'. The 'OK' and 'Close' buttons are at the bottom.

Reference Edit

How to assign RefDes?

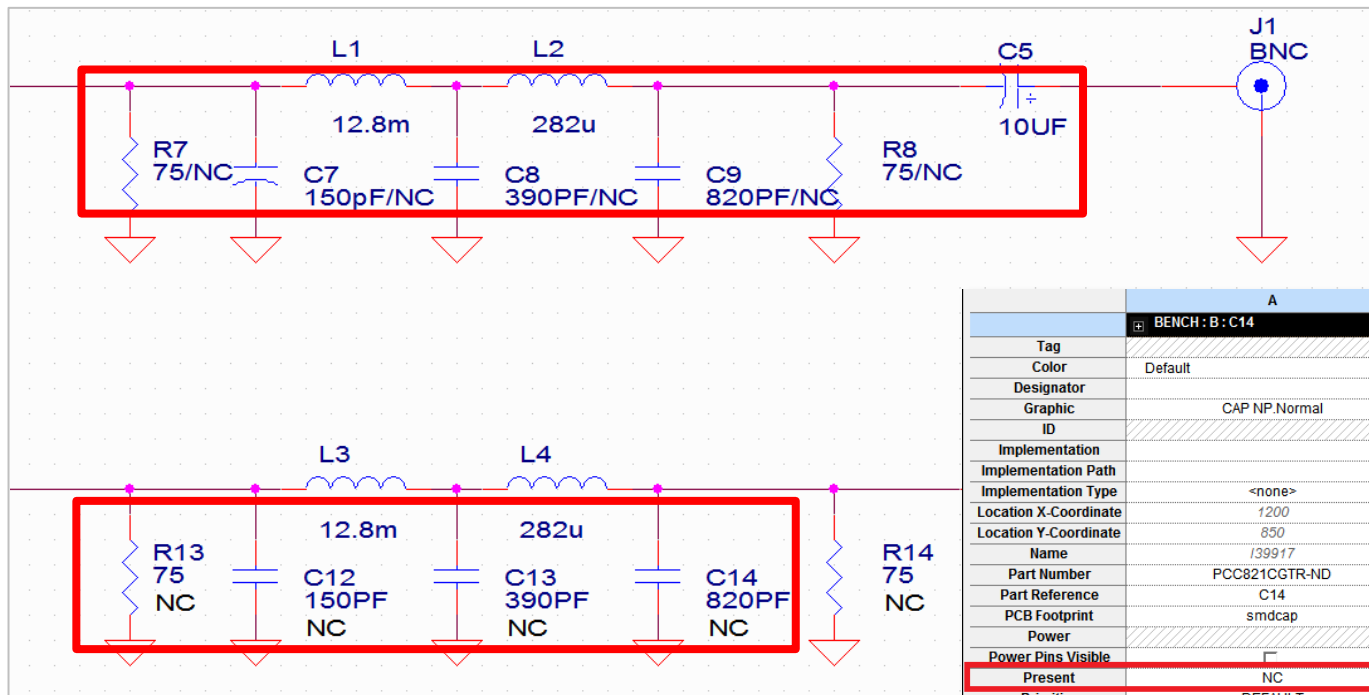
- Traditional
 - Change Part Reference manually



NC Part Setting

How to set parts which are not present?

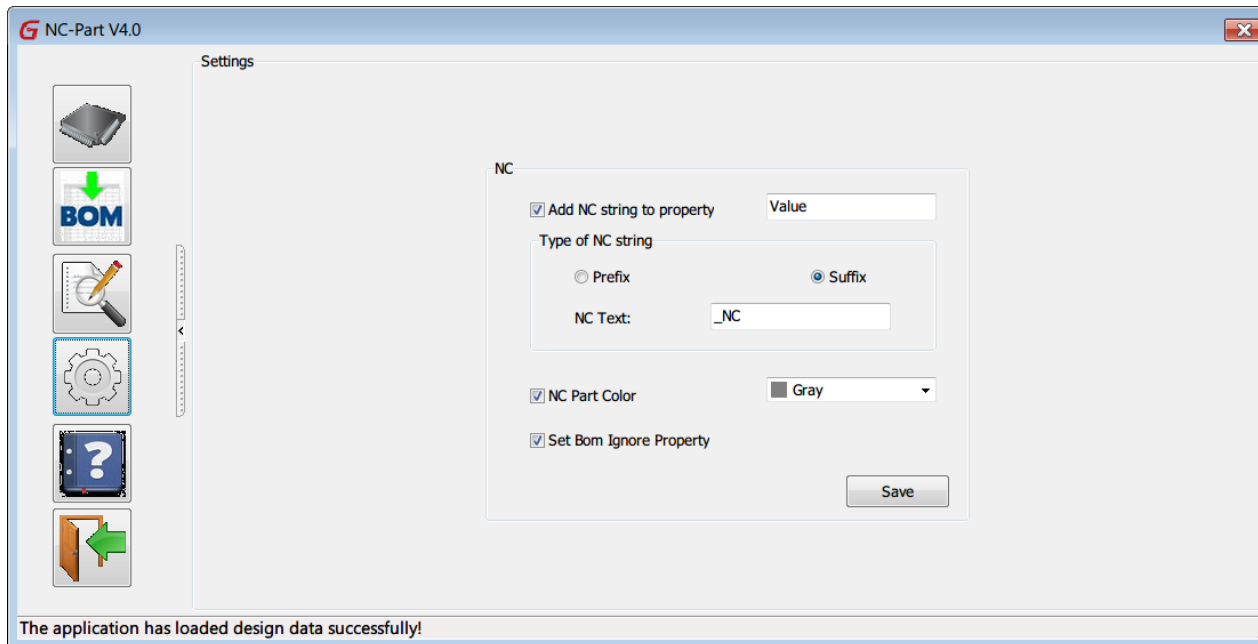
- Traditional
 - Add strings in Value property manually
 - Add a new part property and assign string to display on the page



	A	B
Tag	BENCH : B : C14	BENCH : B : R14
Color	Default	Default
Designator		
Graphic	CAP NP Normal	R.Normal
ID		
Implementation		
Implementation Path		
Implementation Type	<none>	<none>
Location X-Coordinate	1200	1270
Location Y-Coordinate	850	840
Name	I39917	I-956883727
Part Number	PCC821CGTR-ND	ERJ-8GEYJ750V
Part Reference	C14	R14
PCB Footprint	smdcap	smdres
Power		1/8W
Power Pins Visible	<input type="checkbox"/>	<input type="checkbox"/>
Present	NC	NC
Primitive	DEFAULT	YES
PSpice	C	R
Reference	C14	R14
Source Library	D:\ORCAD\WINV9\CAPTURE\LIBRARY1	C:\WINDOWS\TEMP\XP\LTEMP\OLB
Source Package	CAP NP	R

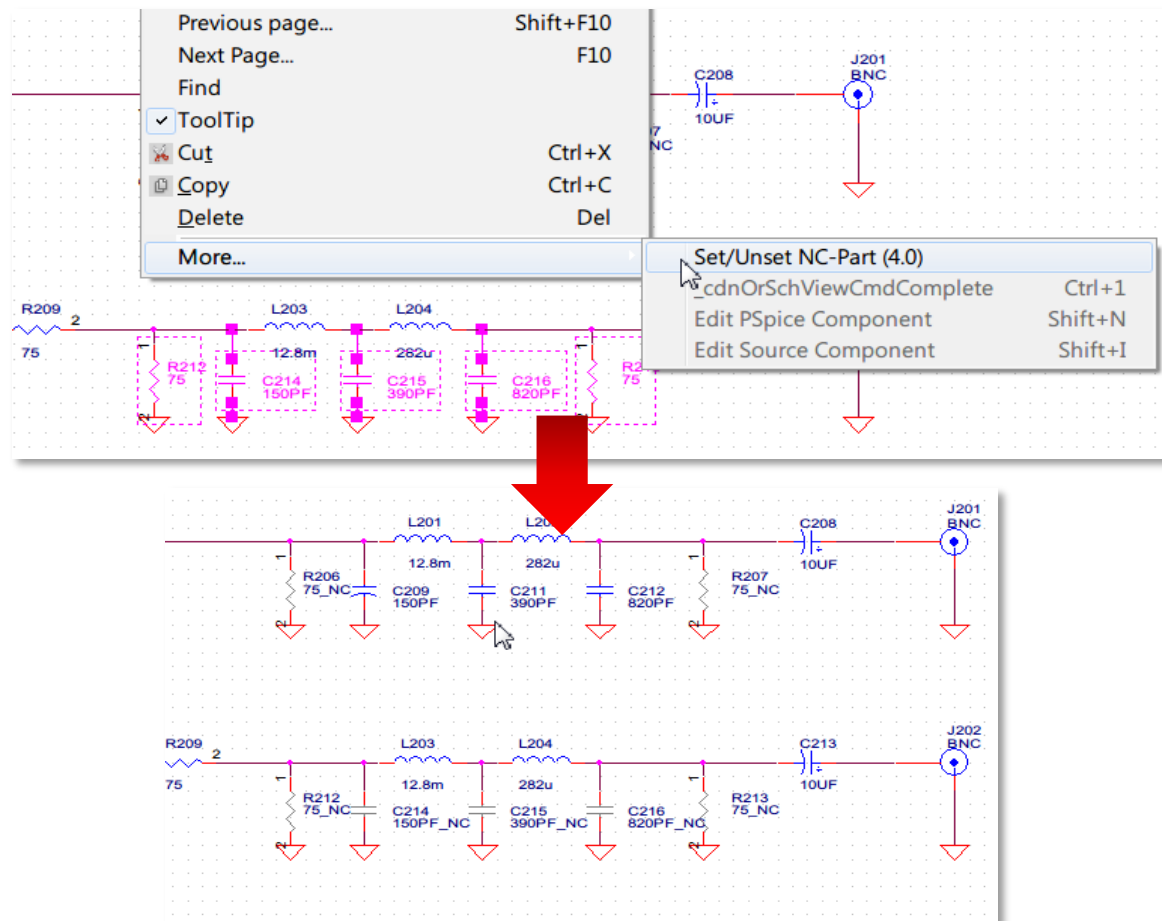
NC Part Setting

- [GraserWARE FrontEnd PACK] - NC Part
 - Add NC string in value property
 - Add BOM_IGNORE property
 - Change NC part color
 - New BOM Export
 - Filter NC Parts and put it on NC Parts section



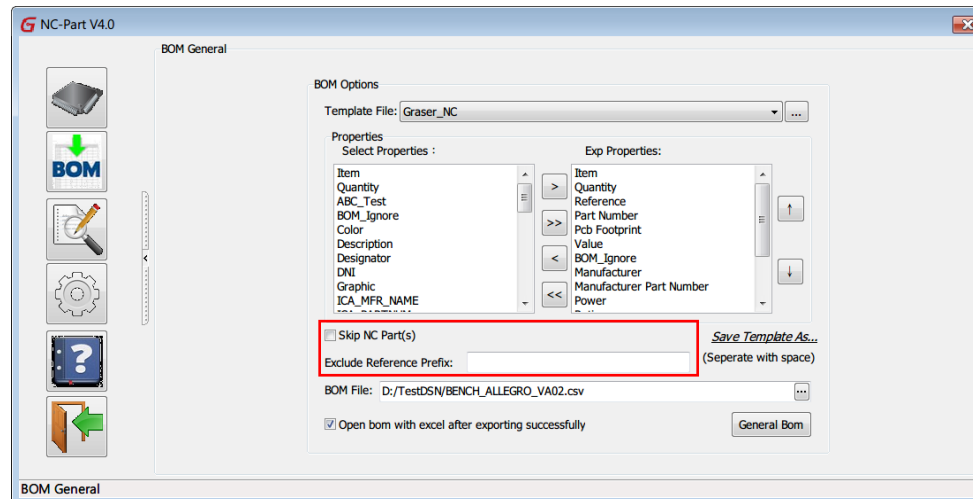
NC Part Setting

- [GraserWARE FrontEnd PACK] - NC Part
 - Easy to set / unset NC Part



NC Part Setting

- [GraserWARE FrontEnd PACK] - NC Part
 - Generate BOM
 - Set part properties in BOM
 - Filter NC Parts and put it on NC Parts section



A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
Standard Part List														
Item	Quantity	Reference	Part Num	Pcb Footp	Value	BOM_Ign	Manuact	Manuact	Power	Rating	Source Pa	Tolerance	Voltage	
115	1	Y201	20-00442		10MHz						CRYSTAL	Normal		
116	1	Y401	20-00443	dip14_3	24.576MHz						OSCR	Normal		
117	1	Y402	20-00444		4.9152MHz						CRYSTAL	Normal		
118	1	Y601	20-00445		3.6864MHz						CRYSTAL	Normal		
NC-Part List														
1	1	C214	PCC151C	smdcap	150PF_NC	TRUE							CAPACITOR NON-	50V
2	1	C215	PCC391B	smdcap	390PF_NC	TRUE							CAPACITOR NON-	50V
3	1	C216	PCC821C	smdcap	820PF_NC	TRUE							CAP NP.Normal	50V
4	2	R212,R21	ERJ-8GE	smdres	75_NC	TRUE			1/8W				R_0.Norm	5%

Part Information Check



- [GraserWARE FrontEnd PACK] – Part Utility
 - Part Information Check
 - Difference with CIS Database
 - Part EOL or EOD
 - Part Number was not found

Part Utility V1.2

Parts Information

Sl.	Referenc	Part Number	Value	Description	Voltage	Tolerance	Source Package	PCB Footprint	Part Approve	Schematic Part	Power
1	C1	PCC100CQTR-ND	10PF	CAP 10PF 50V CER	50V		SMALL CAP	smdcap	YES		
2	C2	PCC100CQTR-ND	10PF	CAP 10PF 50V CER	50V		SMALL CAP	smdcap	YES		
3	C3	PCC220CNTR-ND	22PF	22PF 50V CERAMIC	50V		SMALL CAP	smdcap	EOL		
4	C4	PCC220CNTR-ND	22PF	22PF 50V CERAMIC	50V		SMALL CAP	smdcap	EOL		
5	C5	ECE-V1HA100SP	10UF	CAP 10UF 50V VS I	50V		CP		YES		
6	C6	ECG-C0JB100R	10UF	CAP 10UF 6.3V CB	6.3V		CAP		YES		
7	C7	PCC151CGTR-ND	150PF	150PF 50V CERAM	50V		C	smdcap	EOD		
8	C8	PCC391BNTR-ND	390PF	390PF 50V CERAM	50V		CAPACITOR NON-P	smdcap	YES		
9	C9	PCC821CGTR-ND	820PF	820PF 50V CERAM	50V		CAP NP	smdcap			
10	C10	ECE-V1HA100SP	10UF	CAP 10UF 50V VS I	50V		CP		YES		
11	C11	ECE-B1HGE0R1	0.1UF	CAP 50V .1UF NHE	50V		CAP	smdcap	NO		
12	C12	PCC151CGTR-ND	150PF	150PF 50V CERAM	50V		CAPACITOR NON-P	smdcap	EOD		
13	C13	PCC391BNTR-ND	390PF	390PF 50V CERAM	50V		CAPACITOR NON-P	smdcap	YES		
14	C14	PCC821CGTR-ND	820PF	820PF 50V CERAM	50V		CAP NP	smdcap			
15	C15	ECE-V1HA100SP	10UF	CAP 10UF 50V VS I	50V		CP		YES		
16	C16	ECE-A50ZR1	0.1UF	.1UFD @ 50VDC P	50V		CAP	smdcap	YES		
17	C17	PCC151CGTR-ND	150PF	150PF 50V CERAM	50V		CAPACITOR NON-P	smdcap	EOD		
18	C18	PCC391BNTR-ND	390PF	390PF 50V CERAM	50V		CAPACITOR NON-P	smdcap	YES		
19	C19	PCC821CGTR-ND	820PF	820PF 50V CERAM	50V		CAP NP	smdcap			
20	C20	PCC100CQTR-ND	10PF	CAP 10PF 50V CER	50V		SMALL CAP	smdcap	YES		
21	C21	PCC100CQTR-ND	10PF	CAP 10PF 50V CER	50V		SMALL CAP	smdcap	YES		

Buttons: Compare With DB, 2nd Source Information

Selected Part Compare With DB

<No data to display>

Buttons: Load Dsn Data, Check

Ctrl + Click to locate the part in page

Part Information Check

- [GraserWARE FrontEnd PACK] – Part Utility
 - Generate BOM
 - User define properties
 - Generate to Excel
 - Skip NC Parts

The screenshot shows the '2nd Part Utility V1.5' application window. On the left, there are icons for file operations and settings. The main area is divided into 'Export Options' and 'Selected Properties'. The 'Export Options' section includes a 'Template' dropdown set to 'Graser', a list of 'All Properties' (such as ICA_PARTNUM, ID, Implementation, etc.), and a 'Selected Properties' list (including Item, Quantity, Part Number, Reference, Value, and PCB Footprint). There are also checkboxes for 'Skip NC Part(s)' and 'Open with'. The 'Export File Name' field is empty. At the bottom, a status bar indicates 'The application is processing second source information: 100%'.

Overlaid on the application is an Excel spreadsheet titled '2nd_NC2.xls'. The spreadsheet contains the following data:

Item	Quantity	Part Number	Reference	Description/Manufacturer	Part Approve
1	10	20-000244	U39	IC, 74HC24:Fairchild Ser MM74HC24	YES
2	11	20-00091		IC, 74HC57:Fairchild Ser MM74HC57	YES
3	12	20-00133		IC, 74S133 :Fairchild Ser DM74S133N	YES
4	13	20-003297		IC, 74ALS2:Fairchild Ser MM74HC24	YES
5	20	8 20-00042	U3,U6,U21	FIFO Status Advanced M 7201	YES
6	30	5 20-00062	U1,U2,U4	UCMOS Static Mosel Vitelic MS6264L	YES
7	40	1 20-00067	U12	SCSI Temir Dallas Semic DS2105	YES
8	41	20-00094		High Perform:Advanced MAM53C94	YES
9	42	21-87201		Standard Hig Texas Instru PAL16L8A1	NO
10	50	1 20-00091	U36	IC, 74HC57:Fairchild Ser MM74HC57	YES
11	60	1 20-00094	U72	High Perform:Advanced MAM53C94	YES
12	70	1 20-00133	U43	IC, 74S133 :Fairchild Ser DM74S133N	YES
13	80	6 20-00141	U40,U41,U4	IC 8-CH DA Toshiba TD62081AF	YES
14	90	3 20-00163	U63,U67,U6	IC, 74HC16:Fairchild Ser MM74HC16	YES
15	100	1 20-00165	U60	IC, 74HC16:Fairchild Ser MM74HC16	YES
16	110	2 20-00176	U65,U70	IC, RS485/R National Sen DS75176BN	YES
17	120	1 20-003101	U44	24-Bit Digitz Motorola DSP56001	YES

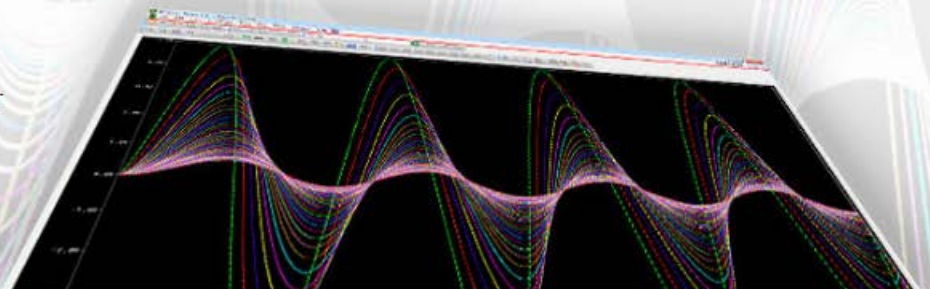
OrCAD Pspice 模擬與驗證

What's OrCAD PSpice Designer

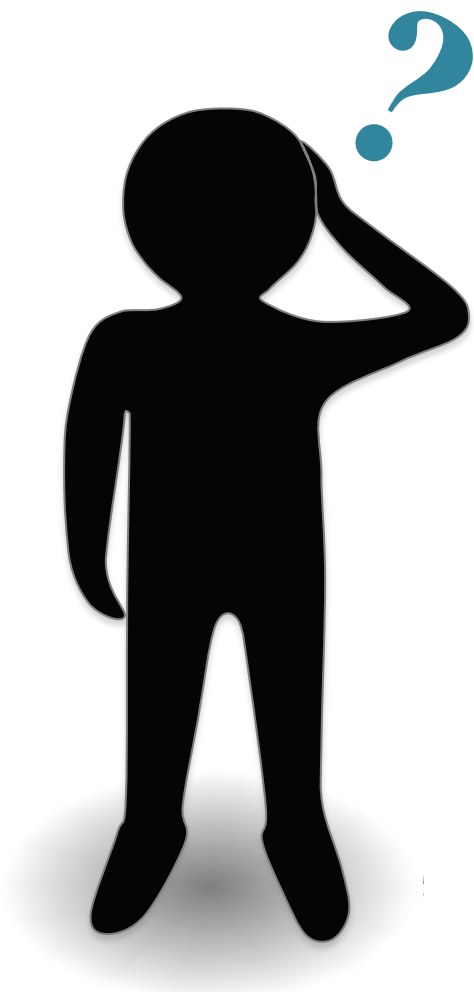
- OrCAD[®] PSpice[®] and Advanced Analysis技術可對類比電路、混合信號模擬和分析，提供完整驗證解決方案。OrCAD PSpice在系統級的電路模擬驗證設計良率和可靠性，提供最佳的方案。

OrCAD PSpice Designer

Advanced circuit simulation and analysis for analog and mixed-signal circuits



Challenges



減少錯誤

提高可靠性

模型開發

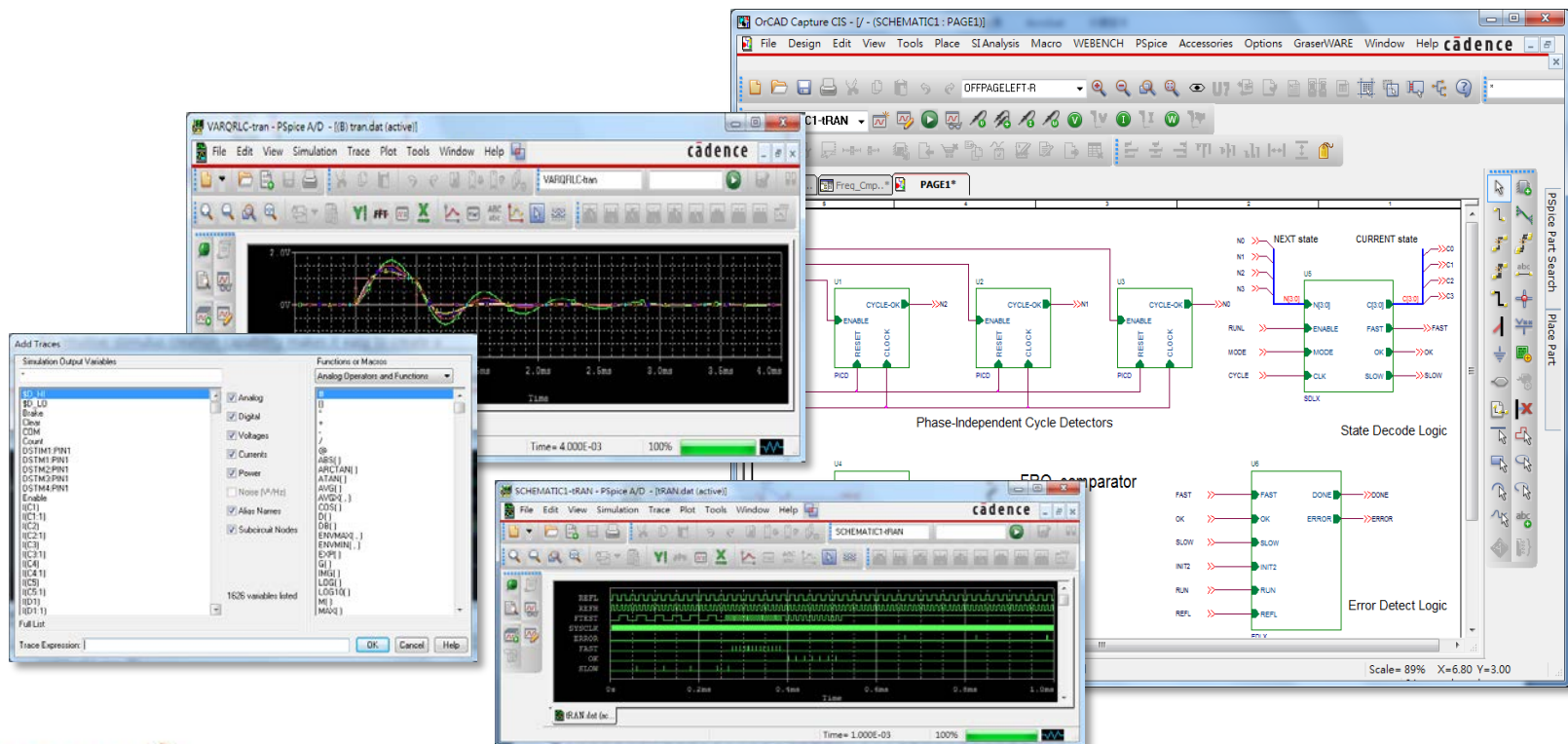
提高設計效率

OrCAD PSpice



- Mixed-signal simulator**

- Full integration with OrCAD® Capture improve productivity and data integrity.
- Powerful waveform viewing and post-processing expression support speed review and analysis without having to rerun simulations.



OrCAD PSpice

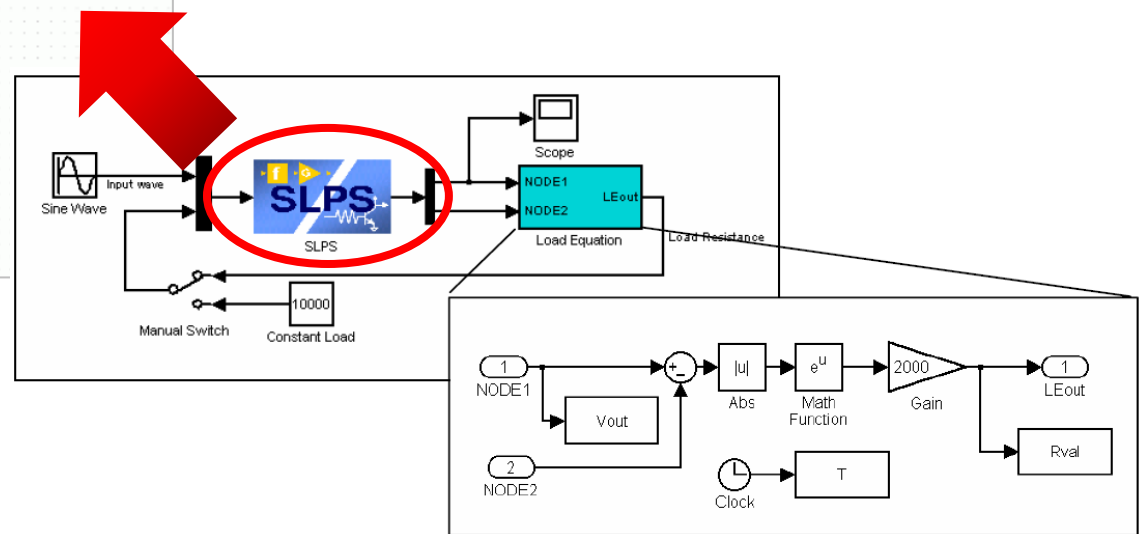
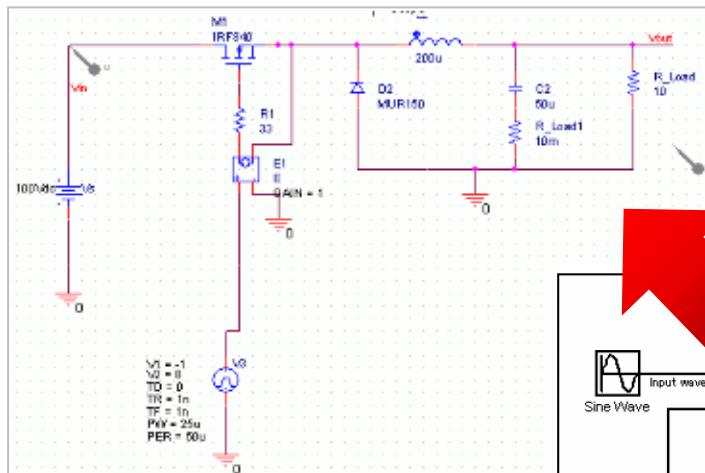


- **Mixed-signal simulator**

- Multi-vendor models, built-in mathematical functions, and behavioral modeling techniques.
- Support multi-modeling type,
 - Algorithmic Models: Matlab/C/C++
 - System Models: SystemC
 - Digital Models with IO/Timing/Constraint
 - Digital Function Model
 - Verilog-A
 - PSpice Behavioral Models

OrCAD PSpice Mixed Domain Integration

- OrCAD PSpice w/ MATLAB
 - Systems Simulation
 - Integration with MATLAB Simulink brings two industry-leading simulation tools, electromechanical systems & electrical, in a co-simulation environment.



PSpice 進階分析功能



- Combine OrCAD[®] PSpice[®] A/D functionality with the powerful Advanced Analysis environment.

The image displays several key analysis windows from the PSpice Advanced Analysis environment:

- Current Plot 2.txt:** A line graph showing multiple signal traces over time.
- Probability Density Graph (Runs: 1 to 100):** A histogram showing the distribution of a parameter, with the x-axis labeled 'Bandwidth(V(LOAD),3)'.
- Statistical Information:** A table summarizing statistical data for various components.

Component	Parameter	Original	(Min)	(Max)	Ref Sensitivity	Linear
R4	VALUE	240	235	244	50.777%	66
R5	VALUE	50	55	45	-44.1907%	66
R6	VALUE	50	45	55	37.0312%	72
R7	VALUE	600	740	812	-24.4919%	67
R8	VALUE	3.6000	3.6000	3.2400	-21.2027%	41
R3	VALUE	6.0000	7.40	8.12	-16.5815%	32
R2	VALUE	30	270	1330	15.0576%	33
R7	VALUE	200	243	287	6.4396%	13
R1	VALUE	240	21.6	26.4	60.0041%	<180>
- Optimizer:** A window for parameter optimization, including an 'Error Graph' showing error percentage over run numbers and a 'Parameters (Best Run)' table.

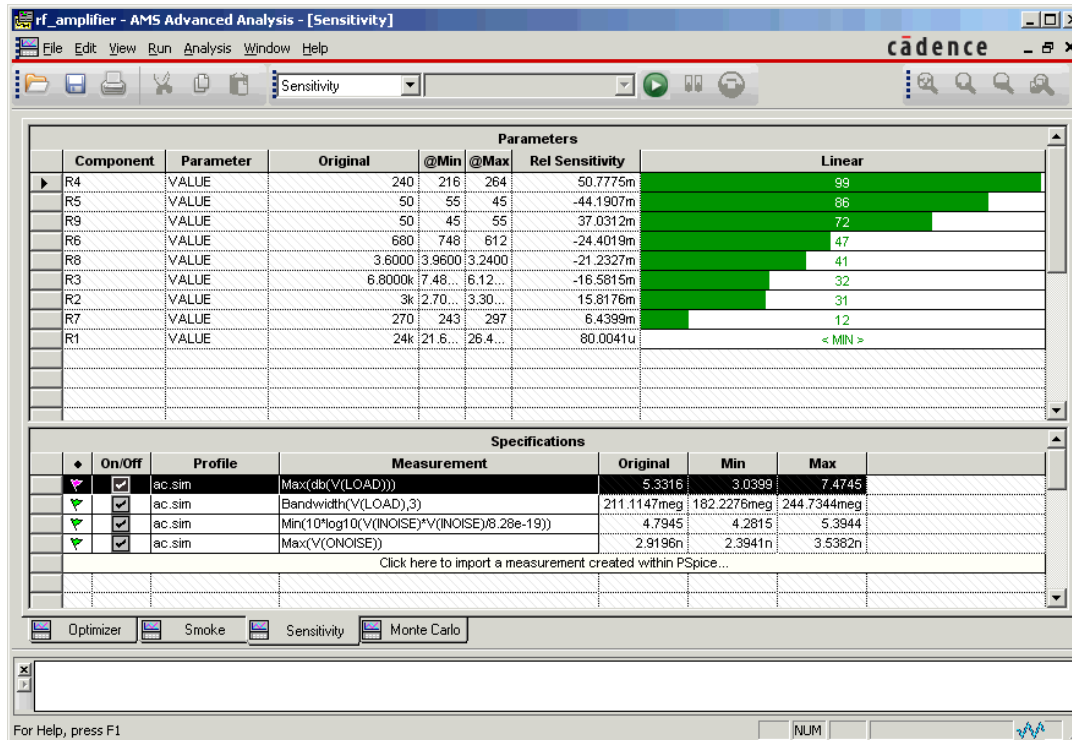
Component	Parameter	Discrete Table	Original	Min	Max	Current
R4	VALUE	Resistor - 10%	470	225	705	240
R5	VALUE	Resistor - 10%	3.3000	3	3.6000	3.6000
R6	VALUE	Resistor - 10%	470	225	705	680
- Waveform Viewer:** A plot showing a signal over time with a 100us scale bar.
- Statistical Summary Table:**

Component	Cursor Min	Cursor Max	Yield	Mean	Std Dev	3 Sigma
Current	8.3843	10.3501	100%	9.1949	425.3143m	100%
1138.8675mg	162.2345mg	100%	150.6752mg	4.7023mg	100%	
DI5EJ6.20e-19j	3.7933	4.5568	100%	4.1528	179.7151m	100%
	3.8853m	4.7339m	100%	4.3330m	201.3021p	100%
- Component Summary Table:**

Component	Parameter	Type	Breaks - %	Max Exceeds	Convergence Error	% Max
V1	V1Z	Average	12	50	3	91.27%
V2	V2Z	Average	12	50	3	91.42%
V3	V3Z	Average	12	50	3	91.29%
V4	V4Z	Average	12	50	3	91.29%
V5	V5Z	Average	12	50	3	91.29%
V6	V6Z	Average	12	50	3	91.29%
V7	V7Z	Average	12	50	3	91.29%
V8	V8Z	Average	12	50	3	91.29%
V9	V9Z	Average	12	50	3	91.29%
V10	V10Z	Average	12	50	3	91.29%
V11	V11Z	Average	12	50	3	91.29%
V12	V12Z	Average	12	50	3	91.29%
V13	V13Z	Average	12	50	3	91.29%
V14	V14Z	Average	12	50	3	91.29%
V15	V15Z	Average	12	50	3	91.29%
V16	V16Z	Average	12	50	3	91.29%
V17	V17Z	Average	12	50	3	91.29%
V18	V18Z	Average	12	50	3	91.29%
V19	V19Z	Average	12	50	3	91.29%
V20	V20Z	Average	12	50	3	91.29%
V21	V21Z	Average	12	50	3	91.29%
V22	V22Z	Average	12	50	3	91.29%
V23	V23Z	Average	12	50	3	91.29%
V24	V24Z	Average	12	50	3	91.29%
V25	V25Z	Average	12	50	3	91.29%
V26	V26Z	Average	12	50	3	91.29%
V27	V27Z	Average	12	50	3	91.29%
V28	V28Z	Average	12	50	3	91.29%
V29	V29Z	Average	12	50	3	91.29%
V30	V30Z	Average	12	50	3	91.29%
V31	V31Z	Average	12	50	3	91.29%
V32	V32Z	Average	12	50	3	91.29%
V33	V33Z	Average	12	50	3	91.29%
V34	V34Z	Average	12	50	3	91.29%
V35	V35Z	Average	12	50	3	91.29%
V36	V36Z	Average	12	50	3	91.29%
V37	V37Z	Average	12	50	3	91.29%
V38	V38Z	Average	12	50	3	91.29%
V39	V39Z	Average	12	50	3	91.29%
V40	V40Z	Average	12	50	3	91.29%
V41	V41Z	Average	12	50	3	91.29%
V42	V42Z	Average	12	50	3	91.29%
V43	V43Z	Average	12	50	3	91.29%
V44	V44Z	Average	12	50	3	91.29%
V45	V45Z	Average	12	50	3	91.29%
V46	V46Z	Average	12	50	3	91.29%
V47	V47Z	Average	12	50	3	91.29%
V48	V48Z	Average	12	50	3	91.29%
V49	V49Z	Average	12	50	3	91.29%
V50	V50Z	Average	12	50	3	91.29%
V51	V51Z	Average	12	50	3	91.29%
V52	V52Z	Average	12	50	3	91.29%
V53	V53Z	Average	12	50	3	91.29%
V54	V54Z	Average	12	50	3	91.29%
V55	V55Z	Average	12	50	3	91.29%
V56	V56Z	Average	12	50	3	91.29%
V57	V57Z	Average	12	50	3	91.29%
V58	V58Z	Average	12	50	3	91.29%
V59	V59Z	Average	12	50	3	91.29%
V60	V60Z	Average	12	50	3	91.29%

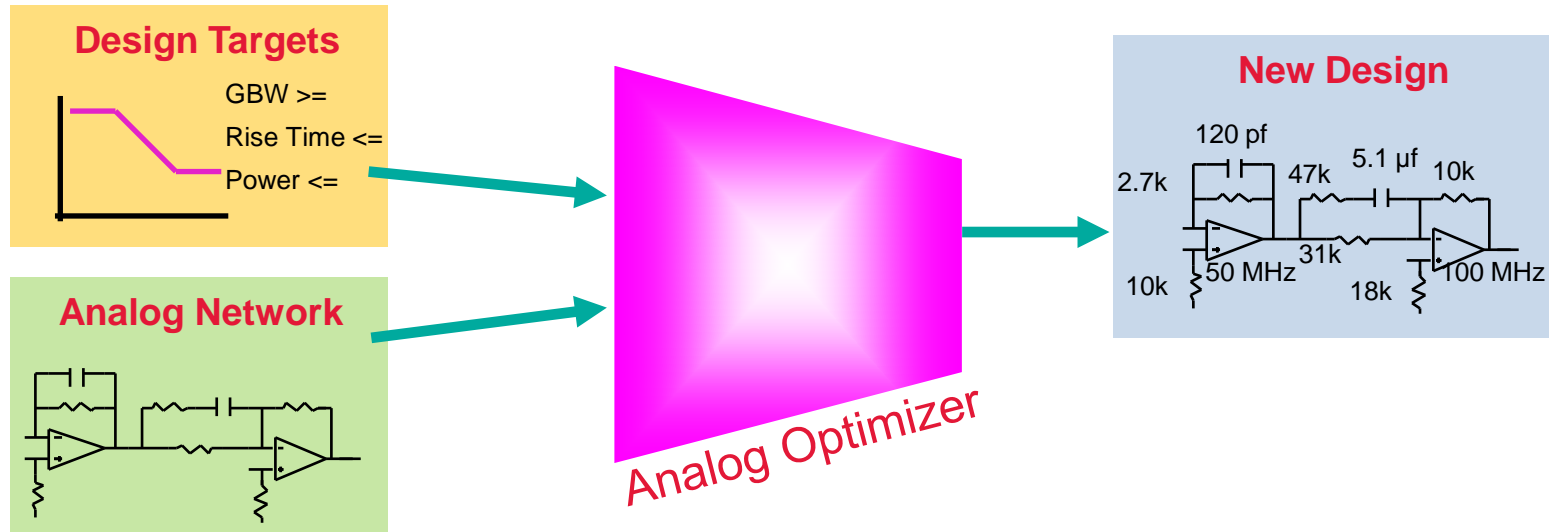
靈敏度分析

- **Easily identify** components impacting key circuit goals and specs.
- **Estimate worst case** performance of the circuit given the device tolerances.
- Identify components whose tolerance does not matter.
 - **Reduce cost** by choosing components with relaxed tolerance.



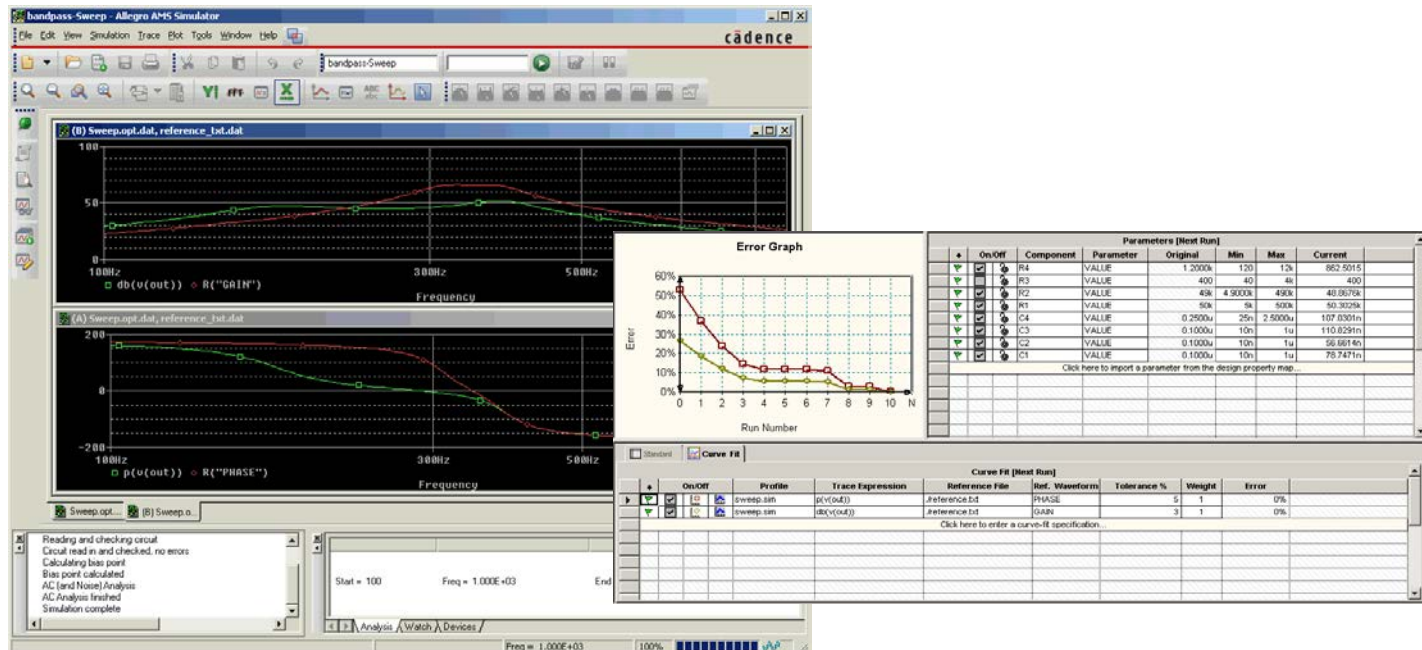
電路最佳化

- Engineer specifies the Circuit Topology and the desired goals.
- **Optimizer does the rest.** It calculates the optimum component values to use to meet the desired goals.
 - One of the **most powerful** analysis tool.
 - Identify components impacting key circuit goals.
 - Identify designs goals and **optimize your design** to meet/beat these goals.
 - Design goals examples: Gain, BW, Overshoot, Pd, Ripple.
 - Design goals can be described as a waveform or Specification.



電路最佳化

- **Finds optimum combination of component values;** automatically simulates, evaluates results, and adjusts component values to reach performance requirements.
- Can be used to retarget an existing design at new goals.
 - To meet requirements of newer circuits.
 - To meet regional requirements.
- **Saves time** for engineers by taking over the often “mindless” task of final optimization
- Can **optimize a set of goal functions** and/or a set of curves.



零件應力分析

- Check components to see if they are approaching or exceeding their recommended **safe operating limits**.
- Allow users to **specify their own derating criteria** to ensure components are not stressed, or exceed safe operating limits.
- **Determine a part's performance under various stresses** and environmental conditions.
- Help in **thermal design** aspect of electronics circuit.
- Calculate **Peak**, **Avg.** and **RMS** power.
- **Cross-probe** to automatically find listed parts in the **schematic**.

Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
XG1	VCE	Average	12	50	6	8.1262	136
XG1	VCE	Peak	12	50	6	8.1422	136
XG1	VCE	RMS	12	50	6	8.1262	136
XG1	PDM	Peak	197.7143m	75	148.2857m	77.7472m	53
XG1	PDM	Average	197.7143m	75	148.2857m	74.7306m	38
XG1	PDM	RMS	197.7143m	75	148.2857m	74.7607m	38
XG1	TJ	Peak	200	100	200	95.0289	48
XG1	TJ	Average	200	100	200	92.9892	47
XG1	TJ	RMS	200	100	200	92.4156	47
R6	PDM	Average	250m	38	96.6888m	40.4885m	42
R6	PDM	Peak	250m	38	96.6888m	40.4885m	42
R6	PDM	RMS	250m	38	96.6888m	40.4885m	42
XG2	VCE	Average	40	50	20	7.6077	39
XG2	VCE	Peak	40	50	20	7.6077	39
XG2	VCE	RMS	40	50	20	7.6077	39
XG1	VCB	Average	20	100	20	7.3391	37
XG1	VCB	Peak	20	100	20	7.3569	37
XG1	VCB	RMS	20	100	20	7.3392	37
XG1	VEB	RMS	2.5000	100	2.5000	797.0463m	32
R6	TB	Average	200	100	200	59.3908	30
R6	TB	Peak	200	100	200	59.3908	30
R6	TB	RMS	200	100	200	59.3908	30
XG1	IC	Peak	50m	80	40m	9.5771m	24
C4	CV	Average	50	90	45	10.6377	24
C4	CV	Peak	50	90	45	10.6377	24
C4	CV	RMS	50	90	45	10.6377	24
XG1	IC	Average	50m	80	40m	9.1877m	23
XG1	IC	RMS	50m	80	40m	9.1918m	23

參數調變分析

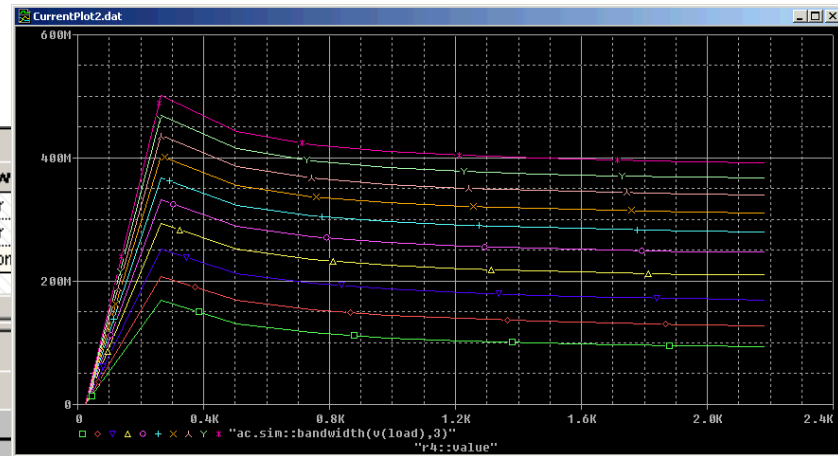
- **Sweep** multiple (nested) parameters.
- Quickly view results and create families of curves.
- **Ensure** there is **no unusual circuit behavior** while sweeping the component values.

Sweep Parameters					
	On/Off	Component	Parameter	Sweep Variable	Sw
▼	☑	r6	value	outer	Linear
▶	☑	r4	value	inner1	Linear

Click here to import a parameter from

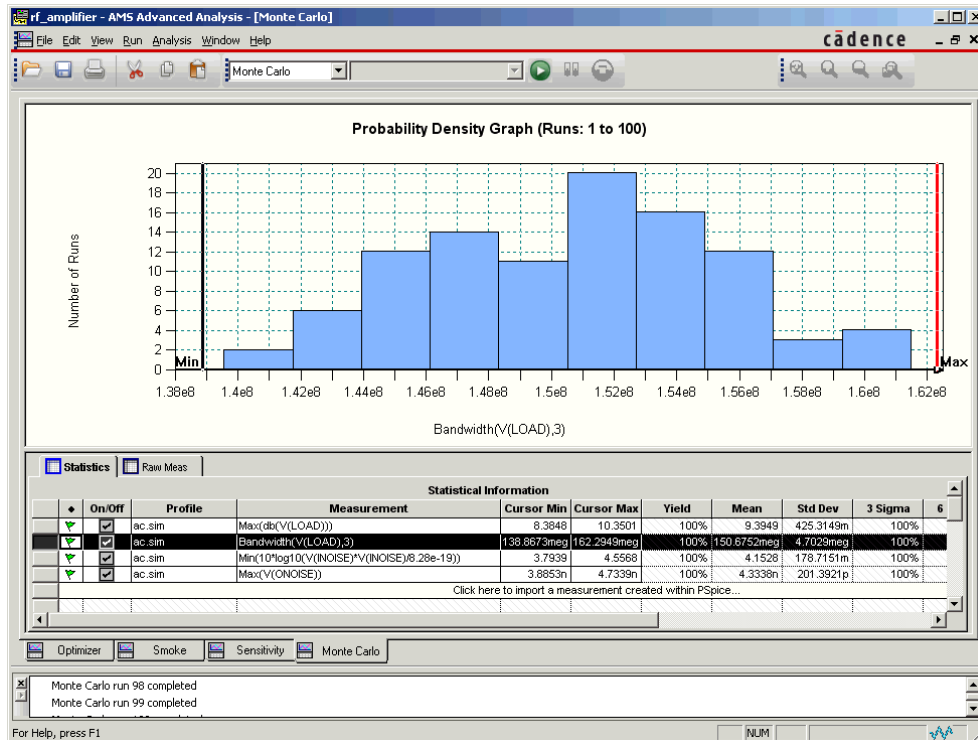
Measurements Results Plot Information

Results		
r6::value	r4::value	
68	24	29308.69938494
68	264	169223297.0415
68	504	131396166.6086
68	744	116343959.5654
68	984	108319360.2365
68	1224	103295419.1038
68	1464	99839677.09986



蒙地卡羅分析

- Calculate Yield before going into manufacturing.
- Produce circuit performance statistics due to device variations.
- Set specification minimum and maximum, and estimate production yield before going to production.
- View graphical results as **probability density histogram**, or as **cumulative distribution function**.



OrCAD PSpice Advanced Analyses



- Help customers to optimize their design while maintaining their cost and yield.

OrCAD® PSpice® Advanced Analyses

成本

靈敏度分析

效率

最佳化分析

預測

調變分析

可靠性

零件應力分析

良率

蒙地卡羅分析