全新OrCAD 2015 SPB Seminar

不僅僅只有電路設計

The New OrCAD is NOT only the Circuit Design

Constructed PCB Layout & ERC／SRC Check
完善的電路板佈局和電性檢查

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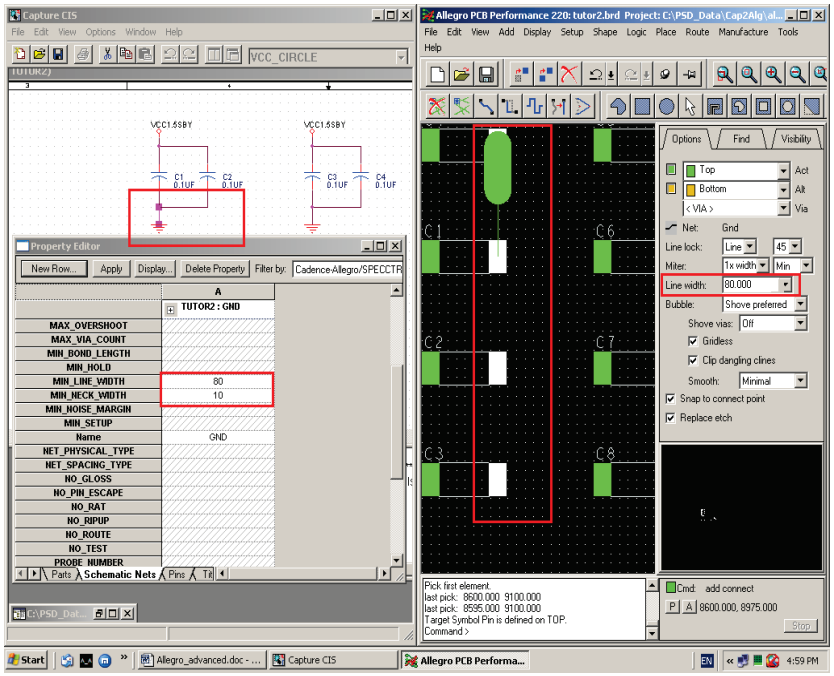
Graser® cādence® CHANNEL PARTNER

The Integration of Capture and PCB Designer

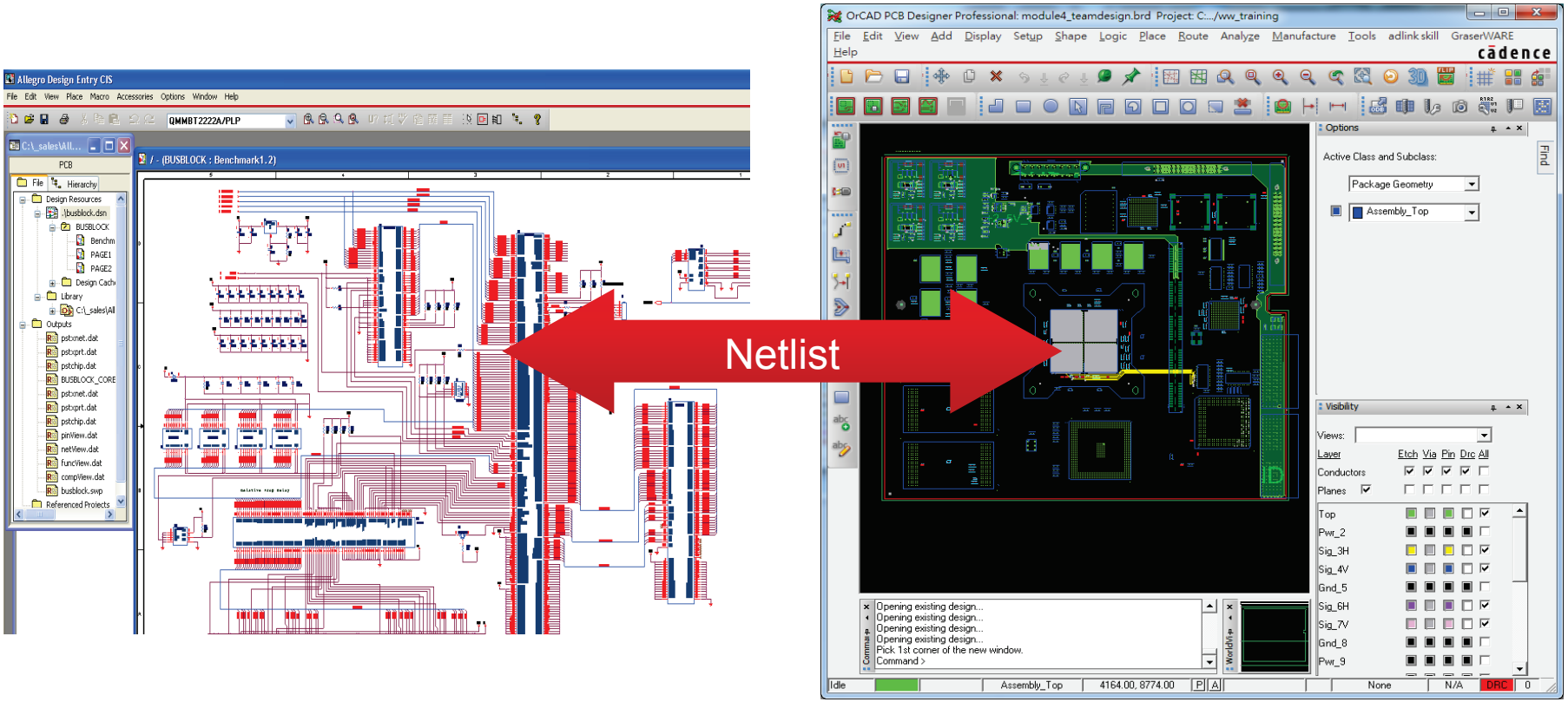
- Capture to OrCAD PCB：
  - 簡潔明瞭的介面方便使用者設定和查看 Constraint。與Capture的結合讓E.E.電子工程師在設計電路線路圖時，把設定好的規則資料一起帶到PCB Layout工作環境中，於Placement及Routing時依規則處理，且這些規則資料的經驗值均可重覆使用在相同性質的PCB設計上。

Capture v.s. PCB Designer



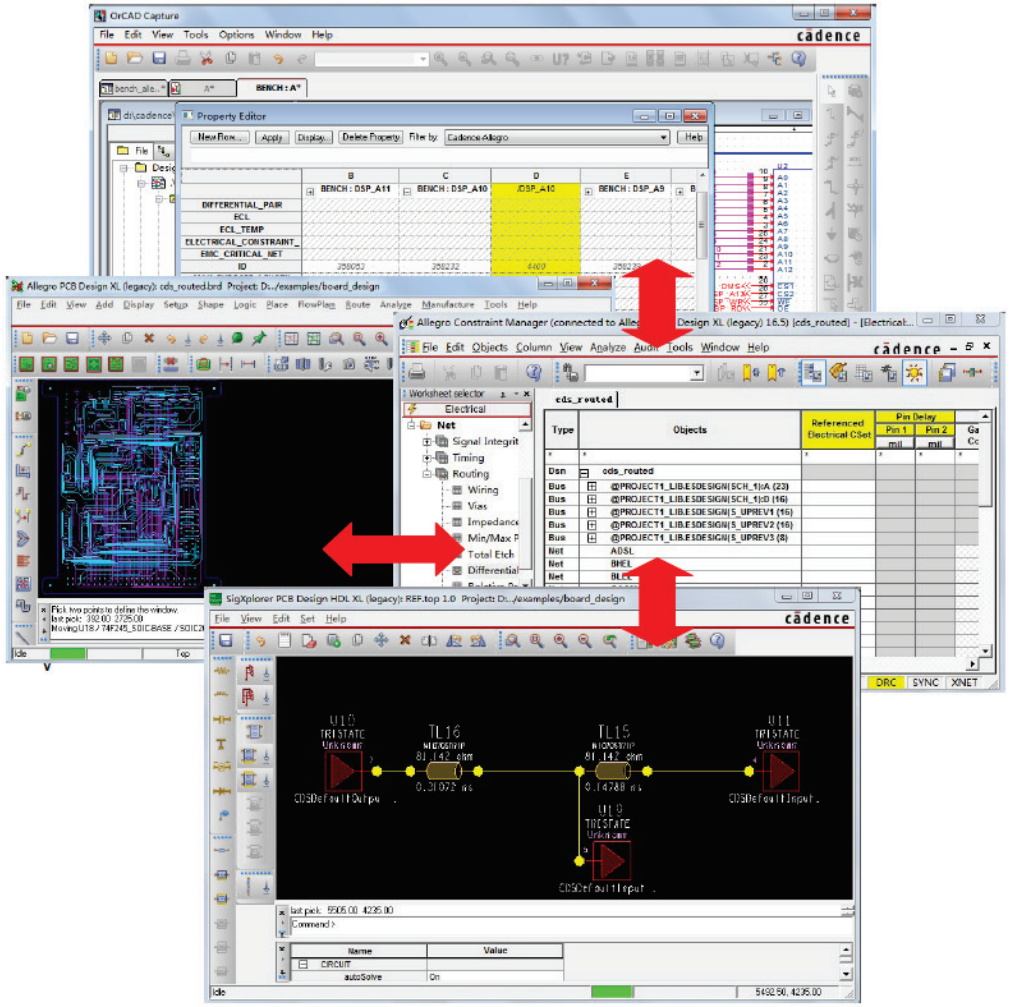
Front to Back Flow

- Netlist is Enough?!
  How about Rules／Guideline & Design Intend

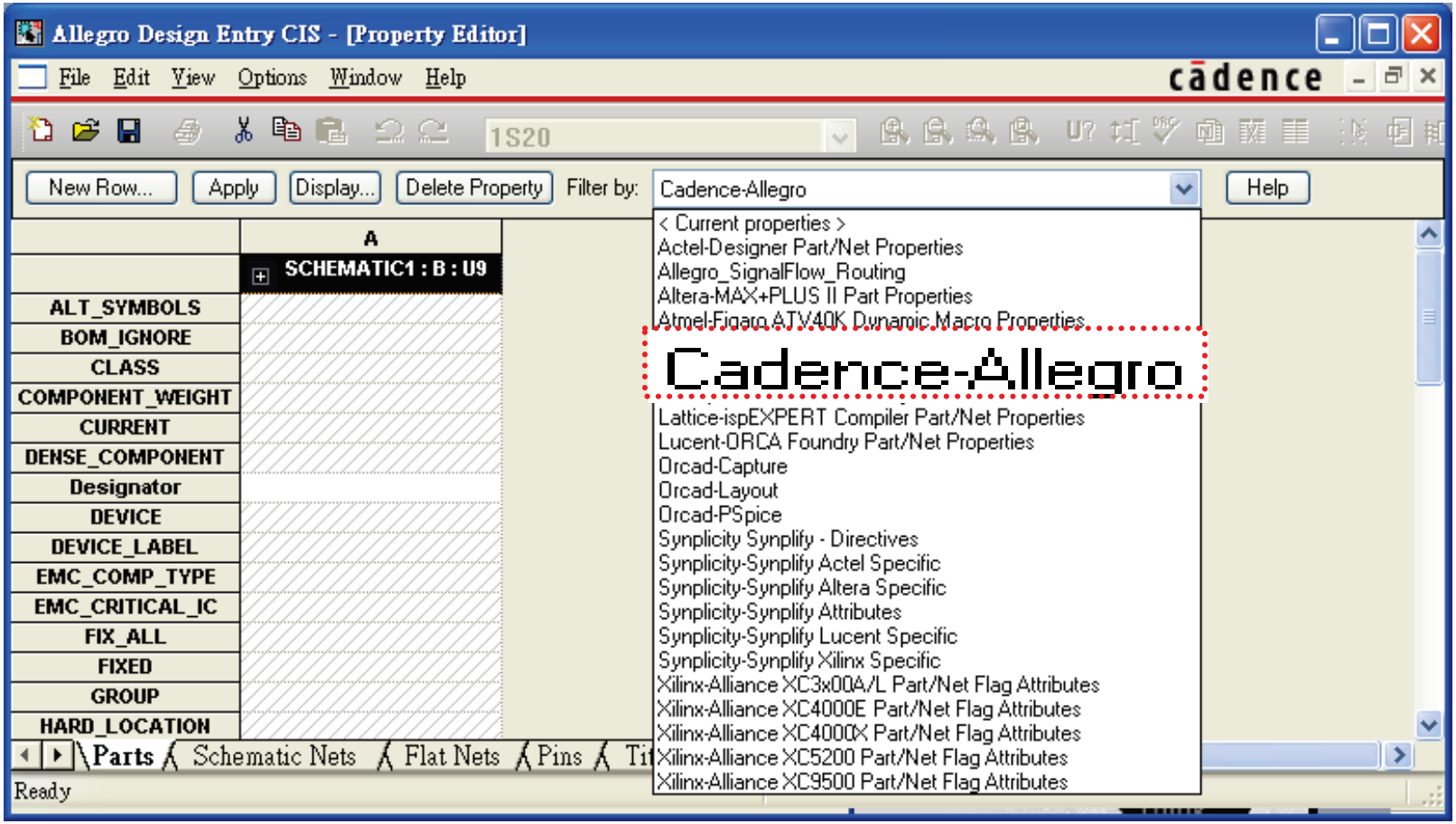


Constraint Management

- 從Schematic、PCB、SI 等工具定義Constraint設定



Properties in Capture

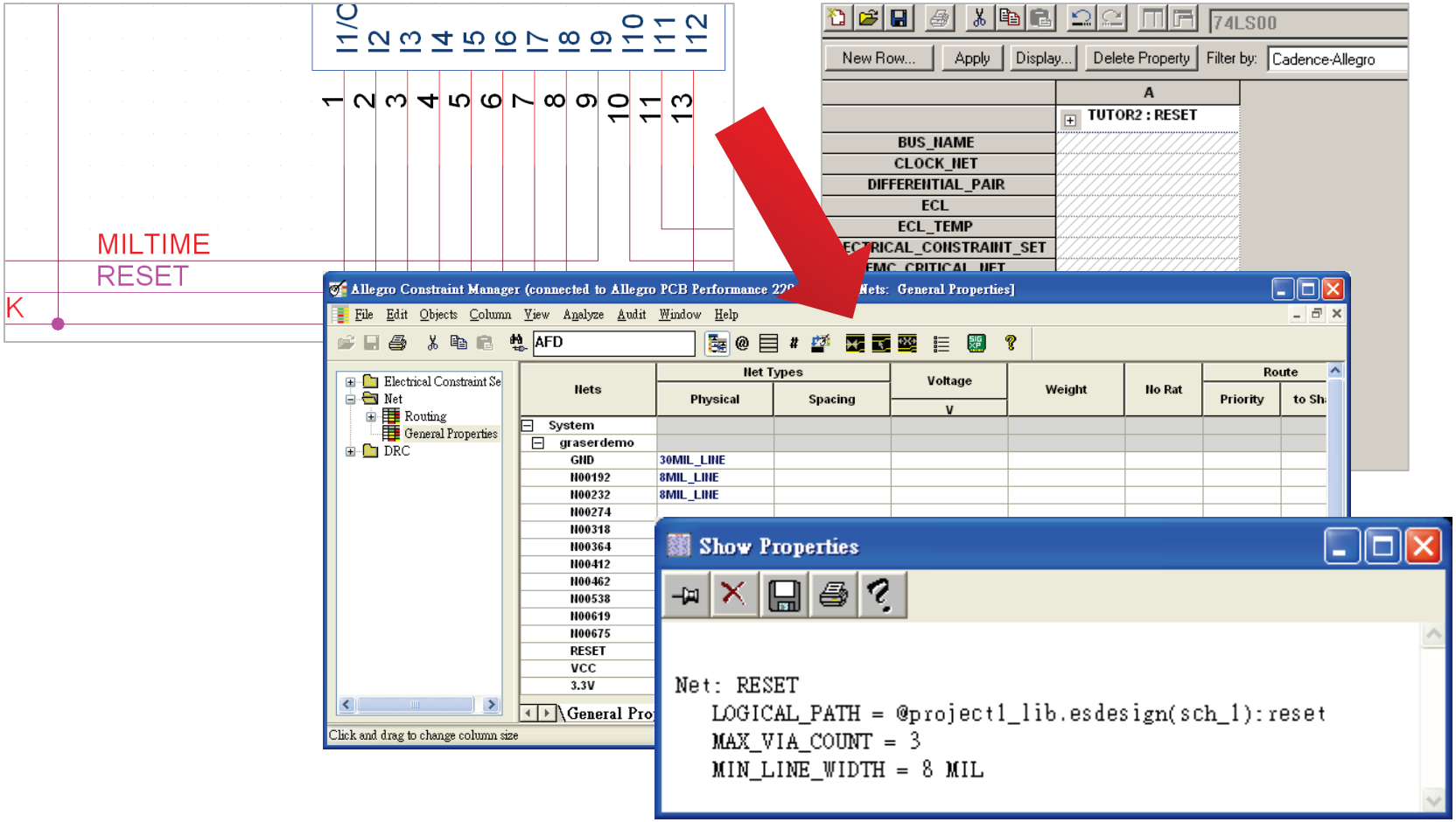


Part Properties

Net Properties

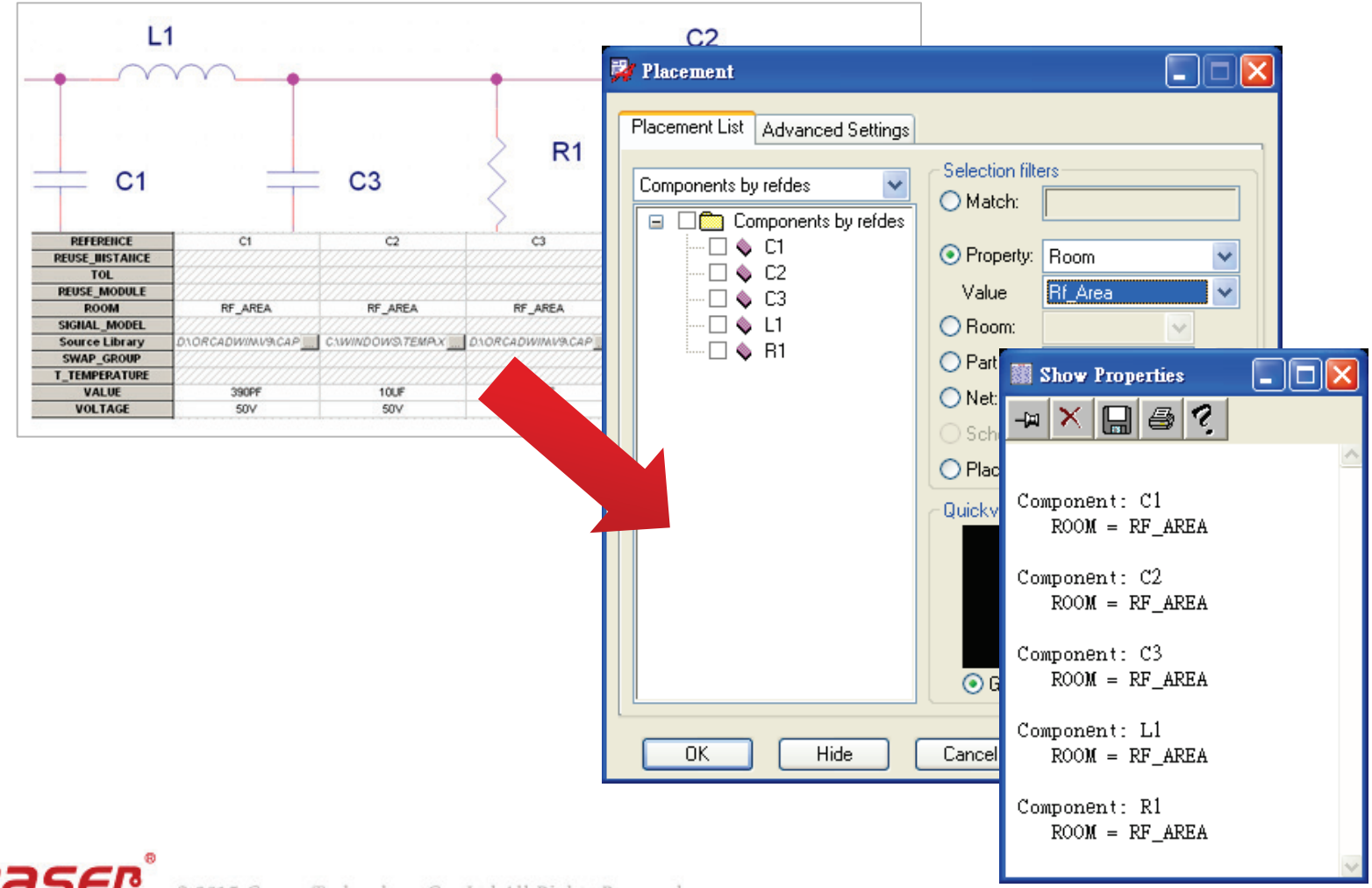
Netlist in With Properties

- 將線路圖之規範直接帶到PCB



Place by Room

- 依SCH設定之區域擺放零件至PCB所對應之位置



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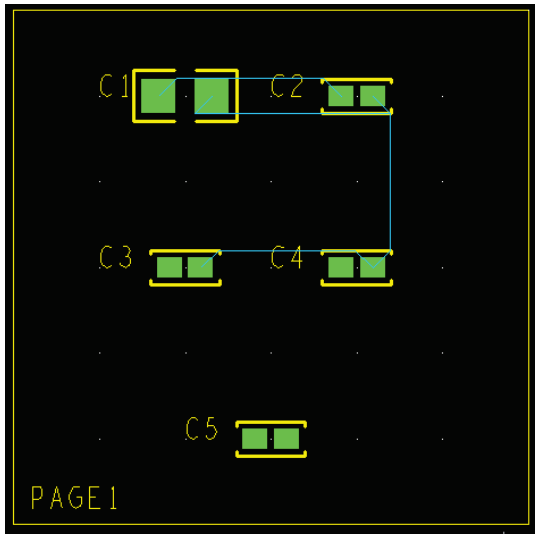
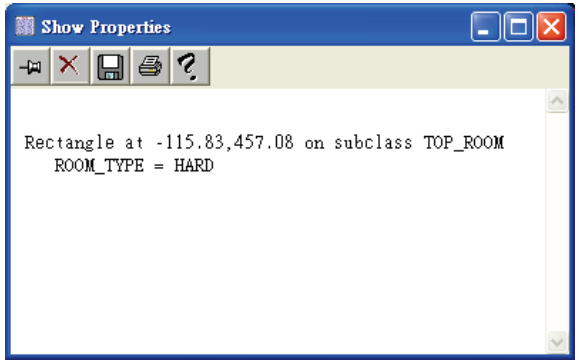
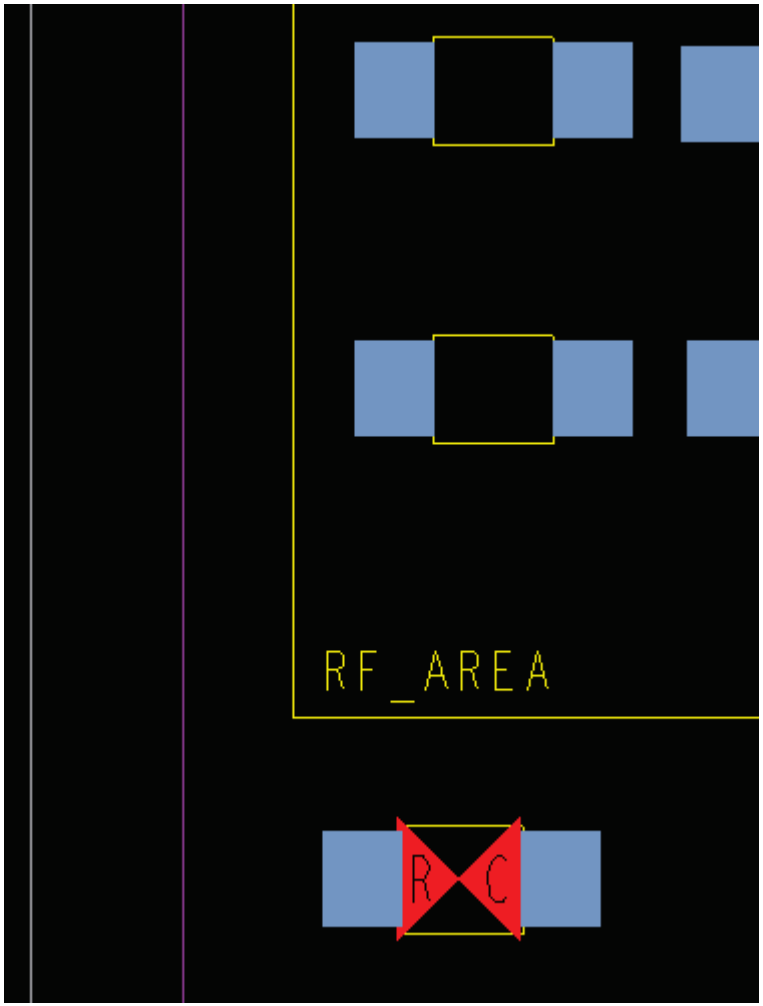
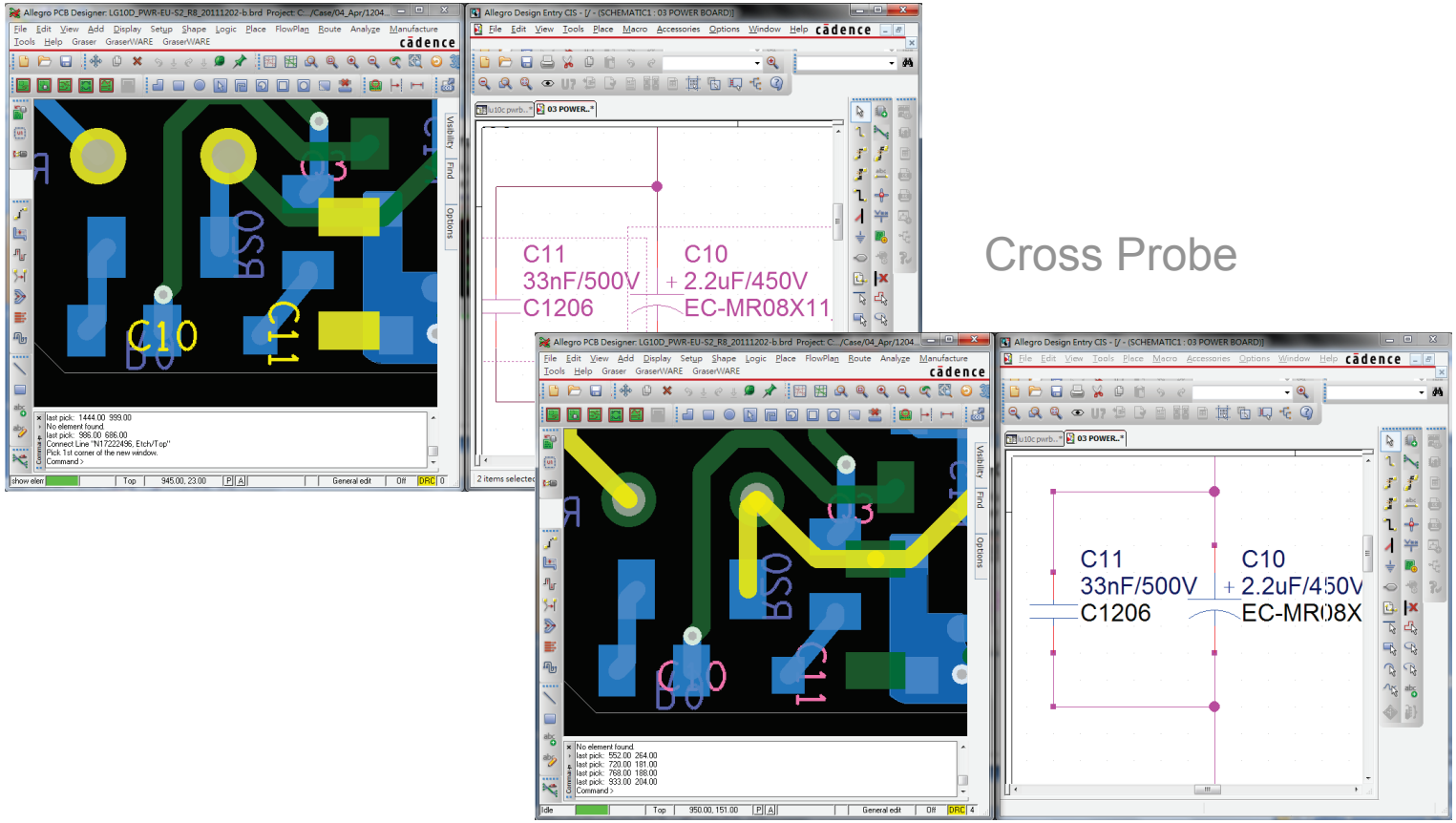






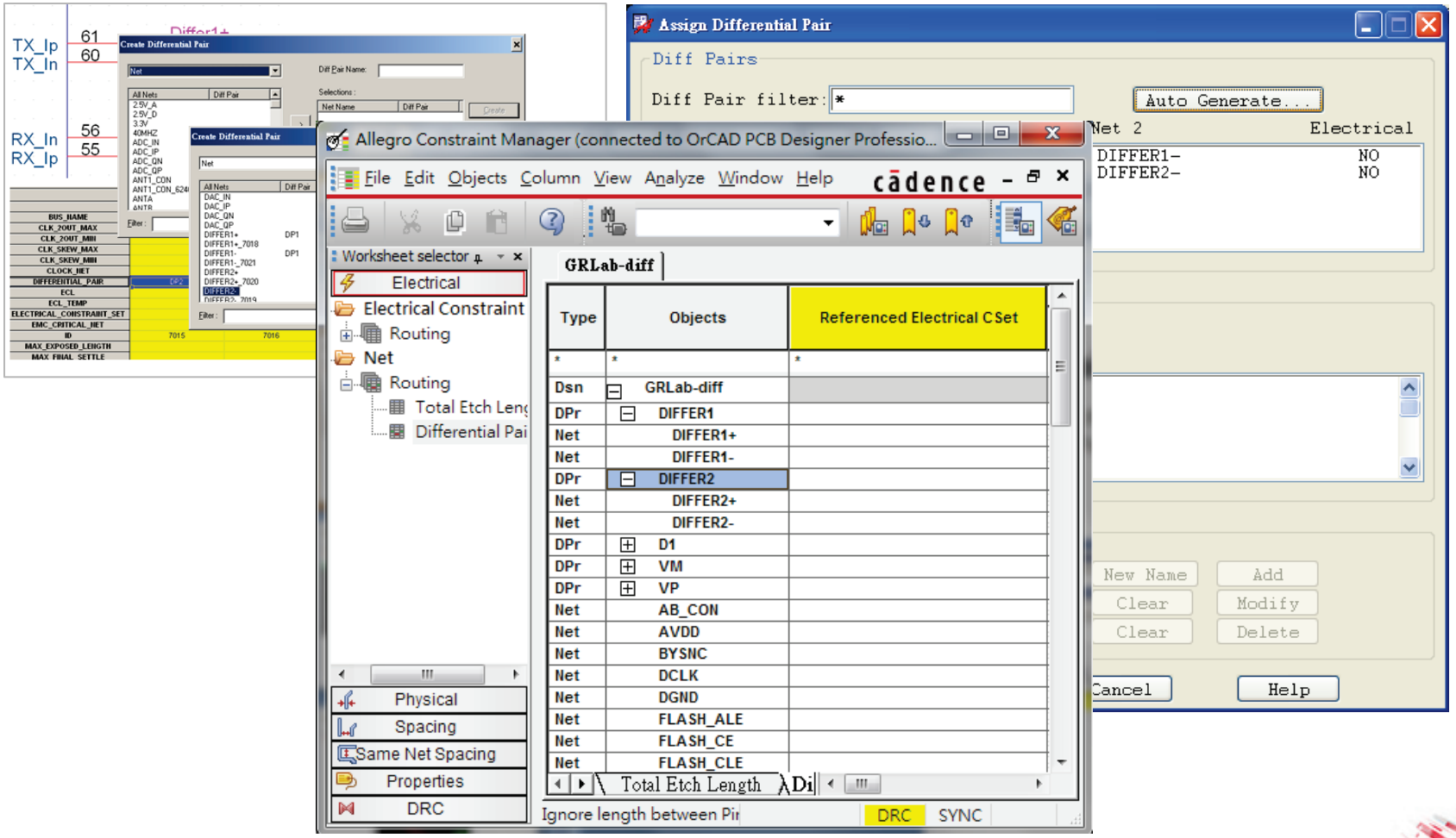
Netlist In And Crosslink

- Capture 與 PCB Designer ：
  可做電路圖 & PCB Layout間的Cross Highlight



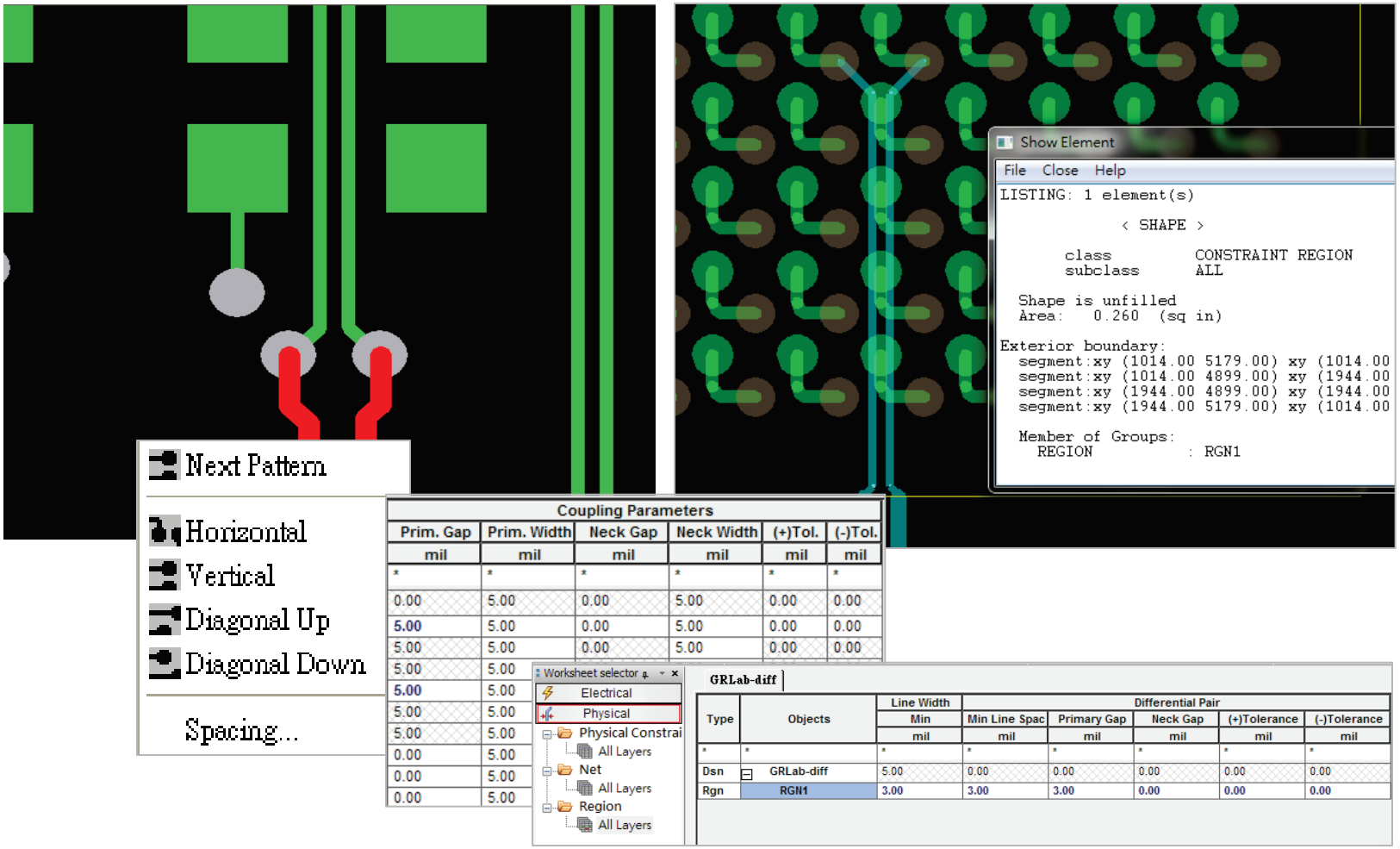
Differential Pair Setting

- 簡易的Differential Pair設定



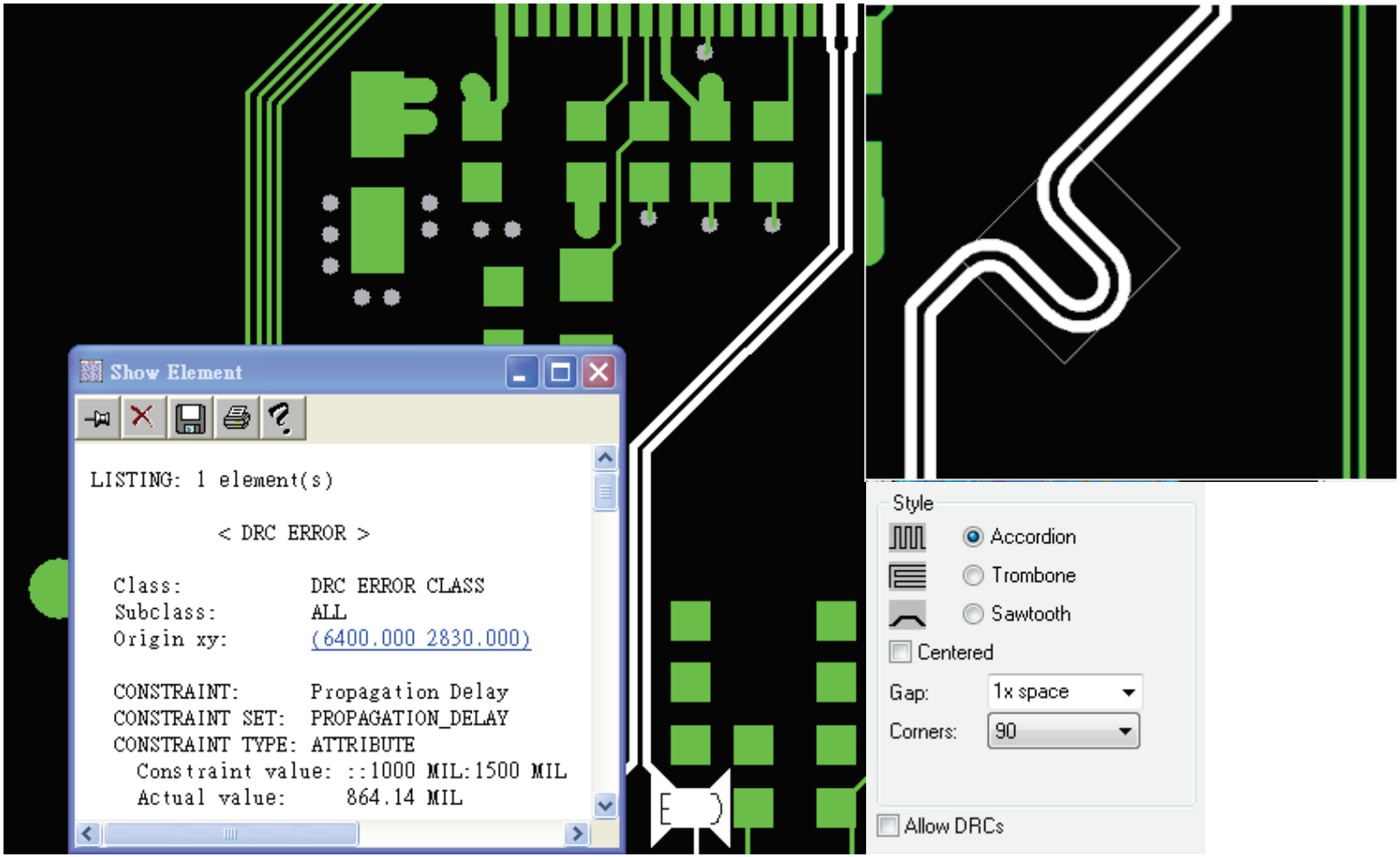
Differential Pair Check & Route

- 方便的Differential Pair走線模式

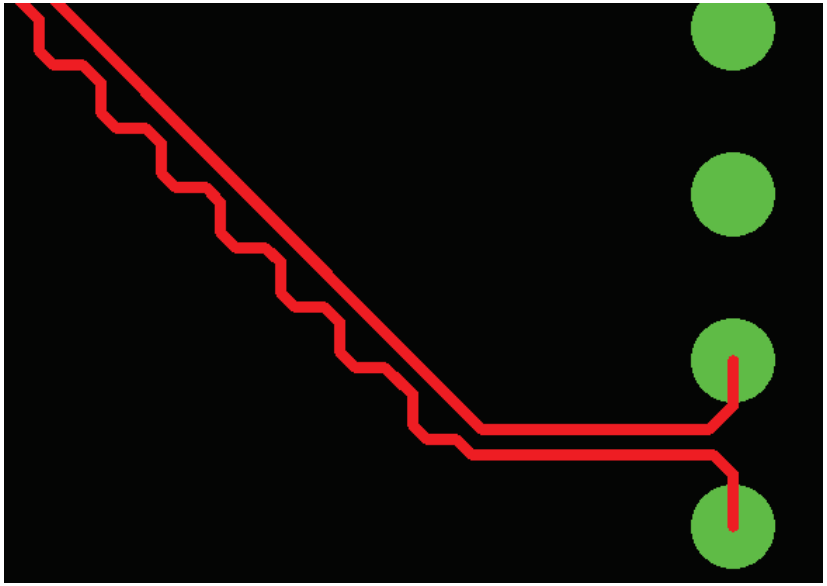


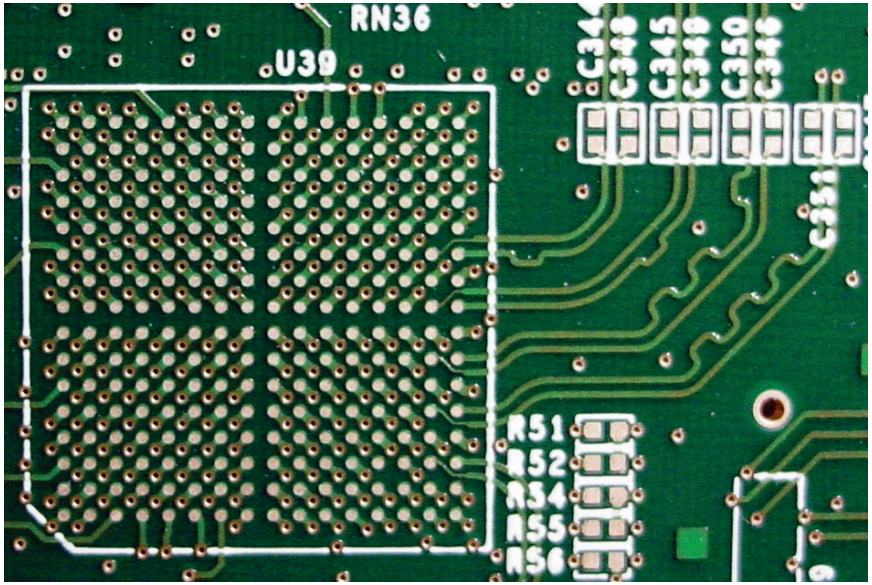
Delay Tune

- Delay Tune走線功能



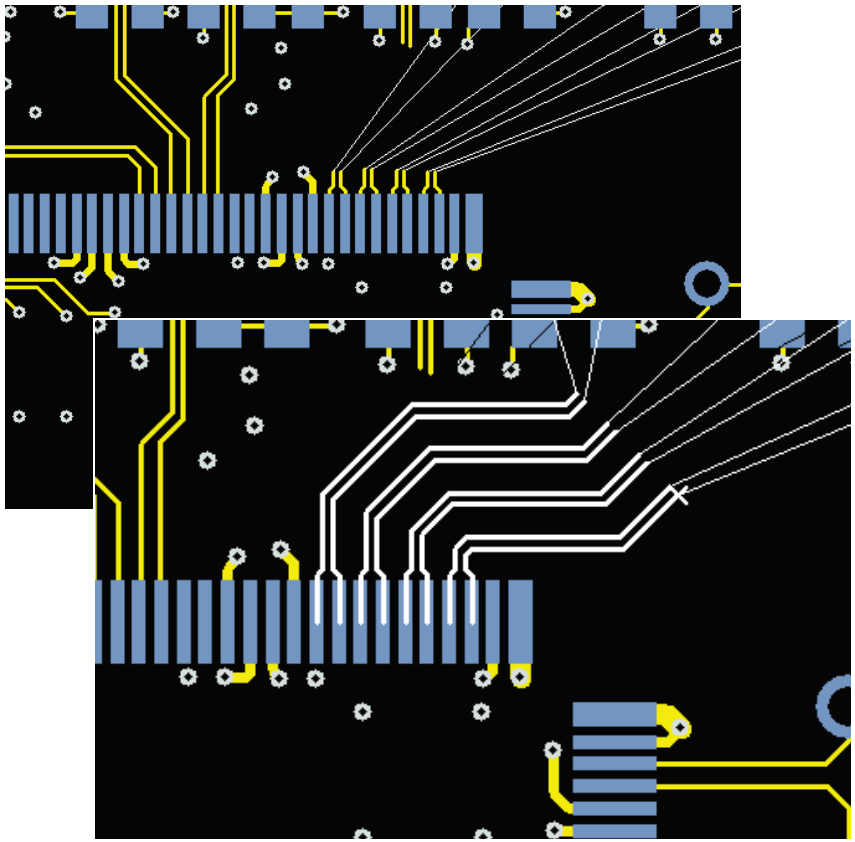
Differential Pair Phase Tuning

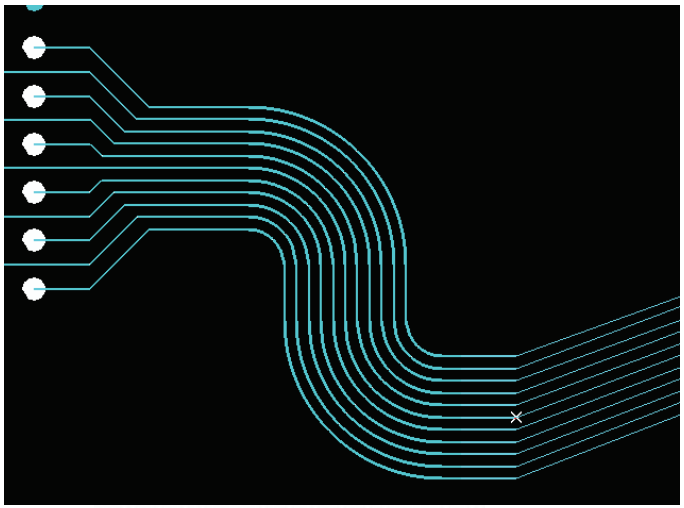




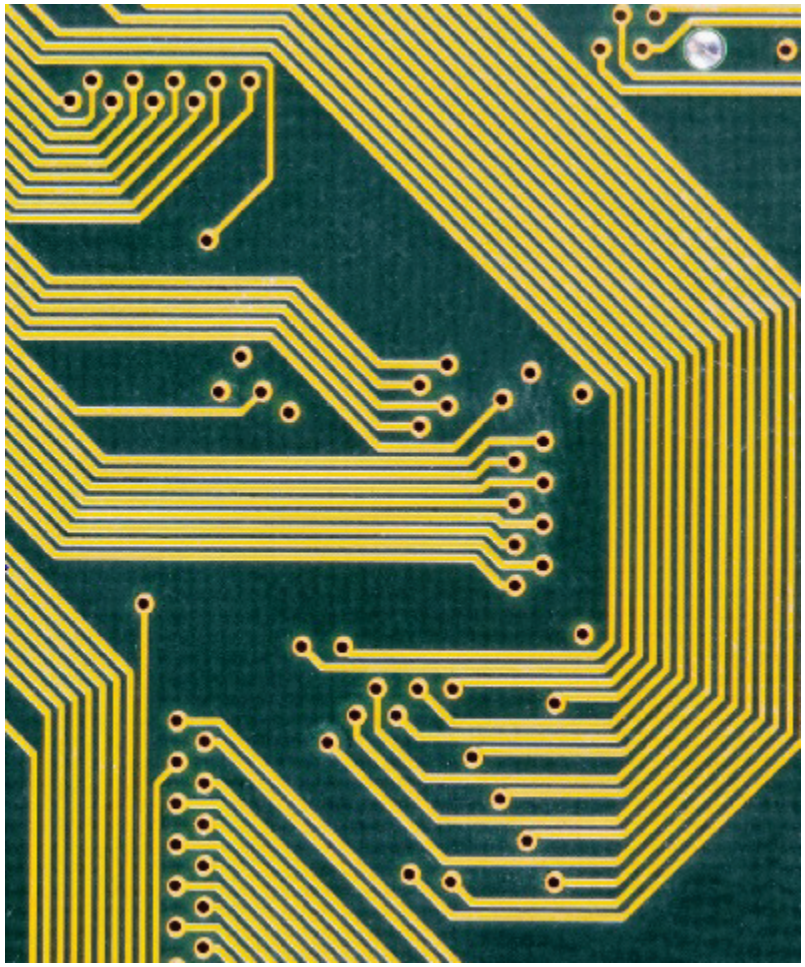
Route／Bus Route

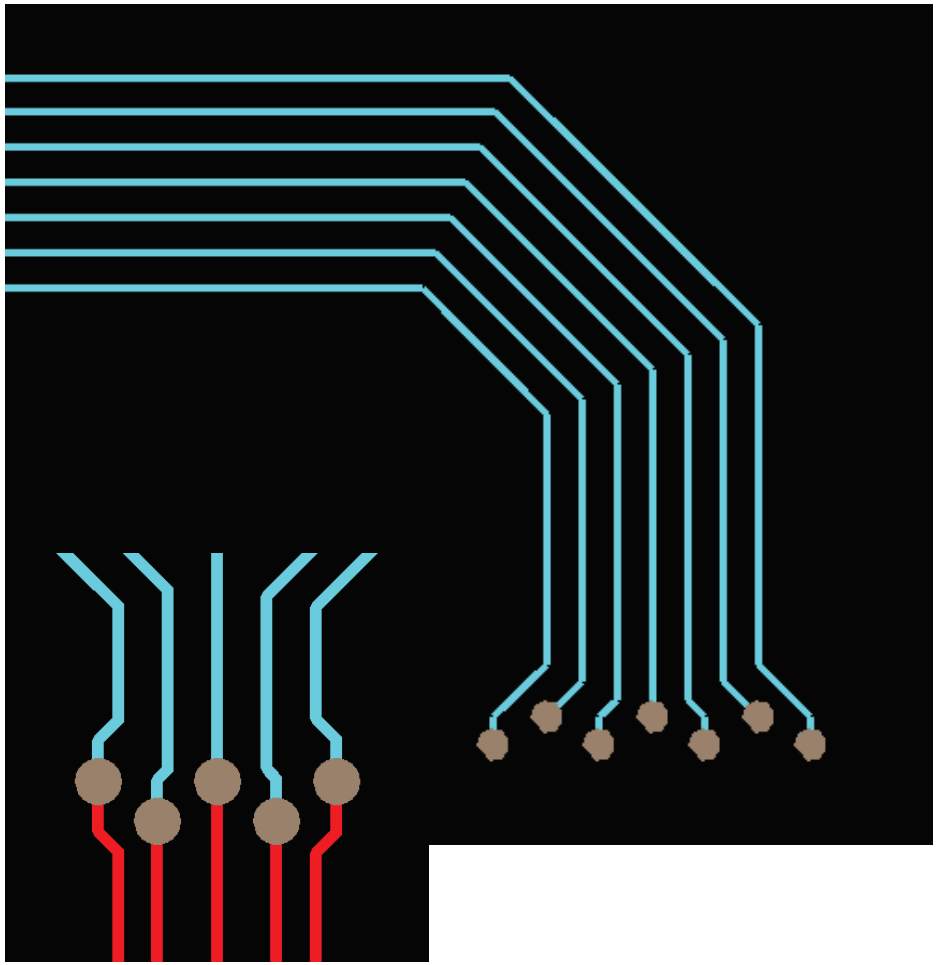
- 方便的Bus走線功能
- Bus 與一般走線皆能以任意角Arc走線



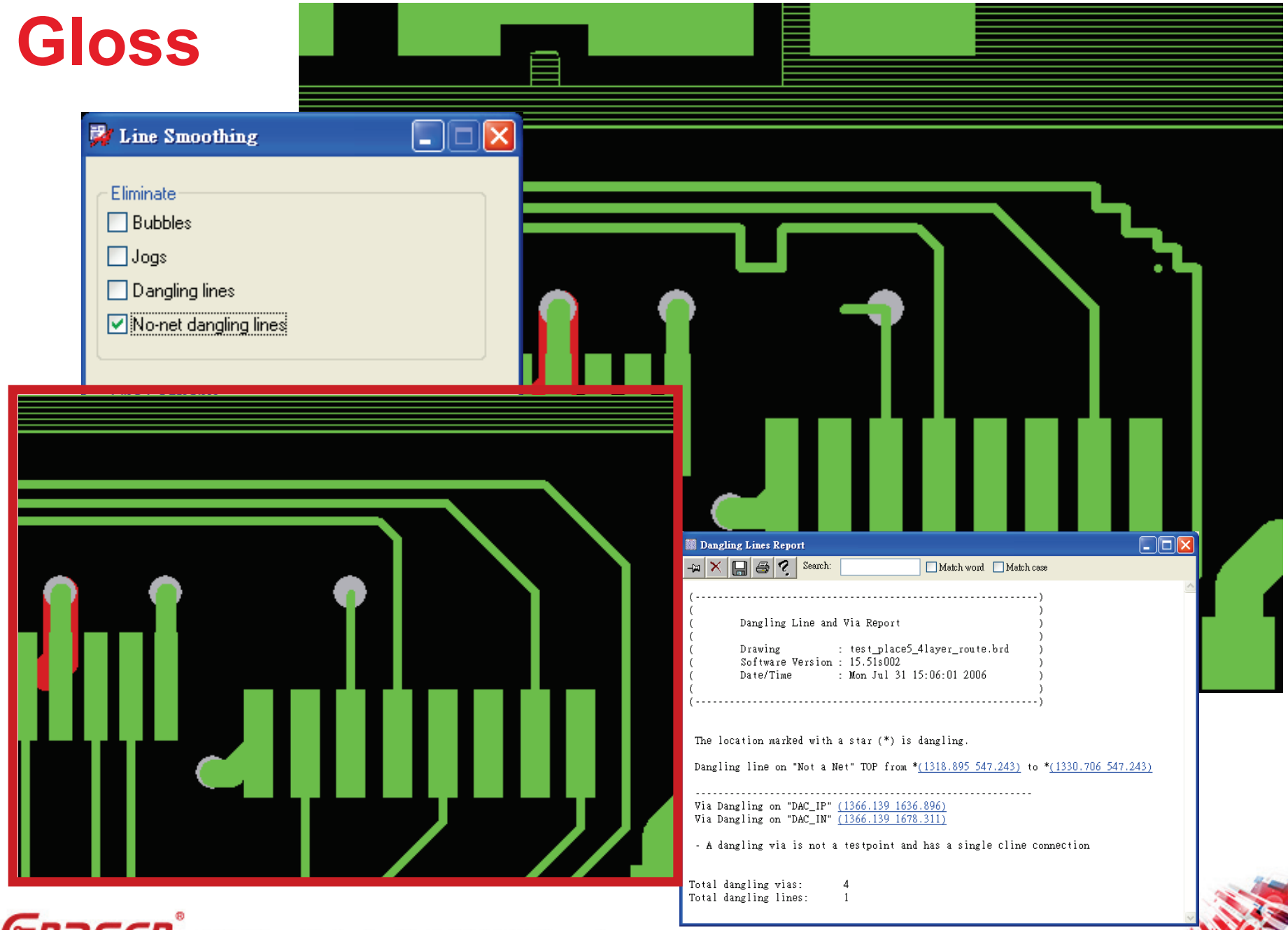


Group Route Via Patterns



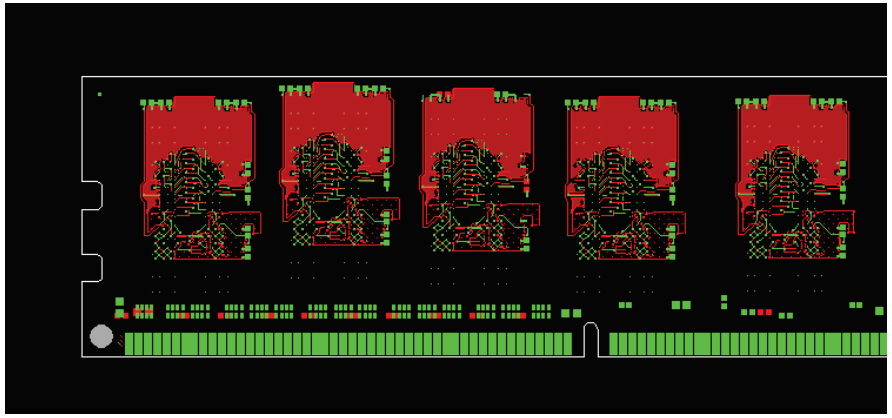


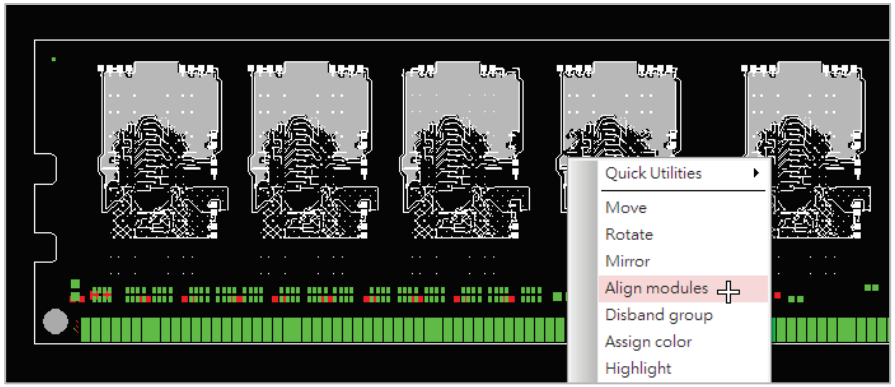
Gloss

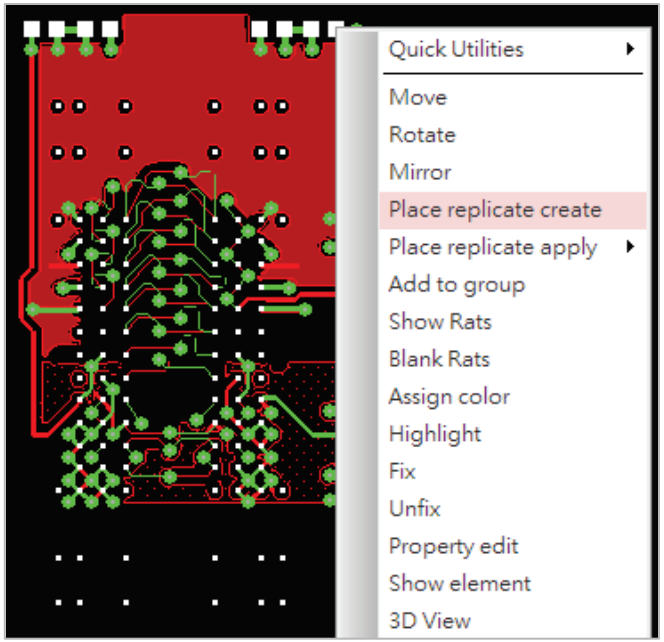


Placement Replication

- Support of metal (clines, vias, shapes)
- Alignment of group circuits

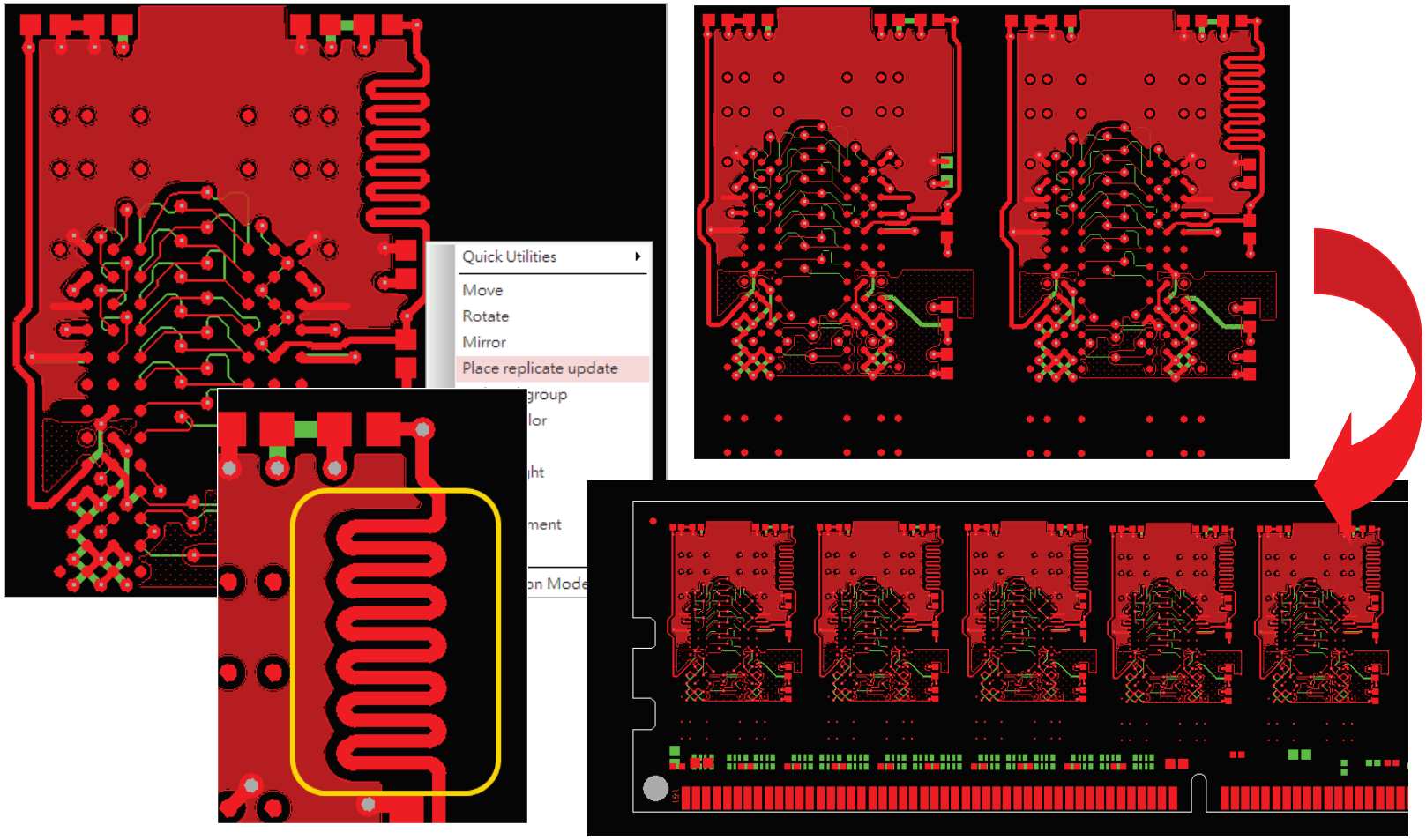






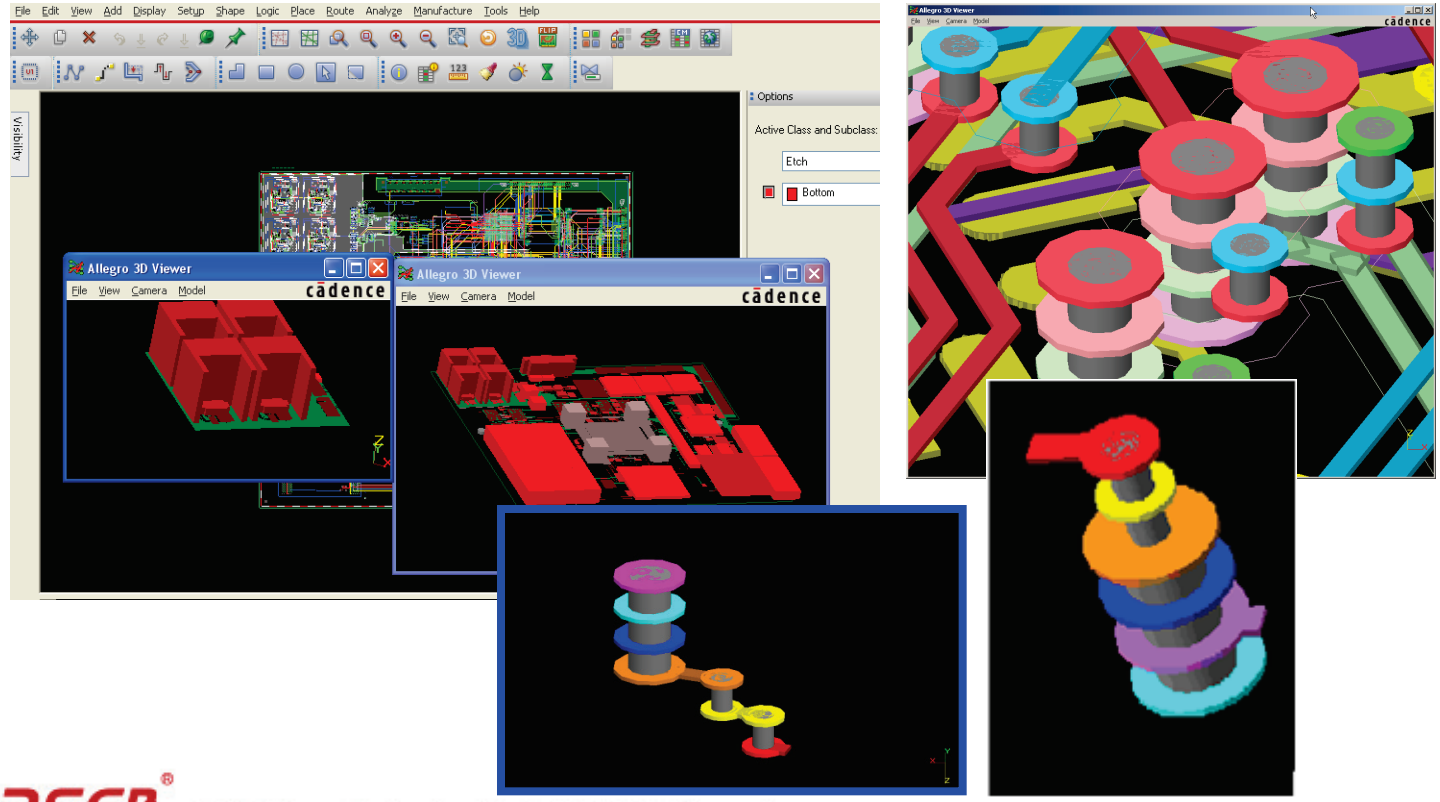
Placement Replication

- Circuit Refresh／Update

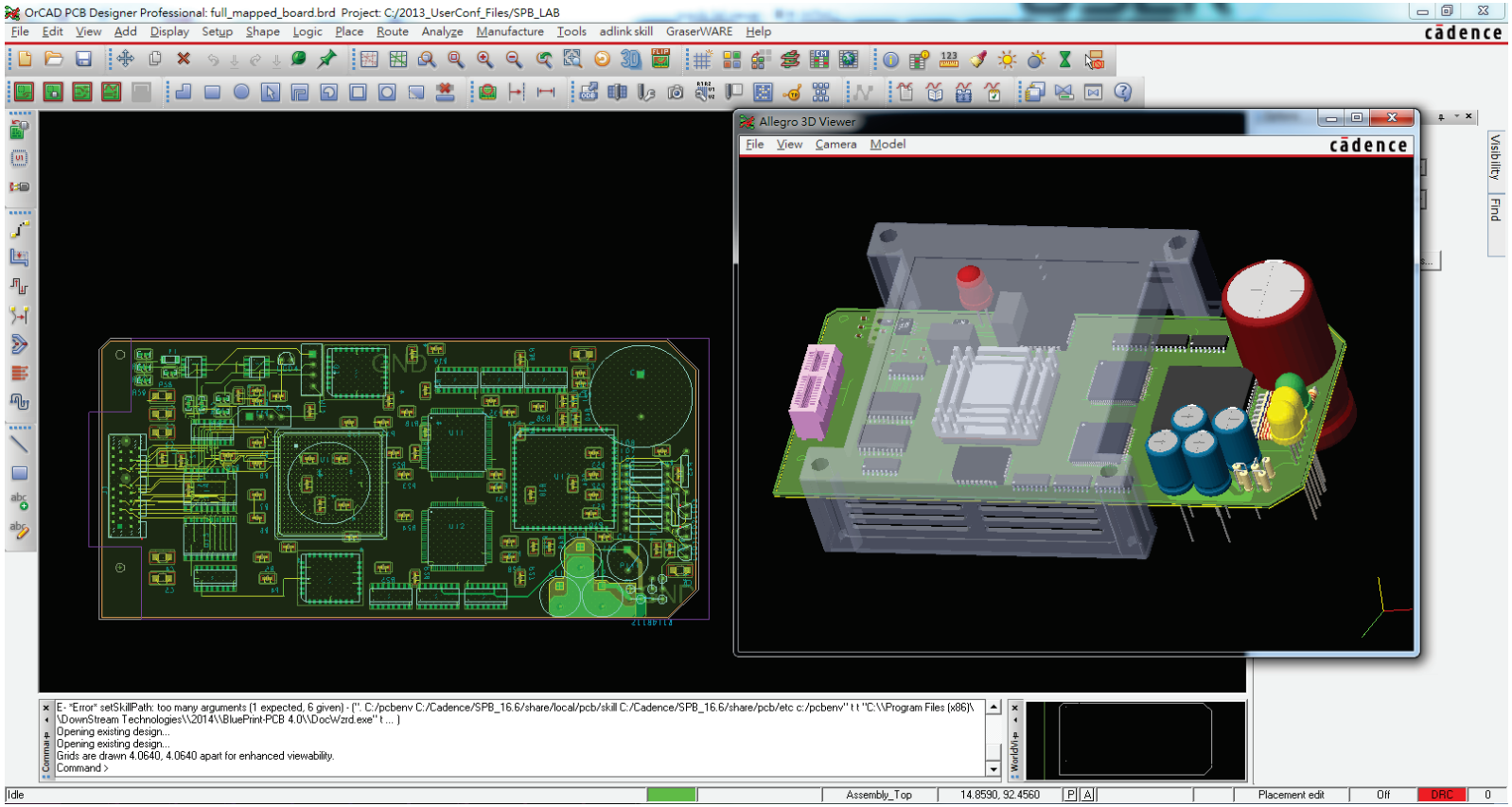


3D Graphics

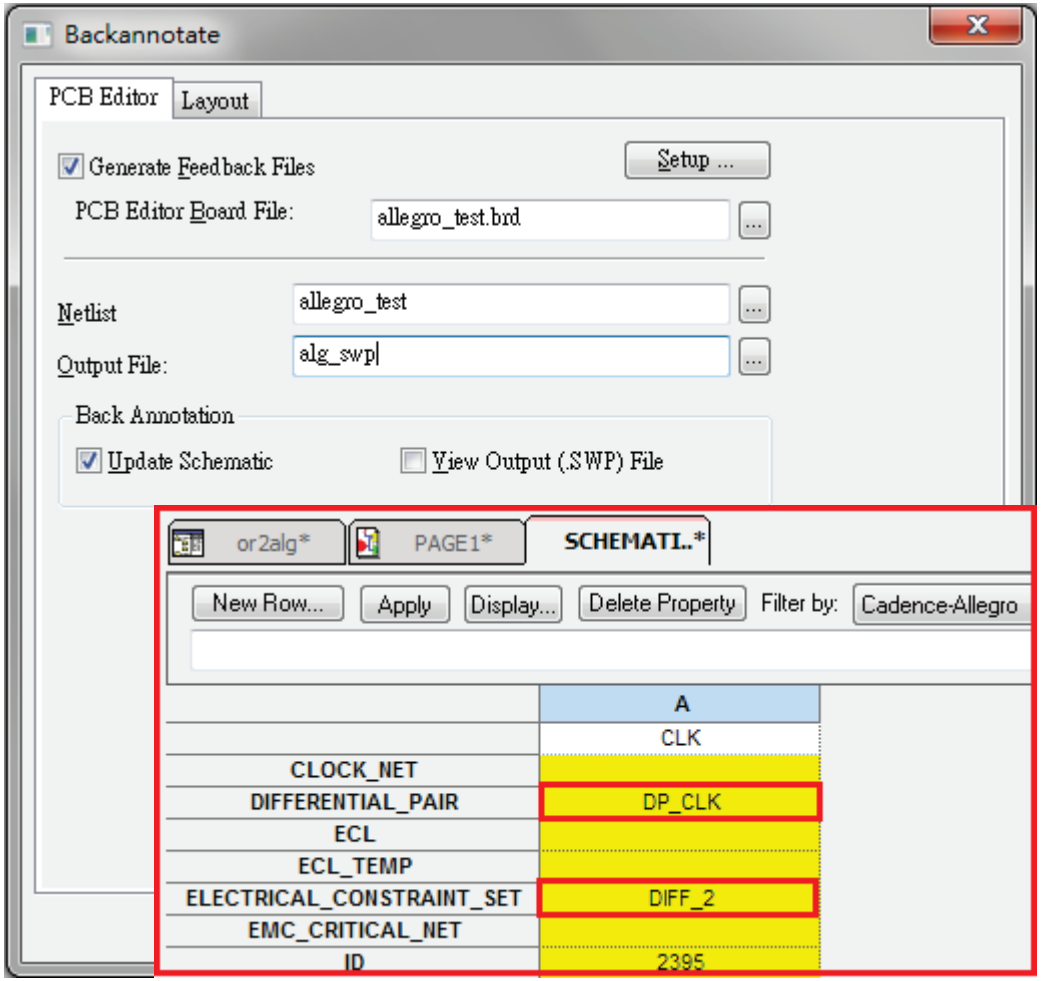
- Support multiple windows
- View micro vias, through hole vias and traces on different layers
- Pre-selection support
- View one net with HDI micro via breakout



STEP File Mapping



Back Annotation



- Property Changes
- Ref-des Changes
- Pin and Gate Swaps

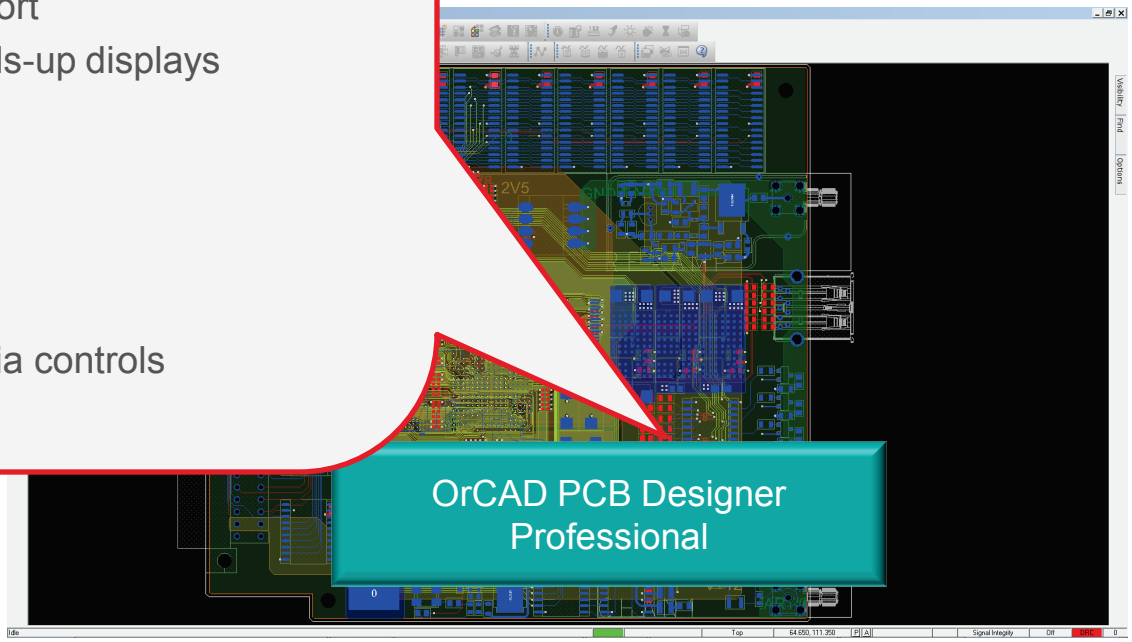
One more thing…

OrCAD V16.6-2015

New OrCAD PCB Designer Professional Functionalities

- High-speed constraints and routing
  - Relative propagation delay
  - Minimum / maximum propagation delay
  - Net scheduling / T-points
  - Differential Pair – static phase control
  - Impedance constraint support
  - High-speed constraint heads-up displays

- Routing productivity
  - Scribble route
  - Contour routing
  - Group routing – spacing / via controls
  - Via arrays

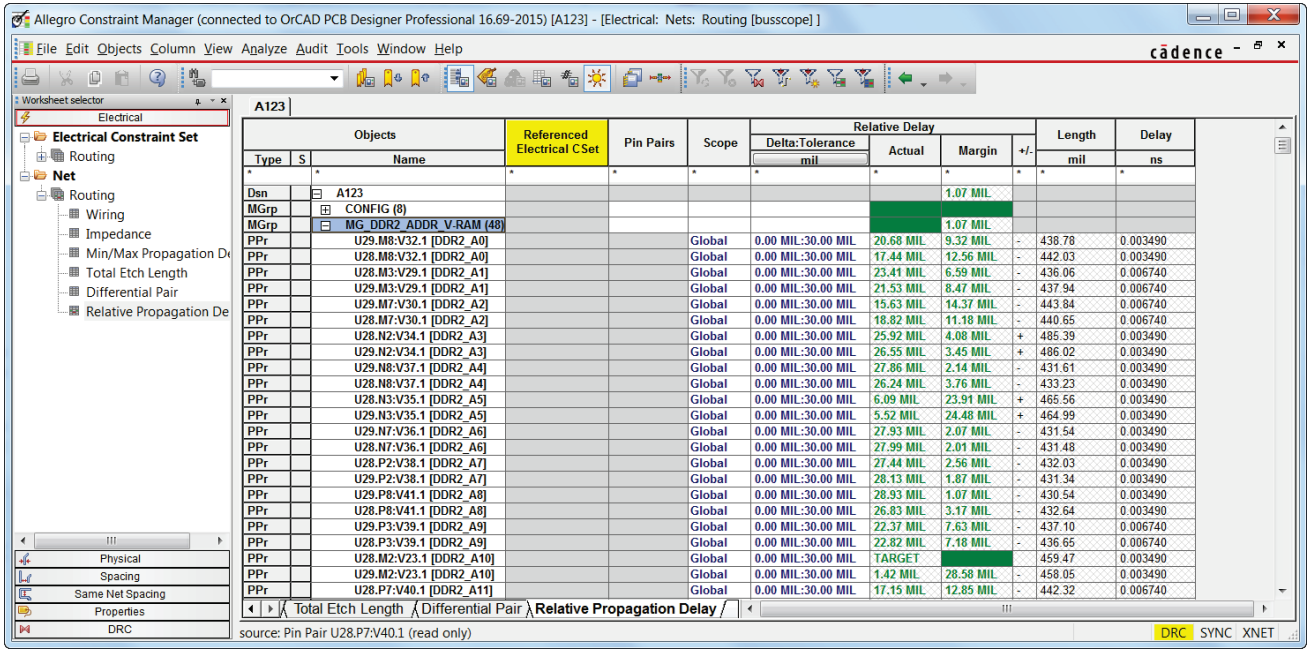


High-speed Constraint Support and Routing

- High-speed memory (DDR), sophisticated serial interfaces (USB), and more complex constraints (timing, impedance) creating new design challenges.
- For example, high-speed memory might require complex constraints such as :
  - Relative Propagation Delay for the Data byte lane
    - x-mils between all members
  - Relative Propagation Delay for Address / Command / Control
    - x-mils between Controller and T-Point
    - x-mils between memory ICs and T-Point
  - Propagation Delay
    - x-mils between Memory ICs
  - Differential Phase Tolerance
    - x-mils for all Data Strobe and Clock Differential Pairs

Relative Propagation Delay

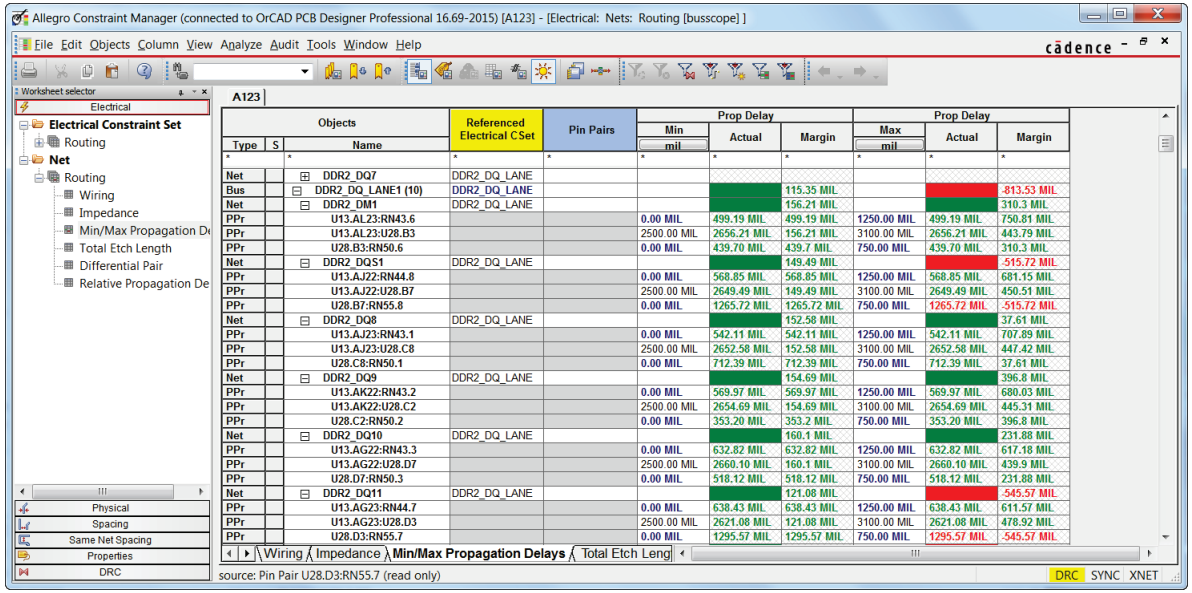
- Manage delay of matched groups between objects of different nets in terms of length, percent of Manhattan length.
- Delta : Tolerance assigns a ‘target’ to object with longest Manhattan length and can be reassigned if necessary.



Objects			Referenced Electrical CSet	Pin Pairs	Scope	Relative Delay				Length	Delay
Type	S	Name				Delta:Tolerance mil	Actual	Margin	+/-	mil	ns
*		*	*	*	*	*	*	*	*	*	*
Dsn		A123						1.07 MIL			
MGrp		CONFIG (8)									
MGrp		MG_DDR2_ADDR_V-RAM (48)						1.07 MIL			
PPr		U29.M8:V32.1 [DDR2_A0]			Global	0.00 MIL:30.00 MIL	20.68 MIL	9.32 MIL	-	438.78	0.003490
PPr		U28.M8:V32.1 [DDR2_A0]			Global	0.00 MIL:30.00 MIL	17.44 MIL	12.56 MIL	-	442.03	0.003490
PPr		U28.M3:V29.1 [DDR2_A1]			Global	0.00 MIL:30.00 MIL	23.41 MIL	6.59 MIL	-	436.06	0.006740
PPr		U29.M3:V29.1 [DDR2_A1]			Global	0.00 MIL:30.00 MIL	21.53 MIL	8.47 MIL	-	437.94	0.006740
PPr		U29.M7:V30.1 [DDR2_A2]			Global	0.00 MIL:30.00 MIL	15.63 MIL	14.37 MIL	-	443.84	0.006740
PPr		U28.M7:V30.1 [DDR2_A2]			Global	0.00 MIL:30.00 MIL	18.82 MIL	11.18 MIL	-	440.65	0.006740
PPr		U28.N2:V34.1 [DDR2_A3]			Global	0.00 MIL:30.00 MIL	25.92 MIL	4.08 MIL	+	485.39	0.003490
PPr		U29.N2:V34.1 [DDR2_A3]			Global	0.00 MIL:30.00 MIL	26.55 MIL	3.45 MIL	+	486.02	0.003490
PPr		U29.N8:V37.1 [DDR2_A4]			Global	0.00 MIL:30.00 MIL	27.86 MIL	2.14 MIL	-	431.61	0.003490
PPr		U28.N8:V37.1 [DDR2_A4]			Global	0.00 MIL:30.00 MIL	26.24 MIL	3.76 MIL	-	433.23	0.003490
PPr		U28.N3:V35.1 [DDR2_A5]			Global	0.00 MIL:30.00 MIL	6.09 MIL	23.91 MIL	+	465.56	0.003490
PPr		U29.N3:V35.1 [DDR2_A5]			Global	0.00 MIL:30.00 MIL	5.52 MIL	24.48 MIL	+	464.99	0.003490
PPr		U29.N7:V36.1 [DDR2_A6]			Global	0.00 MIL:30.00 MIL	27.93 MIL	2.07 MIL	-	431.54	0.003490
PPr		U28.N7:V36.1 [DDR2_A6]			Global	0.00 MIL:30.00 MIL	27.99 MIL	2.01 MIL	-	431.48	0.003490
PPr		U28.P2:V38.1 [DDR2_A7]			Global	0.00 MIL:30.00 MIL	27.44 MIL	2.56 MIL	-	432.03	0.003490
PPr		U29.P2:V38.1 [DDR2_A7]			Global	0.00 MIL:30.00 MIL	28.13 MIL	1.87 MIL	-	431.34	0.003490
PPr		U29.P8:V41.1 [DDR2_A8]			Global	0.00 MIL:30.00 MIL	28.93 MIL	1.07 MIL	-	430.54	0.003490
PPr		U28.P8:V41.1 [DDR2_A8]			Global	0.00 MIL:30.00 MIL	26.83 MIL	3.17 MIL	-	432.64	0.003490
PPr		U29.P3:V39.1 [DDR2_A9]			Global	0.00 MIL:30.00 MIL	22.37 MIL	7.63 MIL	-	437.10	0.006740
PPr		U28.P3:V39.1 [DDR2_A9]			Global	0.00 MIL:30.00 MIL	22.82 MIL	7.18 MIL	-	436.65	0.006740
PPr		U28.M2:V23.1 [DDR2_A10]			Global	0.00 MIL:30.00 MIL	TARGET			459.47	0.003490
PPr		U29.M2:V23.1 [DDR2_A10]			Global	0.00 MIL:30.00 MIL	1.42 MIL	28.58 MIL	-	458.05	0.003490
PPr		U28.P7:V40.1 [DDR2_A11]			Global	0.00 MIL:30.00 MIL	17.15 MIL	12.85 MIL	-	442.32	0.006740

Minimum／Maximum Propagation Delay

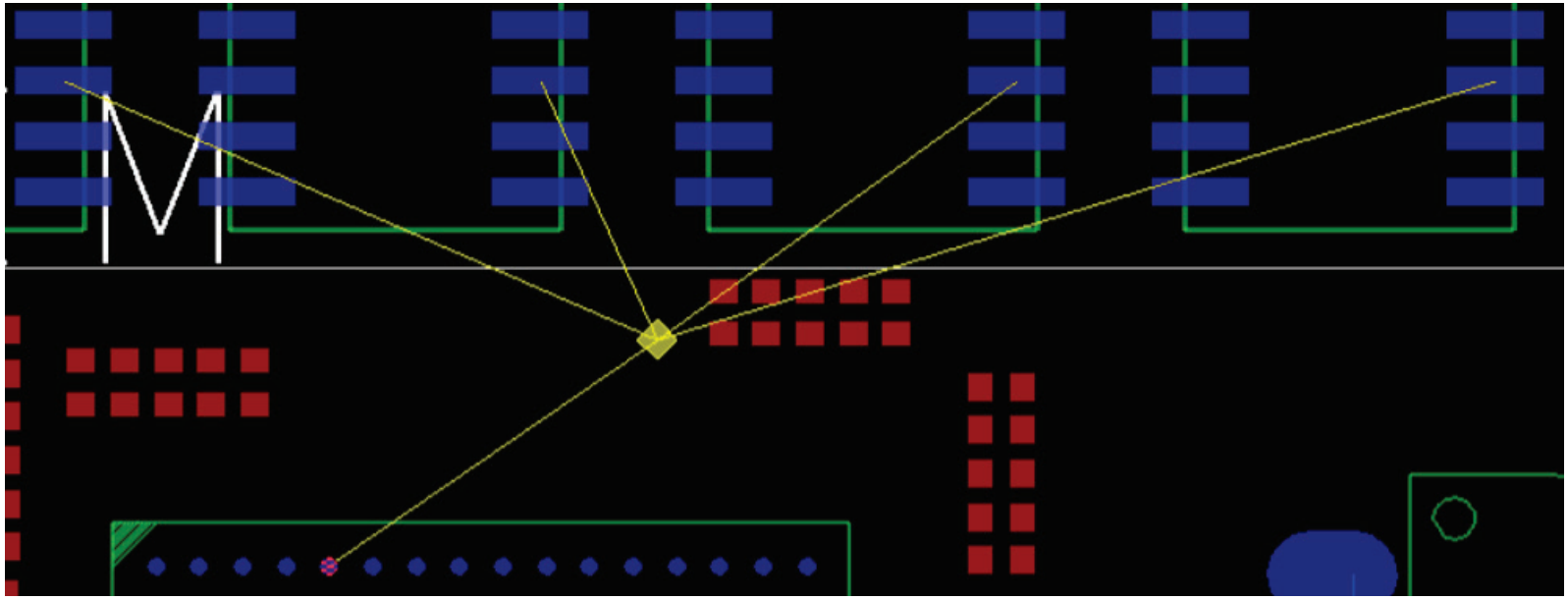
- Manage delay in terms of length, percent of Manhattan length pin-pairs
- DRC responds to both unrouted and routed conditions
- Evaluate timing rules at component placement stage
- Object selection will highlight and zoom-center in PCB



Objects			Referenced Electrical CSet	Pin Pairs	Prop Delay			Prop Delay		
Type	S	Name			Min mil	Actual	Margin	Max mil	Actual	Margin
*		*	*	*	*	*	*	*	*	*
Net		DDR2_DQ7	DDR2_DQ_LANE							
Bus		DDR2_DQ_LANE1 (10)	DDR2_DQ_LANE				115.35 MIL			-813.53 MIL
Net		DDR2_DM1	DDR2_DQ_LANE				156.21 MIL			310.3 MIL
PPr		U13.AL23:RN43.6			0.00 MIL	499.19 MIL	499.19 MIL	1250.00 MIL	499.19 MIL	750.81 MIL
PPr		U13.AL23:U28.B3			2500.00 MIL	2656.21 MIL	156.21 MIL	3100.00 MIL	2656.21 MIL	443.79 MIL
PPr		U28.B3:RN50.6			0.00 MIL	439.70 MIL	439.7 MIL	750.00 MIL	439.70 MIL	310.3 MIL
Net		DDR2_DQS1	DDR2_DQ_LANE				149.49 MIL			-515.72 MIL
PPr		U13.AJ22:RN44.8			0.00 MIL	568.85 MIL	568.85 MIL	1250.00 MIL	568.85 MIL	681.15 MIL
PPr		U13.AJ22:U28.B7			2500.00 MIL	2649.49 MIL	149.49 MIL	3100.00 MIL	2649.49 MIL	450.51 MIL
PPr		U28.B7:RN55.8			0.00 MIL	1265.72 MIL	1265.72 MIL	750.00 MIL	1265.72 MIL	-515.72 MIL
Net		DDR2_DQ8	DDR2_DQ_LANE				152.58 MIL			37.61 MIL
PPr		U13.AJ23:RN43.1			0.00 MIL	542.11 MIL	542.11 MIL	1250.00 MIL	542.11 MIL	707.89 MIL
PPr		U13.AJ23:U28.C8			2500.00 MIL	2652.58 MIL	152.58 MIL	3100.00 MIL	2652.58 MIL	447.42 MIL
PPr		U28.C8:RN50.1			0.00 MIL	712.39 MIL	712.39 MIL	750.00 MIL	712.39 MIL	37.61 MIL
Net		DDR2_DQ9	DDR2_DQ_LANE				154.69 MIL			396.8 MIL
PPr		U13.AK22:RN43.2			0.00 MIL	569.97 MIL	569.97 MIL	1250.00 MIL	569.97 MIL	680.03 MIL
PPr		U13.AK22:U28.C2			2500.00 MIL	2654.69 MIL	154.69 MIL	3100.00 MIL	2654.69 MIL	445.31 MIL
PPr		U28.C2:RN50.2			0.00 MIL	353.20 MIL	353.2 MIL	750.00 MIL	353.20 MIL	396.8 MIL
Net		DDR2_DQ10	DDR2_DQ_LANE				160.1 MIL			231.88 MIL
PPr		U13.AG22:RN43.3			0.00 MIL	632.82 MIL	632.82 MIL	1250.00 MIL	632.82 MIL	617.18 MIL
PPr		U13.AG22:U28.D7			2500.00 MIL	2660.10 MIL	160.1 MIL	3100.00 MIL	2660.10 MIL	439.9 MIL
PPr		U28.D7:RN50.3			0.00 MIL	518.12 MIL	518.12 MIL	750.00 MIL	518.12 MIL	231.88 MIL
Net		DDR2_DQ11	DDR2_DQ_LANE				121.08 MIL			-545.57 MIL
PPr		U13.AG23:RN44.7			0.00 MIL	638.43 MIL	638.43 MIL	1250.00 MIL	638.43 MIL	611.57 MIL
PPr		U13.AG23:U28.D3			2500.00 MIL	2621.08 MIL	121.08 MIL	3100.00 MIL	2621.08 MIL	478.92 MIL
PPr		U28.D3:RN55.7			0.00 MIL	1295.57 MIL	1295.57 MIL	750.00 MIL	1295.57 MIL	-545.57 MIL

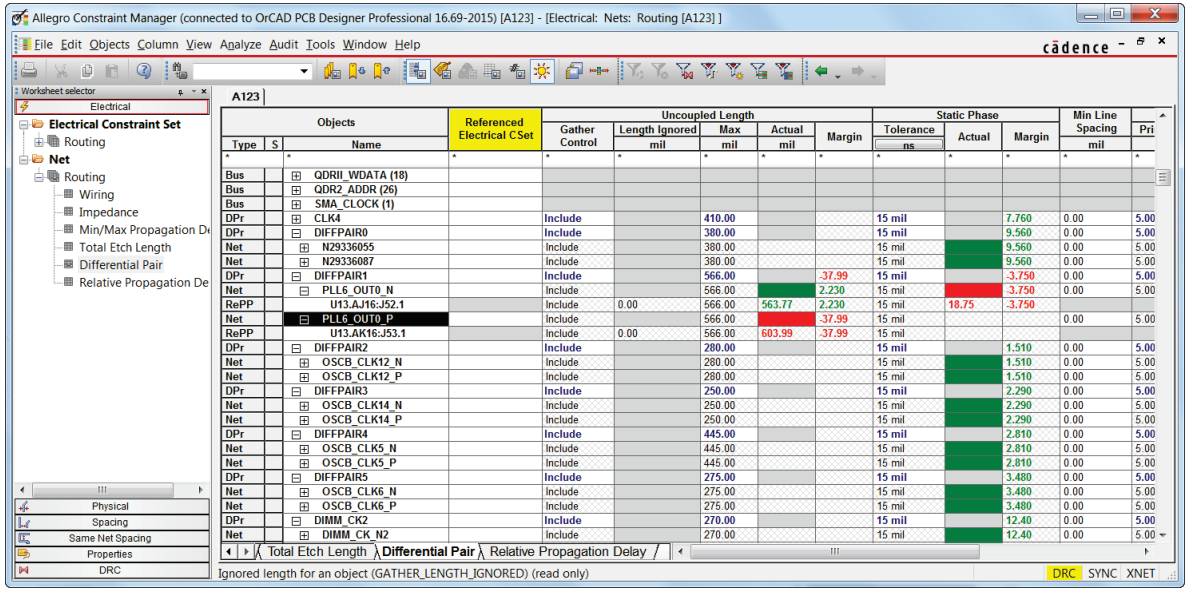
Net Scheduling／T-points

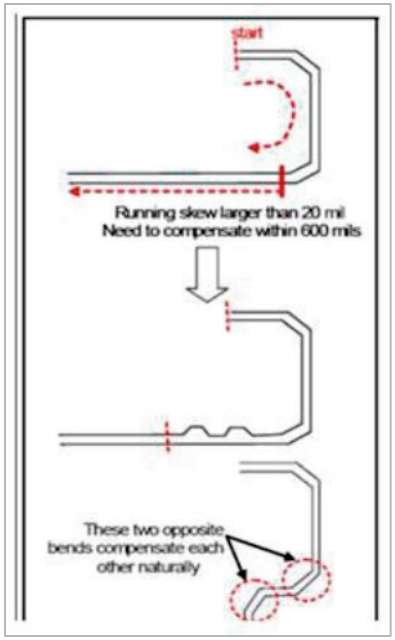
- Scheduling allows nets to be defined for a specific routing path or pattern
- T-points are virtual points which defines a location nets segments will start／end



Differential Pair Static Phase Control

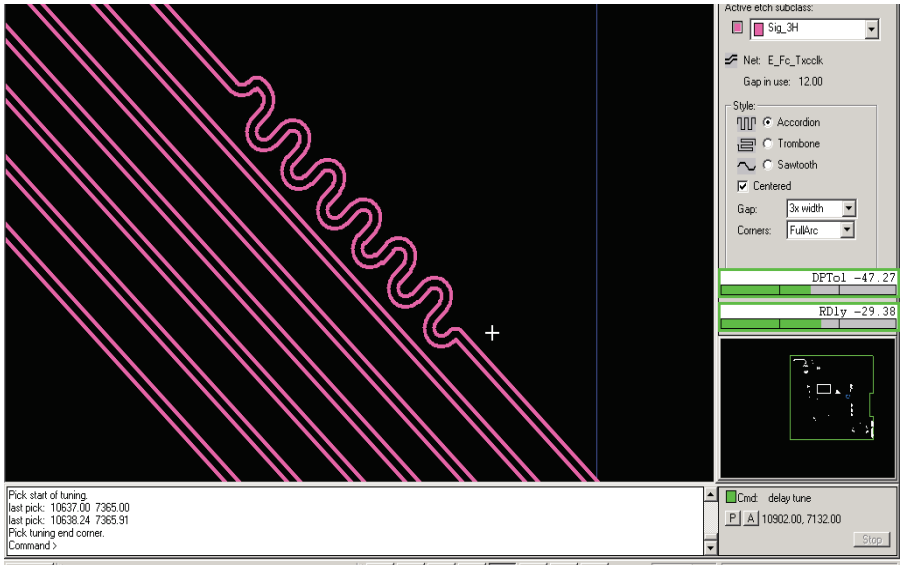
- Control matched length of differential pairs
- Phase is checked over entire net from driver to receiver

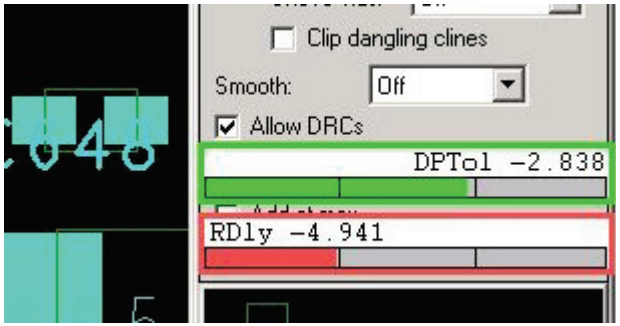




High-speed Constraint Heads-up Displays

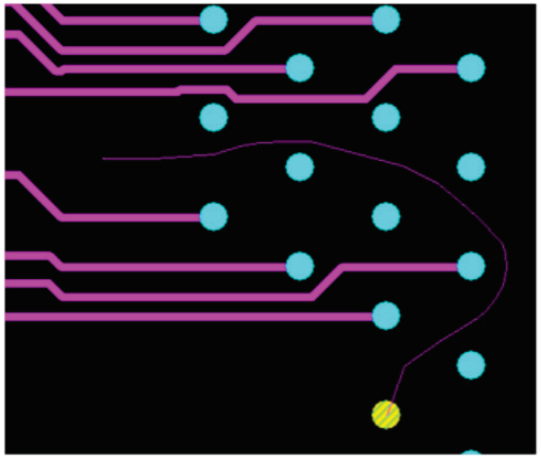
- Real-time heads-up constraint display provides direct feedback while tuning and editing high-speed constrained nets as a guide to see when the nets are in (or out of) compliance.



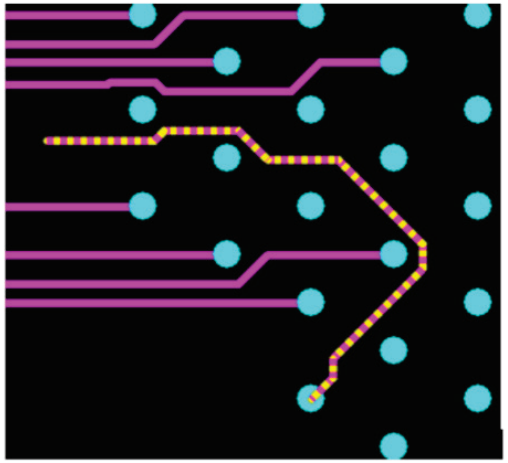


Scribble Route

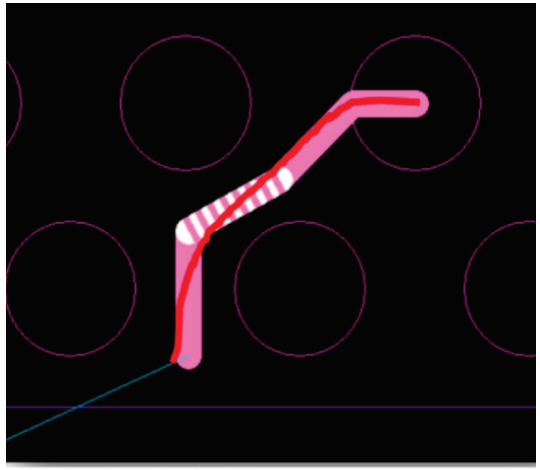
- Scribble is a simple routing mode that enables a drawn path from source to destination.
- Scribble also has ability to navigate routed path through pin pitches that require non-standard routing angles.



Scribble Path



Route Results

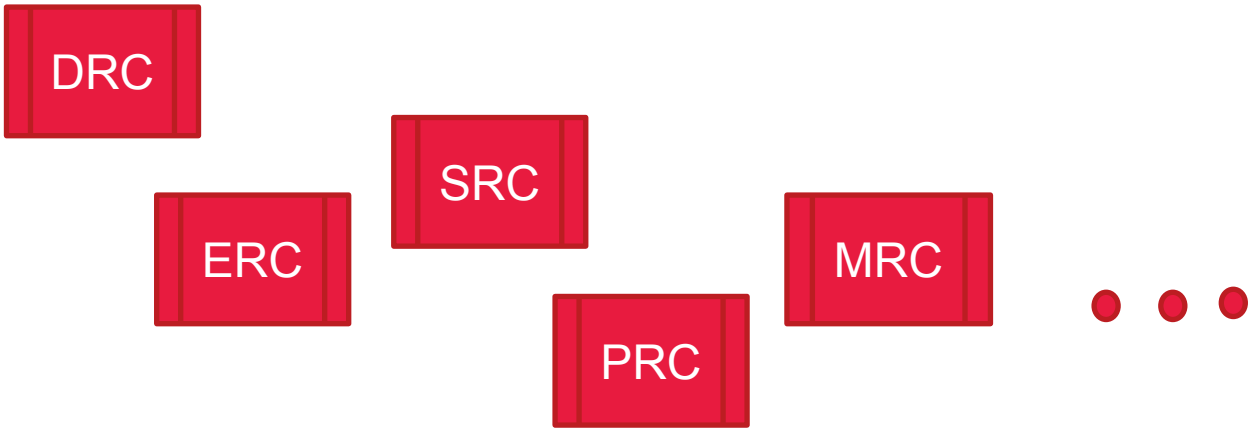


Off Angle Fit

OrCAD ERC/SRC Check

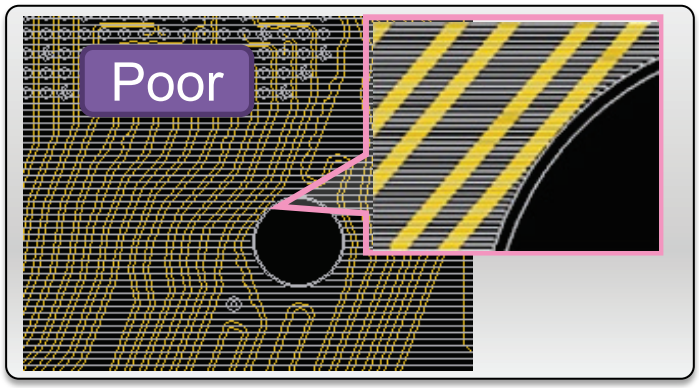
DRC/ERC/…?

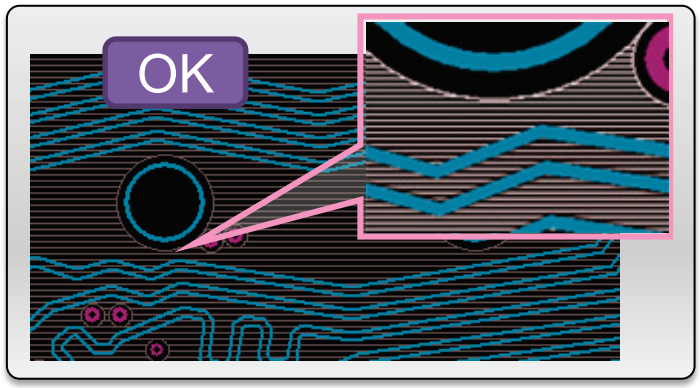
- A bunch of design rules need to implement in your design.
- To check and verify layout rules, to meet design requirements.
- It’s hard to make sure layout meets the origin of design.

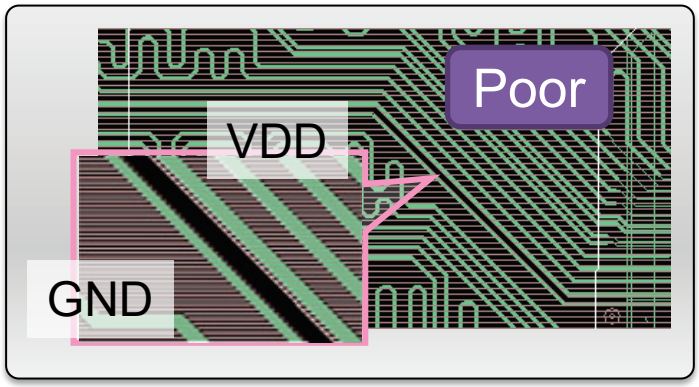


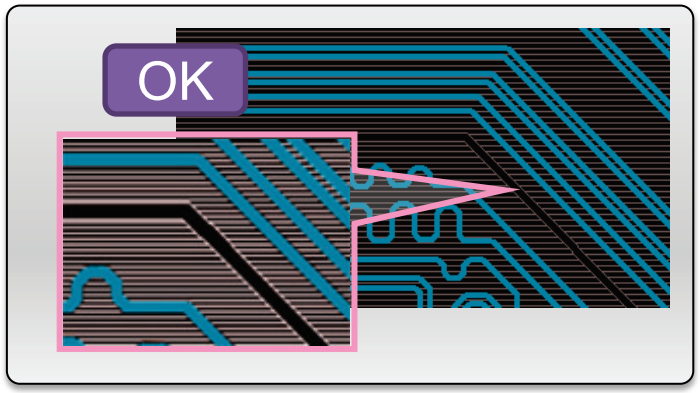
Spacing Constraint Set

Reference Plane Spacing Clearance



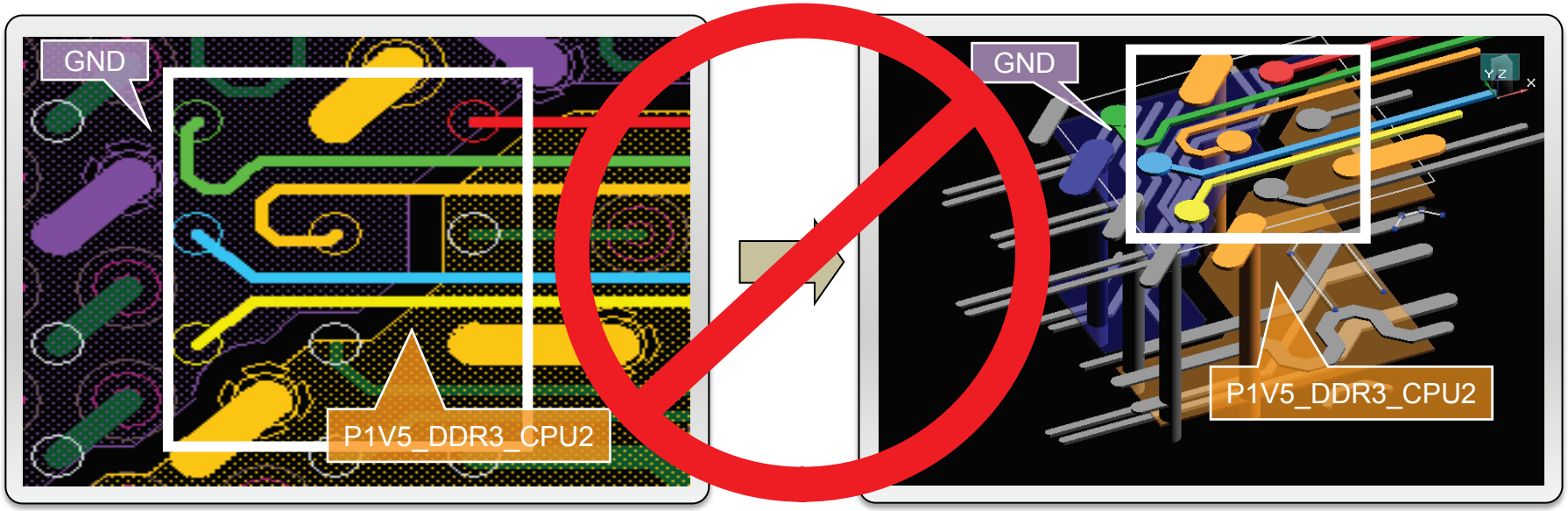






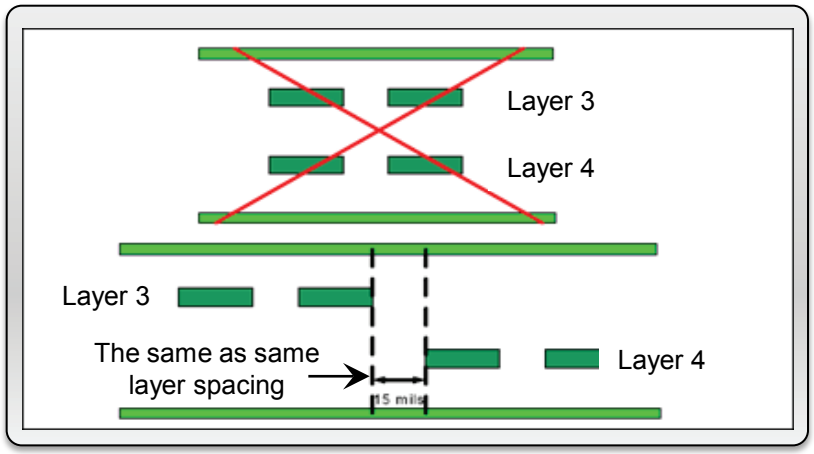
- EMI
- Impedance mismatch

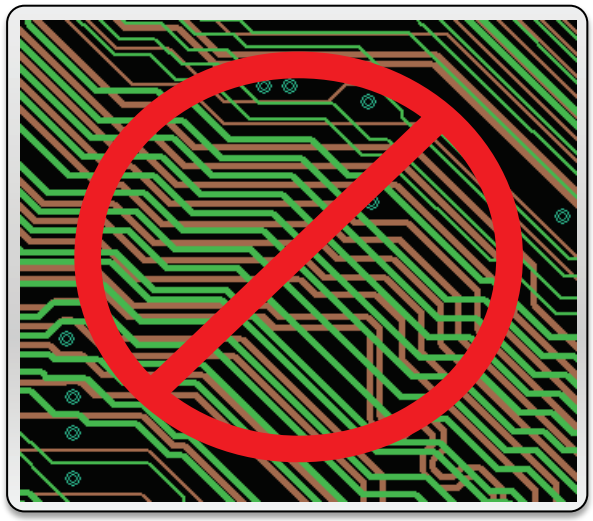
Plane Crossing

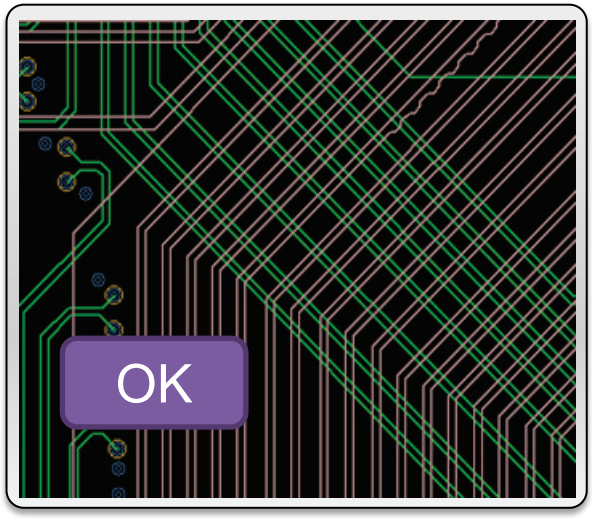


- EMI
- Return current path
- Impedance mismatch
- Signal degradation

Parallelism on Adjacent Layers

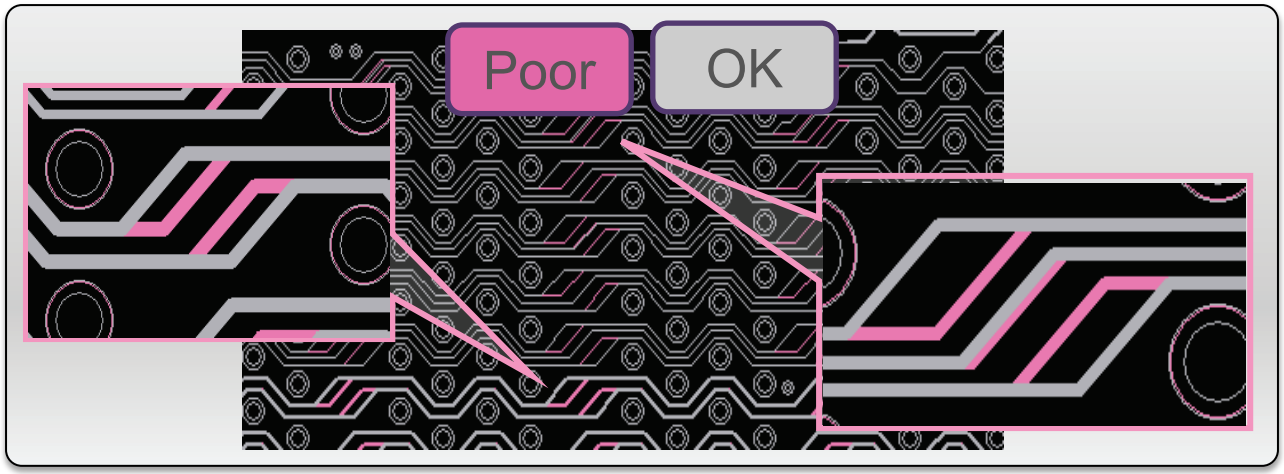


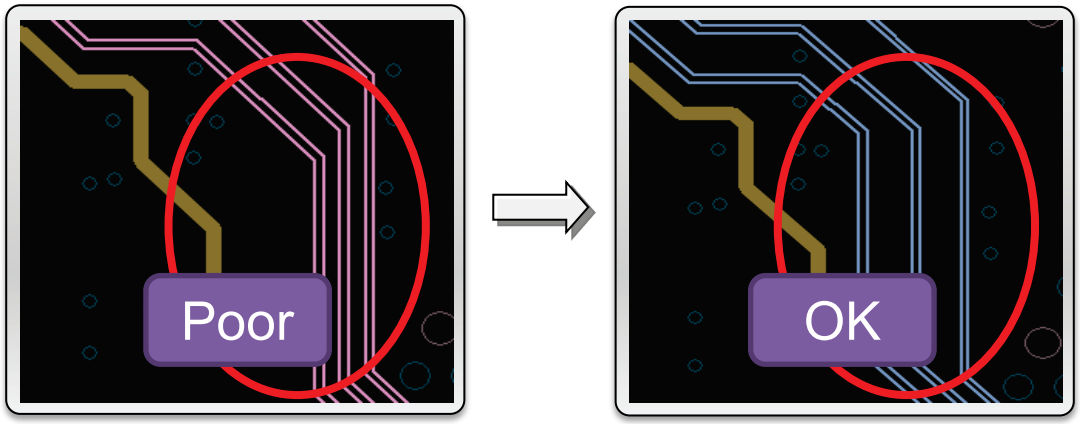




- Crosstalk

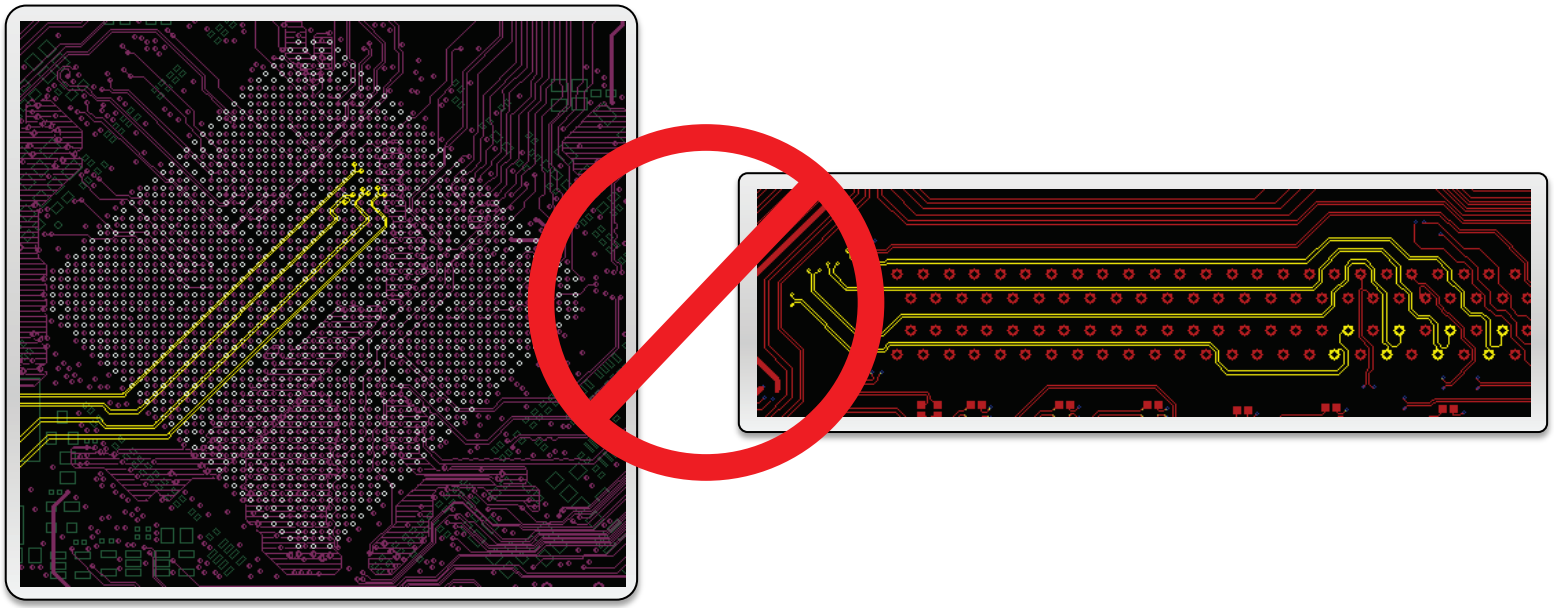
Trace Spacing Distribution





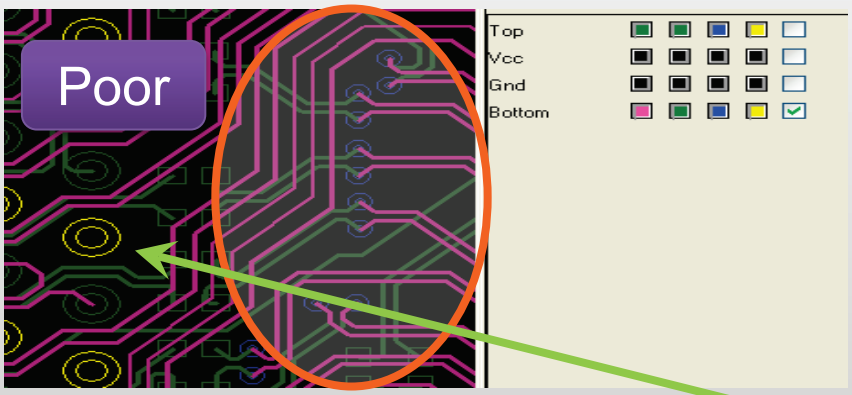
- Crosstalk

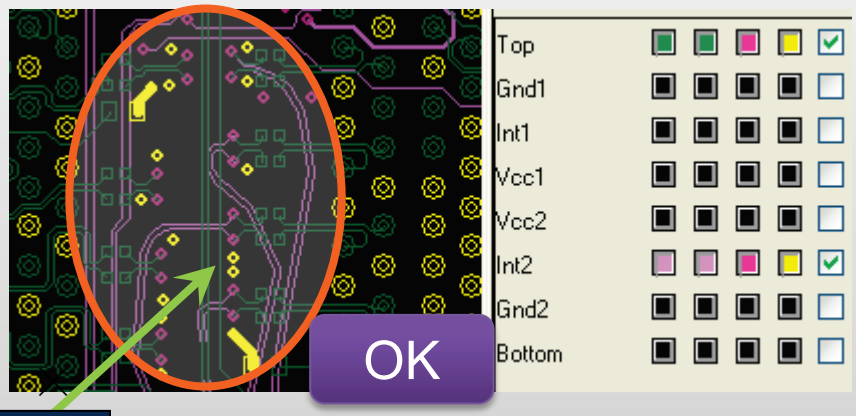
Routing in Connector／Breakout Area



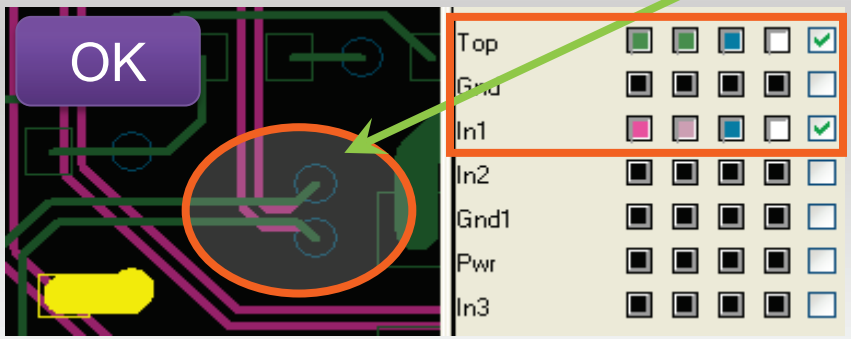
- Impedance mismatch
- Crosstalk

GND Stitching Vias





GND vias

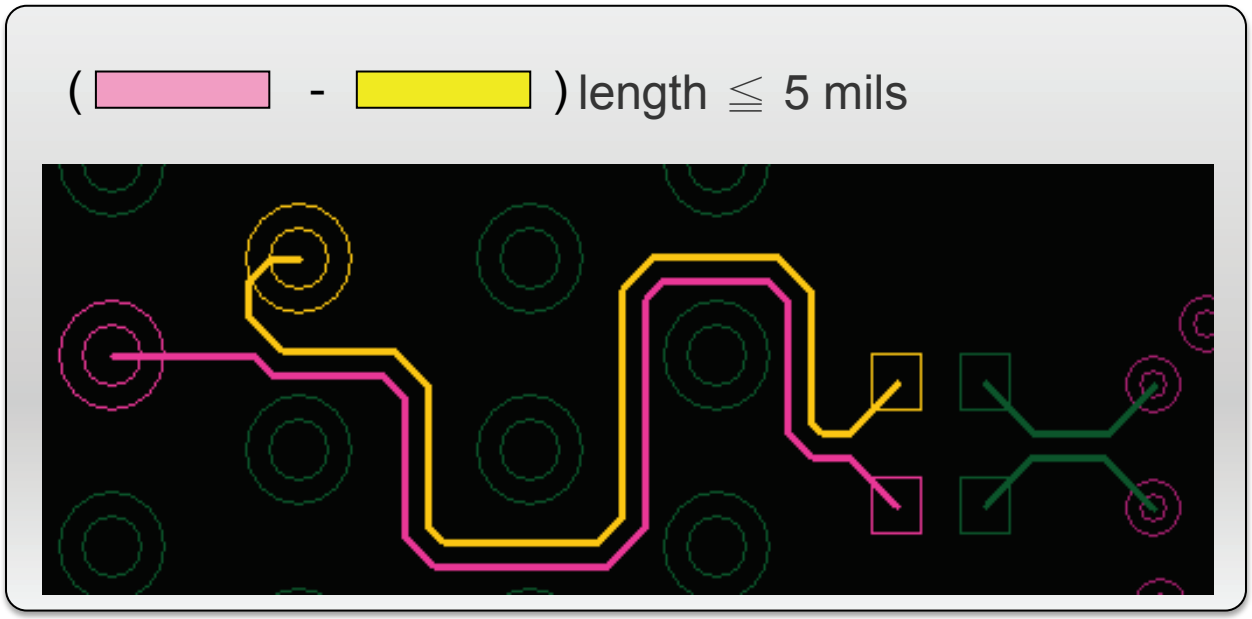


GND stitching via is not necessary for layer changing occurs on adjacent layers because they reference to the same plane.

Return current path

- EMI
- Signal degradation

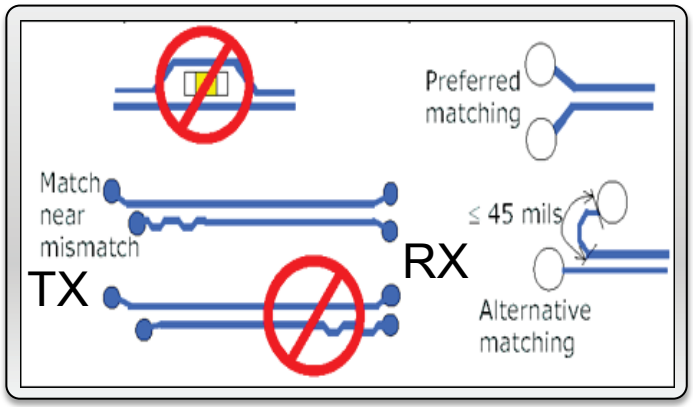
Cline Length Matching (diff. pair)

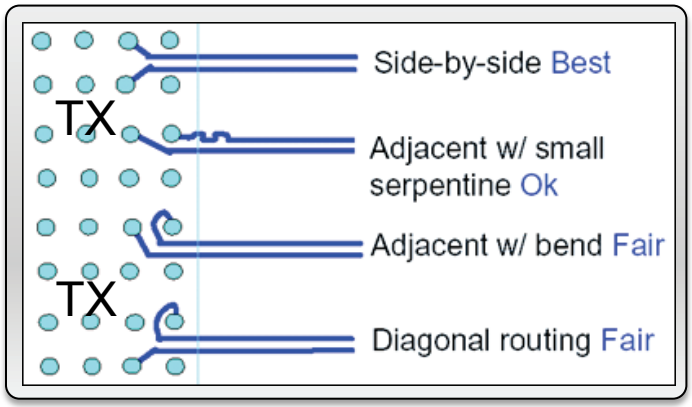


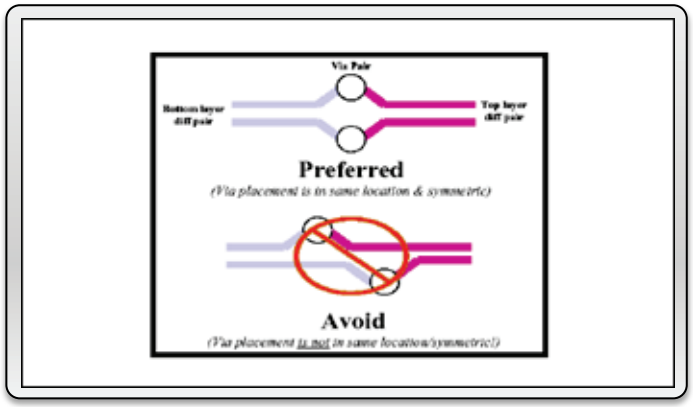
Common mode noise

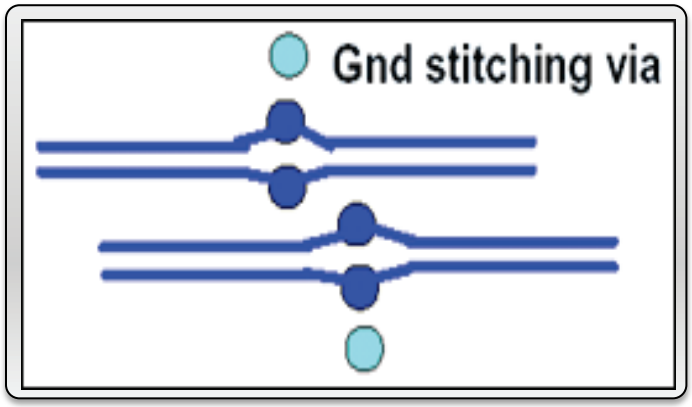
- EMI

General Rules for Differential Pair





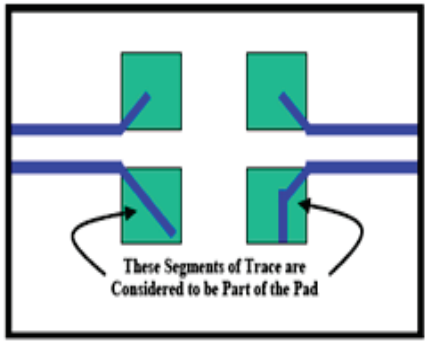




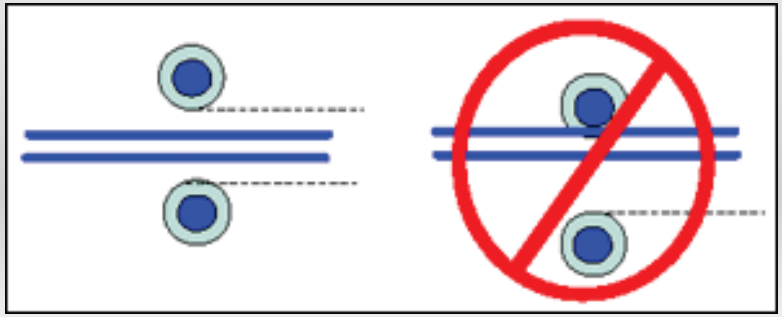
- Common mode noise
- Return current path

General Rules for Differential Pair 2/2

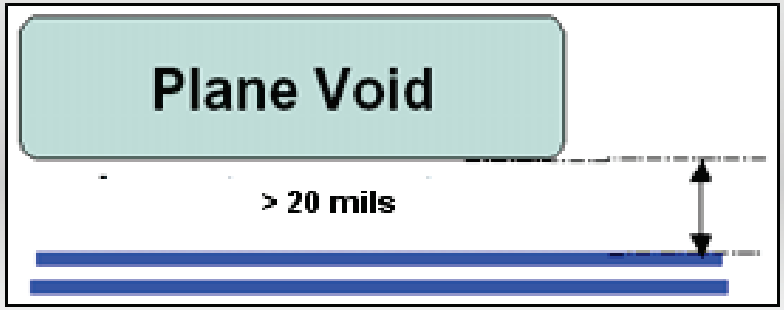
These segments of trace are considered to be part of the pad. Should be avoided.



Avoid trace over anti-pad.

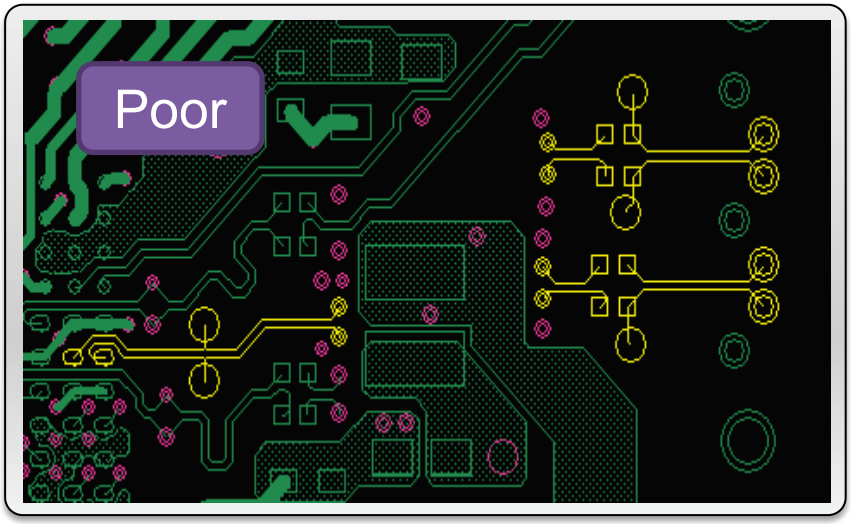


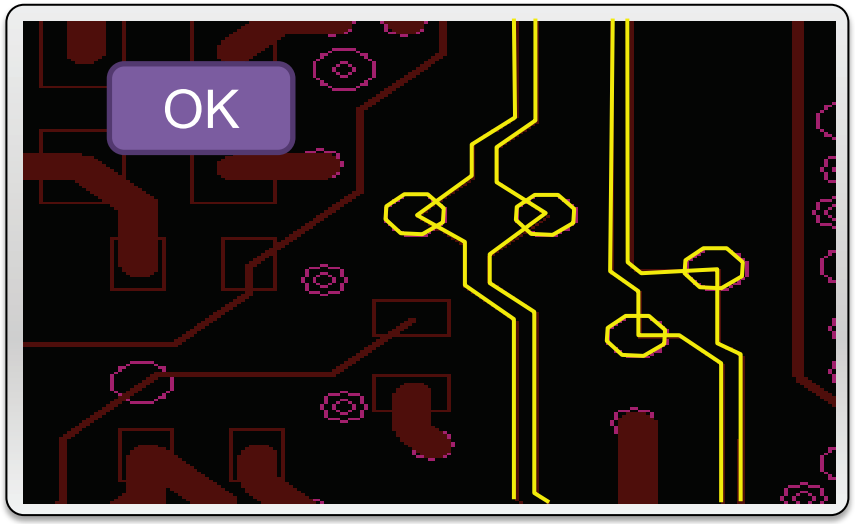
Clearance near plane void.



- Skew
- Impedance mismatch
- EMI

Test Point

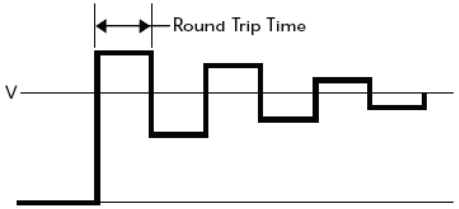




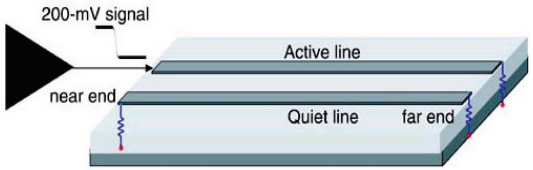
- Impedance mismatch
- Signal reflection

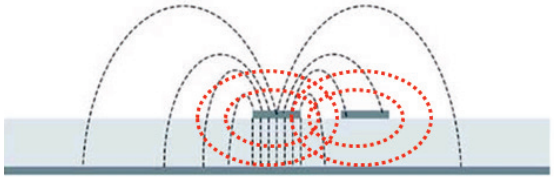
What Are Signal and Power Integrity Addressed Today

- Reflection noise (ringing)
  - Impedance mismatch

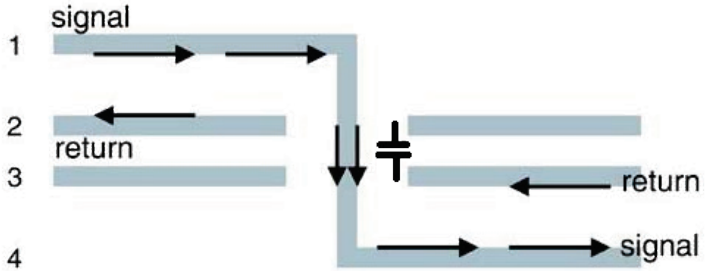


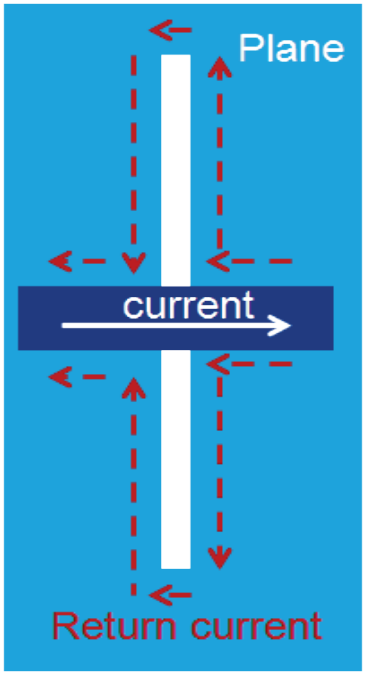
- Crosstalk noise
  - Electromagnetic coupling between adjacent signal lines





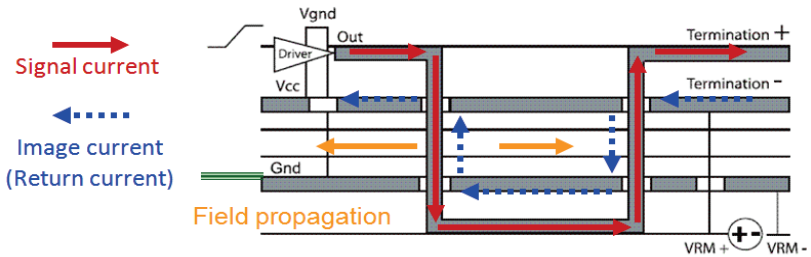
- Discontinuity of signal's current return path
  - Layer transition or across split planes

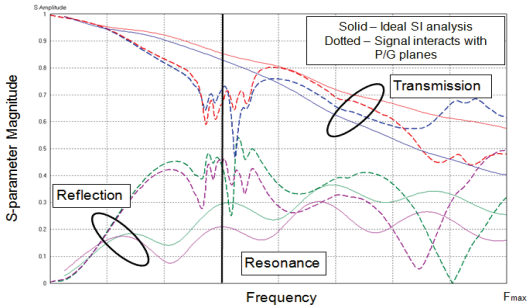




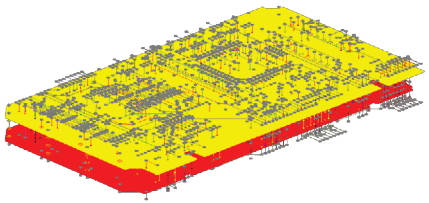
What Are Signal and Power Integrity Addressed Today

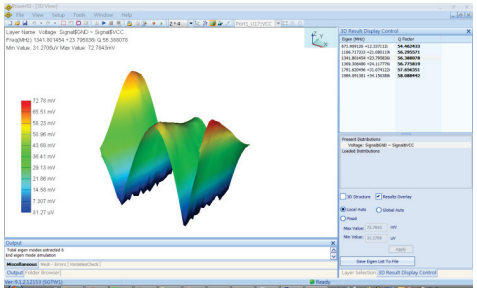
- Interaction between the signal and power distribution systems



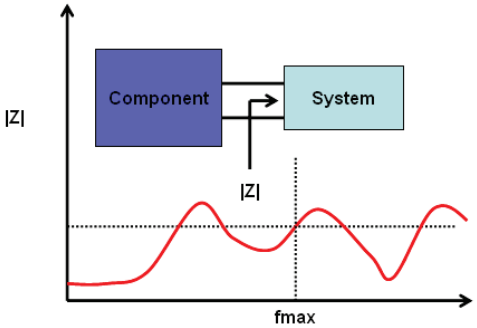


- Resonance on power／ground planes

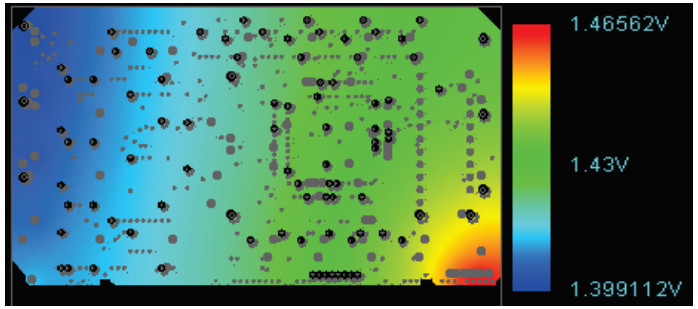




- Low P／G resistance (DC) and impedance (AC)

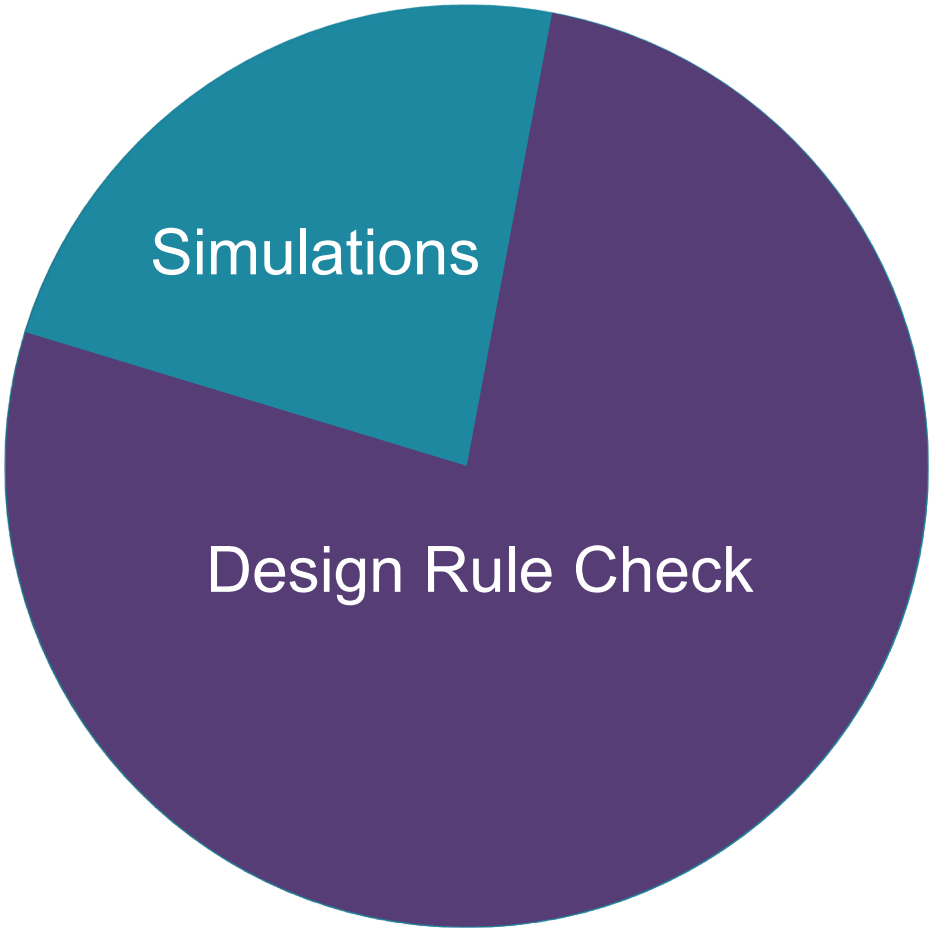


Voltage Distribution Plot



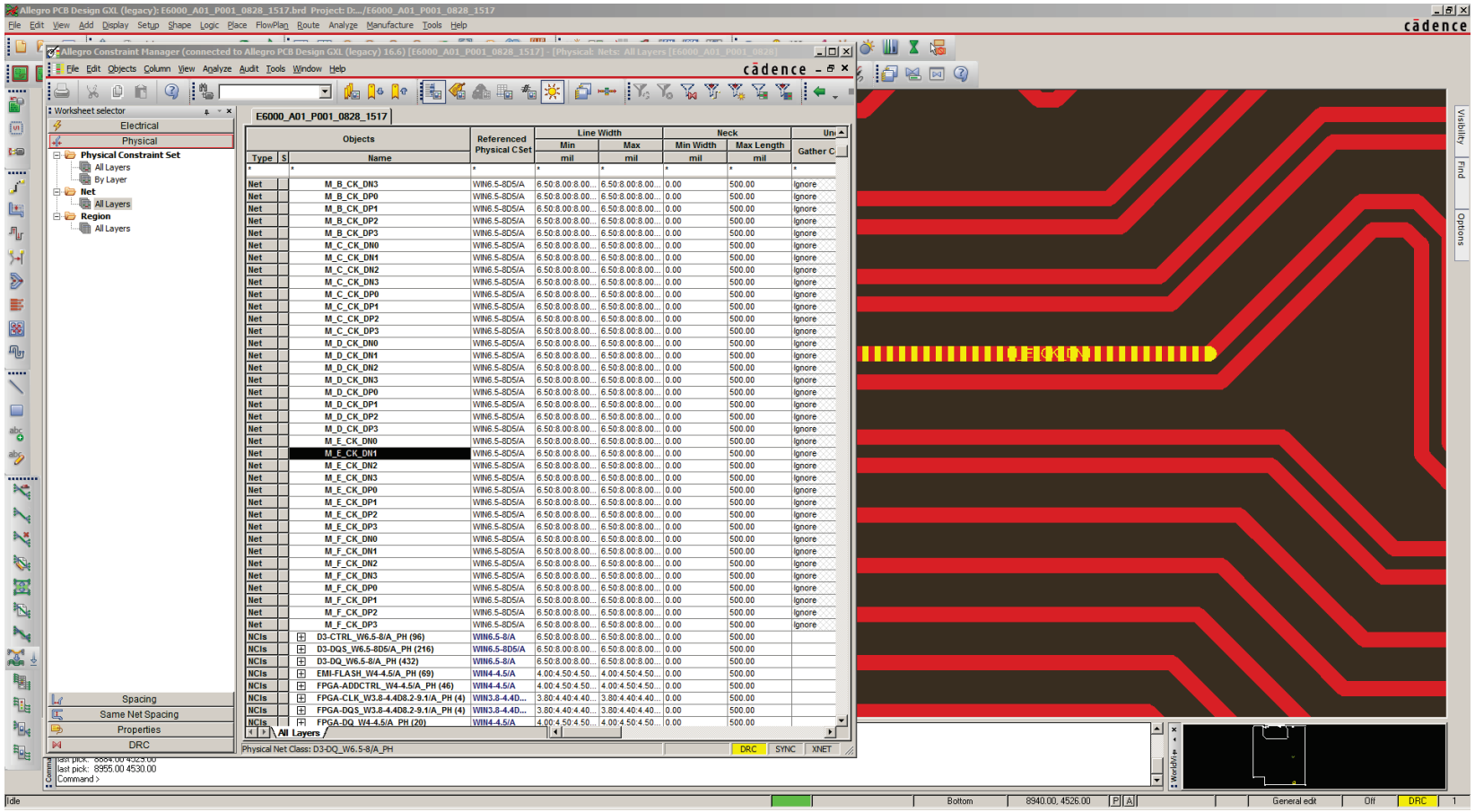
Simulation and Design Rule Check

- All designs are supposed to be 100% covered by simulation results.
- Simulation results will be derived into rules and applied to similar designs.
- The rest of the customized part will be covered by simulation.
- The DRC usually contains only the dimensions information, such as length, width, distance, spacing…etc.
- What does this dimension constraint / DRC forget to tell you?

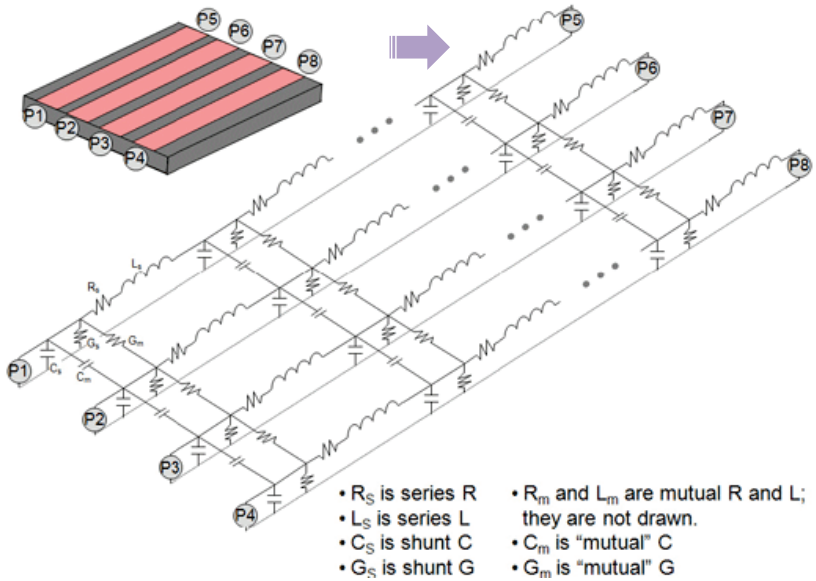


About SI – 1. RLGC Information

- In a well-controlled design, with/without DRC only tells you if the width/spacing follows rules or not. But how's the RLGC information?

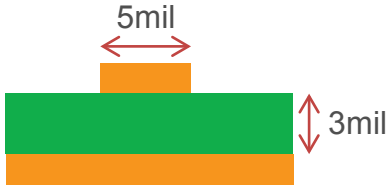


About SI – 1. RLGC Information

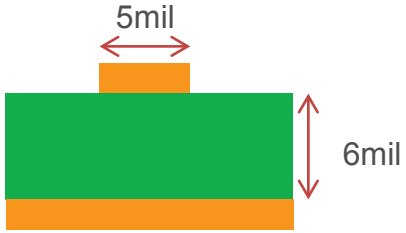


- The generation of equiv. RLGC circuit needs EM calculations.
- Simple design rule check for dimension will not tell you the RLGC value.
- Try to imagine the following case:

Case 1:



Case 2:



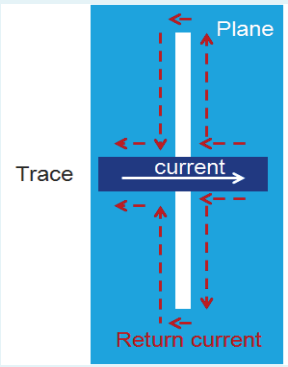
Questions:

1. Are the DRC results of these 2 structures the same or different? **Same**
2. Do these 2 structures have the same or different RLGC properties? **Different**
3. Do these 2 structures have the same impedance or not?

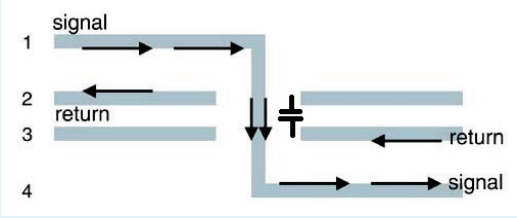
About SI – 2. Z0 and Xtalk

- Talk about impedance Z_0, and let's see the following case :

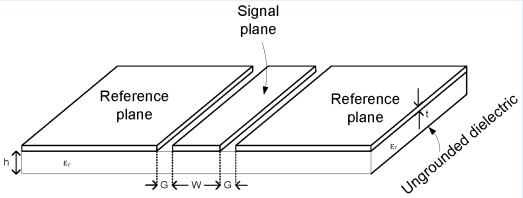
After simulation, you set the trace width to be 5 mil in the constraint system to achieve the impedance you want. Of course, the following picture will show **no DRC** violation. **But if this is a 2-layers design and…**



1. Reference change
2. Cross plane split



1. Layer Transistion

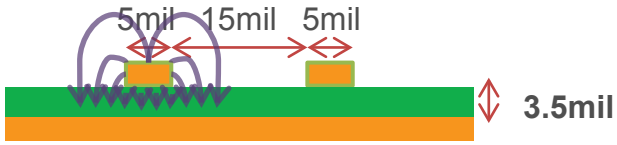


1. Coplarar reference

About SI – 2. Z0 and Xtalk

- Talking about crosstalk, you probably follow the 3W rule – set the spacing between adjacent traces to 3 times the width of the trace as the following :

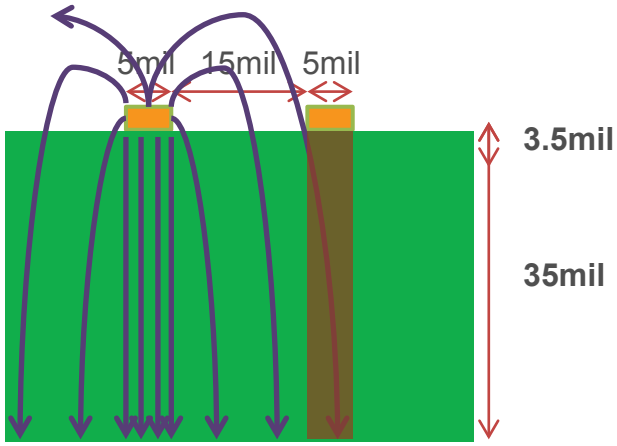
- The 3W rule may work well for the following structure:



No DRC violation ➡ No Xtalk issue

About SI – 2. Z0 and Xtalk

- But if the stack-up looks like the following, will 3W rule still work well?



No DRC violation ➡ No Xtalk issue ?

- Now, you're not satisfied with simply spacing constraint or the related **DRC** violation warning. You feel you probably need **simulation** or other way to tell you:

How Much the Coupling is

The Gap between DRC and SI Performance

- The gap between layout designers and SI engineers is huge
  - Have different design expertise
  - Using different tools
  - Measured by different units

DRC
Design Rule Check

Gap

Simulation
Using Device Models

Layout/Board designer	*SI engineer*
Layout tools	*Simulation tools*
Geometry domain (mil/mm)	*Electrical domain (mv, ps)*

Why You Need Electrical Rule Check

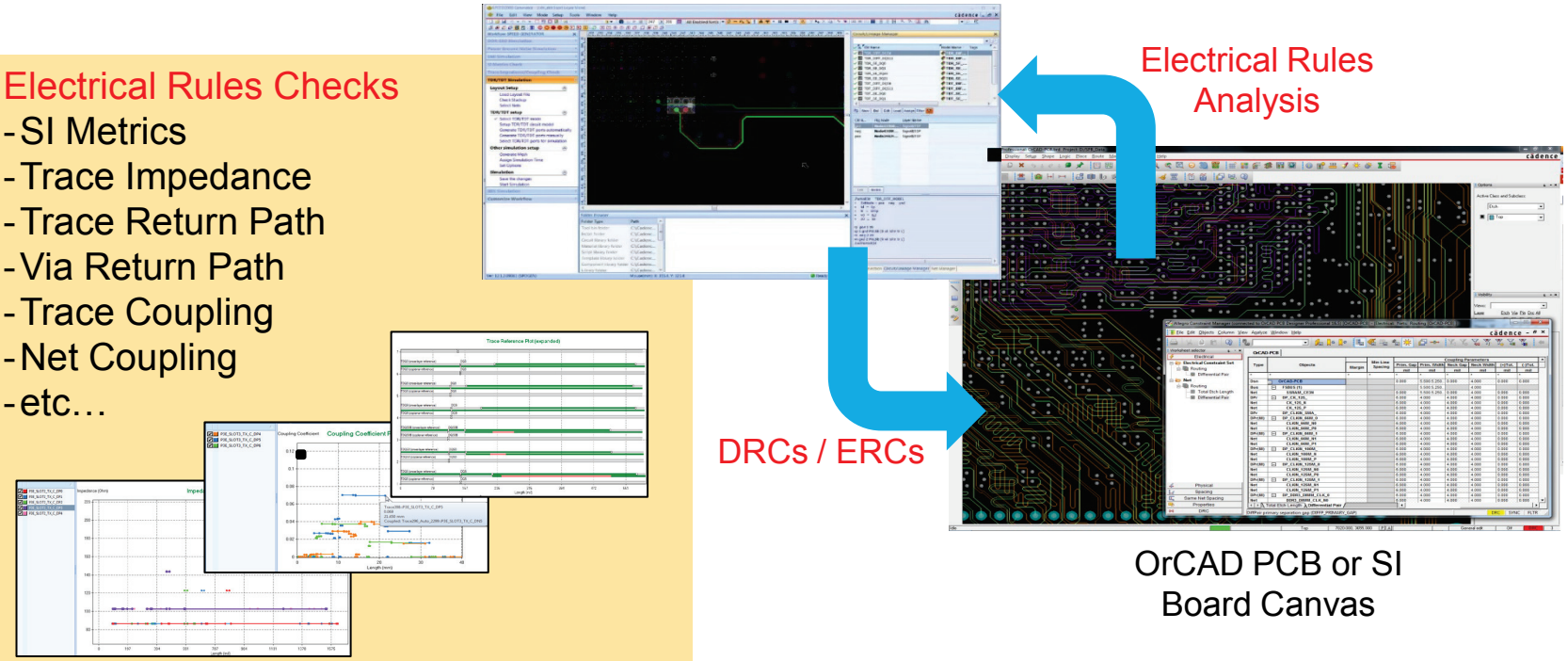
- ERCs are better than DRCs for ‘signal quality’ validation
  - Goes beyond **MINIMUM-ACCEPTANCE, GEOMETRY-BASED** constraint validation
- PCB designers identify and address first-order signal quality issues

OrCAD Sigrity ERC

- A comprehensive set of electrical signal quality checks for PCB enabling the PCB designer to make needed changes before more extensive and exhaustive analysis is performed.

OrCAD Sigrity ERC

Electrical Rules Checks
- SI Metrics
- Trace Impedance
- Trace Return Path
- Via Return Path
- Trace Coupling
- Net Coupling
- etc…



OrCAD PCB or SI Board Canvas

What is Sigrity ERC?

- Sigrity ERC is individual, segment-level view in geometry domain for PCB's SI performance with
  - Trace reference
  - Trace reference-aware impedance
  - Trace reference-aware coupling
  - Differential pair routing phase
  - # of vias and via locations, ….

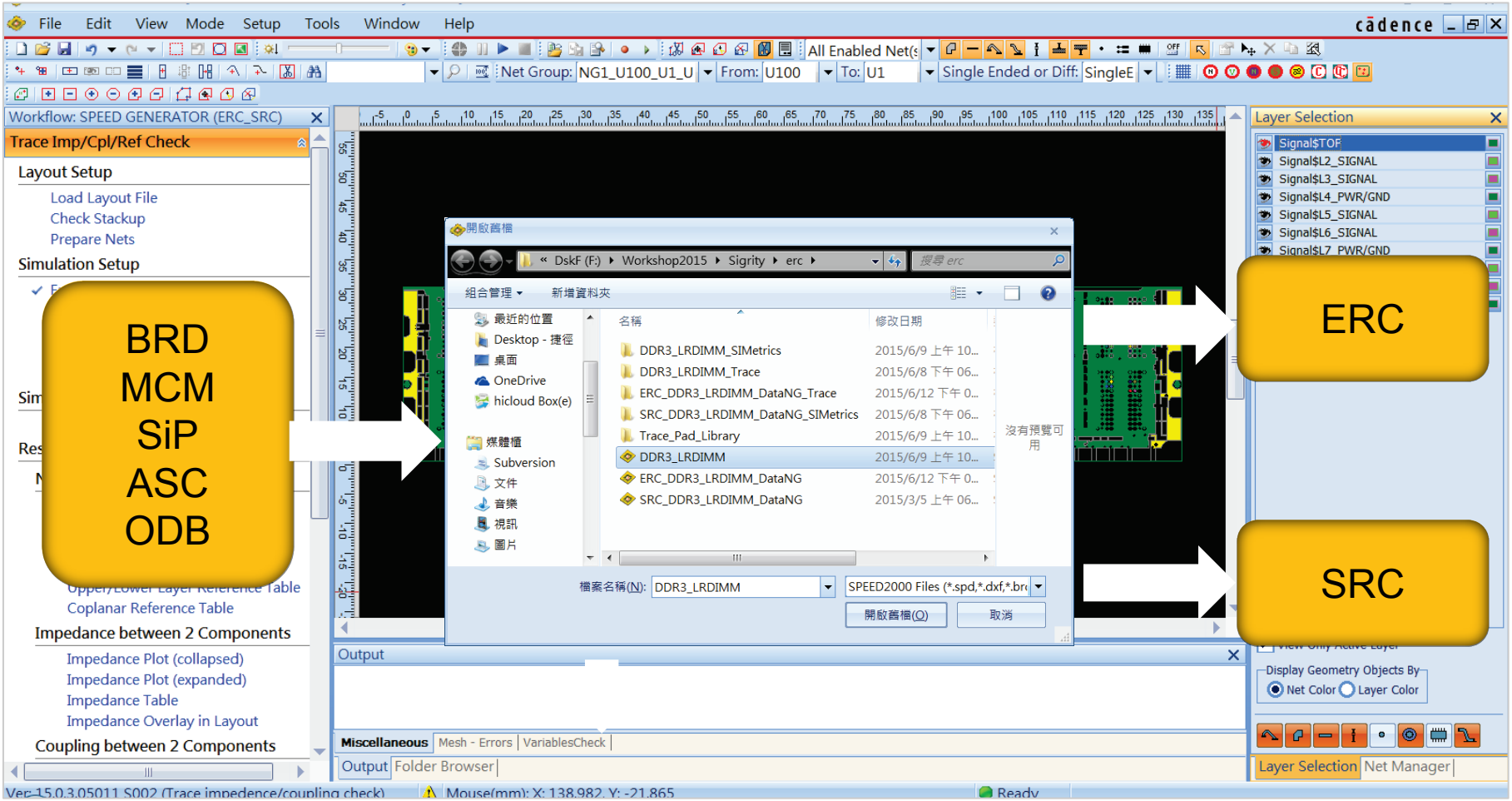
1

  - Organized for easy SI performance interpretation
  - Practical for board level check (setup, simulation, report)

<2min 10-20min auto

2

Sigrity ERC/SRC Checking Flow



ERC HTML Report

4.1 Net group NG1_J1_U0_U4

Click to expand/collapse

4.1.1 From J1 To U0

4.1.2 From J1 To U4

4.2 Net group NG1_J1_U0_U1_U2_U3_U4_U5_U6_U7

cādence

SPEED2000 TRACE IMPEDANCE/COUPLING CHECK REPORT

Date: 8:51 August 13, 2014

For SPB tech session

1 General information

1.1 Spd file name and location

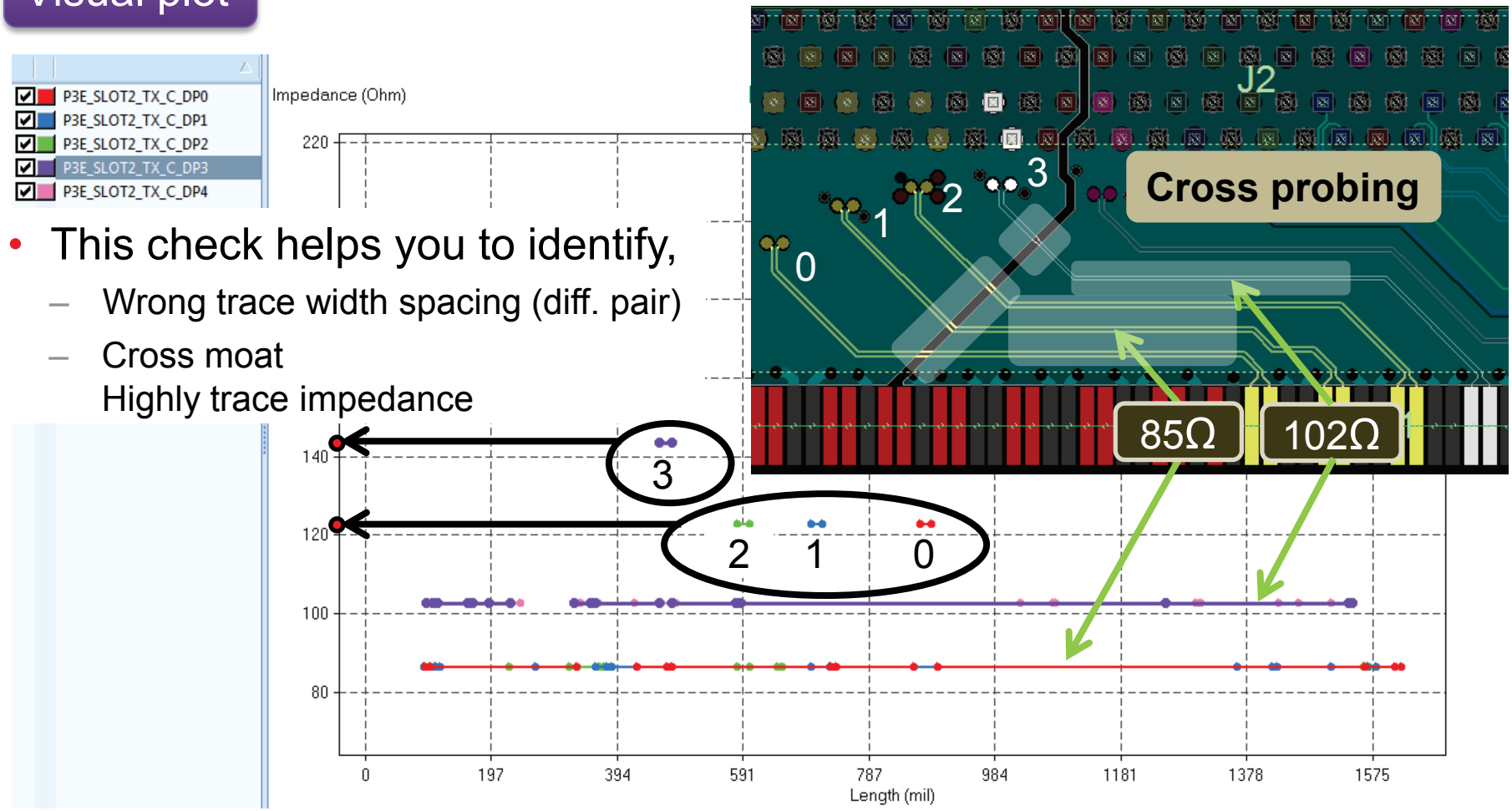
SPDGEN version: 14.0.2.07112

File names and locations:

- Layout spd file
  - D:/Backup/3_Training/TraceCK/movie/TraceCK_sim_NG/SODIMM_TraceCK.spd
- Trace check results file
  - D:/Backup/3_Training/TraceCK/movie/TraceCK_sim_NG/SODIMM_TraceCK_Trace/TraceCKResult_SODIMM_TraceCK_080414_142728_result.xml
  - D:/Backup/3_Training/TraceCK/movie/TraceCK_sim_NG/SODIMM_TraceCK_Trace/SODIMM_TraceCK_ImpSum_080414_142728.csv
  - D:/Backup/3_Training/TraceCK/movie/TraceCK_sim_NG/SODIMM_TraceCK_Trace/SODIMM_TraceCK_ImpDetailed_080414_142728.csv
  - D:/Backup/3_Training/TraceCK/movie/TraceCK_sim_NG/SODIMM_TraceCK_Trace/SODIMM_TraceCK_CplSum_080414_142728.csv
  - D:/Backup/3_Training/TraceCK/movie/TraceCK_sim_NG/SODIMM_TraceCK_Trace/SODIMM_TraceCK_CplDetailed_080414_142728.csv
  - D:/Backup/3_Training/TraceCK/movie/TraceCK_sim_NG/SODIMM_TraceCK_Trace/SODIMM_TraceCK_UpperLowerRefSum_080414_142728.csv

Trace Impedance Check

Visual plot

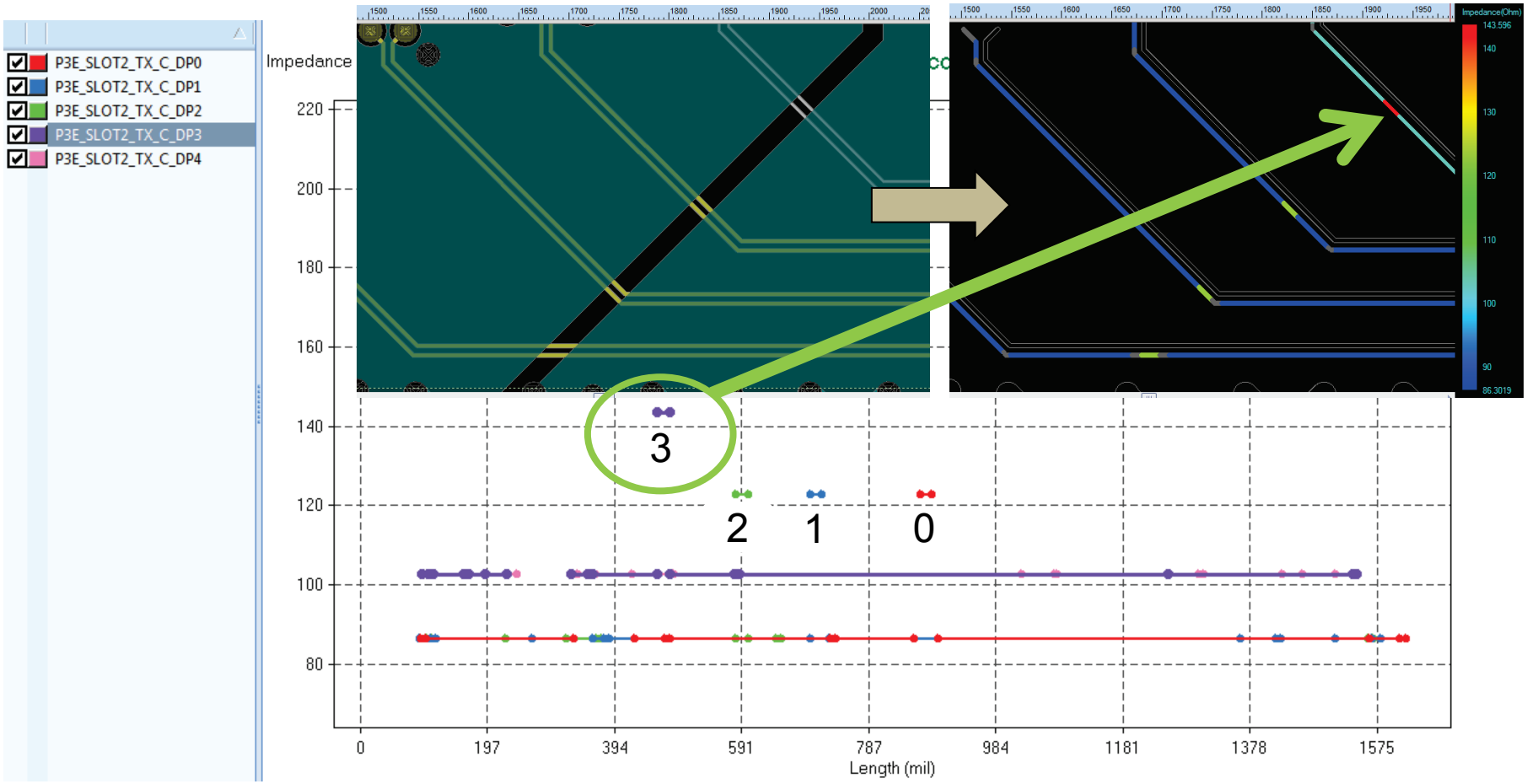


- This check helps you to identify,
  - Wrong trace width spacing (diff. pair)
  - Cross moat
    Highly trace impedance

- Visually or tabular result for trace impedance check that shows trace segments mismatch with target impedance.

Trace Impedance Check

Cross Probing



- Cross probing allows you to identify defects quickly.

Trace Impedance Check

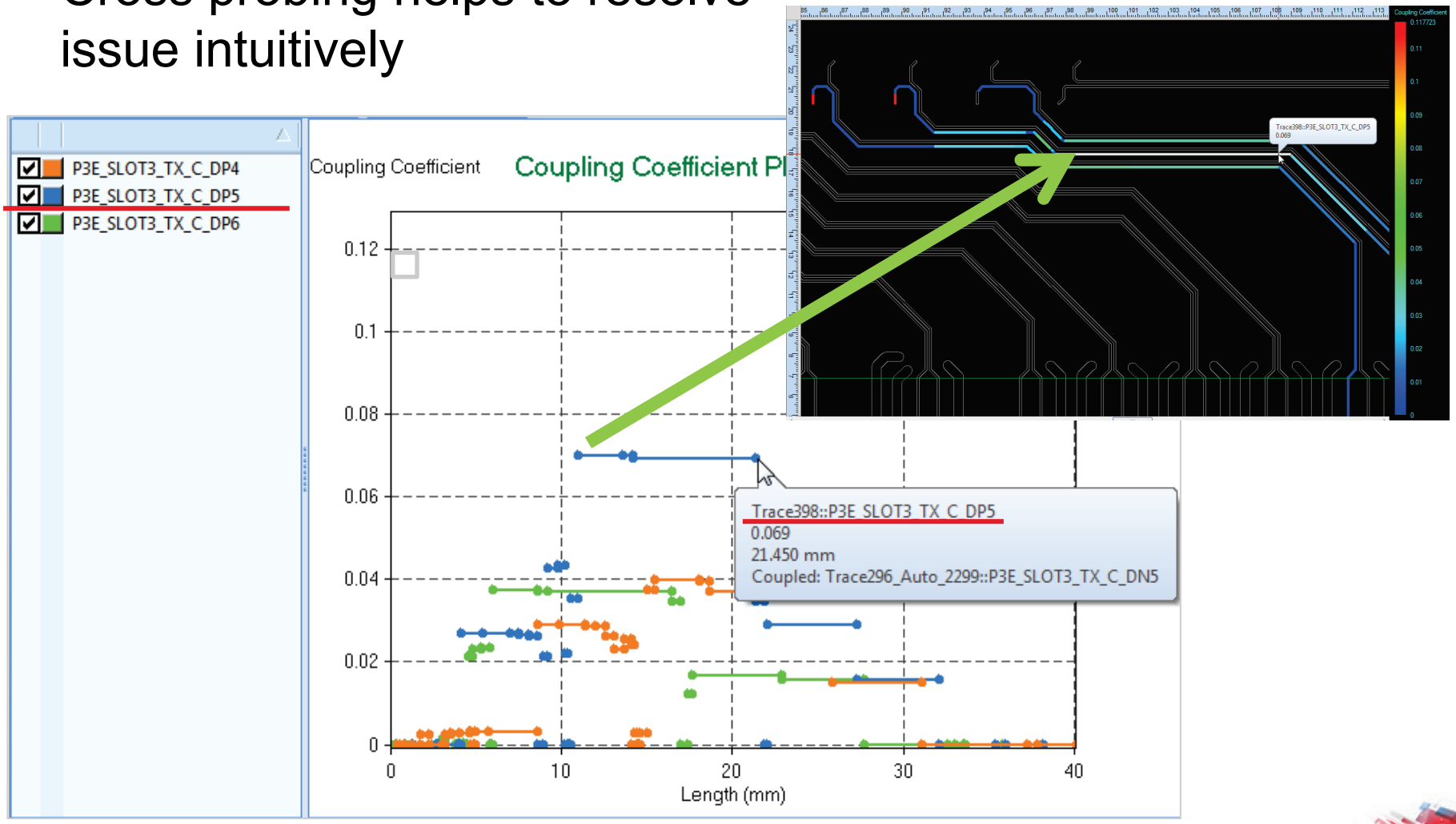
Tabular Results

Net count	Net name	No. of segments without reference	No. of trace reference discontinuities	No. of vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)	Dominant Impedance (Ohm)	Dominant Imp Length (%)	Trace total length (mil)	Trace delay(ns)
1	P3E_SLOT2_TX_C_DN0	1	3	2	144.946	56.449	56.449	92.921	1633.158	0.233
2	P3E_SLOT2_TX_C_DN1	1	3	2	144.946	56.449	56.449	93.168	1583.722	0.225
3	P3E_SLOT2_TX_C_DN2	1	3	2	144.946	56.449	56.449	93.186	1575.168	0.224
4	P3E_SLOT2_TX_C_DN3	1	3	2	153.005	63.836	63.836	93.074	1549.678	0.220
5	P3E_SLOT2_TX_C_DN4	1	1	2	63.836	63.836	63.836	94.228	1513.121	0.214
6	P3E_SLOT2_TX_C_DP0	1	3	2	144.946	56.449	56.449	92.923	1633.643	0.233
7	P3E_SLOT2_TX_C_DP1	1	3	2	144.946	56.449	56.449	93.221	1583.404	0.225
8	P3E_SLOT2_TX_C_DP2	1	3	2	144.946	56.449	56.449	93.184	1574.865	0.224
9	P3E_SLOT2_TX_C_DP3	1	3	2	153.005	63.836	63.836	93.059	1546.528	0.219
10	P3E_SLOT2_TX_C_DP4	1	1	2	63.836	63.836	63.836	94.221	1511.225	0.214
11	P3E_SLOT3_TX_C_DN0	1	1	1	56.449	56.449	56.449	94.142	1490.958	0.211
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	0.208
										0.217
										0.209
										0.225
										0.214
										0.203
										0.212
										0.212
										0.209
										0.217
										0.210
										0.225
										0.214
										0.203
										0.212

- Cross moat?
- Any trace segment mismatch? Cross moat?
- Too much breakout neck length?
- Too much MS/SL routing difference in a group?
- The same trace length means the same trace delay?
- Routing on MS/SL has different trace delay.

Trace Coupling Check

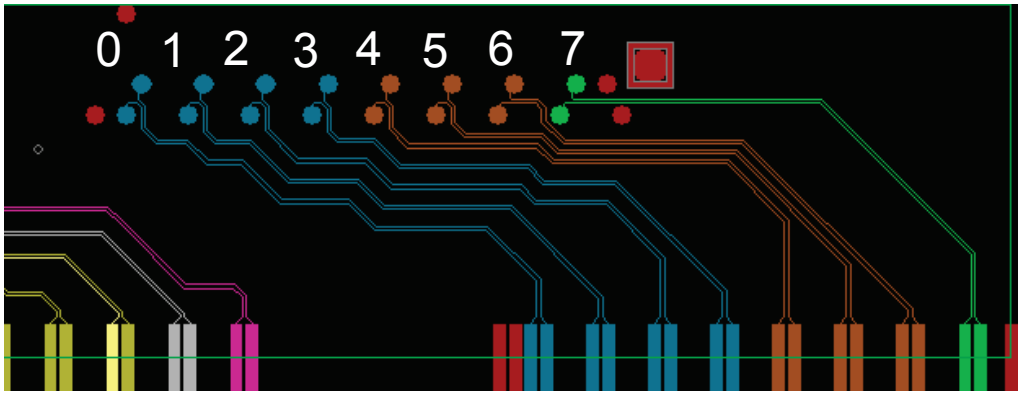
- Cross probing helps to resolve issue intuitively



Trace Coupling Check

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
1	P3E_SLOT2_TX_C_DP0-P3E_SLOT2_TX_C_DN0	P3E_SLOT2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
2	P3E_SLOT2_TX_C_DP1-P3E_SLOT2_TX_C_DN1	P3E_SLOT2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
3	P3E_SLOT2_TX_C_DP2-P3E_SLOT2_TX_C_DN2	P3E_SLOT2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
4	P3E_SLOT2_TX_C_DP3-P3E_SLOT2_TX_C_DN3	P3E_SLOT2_TX_C_DN2	0.125%	36.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.125%	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

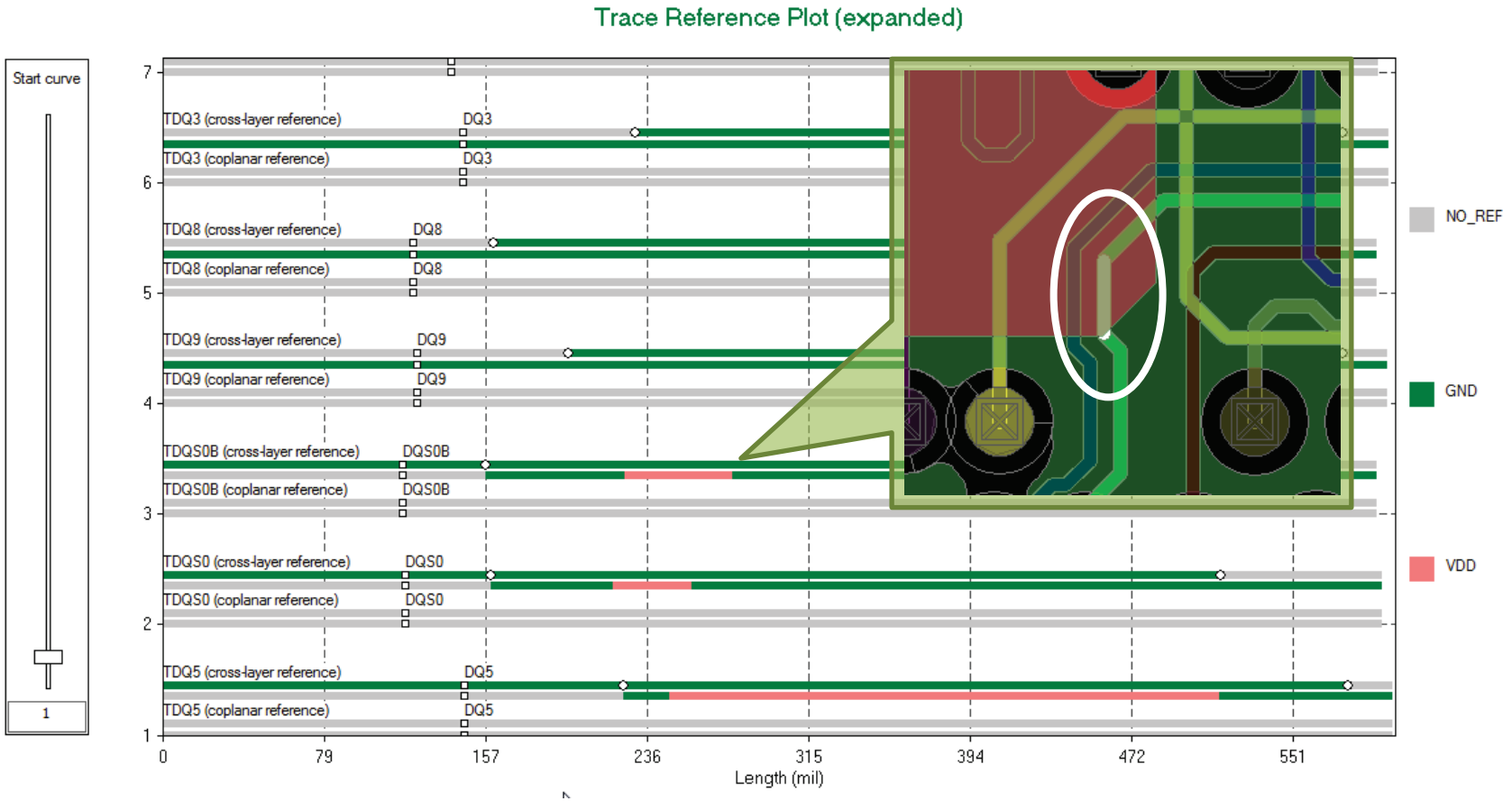
18X



Through this test, you will see,

- Tight coupling pairs
- Max coupling aggressor
- Dangerous vs. safe coupling → **18X** (= 2.81% / 0.156%)

Trace Reference Check (Including co-planar)

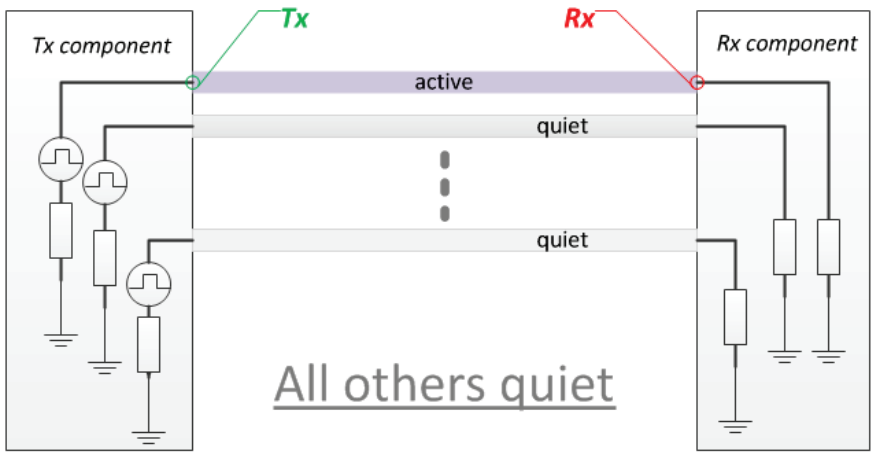


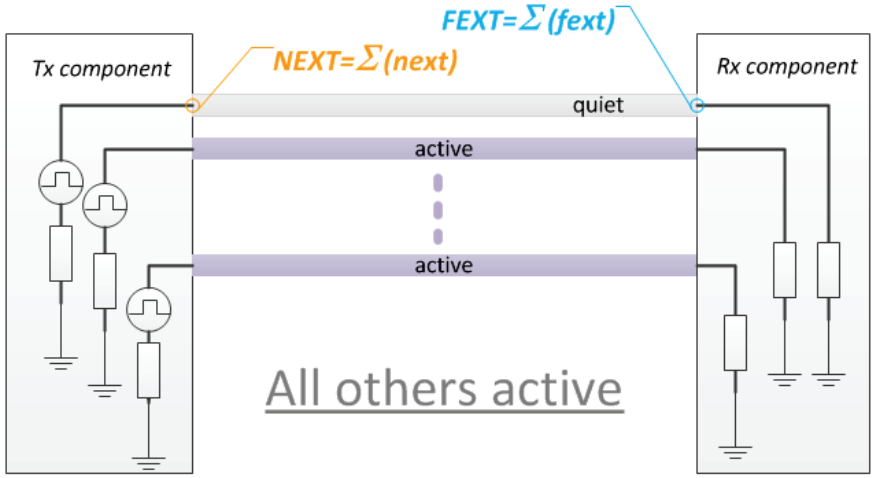
- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

What is Sigrity SRC?

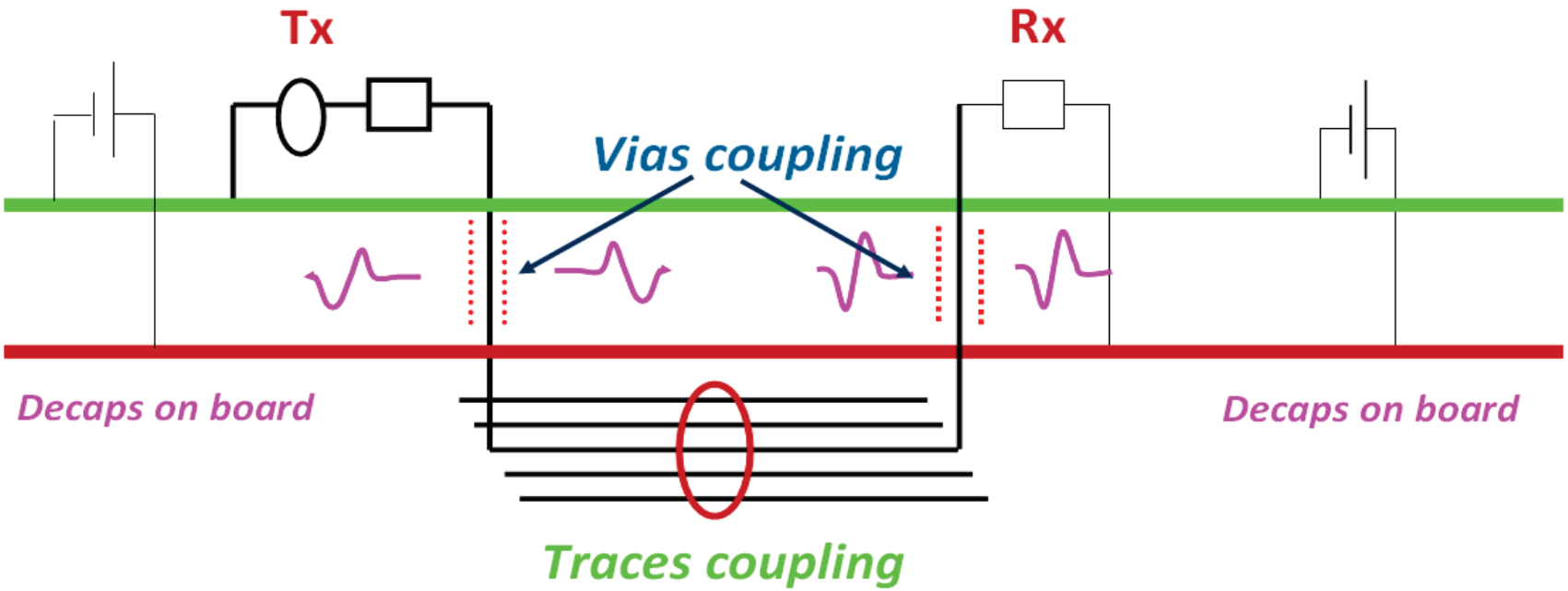
- Sigrity SRC is Macro, combined, net-level view in time-domain of impact due to ERC violations measured in mv&ps (no device model needed)
  - Setup considering termination impedance, data rate (pulse width, rise／fall time), and amplitude
  - Results with Tx／Rx／NEXT／FEXT waveforms, SI performance metrics
  - Organized to easy SI performance interpretation along with ER
- Practical for board level check (setup, simulation, report)

<2min ~ 20min auto



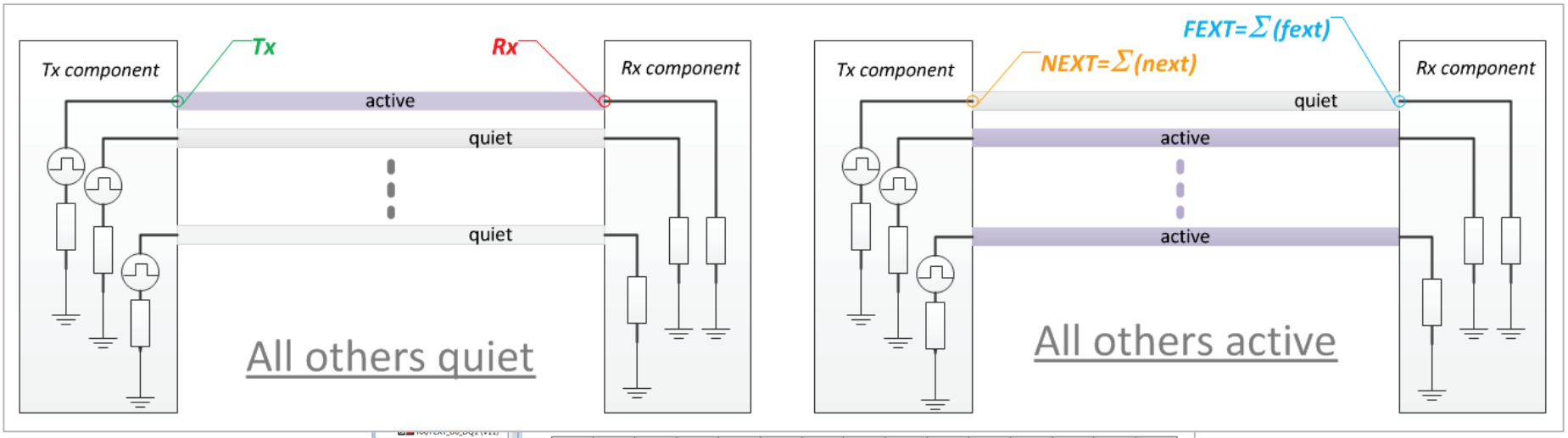


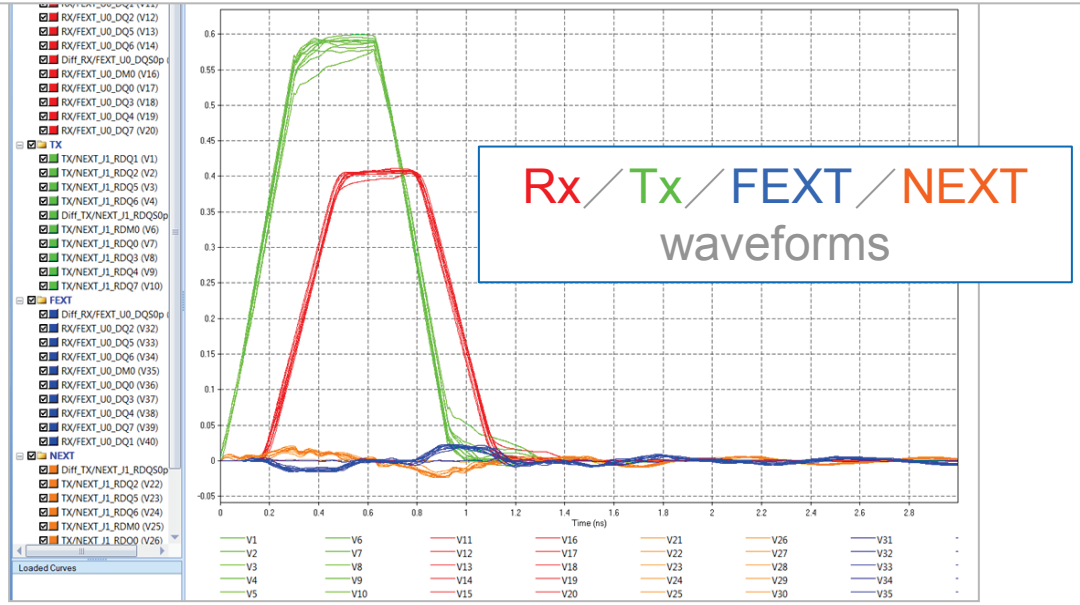
SI Channel Check



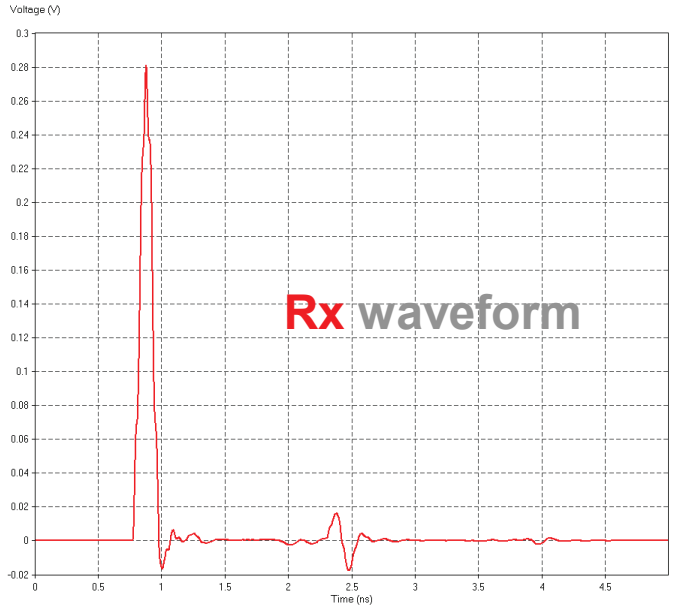
- Signal quality is affected by crosstalk among signals, EM coupling between signal and P／G planes and non-ideal return current path.
- The linear source and load are applied automatically for signal TD simulation
- Post process result waveforms (signal waveform, NEXT／FEXT waveforms) into signal to noise ratio for signal quality judgment

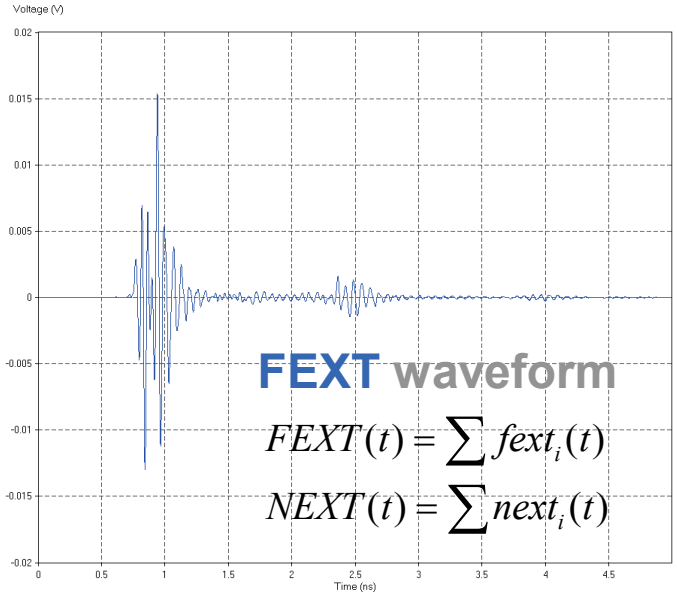
Time-domain Waveforms





SI Metrics





- SI metrics are defined using magnitudes of Rx and FEXT

$$Int\_sig = \int_{t_1}^{t_2} |Rx(t)| dt$$

$$Int\_ISI = \int_0^{t_1} |Rx(t)| dt + \int_{t_2}^{t_{\max}} |Rx(t)| dt$$

$$Int\_xtk = \sum \int_0^{t_{\max}} |fext_i(t)| dt$$

$$SN\_difference = (Int\_sig) - (Int\_ISI) - (Int\_xtk)$$

$$SN\_ratio = \frac{Int\_sig}{(Int\_ISI) + (Int\_xtk)}$$

Where

t_1 and t_2 are starting and ending time for the received pulse (1 UI width)

$t_{\max}$ is maximum time-domain simulation time

Net-level Performance Ranking

Net name	INT_Sig (V*ps)	INT_ISI (V*ps)	INT_XTK (V*ps)	SN_difference (V*ps)	SN_ratio
DQ19	287.97	22.96	3.7	261.31	10.8029
DQ17	288.15	22.79	3.12	262.24	11.1223
DM2	286.52	24.21	3.04	259.28	10.5156
DQS2_P	206.59	104.05	0	102.54	1.98541
DQ20	286.71	23.94	3.14	259.63	10.5871
DQ21	288.2	22.68	5.43	260.09	10.2522
DQ16	286.51	24.21	0	262.3	11.834
DQ22	286.46	24.06	1.6	260.8	11.1639
DQ18	286.47	24.12	0	262.34	11.8752
DQ23	286.65	24.13	7.81	254.71	8.97519

← Ranking by SI Metrics

Net name	NEXT Vmax (mv)	NEXT Vmin (mv)	NEXT pk-2-pk (mv)	FEXT Vmax (mv)	FEXT Vmin (mv)	FEXT pk-2-pk (mv)
DM1	0	0	0	0	0	0
DQ10	0	0	0	0	0	0
DQ11	0	0	0	0	0	0
DQ9	19	-18	37	14	-15	29
DQ12	17	-15	32	16	-16	32
DQ8	2	-2	5	3	-3	6
DQ14	0	0	0	0	0	0
DQS1_P	0	0	0	0	0	0
DQ15	17	-16	33	13	-13	27
DQ13	19	-18	37	14	-14	29

← Ranking by xtalk levels

SRC HTML Report

cādence

SPEED2000 SI Performance Metrics Check Report

Date: 12:11 July 30, 2014

this is a tutorial

1 General information

1.1 Spd file name and location

SPDGEN version: 14.0.2.07112

File names and locations:

- Layout spd file
  - D:/Backup/3_Training/SIM/Movie/SIM_movie_sim/tut
- SI metrics check results file
  - D:/Backup/3_Training/SIM/Movie/SIM_movie_sim/tut

2.2 Net group Data_U0_U4

Tx component	Net name	Passive component	Net name	Passive component	Net name	Rx component (active)	Rx component (standby)	Rx component (notpopulated)	FIR filter	Pulse ca
U0	DQ29	-	-	-	-	U4	-	Not populated		v-ed
U0	DQ31	-	-	-	-	U4	-	Not populated		v-edge
U0	DQ30	-	-	-	-	U4	-	Not populated		v-edg
U0	DQS3_N	-	-	-	-	U4	-	Not populated	no	v-max
U0	DQS3_P	-	-	-	-	U4	-	Not populated	no	v-max
U0	DQ28	-	-	-	-	U4	-	Not populated		v-edge
U0	DQ26	-	-	-	-	U4	-	Not populated		v-edge
U0	DQ24	-	-	-	-	U4	-	Not populated		v-edge
U0	DQ27	-	-	-	-	U4	-	Not populated		v-edg
U0	DM3	-	-	-	-	U4	-	Not populated		v-edge
U0	DQ25	-	-	-	-	U4	-	Not populated		v-edge

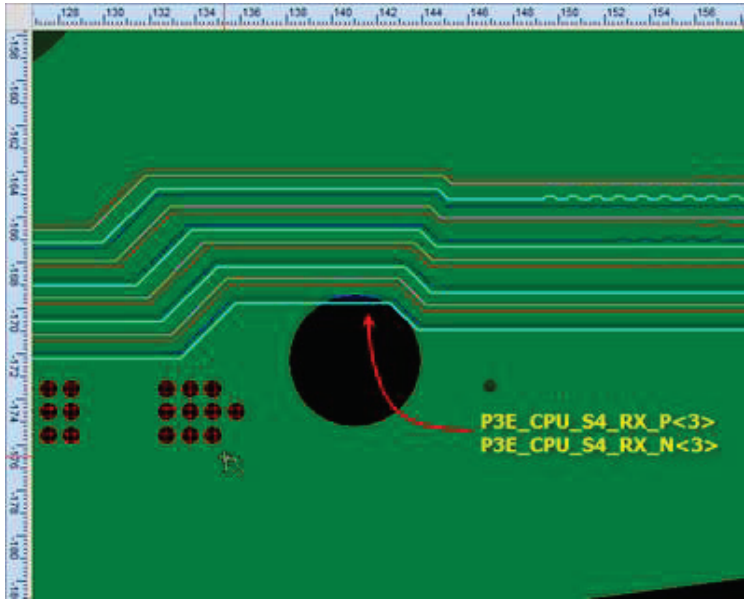
SRC HTML Report – Sort by Columns

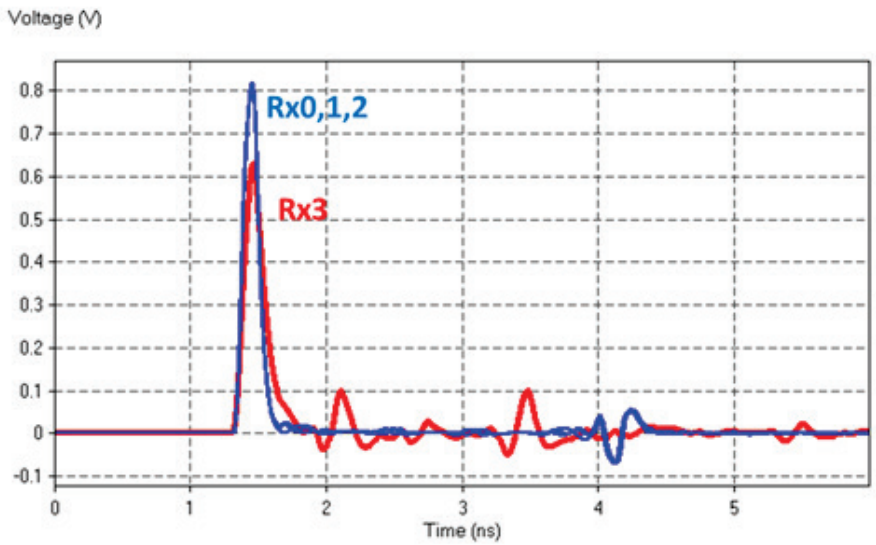
- Click column title to sort by columns

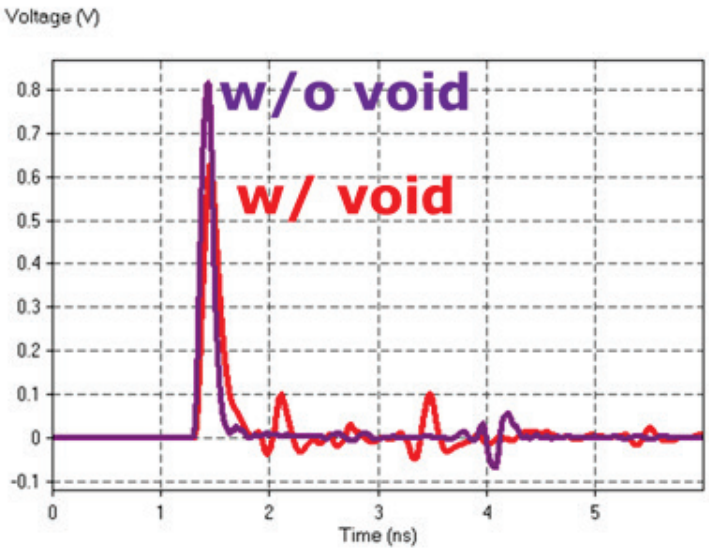
4.2.6 NEXT/FEXT summary table for net group Data_U0_U4

Net name	NEXT Vmax (mv)	NEXT Vmin (mv)	NEXT pk-2-pk (mv)	FEXT Vmax (mv)	FEXT Vmin (mv) ▲	FEXT pk-2-pk (mv)
DQ27	38	-38	76	34	-35	69
DM3	21	-20	41	20	-21	41
DQ29	18	-18	36	14	-14	29
DQ26	7	-7	14	12	-12	24
DQ30	7	-7	14	12	-12	24
DQ24	0	0	0	0	0	0
DQ31	0	0	0	0	0	0
DQ25	0	0	0	0	0	0
DQ28	0	0	0	0	0	0
[illegible]	[illegible]	0	0	[illegible]	[illegible]	0

SI Channel Check







	INT_Sig	INT_ISI	INT_XTK	P-eye	P-ratio
RX3 w/ void	67.84	104.59	5.12	-41.87	0.62
RX3 w/o void	86.00	54.64	5.00	26.36	1.44

- An example shows the trace segment is over the void that causes impedance discontinuity and leads to worse signal quality

SRC Net-level View → ERC's Segment-level View

Sigrity SRC

- Layout SI macro view at net level
- All inclusive end results
- Shows what happened and its effect on performance

Sigrity ERC

- Layout SI micro level view at segment level
- Individual segmented results
- Shows why low performance happened and how to fix it

ERC/SRC Applications (1)

ERC → SRC
→ SI simulation

- To screen board and to identify worst case for further analysis
- To investigate SI impact of design rule violations and trade-offs

Problems found in layout design

What is the impact in mv&ps?

To fix, or not to fix?

If layout problems can be quantified using mv/ps, it is much easier to decide

ERC/SRC Applications (2)

ERC ← SRC

- To find out how to fix SI problems shown in SRC simulation

How to fix them in layout

If problems can be root caused in layout, it is much easier to fix

How to fix it in layout?

Problems found in simulation results

ERC/SRC Applications (3)

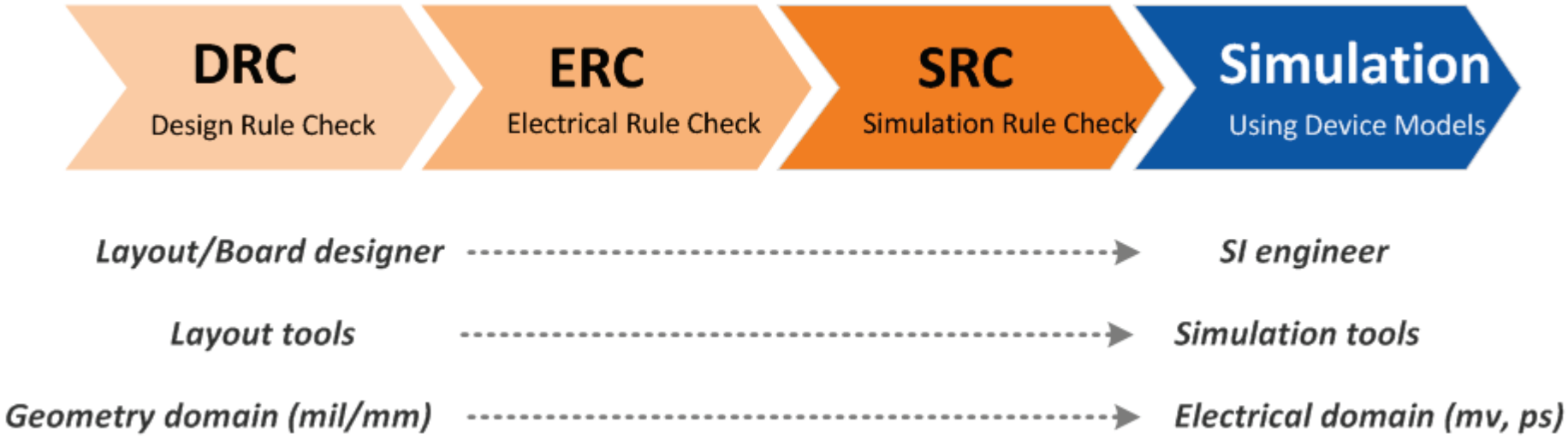
ERC screening & sign-off
SRC screening & sign-off

- To compare against ERC／SRC results with
  - Known-good design
  - Reference design
  - Part of the design that has been fully analyzed

SI engineer : Define ERC/SRC rules → Layout designer : Check for compliance

Summary

- Sigrity ERC/SRC fills the gap between layout designers and SI engineers
  - Expanded expertise
  - Using same tools
  - Measured by same units

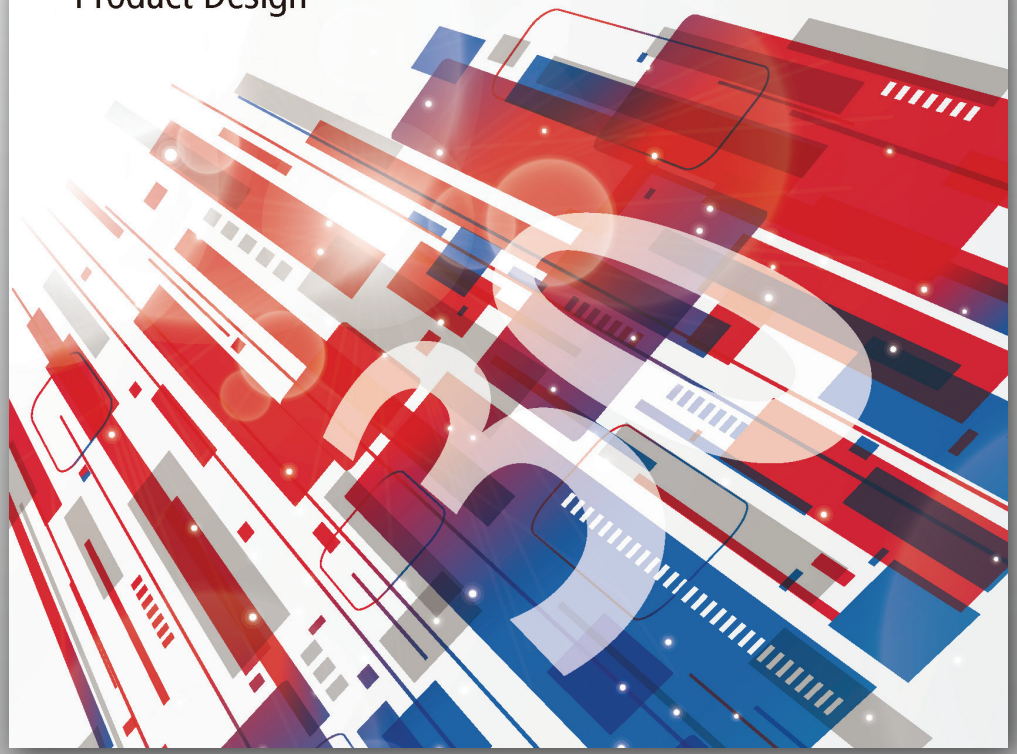


OrCAD™

CADENCE PCB SOLUTIONS

Celebrating the 30th Anniversary of OrCAD

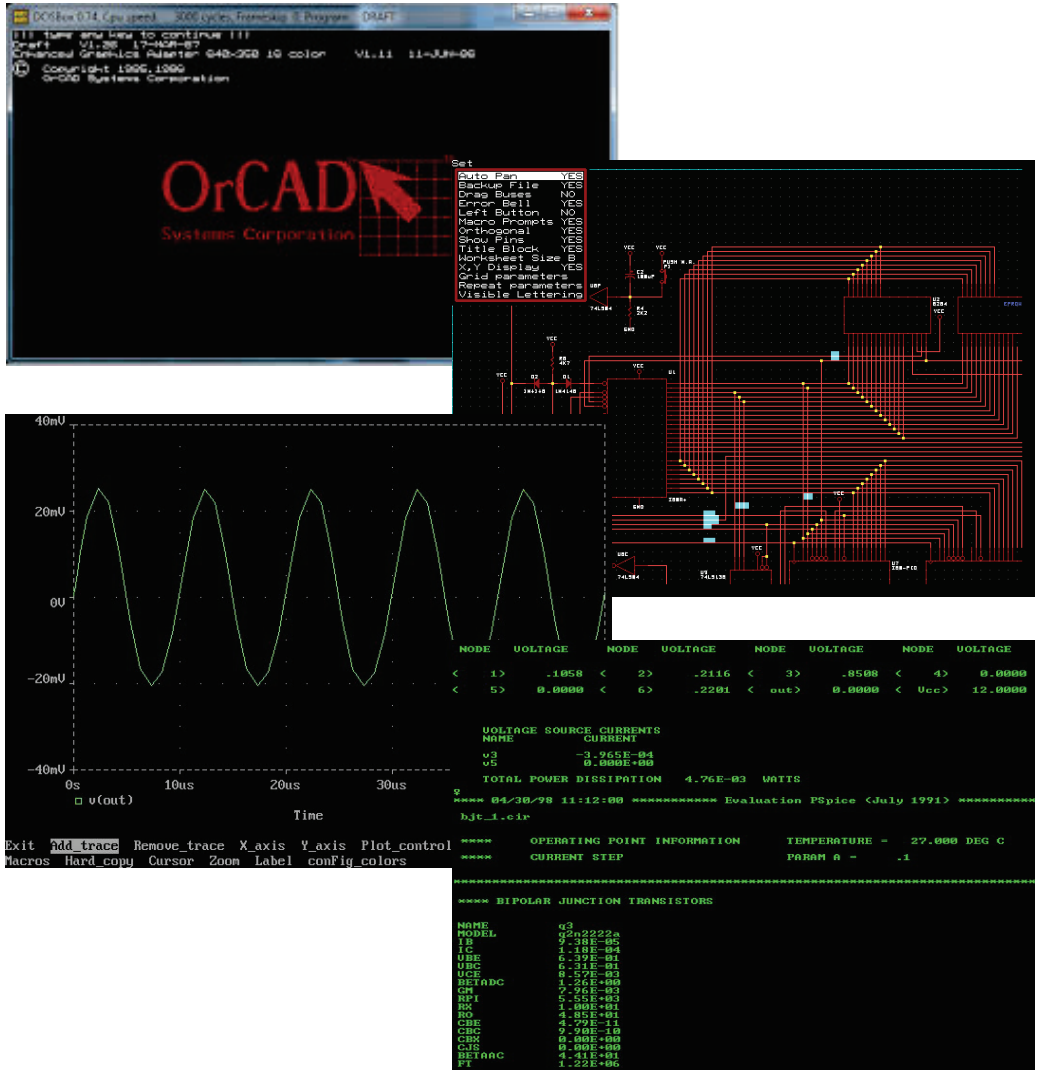
30 Years of OrCAD Innovation and Enabling Product Design



30 Years of Continued Investment and Innovation

- **1985** – OrCAD started with original SDT schematic product
  - Evolved into OrCAD Capture schematic product
- **1995** – Acquired Massteck autorouting technology
  - Evolved into original OrCAD Layout place & route product
- **1996** – Moved from private to public company with IPO
- **1997** – Acquired MicroSim (PSpice) circuit simulation technology
- **1999** – Cadence acquires OrCAD
- **2003** – Formalized worldwide channel partner program
- **2005** – Initiated OrCAD / Allegro integration strategies
  - Truly scalable and future - proof PCB design solutions
- **2007** – Adopted Allegro PCB-based technology
- **2010** – Tcl-based open architecture for unique customization and apps
- **2014** – Launch of new OrCAD brand style and website
- **2015** – OrCAD 30th Anniversary

OrCAD 30th Anniversary … 1985 – 2015



OrCAD Systems Corporation

OrCAD

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New OrCAD