全新OrCAD 2015 SPB Seminar

不僅僅只有電路設計

The New OrCAD is NOT only the Circuit Design

Comprehensive Circuit and Signal Analysis and Verification

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Graser® cādence® CHANNEL PARTNER

Topic

- Design Challenges
- Developing New Design Faster and More Stable
- Constraints Driven (PCB Transmission Line Effects)

Design Challenges

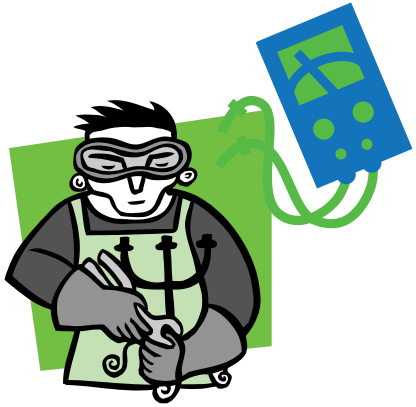
Step 1 :

Make circuit design in your system

- Does it work ?
- Does it work well ?
- Is it stable ?

Step 2 :

Make a Prototype in the laboratory



- Prepare equipment
- Connect to the system and make sure.
- Does it work ?
- Does it work well ?
- Is it stable ?

Traditional Design Process

- Schematic drawing in your design system
- Make prototype
- Measurement in the laboratory
- Repeatedly try and error

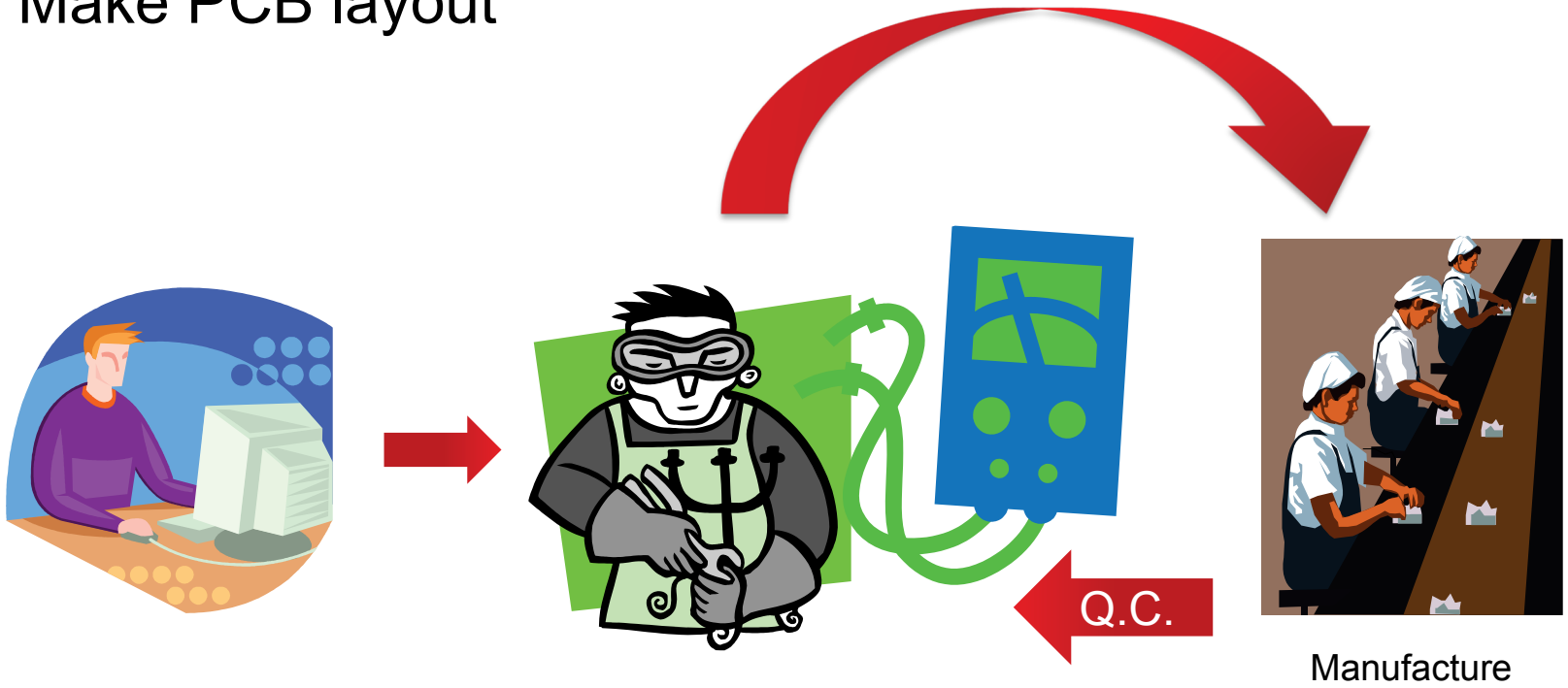
A Virtual Laboratory – OrCAD PSpice

OrCAD PSpice

- Curve Tracer
- Logical Analyzer
- Statistical Analysis
- Oscilloscope
- Measurement Expression
- Network Analyzer
- Function Generator
- Spectrum Analyzer
- Power Supply

Shorting Design Process

- Schematic drawing
- Simulate and confirm results
- Make PCB layout



A Quality Analysis Laboratory

- Mass Production Issues
  - Complexity
  - Stability
  - Components Specifications
  - Cost

Features of PSpice AD Simulator

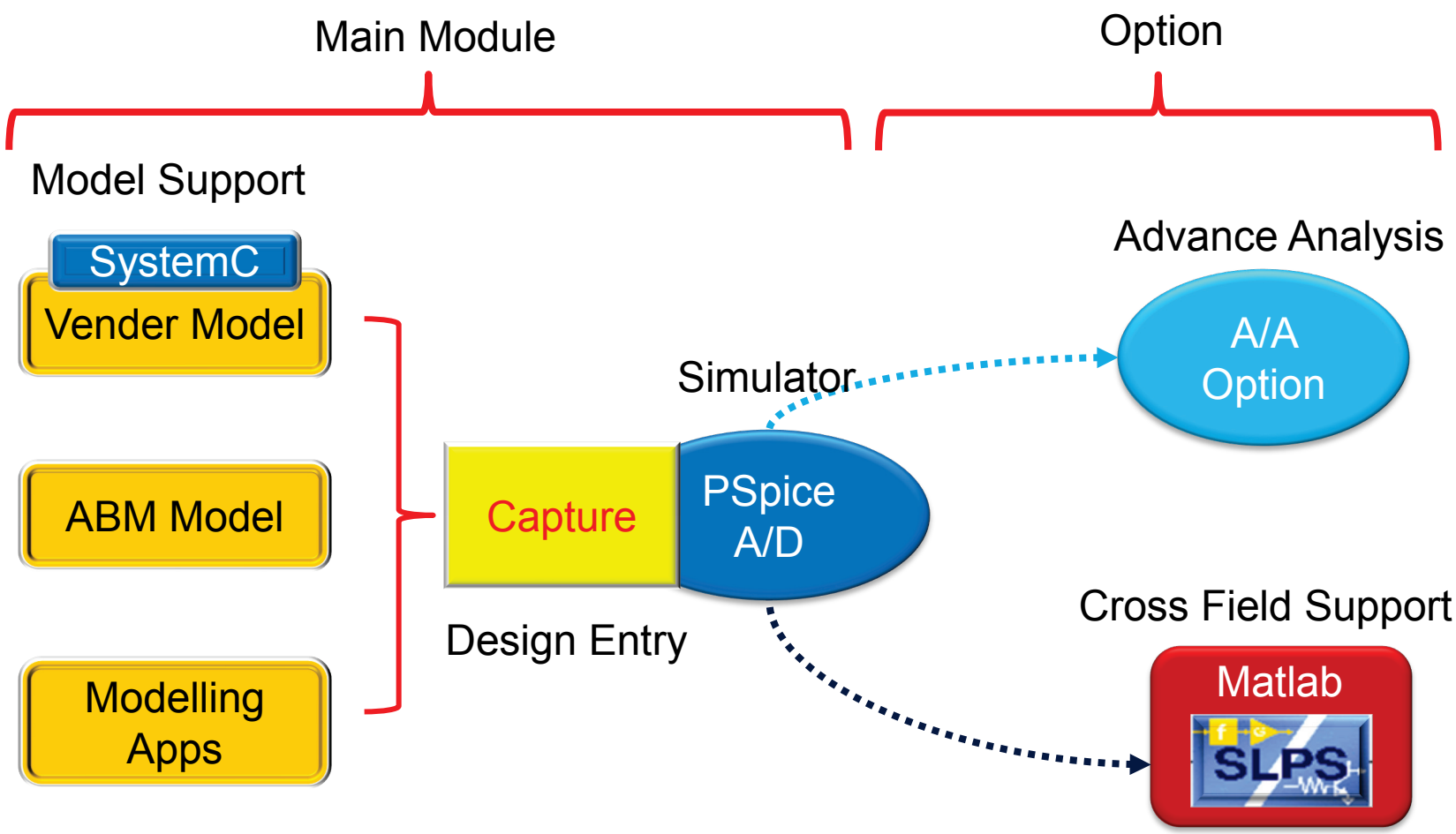
Basic Application

- Analog simulation
  - DC , AC and Transient Analysis
  - Noise ,FFT…
- Digital simulation
  - Limitation Analysis
  - Transient Analysis

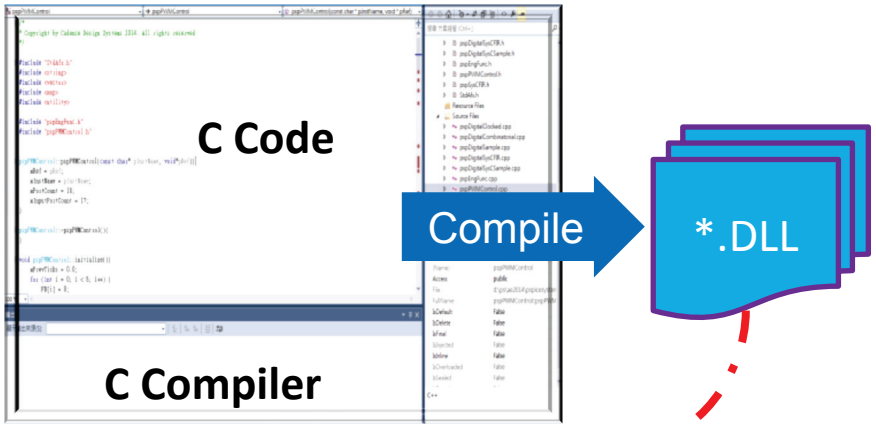
Mass Production

- Parametric Analysis
- Monte Carlo Analysis
- Worst-Case Analysis
- Temperature Analysis

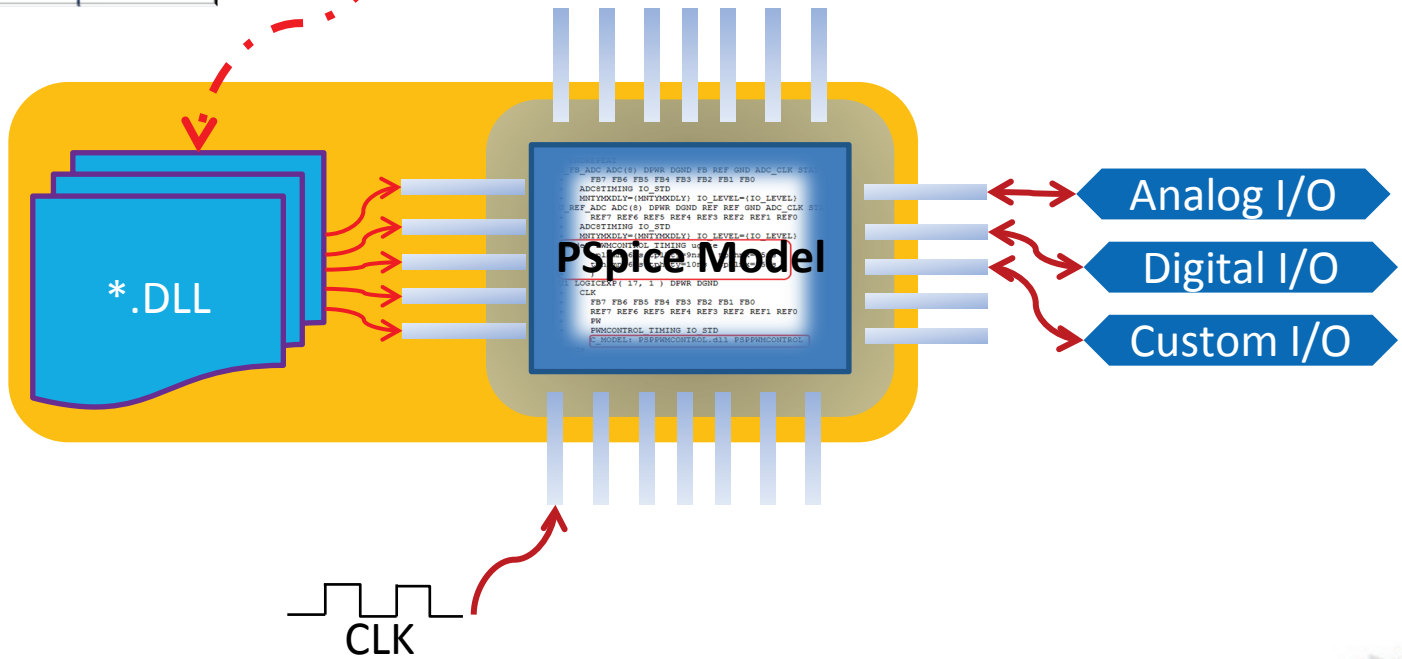
OrCAD PSpice



Embedded SystemC in PSpice Model



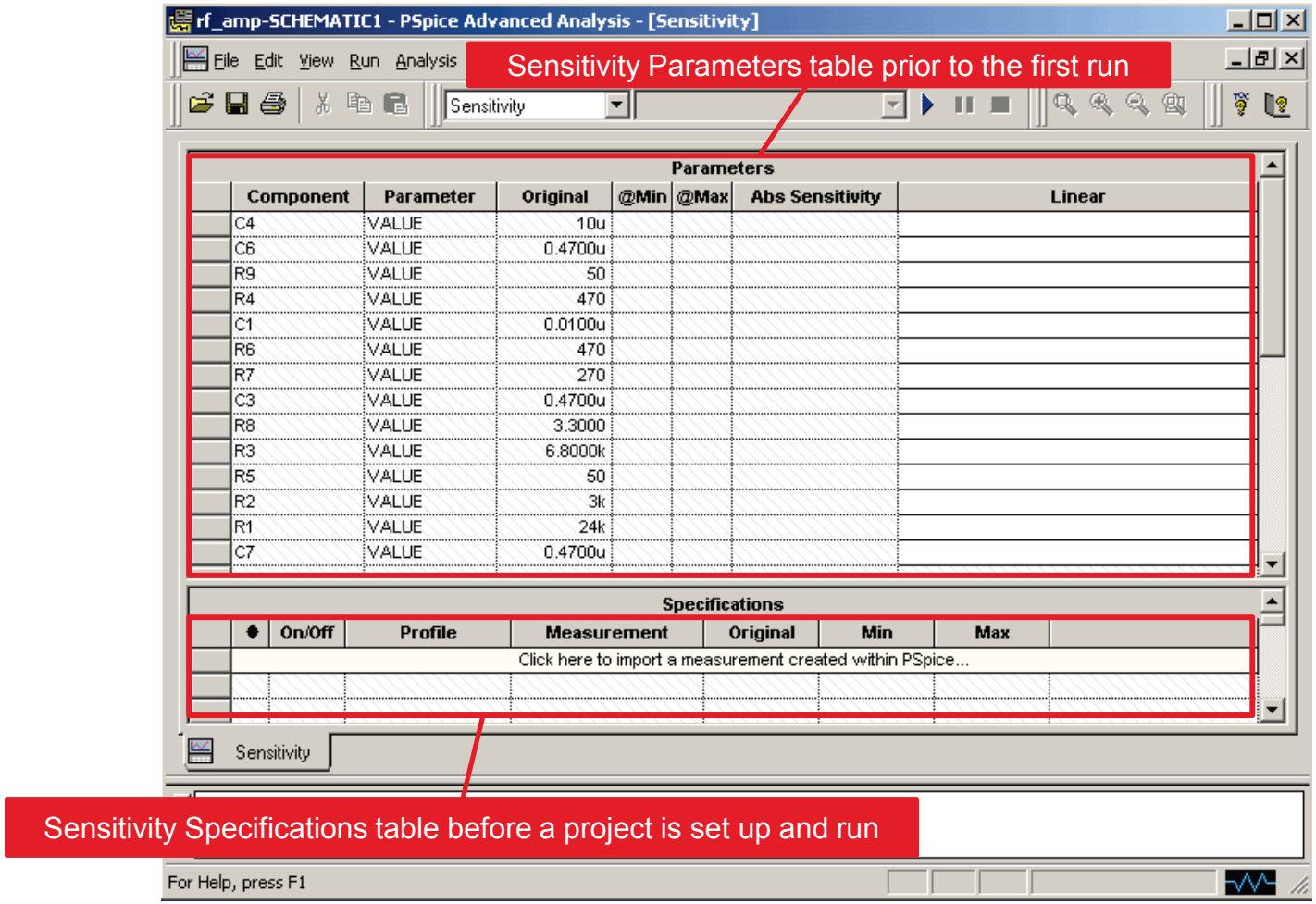
1. Build your functions by C language.
2. Compile and Generate DLL file.
3. Link signal nodes between DLL with spice model.



Advanced Analysis Option

- Sensitivity
  - Sensitivity identifies which components have parameters critical to the measurement goals of your circuit design.
- Optimizer
  - Optimizer is a design tool for optimizing analog circuits and their behavior. It helps you modify and optimize analog designs to meet your performance goals.
- Monte Carlo
  - Monte Carlo predicts the behavior of a circuit statistically when part values are varied within their tolerance range. Monte Carlo also calculates yield, which can be used for mass manufacturing predictions.
- Smoke
  - Smoke warns of component stress due to power dissipation,increase in junction temperature, secondary breakdowns, or violations of voltage／current limits. Over time, these stressed components could cause circuit failure.

Sensitivity Analysis (A/A Option)



Sensitivity Analysis (A/A Option)

- Sensitivity Result

Parameter values that correspond to measurement min and max values

Parameters

Component	Parameter	Original	@Min	@Max	Rel Sensitivity	Linear
R9	VALUE	50	45	55	44.5124m	99
R4	VALUE	470	423	517	37.3404m	83
R5	VALUE	50	55	45	-36.1144m	81
R8	VALUE	3.3000	3.6300	2.9700	-25.2563m	56
R6	VALUE	470	517	423	-21.0667m	47
R3	VALUE	6.8000k	7.4800k	6.1200k	-13.9678m	31
R2	VALUE	3k	2.7000k	3.3000k	13.2341m	29
R7	VALUE	270	243	297	7.3855m	16
C4	VALUE	10u	9u	11u	3.6010n	< MIN >
C6	VALUE	0.4700u	423n	517n	1.0585u	< MIN >
C1	VALUE	0.0100u	9n	11n	500.5676p	< MIN >
C3	VALUE	0.4700u	423n	517n	141.8399n	< MIN >
R1	VALUE	24k	21.6000k	26.4000k	95.0558u	< MIN >
C7	VALUE	0.4700u	423n	517n	375.2423n	< MIN >

Specifications

On/Off	Profile	Measurement	Original	Min	Max
☑	rf_amp-schematic1-ac.sim	max(db(v(load)))	9.4181	7.3142	11.3819
☑	rf_amp-schematic1-ac.sim	bandwidth(v(load),3)	150.5788meg	130.3443meg	174.8395meg
☑	rf_amp-schematic1-ac.sim	min(10*log10(v(inoise)*v(inoise)/8.28e-19))	4.1481	3.6360	4.7507
☑	rf_amp-schematic1-ac.sim	max(v(onoise))	4.3383n	3.5366n	5.2793n

Click here to import a measurement created within PSpice...

The measurement's worst-case minimum and maximum values

Optimizer Analysis (A/A Option)

Optimizer | Modified LSQ
Modified LSQ
Random
Discrete

Optimizer

Error Graph

1%
0.9%
0.8%
0.7%
0.6%
0.5%
0.4%
0.3%
0.2%
0.1%
0%
Error
N
N
Run Number

Parameters [Next Run]

On/Off	Component	Parameter	Original	Min	Max	Current
	R8	VALUE	3.3000	3	3.6000	3.3000
	R6	VALUE	470	235	705	470
	R4	VALUE	470	235	705	470

Click here to import a parameter from the design property map...

Component Value Range define

Standard | Curve Fit

Specifications [Next Run]

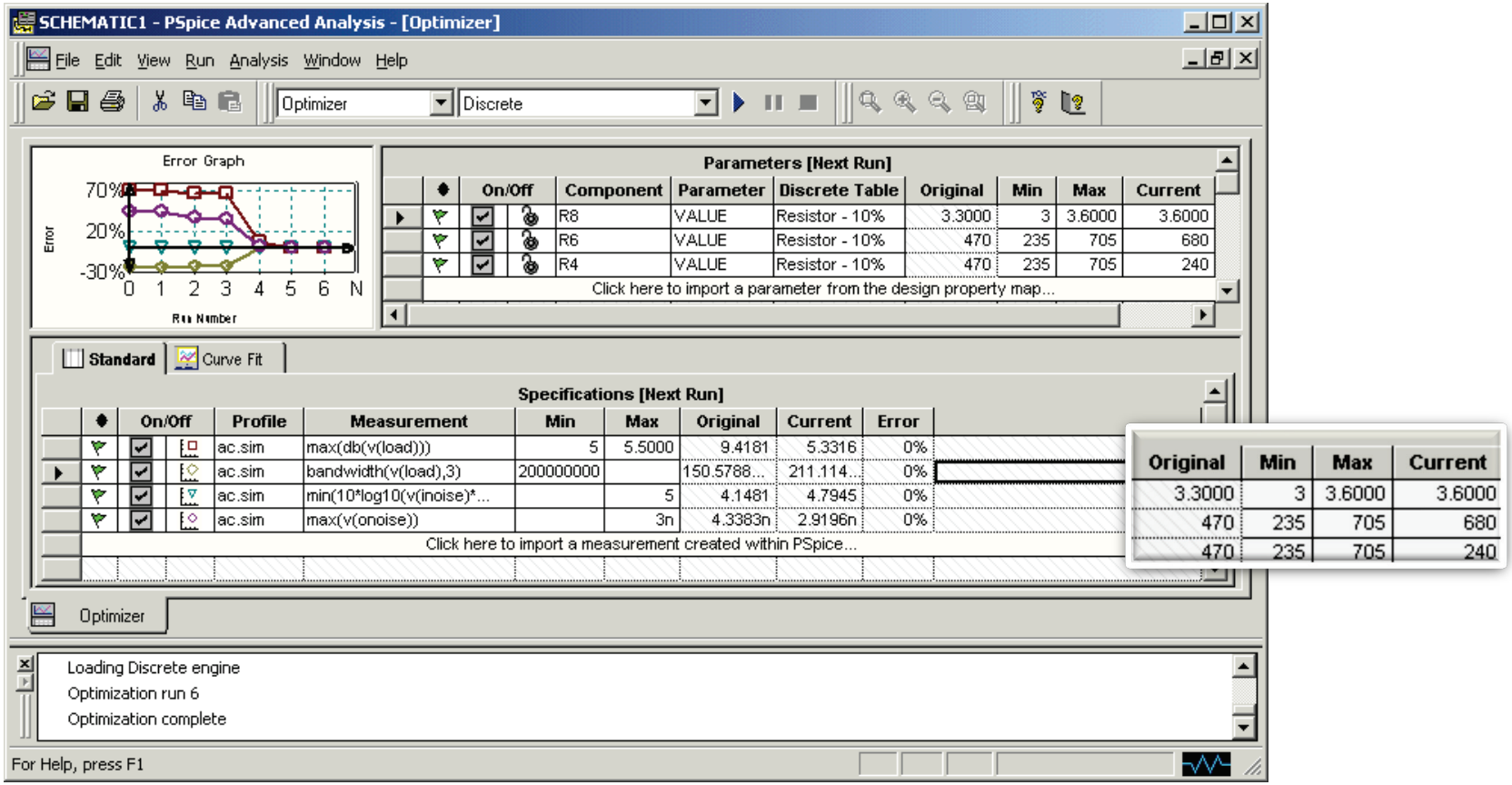
On/Off	Profile	Measurement	Min	Max	Type	Weight	Original	Current	Error
	ac.sim	Max(DB(V(Load)))	5	5.5000	Constraint	20			
	ac.sim	Bandwidth(V(Load),3)	200meg		Goal	1			
	ac.sim	Min(10*Log10(V(inois...		5	Constraint	1			
	ac.sim	Max(V(onoise))		3n	Constraint	20			

Click here to import a measurement created within PSpice...

Assume your spec.

Optimizer Analysis (A/A Option)

- Optimizer Result



Smoke Analysis (A/A Option)

Standard derating factors used in the calculations

Smoke - tran.sim [No Derating] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	Q1	Max C-E voltage	Average	12	50	6	8.1262	136
	Q1	Max C-E voltage	Peak	12	50	6	8.1422	136
	Q1	Max C-E voltage	RMS	12	50	6	8.1262	136
	Q1	Maximum junction temperature	Peak	200	75	148.2857m	77.7764m	53
	Q1	Maximum junction temperature	Average	200	75	148.2857m	74.7301m	51
	Q1	Maximum junction temperature	RMS	200	75	148.2857m	74.7603m	51
	Q1	Maximum power dissipation	Peak	197.7143m	100	200	95.0543	48
	Q1	Maximum power dissipation	Average	197.7143m	100	200	92.3888	47
	Q1	Maximum power dissipation	RMS	197.7143m	100	200	92.4152	47
	Q1	Max C-B voltage	Average	20	38.6675	96.6688m	40.4885m	42
	Q1	Max C-B voltage	Peak	20	38.6675	96.6688m	40.4885m	42
	Q1	Max C-B voltage	RMS	20	38.6675	96.6688m	40.4885m	42
	Q1	Max E-B voltage	RMS	2.5000	50	20	7.6077	39
	R6	Maximum breakdown temperature	Average	200	50	20	7.6077	39
	R6	Maximum breakdown temperature	Peak	200	50	20	7.6077	39
	R6	Maximum breakdown temperature	RMS	200	100	20	7.3391	37
	R6	Maximum power dissipation	Average	250m	100	20	7.3568	37
	R6	Maximum power dissipation	Peak	250m	100	20	7.3392	37
	R6	Maximum power dissipation	RMS	250m	100	2.5000	787.0483m	32
	R7	Maximum breakdown temperature	Average	200	100	200	59.3908	30
	R7	Maximum breakdown temperature	Peak	200	100	200	59.3908	30
	R7	Maximum breakdown temperature	RMS	200	100	200	59.3908	30
	C4	Maximum voltage	Average	50	90	45	10.6377	24
	C4	Maximum voltage	Peak	50	90	45	10.6377	24
	C4	Maximum voltage	RMS	50	90	45	10.6377	24
	R3	Maximum breakdown temperature	Average	200	80	40m	9.5805m	24
	R3	Maximum breakdown temperature	Peak	200	100	200	45.2368	23
	R3	Maximum breakdown temperature	RMS	200	100	200	45.4554	23
	Q1	Max collector current	Peak	50m	100	200	45.2375	23
	Q2	Max C-E voltage	Average	40	80	40m	9.1877m	23

Monte Carol Analysis (A/A Option)

rf_amp-SCHEMATIC1 - PSpice Advanced Analysis - [Monte Carlo]

File Edit View Run Analysis Window Help

Monte Carlo

Probability Density Graph (Runs: 1 to 100)

Number of Runs

15 10 5 0

Min

Max

8.3 8.4 8.5 8.6 8.7 8.8 8.9 9 9.1 9.2 9.3 9.4 9.5 9.6 9.7 9.8 9.9 10 10.1 10.2 10.3 10.4 10.5 10.6 10.7 10.8

max(db(v(load)))

Statistics | Raw Meas

Statistical Information

	On/Off	Profile	Measurement	Cursor Min	Cursor Max	Yield	Mean	Std Dev	3 Sigma	6 Sigma	Median
	☑	rf_amp...	max(db(v(load)))	8.3900	10.8181	100%	9.4268	280.0109m	100%	100%	9.4175
	☑	rf_amp...	bandwidth(v(load),3)	139.9560meg	164.4402meg	100%	151.0197meg	4.9280meg	100%	100%	150.9876meg
	☑	rf_amp...	min(10*log10(v(inoise)*v(inoise)/8.28e-19))	3.7219	4.6057	100%	4.1382	201.3833m	100%	100%	4.1361
	☑	rf_amp...	max(v(onoise))	3.8695n	4.9430n	100%	4.3280n	219.4049p	100%	100%	4.3216n

Click here to import a measurement created within PSpice...

Monte Carlo

Monte Carlo run 99 completed

For Help, press F1

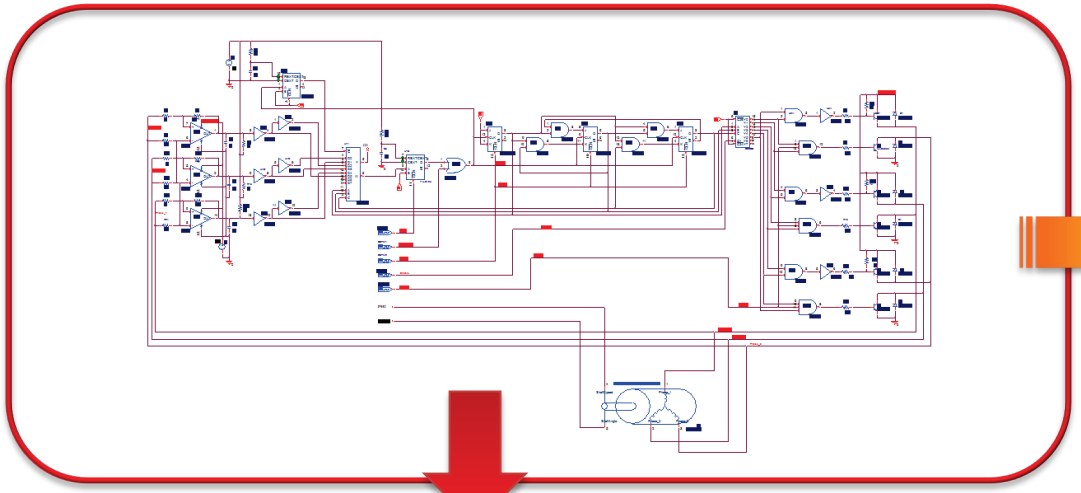
Check for acceptable values compared to design specs

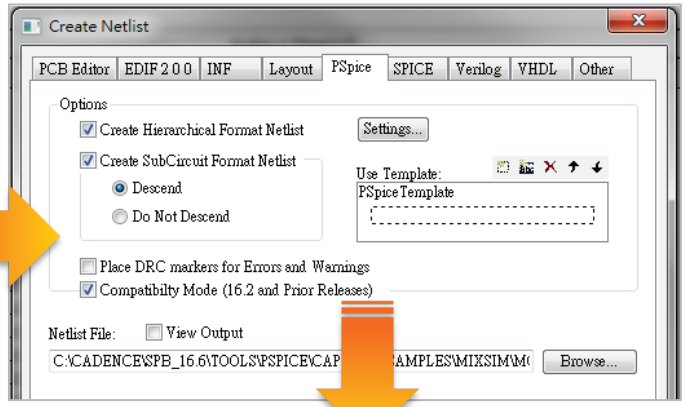
Advance Application

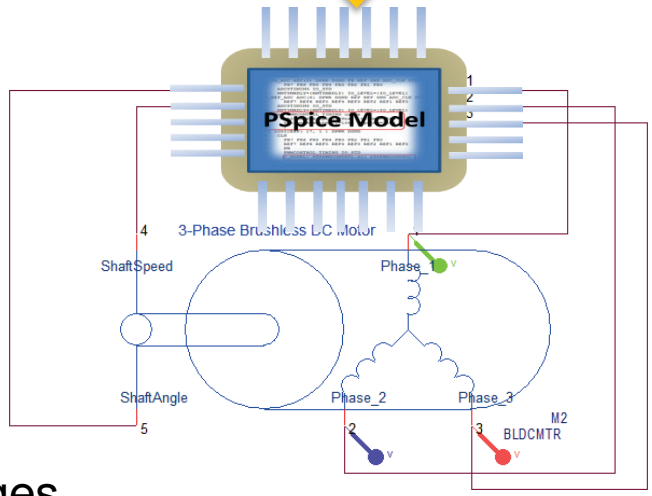
- Simplify Design
- Modularized Design
- Mechatronics Integration Design

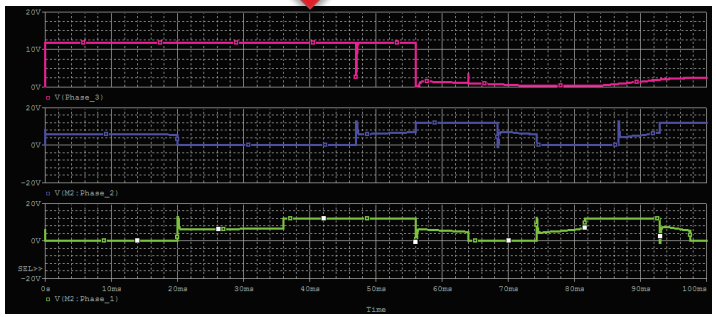
Simplify Design

- Create PSpice Netlist = Generate a system model





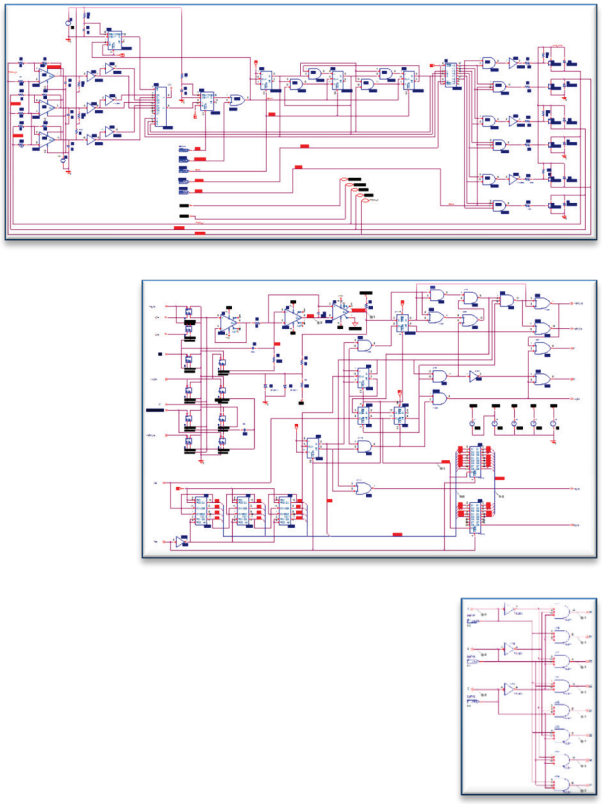


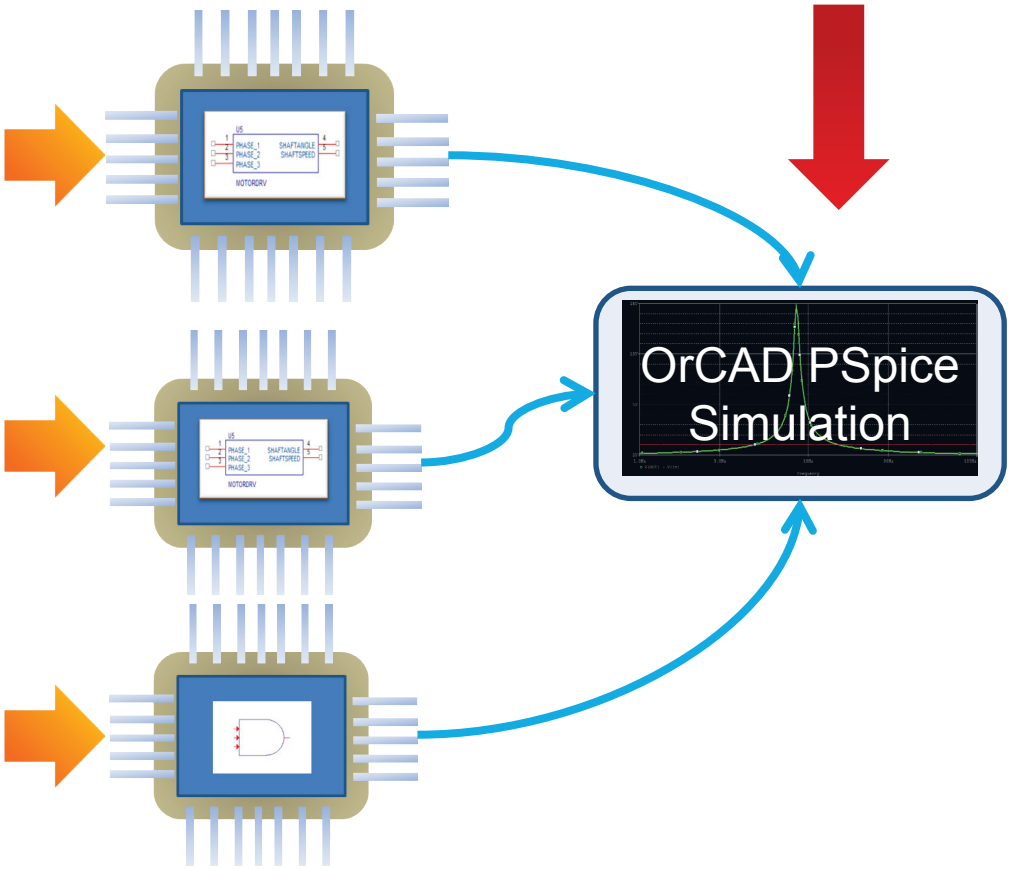


1. Generate a system model (PSpice Netlist)
2. We can get same results by simplified changes

Modularization

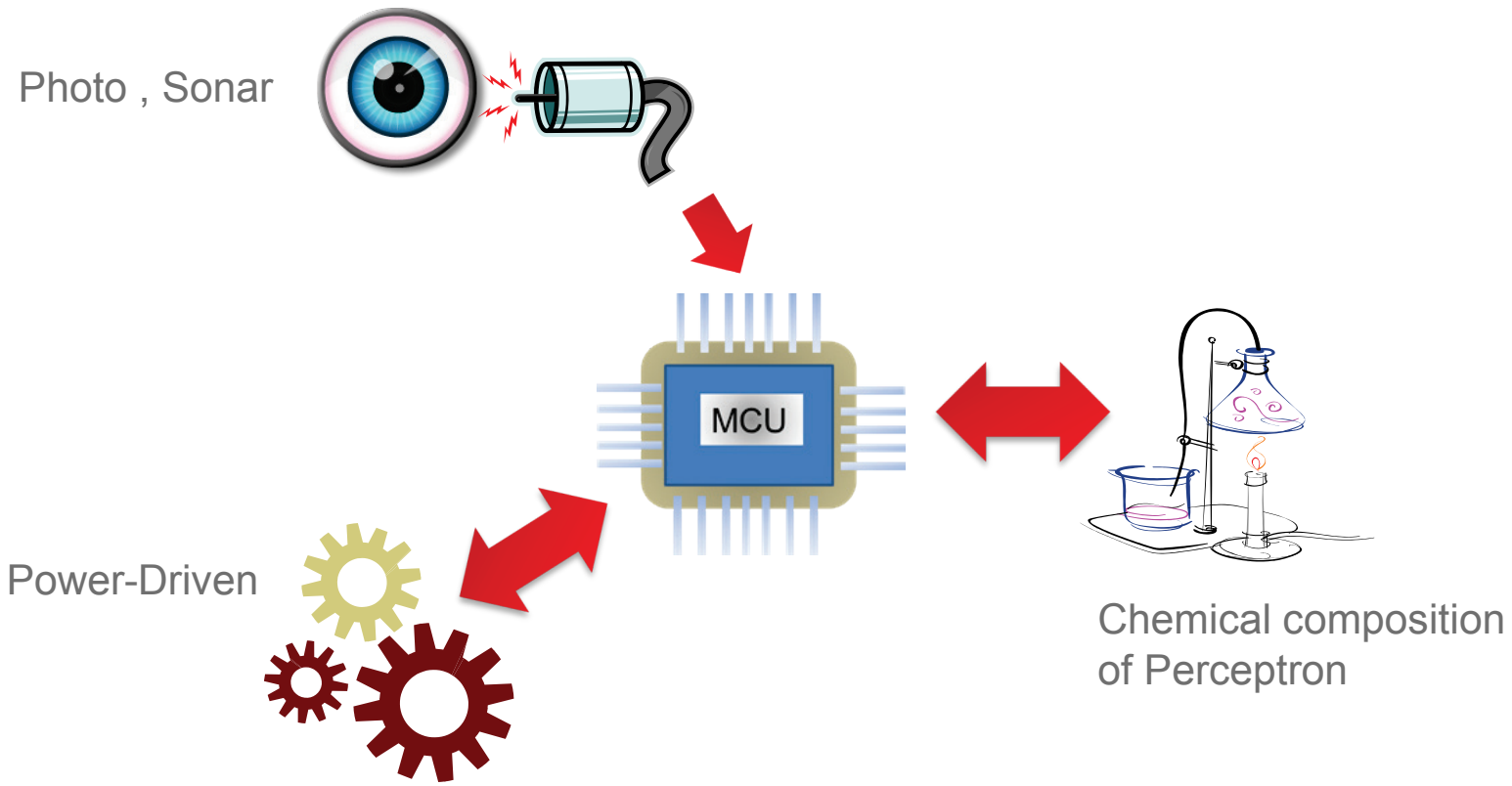
Complex Circuit Drawing → Modularized → A Few Chips Design → Module combination → Simplified Circuit Design





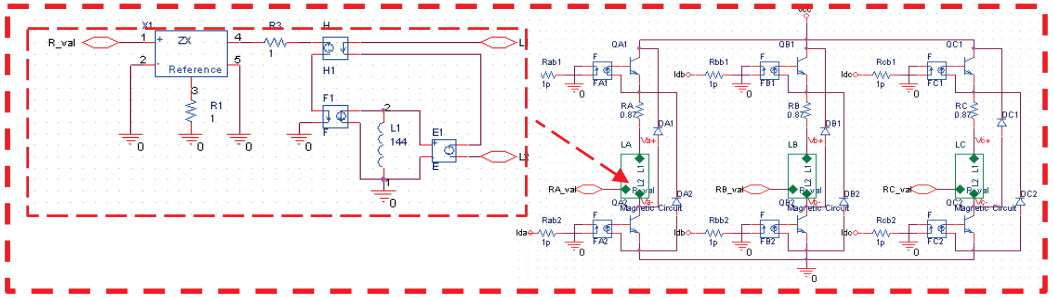
Mechatronics Integration Design

- Automotive Safety System
- Passive mode：ABS、Airbag、Reversing radar
- Active mode：DSTC , ROPS , EBD , CWFAB , PDFAB , DAC , LDW

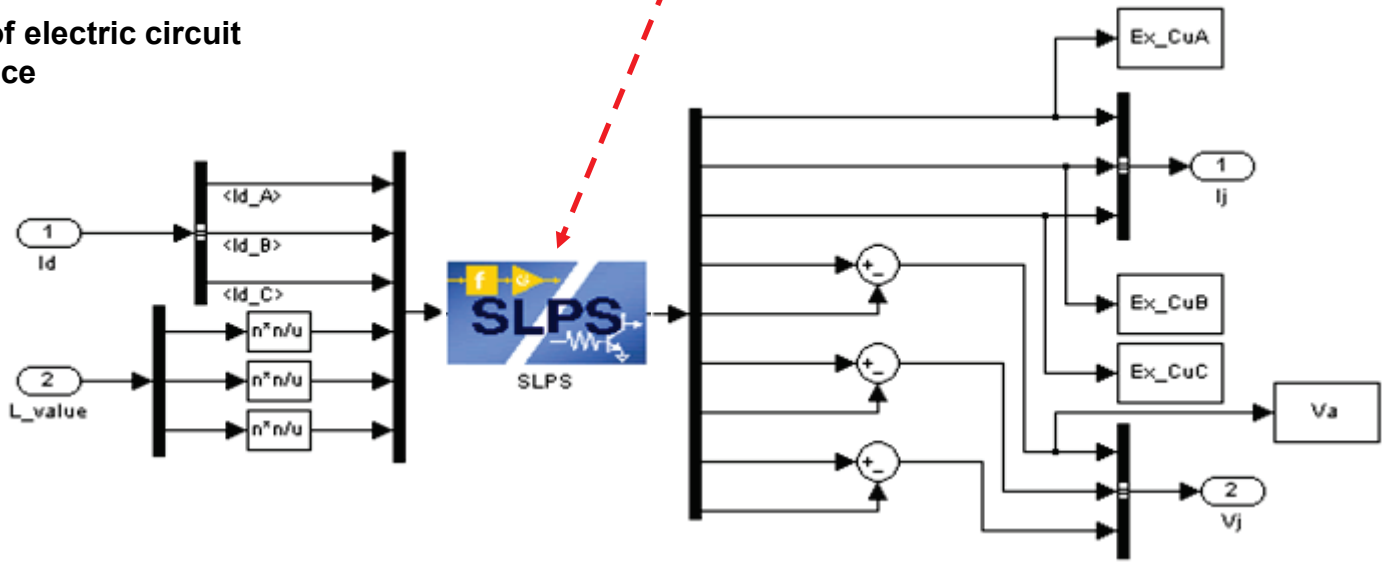


SLPS Option

- The Circuit Design is embedded into Matlab for a system block model(SLPS) with simulink interface for Cross-Field Simulation.

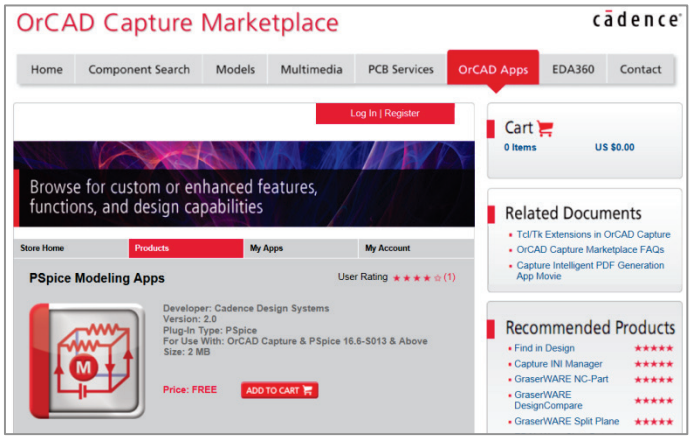


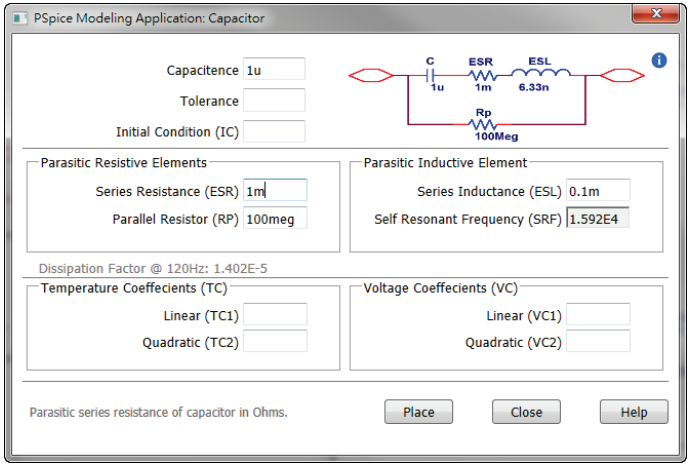
Modeling of electric circuit using PSpice



Model Resources

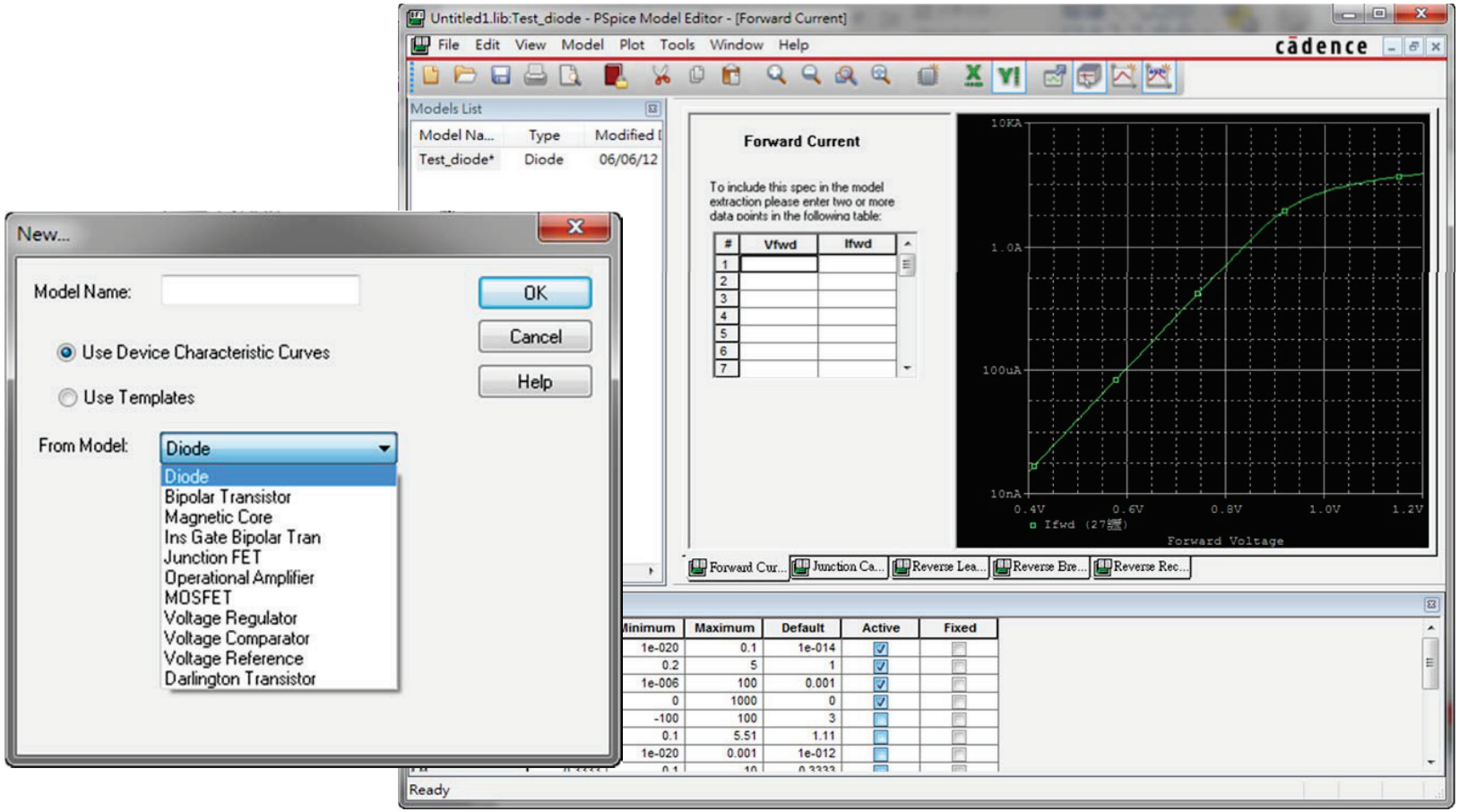
- IC Vender
- Model Editor
- Magnetic Parts Editor
- OrCAD Capture MarketPlace
- Temporary Model from modelling Apps
  (provide both models & symbols)
- Other Resources





Model Editor

- Create new PSpice model from model editor refer datasheet



Magnetic Parts Model Wizard

Magnetic Parts Editor - [Power Transformer-Untitled]

File View Tools Help

cadence

Design Steps

Step 1: Component Selection

Step 2: General Information

Step 3: Electrical Parameters

Step 4: Core Selection

Step 5: Bobbin-Winding Selection

PSpice Model Name: Untitled

PSpice Model .lib: C:\Cadence\SPB_16.6\tools\pspice

Default Model

```
*$
* Generated  by Magnetic Parts Editor on Fri Jun 05 11:38:21 2015
.subckt Untitled V_IN1 V_IN2
+ V_OUT11 V_OUT12
+ PARAMS:  Np=14 RSp=0.0300969 Llp=2.99432e-006
+ Ns1=14 RSs1=0.0435887 Gap = 0
L_LP NLP V_IN2 {Np}
R_RP NRP NLP {RSp}
L_Leak V_IN1 NRP {Llp}
L_LS1 NLS1 V_OUT12 {Ns1}
R_RS1 NLS1 V_OUT11 {RSs1}
K_K2 L_LP L_LS1  1.0 core_model_K1
.model core_model_K1 AKO:core_model  CORE (GAP={Gap})
.model core_model CORE (LEVEL = 3 OD = 4.77 ID = 0 AREA = 0.86 GAP = 0 Br = 1100 Bm = 5000 Hc = 0.175 )
.ends Untitled
*$
```

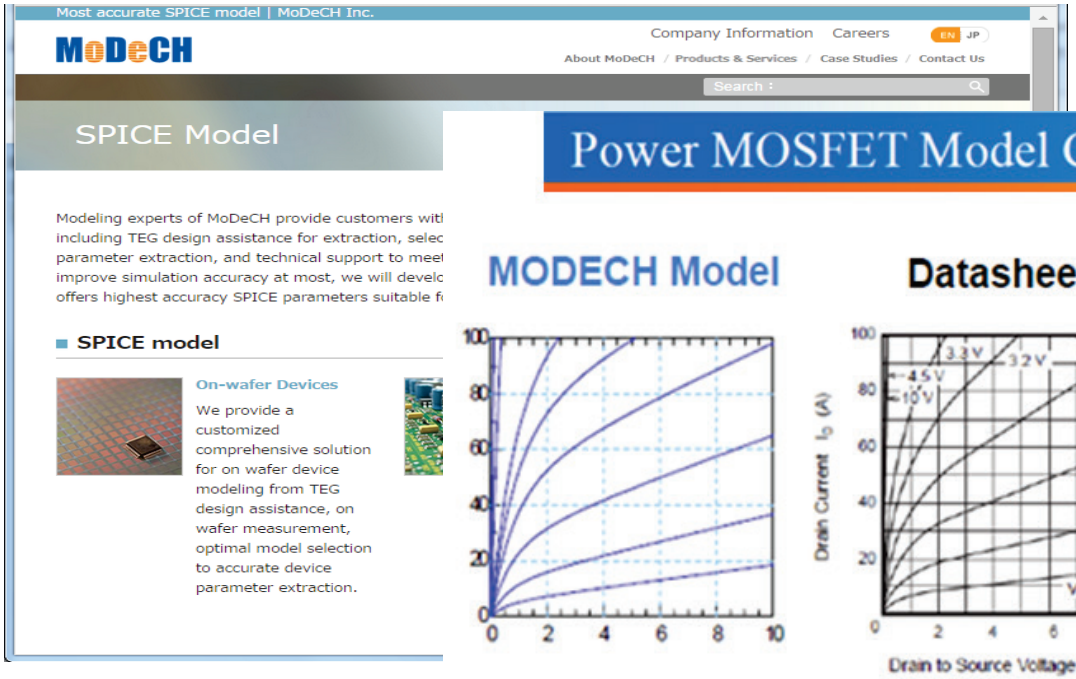
Manufacturer Report | Model View

Original

- INFO: Done.
- WARNING(ORMAGDB-1105): The skin depth value is 0.296055 mm. It is being violated for P0 winding. Select the LITZ type of winding if SINGLE is selected.
- WARNING(ORMAGDB-1105): The skin depth value is 0.296055 mm. It is being violated for S0 winding. Select the LITZ type of winding if SINGLE is selected.
- INFO: Designing winding layout.

For Help, press F1

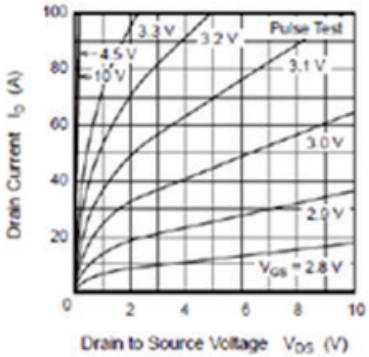
Model Service

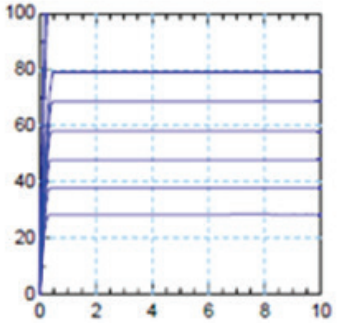


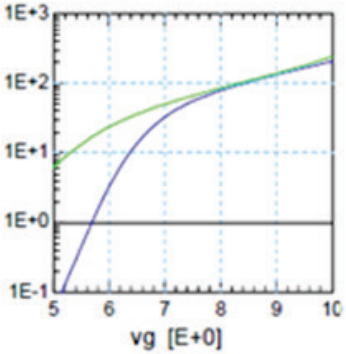
Power MOSFET Model Comparison

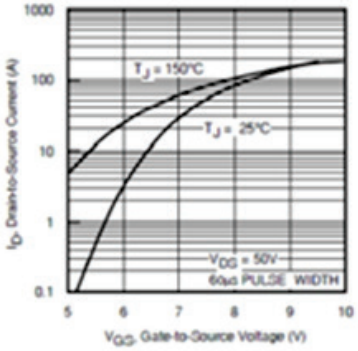
MoDeCH

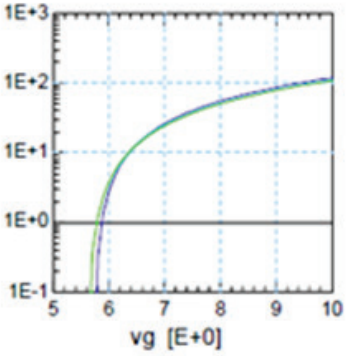
MODECH Model	Datasheet	Free Model









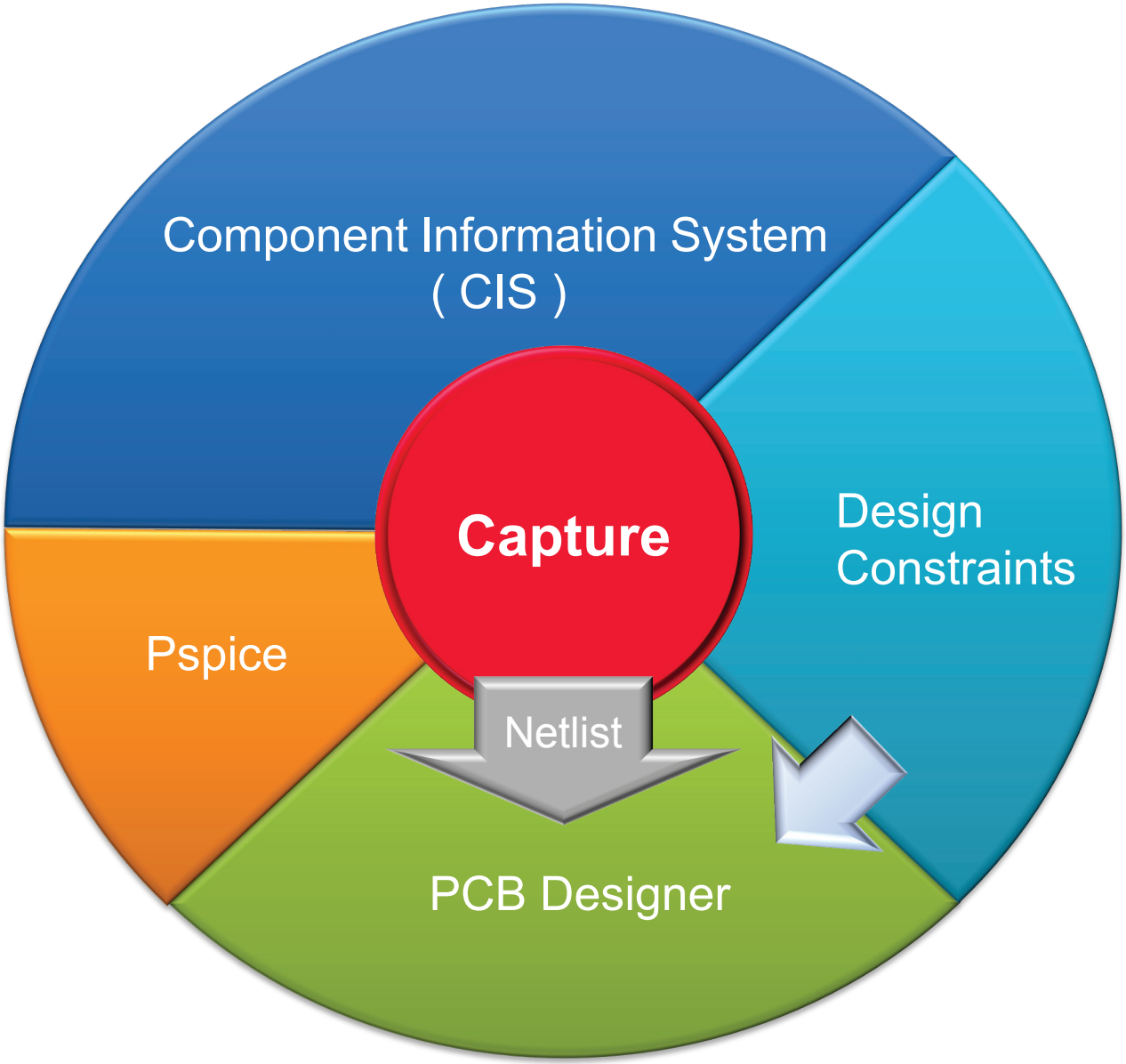


MODECH Model	Datasheet	Free Model

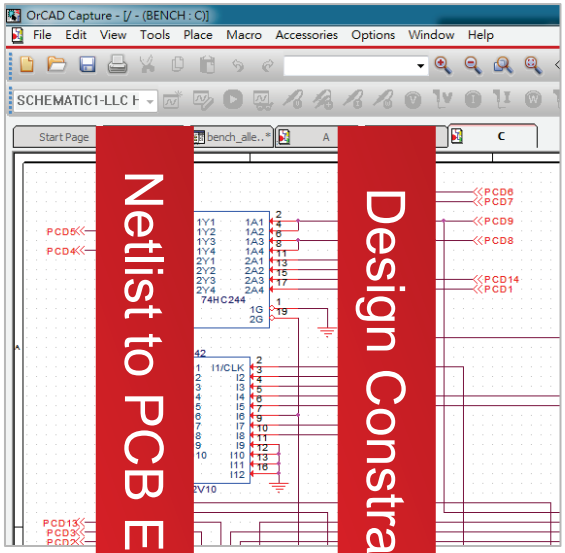
Constraint Setting Determination by OrCAD PCB SI

Concerning PCB Transmission Line Effects

OrCAD™ Design Tool Chart



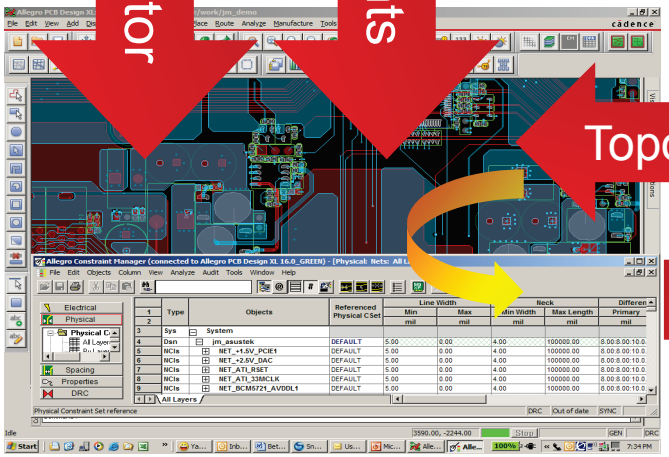
Traditional Flow



Netlist to PCB Editor

Design Constraints

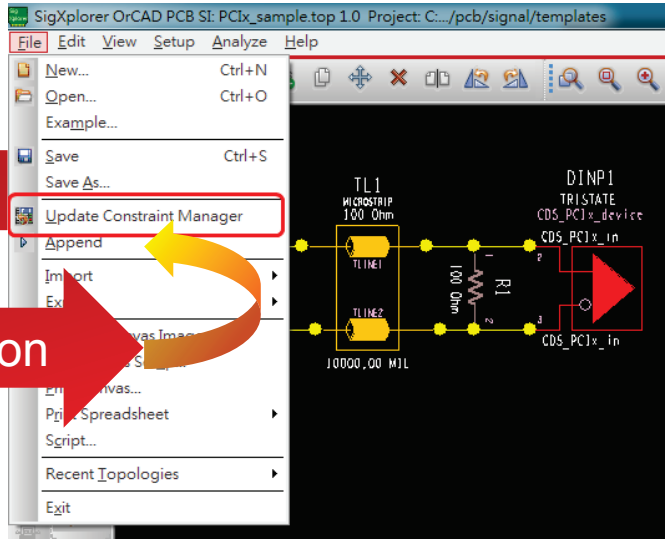
How to determine ?
Design Reuse?
Constraints Update ?



Topology Association

Topology Extraction

Analyze／ Edit Topology



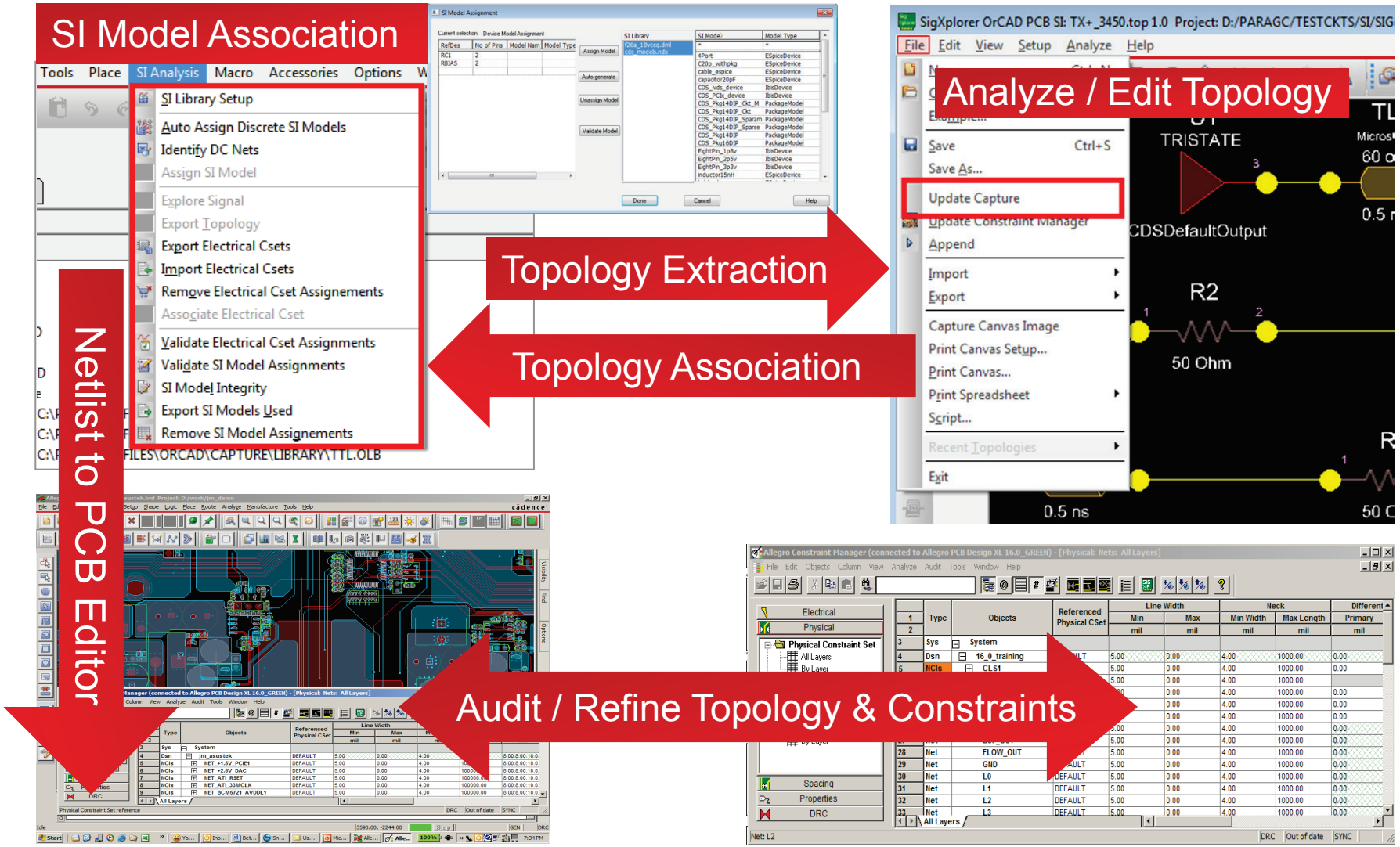
Change Your Constraints Design Flow OrCAD PCB SI

- Determine design constraints in circuit design
- Back annotate ECset and store information in Capture
- Direct translate Design Constraints from Netlist files.

Simplified PCB layout guide writing and reading

Smoothness for PCB design flow from RD to Layout engineers

New Constraints Design Flow

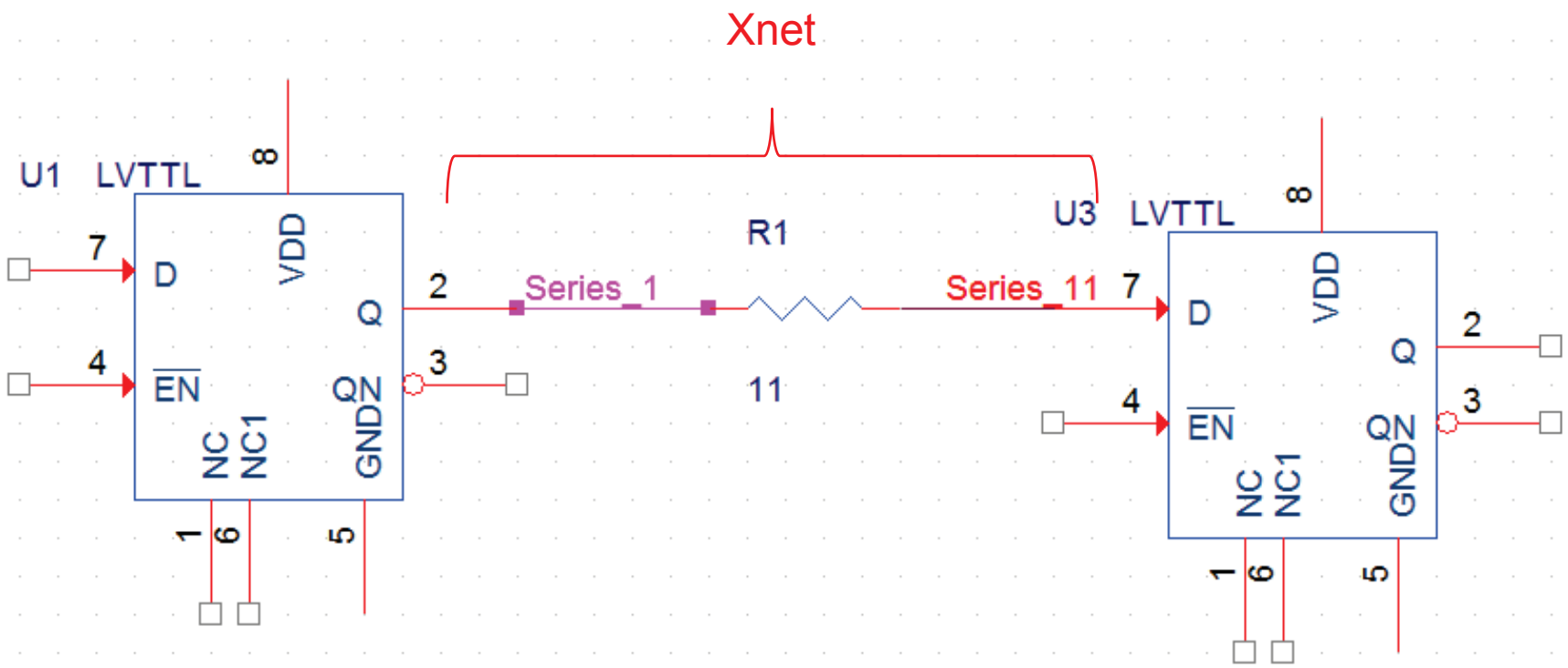


Determine Hi-Speed Constraints in OrCAD PCB SI

- Impendence control
  - Cross section
  - Trace width
- Timing control
  - Trace length control

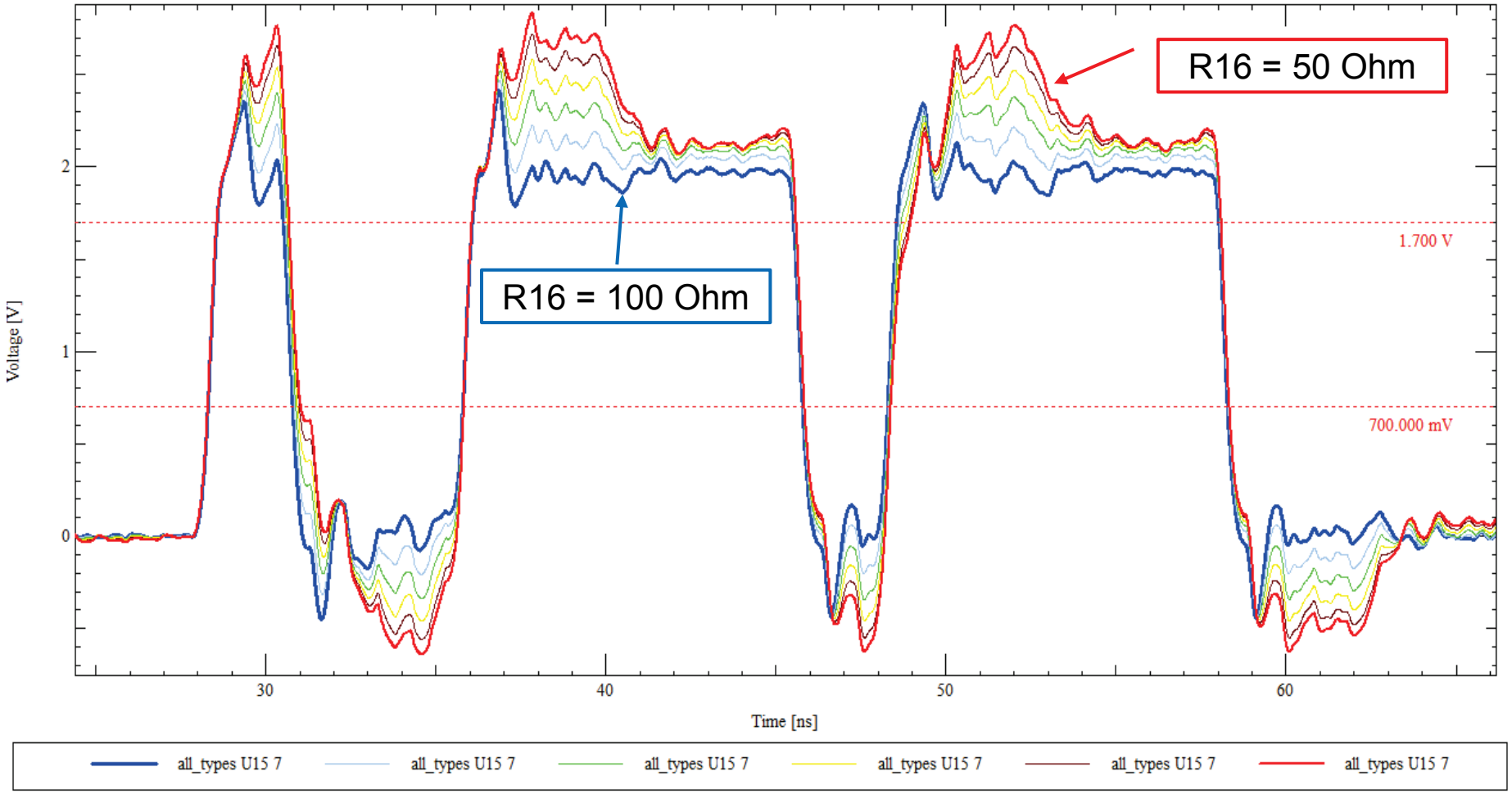
Signal Integrity Analysis in Capture

- Auto assign discrete SI model by component value
- Assign SI model for others



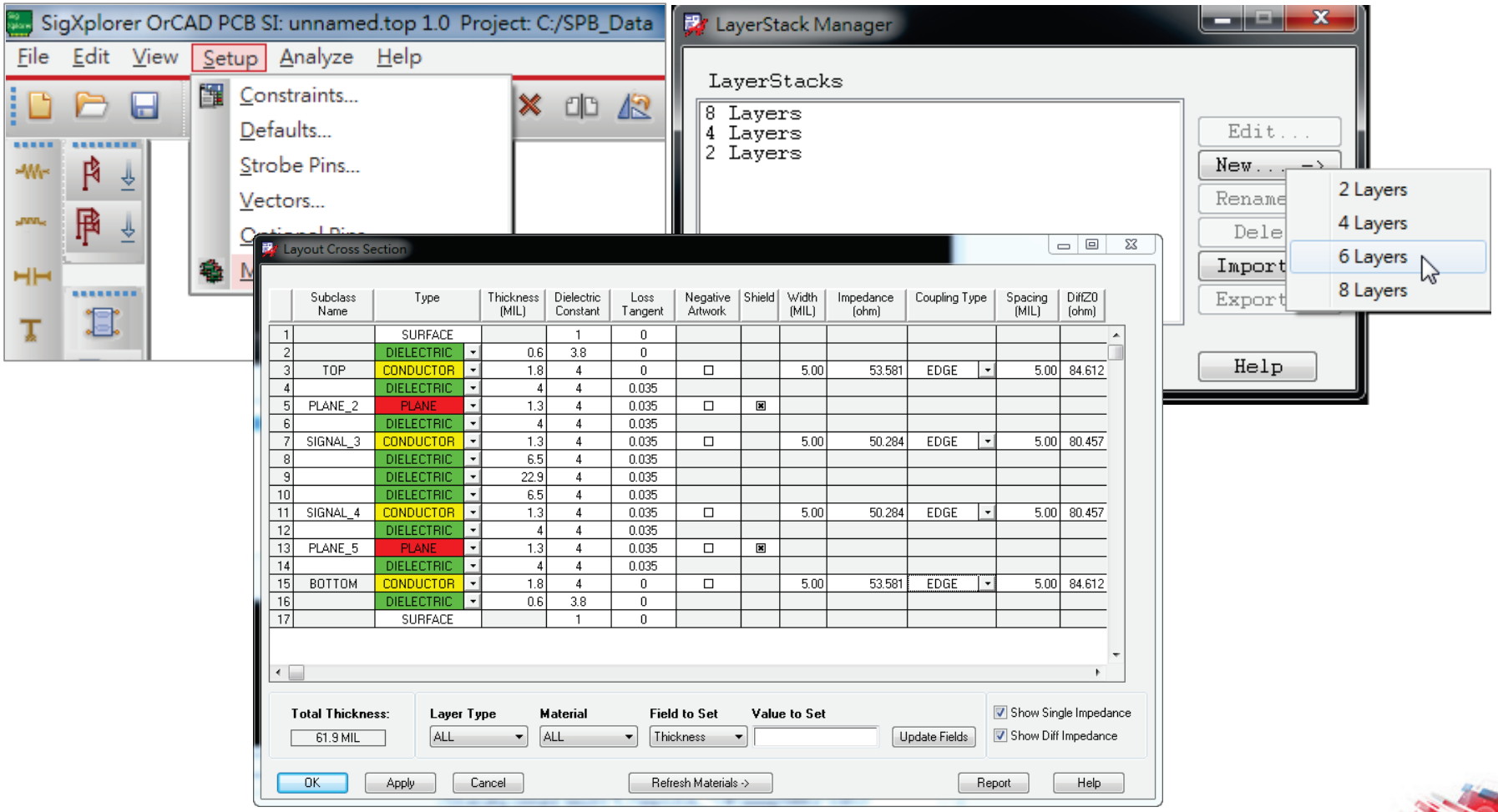
OrCAD PCB SI for Signal Integrity Analysis

Impendence Control - Terminator



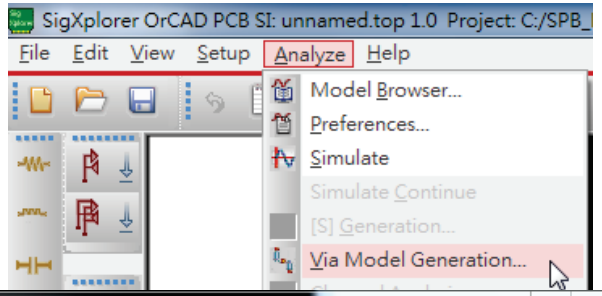
From Idea to Virtual Practicability

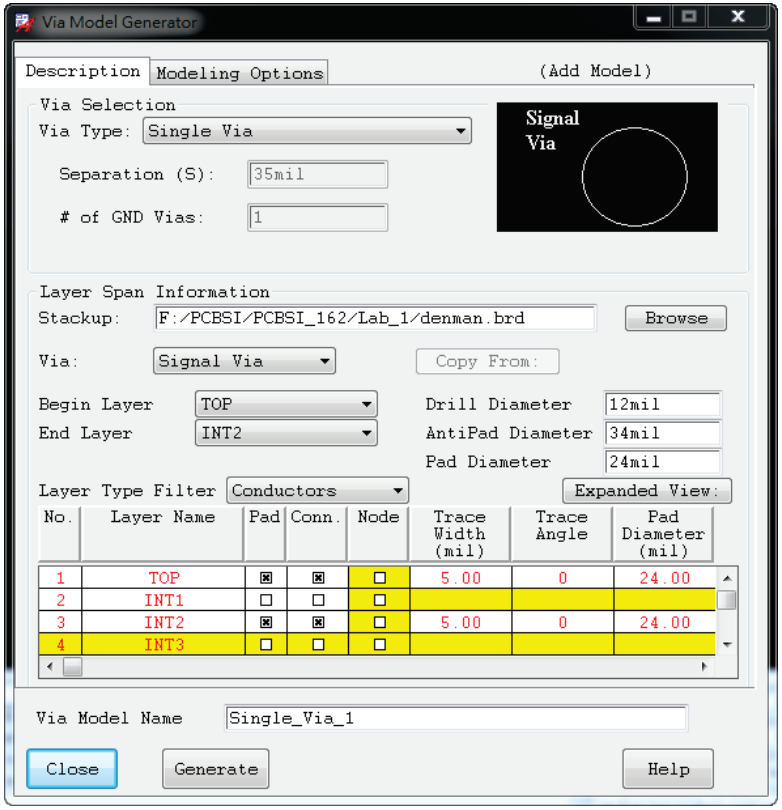
- Virtual Layer Stackup



From Idea to Virtual Practicability

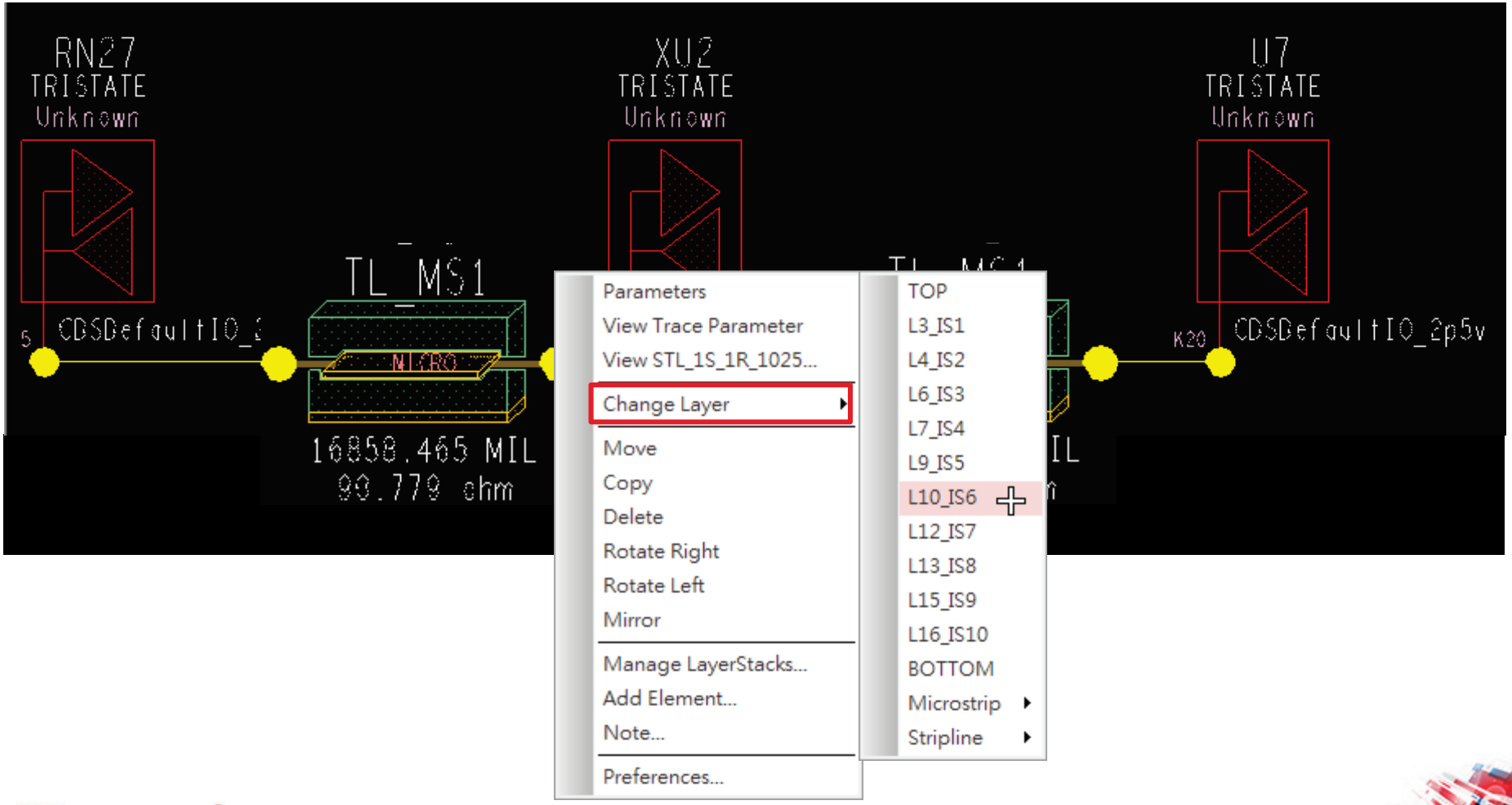
- Virtual Via Padstack Model





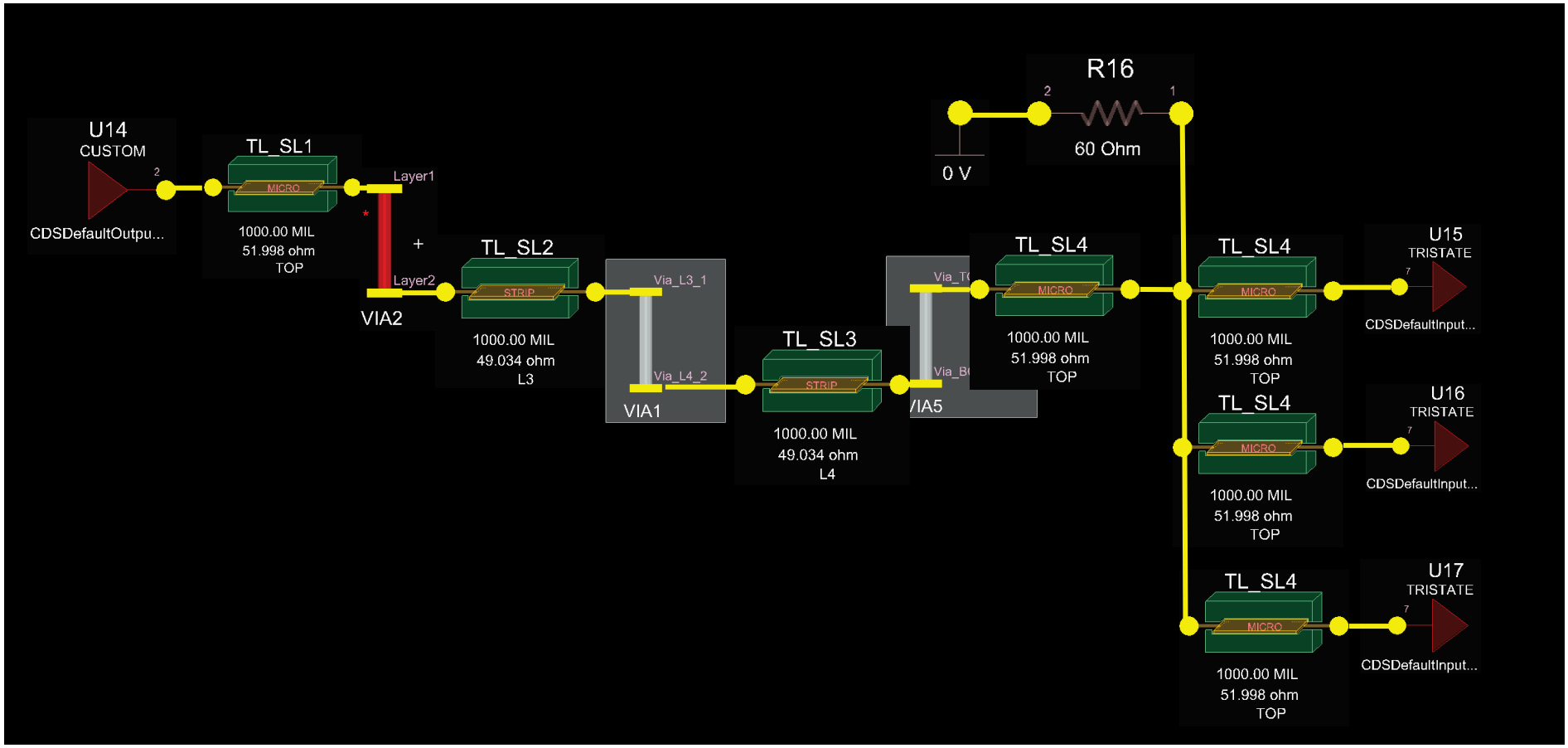
From Idea to Virtual Practicability

- Edit & Assume Transmission Line

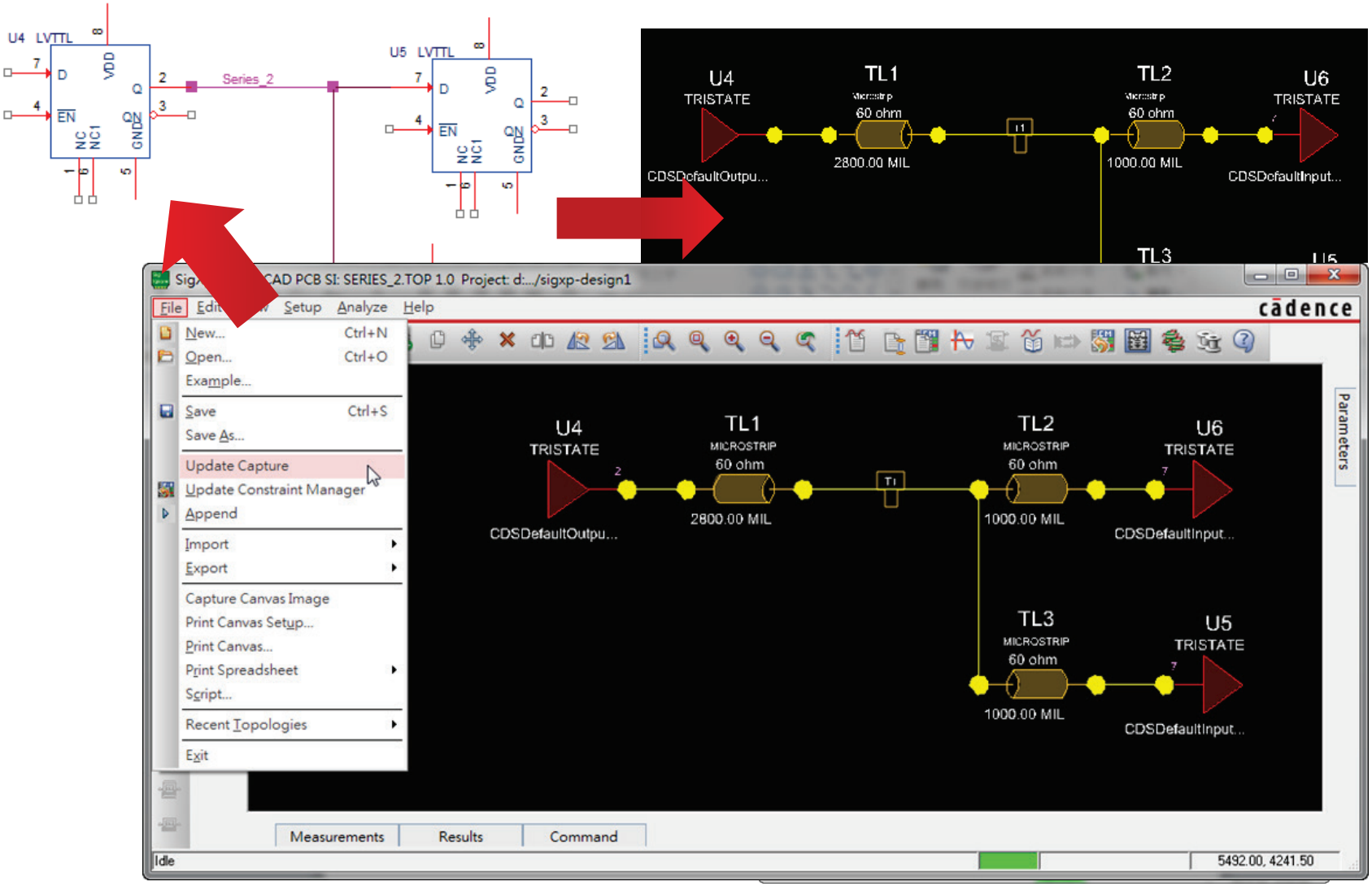


From Idea to Virtual Practicability

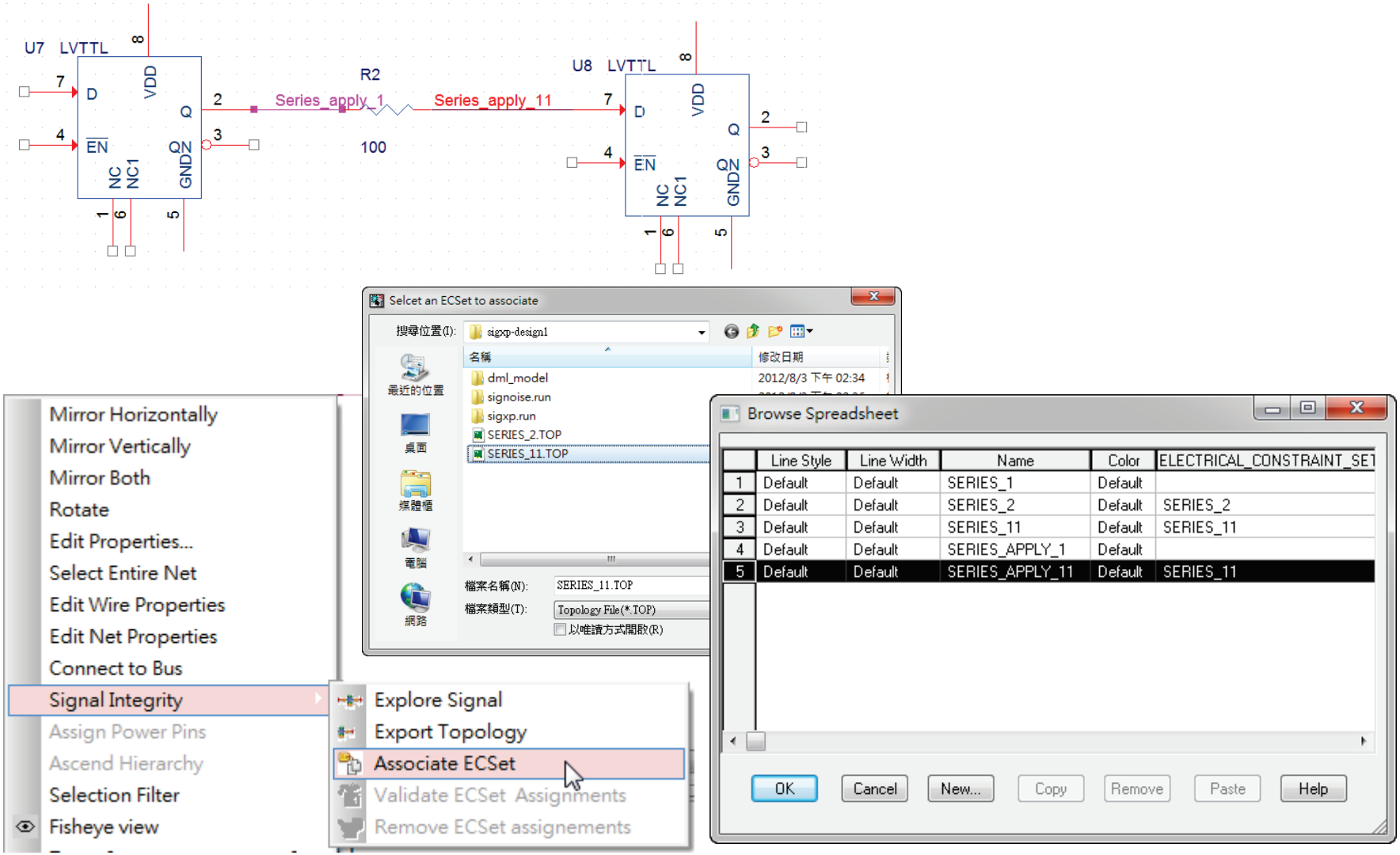
- Restructuring Topology



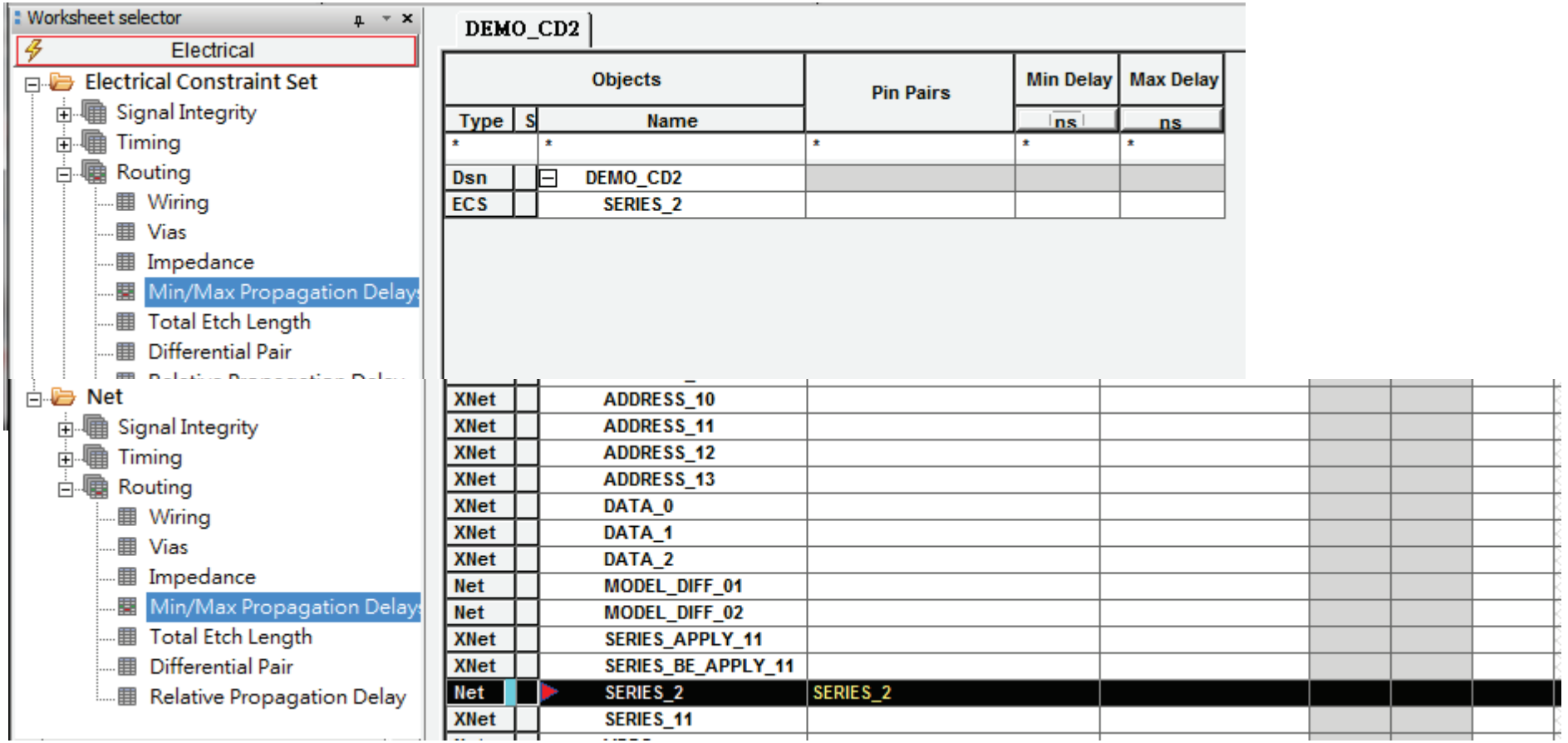
Define Constraints in PCB SI



Replicate ECSet in Schematic



Update To Capture and Netin to OrCAD PCB



Import ECSet From Constraint Manager

Allegro Constraint Manager (connected to Allegro PCB SI XL 16.6) [DEMO_CD2] - [Electrical Constraint Sets: Routing [DEMO_C

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

- Electrical
- Electrical Constraint Set
  - Signal Integrity
  - Timing
  - Routing
    - Wiring
    - Vias
    - Impedance
    - Min/Max Propagation Delay

DEMO_CD2

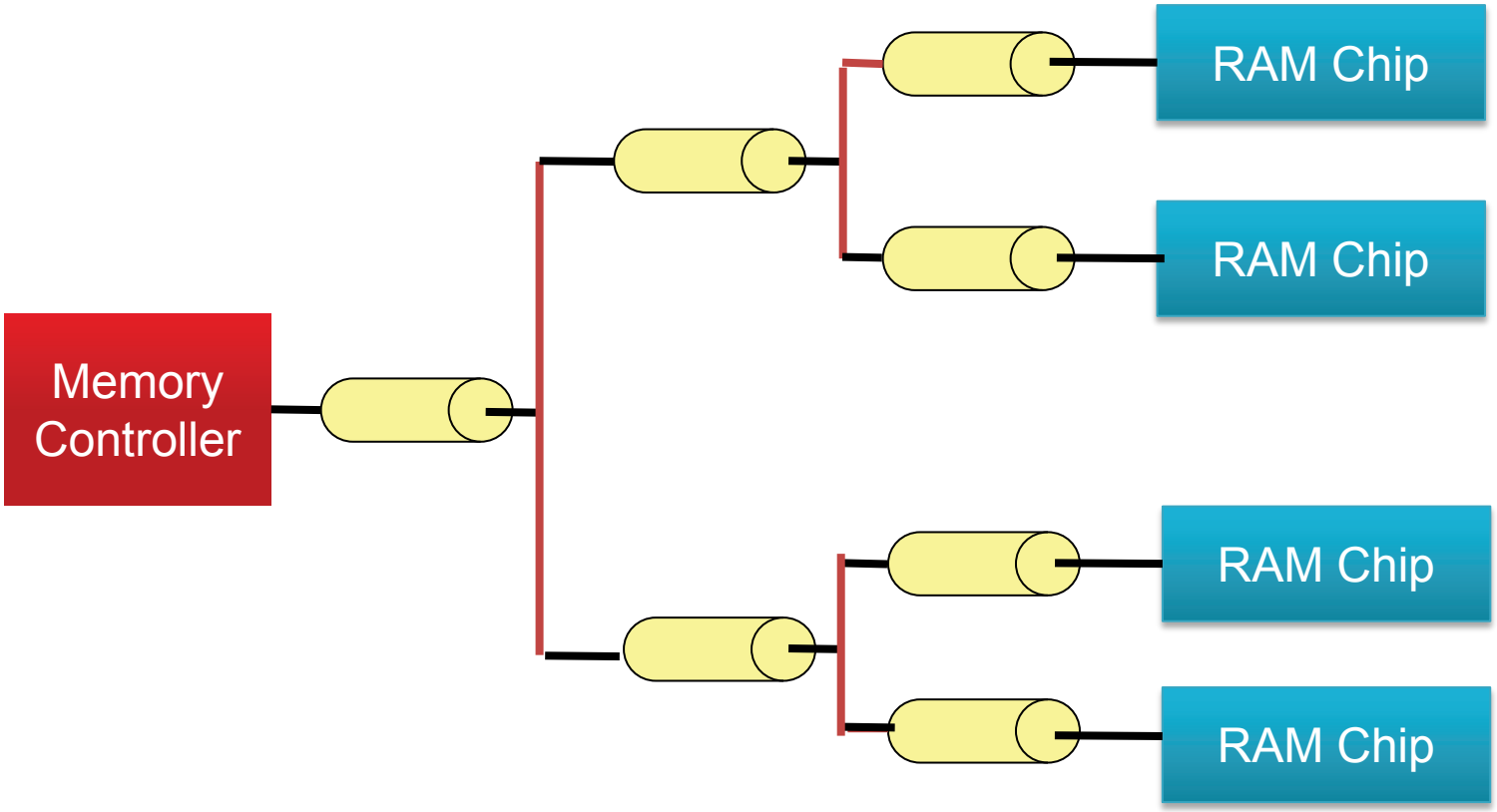
Objects			Pin Pairs	Min Delay	Max Delay
Type	S	Name		ns	ns
*		*	*	*	*
Dsn		DEMO_CD2			
ECS		SERIES_2			
ECSP		NET.T.1:U5.7		1000 mil	1050 mil
ECSP		NET.T.1:U6.7		1000 mil	1050 mil
ECSP		U4.2:NET.T.1		2800 mil	2850 mil

- Net
  - Signal Integrity
  - Timing
  - Routing
    - Wiring
    - Vias
    - Impedance
    - Min/Max Propagation Delay
    - Total Etch Length
    - Differential Pair
    - Relative Propagation Delay

Physical

XNet		ADDRESS_10										
XNet		ADDRESS_11										
XNet		ADDRESS_12										
XNet		ADDRESS_13										
XNet		DATA_0										
XNet		DATA_1										
XNet		DATA_2										
Net		MODEL_DIFF_01										
Net		MODEL_DIFF_02										
XNet		SERIES_APPLY_11										
XNet		SERIES_BE_APPLY_11										
Net		SERIES_2	SERIES_2									50 MIL
PPr		SERIES_2.T.1:U5.7						1000.0...		1050.0...	100.0...	950 MIL
PPr		SERIES_2.T.1:U6.7						1000.0...		1050.0...	1000....	50 MIL
PPr		U4.2:SERIES_2.T.1						2800.0...		2850.0...	1100....	1750 ...

DDRx Routing Topology

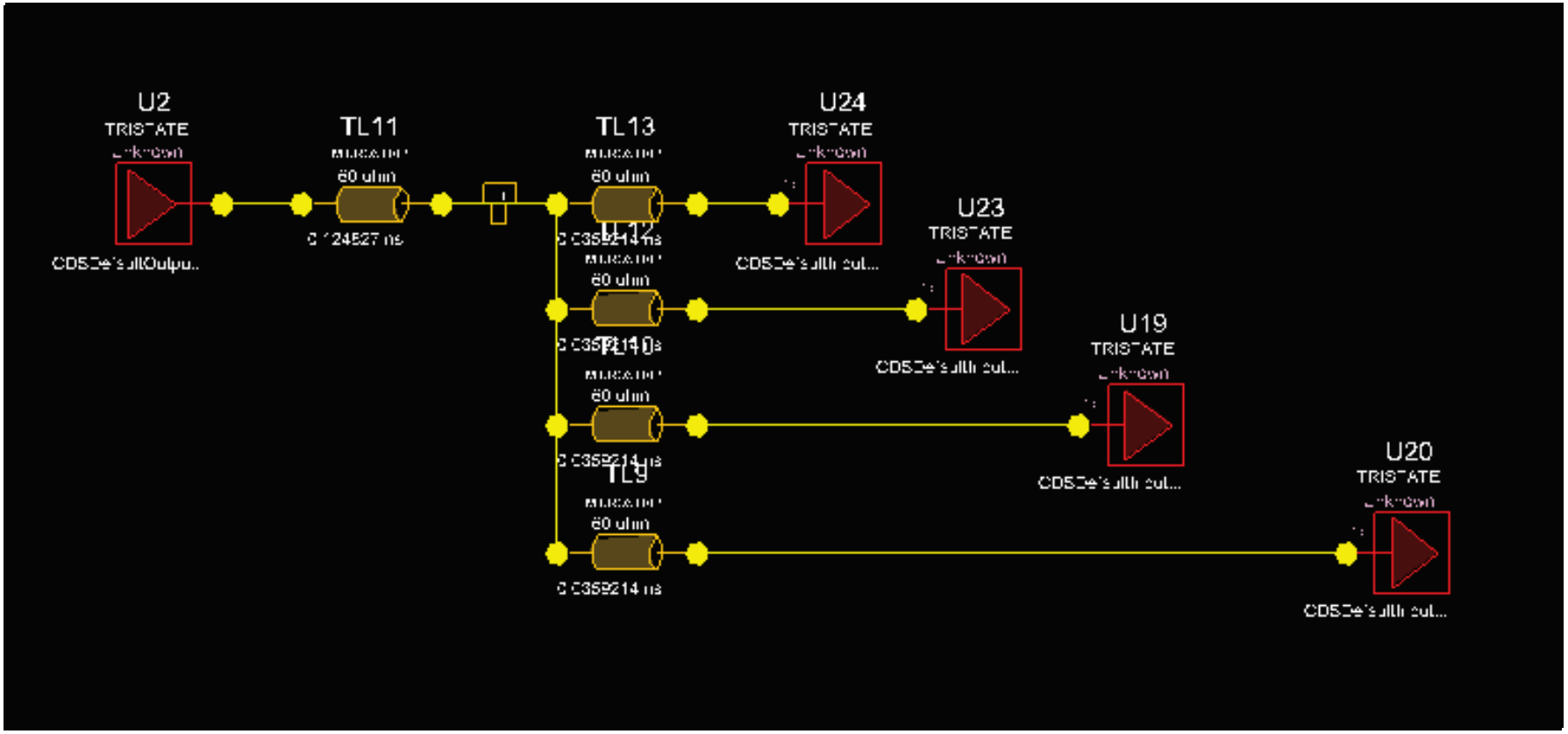


Relative Propagation Delay Constraint Setting Issues

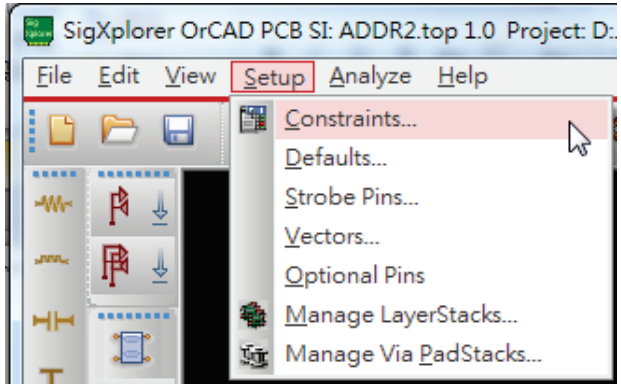
- Create and build bus group
- Create pin-pair by each net
- Match Group by pin-pair
- Assign constraint by each pin-pair
- Determinant who is target for each group

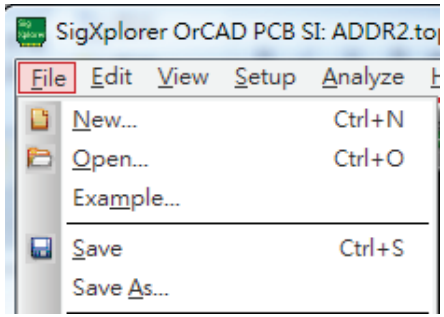
Is it possible much Faster and Easier ?

Determinant Relative Propagation Delay Constraints from PCB SI

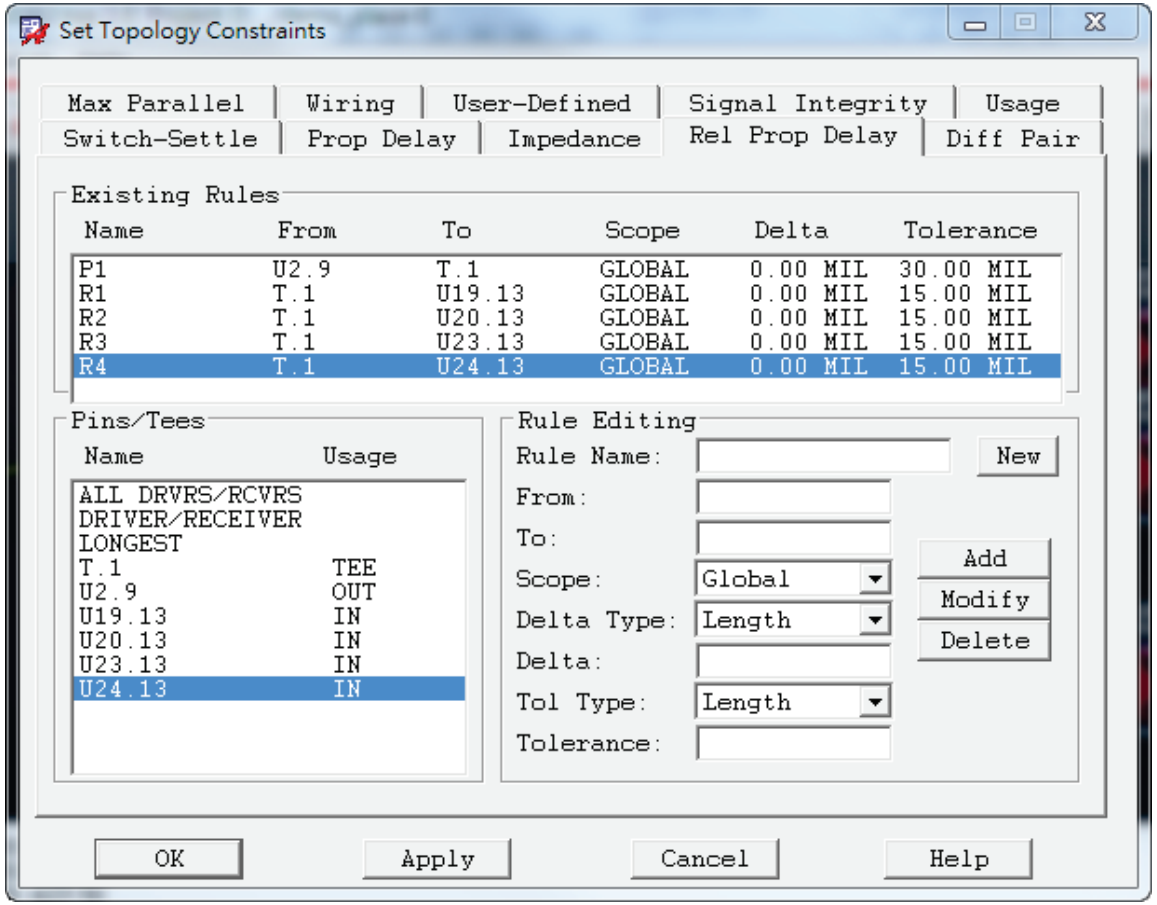


Define Relative Propagation Delay Constraints

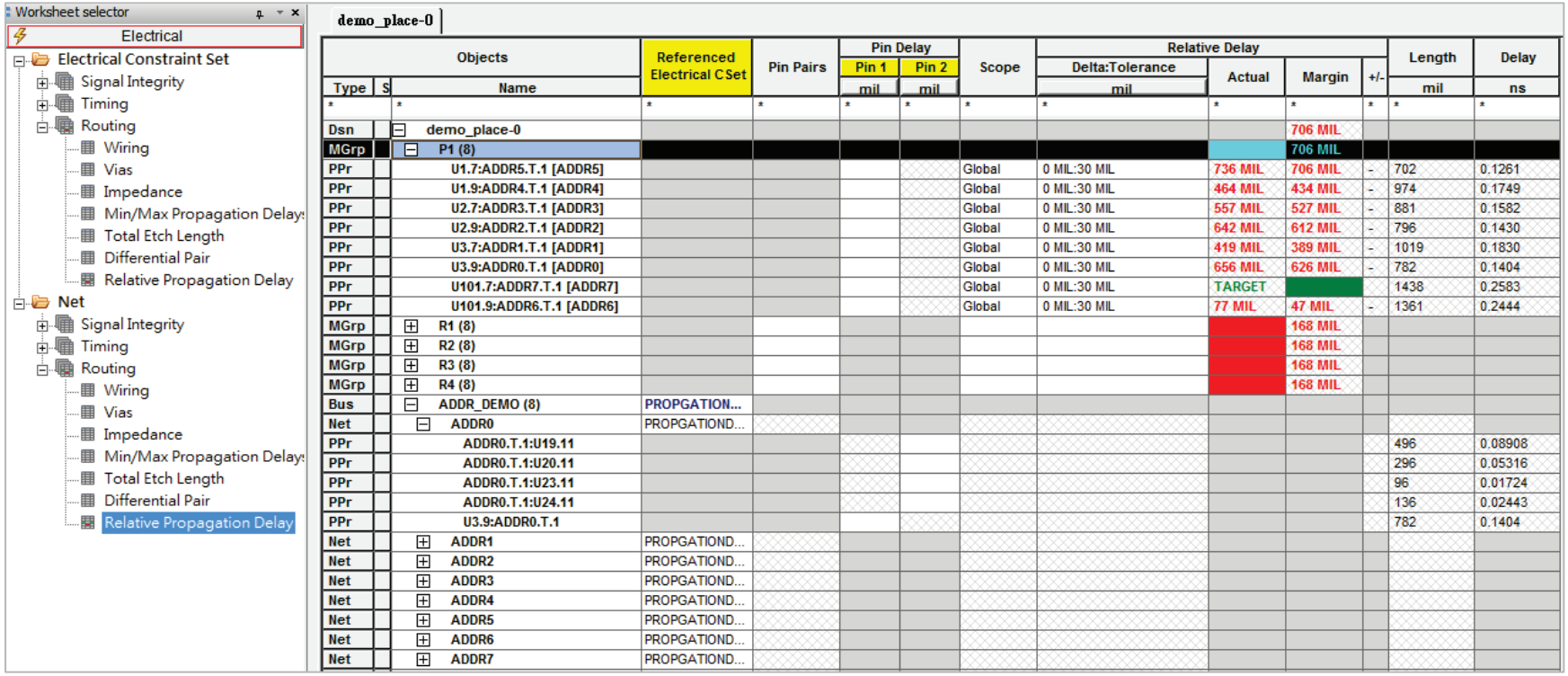




Save topology file for ECset

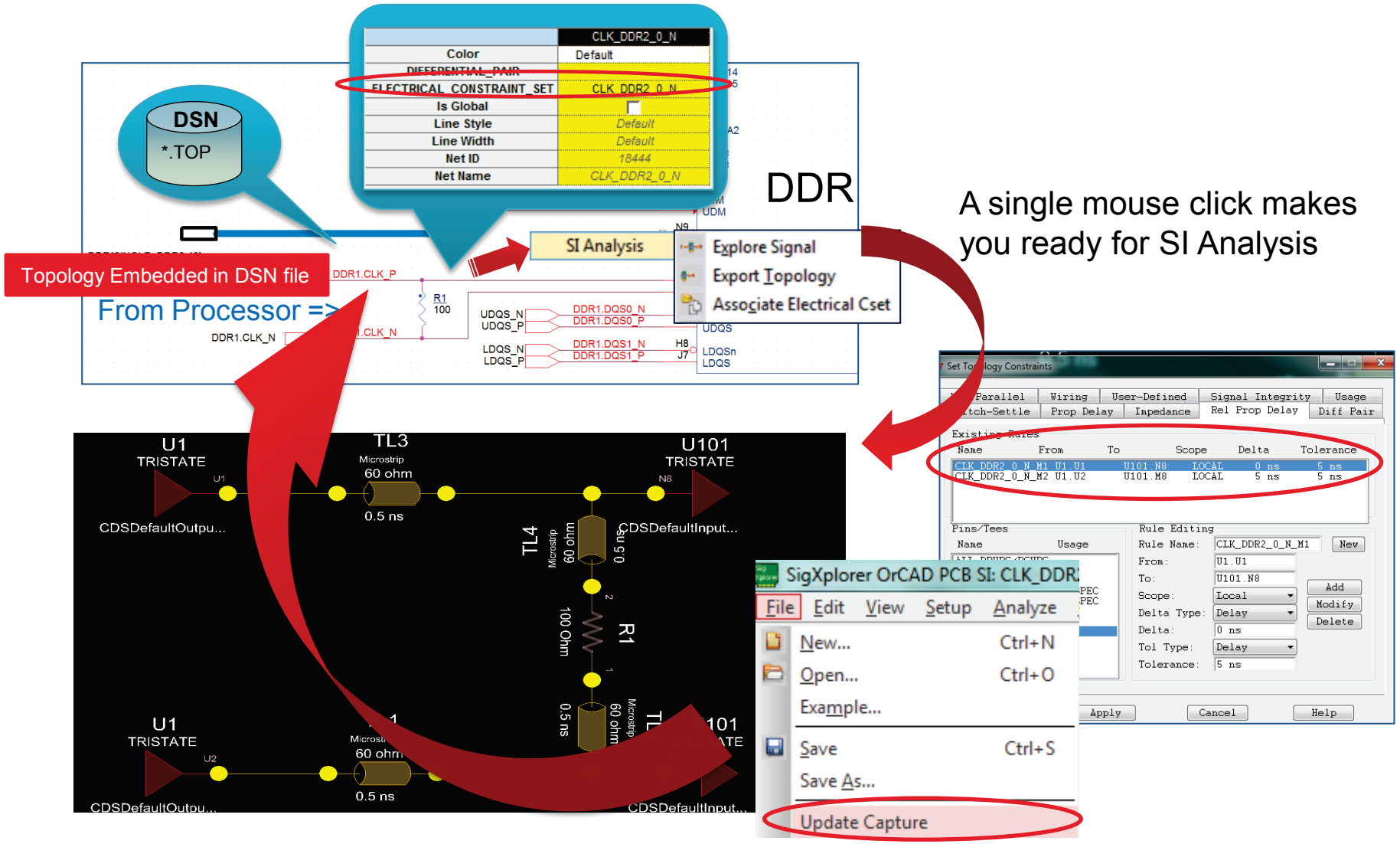


Apply ECset in Constraint Manager



Objects			Referenced Electrical CSet	Pin Pairs	Pin Delay		Scope	Relative Delay				Length	Delay
					Pin 1	Pin 2		Delta:Tolerance	Actual	Margin	+/-		
Type	S	Name			mil	mil		mil				mil	ns
*		*	*	*	*	*	*	*	*	*	*	*	*
Dsn		demo_place-0								706 MIL			
MGrp		P1 (8)								706 MIL			
PPr		U1.7:ADDR5.T.1 [ADDR5]					Global	0 MIL:30 MIL	736 MIL	706 MIL	-	702	0.1261
PPr		U1.9:ADDR4.T.1 [ADDR4]					Global	0 MIL:30 MIL	464 MIL	434 MIL	-	974	0.1749
PPr		U2.7:ADDR3.T.1 [ADDR3]					Global	0 MIL:30 MIL	557 MIL	527 MIL	-	881	0.1582
PPr		U2.9:ADDR2.T.1 [ADDR2]					Global	0 MIL:30 MIL	642 MIL	612 MIL	-	796	0.1430
PPr		U3.7:ADDR1.T.1 [ADDR1]					Global	0 MIL:30 MIL	419 MIL	389 MIL	-	1019	0.1830
PPr		U3.9:ADDR0.T.1 [ADDR0]					Global	0 MIL:30 MIL	656 MIL	626 MIL	-	782	0.1404
PPr		U101.7:ADDR7.T.1 [ADDR7]					Global	0 MIL:30 MIL	TARGET			1438	0.2583
PPr		U101.9:ADDR6.T.1 [ADDR6]					Global	0 MIL:30 MIL	77 MIL	47 MIL	-	1361	0.2444
MGrp		R1 (8)								168 MIL			
MGrp		R2 (8)								168 MIL			
MGrp		R3 (8)								168 MIL			
MGrp		R4 (8)								168 MIL			
Bus		ADDR_DEMO (8)	PROPGATION...										
Net		ADDR0	PROPGATIOND...										
PPr		ADDR0.T.1:U19.11										496	0.08908
PPr		ADDR0.T.1:U20.11										296	0.05316
PPr		ADDR0.T.1:U23.11										96	0.01724
PPr		ADDR0.T.1:U24.11										136	0.02443
PPr		U3.9:ADDR0.T.1										782	0.1404
Net		ADDR1	PROPGATIOND...										
Net		ADDR2	PROPGATIOND...										
Net		ADDR3	PROPGATIOND...										
Net		ADDR4	PROPGATIOND...										
Net		ADDR5	PROPGATIOND...										
Net		ADDR6	PROPGATIOND...										
Net		ADDR7	PROPGATIOND...										

- Auto create Pin-Pair by Each Net
- Auto match Group by Pin-Pair
- Auto assign constraint by each Pin-Pair



Summary

- Verify Your Function Design with OrCAD PSpice
  1. Confirm your design easy and fast
  2. Stability and repeatability for mass production

- Enhance constraints design flow with OrCAD PCB SI
  1. Determine with **PCB effective** design constraints easy and fast
  2. It can back annotate ECset and store information in Capture
  3. Direct translate Design Constraint with Netlist files
  4. Drawing and constraints reuse