Si-Interposer Collaboration in IC/PKG/SI

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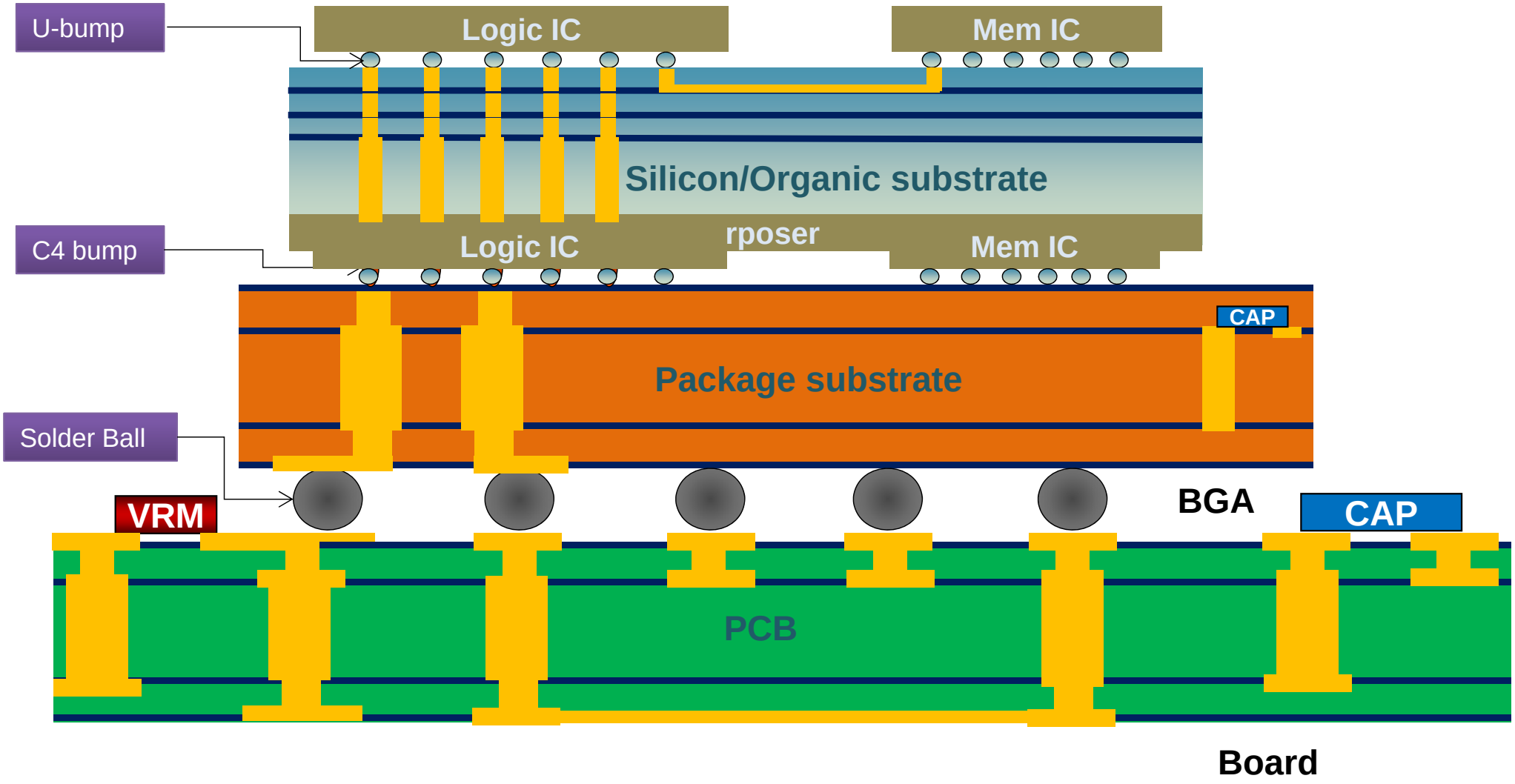
Graser®

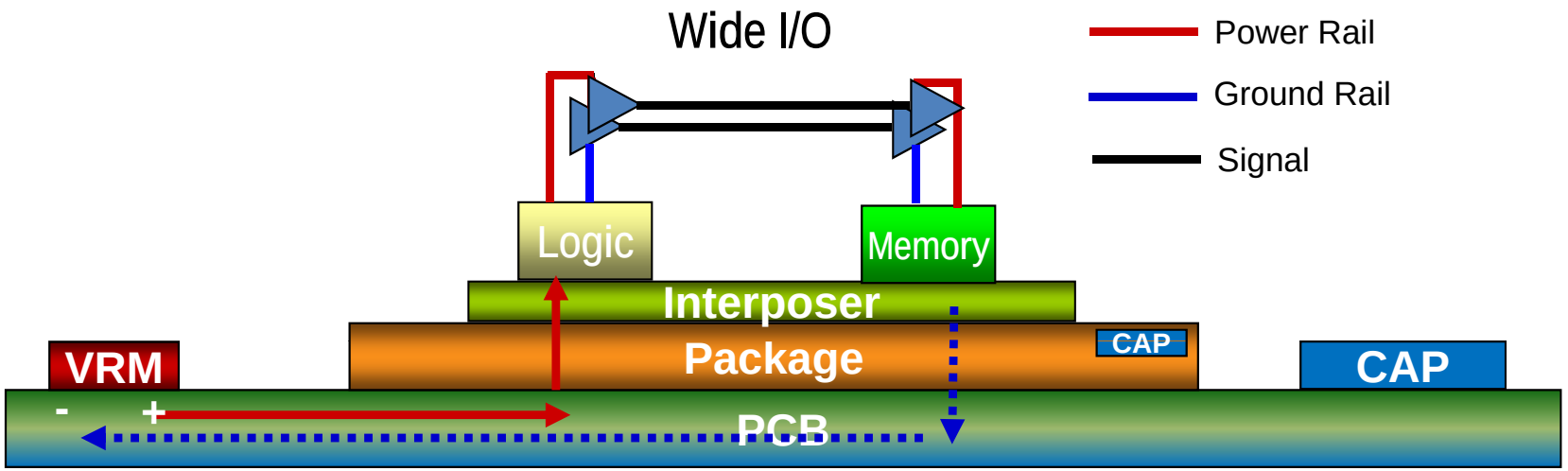
Design Overview



courtesy of TSMC

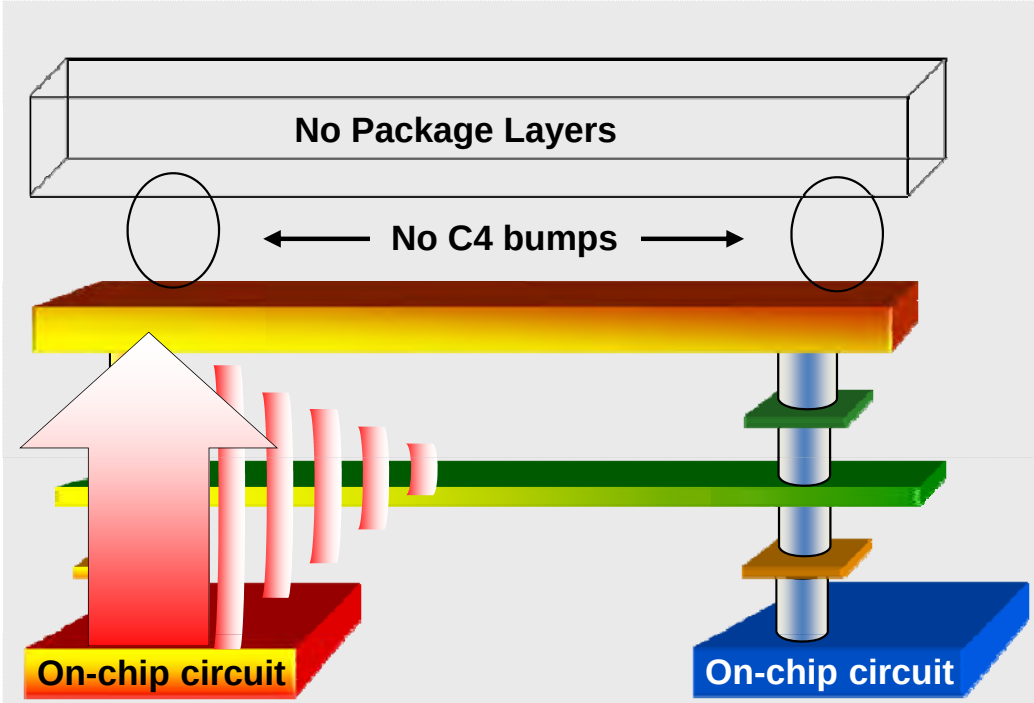
System Architecture

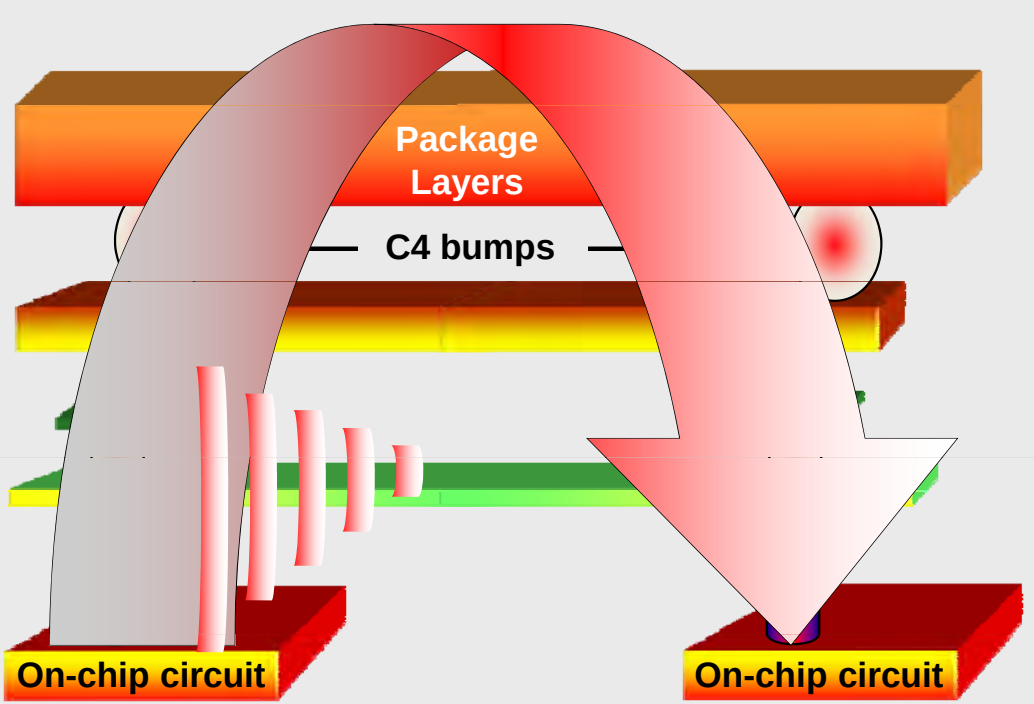
from electrical characteristic perspective



- The system power is supplied by voltage regulation module (VRM) on PCB
- Multiple power delivery path from VRM, decaps on PCB, parasitic of capacitance from chip, package and PCB to fulfill different current demand by wide I/O circuits in different frequency bandwidth
- Signal waveform from output buffer is generated by current sink of I/O circuit from the PDN system

Why does Chip-System Co-Design?





Chip

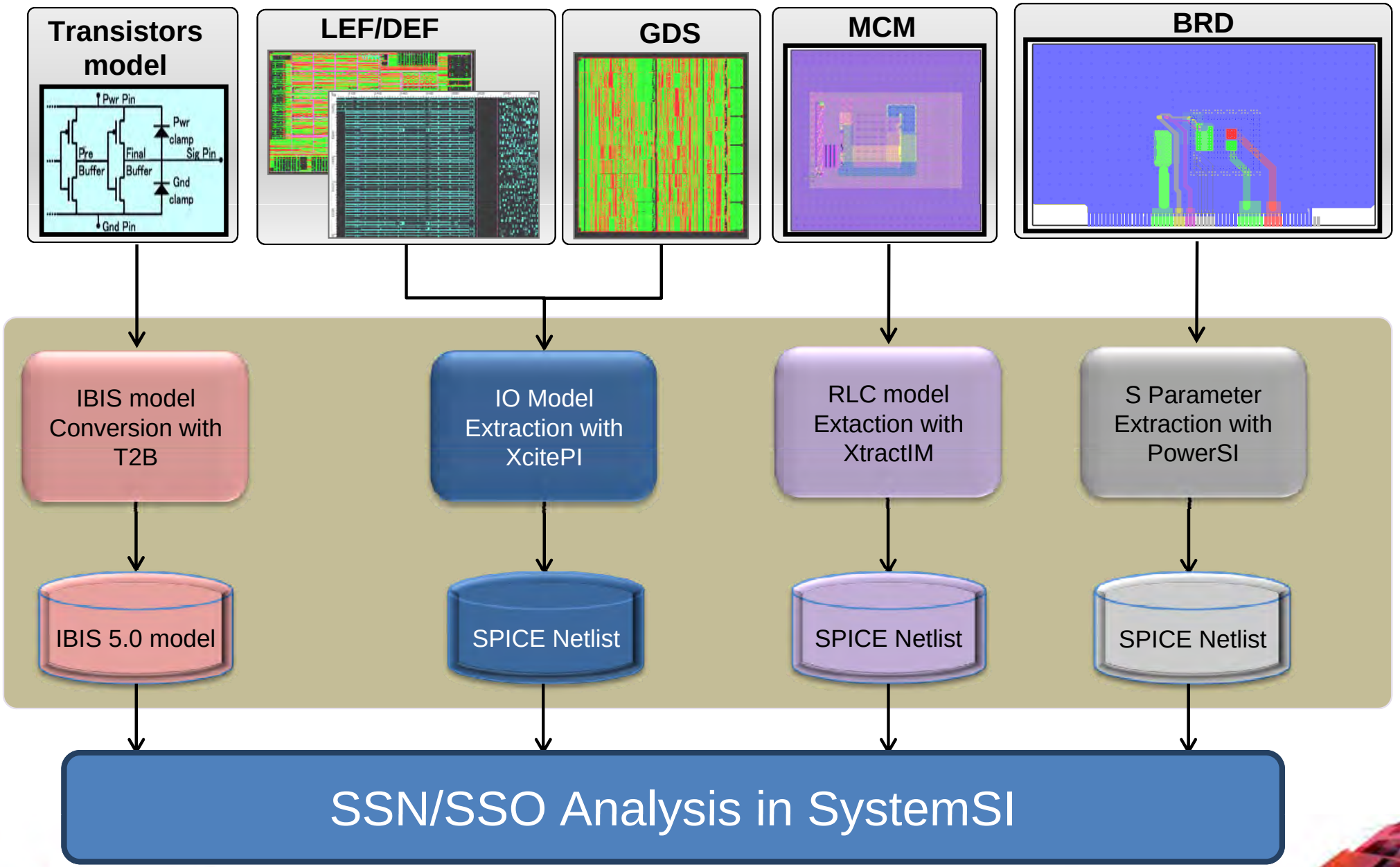
Highly resistive / High-loss system
Results in localized voltage noise effects

Package

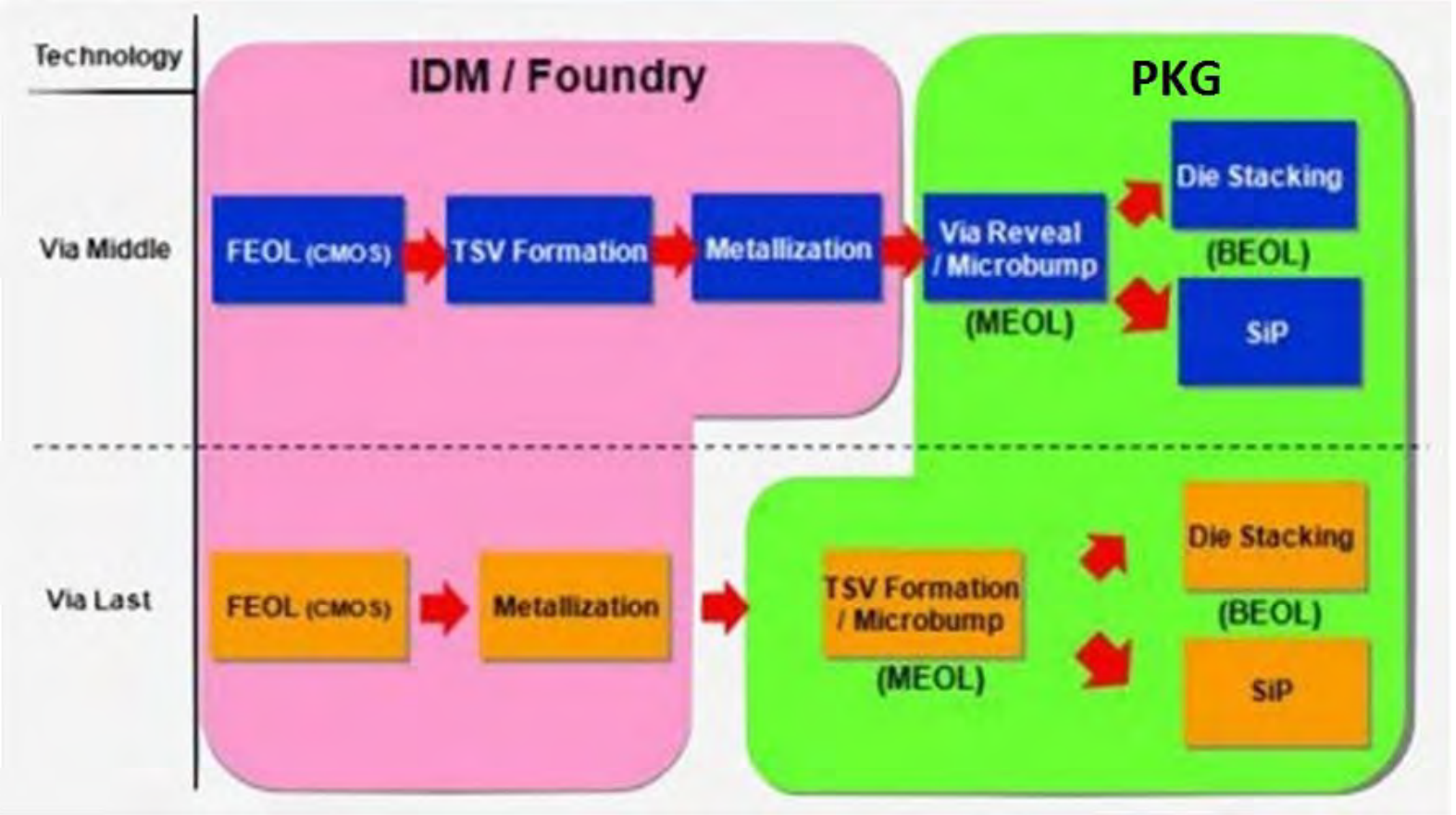
Low impedance / Low-loss system
Results in global voltage noise effects to other IC circuits

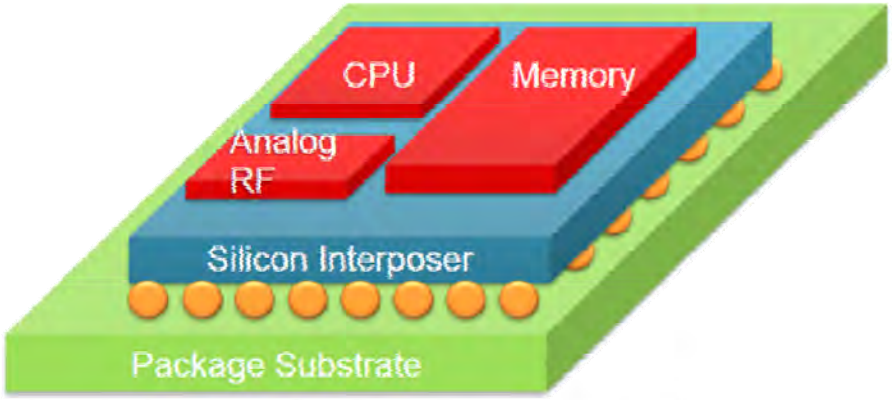
The low-loss power distribution system of the package easily transfers voltage noise effects to other on-chip circuits

SSO/SSN Analysis with Cadence Sigrity



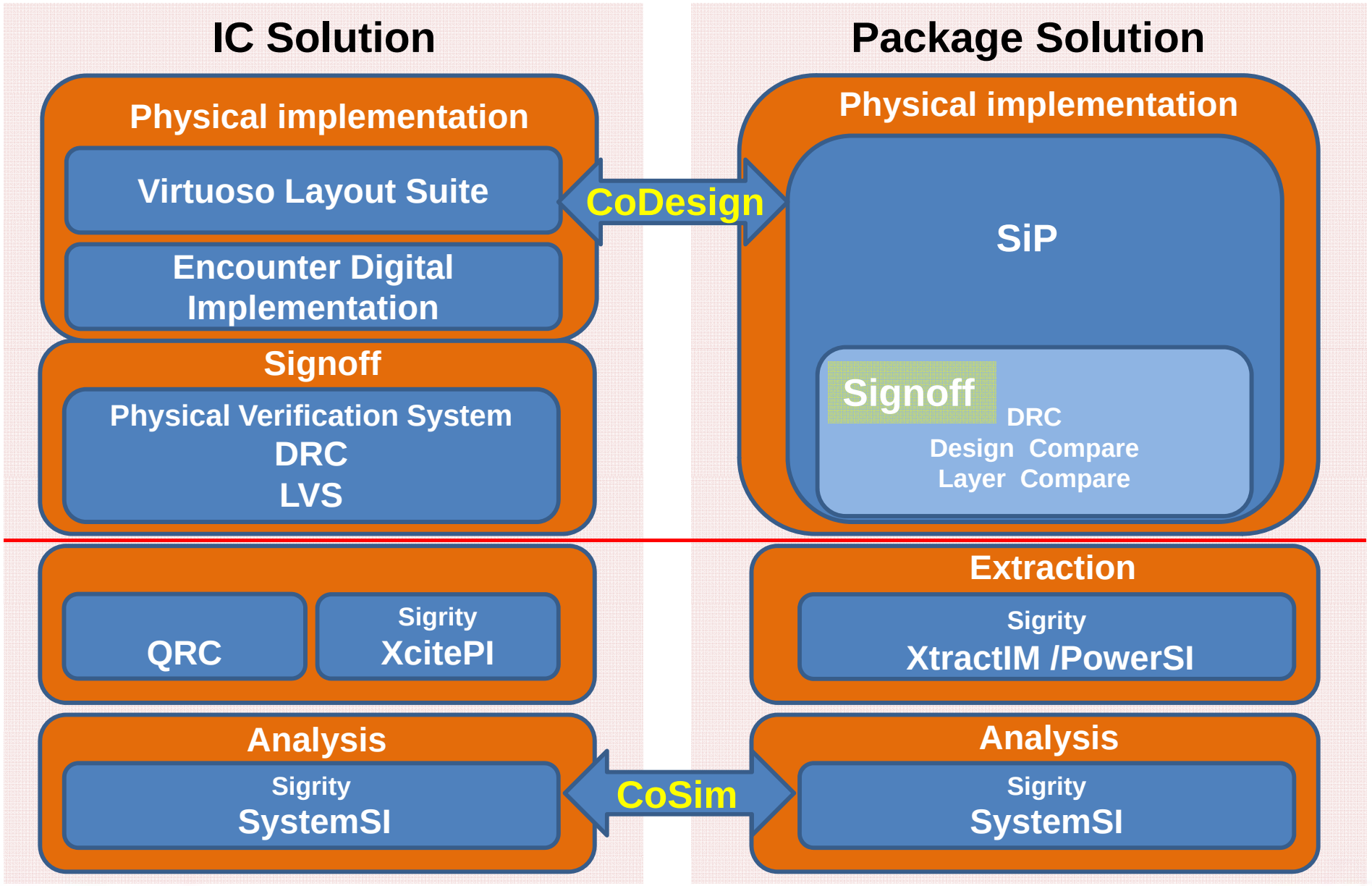
Si-Interposer in IC/SiP





courtesy of PTI

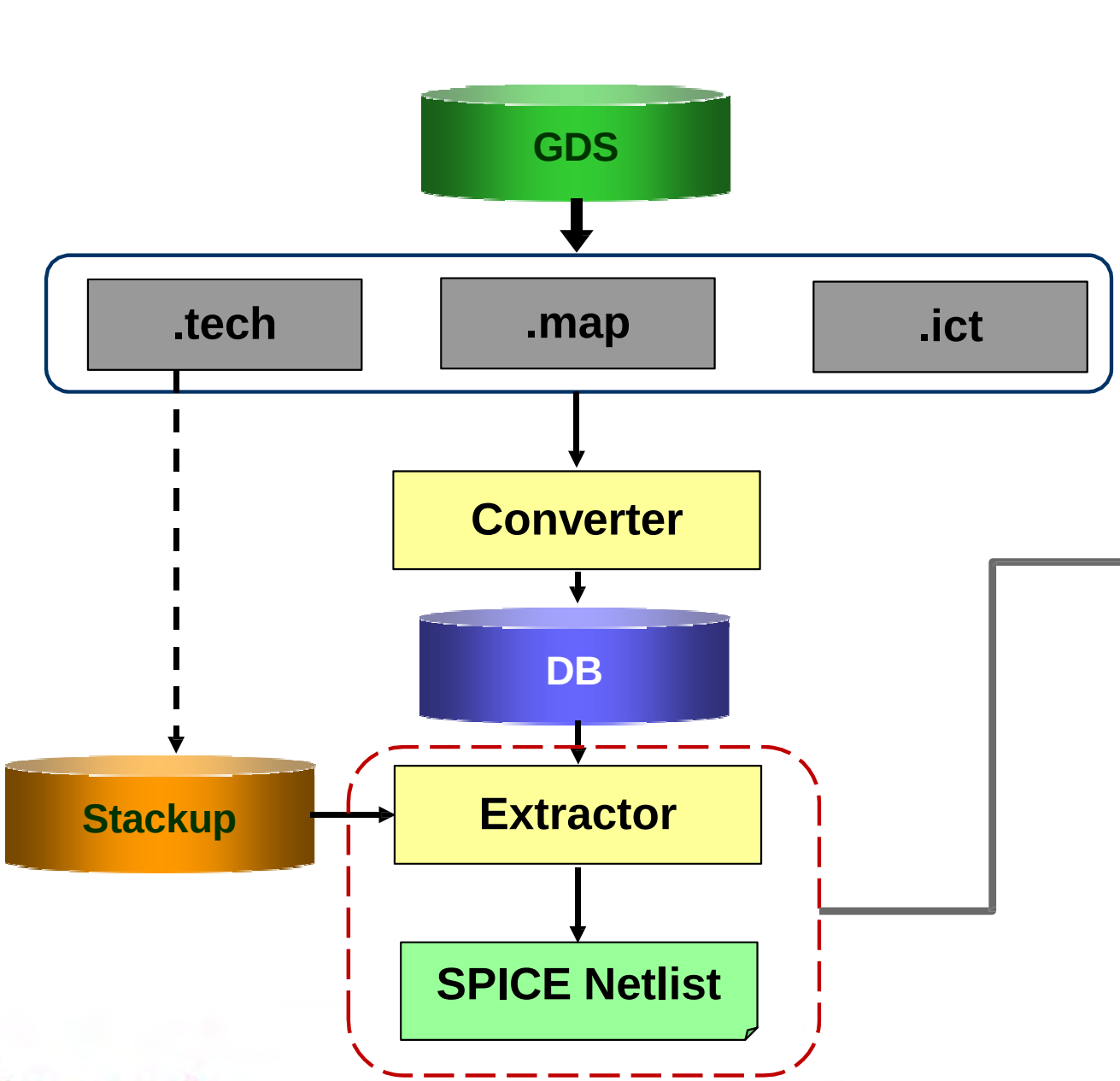
CoDesign/CoSim by IC/PKG/Sigrity



IC-oriented Interposer Model Extraction

XcitePI – IO Model Extraction

I/O Model Extraction with XcitePI-IOME



IO Model Extraction

Manage Design
- New Design
- Open Design
- Save

Technology Setup
- Package Type
- Bump Parameter
- Stackup
- Via Resistance

Chip Setup
- Chip Size
- Net
- Bump
- Via
- Core Area

Circuit Setup
- Definition
- Placement
- Decap
- External Component

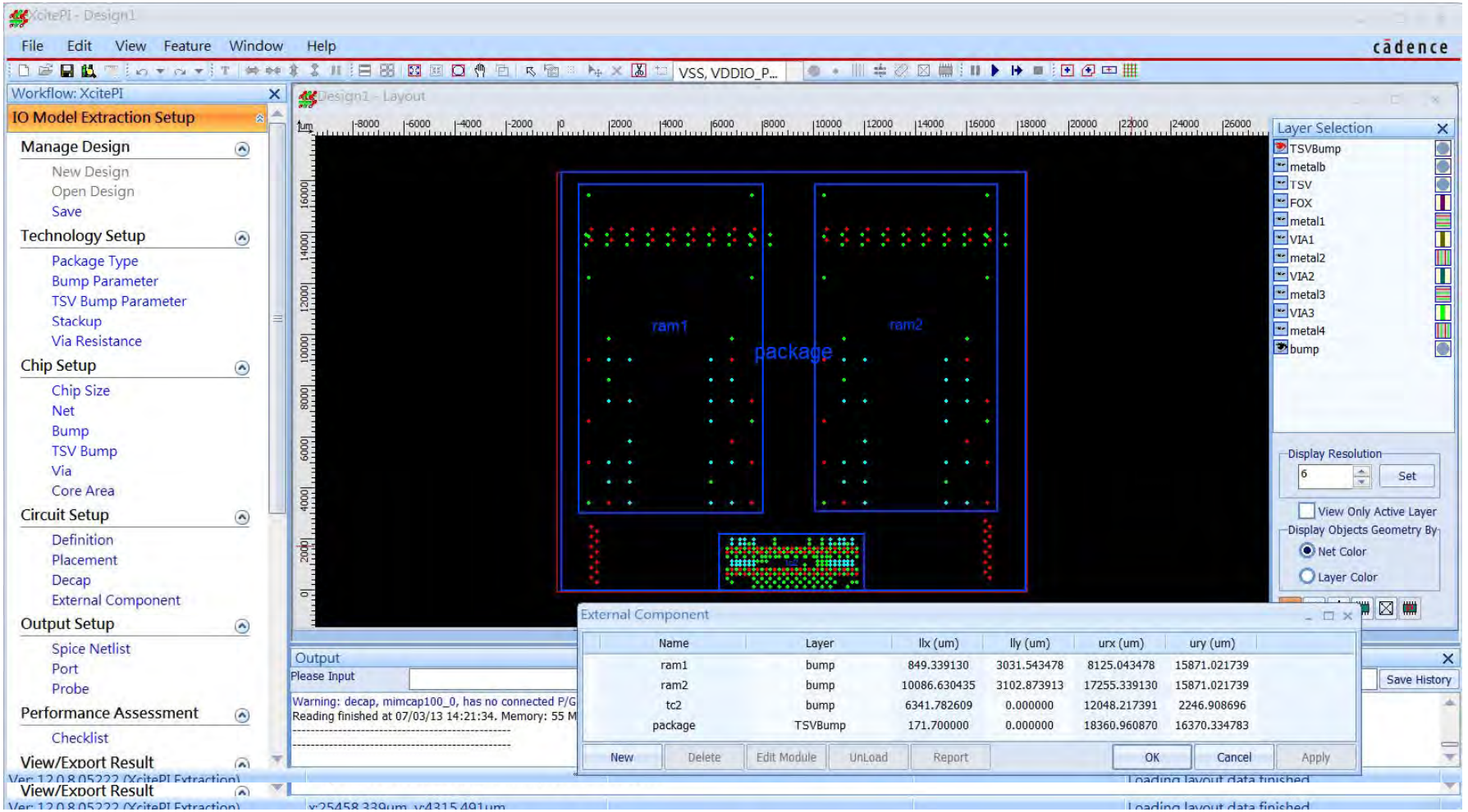
Output Setup
- Spice Netlist
- Port
- Probe

Performance Assessment
- Checklist

View/Export Result

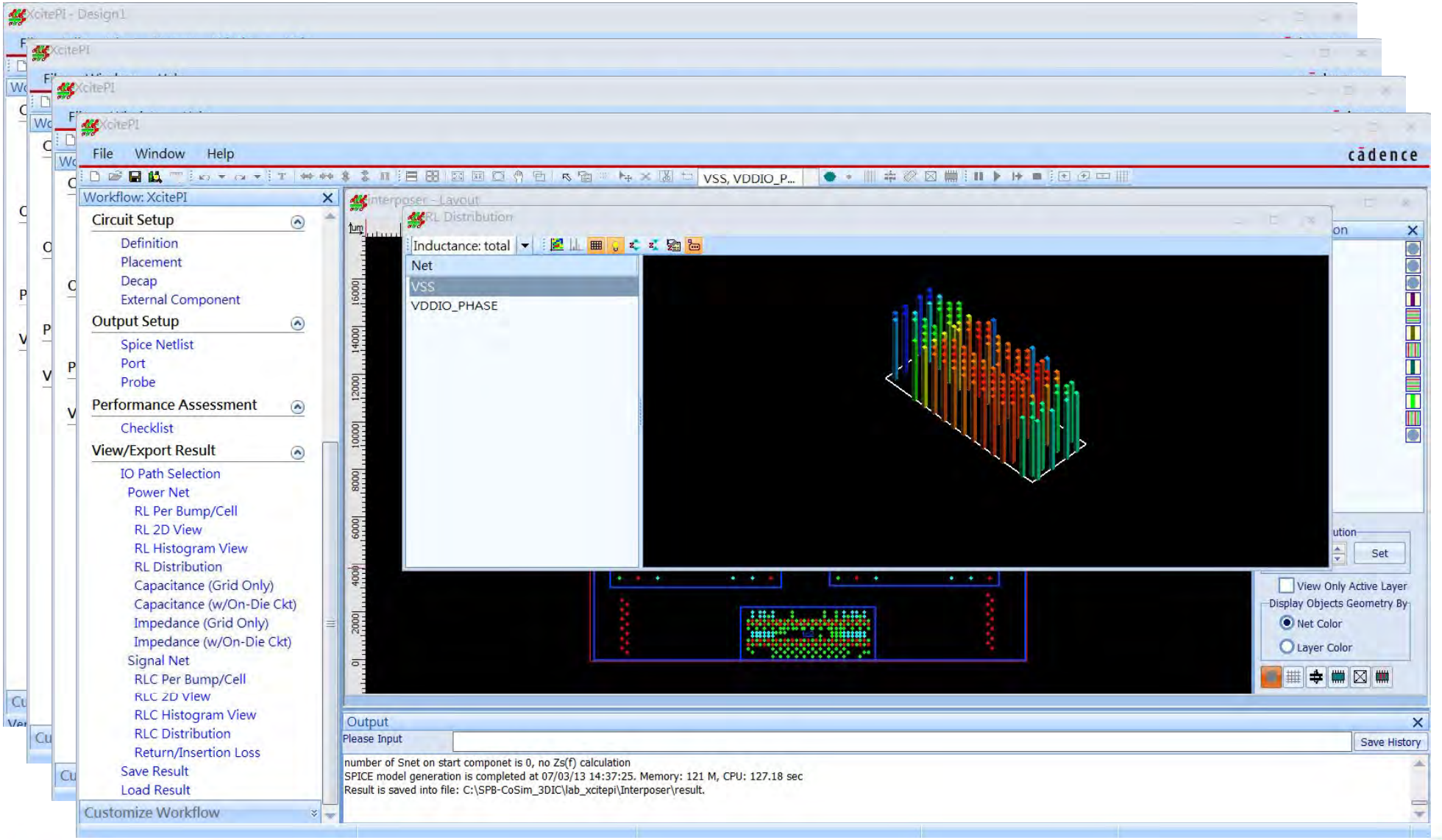
Work flow to guide you how to generate I/O model

XcitePI - IOME

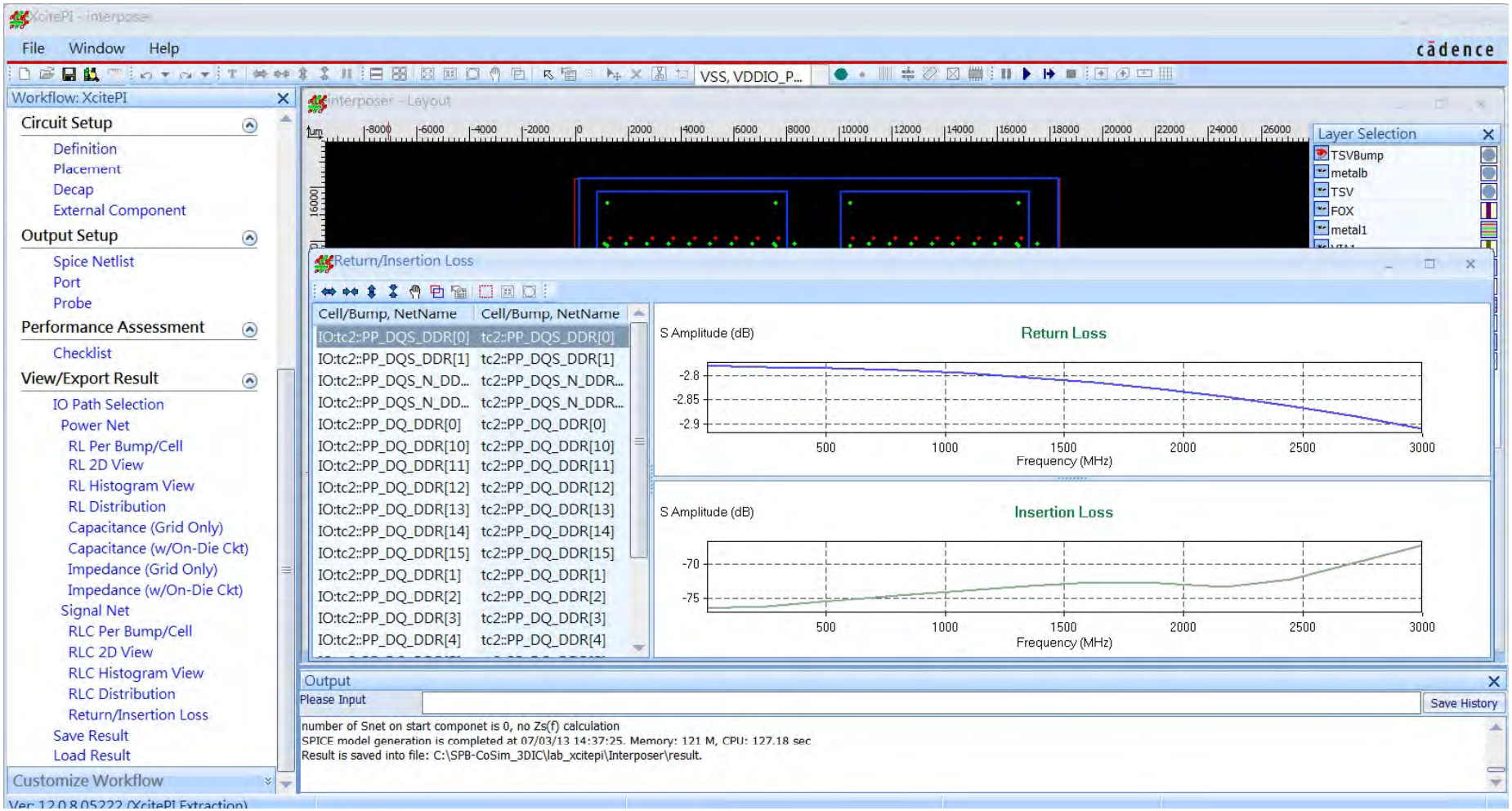


XcitePI - IOME

- EPA

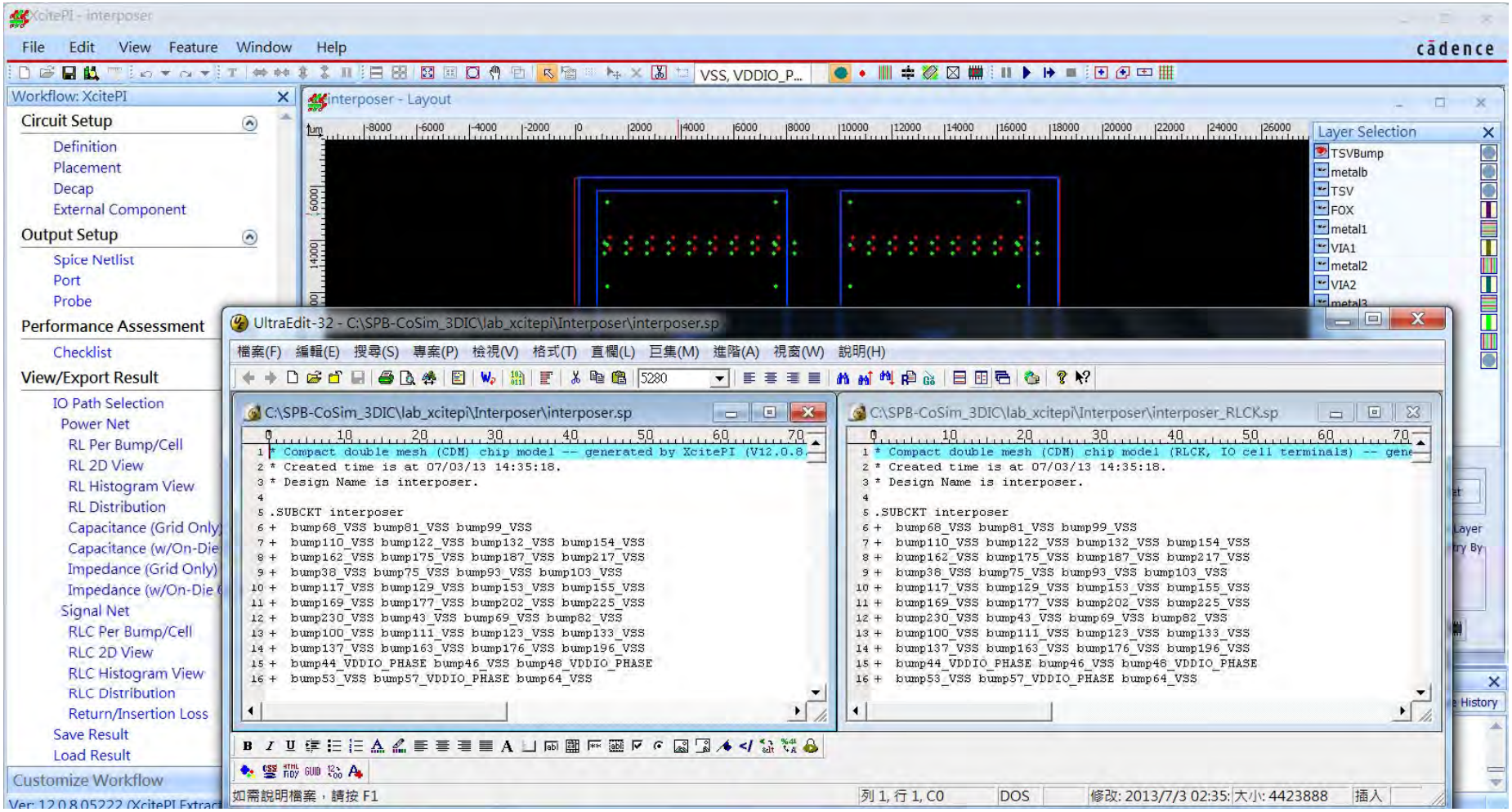


XcitePI - IOME



XcitePI - IOME

- Model extraction



Published TSV Circuit Modeling

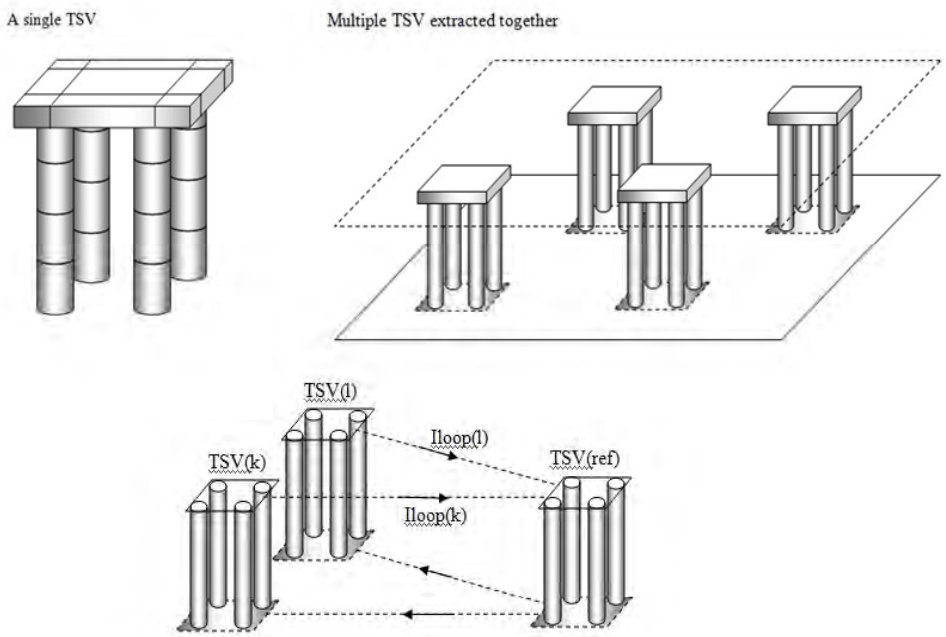
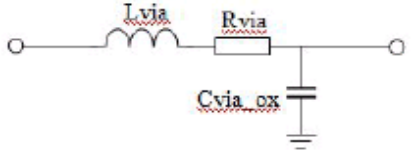
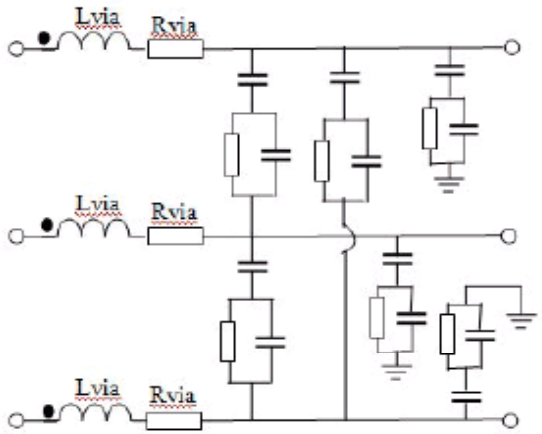
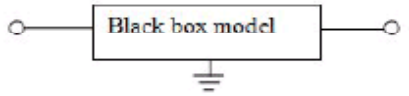


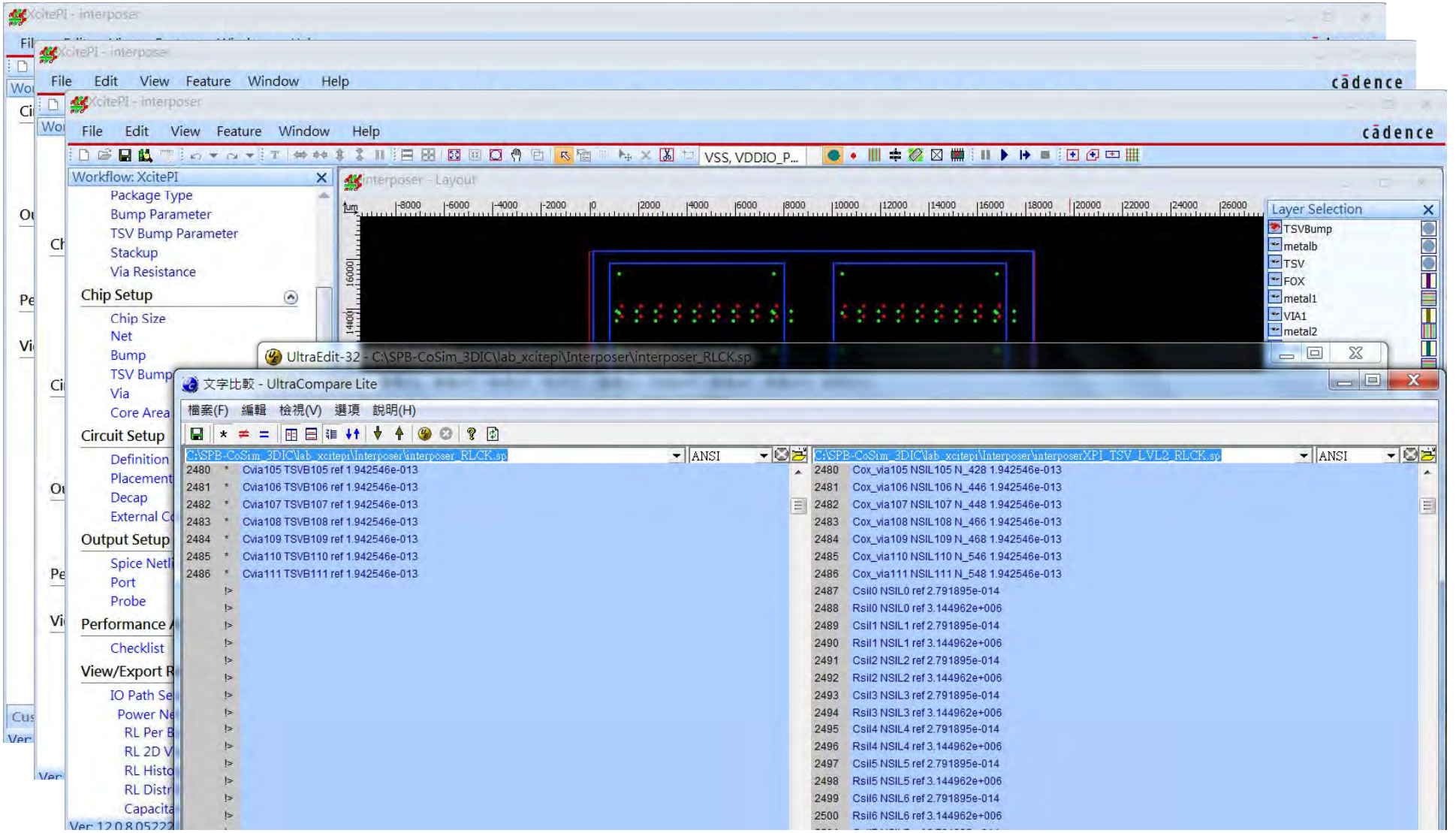
Fig. 12 The loop inductance of TSVs

Level 0: DC circuit, only contained Rvia, used for IR drop analysis or connection testing.	
Level 1: Simple RLC model Have PG loop inductance, capacitance to the substrate, no via-via coupling	
Level 2: Pin based circuit model. Have the L matrix and C matrix based on each TSV branches.	
Level 5: user defined TSV model	

About TSV modeling:

- We didn't calculate each via's partial inductance and mutual inductance. If we do so, that will form a huge circuit matrix that can't be simulated in HSPICE
- We adopt loop calculation. For example, we have n vias, then we have (n-1) loop, then we calculate (n-1) loop and consider coupling between loops. But loop coupling will decay very fast, then final circuit matrix will be small.

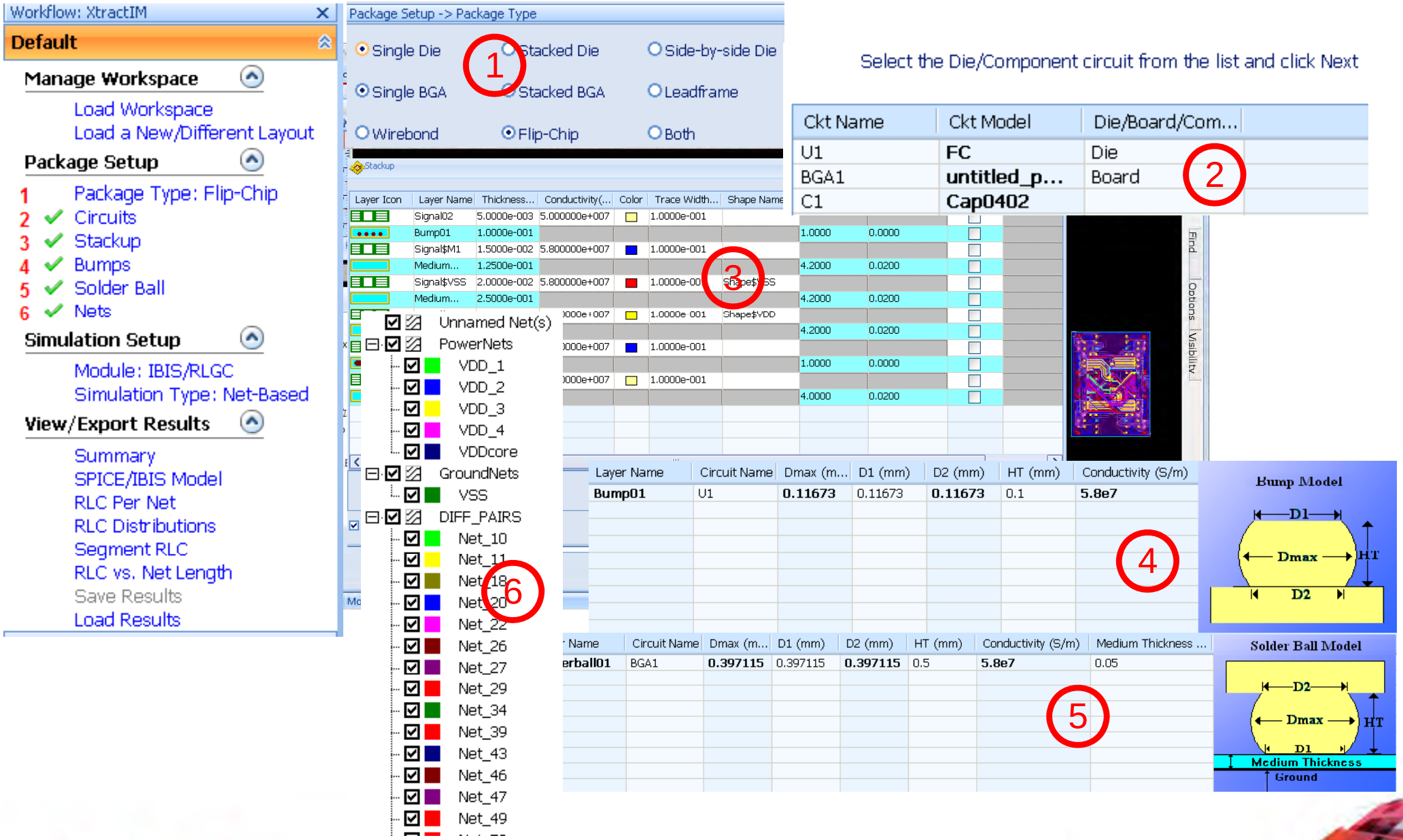
Published TSV Circuit Modeling



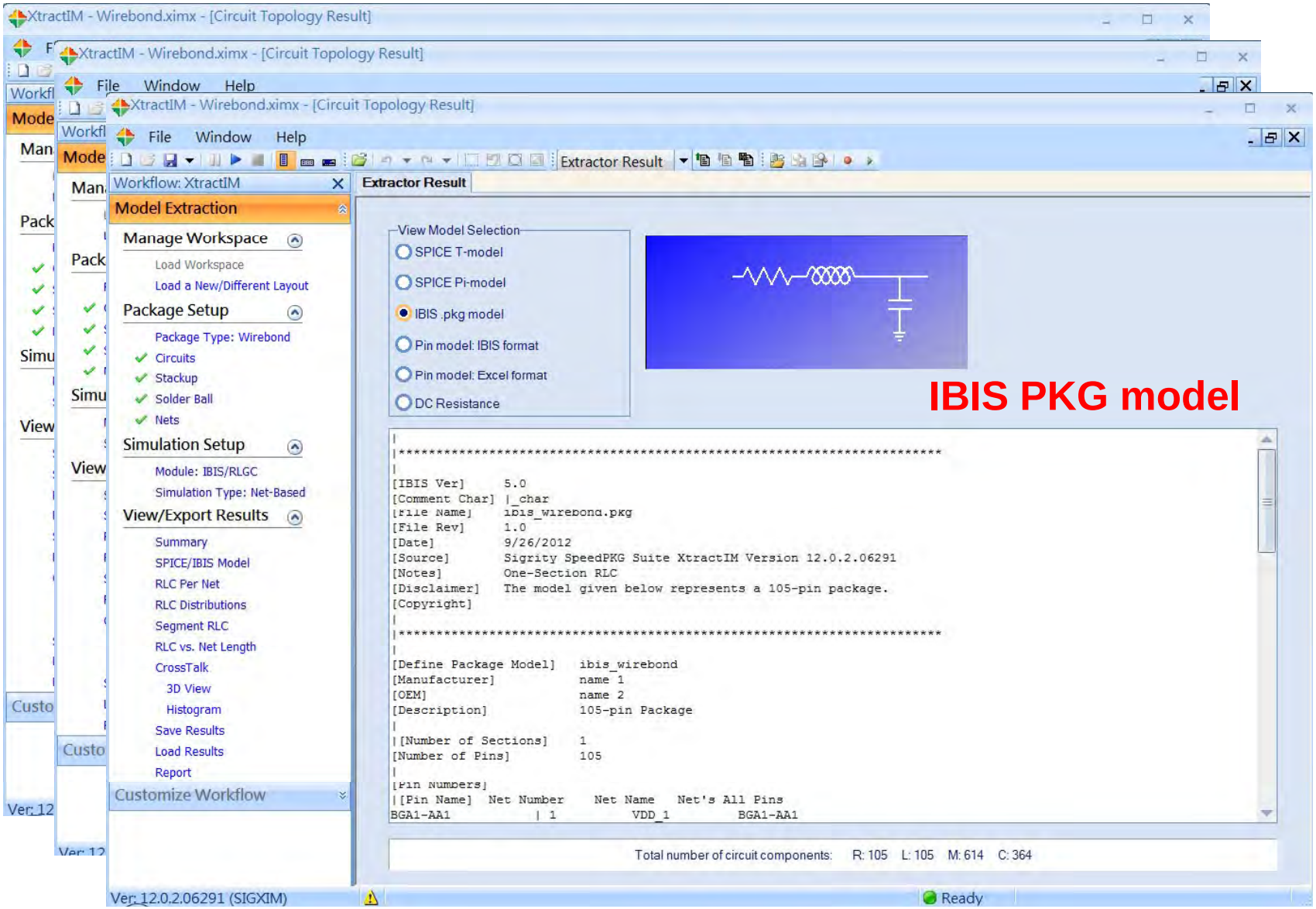
PKG-oriented Interposer Model Extraction

XtractIM – EPA & Model Extraction

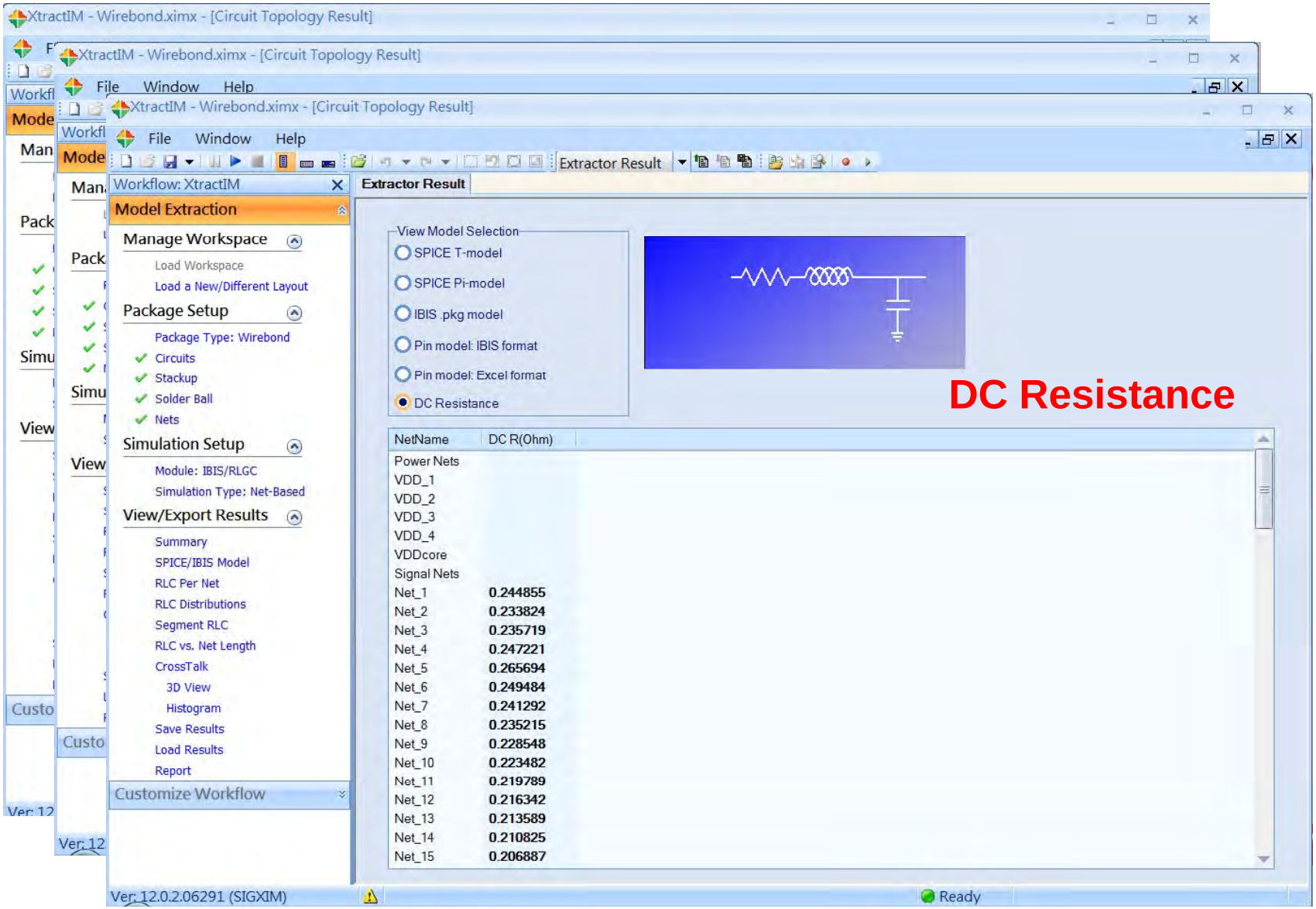
Model Extract



Model Extract



Model Extract

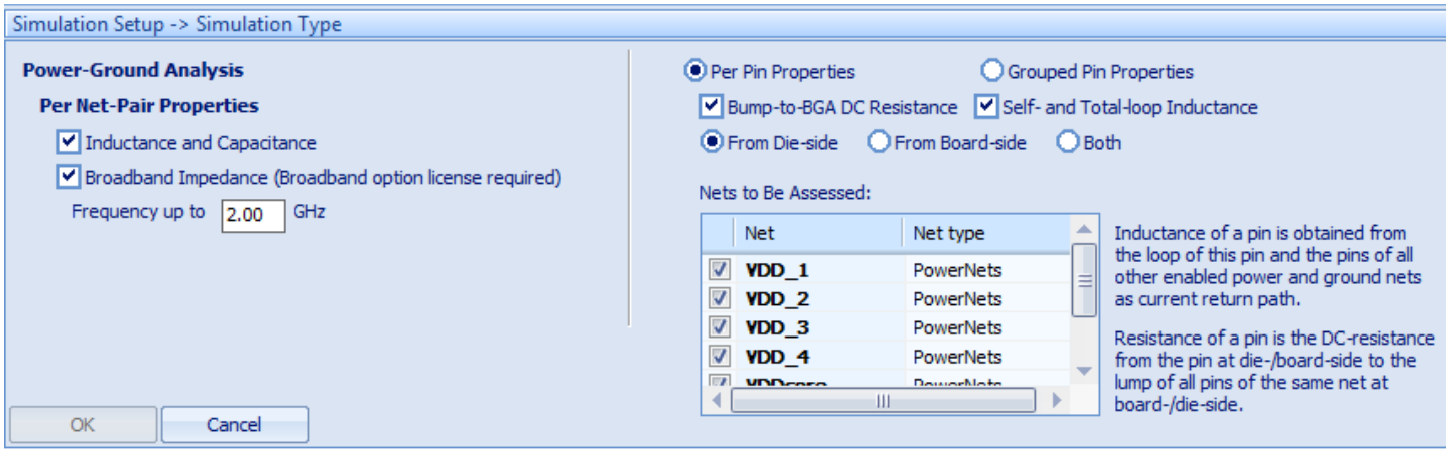


Resource and Result Overview

ResourceProfile_Extractor.log	Resource log file
ExtractorRunTimeError.log	Error log file
Un_Xtracted_NetName.log	log file to tell what nets are open nets and not be extracted.
SPDfilename_PinModel.csv	List pin, net name, net-length, R,L,C, and Delay for Power and Signal nets
SPDfilename_DCResistance.csv	List net name, DC R for Power, Signal, Ground net
SPDfilename_TableContent.csv	Full RLC matrix, including mutual L and mutual C
SPDfilename.pkg	IBIS .pkg file
SPDfilename_pin.ibs	IBIS .ibs file
SPDfilename_SPICE.ckt	SPICE PI-model
SPDfilename_SPICE_t.ckt	SPICE T-model
SPDfilename_SegmentR.csv	Segment R for each metal layer
SPDfilename_SegmentL.csv	Segment L for each metal layer
SPDfilename_SegmentC.csv	Segment C for each metal layer

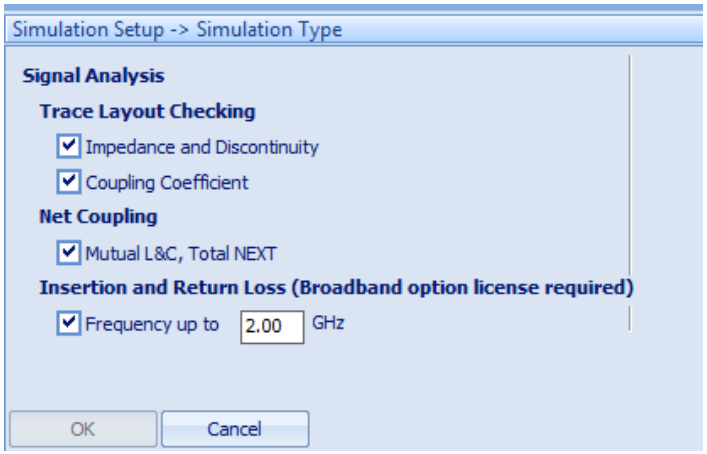
Electrical Performance Assessment

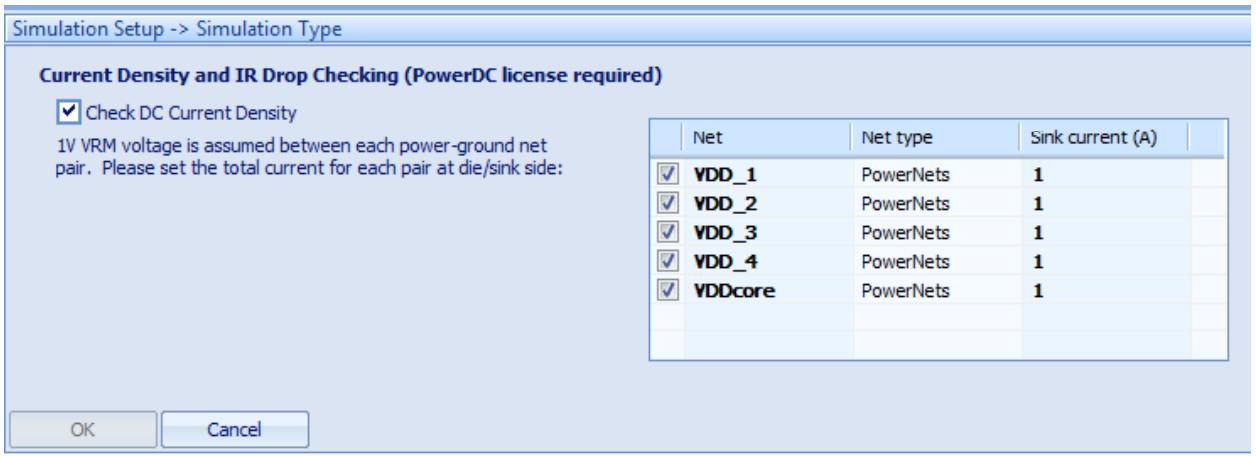
- Power-Ground Analysis



Simulation Report.mht

- Signal Analysis and Current Checking

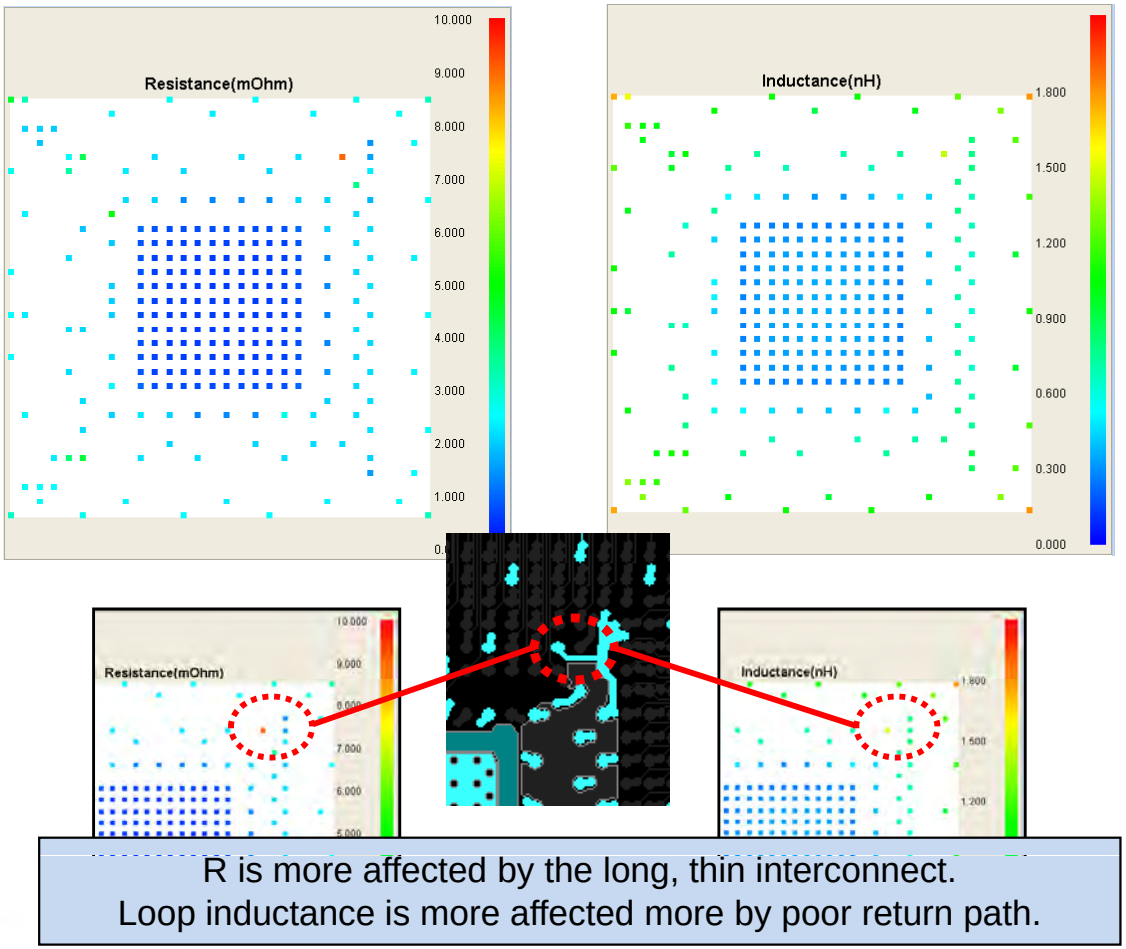




Electrical Performance Assessment

Per-Pin Resistance and Inductance

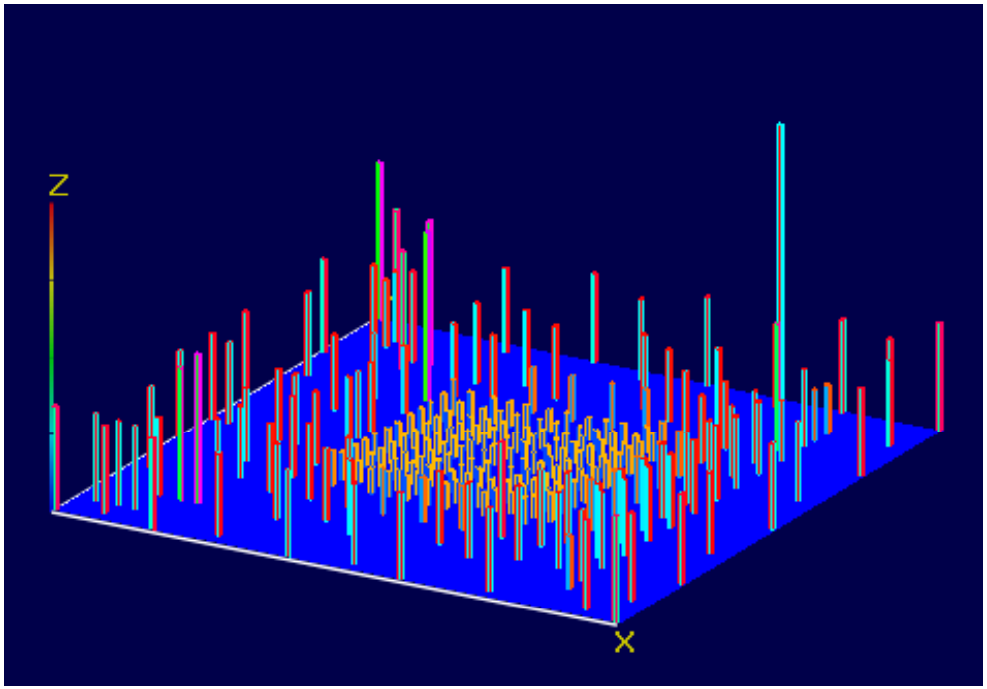
- 2D displays of R and L from the die-side are shown below
  - ‘weak’ pins have higher R and L values and are more **red** than **blue**
  - ‘weak’ pins are rapidly identified with no special expertise required



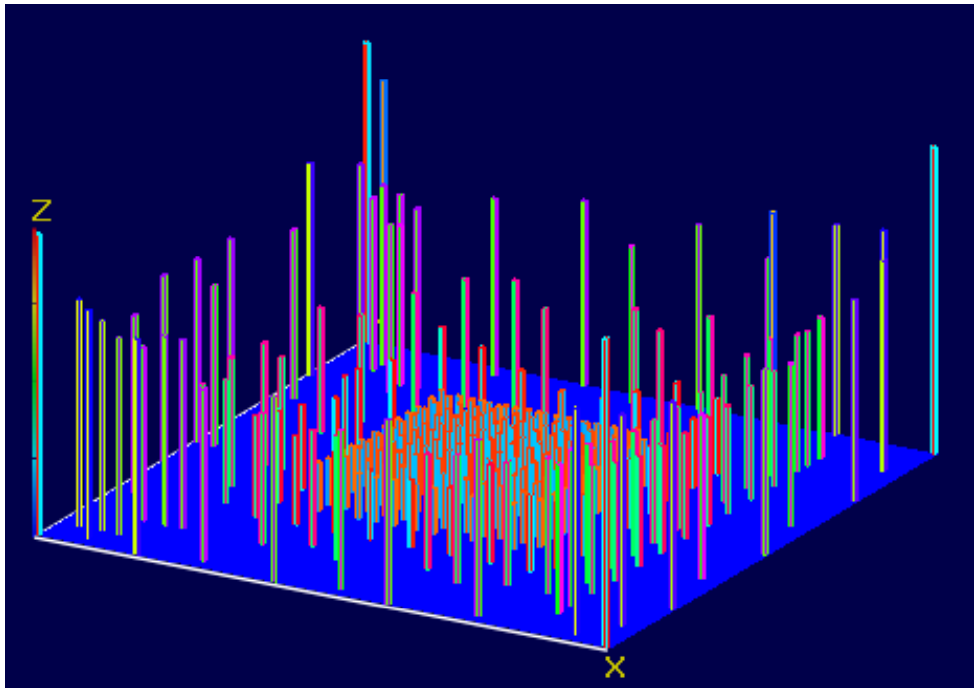
R is more affected by the long, thin interconnect.
Loop inductance is more affected more by poor return path.

Per-Pin Resistance and Inductance Assessment

- 3D displays of R and L are also available
  - helping to intuitively quantify the relative distributions
  - numerical tables are also available



Resistance



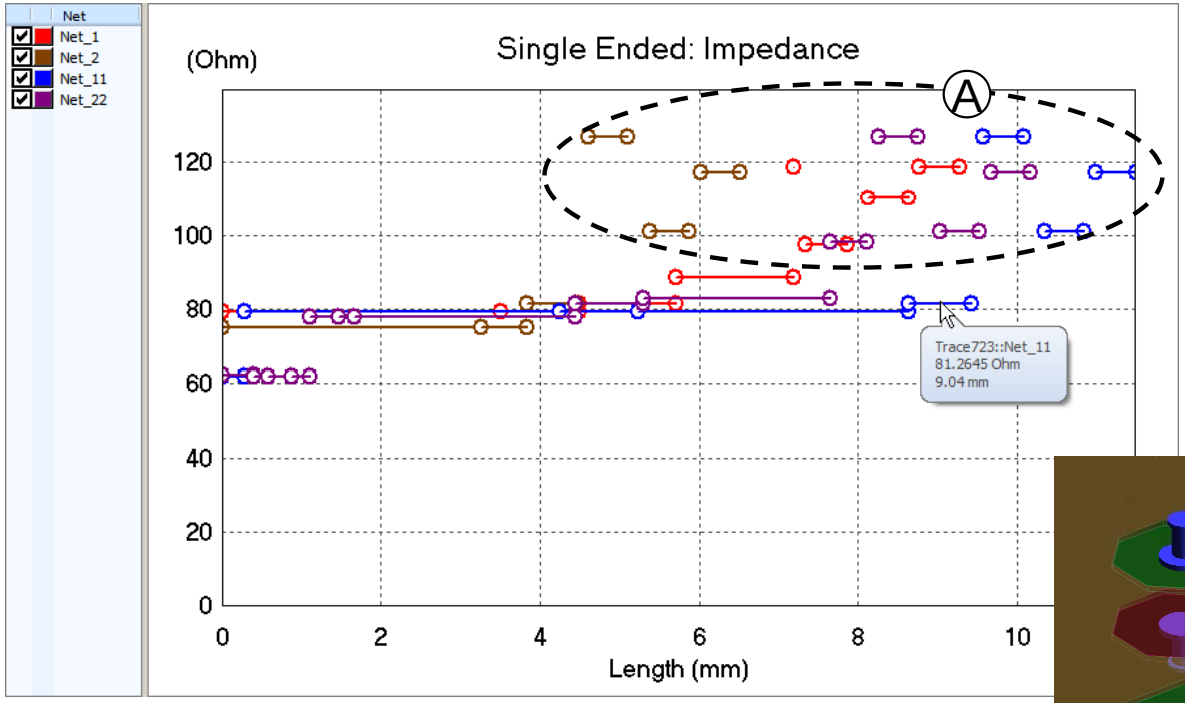
Inductance

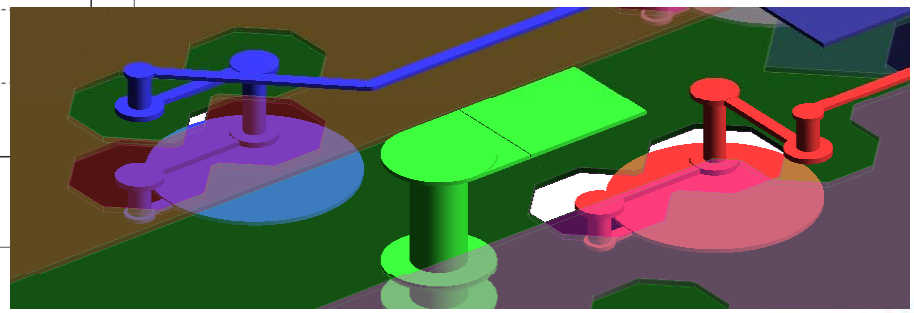
XtractIM

EPA

- Single-ended impedances are displayed along the length of the nets
  - zero length is at die-side
  - trace color is same as net color
  - net, trace segment and impedance are displayed when cursor is positioned on plot

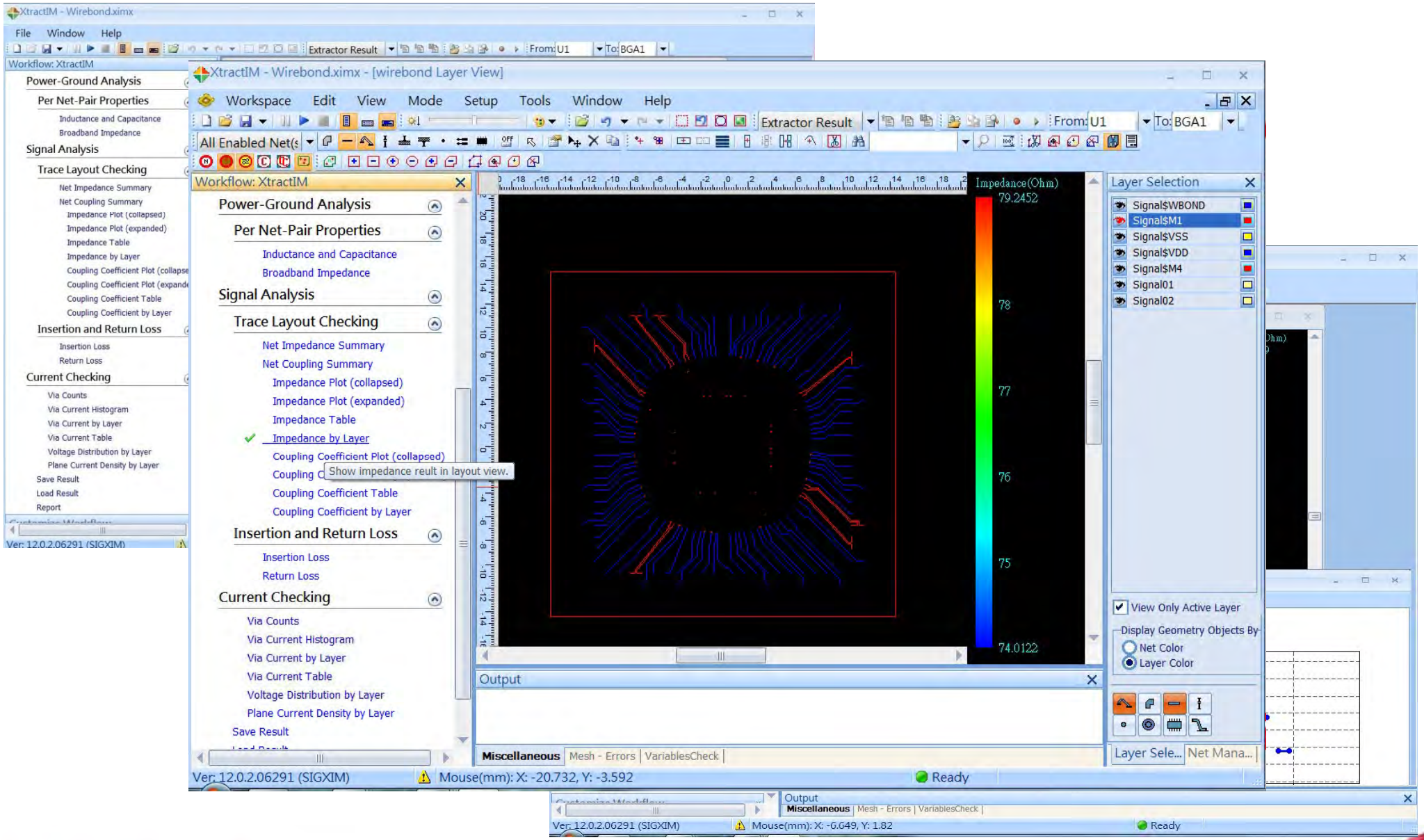
A. potential issue of high impedance at board-side of nets (larger lengths)
   - top-to-bottom layer transition dogleg traces do not have good reference planes





- Quality Check for Package Design

EPA – Impedance Plot

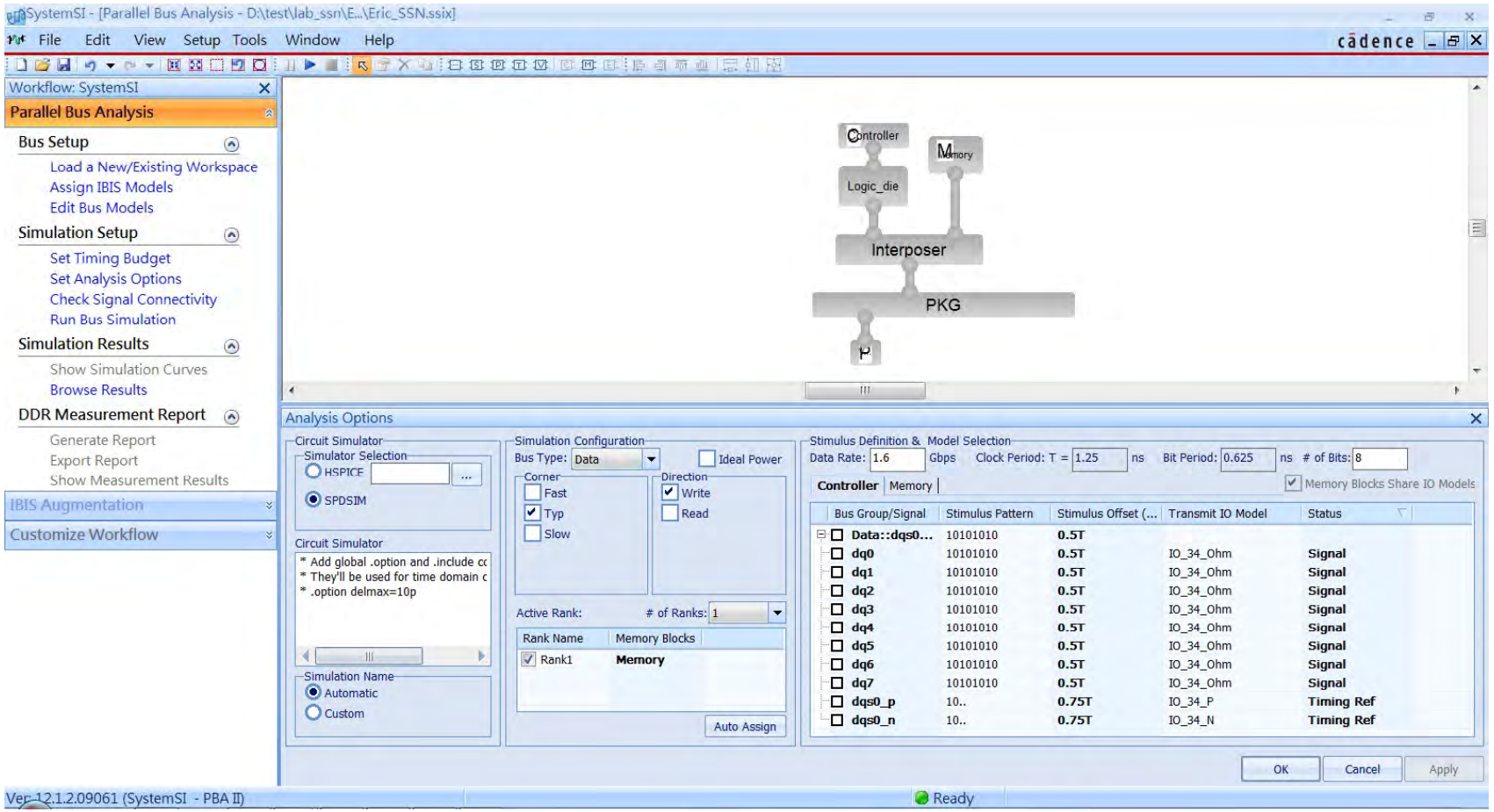


Benefits and Observations

- XtractIM ➔
  generates, displays and exports standard electrical models for IC packages
  - Extended model support
    - High level assessment of package performance.
    - Support of system-level SI and PI analysis.
    - Both net-base and pin-based models.
  - Extraction display support
    - Electrical DRC sign-off and debugging.
- XtractIM ➔
  Electrical Performance Assessment
  - quickly identifies potential power and signal delivery issues
  - quantifies issues intuitively and numerically
    - documents potential issues for colleagues or management
  - helps identify physical root cause of issues and visualize design changes to address them
- XtractIM automates otherwise tedious analysis setup and results post-processing to quickly assess package electrical performance

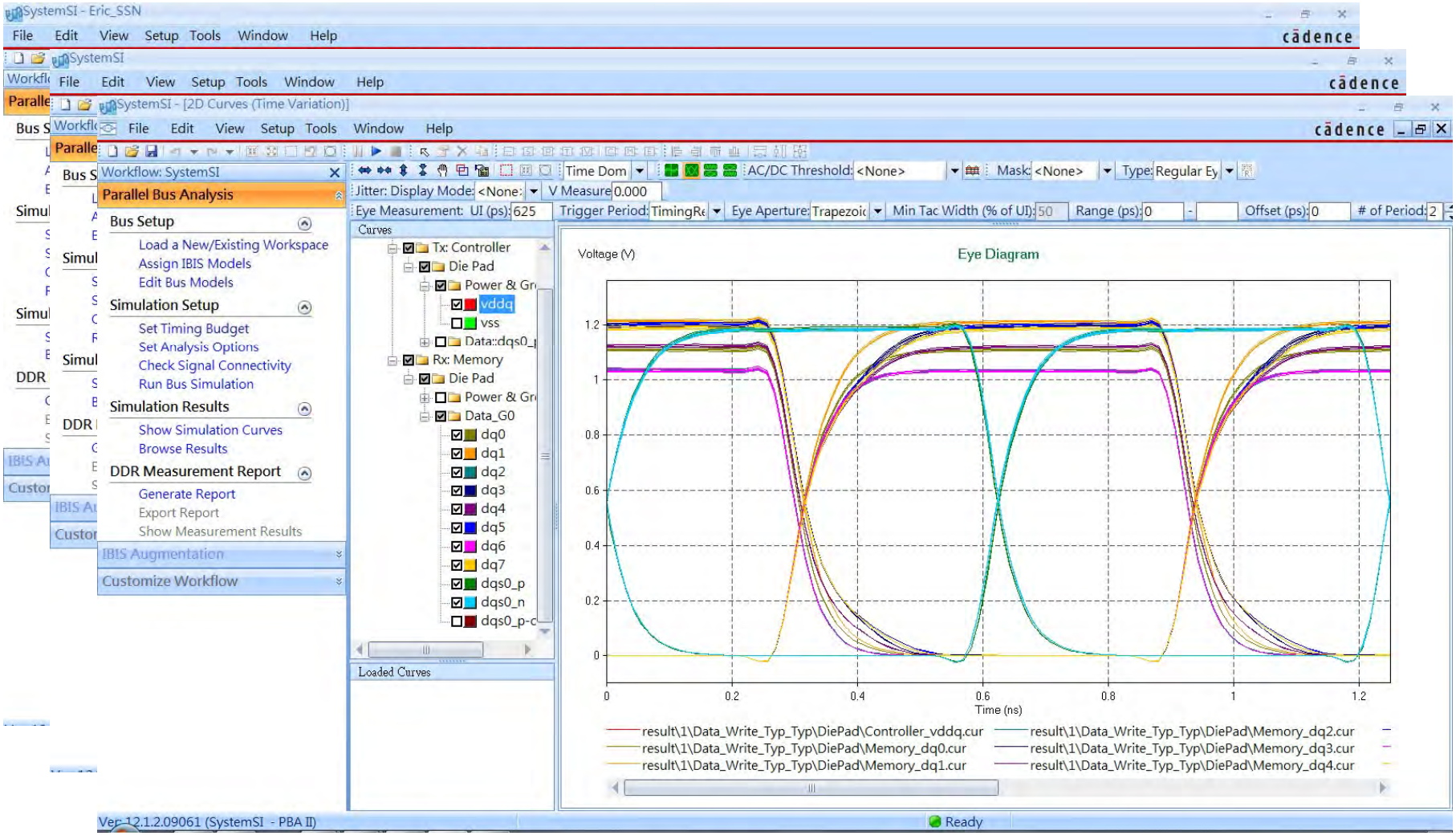
System Simulation by SystemSI
SystemSI – Chip-to-Chip Signal Integrity Analysis

SystemSI PBA – Parallel Bus Analysis

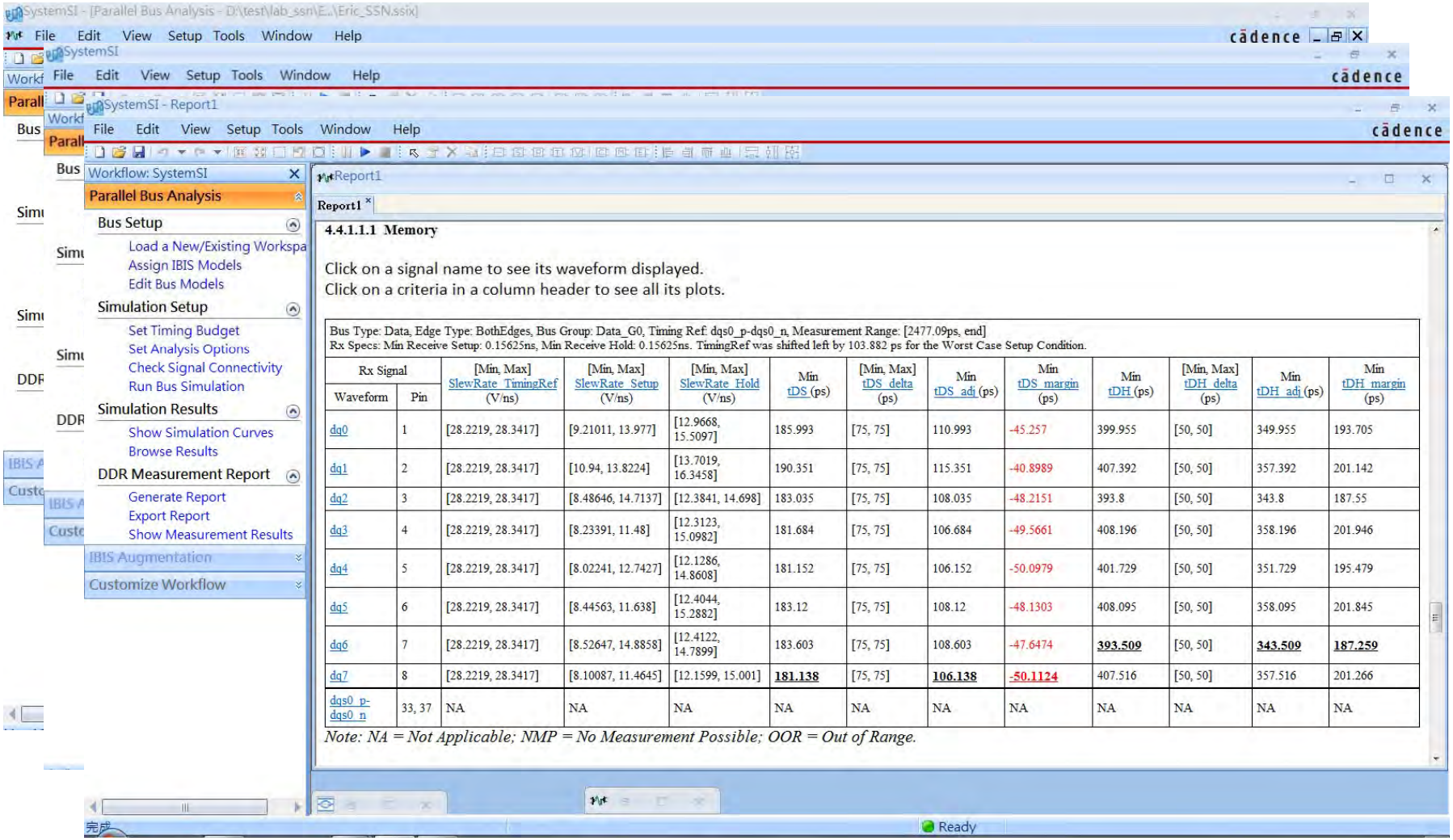


- Blocked based topology editor with SPICE sub-circuits modeling approach
- I/O modeling flexibility for power-aware IBIS and transistor level circuits

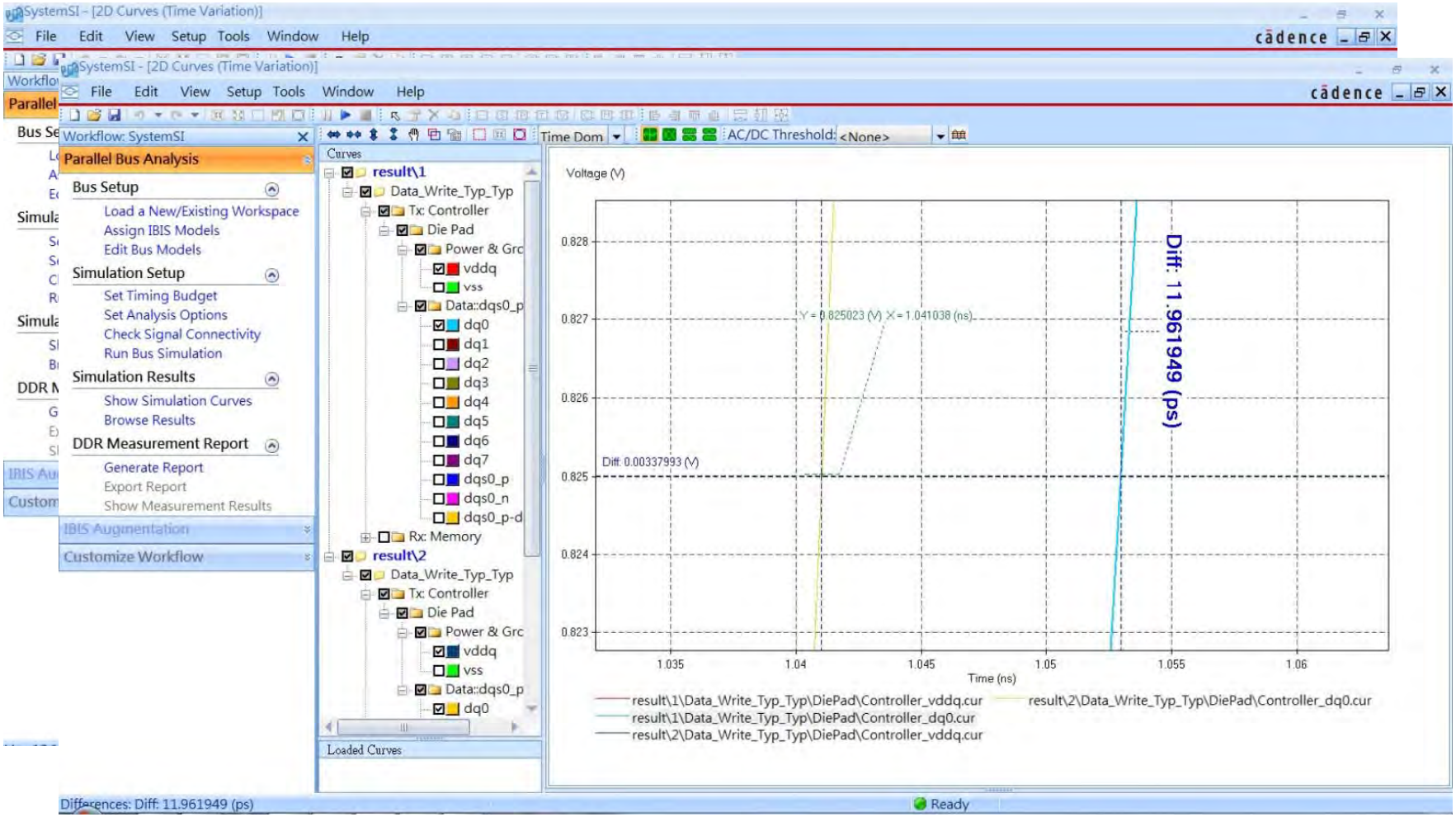
SystemSI PBA – View Waveform & Eye



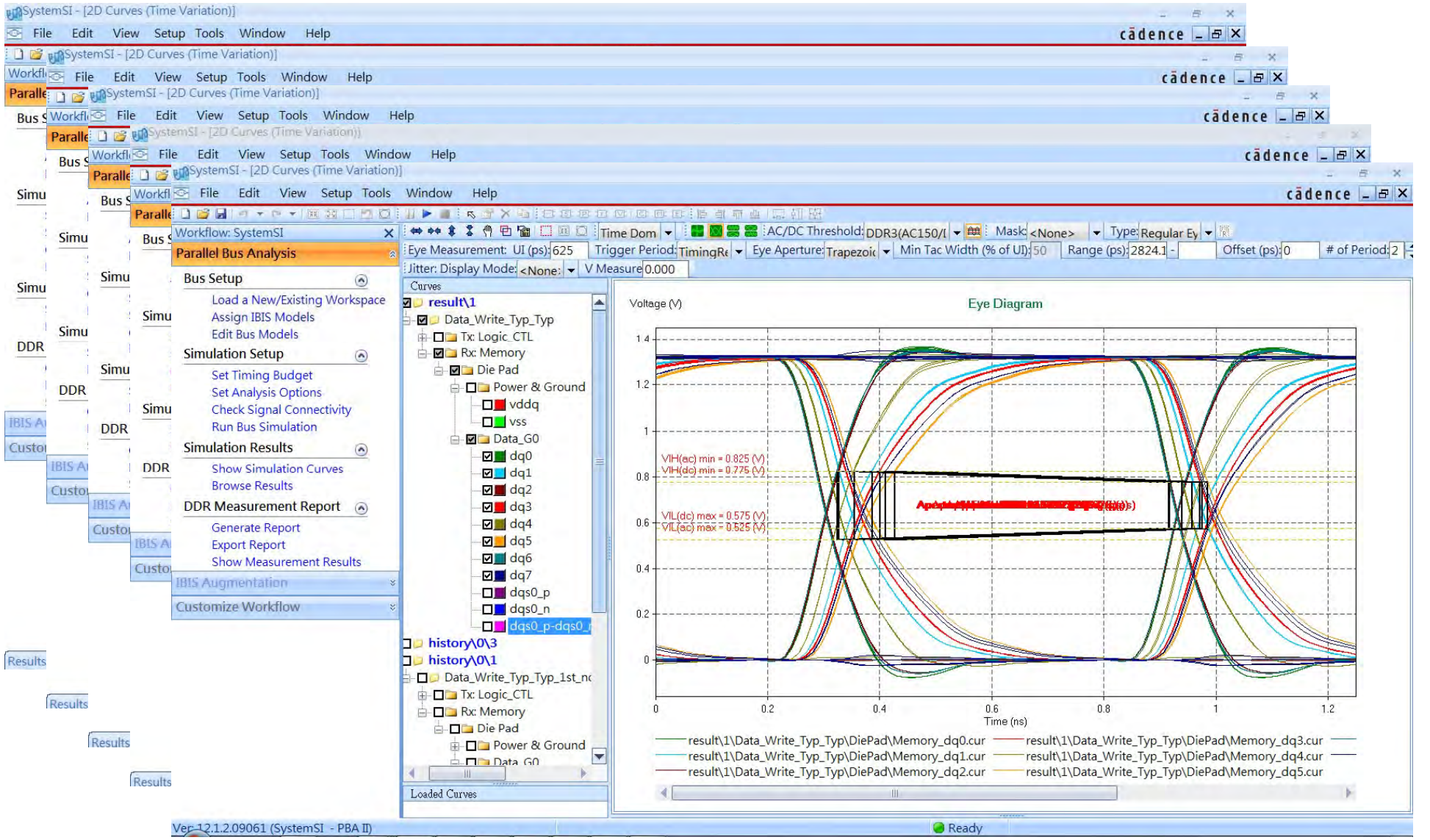
SystemSI PBA – Report Generator



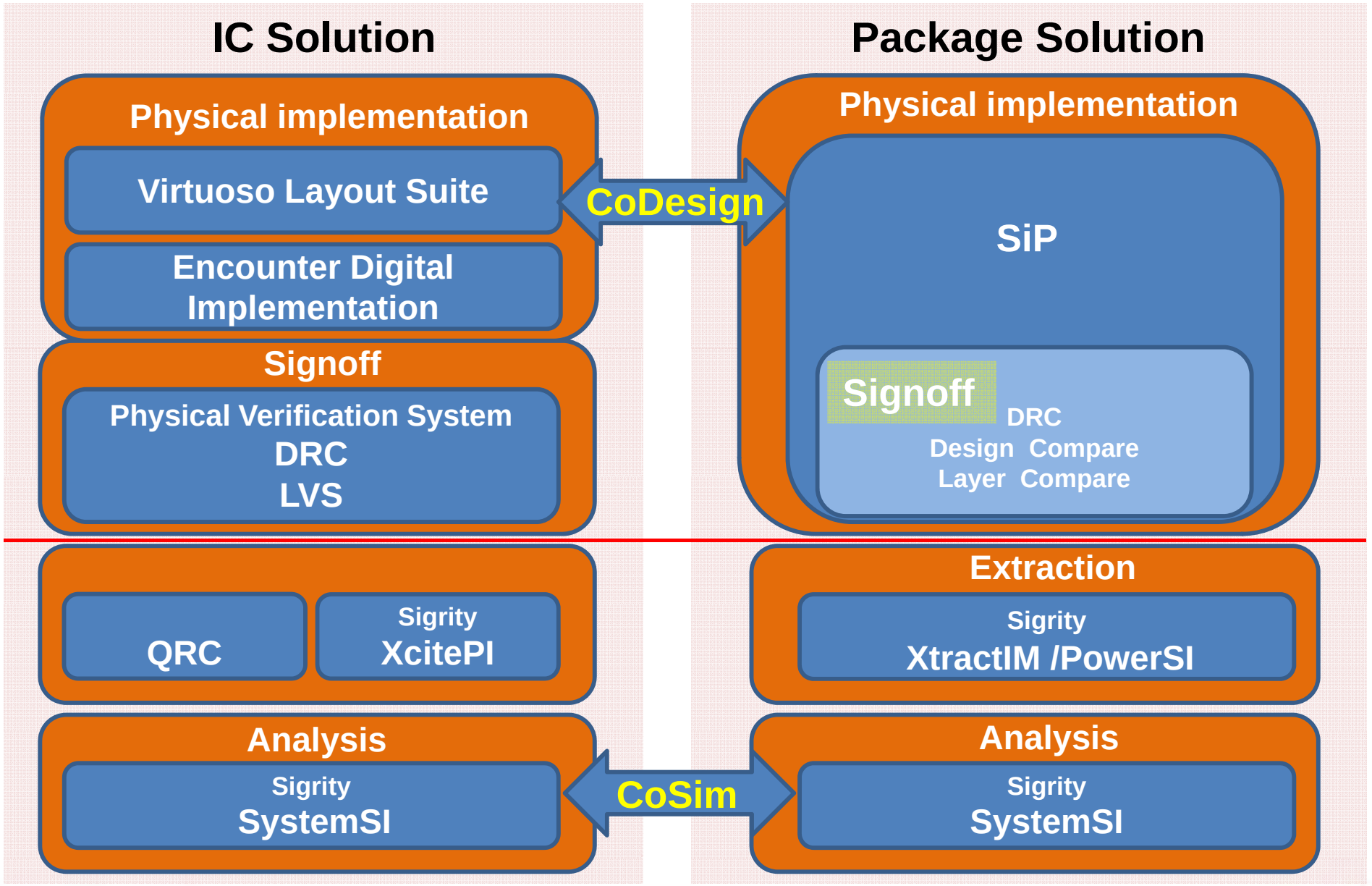
SystemSI PBA – Ideal vs Non-Ideal Power



SystemSI PBA – What if Analysis



Summary



Thanks !!!