

快速 2014 SPB Seminar  
模擬驗證完善  
設計規範  
SIGNAL AND POWER INTEGRITY

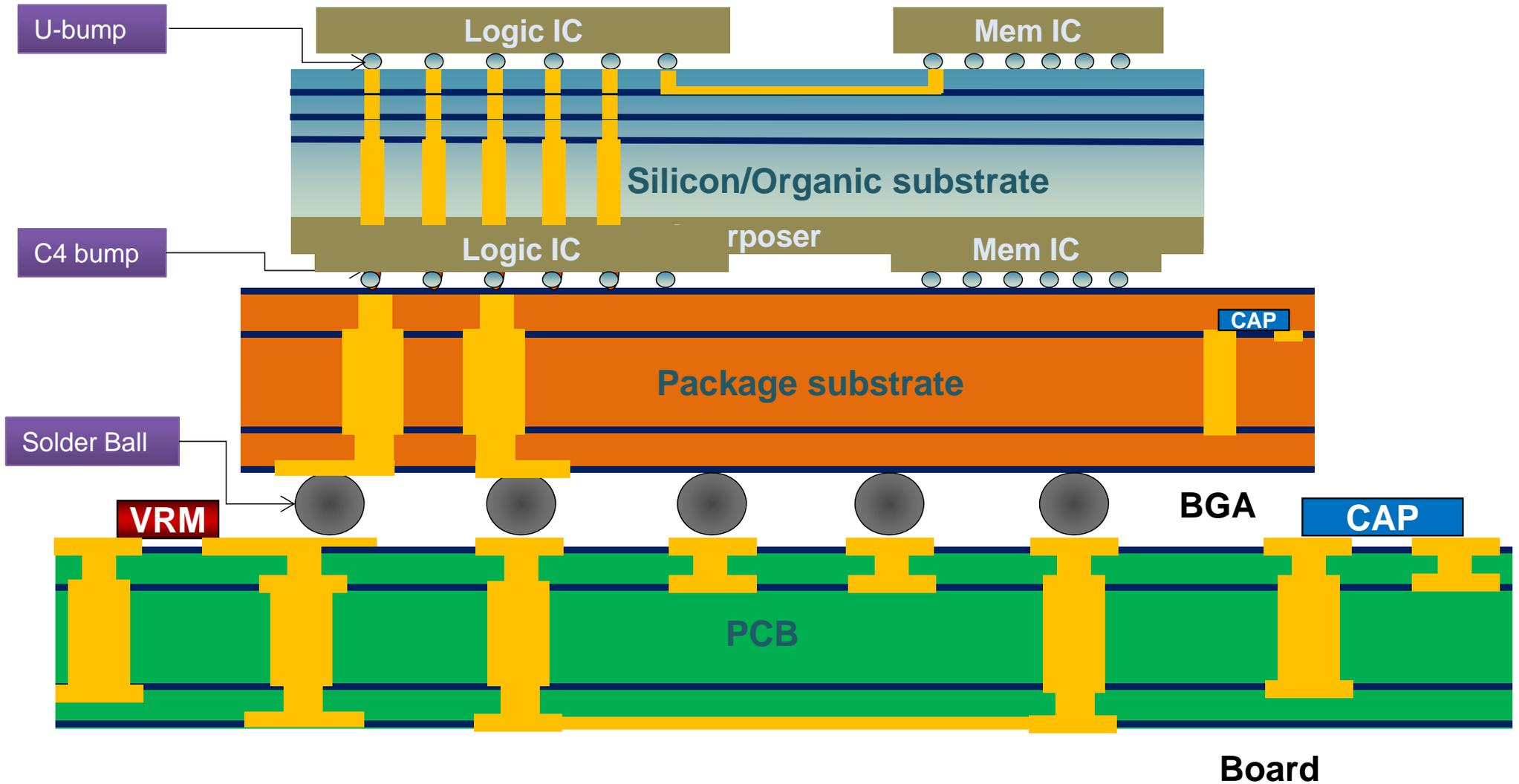
# Si-Interposer Collaboration in IC/PKG/SI

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*4/Jul/2014*

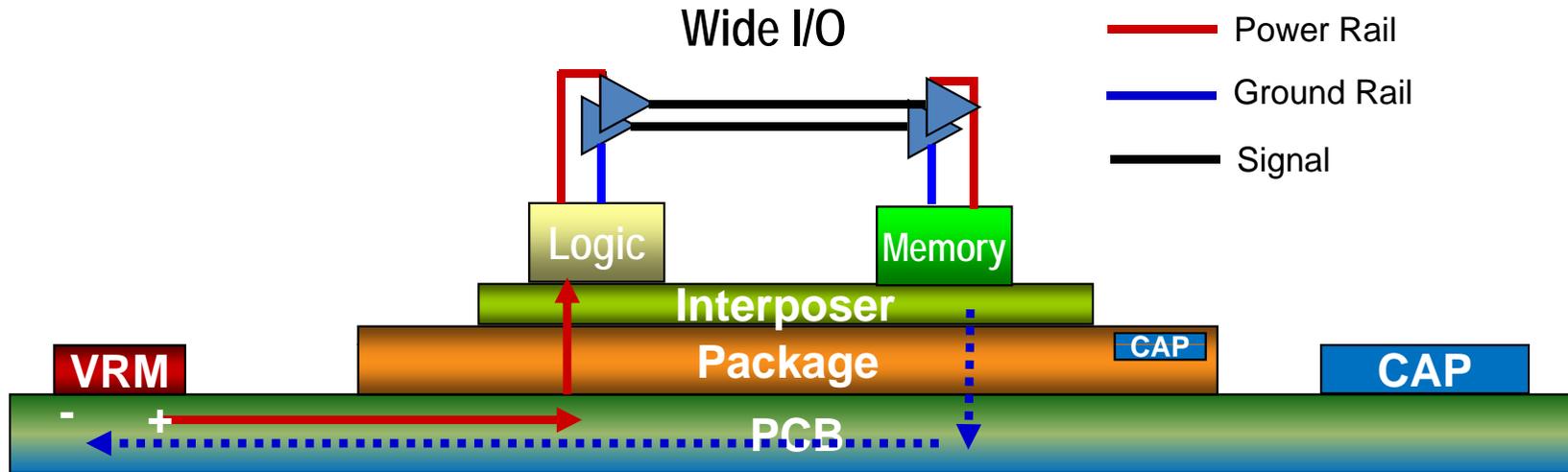
**Graser**<sup>®</sup>

# Design Overview



# System Architecture

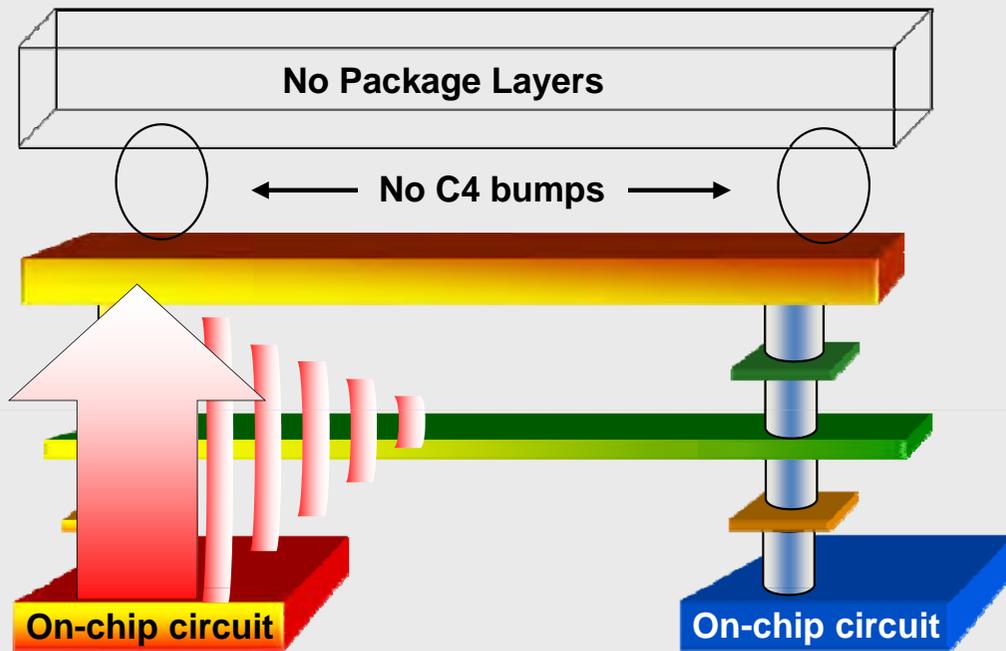
from electrical characteristic perspective



- The system power is supplied by voltage regulation module (VRM) on PCB
- Multiple power delivery path from VRM, decaps on PCB, parasitic of capacitance from chip, package and PCB to fulfill different current demand by wide I/O circuits in different frequency bandwidth
- Signal waveform from output buffer is generated by current sink of I/O circuit from the PDN system

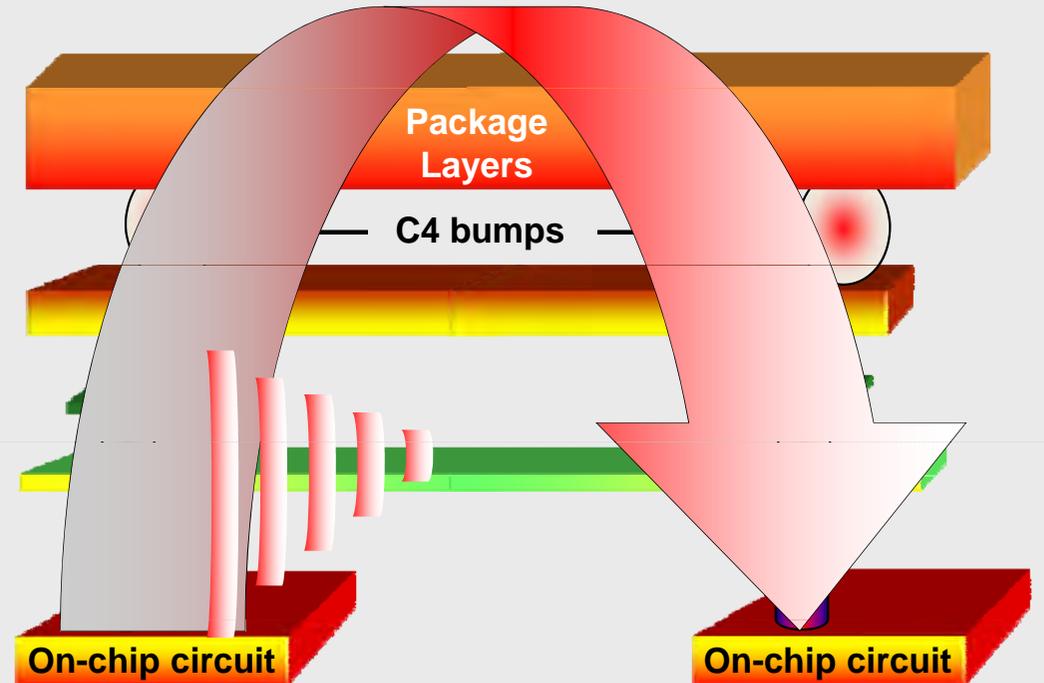


# Why does Chip-System Co-Design?



## Chip

Highly resistive / High-loss system  
Results in localized voltage noise effects



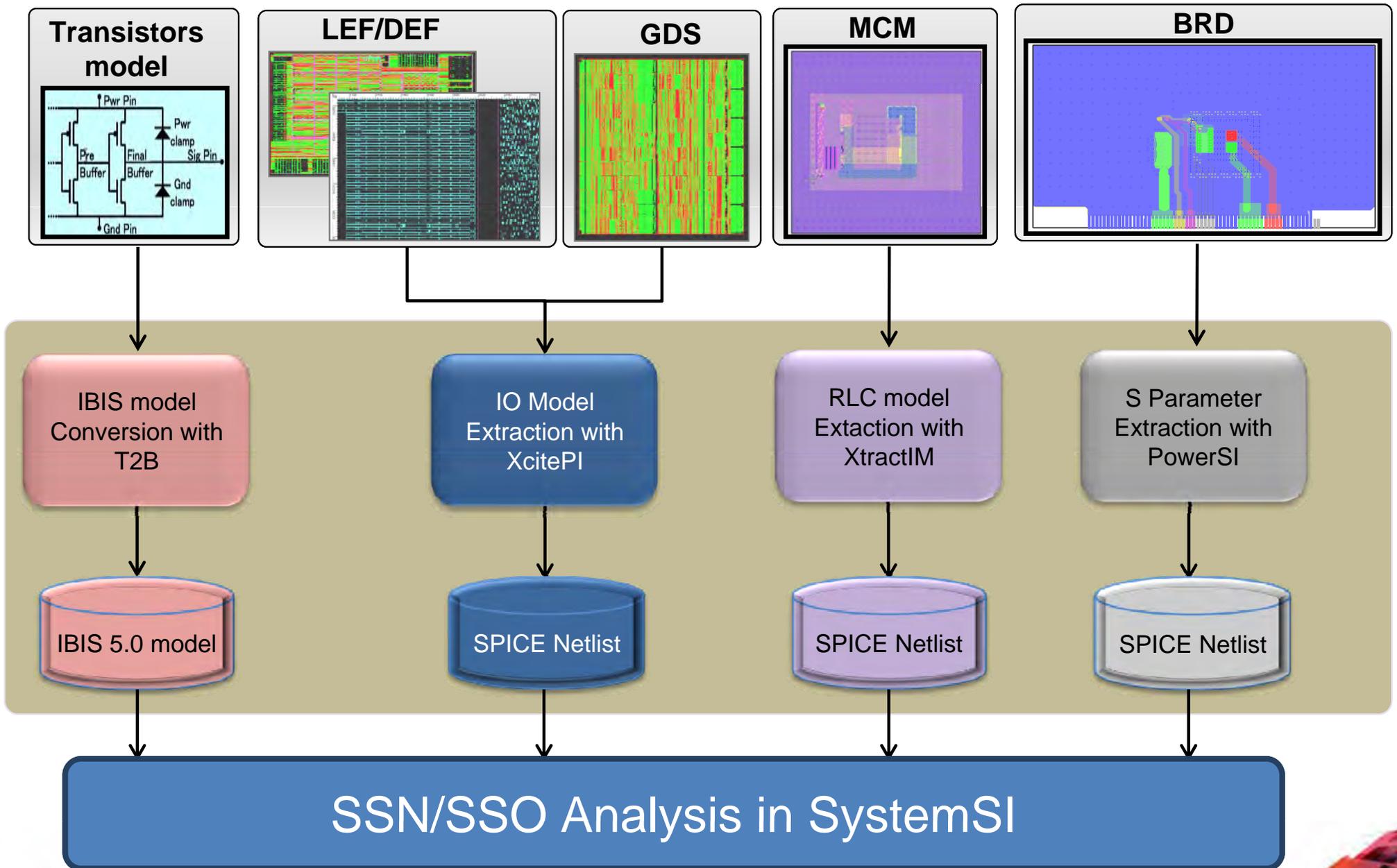
## Package

Low impedance / Low-loss system  
Results in global voltage noise effects to other IC circuits

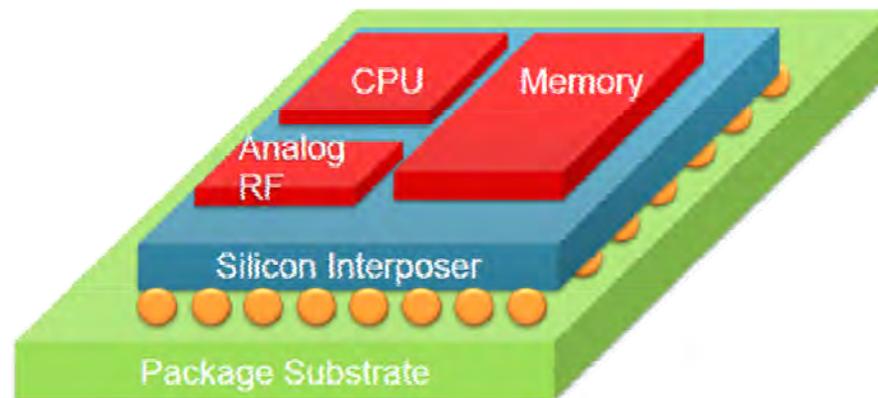
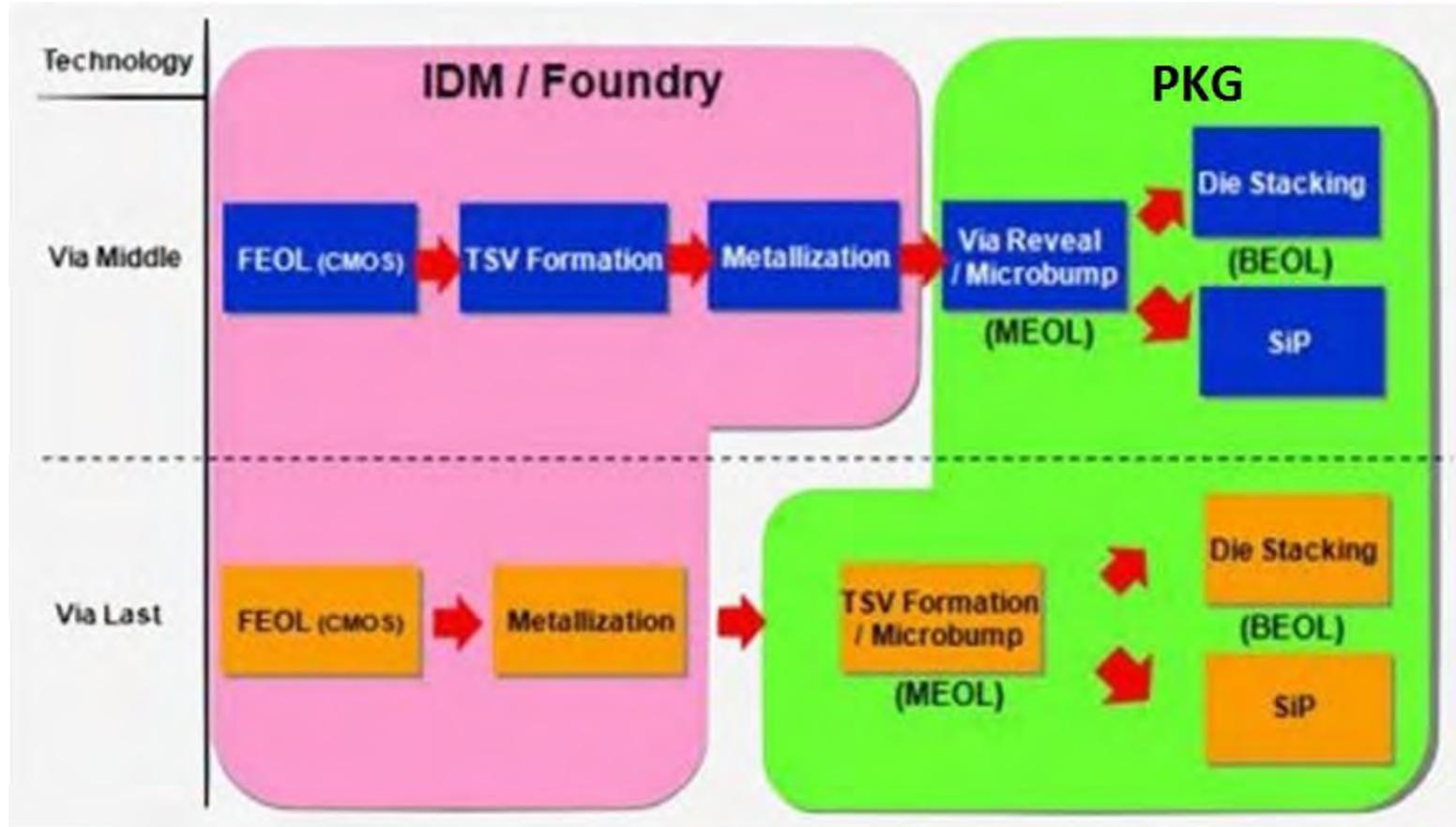
**The low-loss power distribution system of the package easily transfers voltage noise effects to other on-chip circuits**



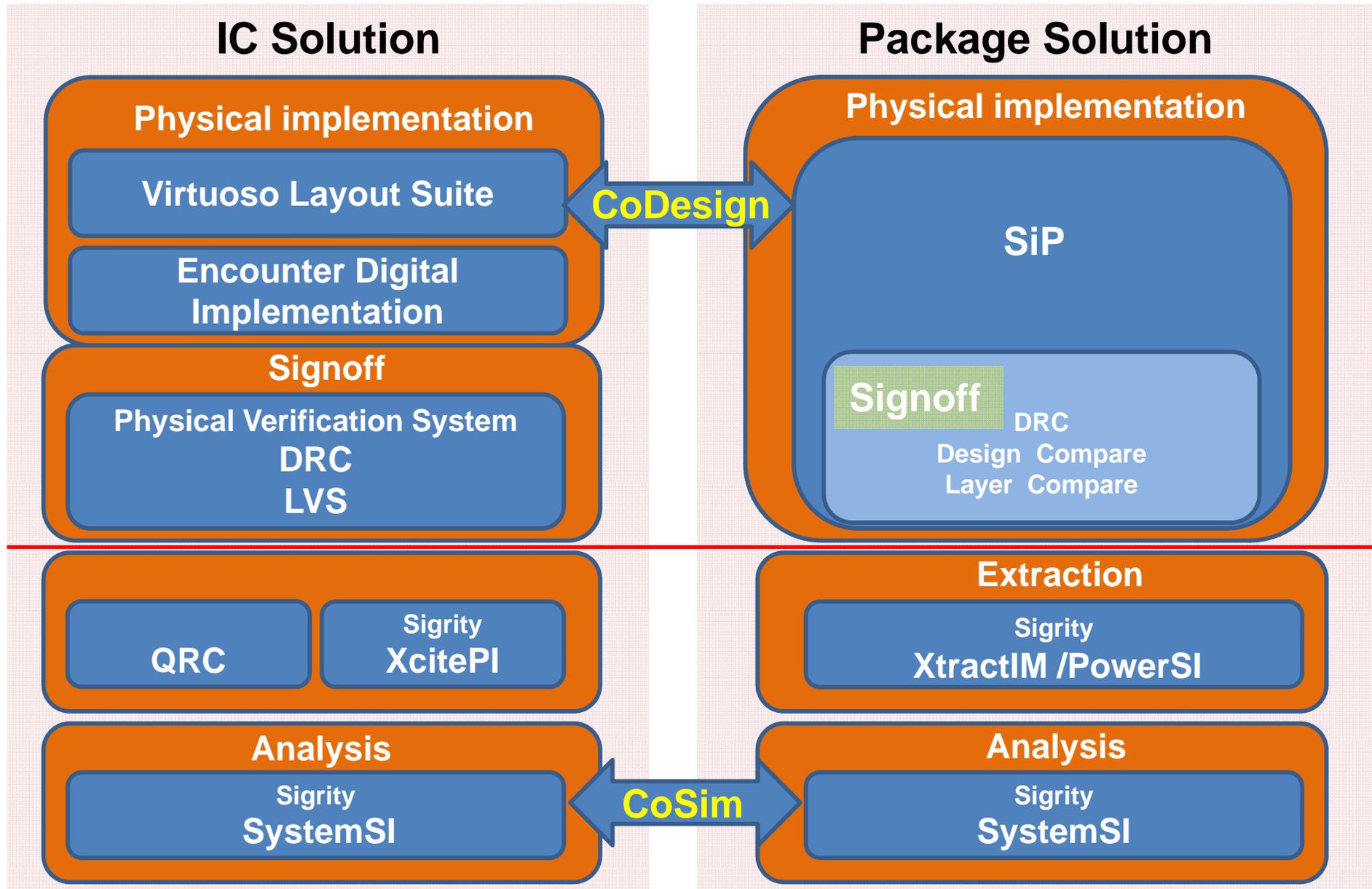
# SSO/SSN Analysis with Cadence Sigrity



# Si-Interposer in IC/SiP



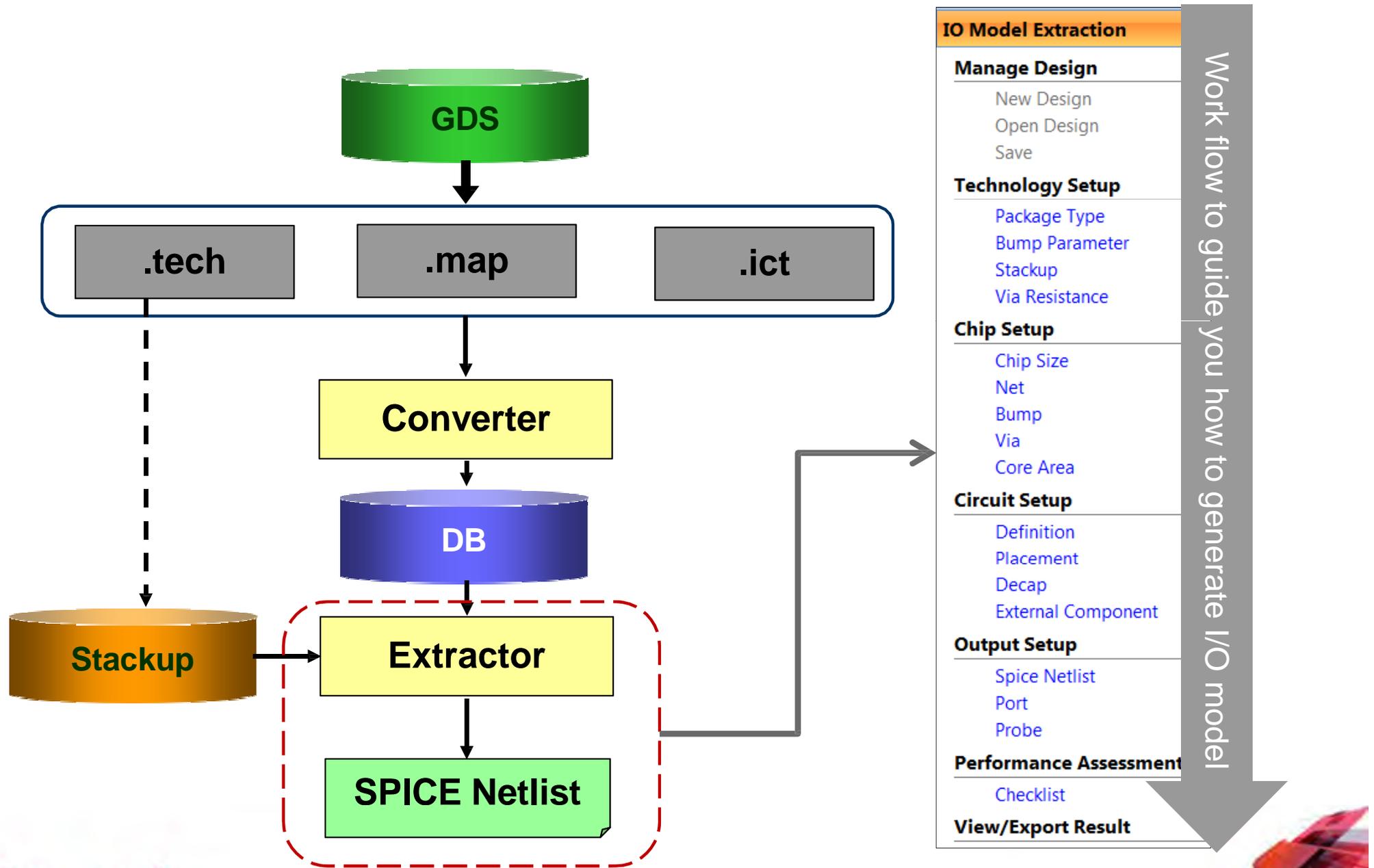
# CoDesign/CoSim by IC/PKG/Sigrity



# IC-oriented Interposer Model Extraction XcitePI – IO Model Extraction



# I/O Model Extraction with XcitePI-IOME



# XcitePI - IOME

The screenshot displays the XcitePI software interface for IO Model Extraction Setup. The main window shows a layout view with components labeled 'ram1', 'package', and 'ram2'. A table titled 'External Component' is open, showing the following data:

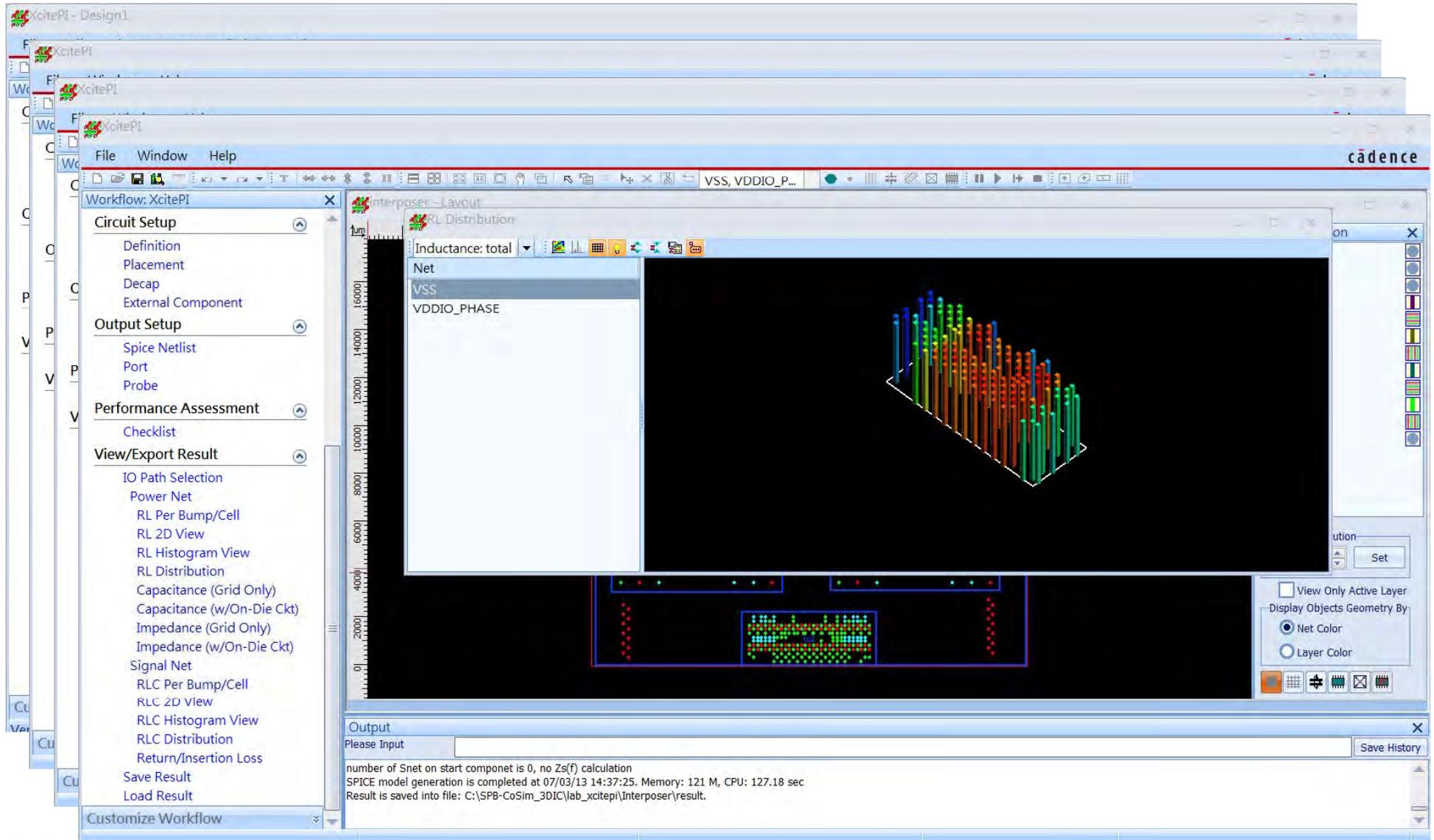
Name	Layer	llx (um)	lly (um)	urx (um)	ury (um)
ram1	bump	849.339130	3031.543478	8125.043478	15871.021739
ram2	bump	10086.630435	3102.873913	17255.339130	15871.021739
tc2	bump	6341.782609	0.000000	12048.217391	2246.908696
package	TSVBump	171.700000	0.000000	18360.960870	16370.334783

The interface also includes a 'Layer Selection' panel on the right with options like TSVBump, metalb, TSV, FOX, metal1, VIA1, metal2, VIA2, metal3, VIA3, metal4, and bump. The 'External Component' dialog has buttons for New, Delete, Edit Module, UnLoad, Report, OK, Cancel, and Apply.

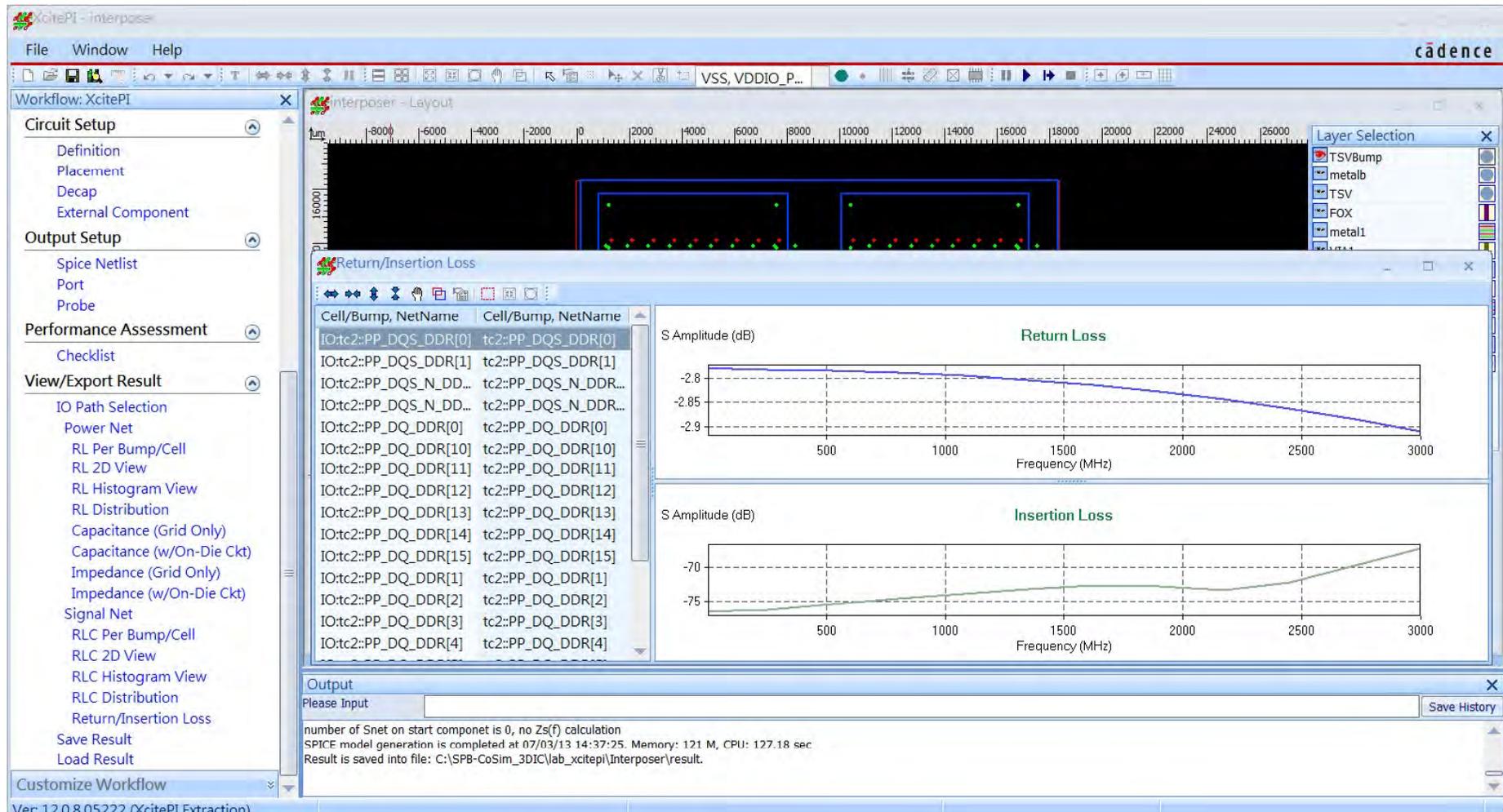


# XcitePI - IOME

- EPA



# XcitePI - IOME



# XcitePI - IOME

- Model extraction

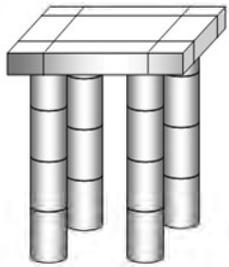
The screenshot displays the XcitePI software interface, which is used for model extraction. The main window shows a layout view of a chip model with two rectangular regions highlighted in blue. The interface includes a menu bar (File, Edit, View, Feature, Window, Help) and a toolbar. On the left, there is a 'Workflow: XcitePI' panel with sections for 'Circuit Setup', 'Output Setup', 'Performance Assessment', and 'View/Export Result'. The 'View/Export Result' section is expanded, showing options for 'IO Path Selection', 'Power Net', 'Signal Net', and 'Save Result'. In the foreground, two UltraEdit-32 windows are open, displaying the extracted model files. The left window shows the file 'interposer.sp' and the right window shows 'interposer\_RLCK.sp'. Both files contain a compact double mesh (CDM) chip model generated by XcitePI (V12.0.8) on 07/03/13. The files list various components and their connections, such as bump connections to VSS and VDDIO\_PHASE.

```
1 * Compact double mesh (CDM) chip model -- generated by XcitePI (V12.0.8)
2 * Created time is at 07/03/13 14:35:18.
3 * Design Name is interposer.
4
5 .SUBCKT interposer
6 + bump69_VSS bump81_VSS bump99_VSS
7 + bump110_VSS bump122_VSS bump132_VSS bump154_VSS
8 + bump162_VSS bump175_VSS bump187_VSS bump217_VSS
9 + bump38_VSS bump75_VSS bump93_VSS bump103_VSS
10 + bump117_VSS bump129_VSS bump153_VSS bump155_VSS
11 + bump169_VSS bump177_VSS bump202_VSS bump225_VSS
12 + bump230_VSS bump43_VSS bump69_VSS bump82_VSS
13 + bump100_VSS bump111_VSS bump123_VSS bump133_VSS
14 + bump137_VSS bump163_VSS bump176_VSS bump196_VSS
15 + bump44_VDDIO_PHASE bump46_VSS bump48_VDDIO_PHASE
16 + bump53_VSS bump57_VDDIO_PHASE bump64_VSS
```



# Published TSV Circuit Modeling

A single TSV



Multiple TSV extracted together

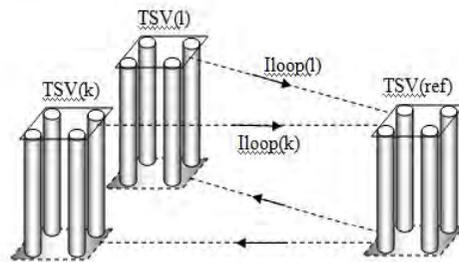
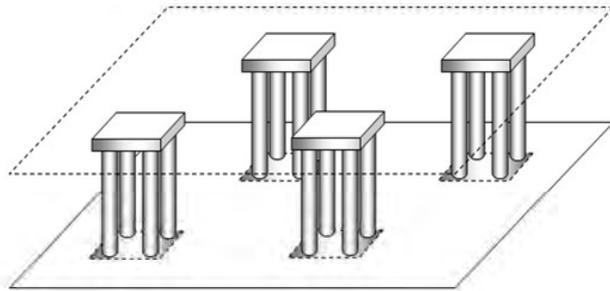


Fig. 12 The loop inductance of TSVs

Level 0: DC circuit, only contained $R_{via}$ , used for IR drop analysis or connection testing.	
Level 1: Simple RLC model Have PG loop inductance, capacitance to the substrate, no via-via coupling	
Level 2: Pin based circuit model. Have the L matrix and C matrix based on each TSV branches.	
Level 5: user defined TSV model	

## About TSV modeling:

- We didn't calculate each via's partial inductance and mutual inductance. If we do so, that will form a huge circuit matrix that can't be simulated in HSPICE
- We adopt loop calculation. For example, we have  $n$  vias, then we have  $(n-1)$  loop, then we calculate  $(n-1)$  loop and consider coupling between loops. But loop coupling will decay very fast, then final circuit matrix will be small.



# Published TSV Circuit Modeling

The screenshot displays the Cadence XcitePI-Interposer software interface. The main window shows a layout view with a grid and two highlighted rectangular areas containing TSV bump patterns. A 'Layer Selection' panel on the right lists layers: TSVBump, metalb, TSV, FOX, metal1, VIA1, and metal2. An 'UltraEdit-32' window titled '文字比較 - UltraCompare Lite' is open in the foreground, comparing two files: 'C:\ASPB-CoSim\_3DIC\lab\_xcitepi\interposer\interposer\_RLCK.sp' and 'C:\ASPB-CoSim\_3DIC\lab\_xcitepi\interposer\interposerXPI\_TSV\_LVL2\_RLCK.sp'. The comparison shows a list of components and their values, such as 'Cvia105 TSVB105 ref 1.942546e-013' and 'Cox\_via105 NSIL105 N\_428 1.942546e-013'.

Line	Component	Value
2480	Cvia105 TSVB105 ref	1.942546e-013
2481	Cvia106 TSVB106 ref	1.942546e-013
2482	Cvia107 TSVB107 ref	1.942546e-013
2483	Cvia108 TSVB108 ref	1.942546e-013
2484	Cvia109 TSVB109 ref	1.942546e-013
2485	Cvia110 TSVB110 ref	1.942546e-013
2486	Cvia111 TSVB111 ref	1.942546e-013
2480	Cox_via105 NSIL105 N_428	1.942546e-013
2481	Cox_via106 NSIL106 N_446	1.942546e-013
2482	Cox_via107 NSIL107 N_448	1.942546e-013
2483	Cox_via108 NSIL108 N_466	1.942546e-013
2484	Cox_via109 NSIL109 N_468	1.942546e-013
2485	Cox_via110 NSIL110 N_546	1.942546e-013
2486	Cox_via111 NSIL111 N_548	1.942546e-013
2487	Csil0 NSIL0 ref	2.791895e-014
2488	Rsil0 NSIL0 ref	3.144962e+006
2489	Csil1 NSIL1 ref	2.791895e-014
2490	Rsil1 NSIL1 ref	3.144962e+006
2491	Csil2 NSIL2 ref	2.791895e-014
2492	Rsil2 NSIL2 ref	3.144962e+006
2493	Csil3 NSIL3 ref	2.791895e-014
2494	Rsil3 NSIL3 ref	3.144962e+006
2495	Csil4 NSIL4 ref	2.791895e-014
2496	Rsil4 NSIL4 ref	3.144962e+006
2497	Csil5 NSIL5 ref	2.791895e-014
2498	Rsil5 NSIL5 ref	3.144962e+006
2499	Csil6 NSIL6 ref	2.791895e-014
2500	Rsil6 NSIL6 ref	3.144962e+006



# PKG-oriented Interposer Model Extraction **XtractIM – EPA & Model Extraction**



# Model Extract

Workflow: XtractIM

**Default**

**Manage Workspace**

- Load Workspace
- Load a New/Different Layout

**Package Setup**

- Package Type: Flip-Chip
- ✓ Circuits
- ✓ Stackup
- ✓ Bumps
- ✓ Solder Ball
- ✓ Nets

**Simulation Setup**

- Module: IBIS/RLGC
- Simulation Type: Net-Based

**View/Export Results**

- Summary
- SPICE/IBIS Model
- RLC Per Net
- RLC Distributions
- Segment RLC
- RLC vs. Net Length
- Save Results
- Load Results

**Package Setup -> Package Type**

- Single Die **1**
- Stacked Die
- Side-by-side Die
- Single BGA
- Stacked BGA
- Leadframe
- Wirebond
- Flip-Chip
- Both

**Stackup**

Layer Icon	Layer Name	Thickness...	Conductivity(...)	Color	Trace Width...	Shape Name
	Signal02	5.0000e-003	5.000000e+007		1.0000e-001	
	Bump01	1.0000e-001				
	Signal\$M1	1.5000e-002	5.800000e+007		1.0000e-001	
	Medium...	1.2500e-001				
	Signal\$VSS	2.0000e-002	5.800000e+007		1.0000e-001	Shape\$VSS
	Medium...	2.5000e-001				

**Net List**

- ✓ Unnamed Net(s)
- ✓ PowerNets
  - ✓ VDD\_1
  - ✓ VDD\_2
  - ✓ VDD\_3
  - ✓ VDD\_4
  - ✓ VDDcore
- ✓ GroundNets
  - ✓ VSS
- ✓ DIFF\_PAIRS
  - ✓ Net\_10
  - ✓ Net\_11
  - ✓ Net\_18
  - ✓ Net\_20
  - ✓ Net\_22
  - ✓ Net\_26
  - ✓ Net\_27
  - ✓ Net\_29
  - ✓ Net\_34
  - ✓ Net\_39
  - ✓ Net\_43
  - ✓ Net\_46
  - ✓ Net\_47
  - ✓ Net\_49

**Table 1: Component Selection**

Ckt Name	Ckt Model	Die/Board/Com...
U1	FC	Die
BGA1	untitled_p...	Board <b>2</b>
C1	Cap0402	

**Table 2: Bump Parameters**

Layer Name	Circuit Name	Dmax (m...)	D1 (mm)	D2 (mm)	HT (mm)	Conductivity (S/m)
Bump01	U1	0.11673	0.11673	0.11673	0.1	5.8e7

**Table 3: Solder Ball Parameters**

Name	Circuit Name	Dmax (m...)	D1 (mm)	D2 (mm)	HT (mm)	Conductivity (S/m)	Medium Thickness ...
Solderball01	BGA1	0.397115	0.397115	0.397115	0.5	5.8e7	0.05

**Diagram 4: Bump Model**

**Diagram 5: Solder Ball Model**

Select the Die/Component circuit from the list and click Next

**2**

**3**

**4**

**5**

**6**



# Model Extract

**IBIS PKG model**

```
[IBIS Ver] 5.0
[Comment Char] |_char
[file Name] 1Dis_wirebond.pkg
[File Rev] 1.0
[Date] 9/26/2012
[Source] Sigriety SpeedPKG Suite XtractIM Version 12.0.2.06291
[Notes] One-Section RLC
[Disclaimer] The model given below represents a 105-pin package.
[Copyright]
|
|
|
[Define Package Model] ibis_wirebond
[Manufacturer] name 1
[OEM] name 2
[Description] 105-pin Package
|
|[Number of Sections] 1
|[Number of Pins] 105
|
|[Pin Numbers]
|[Pin Name] Net Number Net Name Net's All Pins
BGAI-AA1 | 1 VDD_1 BGAI-AA1
```

Total number of circuit components: R: 105 L: 105 M: 614 C: 364



# Model Extract

The screenshot displays the XtractIM software interface. The main window is titled "XtractIM - Wirebond.ximx - [Circuit Topology Result]". The "Extractor Result" tab is active, showing a circuit diagram of a wirebond package with a DC resistance model. The "View Model Selection" section has "DC Resistance" selected. Below this, a table lists the DC resistance values for various nets.

**DC Resistance**

NetName	DC R(Ohm)
Power Nets	
VDD_1	
VDD_2	
VDD_3	
VDD_4	
VDDcore	
Signal Nets	
Net_1	0.244855
Net_2	0.233824
Net_3	0.235719
Net_4	0.247221
Net_5	0.265694
Net_6	0.249484
Net_7	0.241292
Net_8	0.235215
Net_9	0.228548
Net_10	0.223482
Net_11	0.219789
Net_12	0.216342
Net_13	0.213589
Net_14	0.210825
Net_15	0.206887



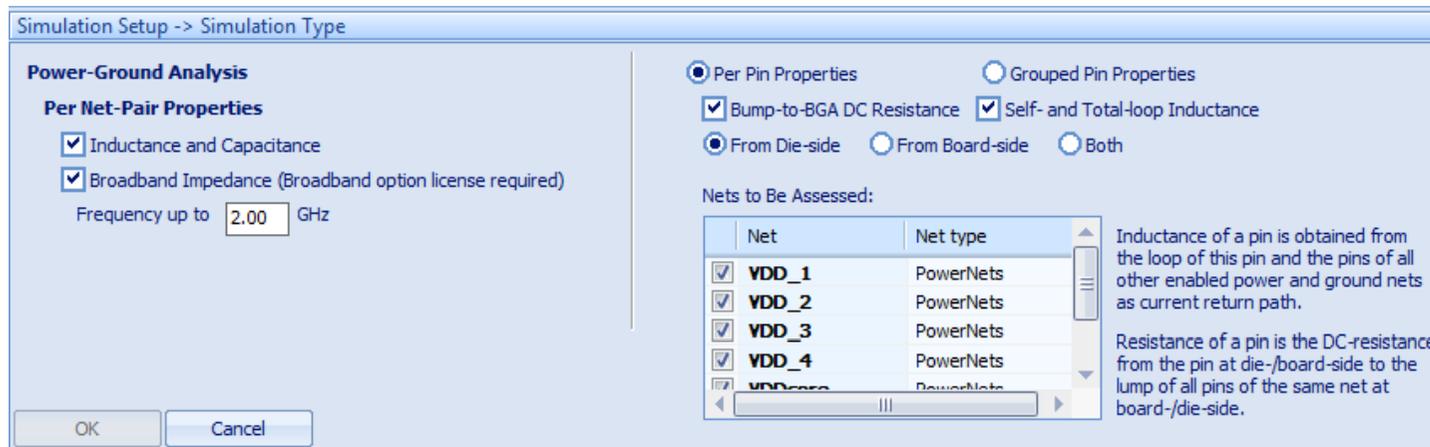
# Resource and Result Overview

ResourceProfile_Extractor.log	Resource log file
ExtractorRunTimeError.log	Error log file
Un_Xtracted_NetName.log	log file to tell what nets are open nets and not be extracted.
SPDfilename_PinModel.csv	List pin, net name, net-length, R,L,C, and Delay for Power and Signal nets
SPDfilename_DCResistance.csv	List net name, DC R for Power, Signal, Ground net
SPDfilename_TableContent.csv	Full RLC matrix, including mutual L and mutual C
SPDfilename.pkg	IBIS .pkg file
SPDfilename_pin.ibs	IBIS .ibs file
SPDfilename_SPICE.ckt	SPICE PI-model
SPDfilename_SPICE_t.ckt	SPICE T-model
SPDfilename_SegmentR.csv	Segment R for each metal layer
SPDfilename_SegmentL.csv	Segment L for each metal layer
SPDfilename_SegmentC.csv	Segment C for each metal layer



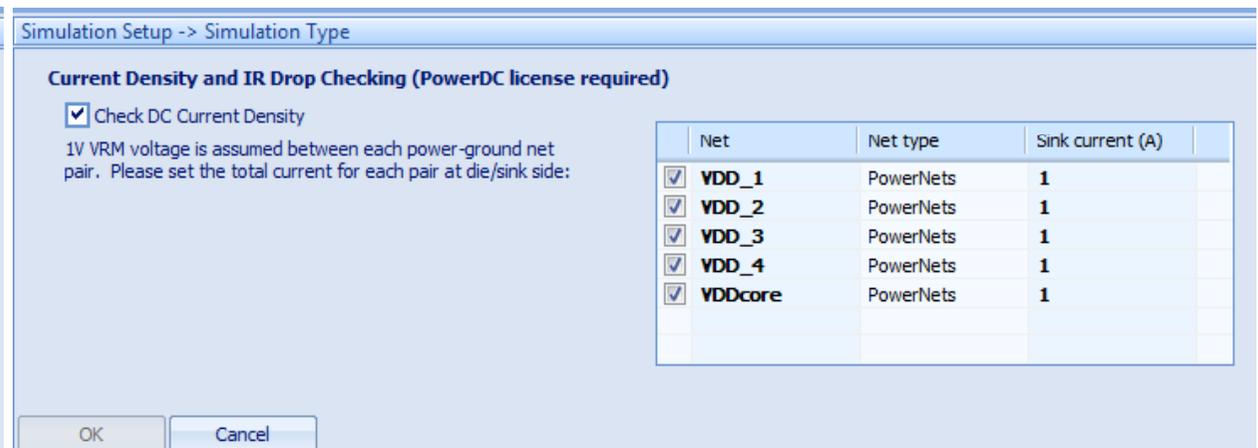
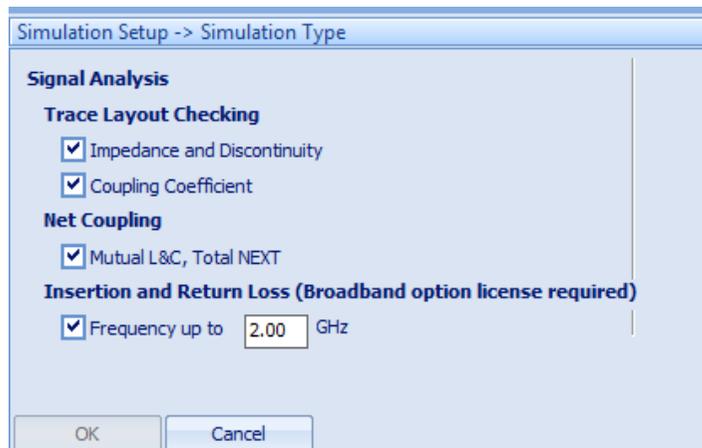
# Electrical Performance Assessment

- Power-Ground Analysis



Simulation Report.mht

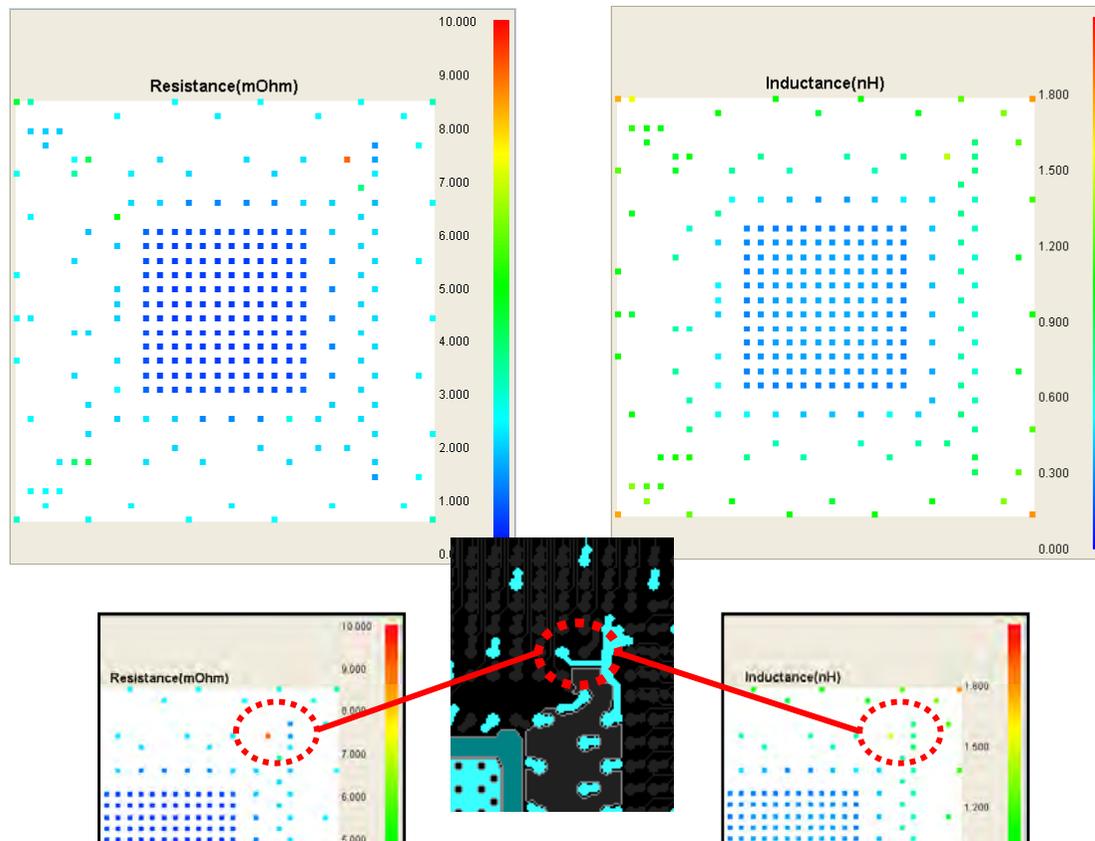
- Signal Analysis and Current Checking



# Electrical Performance Assessment

## Per-Pin Resistance and Inductance

- 2D displays of R and L from the die-side are shown below
  - ‘weak’ pins have higher R and L values and are more **red** than **blue**
  - ‘weak’ pins are rapidly identified with no special expertise required

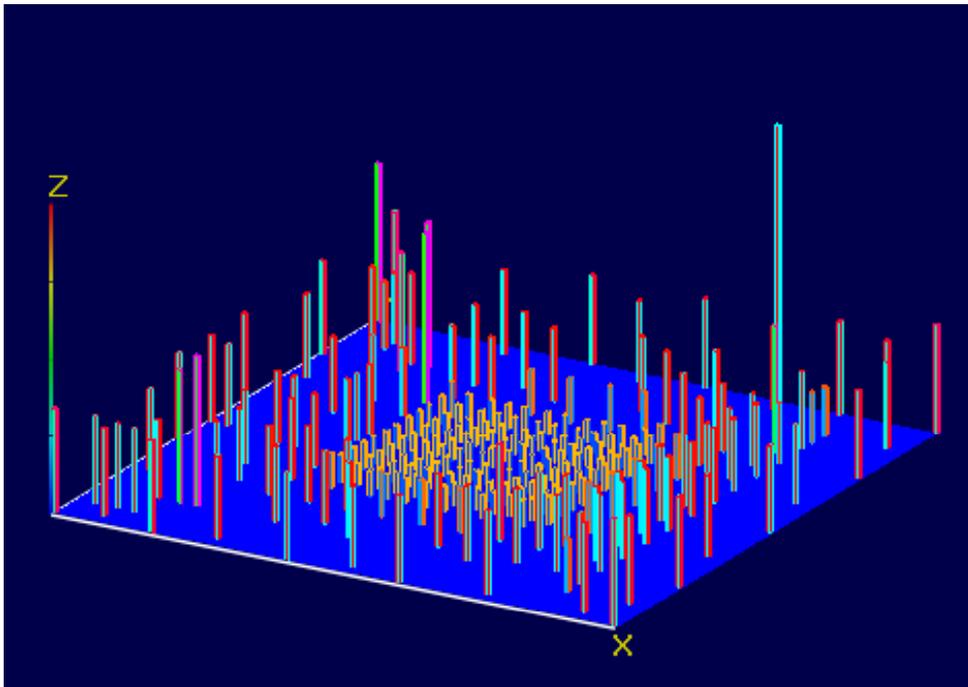


R is more affected by the long, thin interconnect.  
Loop inductance is more affected more by poor return path.

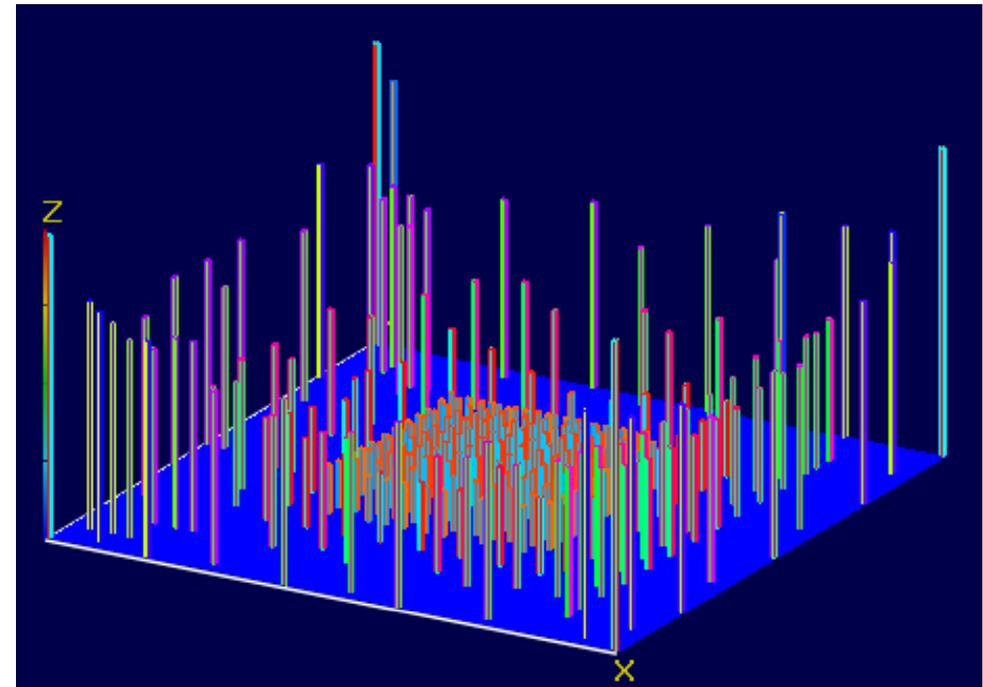


# Per-Pin Resistance and Inductance Assessment

- 3D displays of R and L are also available
  - helping to intuitively quantify the relative distributions
  - numerical tables are also available



Resistance



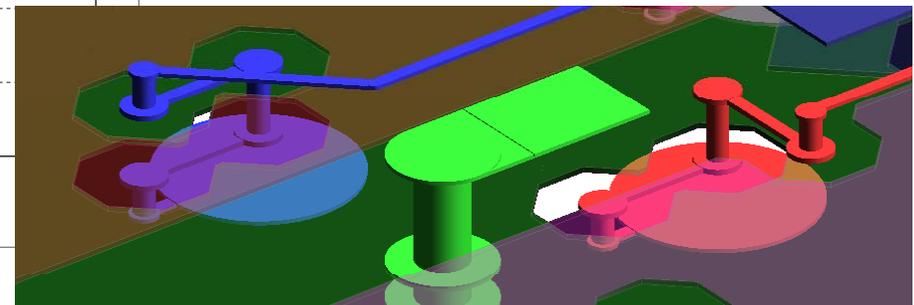
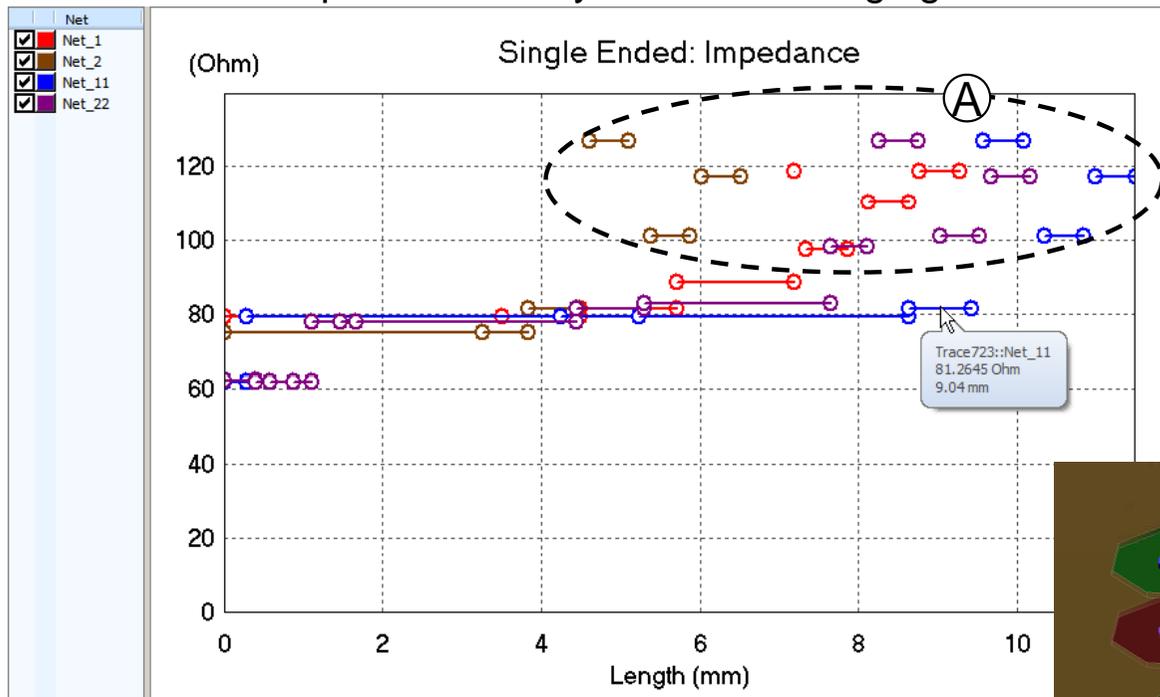
Inductance



# XtractIM

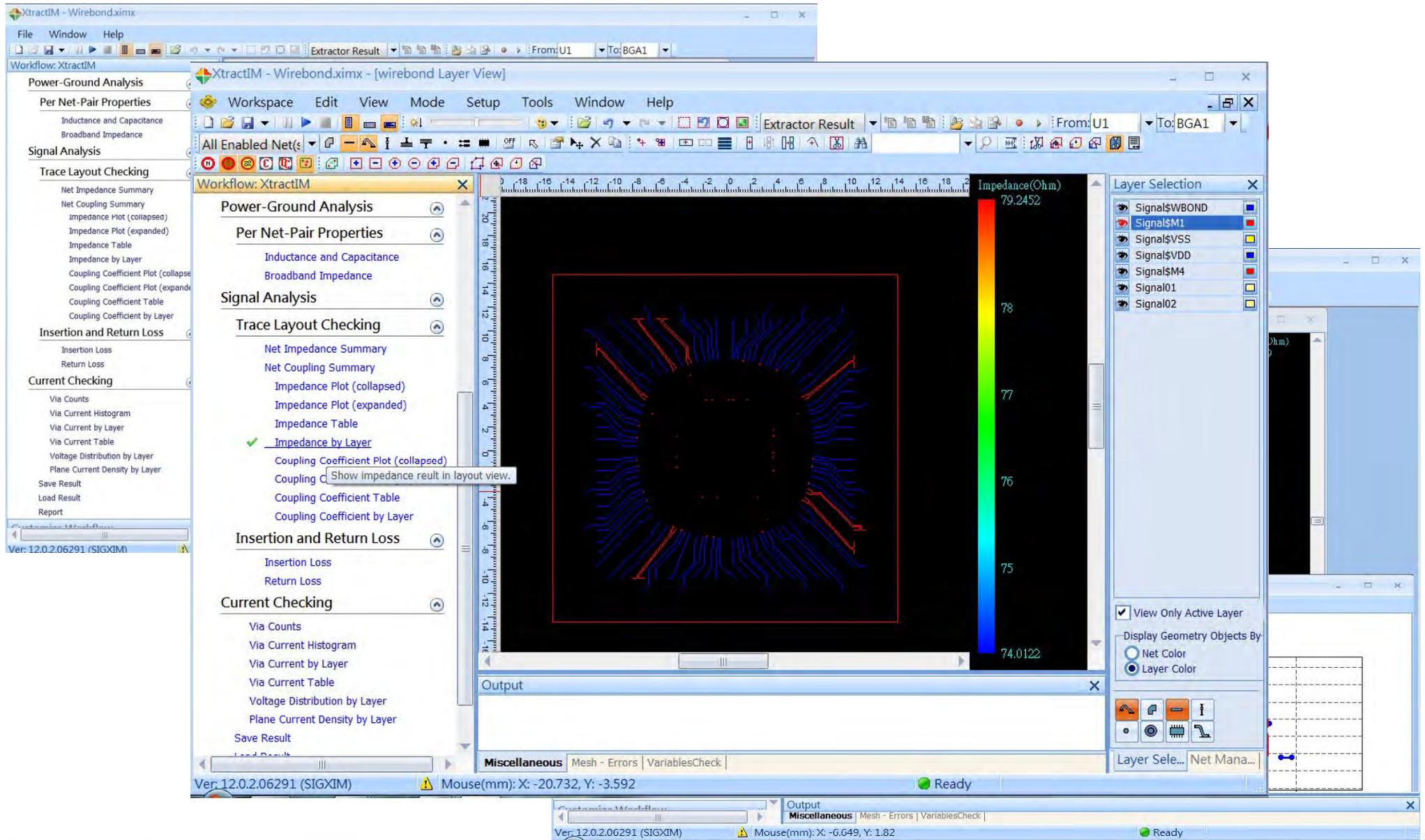
## EPA

- Single-ended impedances are displayed along the length of the nets
  - zero length is at die-side
  - trace color is same as net color
  - net, trace segment and impedance are displayed when cursor is positioned on plot
- A. potential issue of high impedance at board-side of nets (larger lengths)
  - top-to-bottom layer transition dogleg traces do not have good reference planes



- Quality Check for Package Design

# EPA – Impedance Plot



# Benefits and Observations

- XtractIM → generates, displays and exports standard electrical models for IC packages
  - Extended model support
    - High level assessment of package performance.
    - Support of system-level SI and PI analysis.
    - Both net-base and pin-based models.
  - Extraction display support
    - Electrical DRC sign-off and debugging.
- XtractIM → **Electrical Performance Assessment**
  - quickly identifies potential power and signal delivery issues
  - quantifies issues intuitively and numerically
    - documents potential issues for colleagues or management
  - helps identify physical root cause of issues and visualize design changes to address them
- XtractIM automates otherwise tedious analysis setup and results post-processing to quickly assess package electrical performance

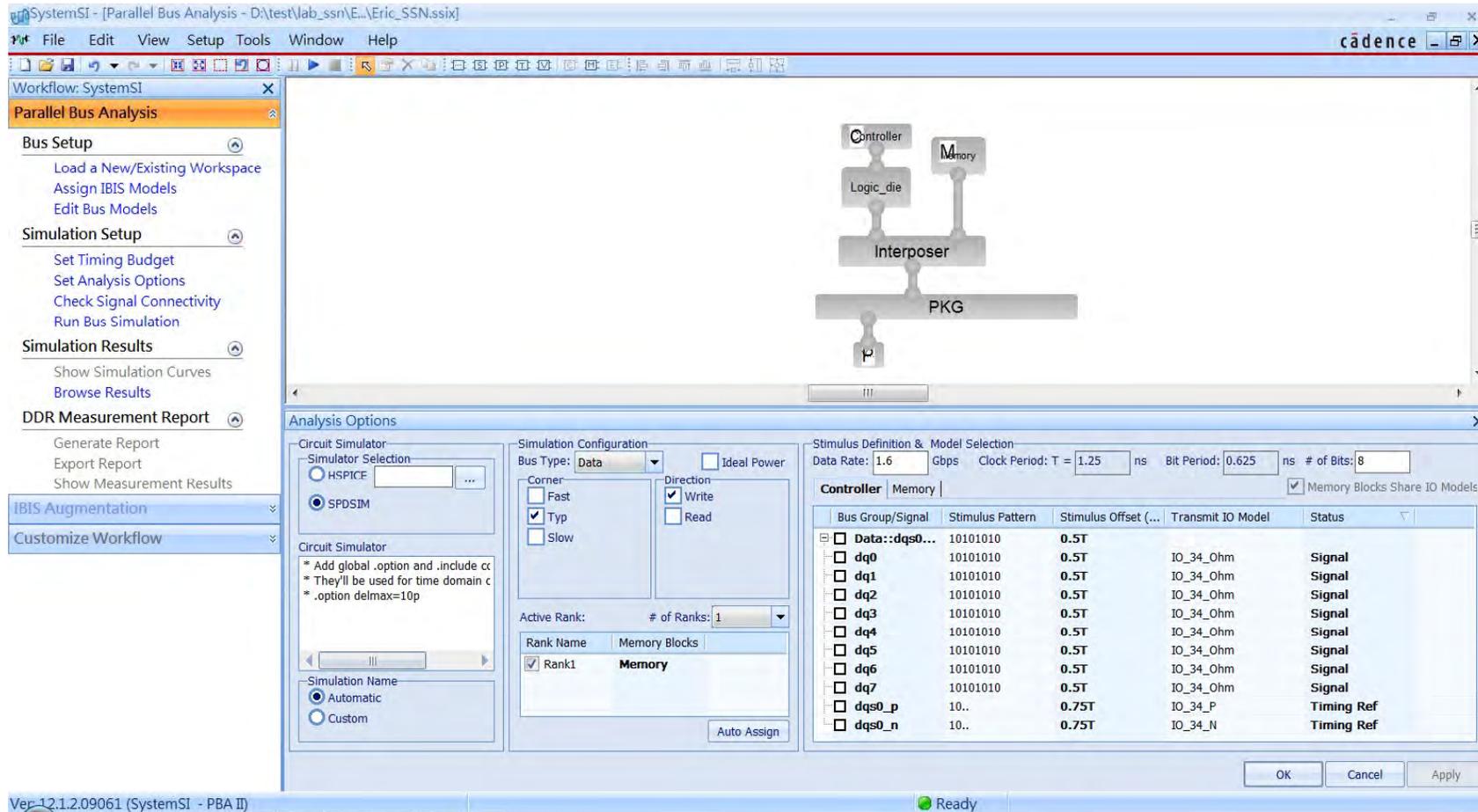


# System Simulation by SystemSI

## SystemSI – Chip-to-Chip Signal Integrity Analysis



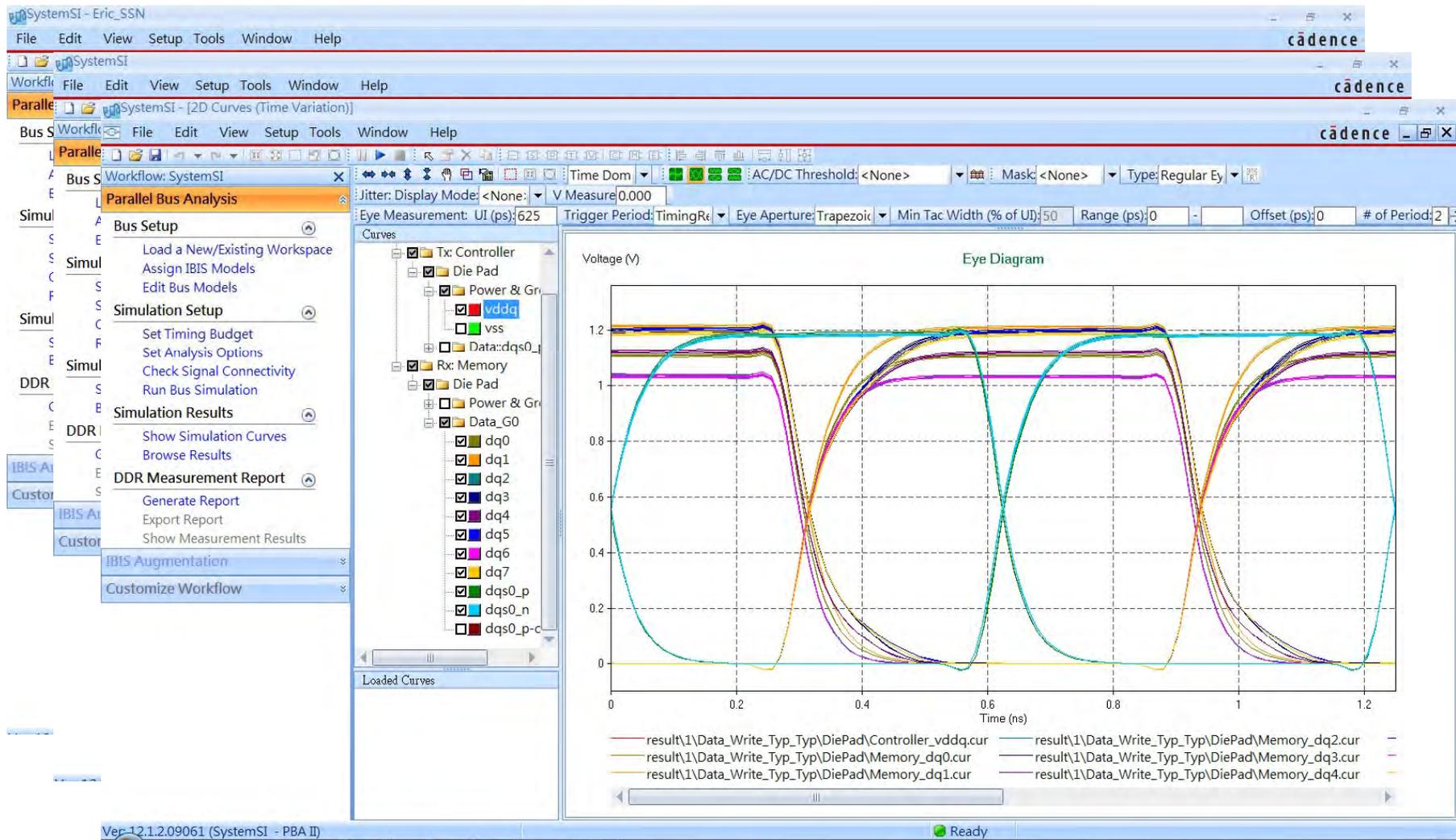
# SystemSI PBA – Parallel Bus Analysis



- Blocked based topology editor with SPICE sub-circuits modeling approach
- I/O modeling flexibility for power-aware IBIS and transistor level circuits



# SystemSI PBA – View Waveform & Eye



# SystemSI PBA – Report Generator

Report1

### 4.4.1.1.1 Memory

Click on a signal name to see its waveform displayed.  
Click on a criteria in a column header to see all its plots.

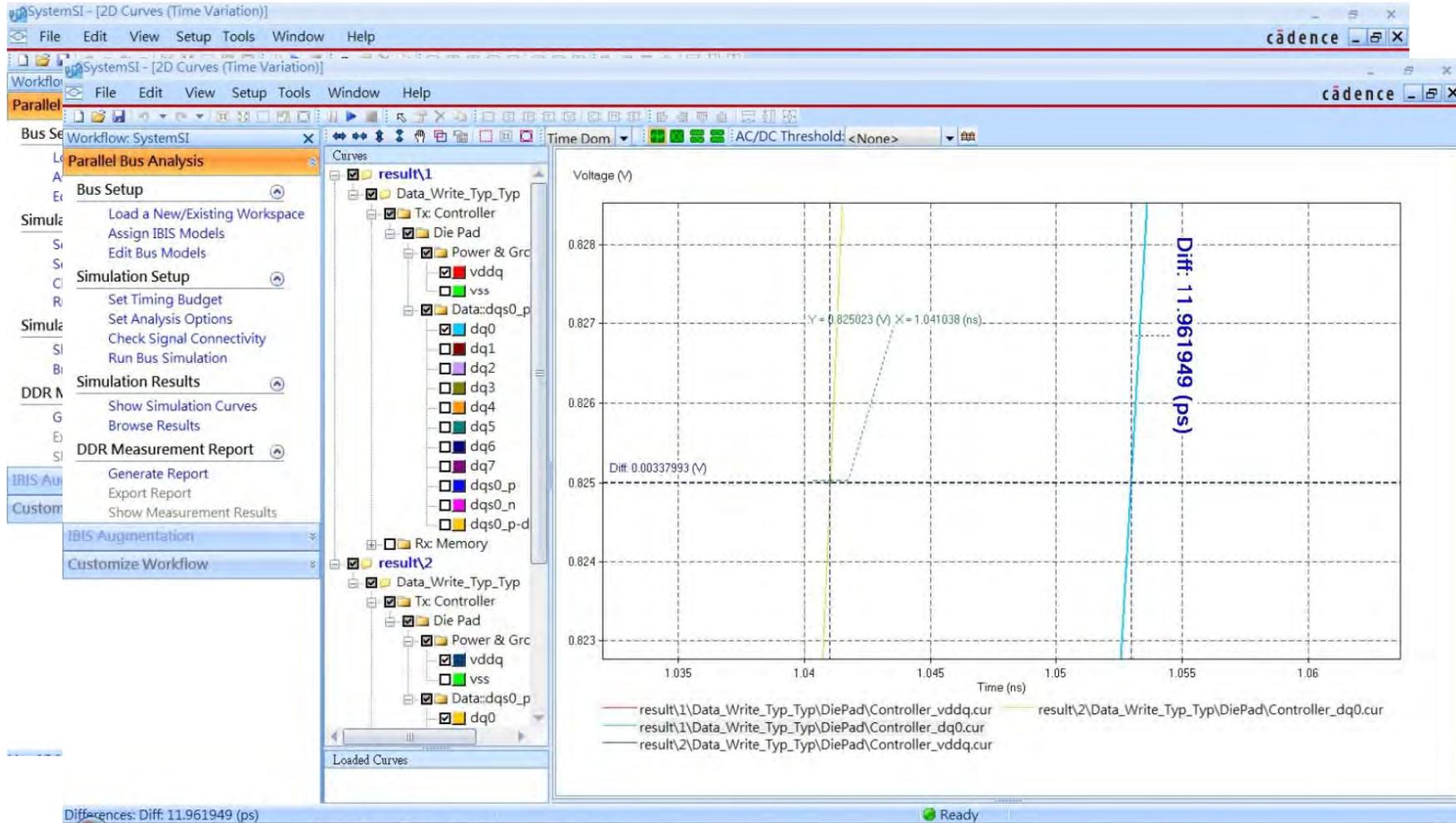
Bus Type: Data, Edge Type: BothEdges, Bus Group: Data\_G0, Timing Ref: dqs0\_p-dqs0\_n, Measurement Range: [2477.09ps, end]  
Rx Specs: Min Receive Setup: 0.15625ns, Min Receive Hold: 0.15625ns. TimingRef was shifted left by 103.882 ps for the Worst Case Setup Condition.

Rx Signal	Pin	[Min, Max]	[Min, Max]	[Min, Max]	Min	[Min, Max]	Min	Min	Min	[Min, Max]	Min	Min
		SlewRate	SlewRate	SlewRate		tDS				tDS delta		
Waveform		TimingRef (V/ns)	Setup (V/ns)	Hold (V/ns)	(ps)	(ps)	tDS adj (ps)	(ps)	(ps)	(ps)	(ps)	(ps)
dq0	1	[28.2219, 28.3417]	[9.21011, 13.977]	[12.9668, 15.5097]	185.993	[75, 75]	110.993	-45.257	399.955	[50, 50]	349.955	193.705
dq1	2	[28.2219, 28.3417]	[10.94, 13.8224]	[13.7019, 16.3458]	190.351	[75, 75]	115.351	-40.8989	407.392	[50, 50]	357.392	201.142
dq2	3	[28.2219, 28.3417]	[8.48646, 14.7137]	[12.3841, 14.698]	183.035	[75, 75]	108.035	-48.2151	393.8	[50, 50]	343.8	187.55
dq3	4	[28.2219, 28.3417]	[8.23391, 11.48]	[12.3123, 15.0982]	181.684	[75, 75]	106.684	-49.5661	408.196	[50, 50]	358.196	201.946
dq4	5	[28.2219, 28.3417]	[8.02241, 12.7427]	[12.1286, 14.8608]	181.152	[75, 75]	106.152	-50.0979	401.729	[50, 50]	351.729	195.479
dq5	6	[28.2219, 28.3417]	[8.44563, 11.638]	[12.4044, 15.2882]	183.12	[75, 75]	108.12	-48.1303	408.095	[50, 50]	358.095	201.845
dq6	7	[28.2219, 28.3417]	[8.52647, 14.8858]	[12.4122, 14.7899]	183.603	[75, 75]	108.603	-47.6474	<b>393.509</b>	[50, 50]	<b>343.509</b>	<b>187.259</b>
dq7	8	[28.2219, 28.3417]	[8.10087, 11.4645]	[12.1599, 15.001]	<b>181.138</b>	[75, 75]	<b>106.138</b>	<b>-50.1124</b>	407.516	[50, 50]	357.516	201.266
dqs0_p-dqs0_n	33, 37	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

Note: NA = Not Applicable; NMP = No Measurement Possible; OOR = Out of Range.

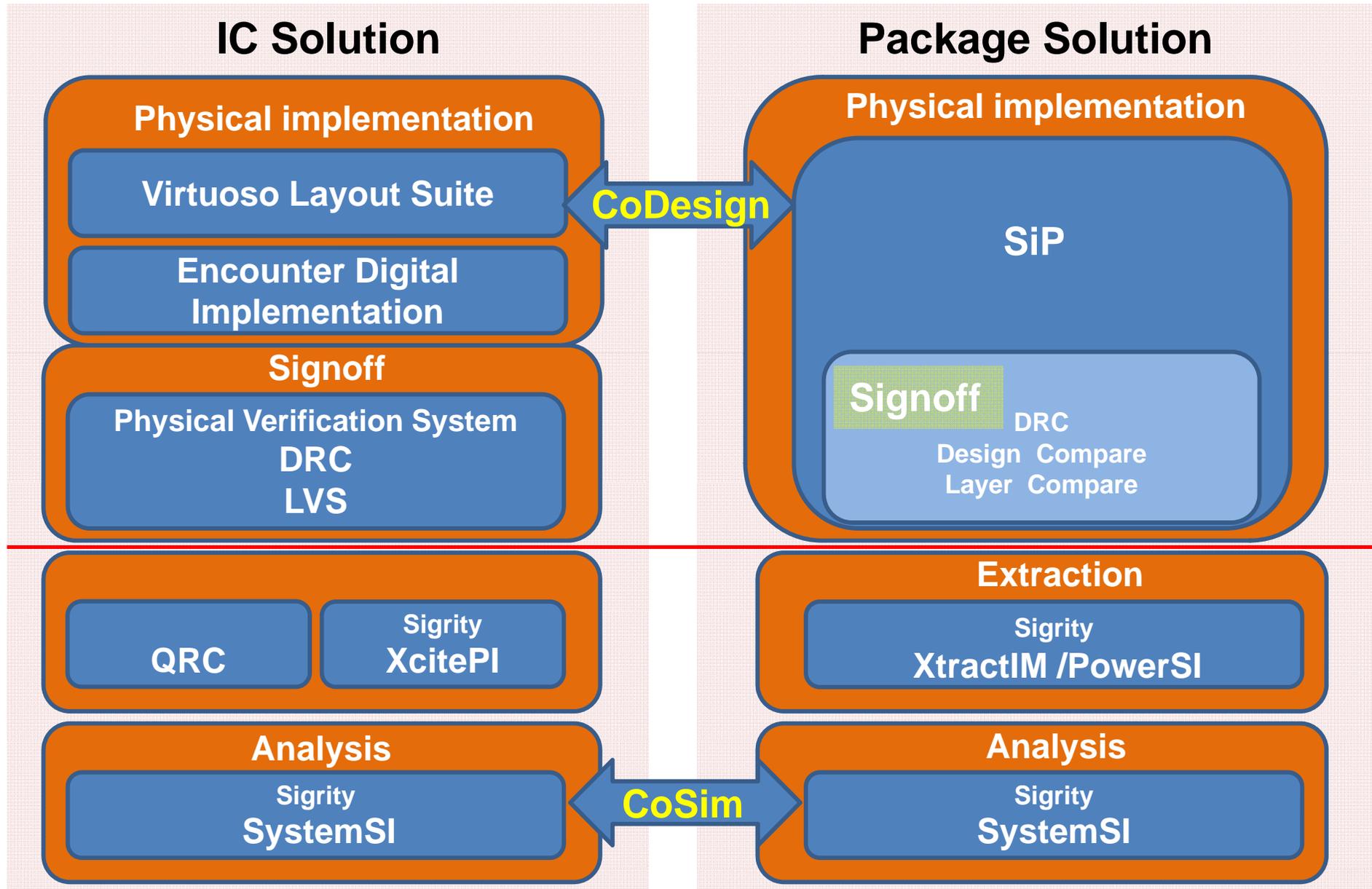


# SystemSI PBA – Ideal vs Non-Ideal Power





# Summary



*Thanks !!!*

