



快速 2014 SPB Seminar  
模擬驗證完善  
設計規範  
SIGNAL AND POWER INTEGRITY

# OrCAD Oriented Pre-Simulation

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4/Jul/2014

**Graser**<sup>®</sup>

# Simplify The Complexity of Product Design Function Verification - OrCAD PSpice



# Topic

- Design Challenges
- Production Challenges
- How to help developing new design faster and more stable
- Mechatronics integration Design
- Modularized simulation
- How to help your customer to get more powerful support

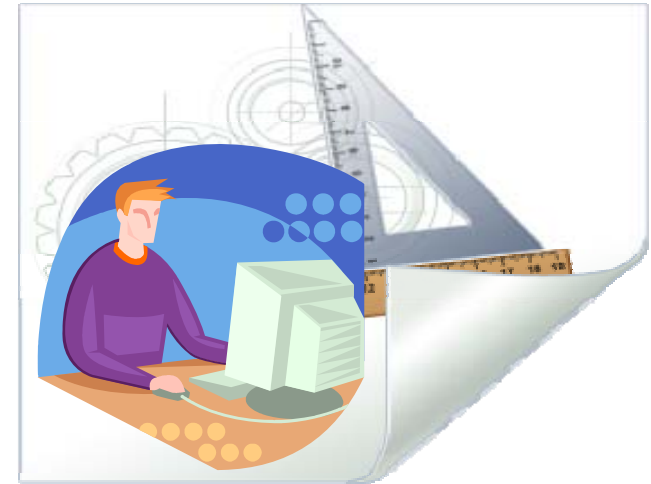


# Design Challenges

Step 1 :

Make circuit design on your system

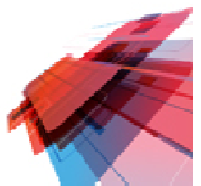
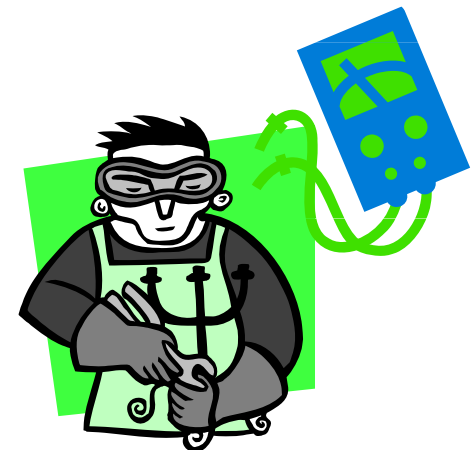
- Does it work ?
- Is it stable ?



Step 2 :

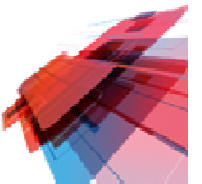
Make a Prototype in Laboratory

- Prepare equipment
- Connect system in between
- Does it work ?
- Is it stable ?

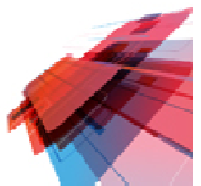
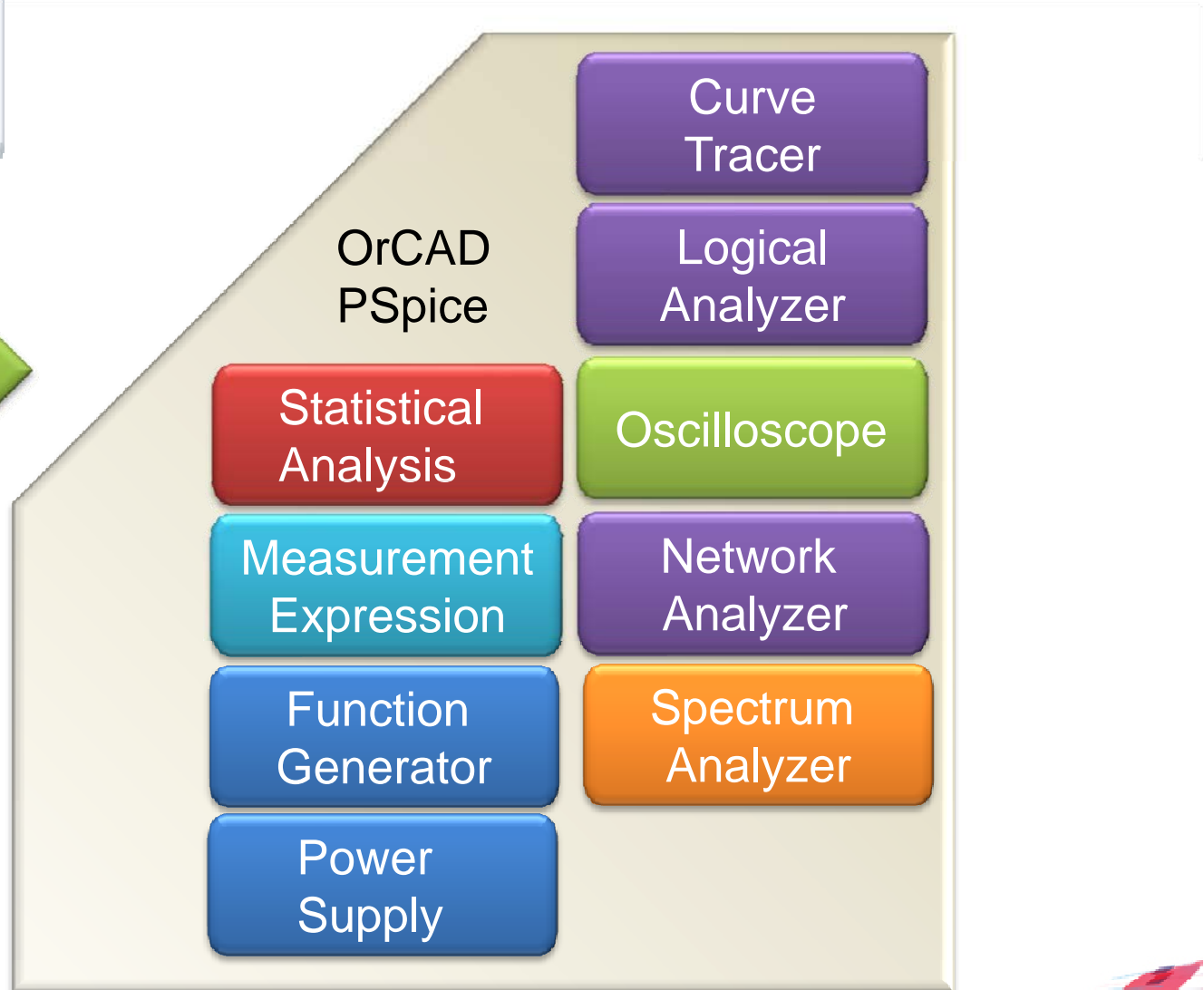


# Traditional Design Flow

- Schematic drawing in your design
- Make prototype
- Measurement in Laboratory
- **Repeatedly try and error**

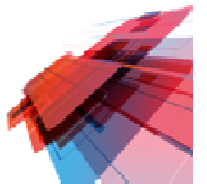
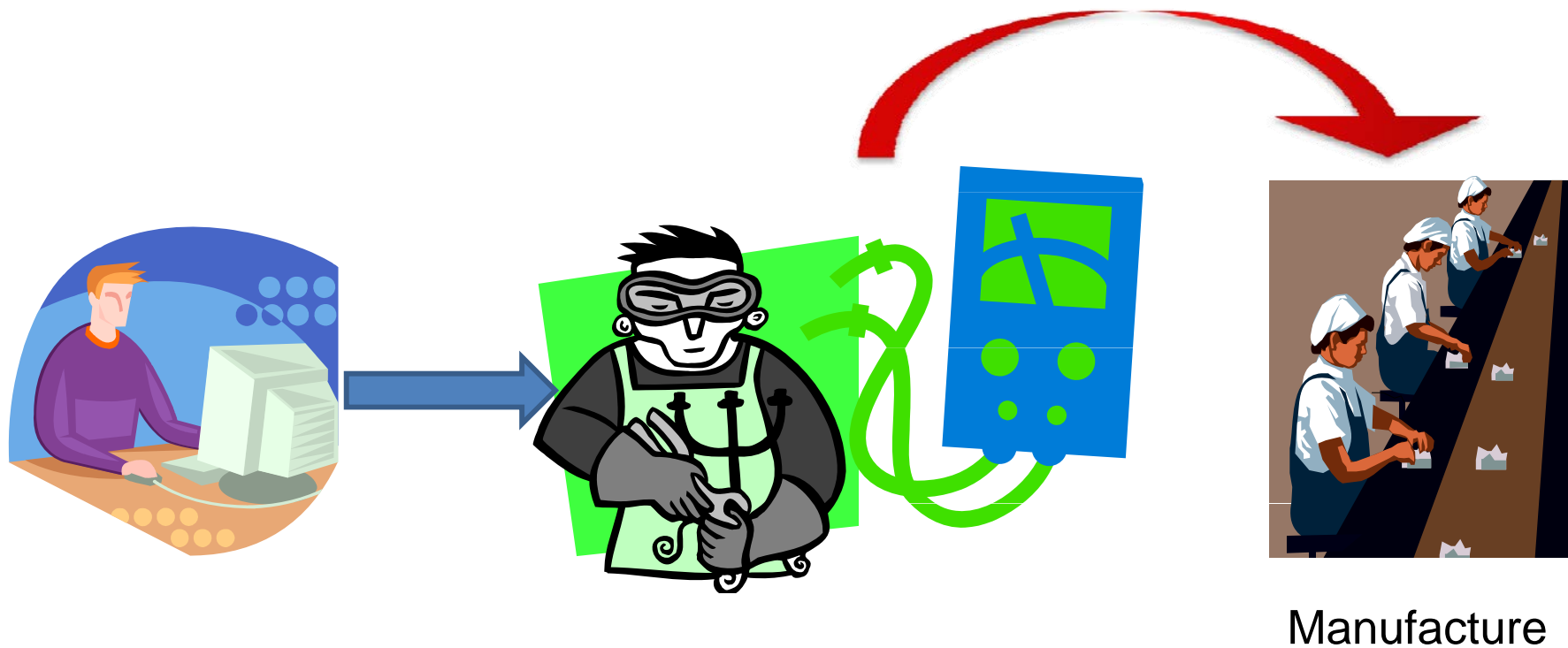


# A Virtual Laboratory – OrCAD PSpice



# Virtual Design Flow

- Schematic drawing
- Simulate and results confirmation
- PCB layout



# A Quality Analysis Laboratory

- **Mass Production Issues**
  - Complexity
  - Stability
  - Components Specification
  - Cost





# Mass Production Challenges

## Prototype

- It works
- It is stable

## How about Mass Production ?

- Parts specification ?
  - Tolerance
  - Temperature issue

**Is it stable ?**



# Enhance Circuit Design Stability

- Is simple best ?
- Using Parts with high accuracy and stable specification to improve stability.
- Enhance stability with compensate circuit design.
- Using other structure design.

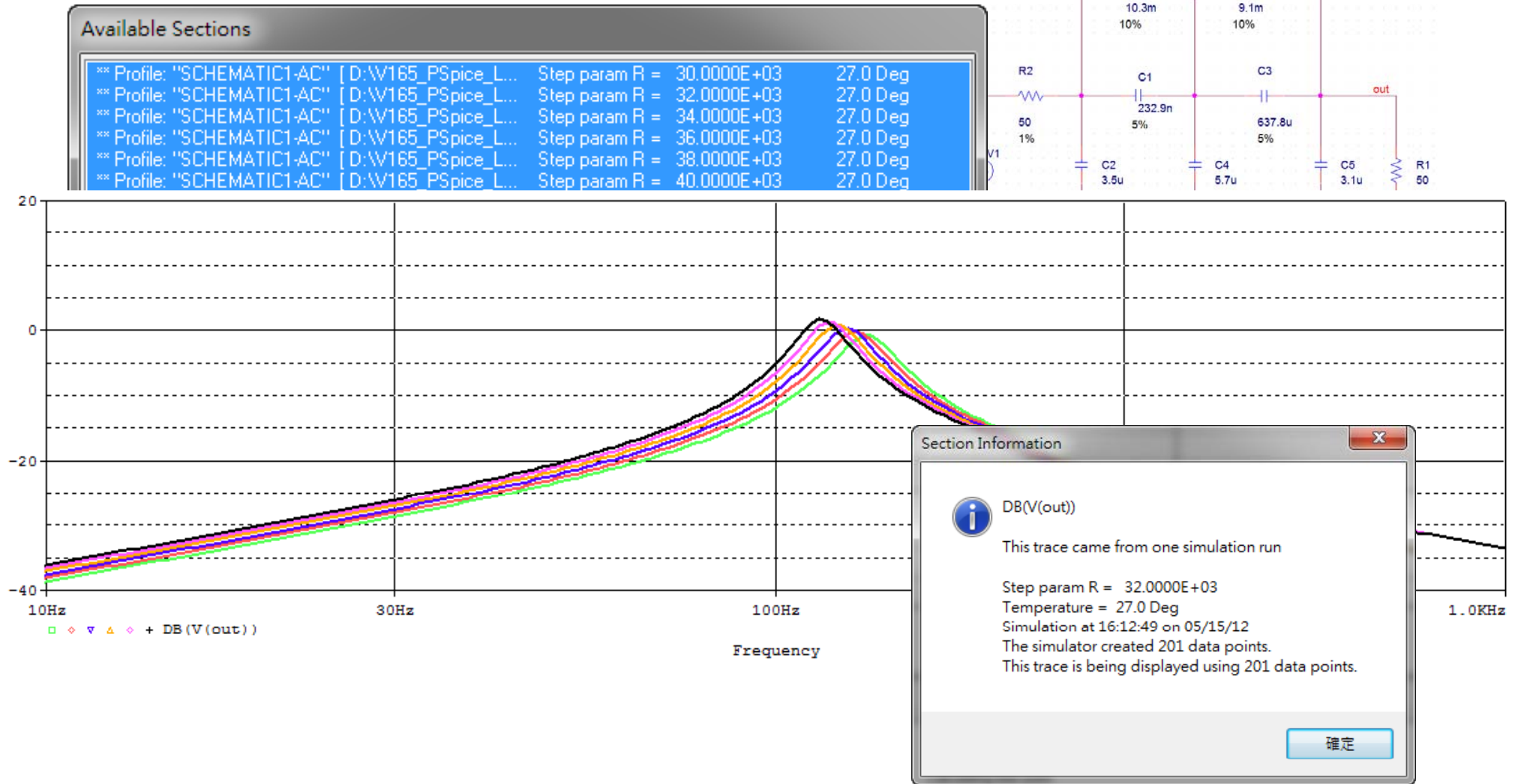


# Design Flow for Mass Production

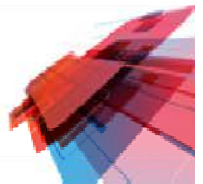
- Get a standard system design from origin
- Measure and find out better structure
- Include tolerance and temperature parameters
  - Parametric Sweep
  - Worst Case Analysis
  - Monte Carlo Analysis ( Yield )



# Parametric Sweep

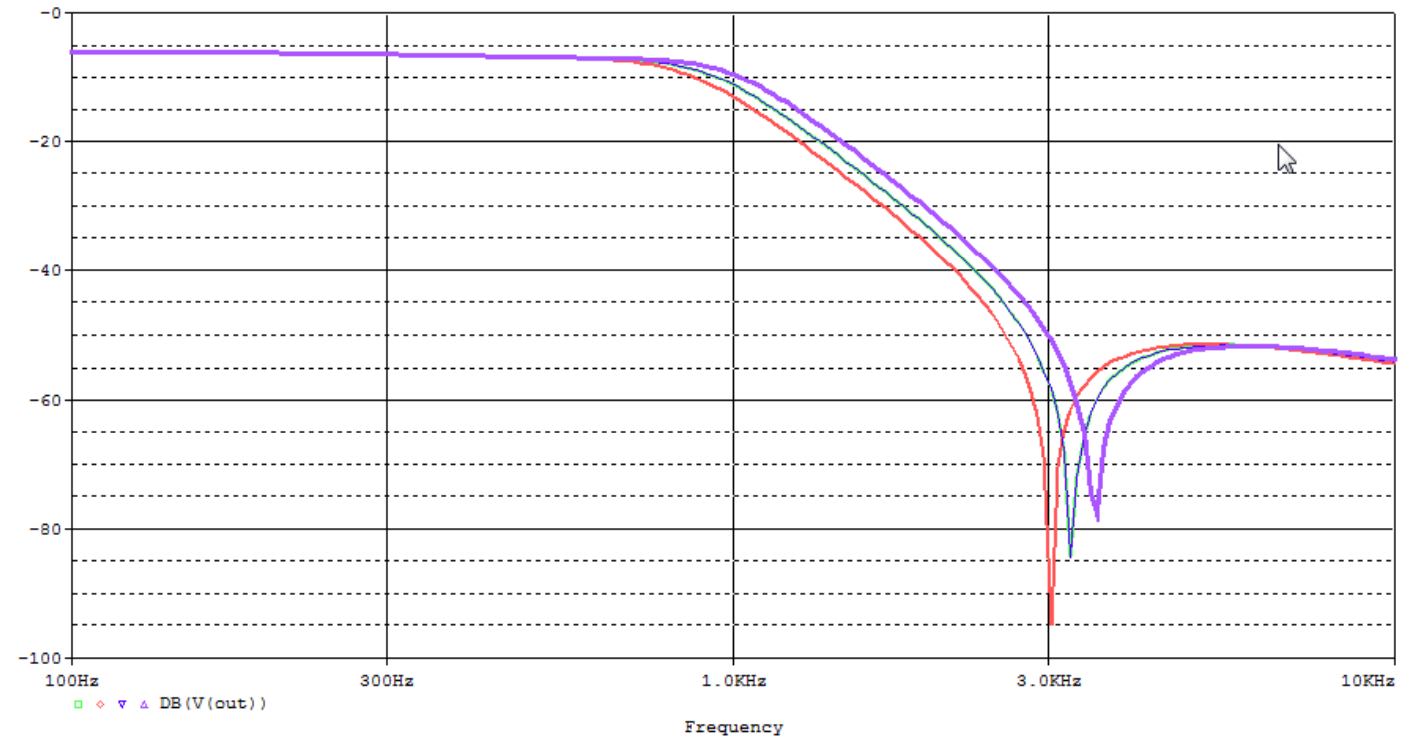
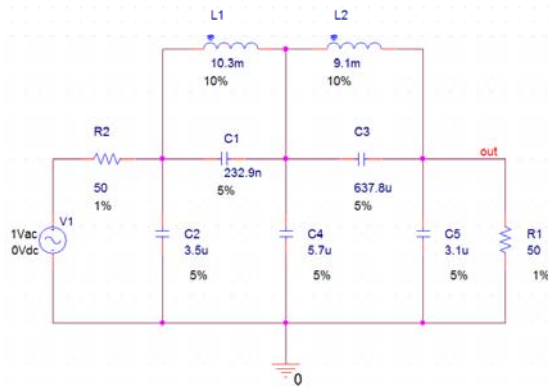


- Make sure structure and parts are good for design.

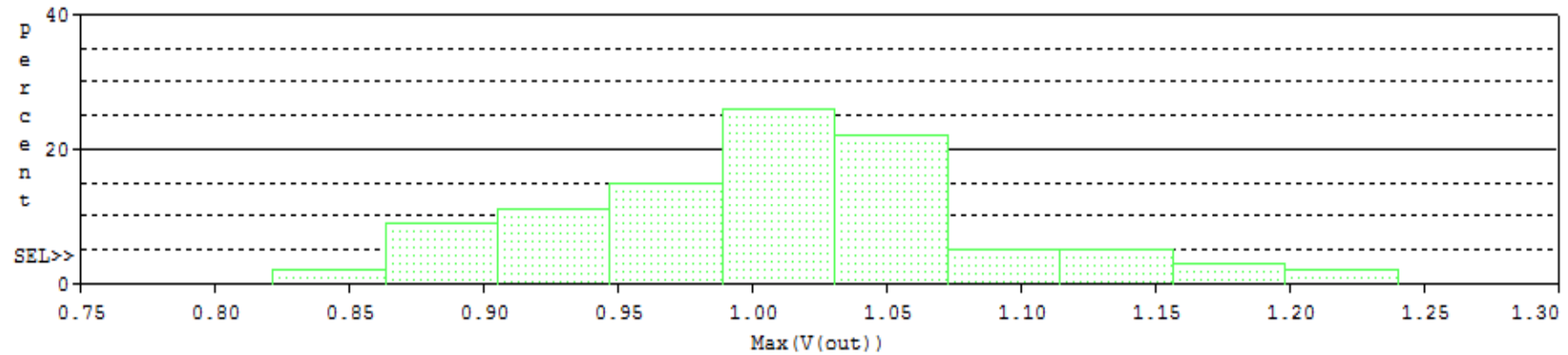


# Worst Case Analysis

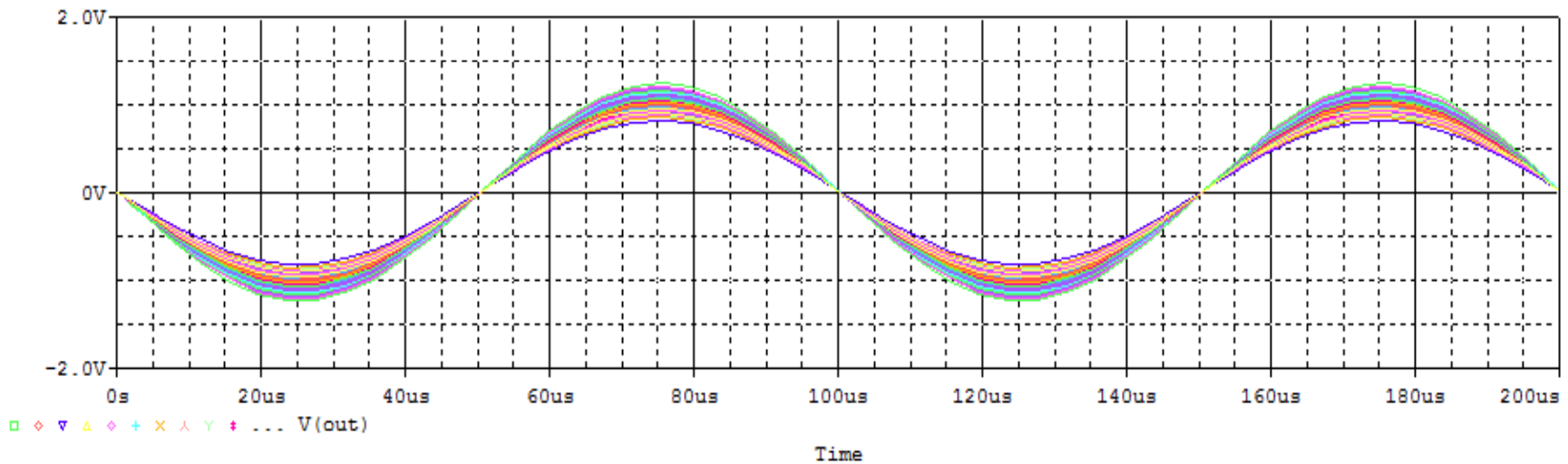
- Effects of Components Tolerance Limitation on Worst-Case Analysis



# Monte Carlo Analysis



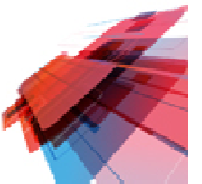
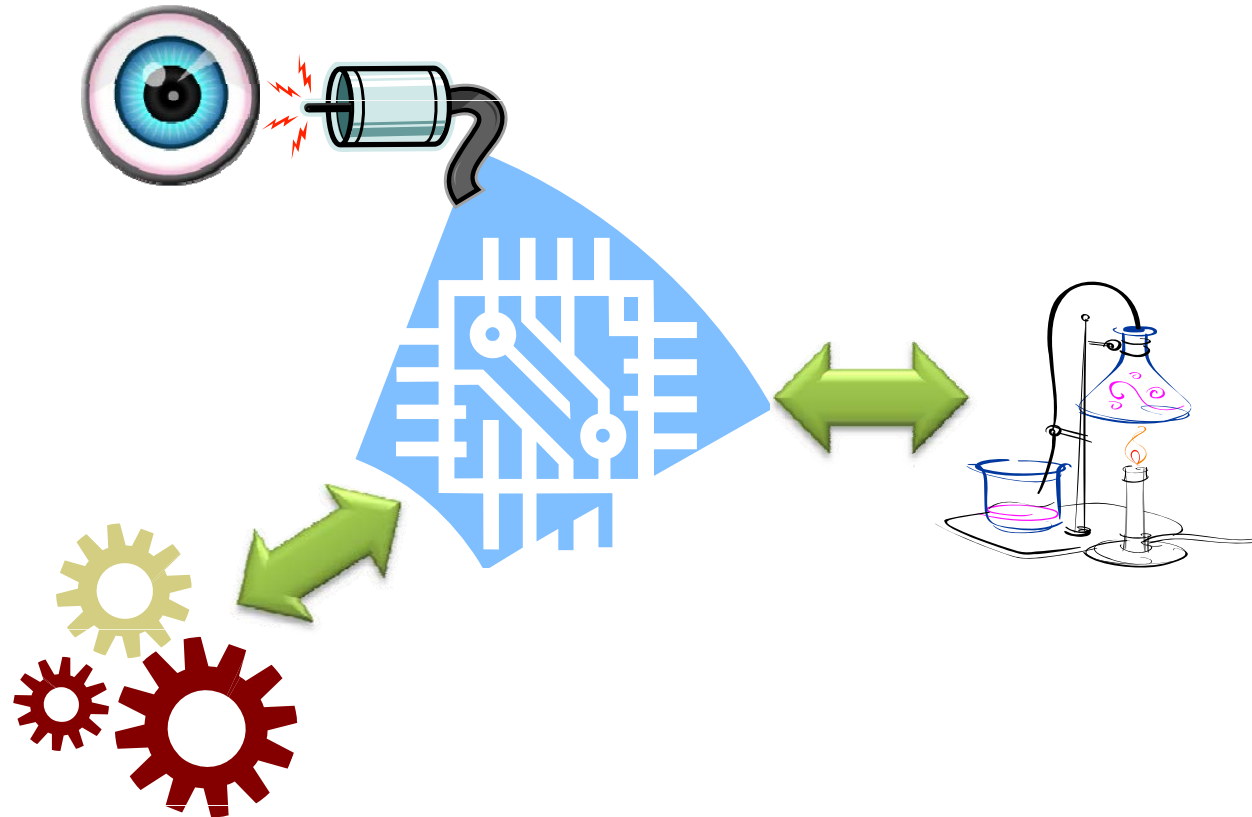
n samples	= 100	mean	= 1.00885	minimum	= 0.821461	median	= 1.00771	maximum	= 1.24008
n divisions	= 10	sigma	= 0.0795893	10th %ile	= 0.899438	90th %ile	= 1.11433	3*sigma	= 0.238768



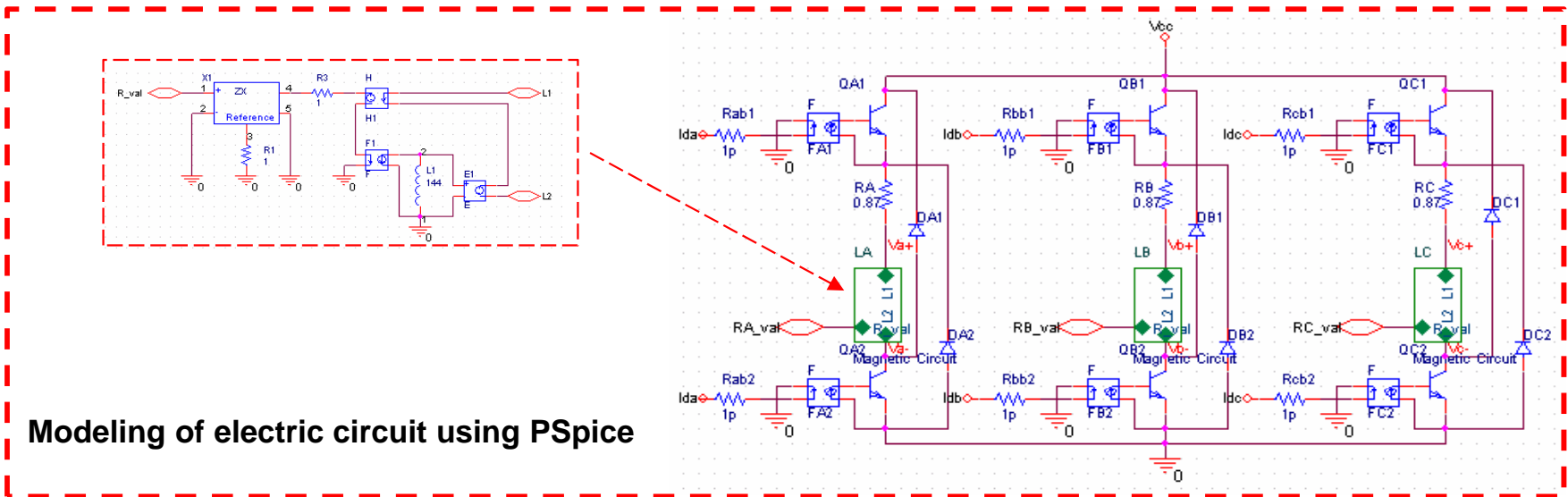
# Mechatronics Integration Design

## Automotive Safety System

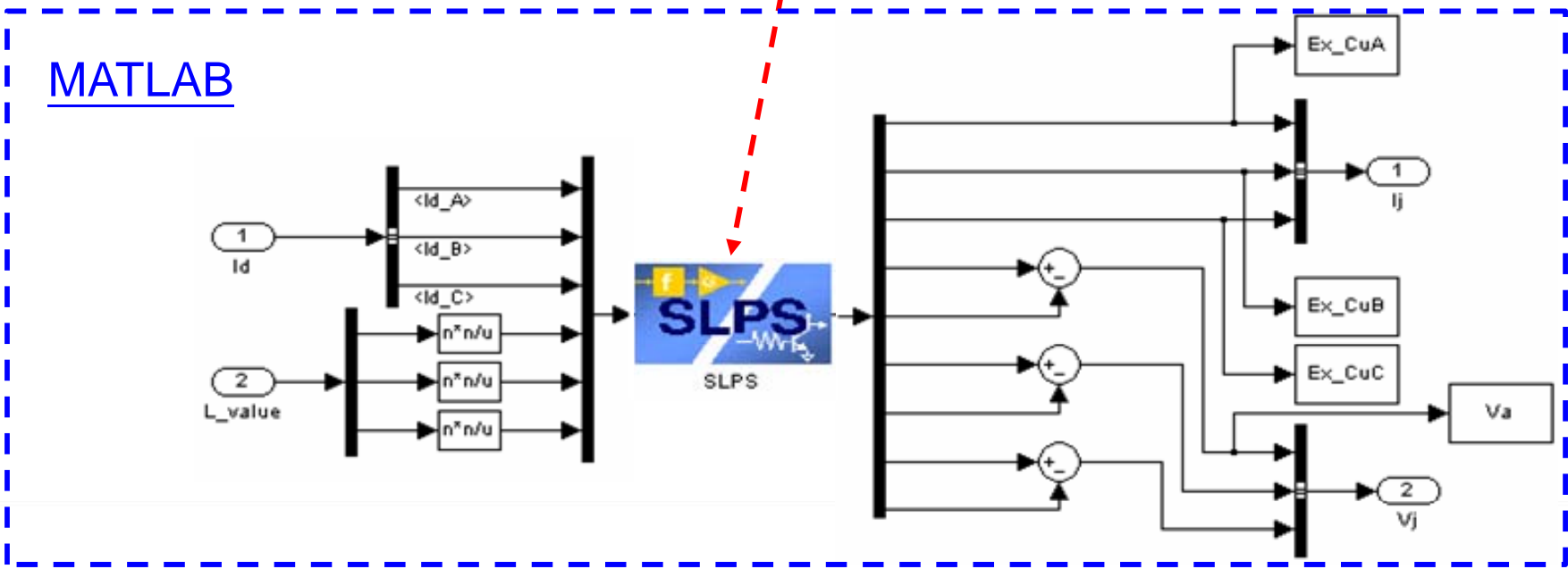
- Passive mode : ABS 、 Airbag 、 Reversing radar
- Active mode : DSTC , ROPS , EBD , CWFAB , PDFAB , DAC , LDW



# SLPS Option

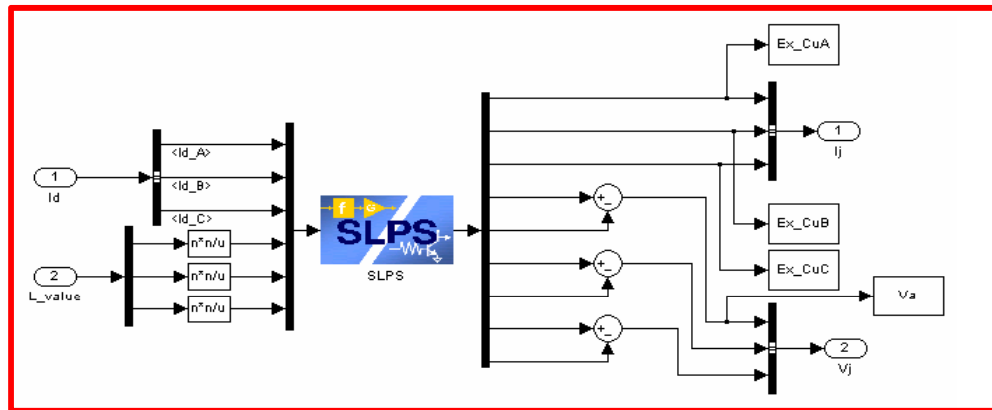


Modeling of electric circuit using PSpice

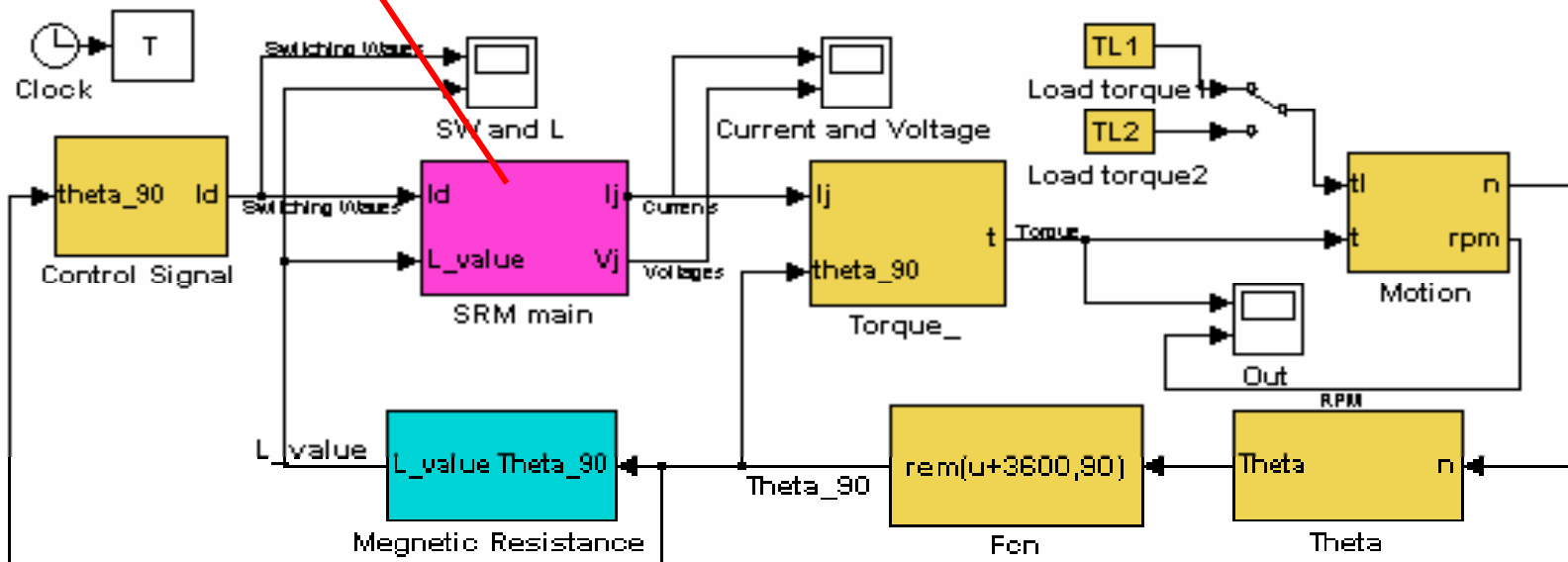




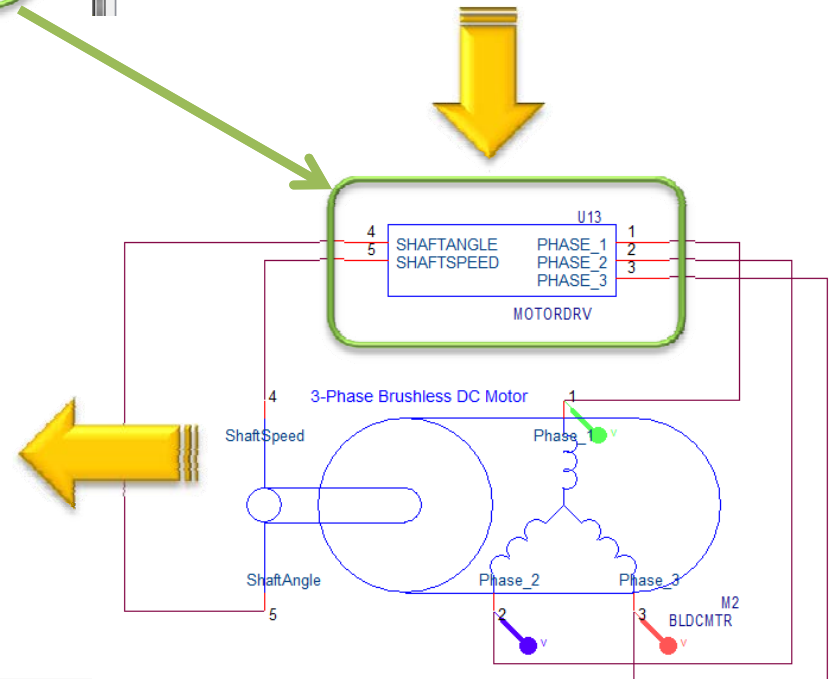
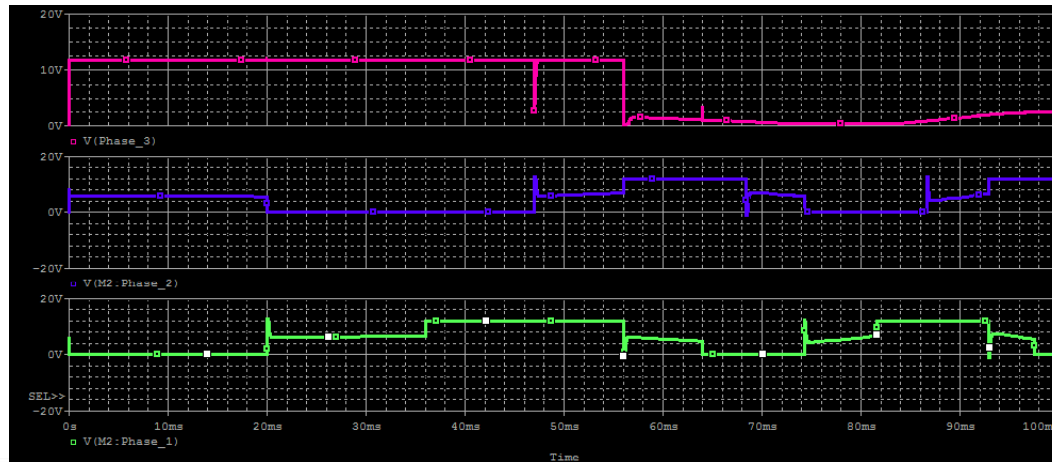
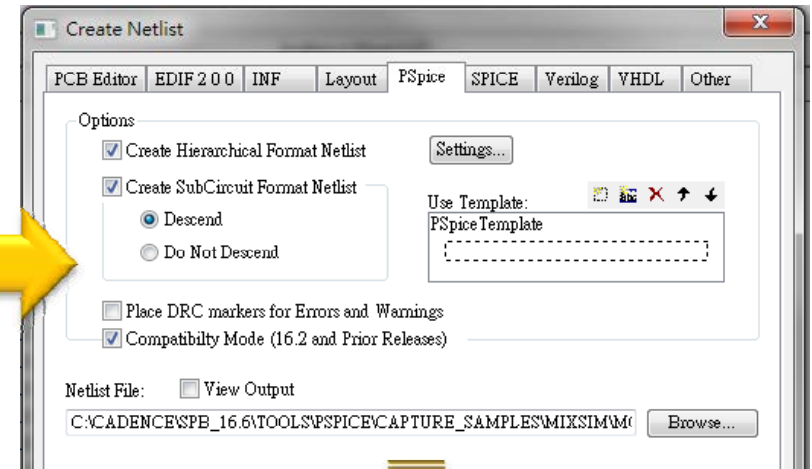
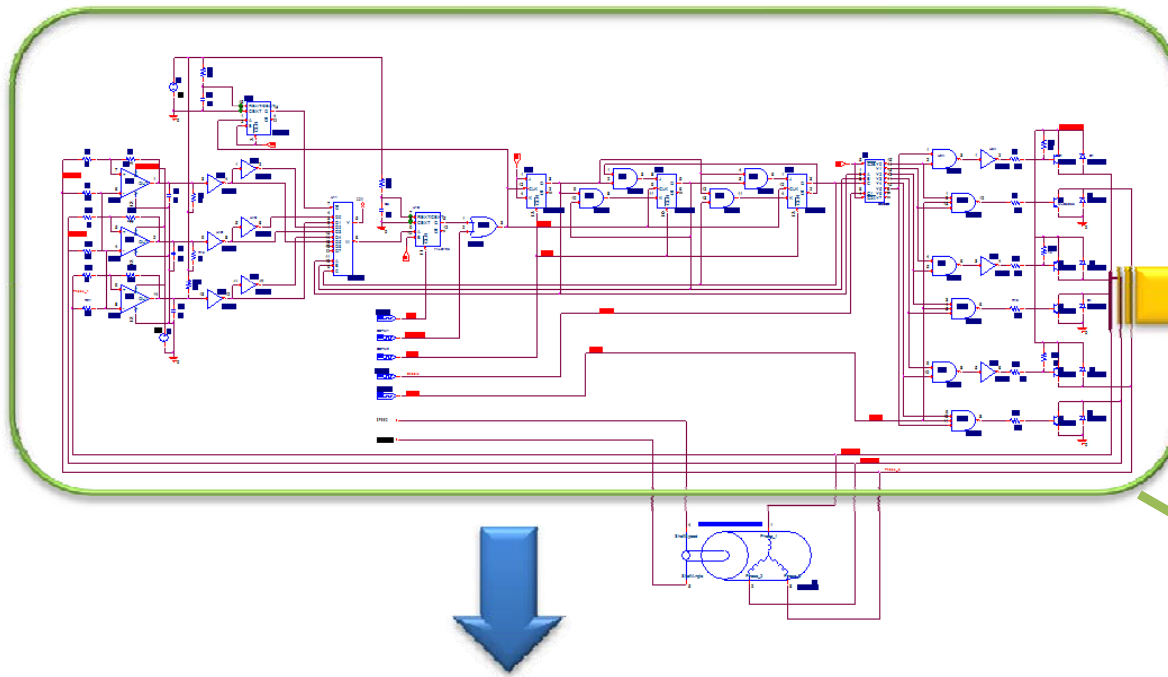
# Multi-System Co-Simulation



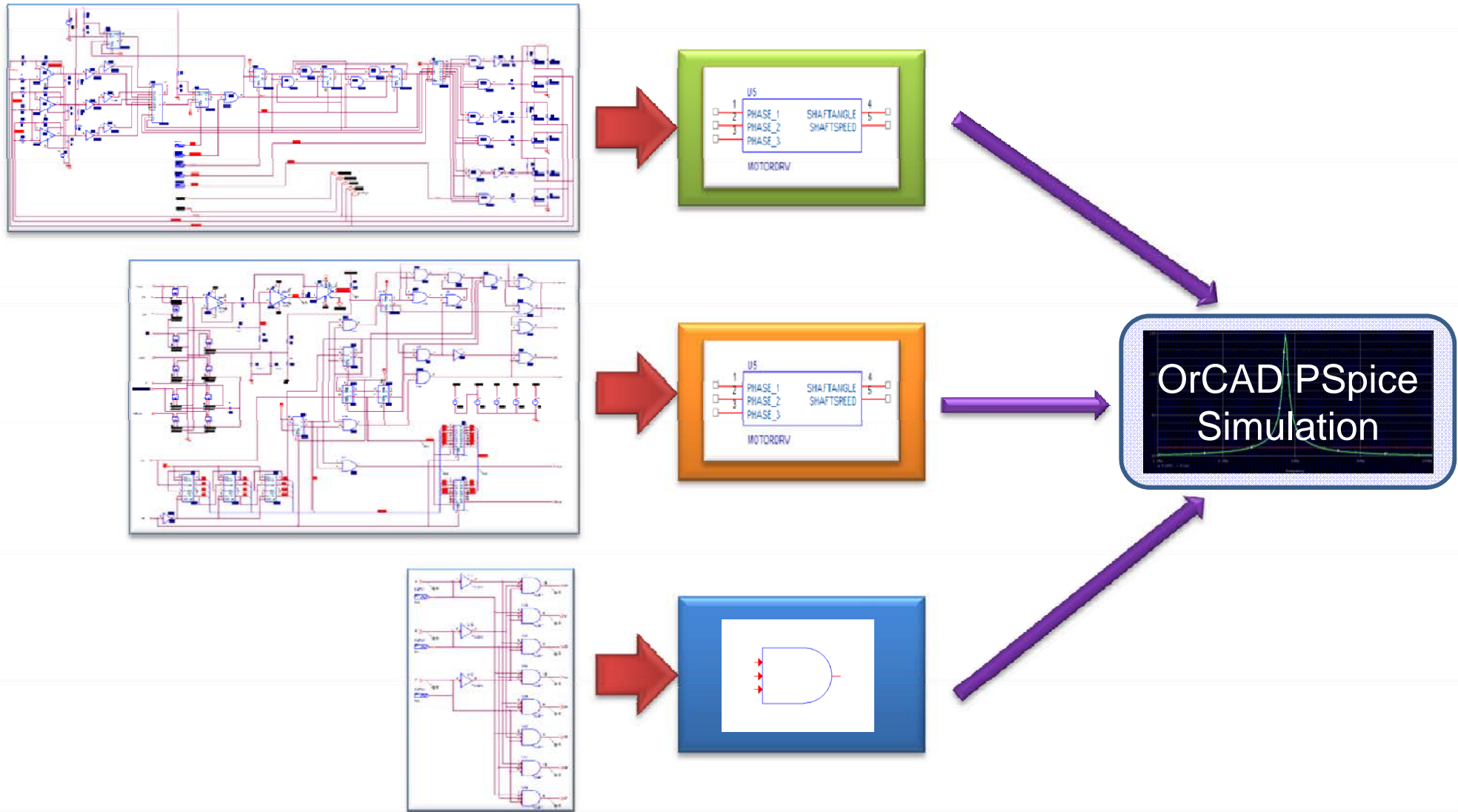
SRM control model with SLPS



# Modularized Design and Simulation



# Modularized Design and Simulation



***P*Spice is a**

Virtual Laboratory

Senior Application Engineer

Quality Analysis Laboratory

- Reduce Loading in Product Design Process
- Cost Down
- Time to Market



# OrCAD SI



# Signal Integrity Flow

## OrCAD Schematic

### SI Model Association

Tools Place **SI Analysis** Macro Accessories Options

- SI Library Setup
- Auto Assign Discrete SI Models
- Identify DC Nets
- Assign SI Model
- Explore Signal
- Export Topology
- Export Electrical Csets
- Import Electrical Csets
- Remove Electrical Cset Assignments
- Associate Electrical Cset
- Validate Electrical Cset Assignments
- Validate SI Model Assignments
- SI Model Integrity
- Export SI Models Used
- Remove SI Model Assignments

SI Model Assignment

RefDes	No of Pins	Model Nam	Model Type
RC1	2		
REBAS	2		

SI Library: c:\si\_library.dmi, c:\si\_models.nls

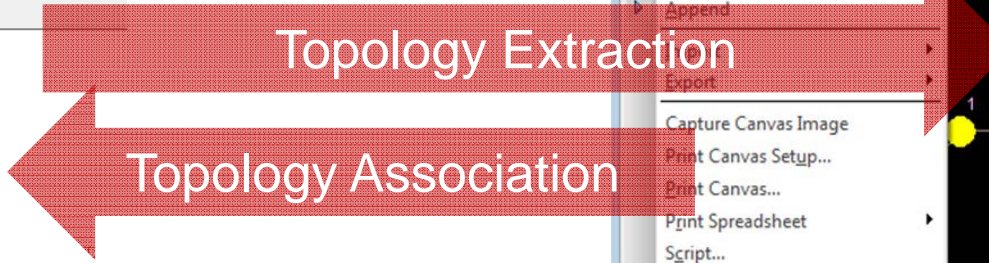
SI Model: 4Port, C2tp\_wthpkg, cable\_espcie, capacitor09pf, CDS\_jds\_device, CDS\_Pch\_device, CDS\_Pkg140IP\_Ckt\_M, CDS\_Pkg140IP\_Sparam, CDS\_Pkg140IP\_Sparse, CDS\_Pkg140IP, CDS\_Pkg160IP, EightPin\_16bv, EightPin\_3p3v, EightPin\_3p3v, inductor15mH

Model Type: ESpcieDevice, ESpcieDevice, ESpcieDevice, ESpcieDevice, IbsDevice, IbsDevice, PackageModel, PackageModel, PackageModel, PackageModel, PackageModel, IbsDevice, IbsDevice, IbsDevice, ESpcieDevice

SigXplorer OrCAD PCB SI: TX+\_3450.top 1.0 Project: D:\PARAGC\TESTCKTS\SI\SIG

File Edit View Setup Analyze Help

- Analyze / Edit Topology
- Update Capture
- Update Constraint Manager
- Append
- Export
- Capture Canvas Image
- Print Canvas Setup...
- Print Canvas...
- Print Spreadsheet
- Script...
- Recent Topologies
- Exit



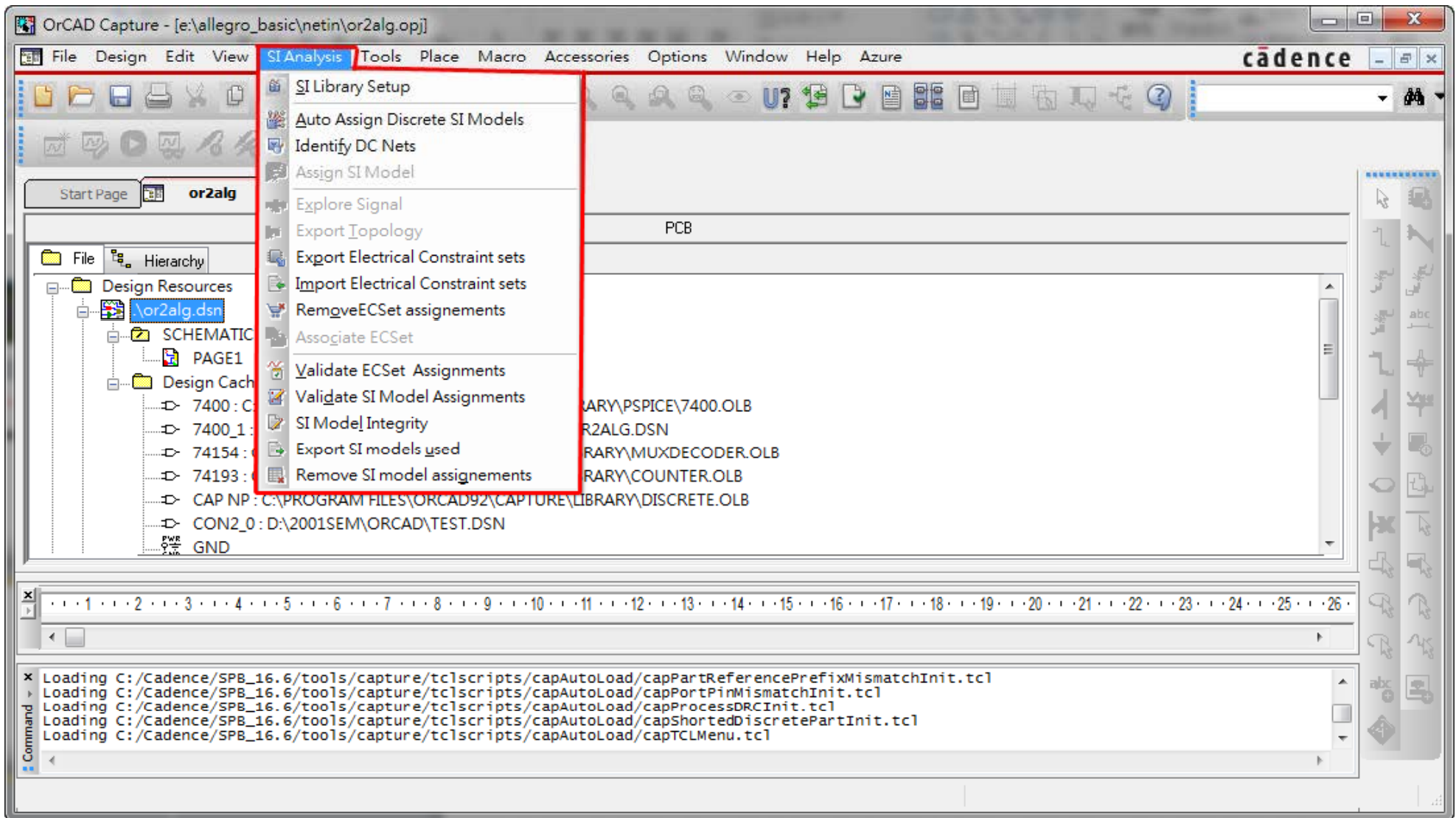
Netlist to PCB Editor

Allegro Constraint Manager (connected to Allegro PCB Design XL 16.0\_GREEN) - [Physical: Nets: All Layers]

Objects	Referenced Physical Cset	Min	Max	Min Width	Max Length	Different
System	System	5.00	0.00	4.00	1000.00	0.00
CL51	DEFAULT	5.00	0.00	4.00	1000.00	0.00
ADDRESS_BUS	DEFAULT	5.00	0.00	4.00	1000.00	0.00
DP_SYNC_CLOCK	DEFAULT	5.00	0.00	4.00	1000.00	0.00
BRANCH_0	DEFAULT	5.00	0.00	4.00	1000.00	0.00
BUF_OUT	DEFAULT	5.00	0.00	4.00	1000.00	0.00
FLOW_OUT	DEFAULT	5.00	0.00	4.00	1000.00	0.00
GND	DEFAULT	5.00	0.00	4.00	1000.00	0.00
L0	DEFAULT	5.00	0.00	4.00	1000.00	0.00
L1	DEFAULT	5.00	0.00	4.00	1000.00	0.00
L2	DEFAULT	5.00	0.00	4.00	1000.00	0.00
L3	DEFAULT	5.00	0.00	4.00	1000.00	0.00

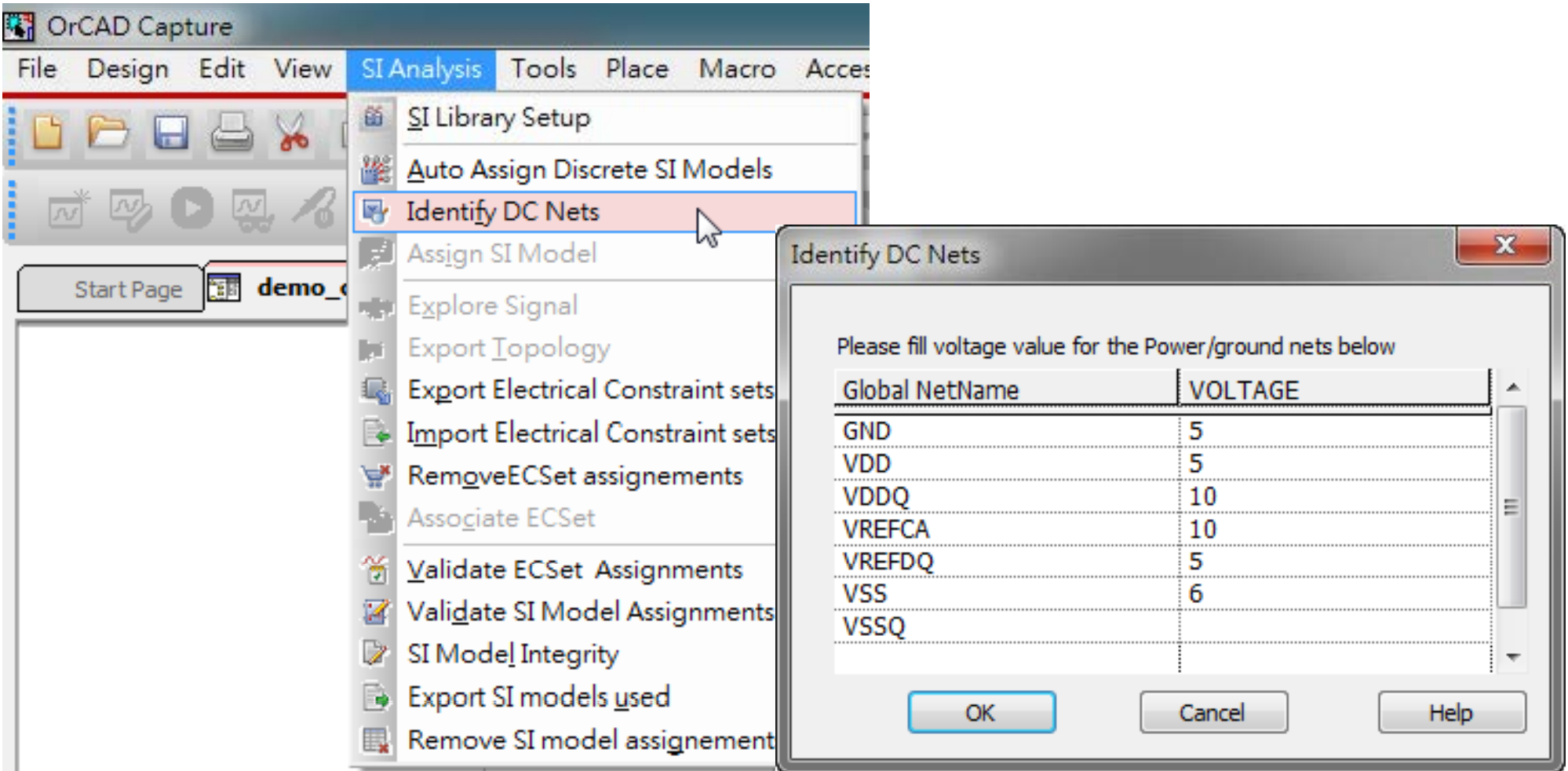
### Audit / Refine Topology & Constraints

# OrCAD SI Analysis Features in 16.6



# Environment Setup

## DC Net Power Value Assignment

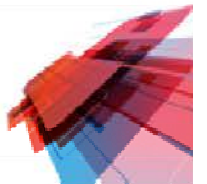


The screenshot shows the OrCAD Capture interface with the SI Analysis menu open. The 'Identify DC Nets' option is selected. A dialog box titled 'Identify DC Nets' is displayed, containing a table for assigning voltage values to power/ground nets.

Please fill voltage value for the Power/ground nets below

Global NetName	VOLTAGE
GND	5
VDD	5
VDDQ	10
VREFCA	10
VREFDQ	5
VSS	6
VSSQ	

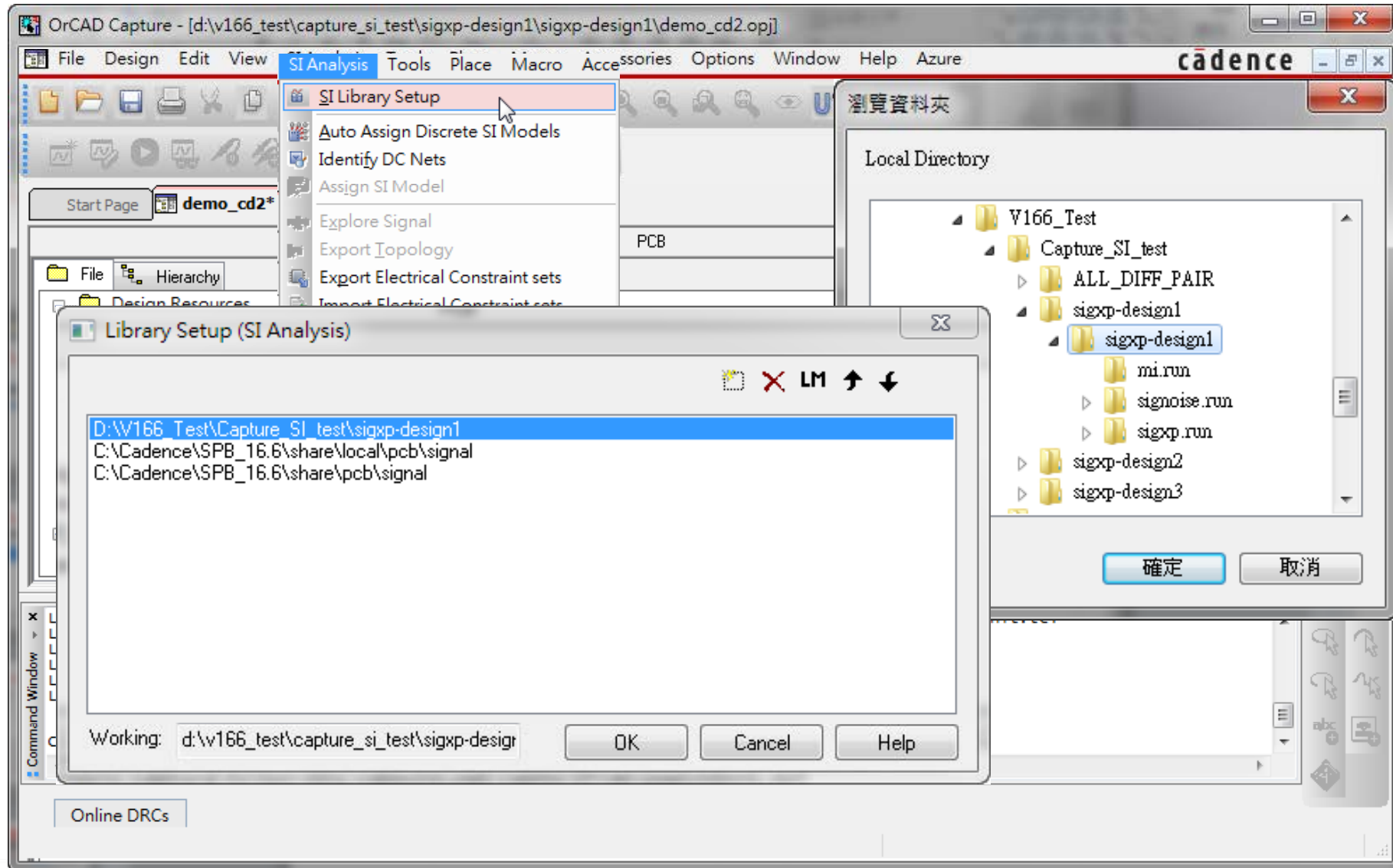
Buttons: OK, Cancel, Help





# Environment Setup

## SI Model Library Path Setup

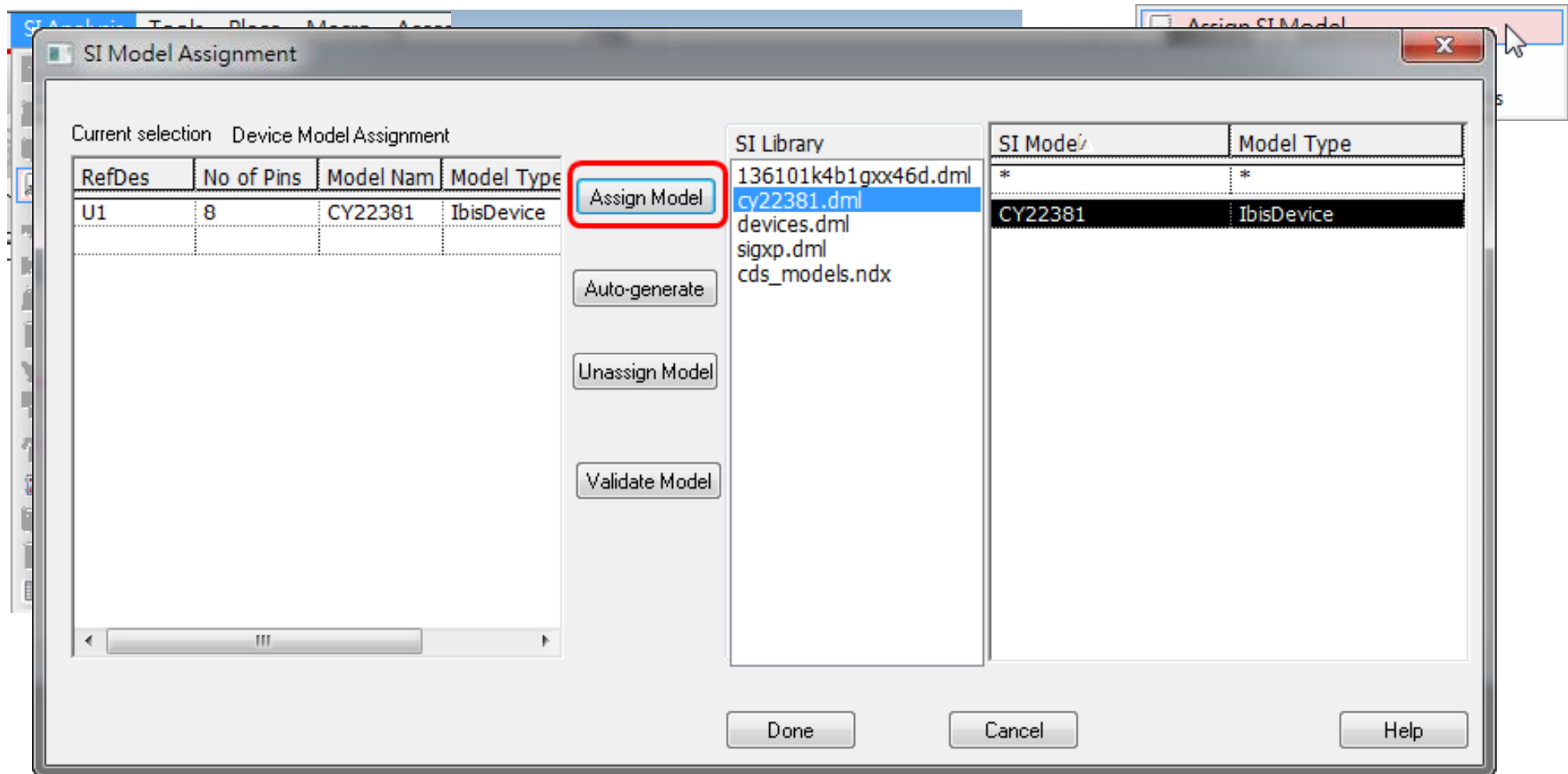


# Environment Setup

## SI Model Assignment

Pull Down Menu

RMB Menu



# Environment Setup

## Auto Model Assignment for Discrete parts

OrCAD Capture

File Design Edit View **SI Analysis** Tools Place Macro Access

SI Library Setup  
Auto Assign Discrete SI Models  
Identify DC Nets

SI Model Assignment

Current selection Device Model Assignment

RefDes	No of Pins	Model Nam	Model Type
R1	2	DEFAULT_	ESpiceDevi
R2	2	DEFAULT_	ESpiceDevi

Assign Model

Auto-generate

Unassign Model

Validate Model

SI Library

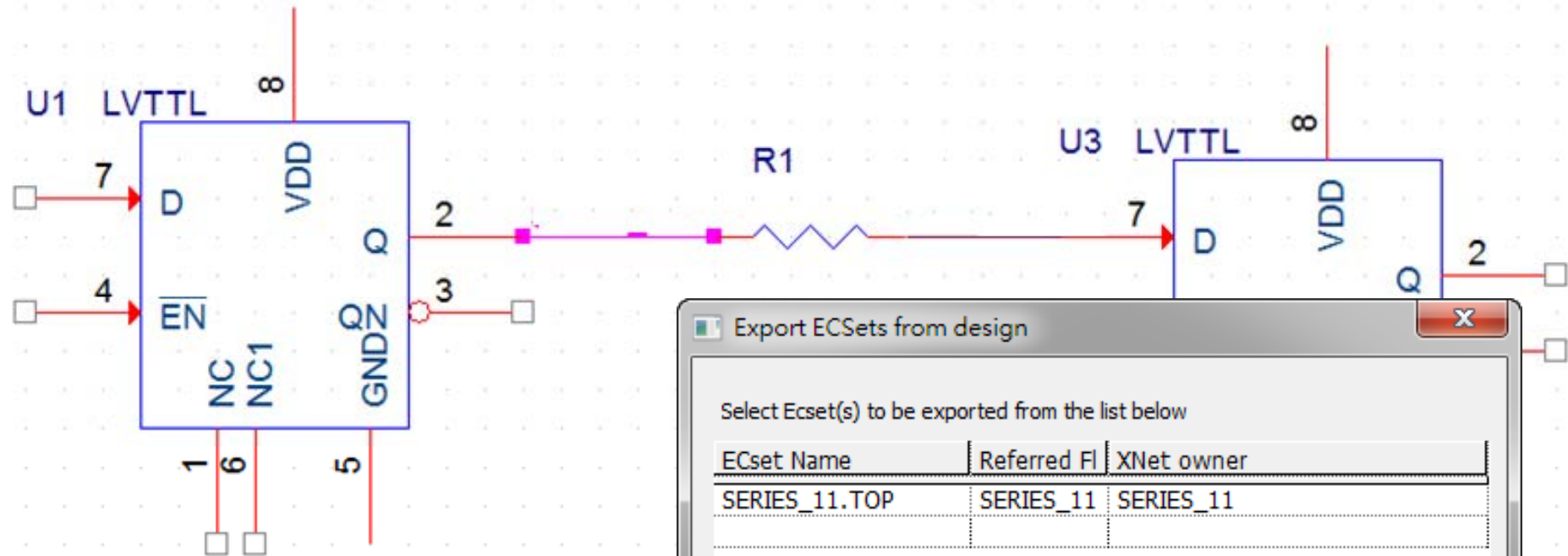
- 136101k4b1gxx46d.dml
- cy22381.dml
- devices.dml
- sigxp.dml
- cds\_models.ndx

SI Model	Model Type
*	*
4Port	ESpiceDevice
C20p_withpkg	ESpiceDevice
cable_espice	ESpiceDevice
capacitor20pF	ESpiceDevice
CDS_lvds_device	IbisDevice
CDS_PCIX_device	IbisDevice
CDS_Pkg14DIP_Ckt_M	PackageModel
CDS_Pkg14DIP_Ckt	PackageModel
CDS_Pkg14DIP_Sparam	PackageModel
CDS_Pkg14DIP_Sparse	PackageModel
CDS_Pkg14DIP	PackageModel
CDS_Pkg16DIP	PackageModel
CY22381	IbisDevice
DEFAULT_RESISTOR_1	ESpiceDevice
DEFAULT_RESISTOR_2	ESpiceDevice
DEFAULT_RESISTOR_4	ESpiceDevice
DEFAULT_RESISTOR_1	ESpiceDevice
DEFAULT_RESISTOR_P	ESpiceDevice

Done Cancel Help



# Xnet Generation Solution



Export ECsets from design

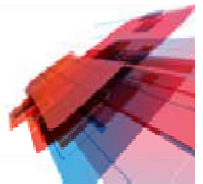
Select Ecset(s) to be exported from the list below

ECset Name	Referred FI	XNet owner
SERIES_11.TOP	SERIES_11	SERIES_11

Export Directory  ...

Remove unused ecsets

Validate Ecset Export Cancel Help



# Extract Topology

## Extract Signal Net Topology

The image illustrates the process of extracting signal net topology in OrCAD PCB SI. It shows a schematic of two LVTTL buffers (U1 and U3) connected via a resistor (R1). A context menu is open over the schematic, with the 'Signal Integrity' option expanded, and 'Explore Signal' selected. The right side of the image shows a detailed signal path diagram with components like TRISTATE, MICRSTRIP, and a resistor.

U1 LVTTL 8  
7 D VDD  
4 EN NC NC1  
1 6 5 GNDZ Q  
2 3  
R1  
11  
U3 LVTTL ∞

SigXplorer OrCAD PCB SI: SERIES\_11.TOP 1.0 Project: d:/sigxp-design1  
File Edit View Setup Analyze Help

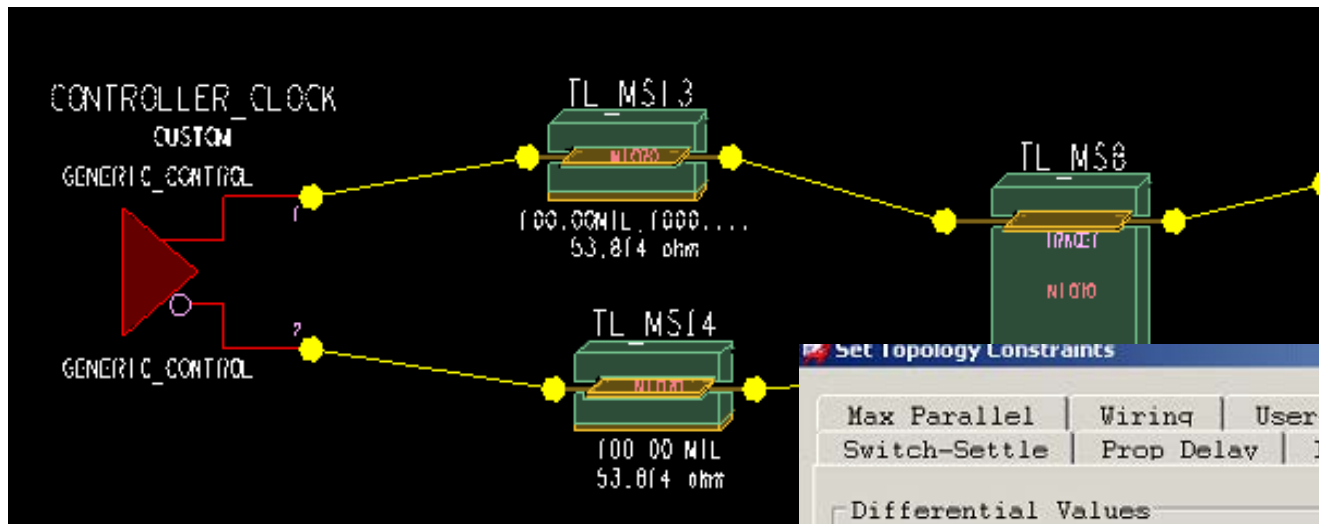
Mirror Horizontally  
Mirror Vertically  
Mirror Both  
Rotate  
Edit Properties...  
Select Entire Net  
Edit Wire Properties  
Edit Net Properties  
Connect to Bus  
Signal Integrity  
Assign Power Pins  
Ascend Hierarchy  
Selection Filter  
Fisheye view

Explore Signal  
Export Topology  
Associate ECSet  
Validate ECSet Assignments  
Remove ECSet assignments

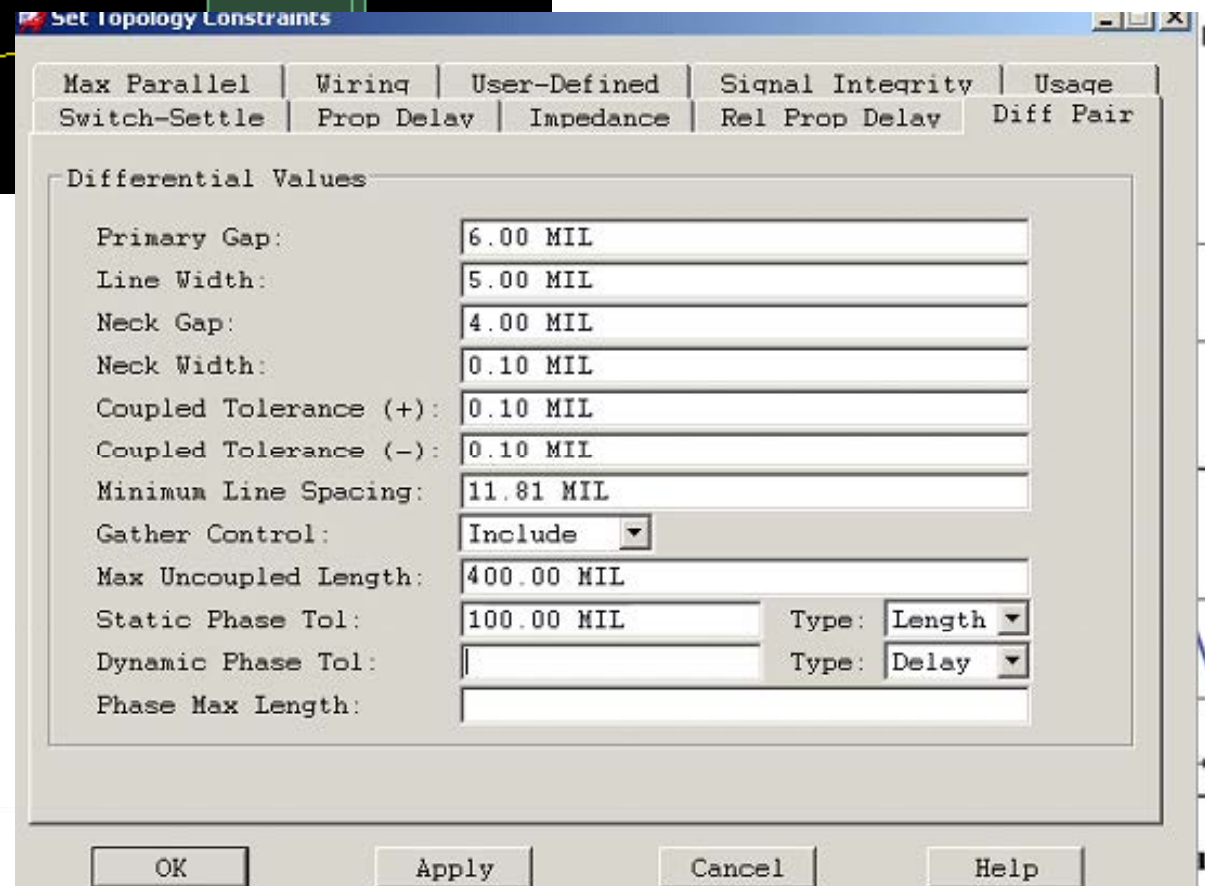
U1 TRISTATE  
TL2 MICRSTRIP 60 ohm 0.5 ns  
R1 1 Ohm  
TL1 MICRSTRIP 60 ohm 0.5 ns  
U3 TRISTATE  
CDSDefaultOutput...  
CDSDefaultInput...



# Differential

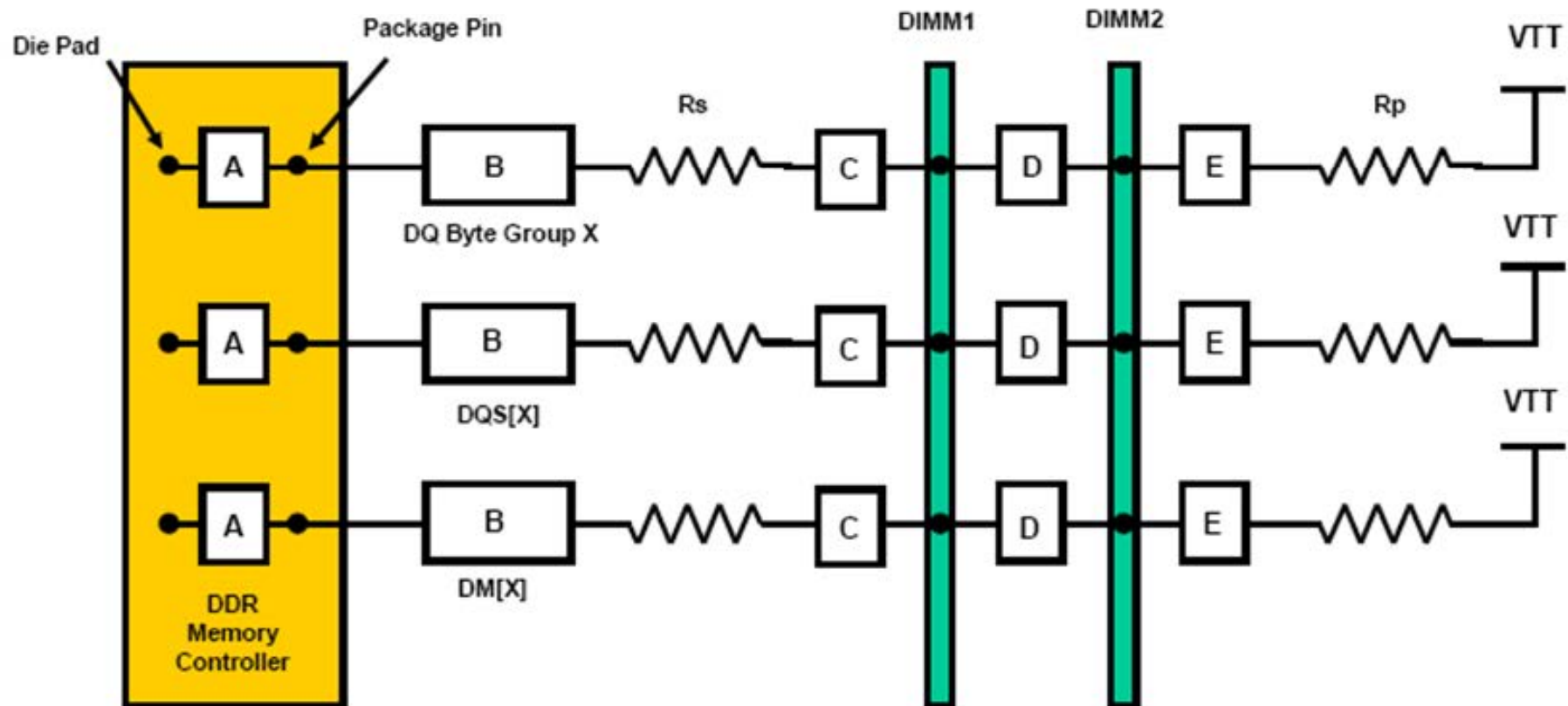


- Max uncoupled parallel length
- Max Static phase



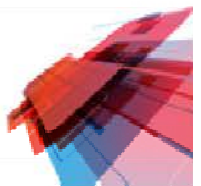
# Data Byte Lane Topology

## Data Byte Lane Topology – Statix Board



# Data Group Routing Rules

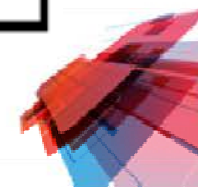
Parameter	Min	Typical	Max
A	Obtain from controller vendor		
B	2.0 inches		3.0 inches
C	0.5 inches		1.0 inches
D	0.2 inches		0.6 inches
Total Length (A + B+ C)	3.0 inches		4.6 inches
Trace Impedance	45 ohms	50 ohms	55 ohms
Trace Width		5 MIL	
Trace Space (A, B, C, D)		15 MIL	
Trace Spacing from DIMM pins		7 MIL	
Trace Spacing from other signal groups		20 MIL	
Length Matching for Data in the Byte Lane		+/- 100 MIL	
Length Matching Byte Lane to Byte Lane	+/- 0.5 inches of clock length		
Termination Voltage	1.00 V	1.25 V	1.50 V



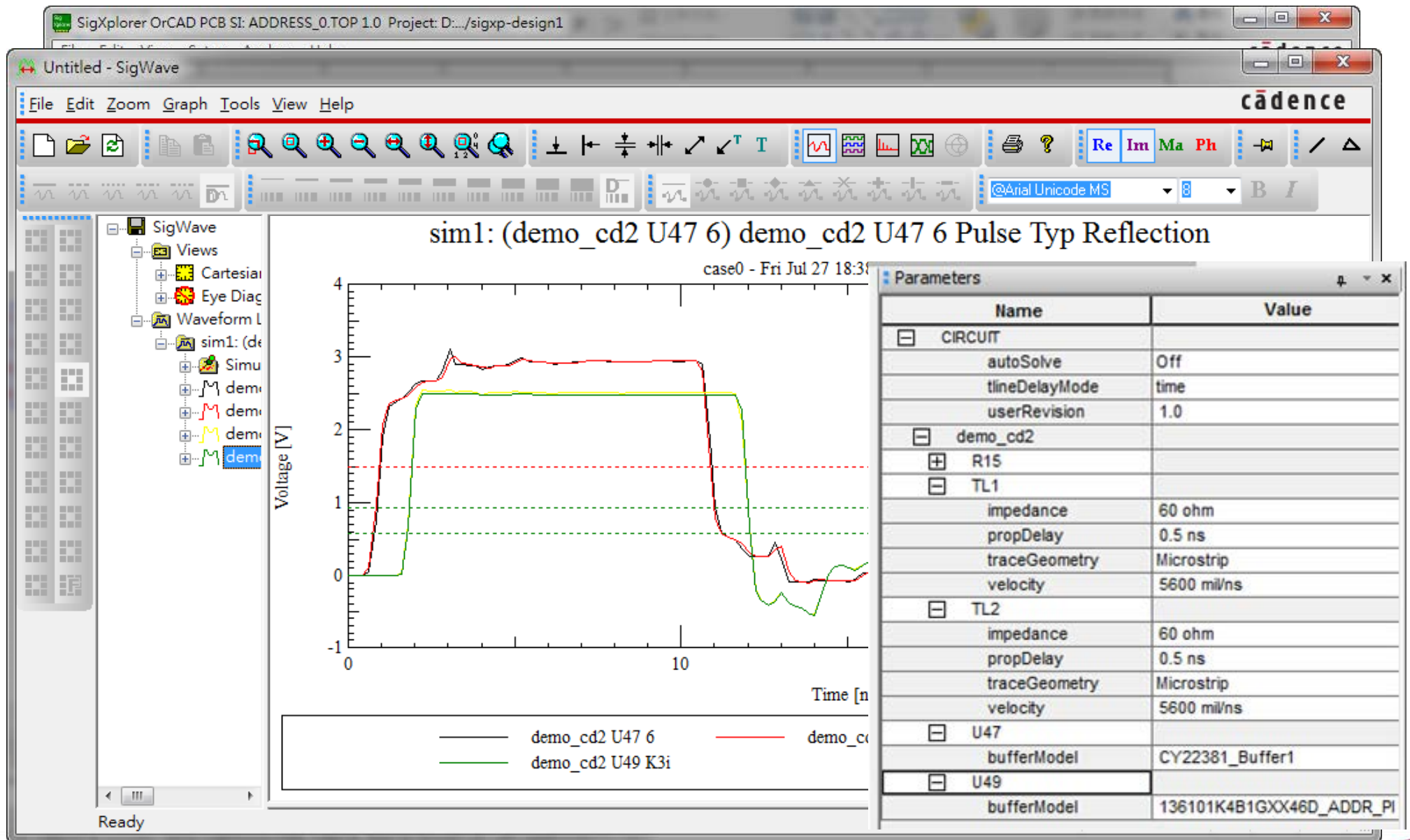


# Variance Table of Design Requirements

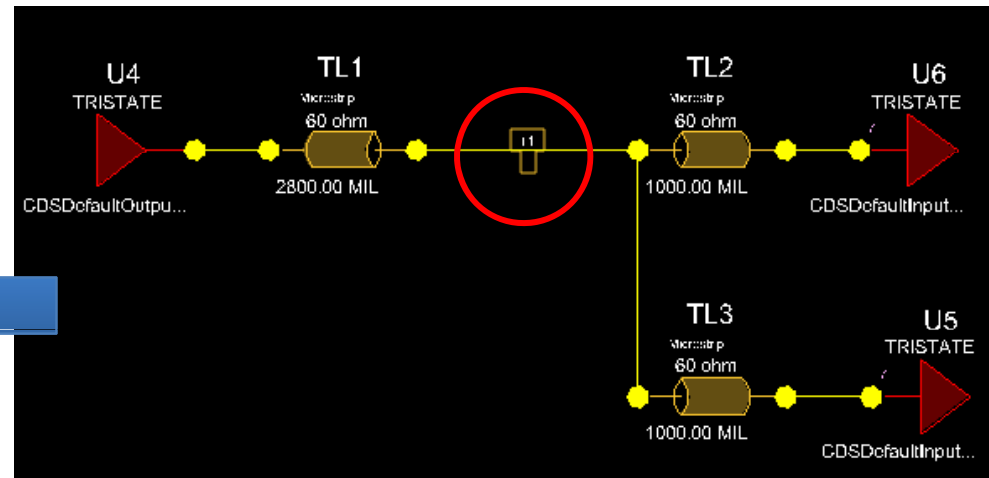
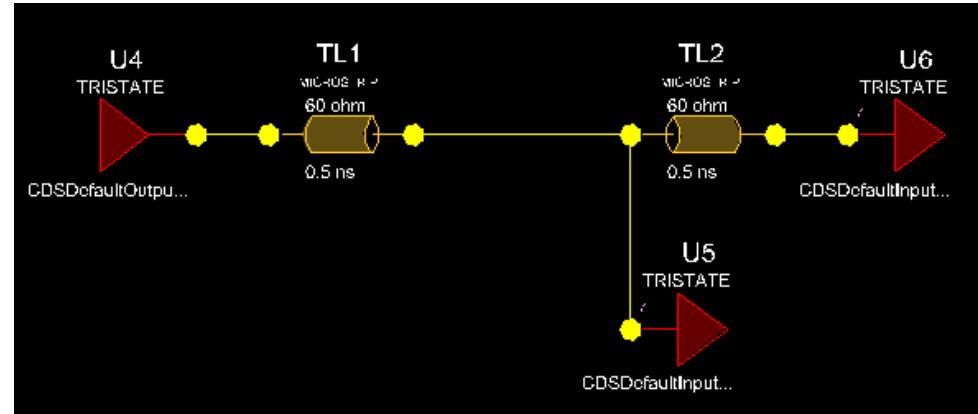
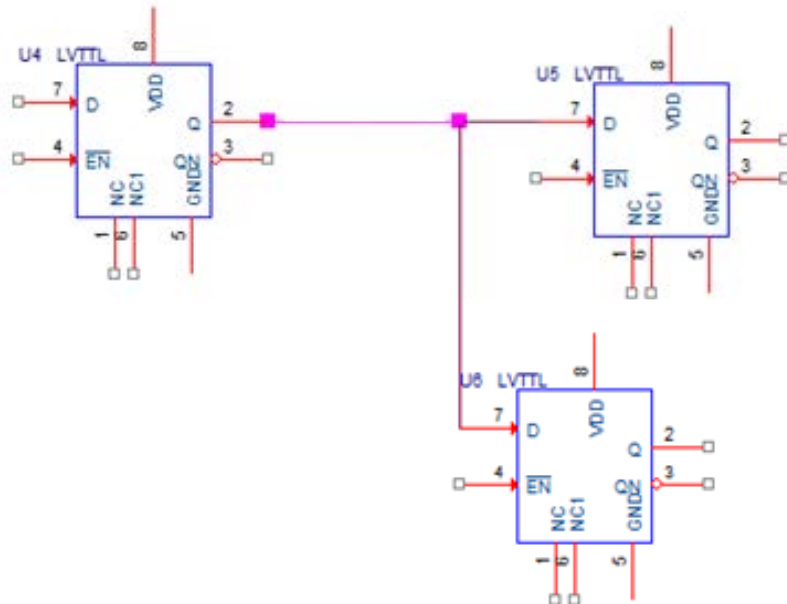
Parameter	Min	Typical	Max	# Sims
FPGA Memory Controller (U7)	Fast		Slow	2
TL1 Impedance	45 ohms	50 ohms	55 ohms	3
TL1 Velocity (microstrip)	5400 MIL/ns	5600 MIL/ns	5800 MIL/ns	3
TL1 Length (equates to D)	200 MIL	400 MIL	600 MIL	3
TL2 Impedance	45 ohms	50 ohms	55 ohms	3
TL2 Velocity (microstrip)	5400 MIL/ns	5600 MIL/ns	5800 MIL/ns	3
TL2 Length (equates to C)	500 MIL	7500 MIL	1000 MIL	3
TL3 Impedance (microstrip)	45 ohms	50 ohms	55 ohms	3
TL3 Velocity	5400 MIL/ns	5600 MIL/ns	5800 MIL/ns	3
TL3 Length (equates to B)	2000 MIL	2150 MIL	3000 MIL	3
RN11 Resistance	9 ohms	10 ohms	11 ohms	3
R32 Resistance	49 ohms	56 ohms	62 ohms	3
Termination Voltage	1.00 V	1.25 V	1.50 V	3
Total Number of Sweep Simulations				3,188,646



# Signal Integrity Simulation



# Define Constraints in OrCAD SigXpolor



Set Topology Constraints

Max Parallel	Wiring	User-Defined	Signal Integrity	Usage
Switch-Settle	Prop Delay	Impedance	Rel Prop Delay	Diff Pair

Existing Rules

From	To	Rule-Type	Min-Delay	Max-Delay
T.1	U5.7	LENGTH	1000.00 mil	1050.00 mil
T.1	U6.7	LENGTH	1000.00 mil	1050.00 mil
U4.2	T.1	LENGTH	2800.00 mil	2850.00 mil

Pins/Tees

Name	Usage
ALL DRVRS/RCVRS	
DRIVER/RECEIVER	
LONGEST/SHORTEST	
T.1	TEE
U4.2	OUT
U5.7	IN
U6.7	IN

Rule Editing

From:

To:

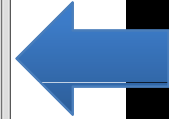
Rule Type: Length

Min Delay:

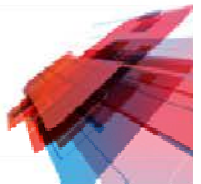
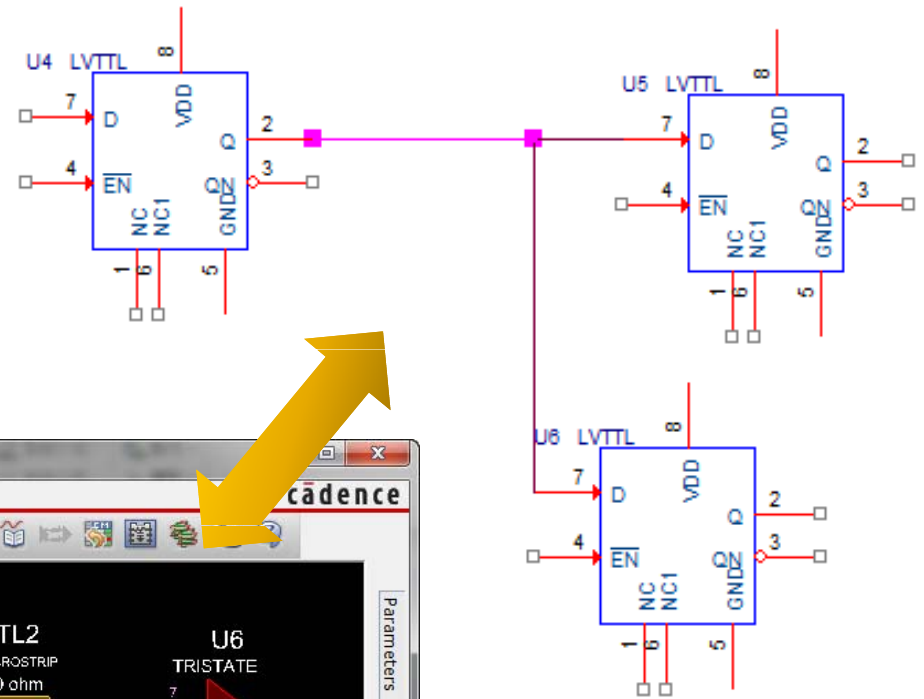
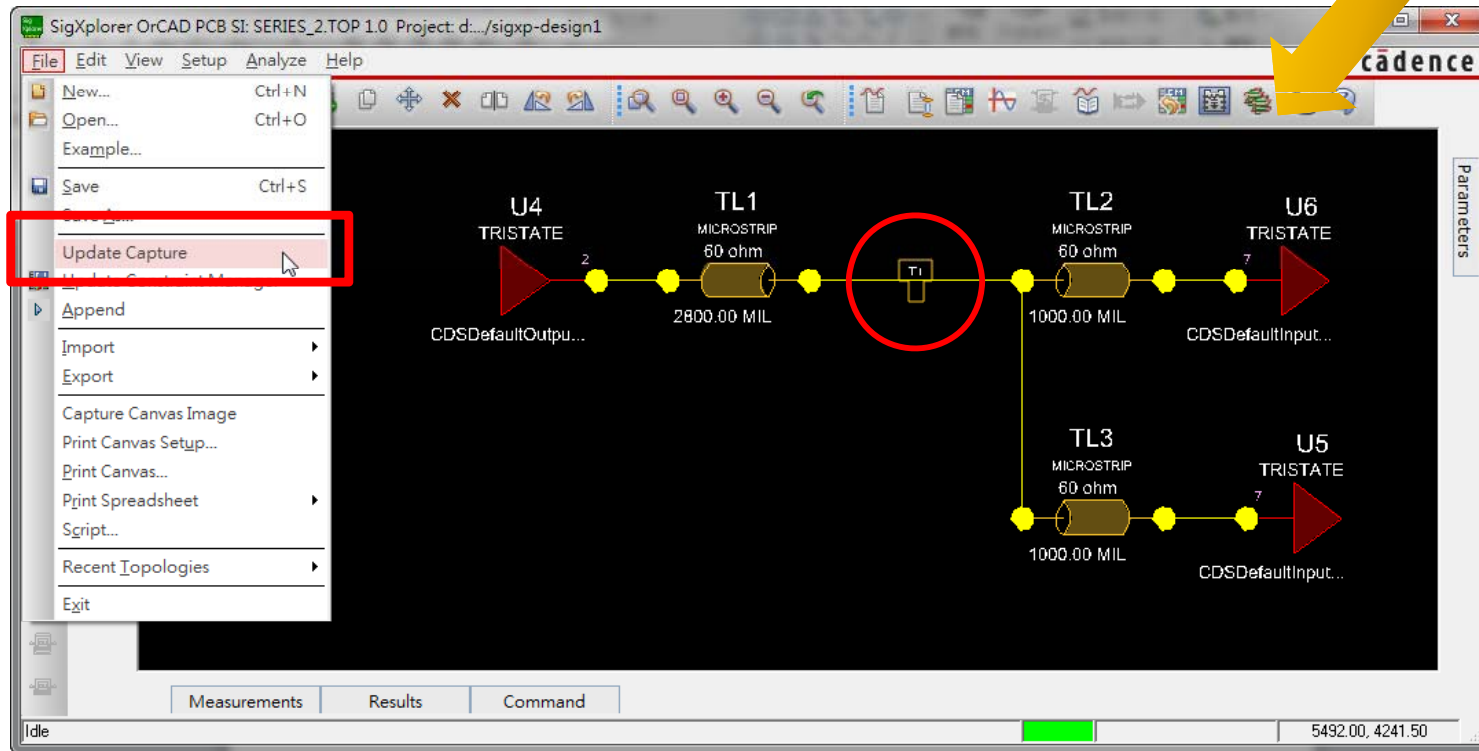
Max Delay:

Buttons: Add, Modify, Delete

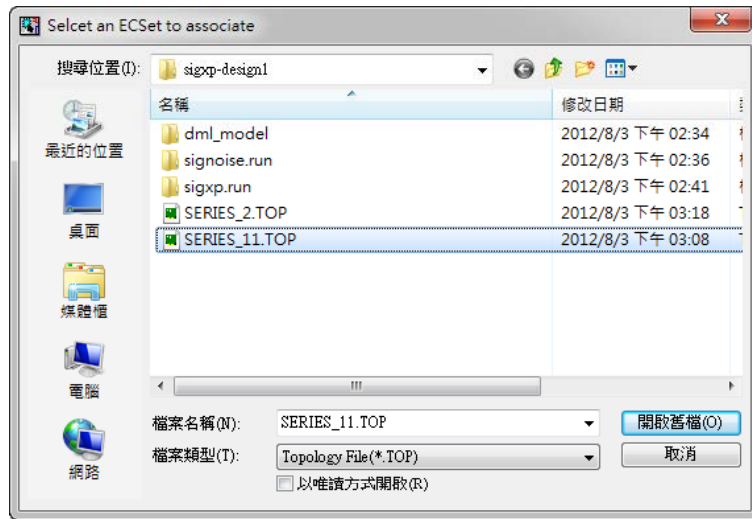
Buttons: OK, Apply, Cancel, Help



# Update Capture



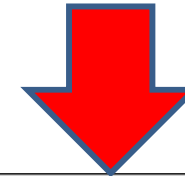
# Replicate ECSet



Object ID	Net Name	Page	Page Number	Sc
Series_1(...)	SERIES_1	02_S...	3	
Series_2(...)	SERIES_2	02_S...	3	
Series_11(...)	SERIES_11	02_S...	3	
Series_ap...	SERIES_A...	02_S...	3	
Series_ap...	SERIES_A...	02_S...	3	
U5/5(Part...	GND	02_S...	3	SI
U5/8(Part...	VDD	02_S...	3	SI

Context menu options:

- Edit Properties (Ctrl+Shift+E)
- Save as HTML
- Save as CSV
- Assign SI Model



- Auto create ECSet
- Easy use to other net

	Line Style	Line Width	Name	Color	ELECTRICAL_CONSTRAINT_SET
1	Default	Default	SERIES_1	Default	
2	Default	Default	SERIES_2	Default	SERIES_2
3	Default	Default	SERIES_11	Default	SERIES_11
4	Default	Default	SERIES_APPLY_1	Default	
5	Default	Default	SERIES_APPLY_11	Default	SERIES_11



# Netin to OrCAD PCB

Worksheet selector

Electrical

- Electrical Constraint Set
  - Signal Integrity
  - Timing
  - Routing
    - Wiring
    - Vias
    - Impedance
    - Min/Max Propagation Delay
    - Total Etch Length
    - Differential Pair
    - Relative Propagation Delay
- All Constraints

DEMO\_CD2

Objects		Pin Pairs	Min Delay	Max Delay
Type	Name		ns	ns
*	*	*	*	*
Dsn	DEMO_CD2			
ECS	SERIES_2			

Net

- Signal Integrity
- Timing
- Routing
  - Wiring
  - Vias
  - Impedance
  - Min/Max Propagation Delay
  - Total Etch Length
  - Differential Pair
  - Relative Propagation Delay

XNet	ADDRESS_10				
XNet	ADDRESS_11				
XNet	ADDRESS_12				
XNet	ADDRESS_13				
XNet	DATA_0				
XNet	DATA_1				
XNet	DATA_2				
Net	MODEL_DIFF_01				
Net	MODEL_DIFF_02				
XNet	SERIES_APPLY_11				
XNet	SERIES_BE_APPLY_11				
Net	SERIES_2	SERIES_2			
XNet	SERIES_11				



# Import EC Sets From Constraint Manager

The screenshot shows the 'DEMO\_CD2' worksheet in the Constraint Manager. The left sidebar shows a tree view under 'Electrical' with 'Electrical Constraint Set' expanded, containing 'Signal Integrity', 'Timing', 'Routing', 'Wiring', 'Vias', 'Impedance', and 'Min/Max Propagation Delay'. The main table displays the following data:

Objects		Pin Pairs	Min Delay	Max Delay
Type	Name		ns	ns
*	*	*	*	*
Dsn	DEMO_CD2			
ECS	SERIES_2			
ECSP	NET.T.1:U5.7		1000 mil	1050 mil
ECSP	NET.T.1:U6.7		1000 mil	1050 mil
ECSP	U4.2:NET.T.1		2800 mil	2850 mil

The screenshot shows the 'Physical' constraint manager interface. The left sidebar shows a tree view under 'Net' with 'Signal Integrity', 'Timing', 'Routing', 'Wiring', 'Vias', 'Impedance', 'Min/Max Propagation Delay', 'Total Etch Length', 'Differential Pair', and 'Relative Propagation Delay'. The main table displays the following data:

XNet	ADDRESS_10									
XNet	ADDRESS_11									
XNet	ADDRESS_12									
XNet	ADDRESS_13									
XNet	DATA_0									
XNet	DATA_1									
XNet	DATA_2									
Net	MODEL_DIFF_01									
Net	MODEL_DIFF_02									
XNet	SERIES_APPLY_11									
XNet	SERIES_BE_APPLY_11									
Net	SERIES_2	SERIES_2								50 MIL
PPr	SERIES_2.T.1:U5.7				1000.0...			1050.0...	100.0...	950 MIL
PPr	SERIES_2.T.1:U6.7				1000.0...			1050.0...	1000.0...	50 MIL
PPr	U4.2:SERIES_2.T.1				2800.0...			2850.0...	1100.0...	1750 ...



# Exploring Signal from OrCAD Capture

DSN  
\*.TOP

Topology Embedded in DSN file  
From Processor =>

Color	CLK_DDR2_0_N
DIFFERENTIAL_PAIR	Default
ELECTRICAL_CONSTRAINT_SET	CLK_DDR2_0_N
Is Global	<input type="checkbox"/>
Line Style	Default
Line Width	Default
Net ID	18444
Net Name	CLK_DDR2_0_N

DDR

Explore Signal  
Export Topology  
Associate Electrical Cset

A single mouse click makes you ready for SI Analysis

U1 TRISTATE  
CDSDefaultOutput...

TL3 Microstrip 60 ohm 0.5 ns

U101 TRISTATE  
CDSDefaultInput...

TL4 Microstrip 60 ohm 0.5 ns

R1 100 Ohm

TL2 Microstrip 60 ohm 0.5 ns

U1 TRISTATE  
CDSDefaultOutput...

TL Microstrip 60 ohm 0.5 ns

SigXplorer OrCAD PCB SI: CLK\_DDR2\_0\_N

File Edit View Setup Analyze

New... Ctrl+N  
Open... Ctrl+O  
Example...  
Save Ctrl+S  
Save As...

Update Capture

Signal Integrity	Usage
Rel Prop Delay	Diff Pair
Delta	Tolerance
CAL	0 ns 5 ns
CAL	5 ns 5 ns

Rule Editing

Rule Name: CLK\_DDR2\_0\_N\_M1

From: U1.U1  
To: U101.N8  
Scope: Local  
Delta Type: Delay  
Delta: 0 ns  
Iol Type: Delay  
Tolerance: 5 ns

Buttons: Add, Modify, Delete, OK, Apply, Cancel, Help





# OrCAD Capture Apps GraserWARE FrontendPack



# GraserWARE FrontendPack

- Replace BUS Alias
- Import/Export Properties
- Design Compare
- Reference Edit

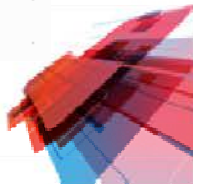


# Replace BUS Alias

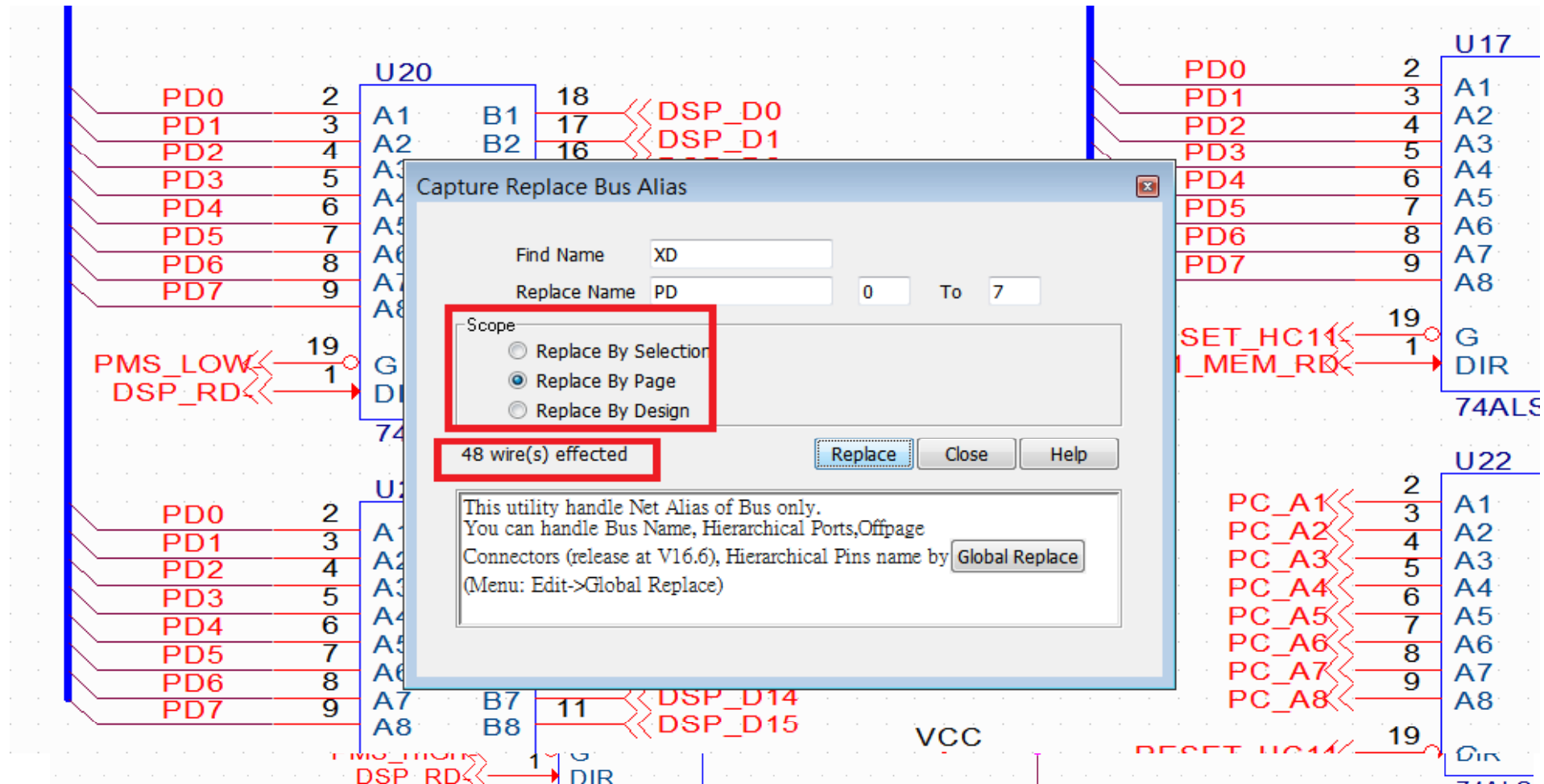
- Replace Bus alias
  - By Selection
  - By Page
  - By Design

The screenshot displays a schematic diagram on the left and a dialog box on the right. The schematic shows a bus alias replacement operation. On the left, a vertical list of bus aliases is shown: BMS RD (45), BMS WR (44), A0 (21), A1 (22), A2 (23), A3 (24), A4 (27), A5 (28), A6 (30), A7 (31), A8 (32), A9 (33), A10 (34), A11 (35), A12 (36), and A13 (36). These are connected to a central bus labeled DSP\_D[0..13]. On the right, a dialog box titled 'Capture Replace Bus Alias' is open. It has a 'Find Name' field containing 'DSP\_A' and a 'Replace Name' field containing 'DSP\_D'. The 'Scope' section has three radio buttons: 'Replace By Selection' (selected), 'Replace By Page', and 'Replace By Design'. Below the radio buttons, a status bar indicates '14 wire(s) effected'. At the bottom of the dialog, there are 'Replace', 'Close', and 'Help' buttons. A text box at the bottom of the dialog contains the following text: 'This utility handle Net Alias of Bus only. You can handle Bus Name, Hierarchical Ports, Offpage Connectors (release at V16.6), Hierarchical Pins name by Global Replace (Menu: Edit->Global Replace)'. The background schematic shows a blue bus line labeled DSP\_D[0..13] connecting to various components. A red arrow points from the bus name in the schematic to the 'Find Name' field in the dialog. Another red arrow points from the bus name in the schematic to the 'Replace Name' field in the dialog.

Bus Alias	Pin Number	Component Name
BMS RD	45	BMS-
BMS WR	44	DSP_RD- DSP_WR-
A0	21	DSP_D0
A1	22	DSP_D1
A2	23	DSP_D2
A3	24	DSP_D3
A4	25	DSP_D4
A5	27	DSP_D5
A6	28	DSP_D6
A7	30	DSP_D7
A8	31	DSP_D8
A9	32	DSP_D9
A10	33	DSP_D10
A11	34	DSP_D11
A12	35	DSP_D12
A13	36	DSP_D13



# Replace BUS Alias



# Import/Export Properties

## Export Design Properties to Excel

The screenshot shows the 'Import & Export Property V1.0' dialog box with the 'Export' tab selected. The design path is 'D:\TestDSN\com\_pare\BENCH\_ALLEGRO\_NEW.DSN'. The 'Mode' is set to 'Instance' and the 'Scope' is 'BENCH\_ALLEGRO\_NEW'. The 'Template' is 'C:\Program Files (x86)\GraserWARE\FrontendPack\graser.tpr'. The 'Property Editor' window is open, showing a list of properties. The spreadsheet below shows the following data:

	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Design	D:\TestDSN\com_pare\BENCH_ALLEGRO_NEW.DSN											
2	HEADER	ID	Page	Name	Part Reference	PCB Footprint	Value	Part Number	Tolerance	Description			
3	PARTINST:BE	3338083398:U9	A	I-956883898	U9	dip16_3	74ALS138	20-00045		IC, 74ALS138, multiplexer, Standard input, Inverted, totem ouput			
4	PARTINST:BE	3338083401:U8	A	I-956883895	U8	dip20_3	74ALS273	20-81432		IC, 74ALS273 OCTAL D POS EDGE TRIGG 20 DIP			
5	PARTINST:BE	3338083402:U10	A	I-956883894	U10	dip20_3	74ALS245	20-003297		IC, 74ALS245 (N)OCTL TRI-ST TRANSCVR 20DIP			
6	PARTINST:BE	3338083403:D1	A	I-956883893	D1	SMDLED	RA-LED	40-00017		LED Red			
7	PARTINST:BE	3338083404:U11	A	I-956883892	U11	plcc28	22V10	20-00033		Bipolar PLD Device			
8	PARTINST:BE	3338083405:U6	A	I-956883891	U6	dip16_3	7201	20-00042		FIFO Status Flag Expandable 512x9			
9	PARTINST:BE	3338083406:U3	A	I-956883890	U3	dip16_3	7201	20-00042		FIFO Status Flag Expandable 512x9			
10	PARTINST:BE	3338083407:U5	A	I-956883889	U5	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
11	PARTINST:BE	3338083408:U2	A	I-956883888	U2	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
12	PARTINST:BE	3338083409:U1	A	I-956883887	U1	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
13	PARTINST:BE	3338083410:U4	A	I-956883886	U4	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
14	PARTINST:BE	3338083411:U7	A	I-956883885	U7	dip20_3	6264	20-00062		CMOS Static RAM 8Kx8			
15	PARTINST:BE	3338083412:TP1	A	I-956883884	TP1	TP20	TESTPOINT	60-00038		Header, 1 row, 1 pin			
16	PARTINST:BE	3338083413:P1	A	I-956883883	P1	headx12x45	HEADER12	60-00037		Header, 2 row x 6 pin			
17	PARTINST:BE	3338083414:R2	A	I-956883882	R2	smdres	100	ERJ-2GEJ101X	5%	Carbon Film Resistor 100 OHM 1/16W 5% 0402 SMD			
18	PARTINST:BE	3338083415:R1	A	I-956883881	R1	smdres	100	ERJ-2GEJ101X	5%	Carbon Film Resistor 100 OHM 1/16W 5% 0402 SMD			
19	PARTINST:BE	3338083416:R3	A	I-956883880	R3	res400	10K	ERJ-8GEYJ103	5%	Carbon Film Resistor 10K OHM 1/8W 5% 1206 SMD			



# Import/Export Properties

## Import Part Properties from Excel to Design

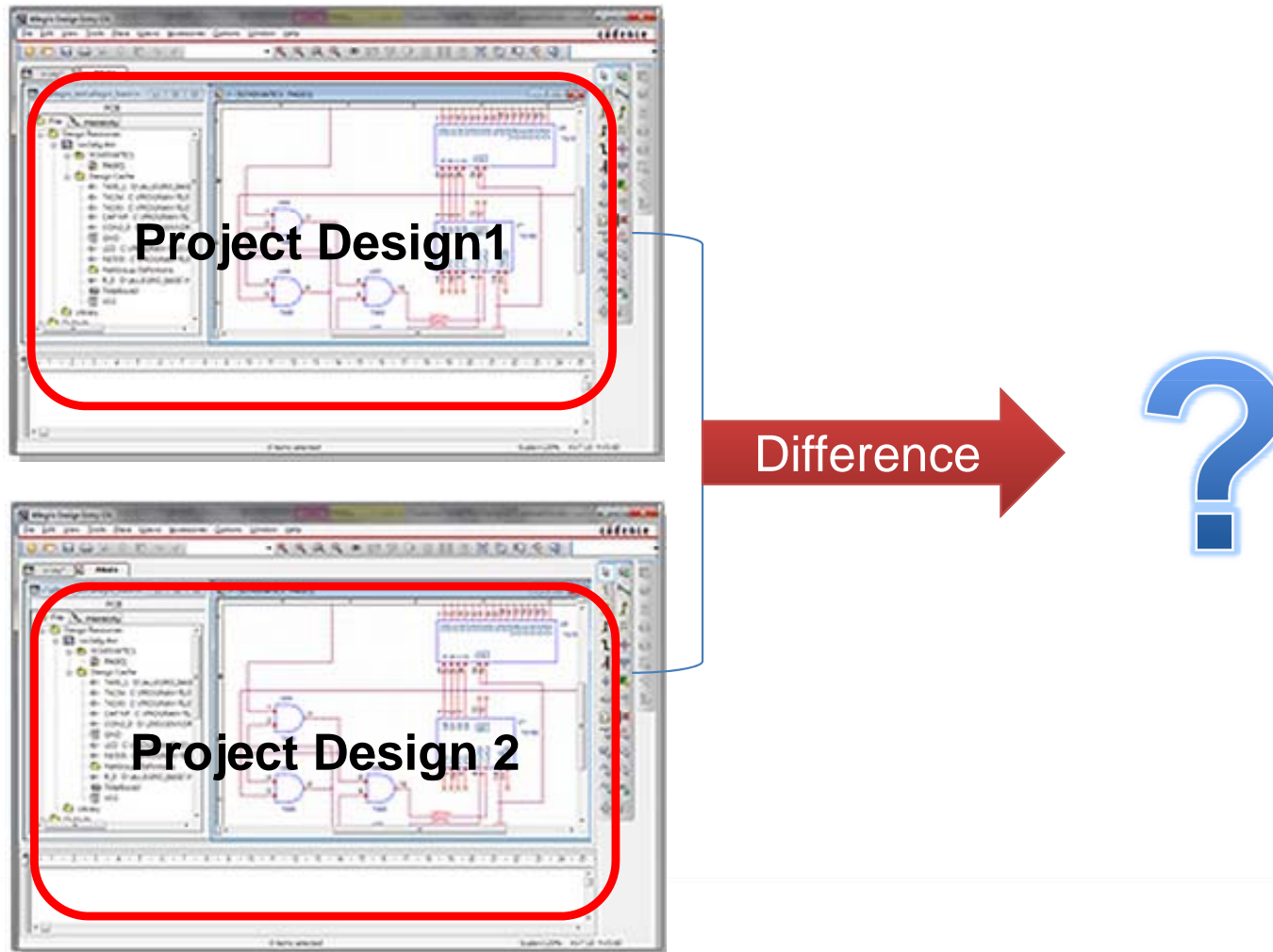
The screenshot shows a PCB design environment with two components: U9 (74ALS138) and U11 (22V10). U9 is a 3-to-8 decoder with inputs A, B, C and outputs Y0-Y7. U11 is a 22V10 PLD with various inputs and outputs. The Property Editor window on the right displays a table of properties for these components, with some cells highlighted in red.

	A	B	C
	BENCH : A : D1	BENCH : A : U9	BENCH : A : U11
Tag			
Color	Default	Default	Default
Description	LED Red	IC, 74ALS138, multi	Bipolar PLD Device
Designator			
Graphic	LED1.Normal	74ALS138.Normal	22V10.Normal
ID			
Implementation	D	74ALS138	
Implementation Path			
Implementation Type	Schematic View	Schematic View	<none>
Location X-Coordinate	1540	710	510
Location Y-Coordinate	850	850	1000
Name	I-956883893	I-956883898	I-956883892
Part Number	40-00017	20-00045	20-00033
Part Reference	D1	U9	U11
PCB Footprint	SMDLED	dip16_3	plcc28
Power Pins Visible	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Primitive	YES	YES	YES
PSpice	D	74ALS138	
Rating	2.0V		
Reference	D1	U9	U11
Source Library	C:WINDOWSIT	C:WINDOWSIT	C:WINDOWSIT
Source Package	LED1	74ALS138	22V10
Source Part	LED1.Normal	74ALS138.Normal	22V10.Normal
Tolerance			
Value	RA-LED	74ALS138	22V10



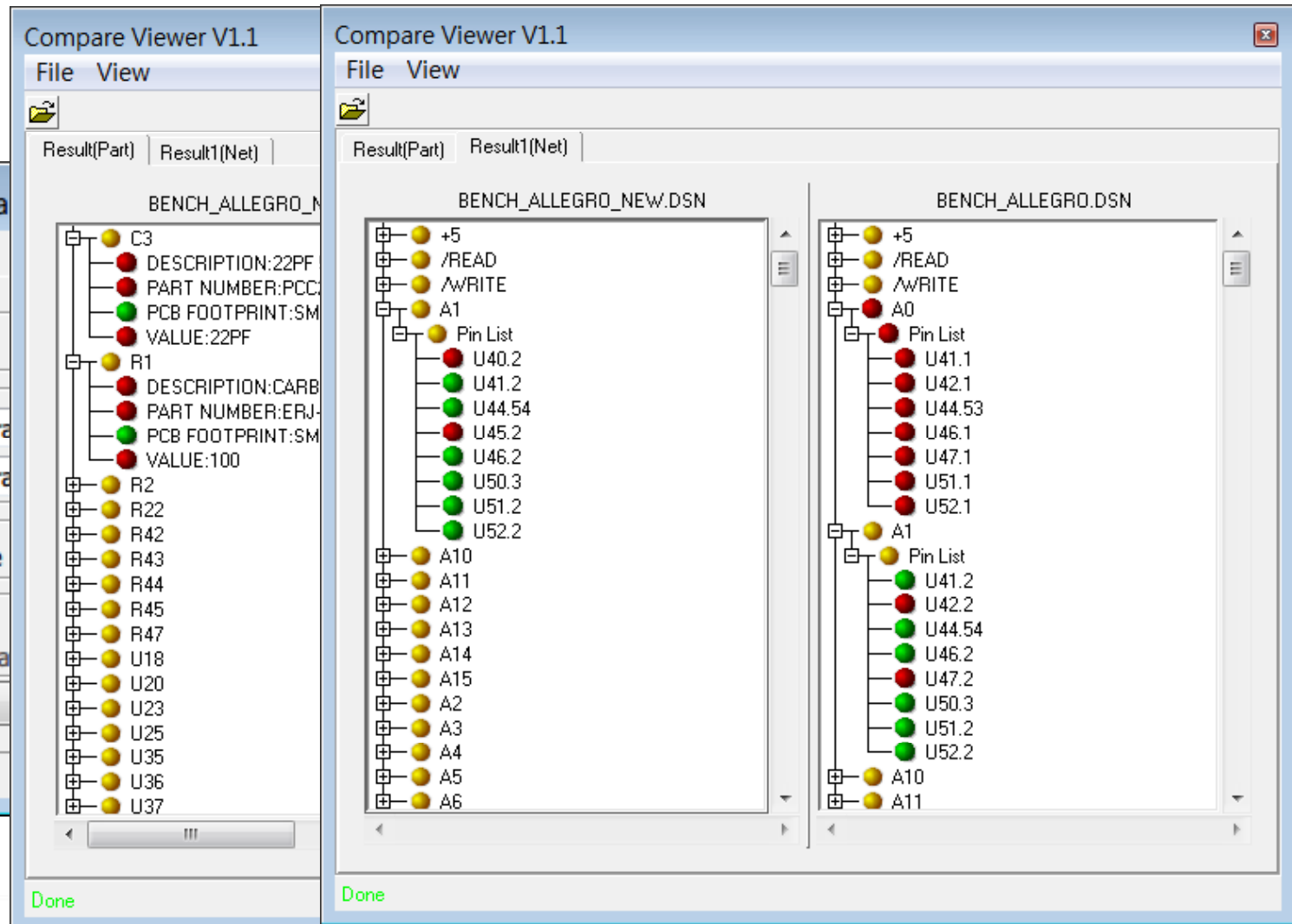
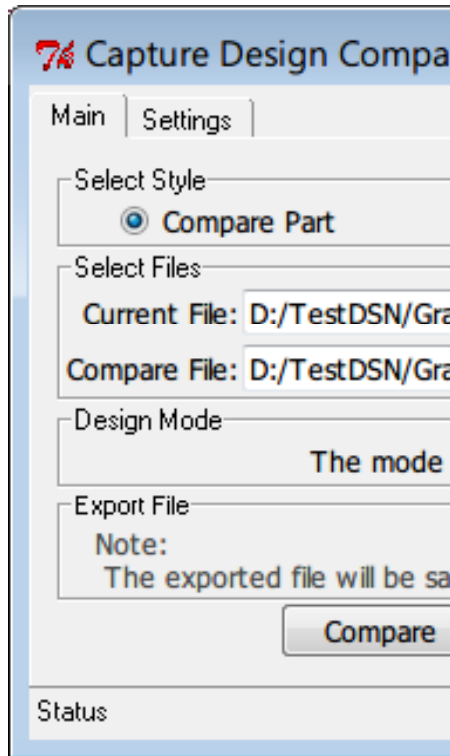
# Capture Design Compare

- Design version1 and version 2
- How do you know which part or Net-list is different??



# Capture Design Compare

- Design Compare
  - By Part
  - By Net
  - Both





# Reference Edit

- Modify RefDes
  - Insert/Delete/Modify Reference Prefix

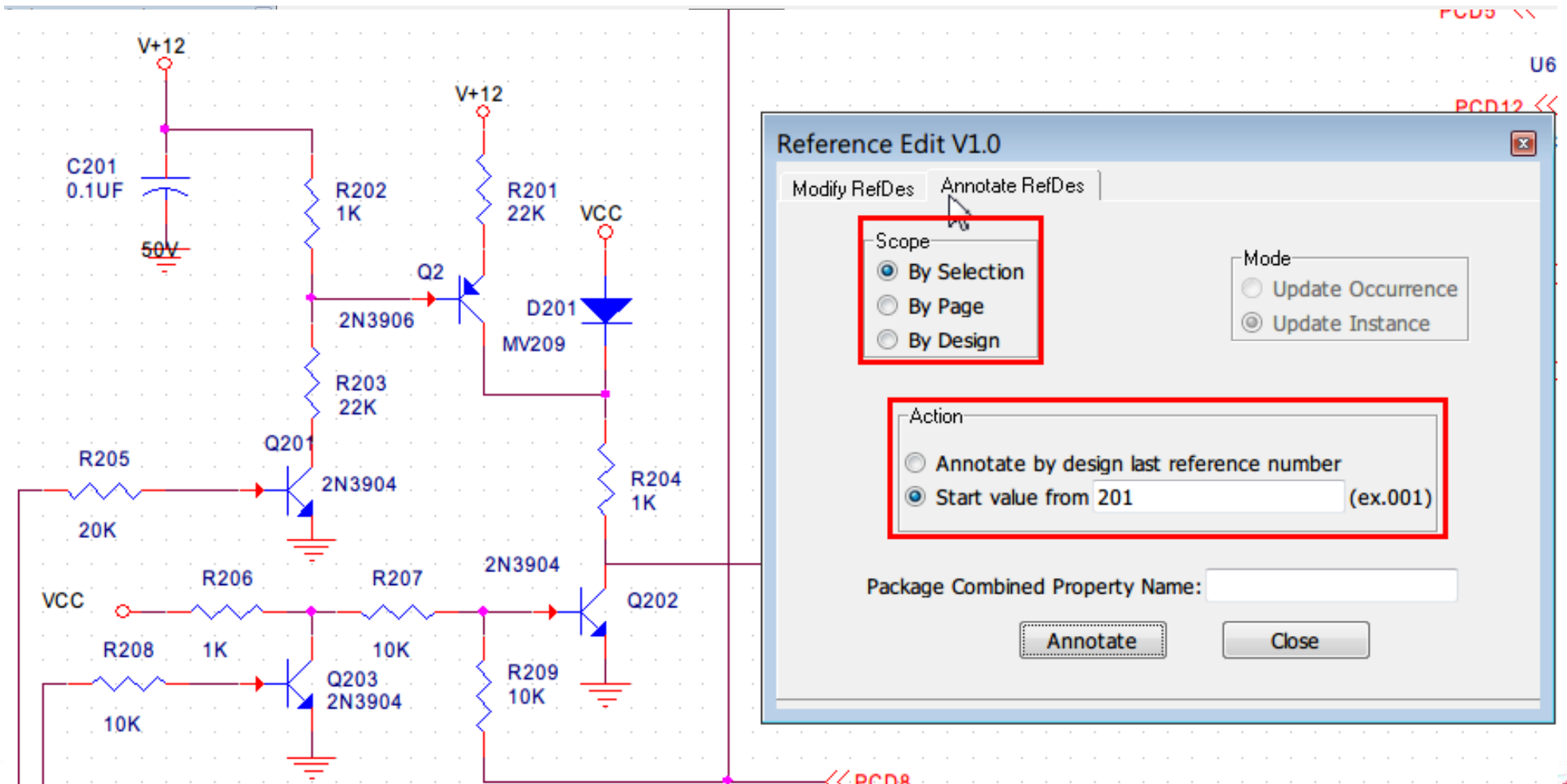
The image displays a PCB layout editor interface. On the left, a grid of components is shown, each consisting of a capacitor symbol connected to a VCC net and a 50V net. The components are labeled CP37 through CP56, all with a value of 0.1UF. A 'Reference Edit V1.0' dialog box is open on the right, showing the 'Modify RefDes' tab. The dialog has the following settings:

- Scope:  By Selection,  By Page,  By Design
- Mode:  Update Occurrence,  Update Instance
- Action: Position  Prefix,  Middle,  Suffix
- RefDes Prefix reset to default:
- Operation:  Insert,  Delete,  Modify
- Operation field: 'P' in a text box, followed by a right arrow and an empty text box.
- Buttons:



# Reference Edit

- Annotate RefDes
  - Annotate Reference by page or selection



# Graser WARE Front-End Pack Roadmap - Part Utility

Is the property editor in Schematic always annoying??

The screenshot displays the OrCAD Capture CIS interface. The main window shows a schematic diagram with components like resistors (R4, R5, R6, R10, R11, R12, R17, R18), capacitors (C6, C11, C16), and operational amplifiers (U14A, U14B, U14C). The Property Editor window is open on the right, showing a table of properties for selected components.

	A	B	C	D
Tag	BENCH : B : C3	BENCH : B : C4	BENCH : B : C5	BENCH : B :
Color	Default	Default	Default	Default
Description	22PF 50V CERAMI	22PF 50V CERAMI	CAP 10UF 50V VS	Default
Designator				
Graphic	SMALL CAP Normal	SMALL CAP Normal	CP Normal	CAP Norma
ID				
Implementation				
Implementation Path				
Implementation Type	<none>	<none>	<none>	<none>
Location X-Coordinate	260	260	1340	550
Location Y-Coordinate	130	170	650	680
Name	I-956883785	I-956883784	I-956883704	I-95688370
Part Number	PCC220CNTR-ND	PCC220CNTR-ND	ECE-V1HA100SP	
Part Reference	C3	C4	C5	C6
PCB Footprint	smdcap	smdcap		
Power				
Power Pins Visible	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Primitive	YES	YES	YES	YES
PSpice	C	C	C	
Rating				
Reference	C3	C4	C5	C6
Source Library	C:WINDOWS\SI	C:WINDOWS\SI	C:WINDOWS\SI	C:WINDOWS\SI
Source Package	SMALL CAP	SMALL CAP	CP	CAP
Source Part	SMALL CAP Norma	SMALL CAP Norma	CP Normal	CAP Norma
Tolerance				
Value	22PF	22PF	10UF	0.1UF
Voltage	50V	50V	50V	



# Graser WARE Front-End Pack Roadmap

## - Part Utility

- Getting Part Information from Part Database
- Check Part Status
  - EOL Part
  - DNI Part
- General BOM File

2nd Part Utility V1.5

Check Part Status

Parts Information

St.	Reference	Value	Part Number	Description	PCB Footprint	Part Approve
1	C1	10PF	PCC100CQTR-ND	CAP 10PF 50V CERAMIC 040	smdcap	YES
2	C2	10PF	PCC100CQTR-ND	CAP 10PF 50V CERAMIC 040	smdcap	YES
3	C3	22PF	PCC220CNTR-ND	22PF 50V CERAMIC CAP 080	smdcap	EOL
4	C4	22PF	PCC220CNTR-ND	22PF 50V CERAMIC CAP 080	smdcap	EOL
5	C5	10UF	ECE-V1HA100SP	CAP 10UF 50V VS ELECT SM		YES
6	C6	10pF	ECG-C0JB100R	CAP 10UF 6.3V CB SERIES S		YES
7	C7	150PF	PCC151CGTR-ND	150PF 50V CERAMIC CAP 08	smdcap	EOD
8	C8	390PF	PCC391BNTR-ND	390PF 50V CERAMIC CAP 08	smdcap	YES
9	C9	820PF	PCC821CGTR-ND	820PF 50V CERAMIC CAP 08	smdcap	
10	C10	10UF	ECE-V1HA100SP	CAP 10UF 50V VS ELECT SM		YES
11	C11	0.1pF	ECE-B1HGE0R1	CAP 50V .1UF NHE AXIAL EL	smdcap	NO
12	C12	150PF	PCC151CGTR-ND	150PF 50V CERAMIC CAP 08	smdcap	EOD
13	C13	390PF	PCC391BNTR-ND	390PF 50V CERAMIC CAP 08	smdcap	YES
14	C14	820PF	PCC821CGTR-ND	820PF 50V CERAMIC CAP 08	smdcap	
15	C15	10UF	ECE-V1HA100SP	CAP 10UF 50V VS ELECT SM		YES
16	C16	0.1UF	ECE-A50ZR1	.1UFD @ 50VDC PANASONIC	C0402	YES
17	C17	150PF	PCC151CGTR-ND	150PF 50V CERAMIC CAP 08	smdcap	EOD

	A	B	C	D	E	F	G	H	I
	Item	Quantity	Part Number	Reference	Description	Manufacturer(DB)	Manufacturer Part Number(DB)	Distributor(DB)	Distributor Part Number(DB)
2	10	6	PCC100CQTR-ND	C1,C2,C20,C21,C22,C2	CAP 10PF 50V CERAM	Panasonic - SCD	ECU-E1H100DCQ	Digi-Key	PCC100CQTR-ND
3	20	9	PCC220CNTR-ND	C3,C4,C24,C25,C26,C22	22PF 50V CERAMIC C	Panasonic - SCD	ECU-V1H220JCN	Digi-Key	PCC220CNTR-ND
4	30	5	ECE-V1HA100SP	C5,C10,C15,C123,C134	CAP 10UF 50V VS ELI	Panasonic - SCD	ECE-V1HA100SP	Digi-Key	PCE3089TR-ND
5	40	6	ECG-C0JB100R	C6,C121,C124,C126,C1	CAP 10UF 6.3V CB SE	Panasonic - SCD	ECG-C0JB100R	Digi-Key	PCS1100BTR-ND
6	50	3	PCC151CGTR-ND	C7,C12,C17	150PF 50V CERAMIC	Panasonic - SCD	ECU-V1H151JCG	Digi-Key	PCC151CGTR-ND
7	60	3	PCC391BNTR-ND	C8,C13,C18	390PF 50V CERAMIC	Panasonic - SCD	ECU-V1H391KBN	Digi-Key	PCC391BNTR-ND
8	70	3	PCC821CGTR-ND	C9,C14,C19	820PF 50V CERAMIC	Panasonic - SCD	ECU-V1H821JCX	Digi-Key	PCC821CGTR-ND
9	80	13	ECE-B1HGE0R1	C11,C39,C43,C44,C46,	CAP 50V .1UF NHE A	Panasonic - SCD	ECE-B1HGE0R1	Digi-Key	P5461-ND
10	90	1	ECE-A50ZR1	C16	.1UFD @ 50VDC PAN.	Panasonic - SCD	ECE-A50ZR1	Digi-Key	P6638-ND
11	100	10	ECE-A1HKK0R1	C29,C41,C51,C55,C61,	CAP ELECT .1UF 50V	Panasonic - SCD	ECE-A1HKK0R1	Digi-Key	P985-ND
12	110	4	ECE-A2AGE100	C32,C36,C118,C119	NHE RADIAL ELECT	Panasonic - SCD	ECE-A2AGE100	Digi-Key	P5297-ND
13	120	1	ECE-V1EA100SR	C33	CAP 10UF 25V VS ELI	Panasonic - SCD	ECE-V1EA100SR	Digi-Key	PCE3067TR-ND
14	130	1	A104Z15Z5UFVWVN	C34	CAP 50V .1UF AXIAL PHILIPS	COMPONENT	A104Z15Z5UFVWVN	Digi-Key	1203PHTR-ND
15	140	7	ECE-V1HV100SP	C35,C116,C117,C120,C	10UF/50V SMD ALUM	Panasonic - SCD	ECE-V1HV100SP	Digi-Key	PCE1022TR-ND

