

Getting Confidence
in Your Design Early!

跨界整合 翻轉設計

Graser User Conference

Taipei

2016
7.14



OrCAD[®] PCB Designer

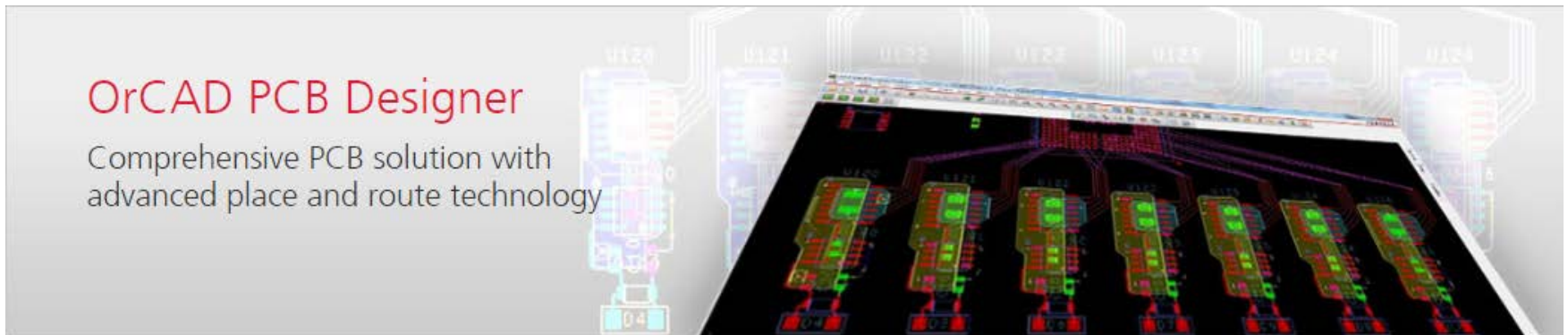
佈線與訊號阻抗驗證

Mark Wu/ Graser
14 / July / 2016



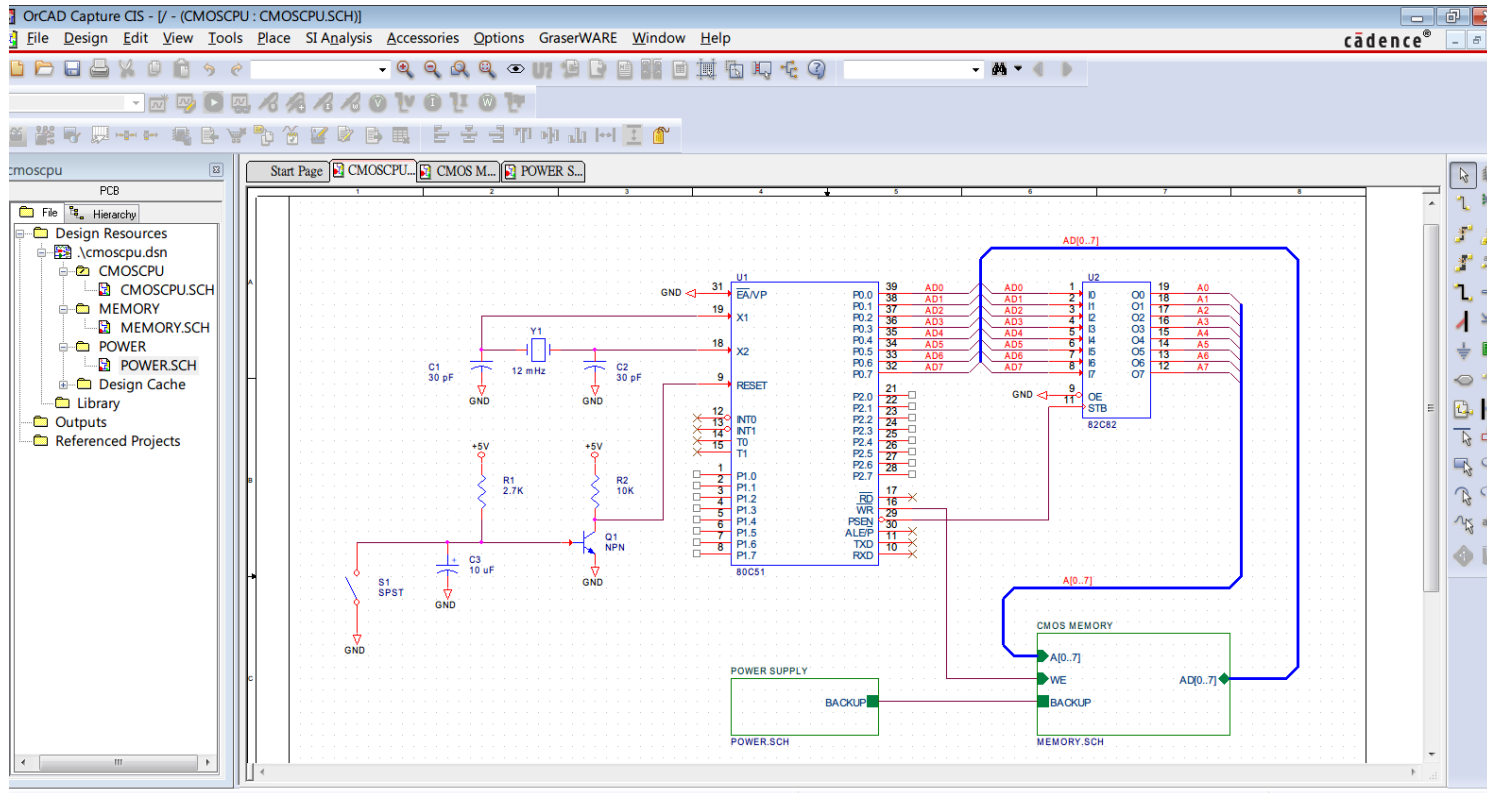
What's OrCAD PCB Designer?

- OrCAD® PCB Designer is powerful, tightly integrated PCB design technologies
 - Include Capture schematic
 - Constraint Manager setting
 - PCB editing and routing
 - Signal integrity and auto routing
 - Optional mixed-signal circuit simulation



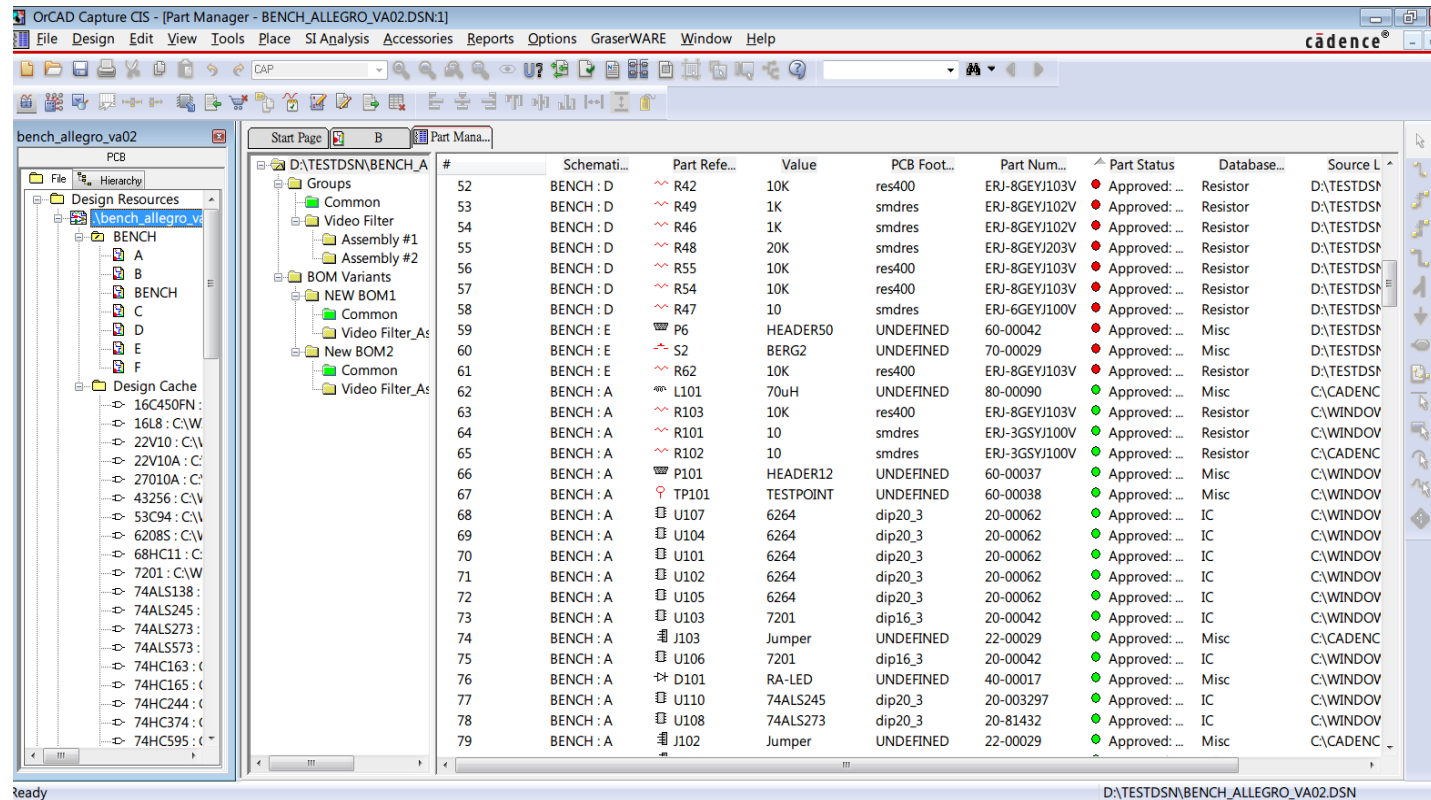
OrCAD Capture CIS Support

- Powerful Schematic Entry
 - Streamline the creation of your more complex schematic designs with hierarchical and reuse design capabilities



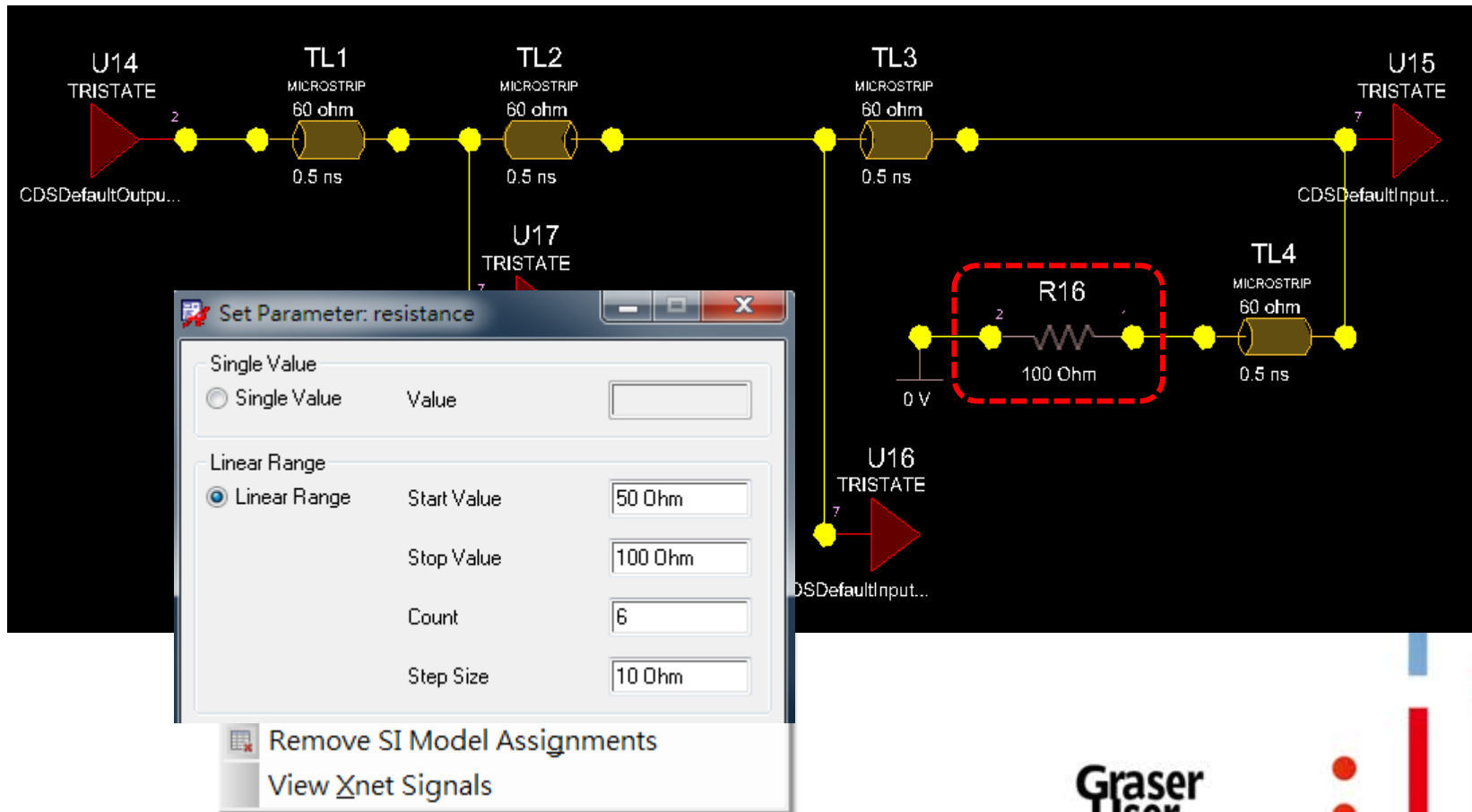
OrCAD Capture CIS Support

- Powerful part management
 - OrCAD® Capture CIS (Component Information System) provides easy access to your company's component databases and part information.



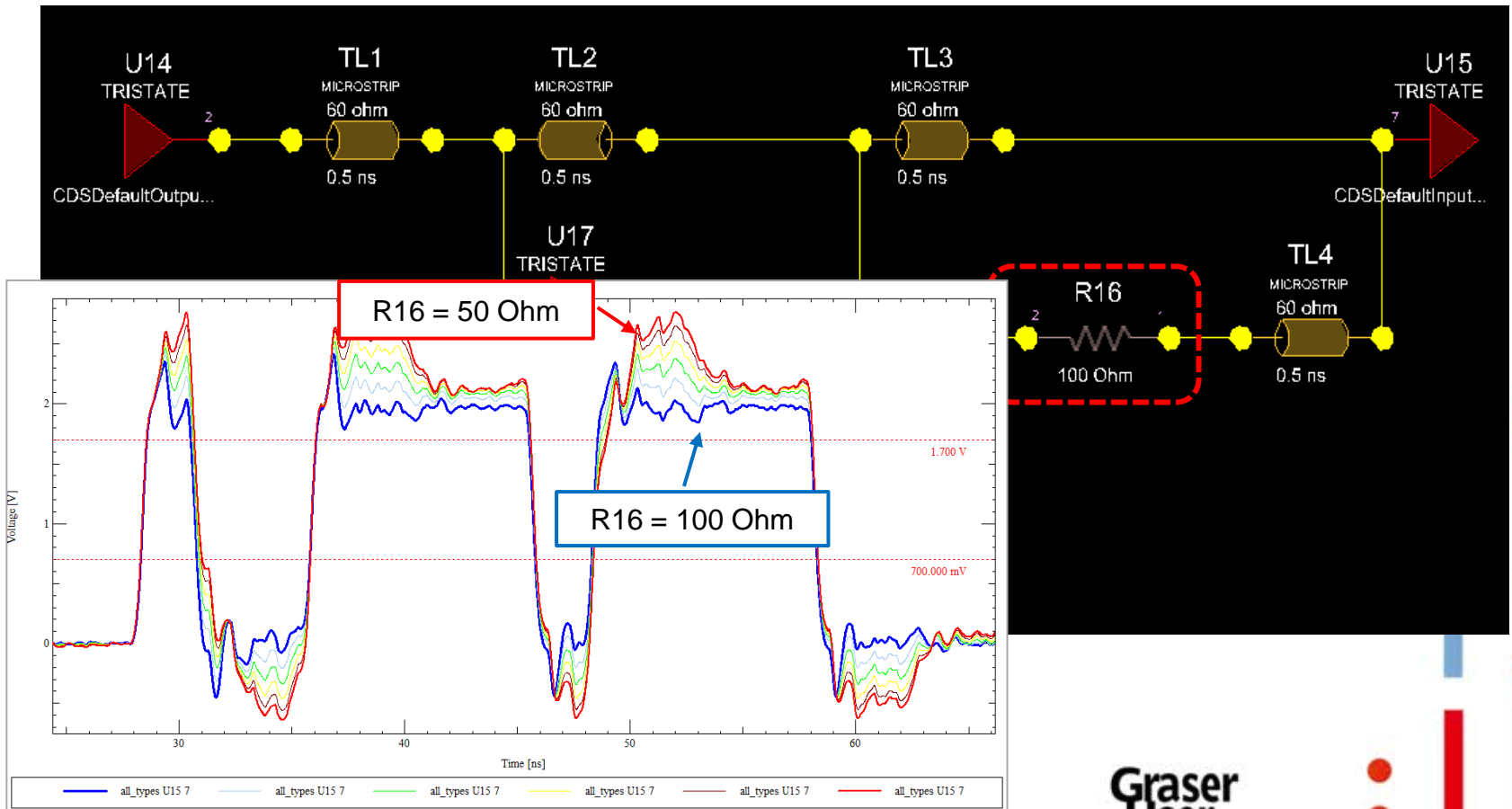
Pre-Simulation

- Easy to perform quick and accurate SI analysis on nets in OrCAD® PCB Designer. Impedance Control - Terminator



Pre-Simulation

- Easy to perform quick and accurate SI analysis on nets in OrCAD® PCB Designer. Impedance Control - Terminator



Constraint Setting

- Constraint Manager Setting
- Layer Set DRC and Routing
 - layer set functionality insures layer constrained nets are routed to wiring

Allegro Constraint Manager (connected to OrCAD PCB Designer Professional 17.2) [OR2ALG1_V2P1] - [Electrical / Net / Routing]

Worksheet Selector: OR2ALG1_V2P1 |

Objects		Referenced Electrical CSet	Uncoupled Length				Static Phase			
Type	Name		Gather Control	Length Ignore	Max	Actual	Margin	Tolerance	Actual	N
Dsn	OR2ALG1_V2P1			mil	mil	mil	mil	mil		
OType	Buses									
Bus	LED_BUS (16)									
OType	Diff Pairs									
DPr	DP1									
Net	DIFF A+									
Net	DIFFA-									
OType	XNets/Nets									
Net	+12V									
Net	CLK									
Net	DIS									
Net	GND									
Net	G0V									
Net	N01389									
Net	N01391									
Net	N01393									
Net	N03299									
Net	N03385									
Net	N03503									
Net	N06750									
Net	N06781									
Net	N06914									
Net	N07119									
Net	N07713									
Net	N106934									

Worksheet Selector: Electrical

Objects		Topology		Stub Length	Layer Sets
Type	Name	Verify Schedule	Schedule	mil	
Dsn	layer_sets				
ECS	AD_BUS	TEMPLATE		300.00	Is3-4:Is6-7
ECS	DIFF				Is3-4

OrCAD PCB/CM - Min/Max Propagation Delay

cdn_design1match_routed

Type	Objects	Referenced Electrical CSet	Pin Pairs	Pin Delay		Prop Delay			Prop Delay		
				Pin 1	Pin 2	Min	Actual	Margin	Max	Actual	Margin
				mil	mil	mil			mil		
Bus	LAMP_BUS (8)	LAMP_BUS									
XNet	LAMP0	LAMP_BUS									
PPr	LAMP0.T.1:U23.2					500.00 MIL	851.49 MIL	351.49 MIL	1500.00 MIL	851.49 MIL	648.51 MIL
PPr	LAMP0.T.1:U24.2					500.00 MIL	500.01 MIL	0.01 MIL	1500.00 MIL	500.01 MIL	999.99 MIL
PPr	LAMP0.T.2:U39.2					500.00 MIL	866.50 MIL	366.5 MIL	1500.00 MIL	866.50 MIL	633.5 MIL
PPr	LAMP0.T.2:U52.2					500.00 MIL	500.00 MIL	0 MIL	1500.00 MIL	500.00 MIL	1000 MIL
PPr	U20.38:LAMP0.T.1					8000.00 MIL	9152.45 MIL	1152.45 ...	11000.00 MIL	9152.45 MIL	1847.55 MIL
PPr	U20.38:LAMP0.T.2					8000.00 MIL	9432.44 MIL	1432.44 ...	11000.00 MIL	9432.44 MIL	1567.56 MIL
XNet	LAMP1	LAMP_BUS									
PPr	LAMP1.T.1:U23.3					500.00 MIL	824.49 MIL	324.49 MIL	1500.00 MIL	824.49 MIL	675.51 MIL
PPr	LAMP1.T.1:U24.3					500.00 MIL	500.01 MIL	0.01 MIL	1500.00 MIL	500.01 MIL	999.99 MIL
PPr	LAMP1.T.2:U39.3					500.00 MIL	838.00 MIL	338 MIL	1500.00 MIL	838.00 MIL	662 MIL
PPr	LAMP1.T.2:U52.3					500.00 MIL	500.00 MIL	0 MIL	1500.00 MIL	500.00 MIL	1000 MIL
PPr	U20.37:LAMP1.T.1					8000.00 MIL	9647.18 MIL	1647.18 ...	11000.00 MIL	9647.18 MIL	1352.82 MIL
PPr	U20.37:LAMP1.T.2					8000.00 MIL	9632.65 MIL	1632.65 ...	11000.00 MIL	9632.65 MIL	1367.35 MIL
XNet	LAMP2	LAMP_BUS									
PPr	LAMP2.T.1:U23.4					500.00 MIL	868.49 MIL	368.49 MIL	1500.00 MIL	868.49 MIL	631.51 MIL
PPr	LAMP2.T.1:U24.4					500.00 MIL	500.01 MIL	0.01 MIL	1500.00 MIL	500.01 MIL	999.99 MIL
PPr	LAMP2.T.2:U39.4					500.00 MIL	726.00 MIL	226 MIL	1500.00 MIL	726.00 MIL	774 MIL
PPr	LAMP2.T.2:U52.4					500.00 MIL	500.00 MIL	0 MIL	1500.00 MIL	500.00 MIL	1000 MIL
PPr	U20.36:LAMP2.T.1					8000.00 MIL	9195.54 MIL	1195.54 ...	11000.00 MIL	9195.54 MIL	1804.46 MIL
PPr	U20.36:LAMP2.T.2					8000.00 MIL	9717.03 MIL	1717.03 ...	11000.00 MIL	9717.03 MIL	1282.97 MIL
XNet	LAMP3	LAMP_BUS									
PPr	LAMP3.T.1:U23.5					500.00 MIL	829.50 MIL	329.5 MIL	1500.00 MIL	829.50 MIL	670.5 MIL
PPr	LAMP3.T.1:U24.5					500.00 MIL	500.00 MIL	0 MIL	1500.00 MIL	500.00 MIL	1000 MIL
PPr	LAMP3.T.2:U39.5					500.00 MIL	500.00 MIL	0 MIL	1500.00 MIL	500.00 MIL	1000 MIL
PPr	LAMP3.T.2:U52.5					500.00 MIL	857.50 MIL	357.5 MIL	1500.00 MIL	857.50 MIL	642.5 MIL
PPr	U20.35:LAMP3.T.1					8000.00 MIL	9955.78 MIL	1955.78 ...	11000.00 MIL	9955.78 MIL	1044.22 MIL
PPr	U20.35:LAMP3.T.2					8000.00 MIL	10692.78 MIL	2692.78 ...	11000.00 MIL	10692.78 MIL	307.22 MIL
XNet	LAMP4	LAMP_BUS									
PPr	LAMP4.T.1:U23.6					500.00 MIL	834.49 MIL	334.49 MIL	1500.00 MIL	834.49 MIL	665.51 MIL
PPr	LAMP4.T.1:U24.6					500.00 MIL	500.01 MIL	0.01 MIL	1500.00 MIL	500.01 MIL	999.99 MIL

source: Pin Pair LAMP2.T.2:U39.4 (read only)

OrCAD PCB/CM - Relative Propagation Delay

Worksheet selector: cdn_design1match_routed

Allegro Constraint Manager (connected to Allegro PCB Designer 16.5) [cdn_design1match_routed] - [Electrical: Nets: Routing [cdn_design1match_routed]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector: cdn_design1match_routed

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
- Wiring
- Vias
- Impedance
- Min/Max Propagation Delays
- Total Etch Length
- Differential Pair
- Relative Propagation Delay

All Constraints

Net

- Signal Integrity
- Timing
- Routing
- Wiring
- Vias
- Impedance
- Min/Max Propagation Delays
- Total Etch Length
- Differential Pair
- Relative Propagation Delay

Type	Objects	Pin Pairs	Scope	Relative Delay				Length mil	Delay ns
				Delta:Tolerance mil	Actual	Margin	+/-		
Dsn	cdn_design1match_routed					0 MIL			
MGrp	BRIDGE_RX_MATCH (32)	All Drivers/All Receive...	Global	:500.00 MIL		29.47 MIL			
MGrp	LAMP_BUS_M1 (16)					0 MIL			
PPr	U20.31:LAMP7.T.1 [LAMP7]		Local	:1000.00 MIL	1000.00 MIL	0 MIL	9724.64	1.783	
PPr	U20.31:LAMP7.T.2 [LAMP7]		Local	:1000.00 MIL	1000.00 MIL	0 MIL	10724.64	1.967	
PPr	U20.32:LAMP6.T.1 [LAMP6]		Local	:1000.00 MIL	379.01 MIL	620.99 MIL	10476.74	1.917	
PPr	U20.32:LAMP6.T.2 [LAMP6]		Local	:1000.00 MIL	379.01 MIL	620.99 MIL	10097.73	1.847	
PPr	U20.33:LAMP5.T.1 [LAMP5]		Local	:1000.00 MIL	97.99 MIL	902.01 MIL	9609.40	1.760	
PPr	U20.33:LAMP5.T.2 [LAMP5]		Local	:1000.00 MIL	97.99 MIL	902.01 MIL	9511.41	1.742	
PPr	U20.34:LAMP4.T.1 [LAMP4]		Local	:1000.00 MIL	224.01 MIL	776.99 MIL	9552.31	1.749	
PPr	U20.34:LAMP4.T.2 [LAMP4]		Local	:1000.00 MIL	224.01 MIL	776.99 MIL	9328.30	1.708	
PPr	U20.35:LAMP3.T.1 [LAMP3]		Local	:1000.00 MIL	737.00 MIL	263 MIL	9955.78	1.767	
PPr	U20.35:LAMP3.T.2 [LAMP3]		Local	:1000.00 MIL	737.00 MIL	263 MIL	10692.78	1.952	
PPr	U20.36:LAMP2.T.1 [LAMP2]		Local	:1000.00 MIL	521.49 MIL	478.51 MIL	9195.54	1.684	
PPr	U20.36:LAMP2.T.2 [LAMP2]		Local	:1000.00 MIL	521.49 MIL	478.51 MIL	9717.03	1.779	
PPr	U20.37:LAMP1.T.1 [LAMP1]		Local	:1000.00 MIL	14.53 MIL	985.47 MIL	9647.18	1.765	
PPr	U20.37:LAMP1.T.2 [LAMP1]		Local	:1000.00 MIL	14.53 MIL	985.47 MIL	9632.65	1.762	
PPr	U20.38:LAMP0.T.1 [LAMP0]		Local	:1000.00 MIL	279.99 MIL	720.01 MIL	9152.45	1.677	
PPr	U20.38:LAMP0.T.2 [LAMP0]		Local	:1000.00 MIL	279.99 MIL	720.01 MIL	9432.44	1.728	
MGrp	XCVR_RX_MATCH (40)	All Drivers/All Receive...	Global	:300.00 MIL		6.47 MIL			
Net	XCVR_RX_N<0>	All Drivers/All Receivers	Global	:300.00 MIL		15.99 MIL			
Net	XCVR_RX_N<1>	All Drivers/All Receivers	Global	:300.00 MIL		104.54 MIL			
Net	XCVR_RX_N<2>	All Drivers/All Receivers	Global	:300.00 MIL		6.5 MIL			
Net	XCVR_RX_N<3>	All Drivers/All Receivers	Global	:300.00 MIL		34.89 MIL			
Net	XCVR_RX_N<4>	All Drivers/All Receivers	Global	:300.00 MIL		6.47 MIL			
Net	XCVR_RX_N<5>	All Drivers/All Receivers	Global	:300.00 MIL		8.23 MIL			
Net	XCVR_RX_N<6>	All Drivers/All Receivers	Global	:300.00 MIL		7.76 MIL			
Net	XCVR_RX_N<7>	All Drivers/All Receivers	Global	:300.00 MIL		47.71 MIL			
Net	XCVR_RX_N<8>	All Drivers/All Receivers	Global	:300.00 MIL		109.11 MIL			
Net	XCVR_RX_N<9>	All Drivers/All Receivers	Global	:300.00 MIL		36.13 MIL			
Net	XCVR_RX_N<10>	All Drivers/All Receivers	Global	:300.00 MIL		67.15 MIL			
Net	XCVR_RX_N<11>	All Drivers/All Receivers	Global	:300.00 MIL		126.24 MIL			

Physical

Spacing

Same Net Spacing

Properties

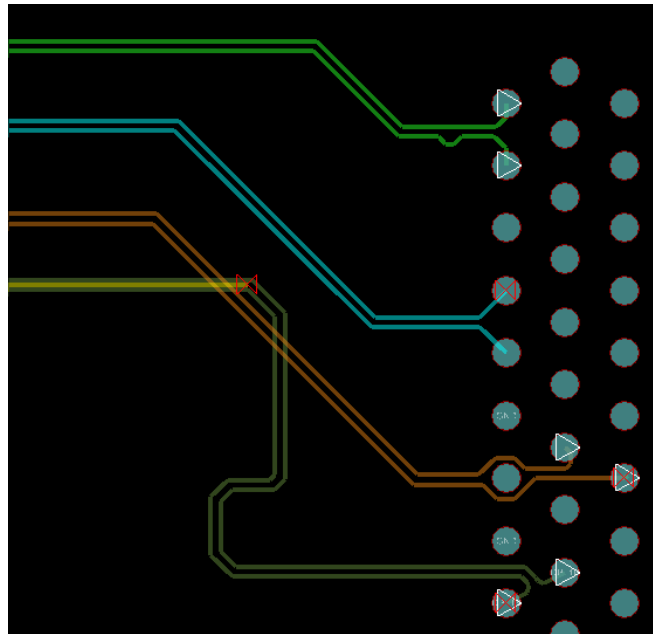
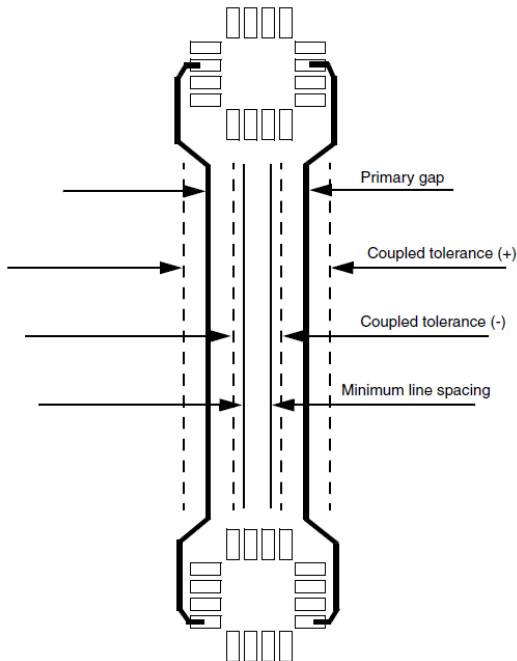
DRC

Relative Propagation Delay /

Delay of an object (RELATIVE_PROPAGATION_OBJECT_DELAY) (read only)

OrCAD PCB/CM - Differential Pair

Gather Control	Uncoupled Length				Static Phase			Min Line Spacing	Coupling Parameters					
	Length Ignored	Max	Actual	Margin	Tolerance	Actual	Margin		Prim. Gap	Prim. Width	Neck Gap	Neck Width	(+Tol.	(-)Tol.
					mil									
*	*	*	*	*	*	*	*	*	*	*	*	*	*	
Ignore		300.00			5 mil		-60.71	0.00	0.00	5.00	0.00	0.00	0.00	
Ignore		300.00			5 mil		-36.98	3.80	6.00	6.00	3.90	3.40	0.10	
Ignore		300.00			5 mil		-5.220	3.80	6.00	6.00	3.90	3.40	0.10	
Ignore		300.00			5 mil		-40.32	3.80	6.00	6.00	3.90	3.40	0.10	
Ignore		300.00			5 mil		-22.16	3.80	6.00	6.00	3.90	3.40	0.10	
Ignore		300.00			5 mil		-12.36	3.80	6.00	6.00	3.90	3.40	0.10	
Ignore		300.00			5 mil		-60.71	3.80	6.00	6.00	3.90	3.40	0.10	
Ignore		300.00			5 mil		-12.51	3.80	6.00	6.00	3.90	3.40	0.10	



Support X-Net

- eXtend Net

The screenshot displays the OrCAD PCB Designer Professional interface. The main workspace shows a PCB layout with two U100 components connected to a central RN1 component. The interface includes a top menu bar, a toolbar, and a Design Object Find Filter panel on the right.

Design Object Find Filter

All On	All Off
<input type="checkbox"/> Groups	<input checked="" type="checkbox"/> Shapes
<input type="checkbox"/> Comps	<input checked="" type="checkbox"/> Voids/Cavities
<input checked="" type="checkbox"/> Symbols	<input checked="" type="checkbox"/> Cline segs
<input type="checkbox"/> Functions	<input checked="" type="checkbox"/> Other segs
<input checked="" type="checkbox"/> Nets	<input checked="" type="checkbox"/> Figures
<input checked="" type="checkbox"/> Pins	<input checked="" type="checkbox"/> DRC errors
<input checked="" type="checkbox"/> Vias	<input checked="" type="checkbox"/> Text
<input checked="" type="checkbox"/> Clines	<input checked="" type="checkbox"/> Ratsnests

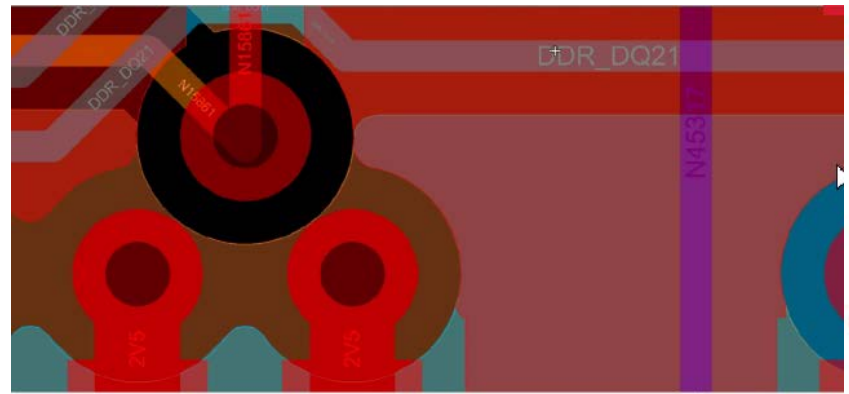
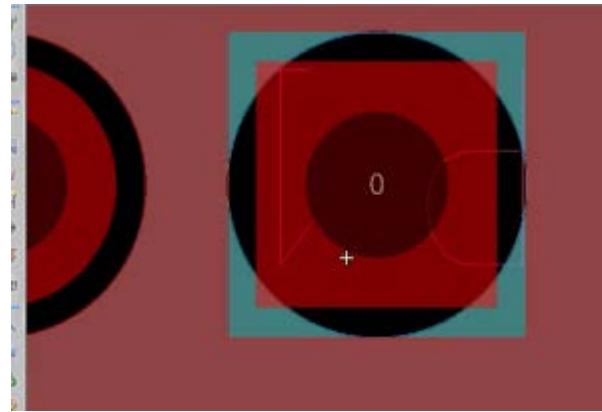
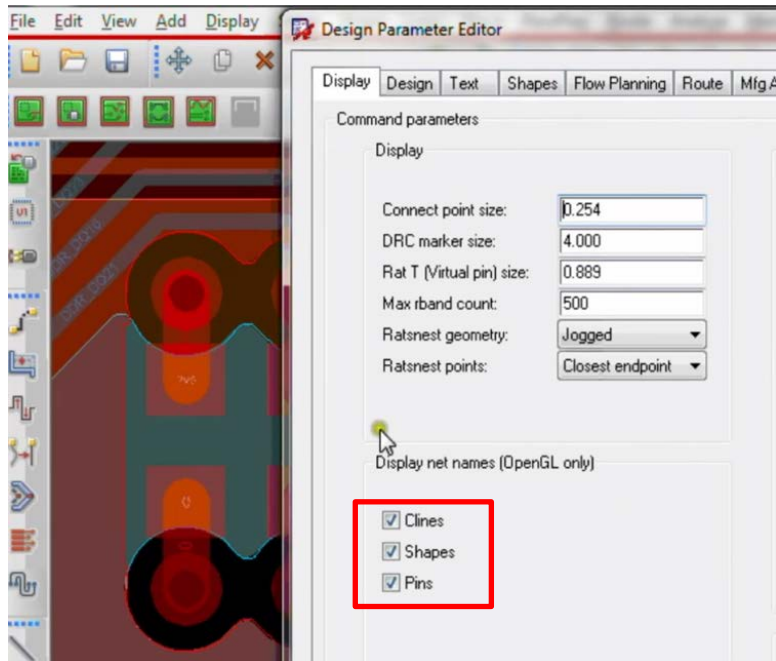
Allegro Constraint Manager (connected to OrCAD PCB Designer Professional 17.2) [cads_routed_Rat_XNET_172] - [Electrical / Net / Ro]

Worksheet Selector: cds_routed_Rat_XNET_172

Objects		Pin Pairs	Scope	Delta: Tolerance
Type	Name			mil
Dsn	cds_routed_Rat_XNET_172			
OTyp	Match Groups			
MGGrp	MG1 (2)	All Drivers/All Rece...	Global	0 mil:50 mil
PPr	U101.3:U100.13 [AA]		Global	0 mil:50 mil
PPr	U100.10:U101.5 [BB]		Global	0 mil:50 mil
OTyp	Buses			
OTyp	XNets/Nets			
XNet	AA			
PPr	U101.3:U100.13			
Net	ADSL			
XNet	BB			
PPr	U100.10:U101.5			
Net	BHEL			
Net	BLEL			
Net	CAS0L			
Net	CAS1L			
Net	CLEAR			
Net	CLK1+			

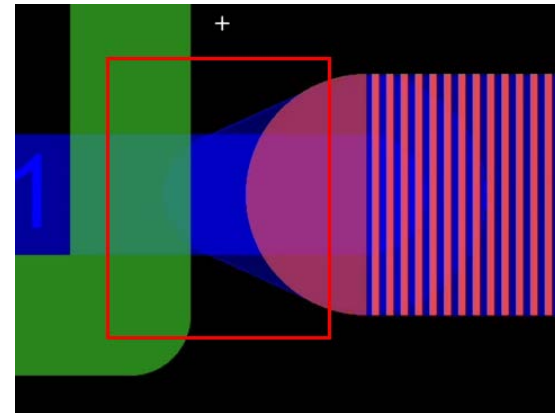
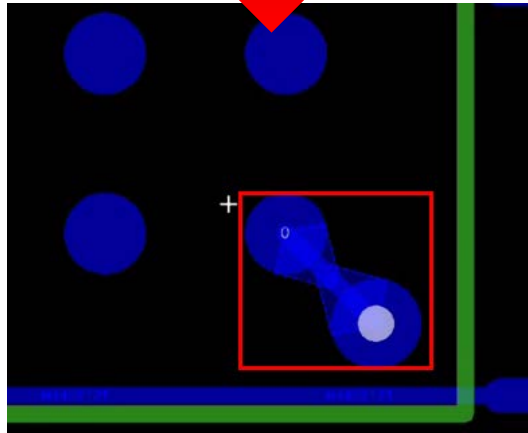
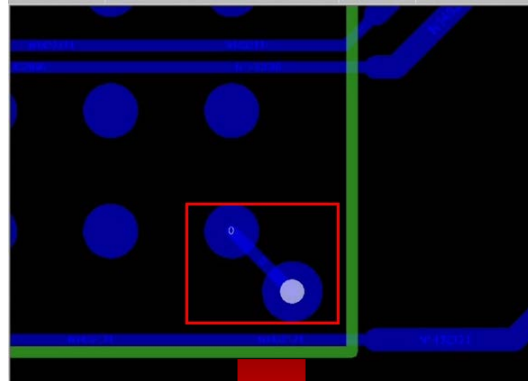
Embedded Net Names

- Set net name function to display so that the net names are shown.



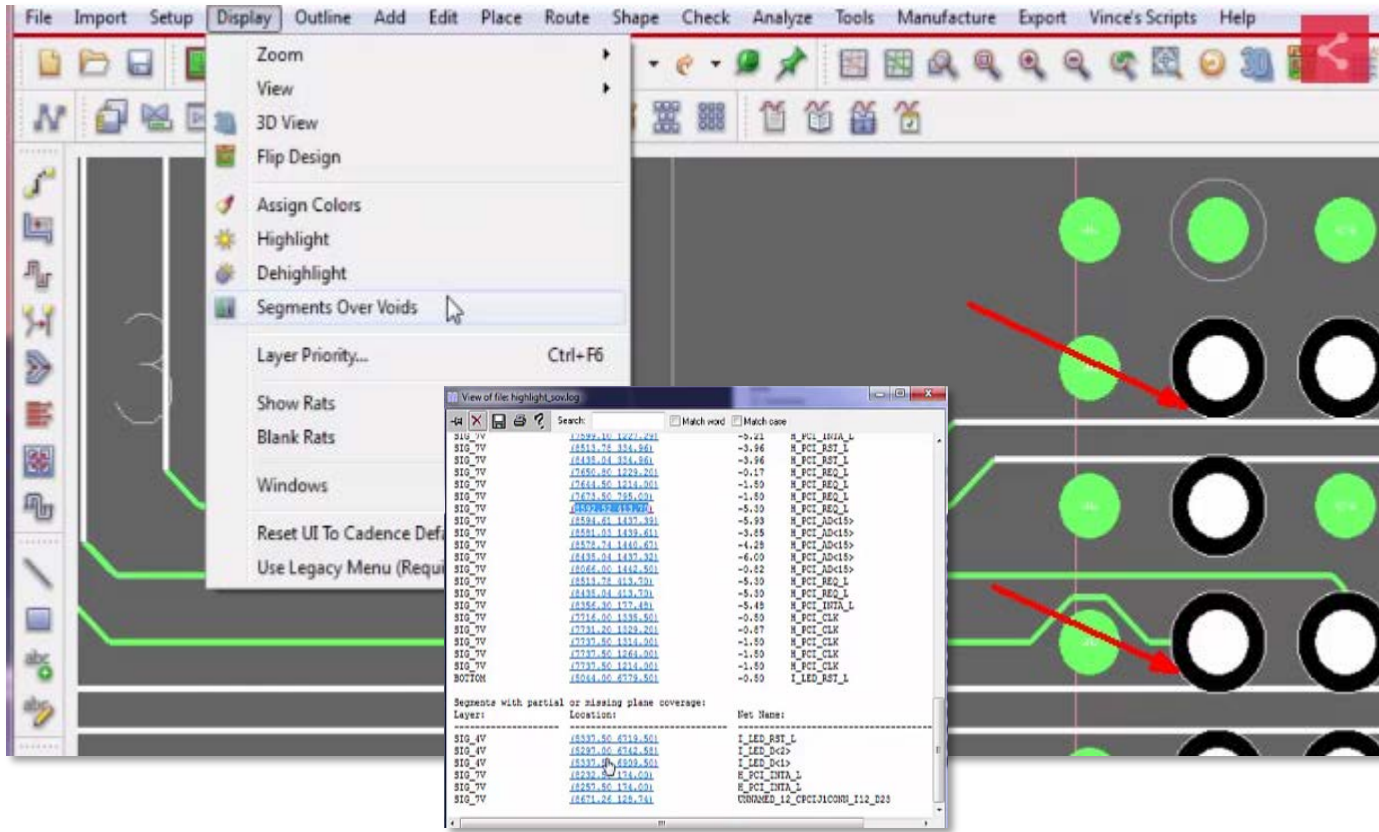
Fillet and Tapered Traces

- Use the Fillet Tapered Traces function



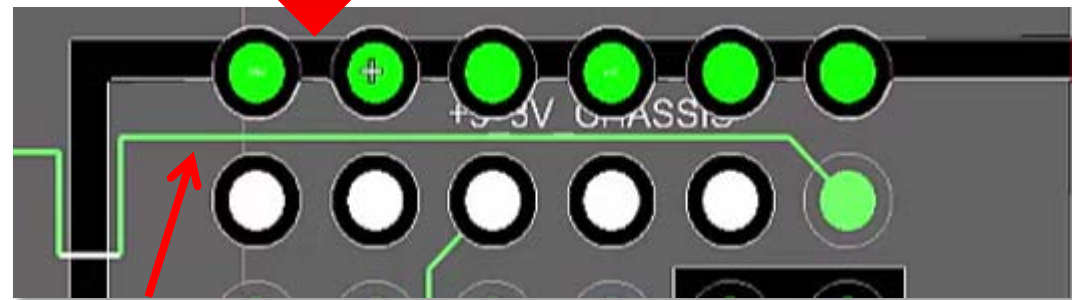
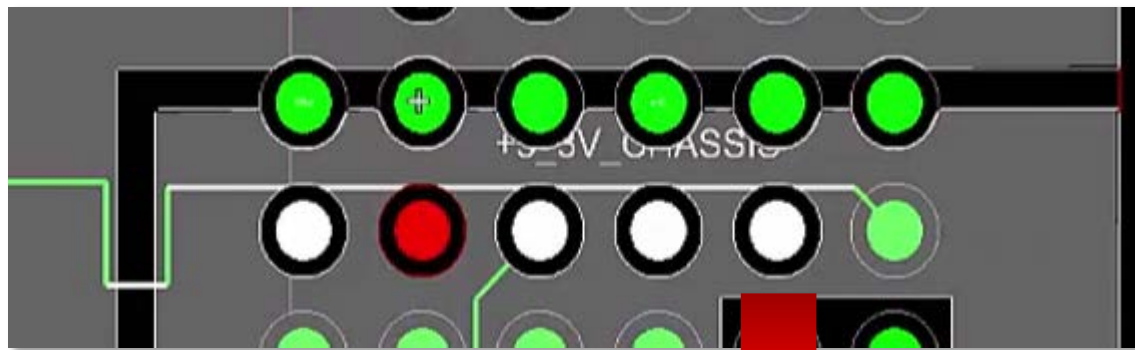
Segment Over Voids

- *Segment Over Voids* detects cline segments crossing adjacent plane layer voids.



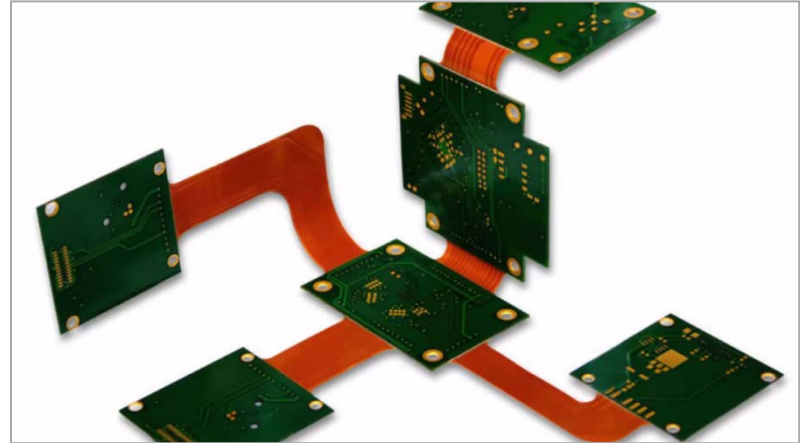
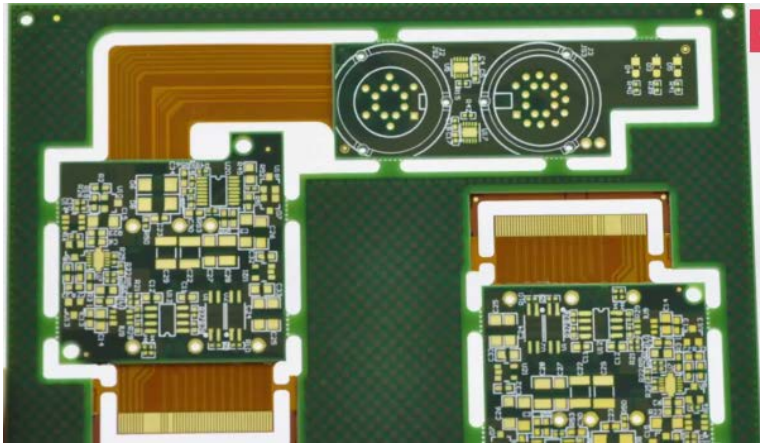
Segment Over Voids

- *Segment Over Voids* detects cline segments crossing adjacent plane layer voids.



Flex and Rigid Flex Technologies

- To enable a faster and more efficient flex and rigid-flex design, capabilities for flex and rigid flex design to minimize design iterations. Key flex and rigid flex features include :
 - Stack-up by zone for flex and rigid-flex designs
 - Inter-layer checks for rigid-flex designs
 - Contour and arc-aware routing



Flex and Rigid Flex Technologies

- Layer Setting

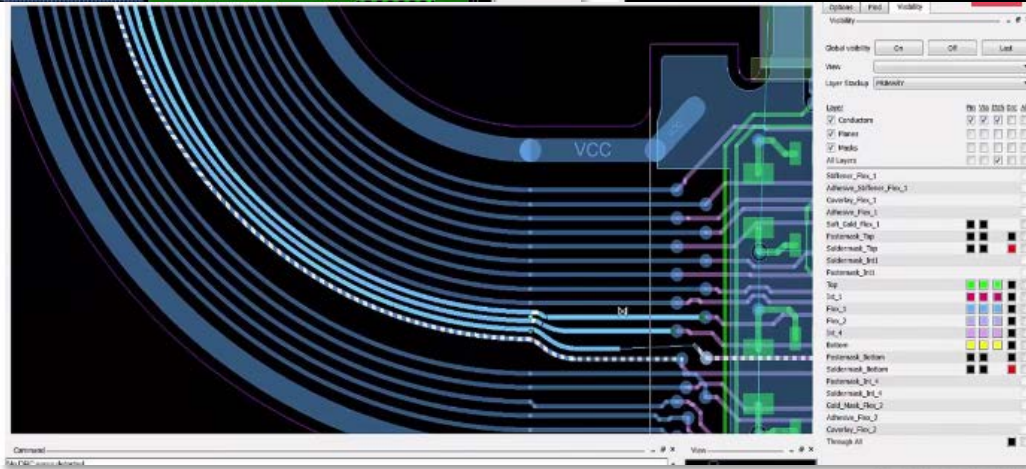
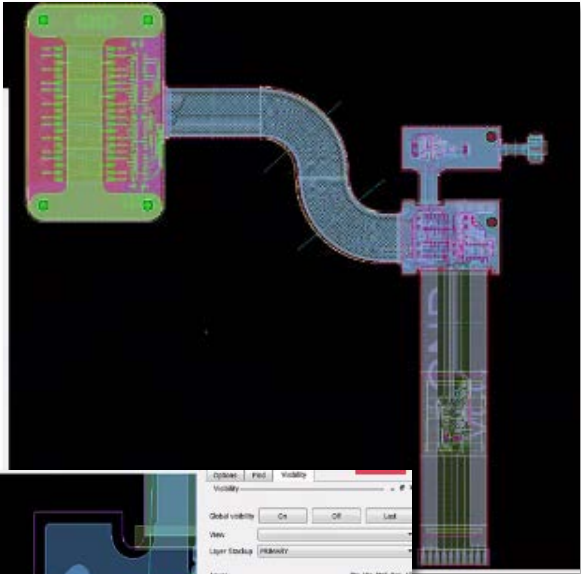
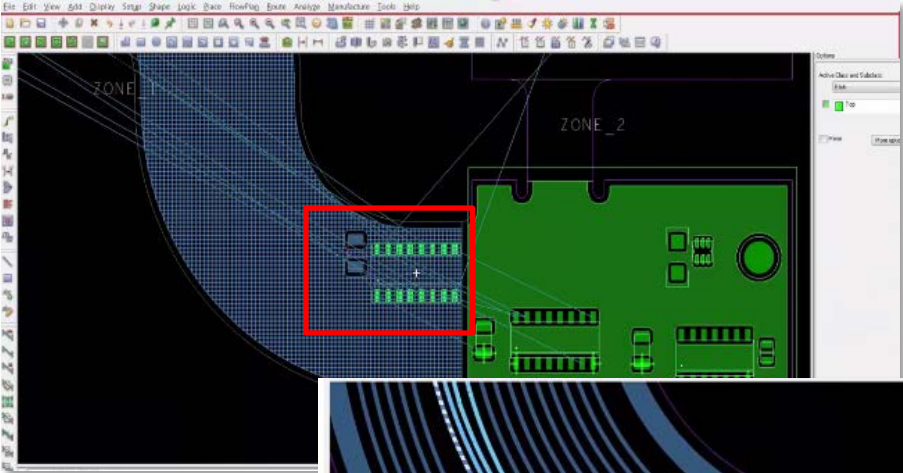
The screenshot shows the Cadence PCB Editor interface with the Cross Section Editor (Multi Stackups) open. The main window displays a table of layer properties for technology IPC3581. The table includes columns for Name, Layer, Types, Thickness (mil), Material, and Primary/Flex-1/Flex-2/Flex-3 checkboxes.

#	Name	Layer	Types	Thickness (mil)	Material	Primary	Flex-1	Flex-2	Flex-3
	STIFFENER_FLEX_1	Surface			Fr-4				
	TIN_PLATE_TOP	Mask		0.5	Tin				
	ADHESIVE_STIFFENER_FLEX_1	Mask		0.84252	Adhesive E...				
	COVERLAY_FLEX_1	Mask		8	Polyimide				
	ADHESIVE_FLEX_1	Mask		0.5	Adhesive A...				
	PASTERMASK_FLEX_1	Mask		3	Solder Past...				
	GOLD_SOFT_FLEX_1	Mask		8	Polyimide				
	PASTERMASK_TOP	Mask		3	Solder Past...				
	SOLDERMASK_TOP	Mask		0.590551	Soldermas...				
	PASTERMASK_INT1	Mask		3	Solder Past...				
1	TOP	Conductor		1.2	Copper				
		Dielectric		8	Fr-4				
2	INT_1	Conductor		1.2	Copper				
		Dielectric		5	Polyimide B...				
3	FLEX_1	Conductor		1.2	Copper				
		Dielectric		3	Polyimide F...				
4	FLEX_2	Conductor		1.2	Copper				
		Dielectric		5	Polyimide B...				
5	INT_4	Conductor		1.2	Copper				
		Dielectric		8	Fr-4				
6	BOTTOM	Conductor		1.2	Copper				
		Mask		3	Solder Past...				
	PASTERMASK_BOTTOM	Mask		0.590551	Soldermas...				
	PASTERMASK_INT_4	Mask		0.5	Adhesive A...				

The interface also shows a 3D cross-section view of the board stackup, a detailed layer stackup list on the right, and a Properties panel at the bottom. The Properties panel includes sections for Embedded Layers Setup and Unused Pads Suppression, with a 3D model of a pad and its suppression options.

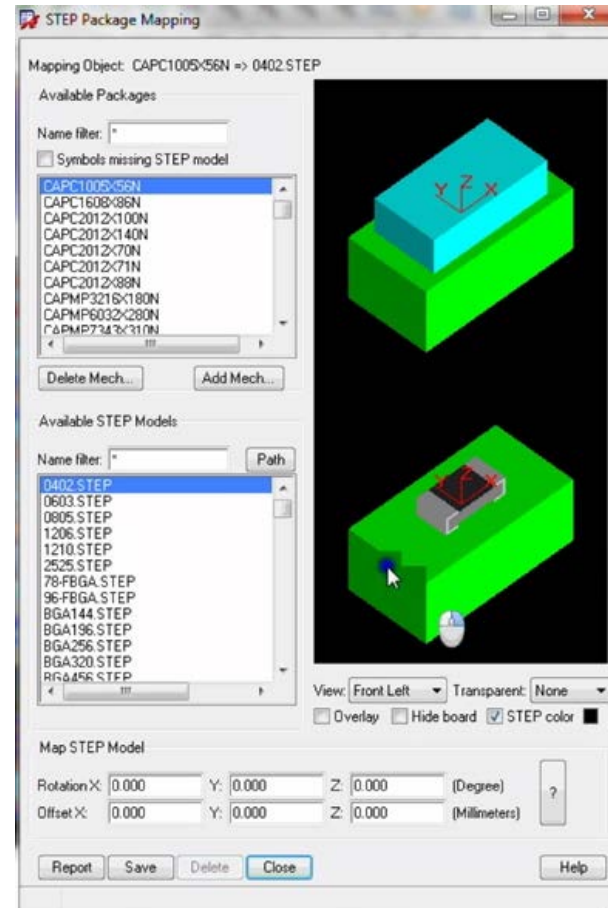
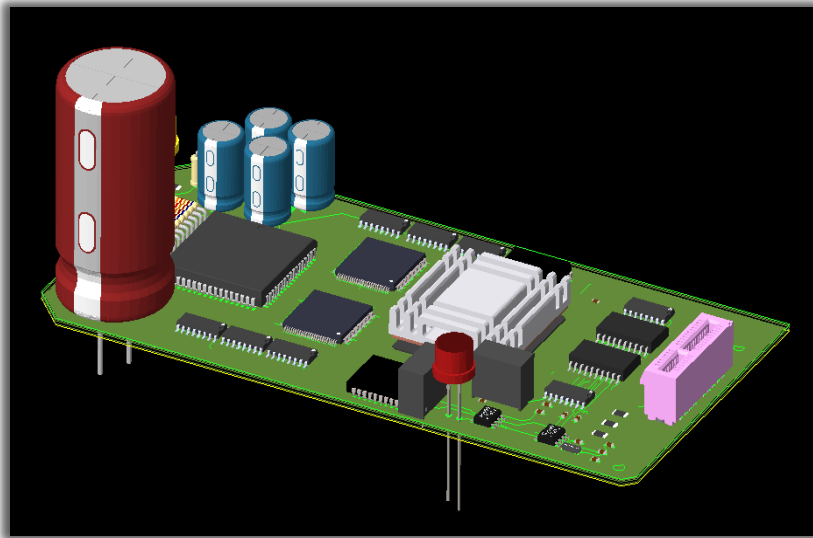
Flex and Rigid Flex Technologies

- Component place on Rigid Flex
- Routing on Rigid Flex



STEP Support - Mapping 3D Models

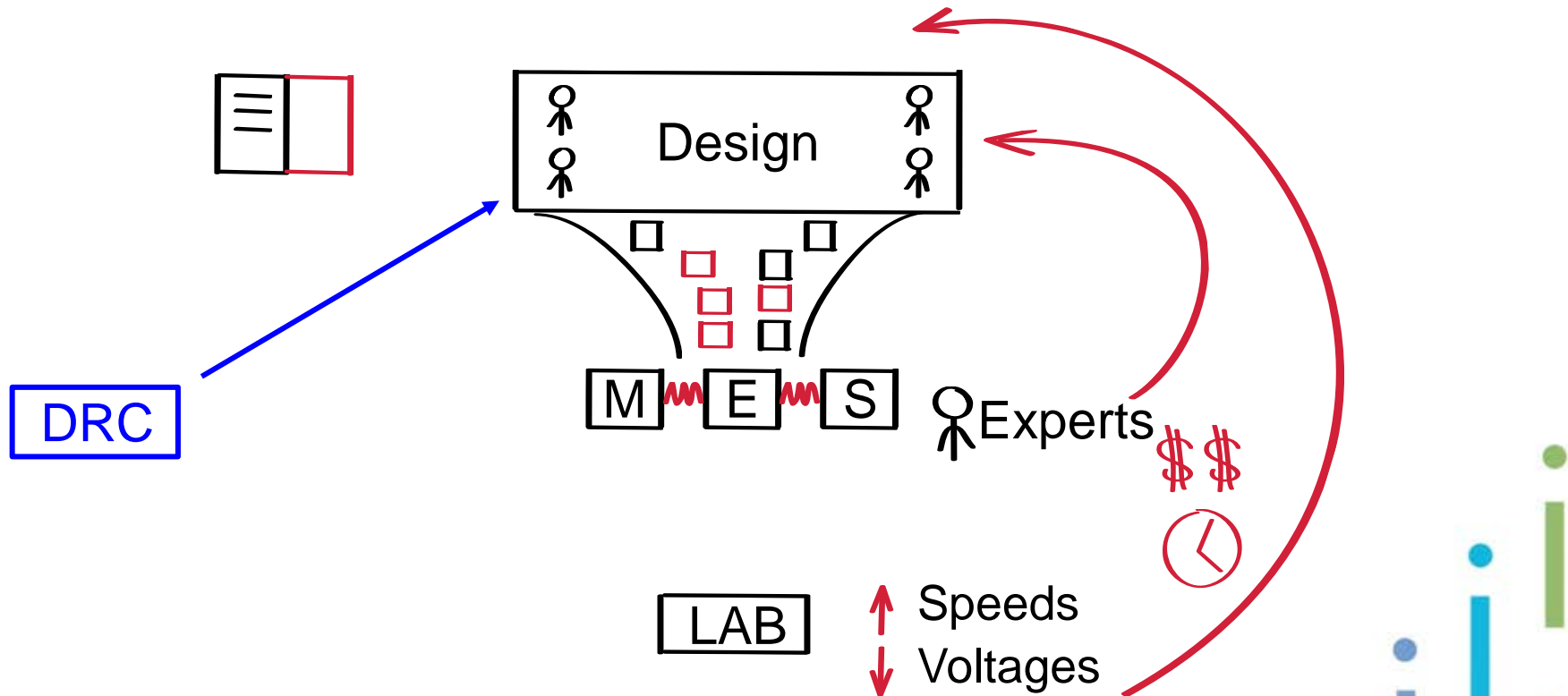
- Explore the ability to map and link a 3D STEP model to your components.



OrCAD® Sigrity™ ERC / SRC Verification



PCB Design Flow



Signal and Power Chaos



Product Design Requirements



Low Cost



High Performance



Shorter Design Phases

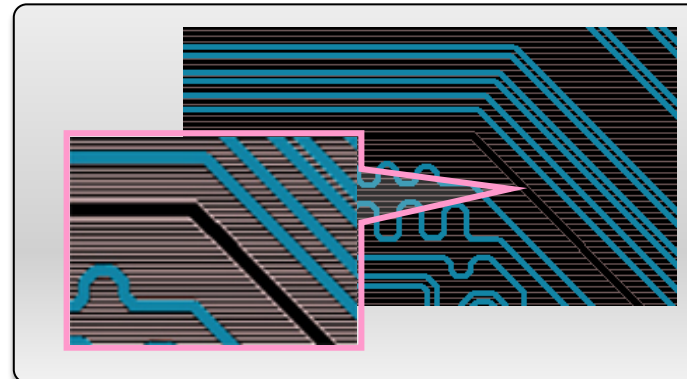
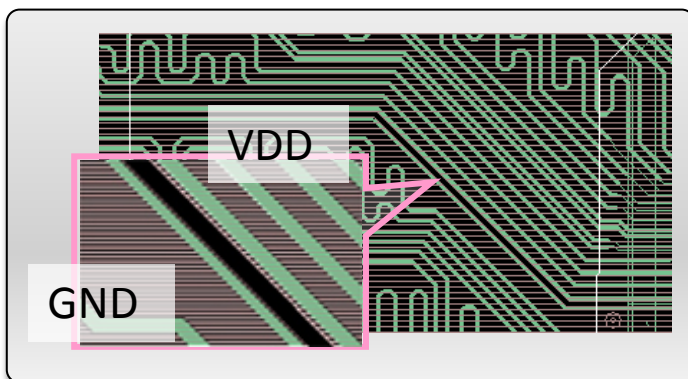
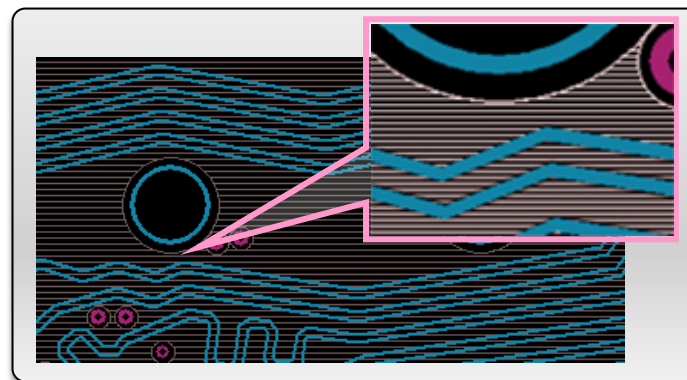
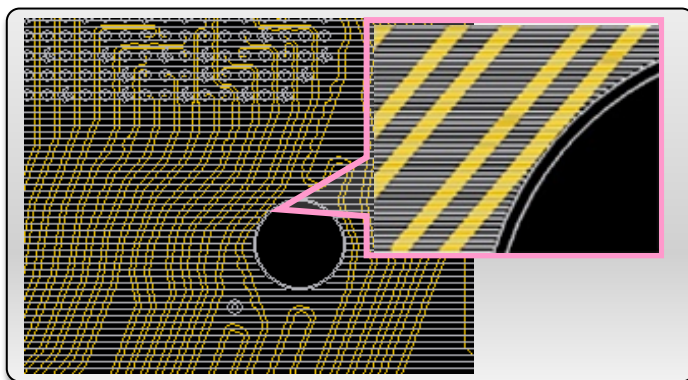


First-Time Design Success!



Spacing Constraint Set

Reference Plane Spacing Clearance



- EMI
- Impedance mismatch



GND Stitching Vias

Return current path

Poor

Top	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Vcc	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Gnd	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bottom	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>

OK

Top	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Gnd1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Int1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Vcc1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Vcc2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Int2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Gnd2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bottom	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

OK

Top	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Gnd	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
In1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
In2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Gnd1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Pwr	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
In3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

GND vias

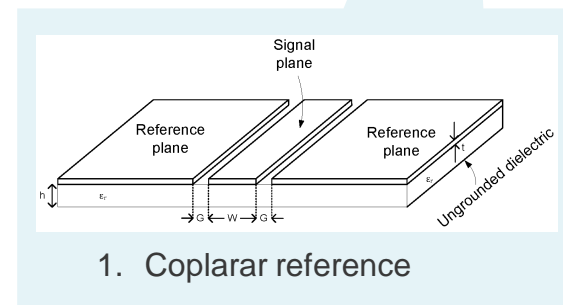
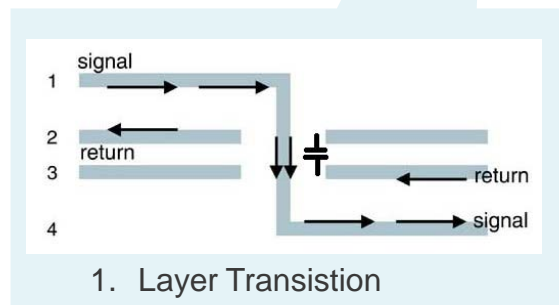
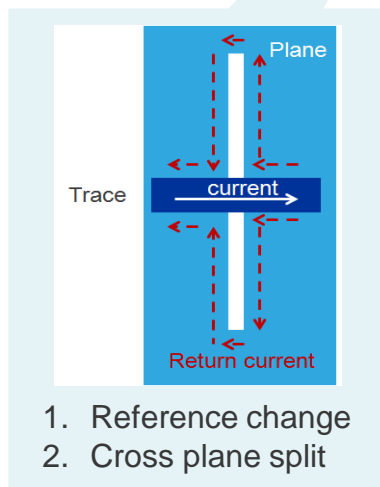
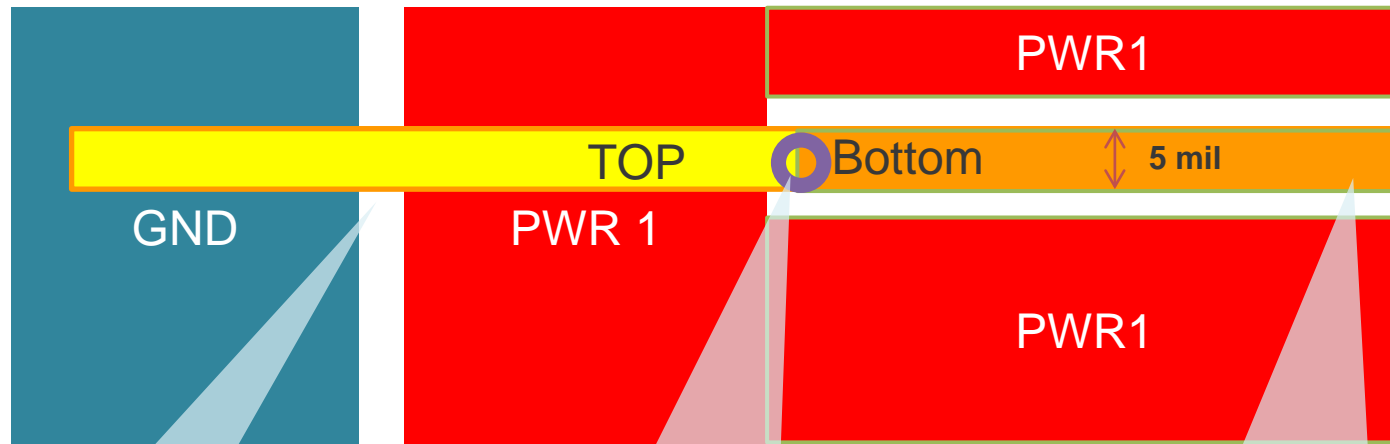
GND stitching via is not necessary for layer changing occurs on adjacent layers because they reference to the same plane.

- EMI
- Signal degradation



About SI – Impedance and Xtalk

- After pre-simulation, you set the trace width to be 5 mil in the constraint system to achieve the impedance you want. Of course, the following picture will show **no DRC** violation. **But if this is a 2-layers design and...**

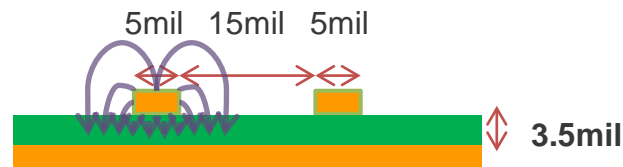


About SI – Impedance and Xtalk

- Talking about crosstalk, you probably follow the 3W rule – set the spacing between adjacent traces to 3 times the width of the trace as the following:



- The 3W rule may work well for the following structure:

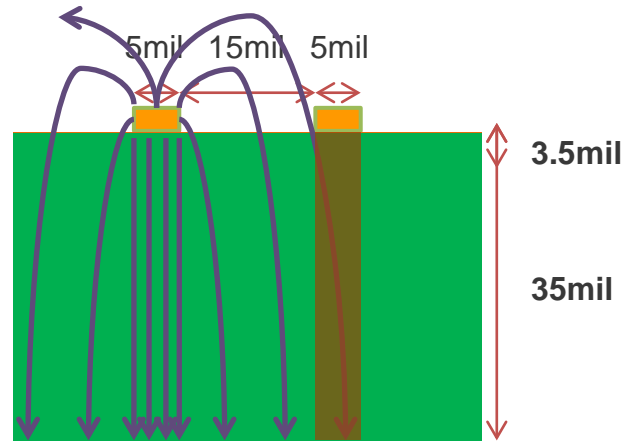


No DRC violation → No Xtalk issue



About SI – Impedance and Xtalk

- But if the stack-up looks like the following, will 3W rule still works well?



No DRC violation → No Xtalk issue ?

Now, you're not satisfied with simply spacing constraint or the related **DRC** violation warning. You feel you probably need **simulation** or other way to tell you :

How Much the Coupling is



The gap between DRC and SI performance

- The gap between layout designers and SI engineers is huge
 - Have different design expertise
 - Using different tools
 - Measured by different units

DRC

Design Rule Check

Layout/Board designer

Layout tools

Geometry domain (mil/mm)

Gap

Simulation

Using Device Models

SI engineer

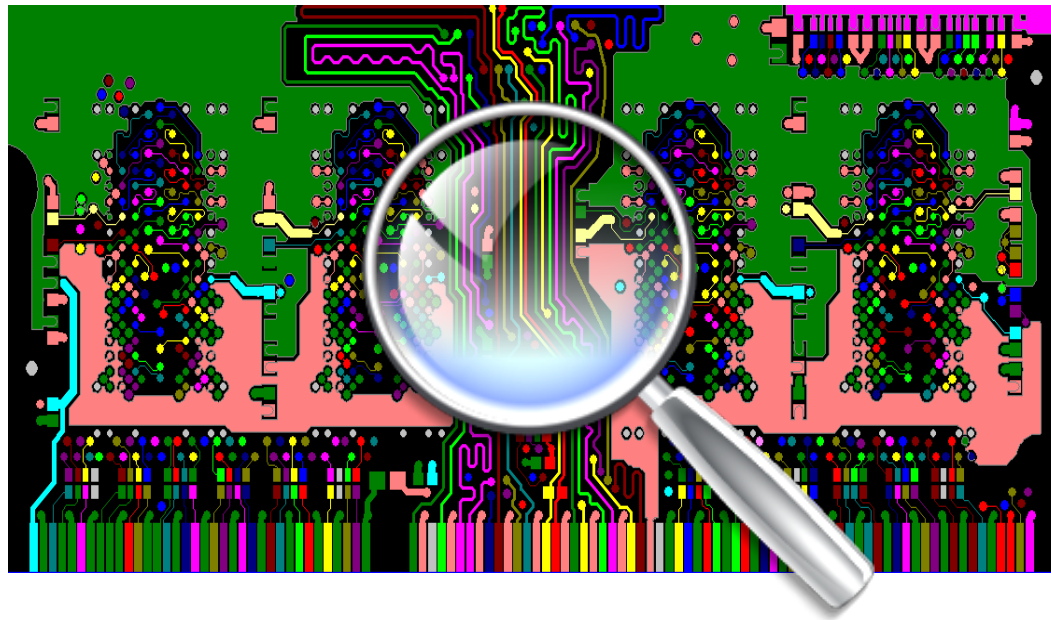
Simulation tools

Electrical domain (mv, ps)



Why Electrical Rule Check

- ERCs are better than DRCs for 'signal quality' validation
 - Goes beyond **MINIMUM-ACCEPTANCE, GEOMETRY-BASED** constraint validation
- PCB designers identify and address first-order signal quality issues



What is Sigrity ERC?

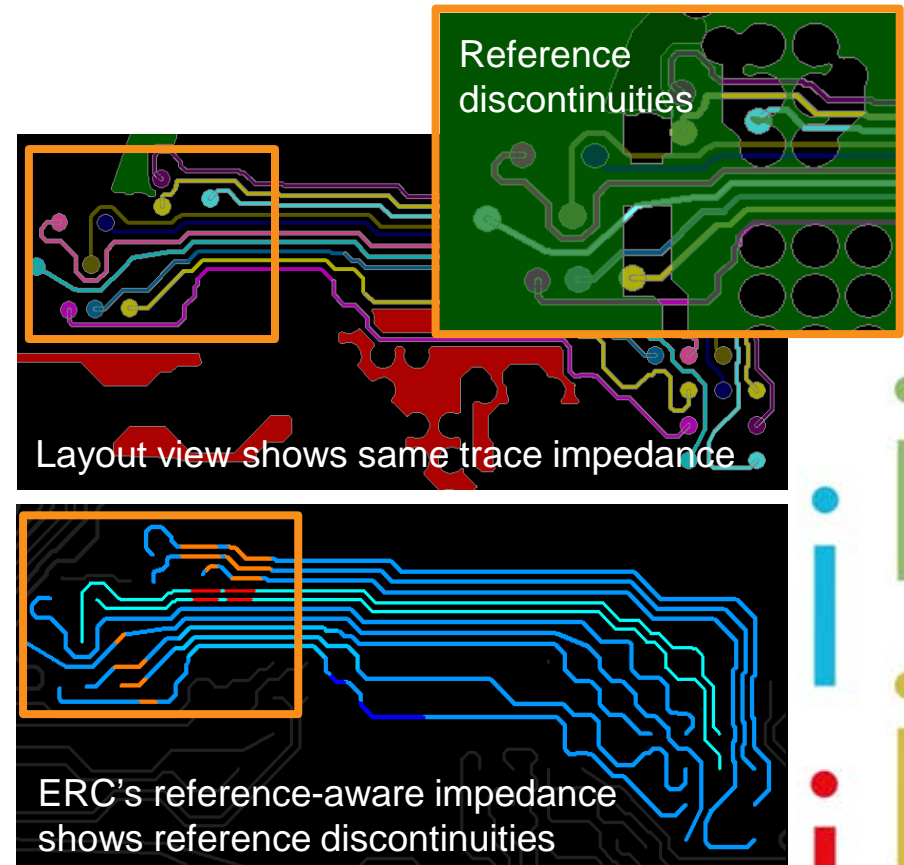
- OrCAD® Sigrity™ ERC is individual, segment-level view in geometry domain for PCB's SI performance

with

- Trace reference
- Trace reference-aware impedance
- Trace reference-aware coupling
- Differential pair routing phase
- # of vias and via locations,
- Practical for board level check

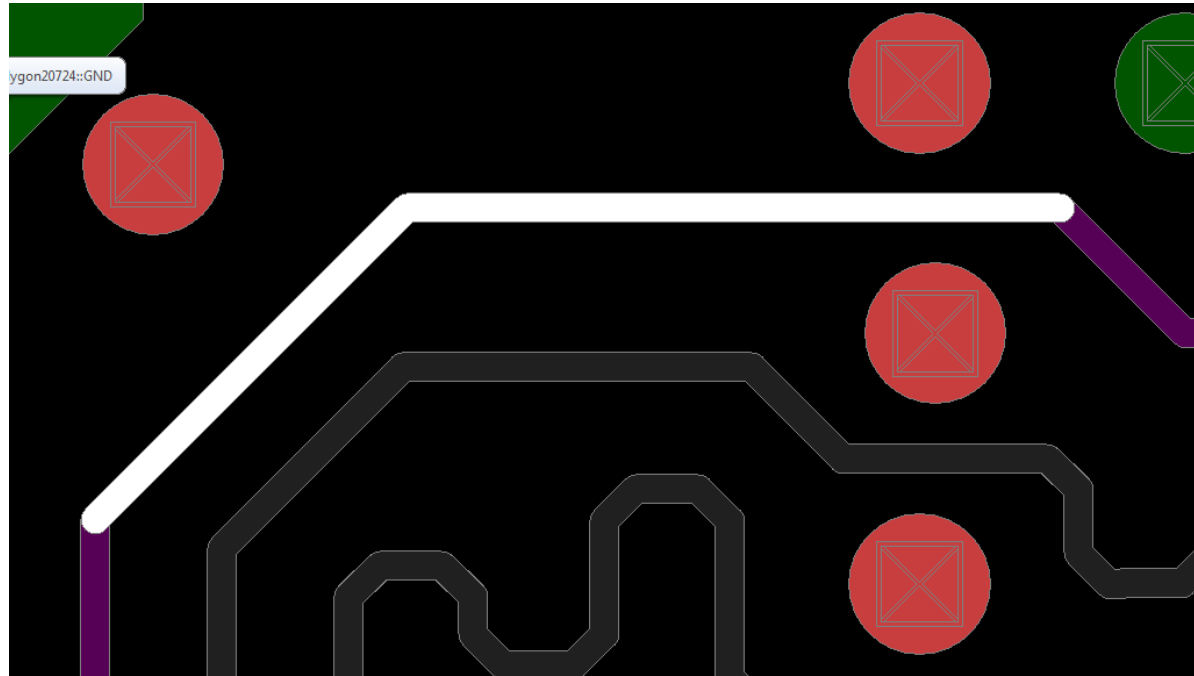
(setup, simulation, report)

<2min 10-20min auto



What is Sigrity ERC?

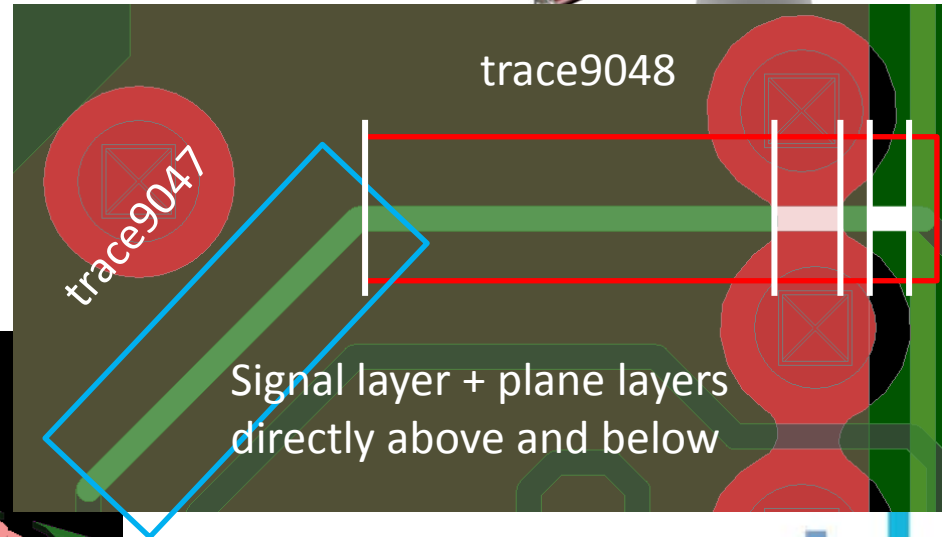
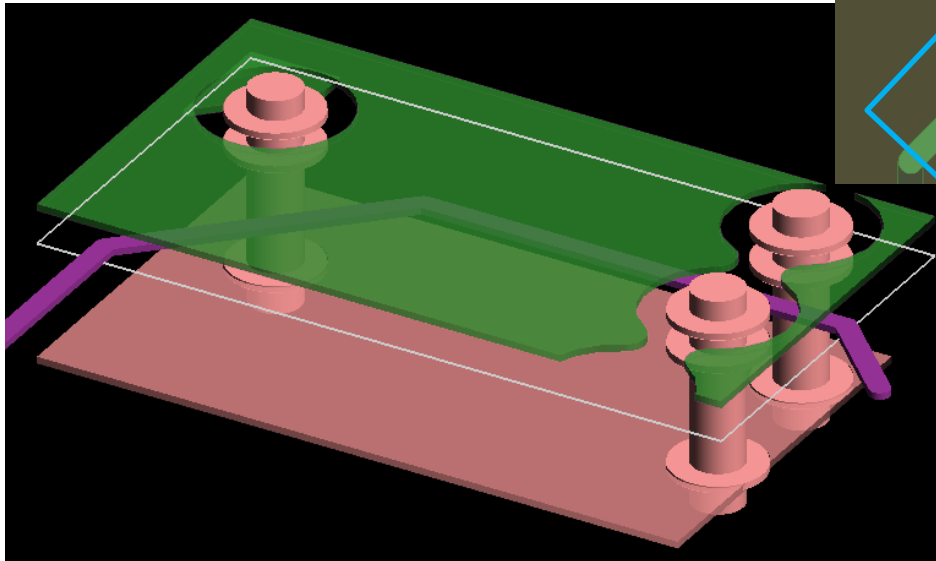
- DRC – Simplified impedance view
 - Two trace segments example
 - 2 trace segments, same trace width, same impedance
 - You can also see trace segment length



What is Sigrity ERC?

- If you look close enough...
Two trace segments example

- **Trace9047:**
one uniform impedance section
- **Trace9048:**
4 impedance sections



What is Sigridy ERC?

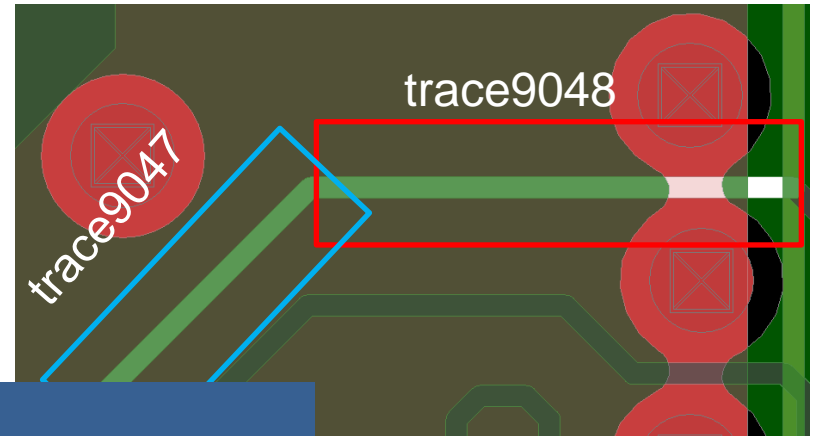
- Trace coupling
 - Trace9047 is one uniform impedance section
 - Trace9047 broken into 5 sections based on trace coupling
 - two no coupling sections (1 & 5)
 - two 2-line coupling sections (2 & 4)
 - one 3-line coupling section (3)

ERC results			
Trace Name	Aggressor Trace Names	Coupling Coefficient (%)	Length (%)
Trace9047::DQ0	-	-	← 1 1.82
Trace9047::DQ0	Trace9024::DQ1	5.3	← 2 1.46
Trace9047::DQ0	Trace9024_Auto_190::DQ1	5.3	← 3 1.16
	Trace8280::DQ4	0.6	
Trace9047::DQ0	Trace9024_Auto_191::DQ1	5.3	← 4 4.10
Trace9047::DQ0	-	-	← 5 3.04



What is Sigrity ERC?

- Trace upper / lower layer reference
 - Based on upper / lower layer references
 - Trace9047 → one section
 - Trace9048 → 5 sections



ERC results

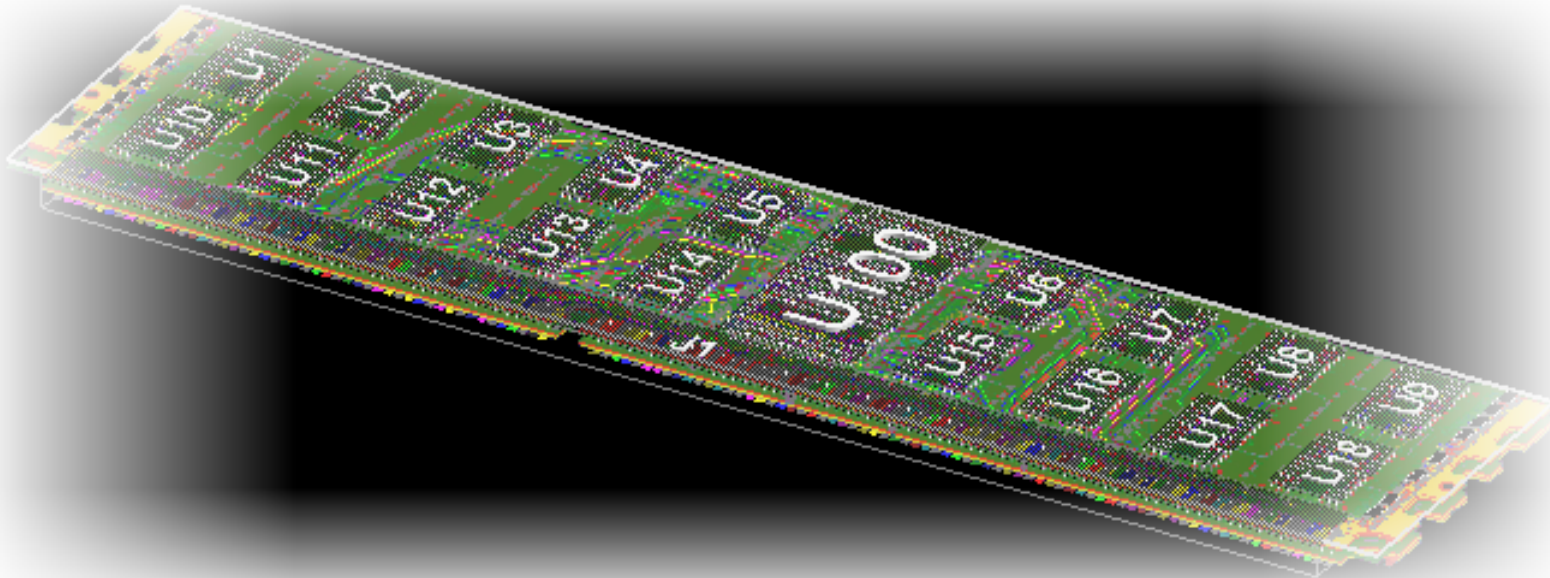
Trace Name	Length (%)	Upper-lyr ref net name	Lower-lyr ref net name
Trace9047::DQ0	11.58	GND	VDD
Trace9048::DQ0	12.74	GND	VDD
Trace9048::DQ0	1.78	VDD	VDD
Trace9048::DQ0	0.11	-	VDD
Trace9048::DQ0	0.89	GND	VDD
Trace9048::DQ0	1.66	GND	GND

*Note:
This is the reason why
there are 5
impedance sections.*



OrCAD ERC/SRC Checking Flow

- Example : DDR3 DIMM module
 - 1 buffer: U100
 - 36 DRAMs: U1 – U36
 - 10 layers



Easy Workflow

The screenshot displays the OrCAD Sigrity ERC - [DDR3_LRDIMM Layer View] interface. The main window shows a PCB layout with a color-coded impedance and coupling analysis. A large red arrow points from the 'Impedance between 2 Components' section in the left-hand 'Workflow: SPEED GENERATOR' pane to the corresponding analysis results in the central layout view.

Workflow: SPEED GENERATOR

- ERC - Trace Imp/Cpl/Ref Check**
- Layout Setup**
 - Load Layout File
 - Check Stackup
 - Prepare Nets
- Simulation Setup**
 - Enable Trace Check Mode
 - Optional: Set up Net Groups
 - Optional: Show Net Groups
 - Set up Trace Check Parameters
 - Save File without Error Check
- Simulation**
 - Start Simulation
- Results and Report**
 - Net Based Tables/Plots**
 - Impedance Summary Table
 - Impedance Detailed Table
 - Coupling Summary Table
 - Coupling Detailed Table
 - Upper/Lower Layer Reference Table
 - Coplanar Reference Table
 - Board Routing Information Table
 - Impedance Layout Overlay
 - Coupling Layout Overlay
 - Impedance between 2 Components**
 - Impedance Plot (collapsed)
 - Impedance Plot (expanded)
 - Impedance Table
 - Impedance Layout Overlay
 - Coupling between 2 Components**
 - Coupling Plot (collapsed)
 - Coupling Plot (expanded)
 - Coupling Table
 - Coupling Layout Overlay
 - Reference between 2 Components**
 - Reference Plot (expanded)

Layer Selection

- Signal\$TOP
- Signal\$L2_SIGNAL
- Signal\$L3_SIGNAL
- Signal\$L4_PWR/GND
- Signal\$L5_SIGNAL
- Signal\$L6_SIGNAL
- Signal\$L7_PWR/GND
- Signal\$L8_SIGNAL
- Signal\$L9_SIGNAL
- Signal\$BOTTOM

Output

Miscellaneous | Mesh - Errors | VariablesCheck |

Output | Folder Browser |

Ver: 16.0.0.1291.0 000 Mouse(mm): X: 121.528, Y: 49.43 Ready



Check Stackup

The image shows two overlapping windows from the Cadence Allegro PCB Editor. The left window is the 'Cross Section Editor' showing a table of layer properties. The right window is the 'Layer Manager -> Stack Up' dialog showing a detailed table of the board stackup. A red arrow points from the 'Cross Section Editor' table to the 'Layer Manager' table.

Cross Section Editor Table:

Objects	Types >>	Thickness >>	Phys
#	Name	Value mm	Layer ID
1	TOP	0.04318	1
2	L2_SIGNAL	0.03048	2
3	L3_SIGNAL	0.03048	3
4	L4_PWR/GND	0.03048	4
5	L5_SIGNAL	0.01524	5
6	L6_SIGNAL	0.01524	6
7	L7_PWR/GND	0.03048	7
8	L8_SIGNAL	0.03048	8
9	L9_SIGNAL	0.03048	9
10	BOTTOM	0.04318	10

Layer Manager -> Stack Up Table:

Layer #	Color	Layer Icon	Layer Name	Thickness...	Material	Conductivity...	Fill-in Dielectric	Er	Loss Tangent	Shape
1			Medium\$40	0.038	SOLDERMASK	0				
			Signal\$TOP	0.04318	COPPER	5.959e+007		3	0	Plane\$
2			Medium\$42	0.057	NPG-170_PP	0				
			Signal\$L2_SIGNAL	0.03048	COPPER	5.959e+007		3.85	0	Signal\$
3			Medium\$44	0.065	NPG-170_PP	0				
			Signal\$L3_SIGNAL	0.03048	COPPER	5.959e+007		3.85	0	Signal\$
4			Signal\$L4_PWR/GND	0.03048	COPPER	5.959e+007		3.85	0	Plane\$
			Medium\$48	0.075	NPG-170_(C...	0				
			Signal\$L5_SIGNAL	0.01524	COPPER	5.959e+007		3.91	0	Signal\$
6			Medium\$50	0.363	NPG-170_PP_1	0				
			Signal\$L6_SIGNAL	0.01524	COPPER	5.959e+007		3.91	0	Signal\$
7			Medium\$52	0.075	NPG-170_(C...	0				
			Signal\$L7_PWR/GND	0.03048	COPPER	5.959e+007		3.85	0	Plane\$
8			Medium\$54	0.074	NPG-170_PP	0				
			Signal\$L8_SIGNAL	0.03048	COPPER	5.959e+007		3.85	0	Signal\$
			Medium\$56	0.065	NPG-170_PP	0				
9			Signal\$L9_SIGNAL	0.03048	COPPER	5.959e+007		3.85	0	Signal\$
			Medium\$58	0.057	NPG-170_PP	0				
10			Signal\$BOTTOM	0.04318	COPPER	5.959e+007		3	0	Plane\$
			Medium\$60	0.038	SOLDERMASK	0				

Properties Panel:

Total thickness: 1.28072 mm
Total thickness without masks: 1.28072 mm
Layers: 10
Conductor: 6
Plane: 4
Mask: 0

Layer Manager -> Stack Up Summary:

Total Thickness: 1.2807e+000 mm

Unit: mm

Classify Nets

The screenshot displays the OrCAD Sigrity ERC interface for a DDR3_LRDIMM Layer View. The central workspace shows a PCB layout with components labeled U1 through U18 and U100. The left sidebar contains the 'ERC - Trace Imp/Cpl/Ref Check' panel, with the 'Simulation Setup' section highlighted by a red box. This section includes the following steps:

1. Open Net Manager
2. Classify P/G nets
3. Enable signal nets for Trace Check

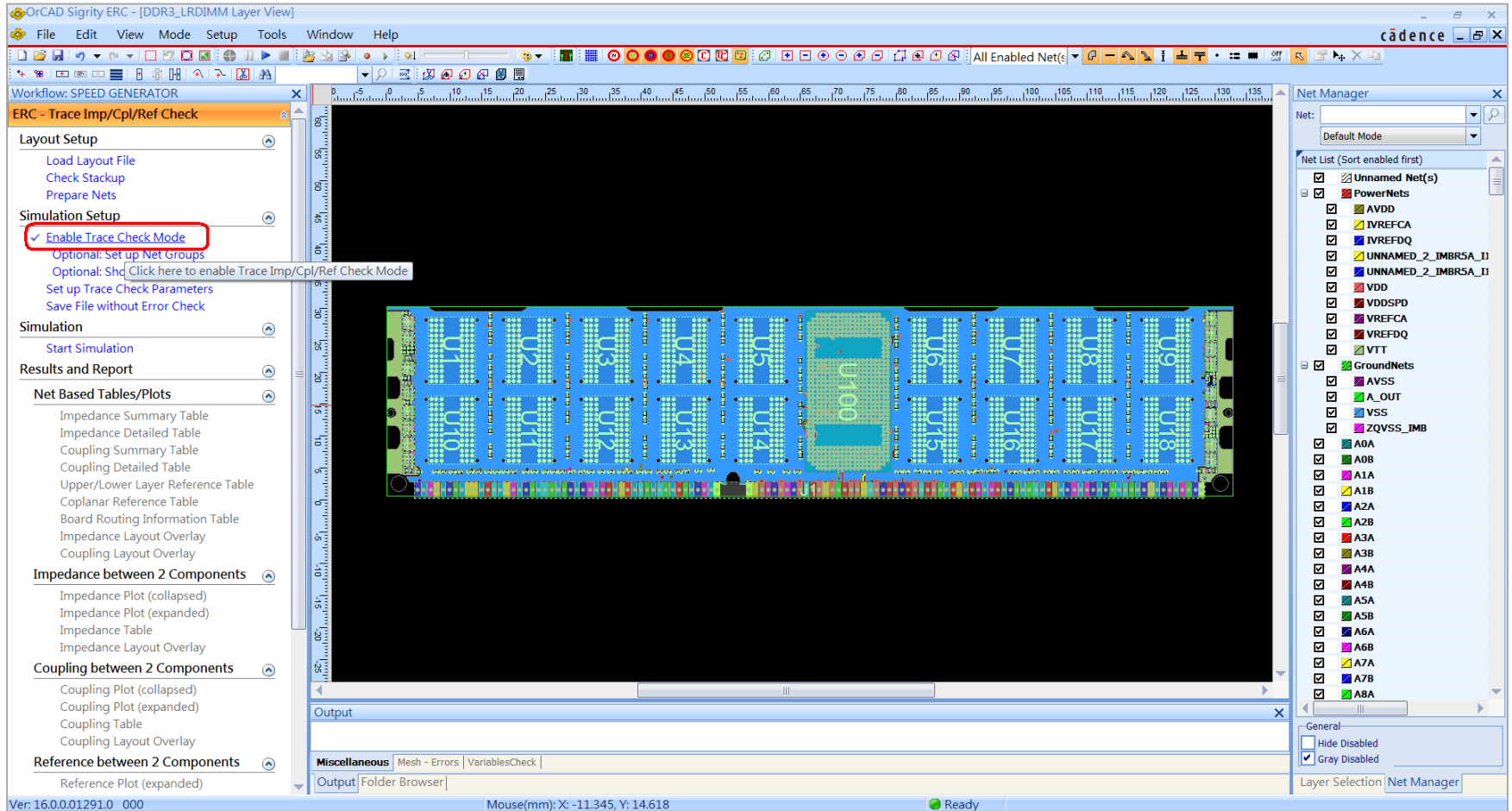
The right sidebar shows the 'Net Manager' panel, which is also highlighted by a red box. It displays a 'Net List (Sort enabled first)' with the following categories and items:

- Unnamed Net(s)
- PowerNets
 - AVDD
 - IVREFCA
 - IVREFDQ
 - UNNAMED_2_IMBRSA_I1
 - UNNAMED_2_IMBRSA_I2
 - VDD
 - VDDSPD
 - VREFCA
 - VREFDQ
 - VTT
- GroundNets
 - AVSS
 - A_OUT
 - VSS
 - ZQVSS_IMB
- A0A
- A0B
- A1A
- A1B
- A2A
- A2B
- A3A
- A3B
- A4A
- A4B
- A5A
- A5B
- A6A
- A6B
- A7A
- A7B
- A8A

The 'Net Manager' panel also includes a 'General' section with 'Hide Disabled' and 'Gray Disabled' options, and a 'Layer Selection' section with 'Net Manager' selected.



Enable Trace Check Mode



Nets Select Tx & Rx Components

Workflow: SPEED GENERATOR
ERC - Trace Imp/Cpl/Ref Check

Layout Setup
Load Layout File
Check Stackup
Prepare Nets

Simulation Setup
Enable Trace Check Mode
Optional: Set up Net Groups
Optional: Show Net Groups
Set up Trace Check Parameters
Save File without Error Check

Simulation
Start Simulation

Results and Report
Net Based Tables/Plots
Impedance Summary Table
Impedance Detailed Table
Coupling Summary Table
Coupling Detailed Table
Upper/Lower Layer Reference Table
Coplanar Reference Table
Board Routing Information Table
Impedance Layout Overlay
Coupling Layout Overlay

Impedance between 2 Components
Impedance Plot (collapsed)

Trace check setup -> Net groups
Net group names

Ver: 16.0.0.1291.0_000

Set up NG wizard: Tx page
Select Tx component or memory controller
Find component by name: [Search]
Model Name
8P4R_0402-36_5%_36
240PIN_CONN_DDR3
DDR3_ZSRALL_V0_05TV_E0_PGA
EEPROM
IMB
Set up NG wizard: Tx page

Select Tx component or memory controller
Find component by name: [Search]
Model Name
 U9
 U10
 U11
 U12
 U13
 U14
 U15
 U16
 U17
 U18
 U19
 U20
 U21
 U22
 U23
 U24
 U25
 U26
 U27
 U28
 U29
 U30
 U31
 U32
 U33
 U34
 U35
 U36
 IMB_RSA
 U100

Show component with pin number => 50 pins Update

< 上一步(B) 下一步(N) > 取消

cadence
All Enabled Net(s)
Net Manager
Net: [Search]
Default Mode
Net List (Sort enabled first)
 Unnamed Net(s)
 PowerNets
 AVDD
 IVREFCA
 IVREFDQ
 UNNAMED_2_IMBR5A_I1
 UNNAMED_2_IMBR5A_I1
 VDD
 VDDSPD
 VREFCA
 VREFDQ
 VTT
 GroundNets
 AVSS
 A_OUT
 VSS
 ZQVSS_IMB
 A0A
 A0B
 A1A
 A1B

General
 Hide Disabled
 Gray Disabled
Layer Selection Net Manager

Rx component(s)

Import Net Groups Net Groups Wizard

Select Tx (Rx)
Component

Set up Net Groups (Signal nets)

The screenshot displays the OrCAD Sigrity ERC interface with the Net Groups Wizard open. The wizard is currently on the "NG pre-view page", which shows a preview of the net groups that will be created. The wizard consists of several steps: "Set up NG wizard: P/G nets page", "Set up NG wizard: Signal nets found page", and "Set up NG wizard: NG pre-view page".

The "Set up NG wizard: Signal nets found page" shows a list of components to be included in the net groups:

Tx component	Net name	Net name
<input checked="" type="checkbox"/> U100	A0A	-
<input checked="" type="checkbox"/> U100	A0B	-
<input checked="" type="checkbox"/> U100	A1A	-
<input checked="" type="checkbox"/> U100	A1B	-
<input checked="" type="checkbox"/> U100	A2A	-
<input checked="" type="checkbox"/> U100	A2B	-
<input checked="" type="checkbox"/> U100	A3A	-
<input checked="" type="checkbox"/> U100	A3B	-
<input checked="" type="checkbox"/> U100	A4A	-
<input checked="" type="checkbox"/> U100	A4B	-
<input checked="" type="checkbox"/> U100	A5A	-
<input checked="" type="checkbox"/> U100	A5B	-
<input checked="" type="checkbox"/> U100	A6A	-
<input checked="" type="checkbox"/> U100	A6B	-
<input checked="" type="checkbox"/> U100	A7A	-
<input checked="" type="checkbox"/> U100	A7B	-
<input checked="" type="checkbox"/> U100	A8A	-
<input checked="" type="checkbox"/> U100	A8B	-
<input checked="" type="checkbox"/> U100	A9A	-
<input checked="" type="checkbox"/> U100	A9B	-
<input checked="" type="checkbox"/> U100	A10A	-
<input checked="" type="checkbox"/> U100	A10B	-
<input checked="" type="checkbox"/> U100	A11A	-
<input checked="" type="checkbox"/> U100	A11B	-

The "Set up NG wizard: NG pre-view page" shows a preview of the net groups:

Net group names	Tx component	Net name	Rx component(s)
ddr_U100_U11...			
	U100	MDQ0	U1, U10, U27, U36
	U100	MDQ1	U1, U10, U27, U36
	U100	MDQ2	U1, U10, U27, U36
	U100	MDQ3	U1, U10, U27, U36
	U100	MDQ4	U1, U10, U27, U36
	U100	MDQ5	U1, U10, U27, U36
	U100	MDQ6	U1, U10, U27, U36
	U100	MDQ7	U1, U10, U27, U36
ddr_U100_U12...			
	U100	MDQ8	U11, U2, U26, U35
	U100	MDQ9	U11, U2, U26, U35
	U100	MDQ10	U11, U2, U26, U35
	U100	MDQ11	U11, U2, U26, U35
	U100	MDQ12	U11, U2, U26, U35
	U100	MDQ13	U11, U2, U26, U35
	U100	MDQ14	U11, U2, U26, U35
	U100	MDQ15	U11, U2, U26, U35
ddr_U100_U13...			
	U100	MDQ16	U12, U25, U3, U34
	U100	MDQ17	U12, U25, U3, U34
	U100	MDQ18	U12, U25, U3, U34
	U100	MDQ19	U12, U25, U3, U34
	U100	MDQ20	U12, U25, U3, U34
	U100	MDQ21	U12, U25, U3, U34
	U100	MDQ22	U12, U25, U3, U34
	U100	MDQ23	U12, U25, U3, U34
	U100	MDQ24	U13, U24, U33, U4
	U100	MDQ25	U13, U24, U33, U4
	U100	MDQ26	U13, U24, U33, U4
	U100	MDQ27	U13, U24, U33, U4
	U100	MDQ28	U13, U24, U33, U4
	U100	MDQ29	U13, U24, U33, U4

The "Set up NG wizard: Signal nets found page" shows a list of signal nets:

Net name	Rx component	Interface
U19, U20, U21, U22...	RP15, RP17, U1, U2...	ddr
RP15, RP17, U1, U2...	RP15, RP17, U19, U...	ddr
RP23, RP28, U28, U...	RP23, RP28, U10, U...	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr
U14, U23, U32, U5	U14, U23, U32, U5	ddr

Simulation & View Result

Cross-link result

- Trace impedance checking
- Trace coupling effect checking
- Trace reference plane checking

Command
Grids are drawn 2.5600, 2.5600 apart for enhanced visibility.
Grids are drawn 1.2800, 1.2800 apart for enhanced visibility.

Results and Report

Net Based Tables/Plots

- Impedance Summary Table
- Impedance Detailed Table
- Coupling Summary Table
- Coupling Detailed Table
- Upper/Lower Layer Reference Table
- Coplanar Reference Table
- Board Routing Information Table
- Impedance Layout Overlay
- Coupling Layout Overlay
- Impedance between 2 Components**
- Impedance Plot (collapsed)
- Impedance Plot (expanded)
- Impedance Table
- Impedance Layout Overlay
- Coupling between 2 Components**
- Coupling Plot (collapsed)
- Coupling Plot (expanded)
- Coupling Table
- Coupling Layout Overlay
- Reference between 2 Components**
- Reference Plot (expanded)

Net Manager

Net: [dropdown]
Show Coupled Line [dropdown]

Net List (Sort enabled first)

- Unnamed Net(s)
- PowerNets
 - AVDD
 - IVREFCA
 - IVREFDQ
 - UNNAMED_2_IMBRSA_I168
 - UNNAMED_2_IMBRSA_I168
 - VDD
 - VDDSPD
 - VREFCA
 - VREFDQ
 - VTT
- GroundNets
 - AVSS
 - A_OUT
 - VSS
 - ZQVSS_IMB
- A0A
- A0B
- A1A
- A1B
- A2A
- A2B
- A3A
- A3B
- A4A
- A4B
- A5A
- A5B
- A6A

General

- Hide Disabled
- Gray Disabled

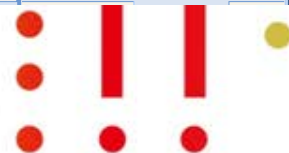
Coupled Lines

- Disable Coupled Line Simulation

Coupled Lines Report

Output

Breaking Traces ...
Forming Coupled Traces



Trace Impedance Check

Impedance Plot (collapsed)

- P3E_SLOT2_TX_C_DP0
- P3E_SLOT2_TX_C_DP1
- P3E_SLOT2_TX_C_DP2
- P3E_SLOT2_TX_C_DP3
- P3E_SLOT2_TX_C_DP4

Impedance (Ohm)

220

140

120

100

80

0

197

394

591

787

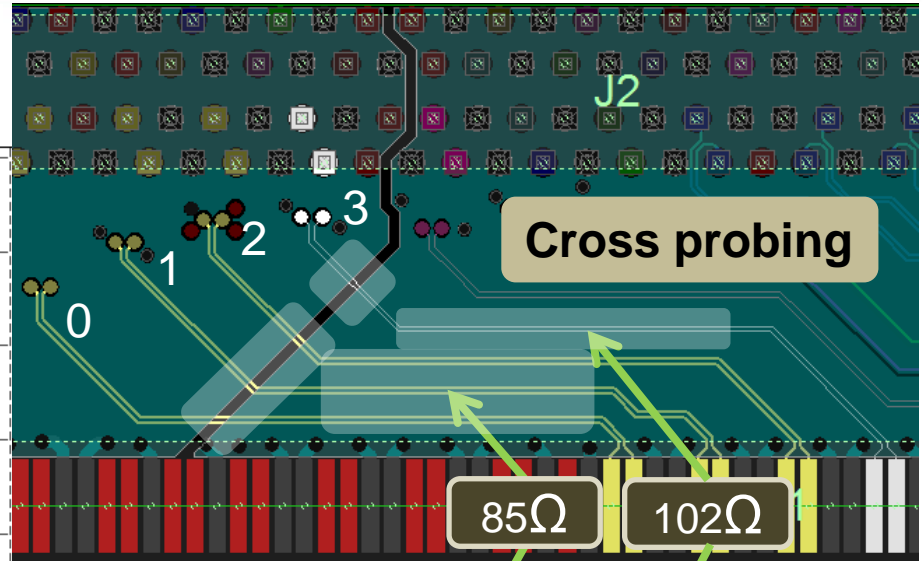
984

1181

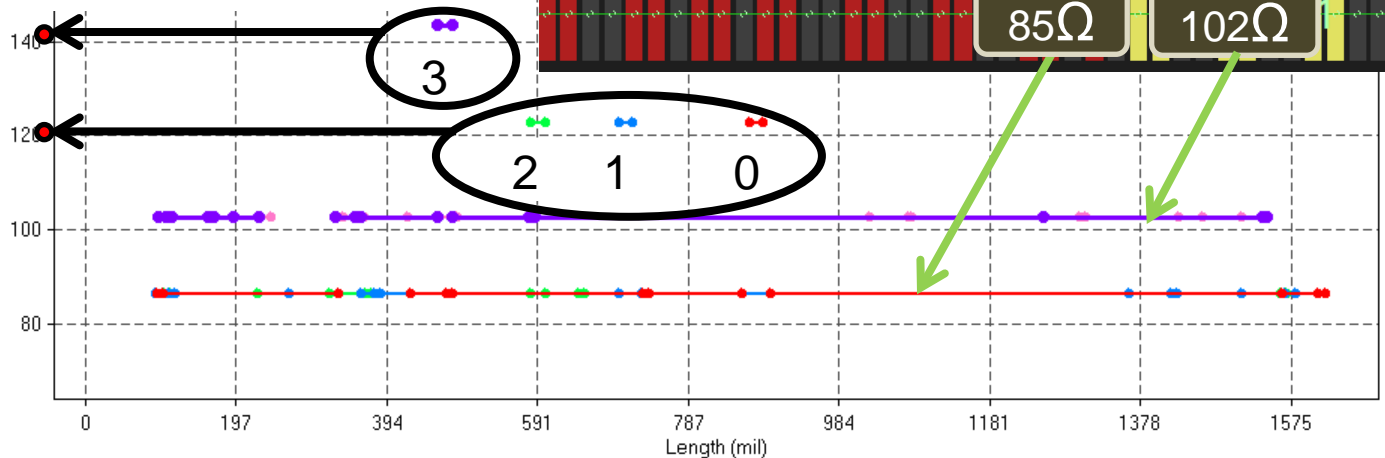
1378

1575

Length (mil)



- This check helps you to identify,
 - Wrong trace width spacing (diff. pair)
 - Cross moat
 - Highly trace impedance



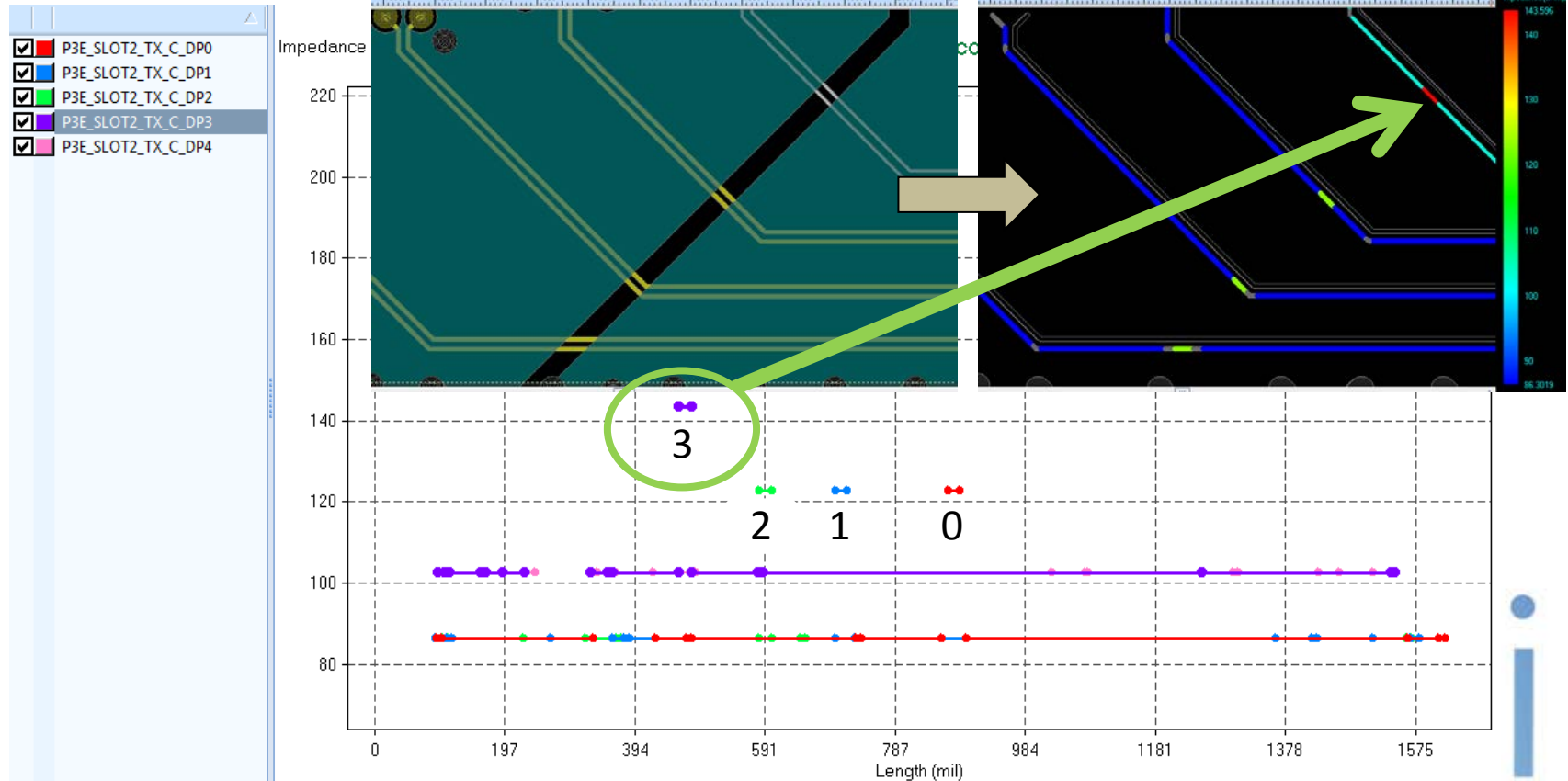
- Visually or tabular result for trace impedance check that shows trace segments mismatch with target impedance.



Trace Impedance Check

Cross Probing

Impedance Plot (collapsed)

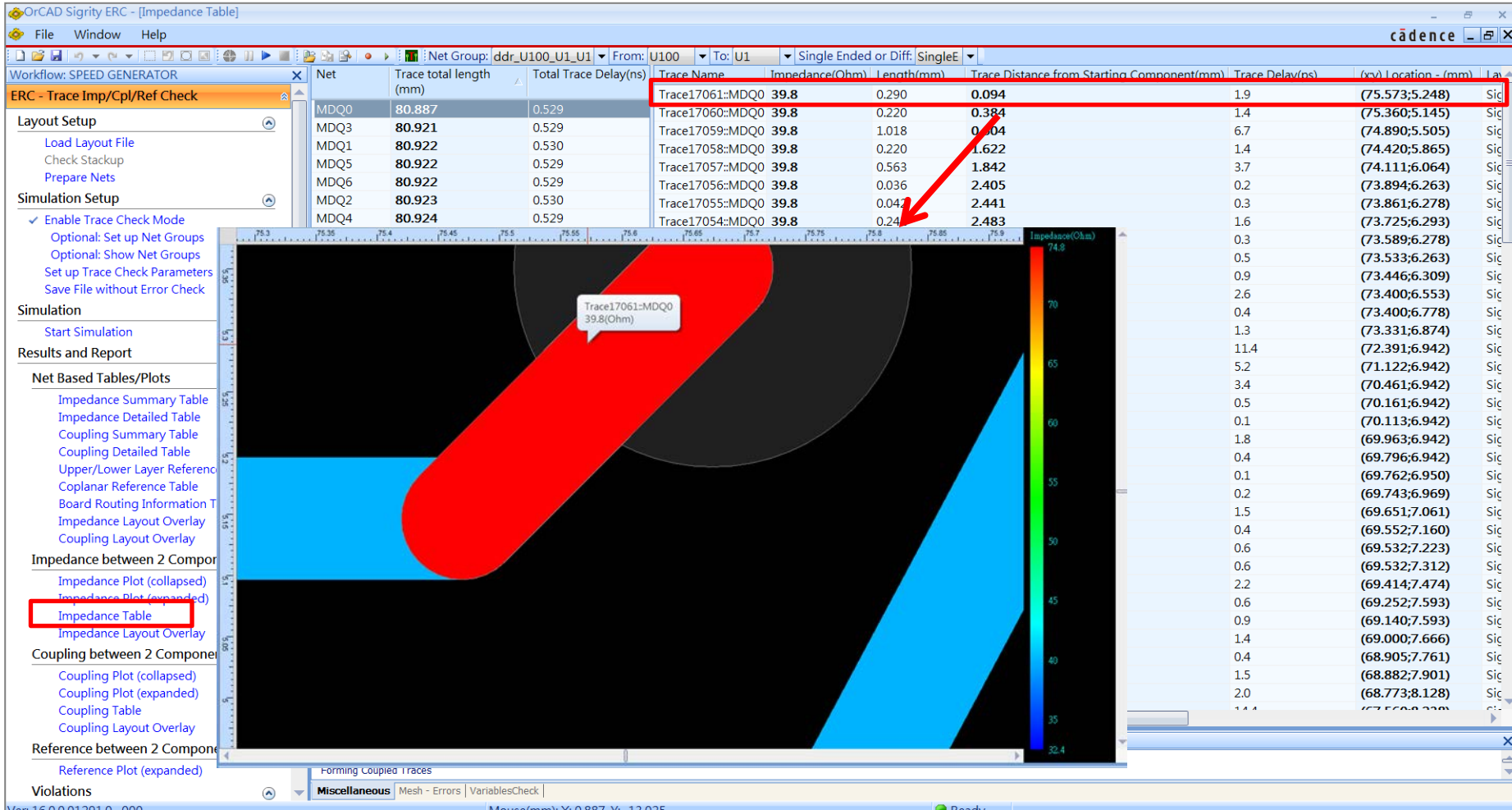


- Cross probing allows you to identify defects quickly.



Trace Impedance Check

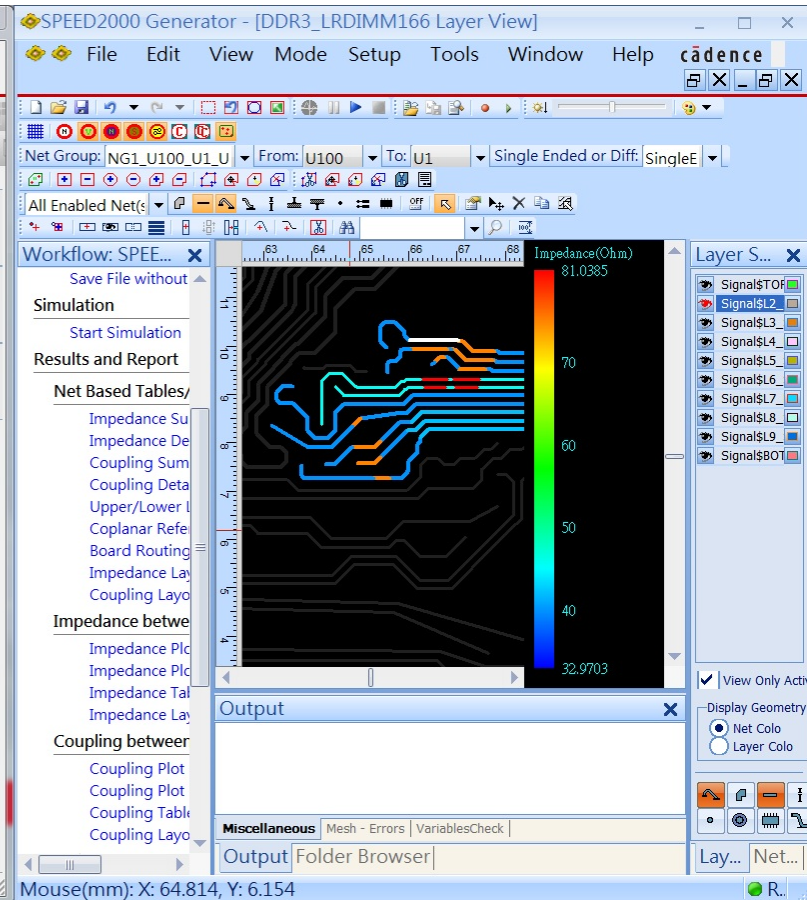
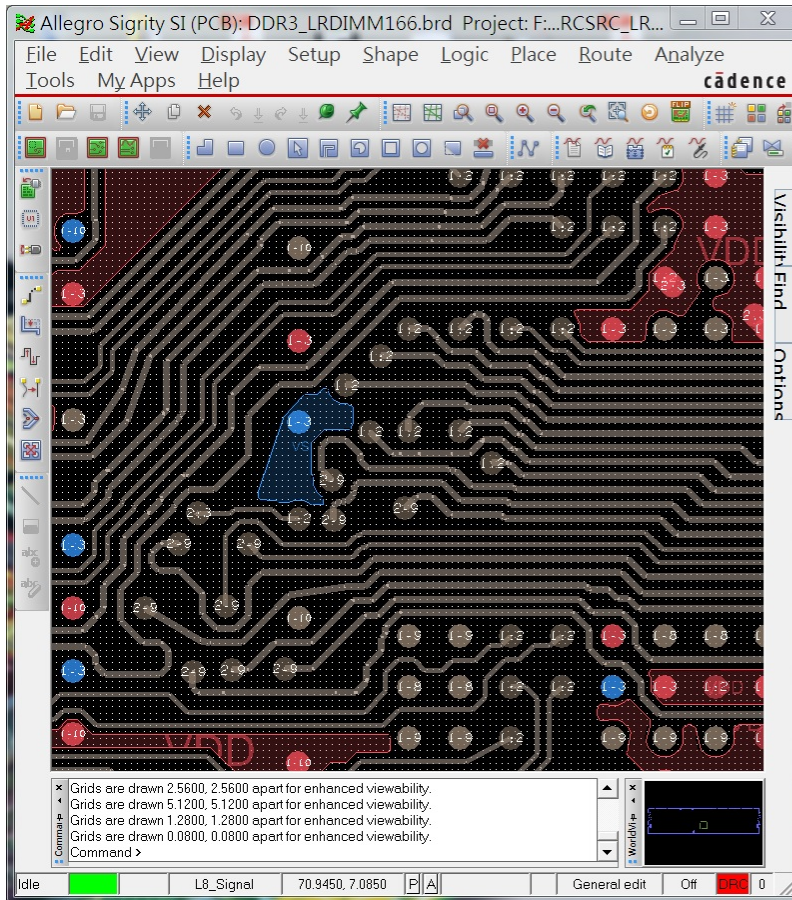
Tabular Results



Trace Impedance Check

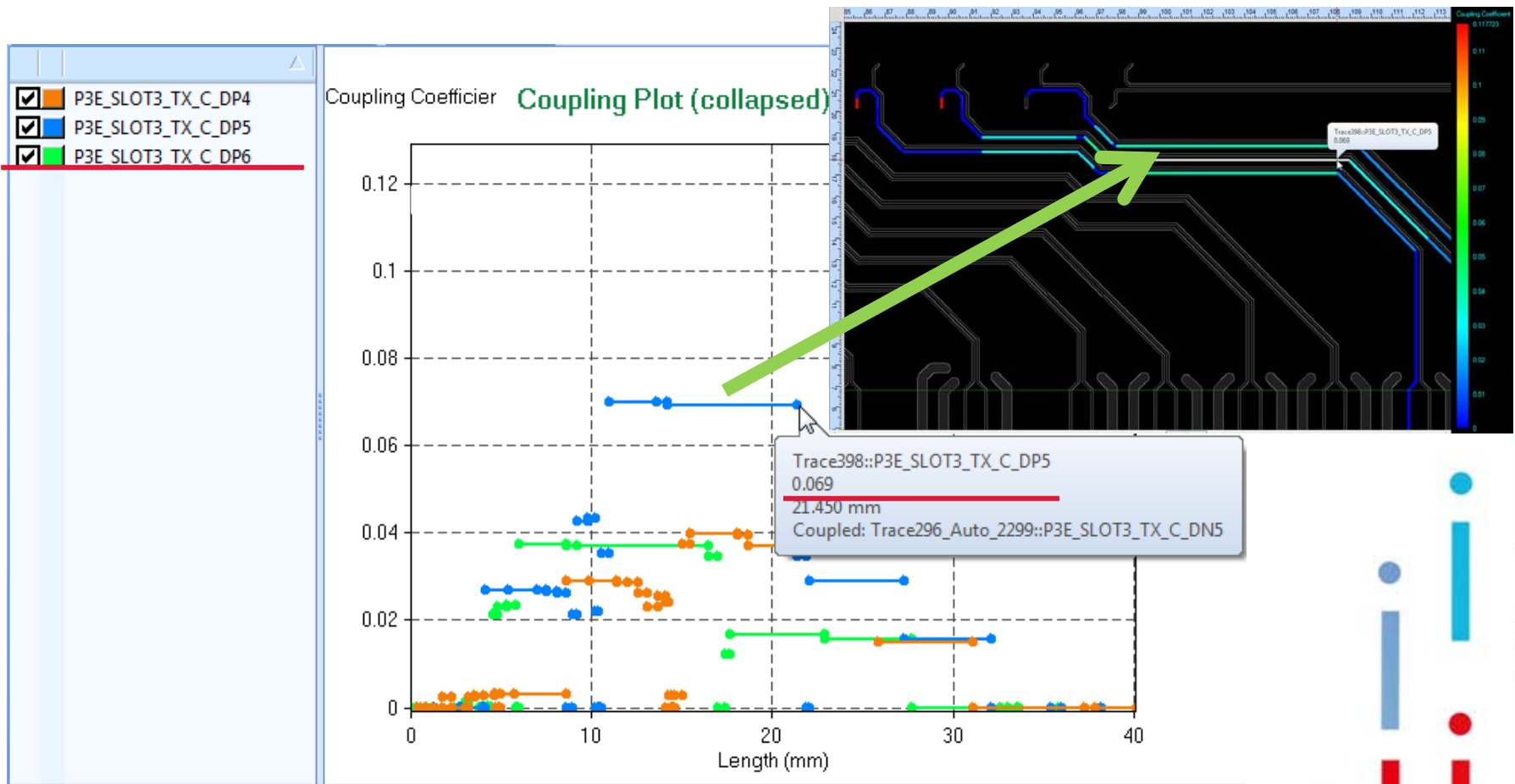
Auto-Zoom in board

Impedance Layout Overlay

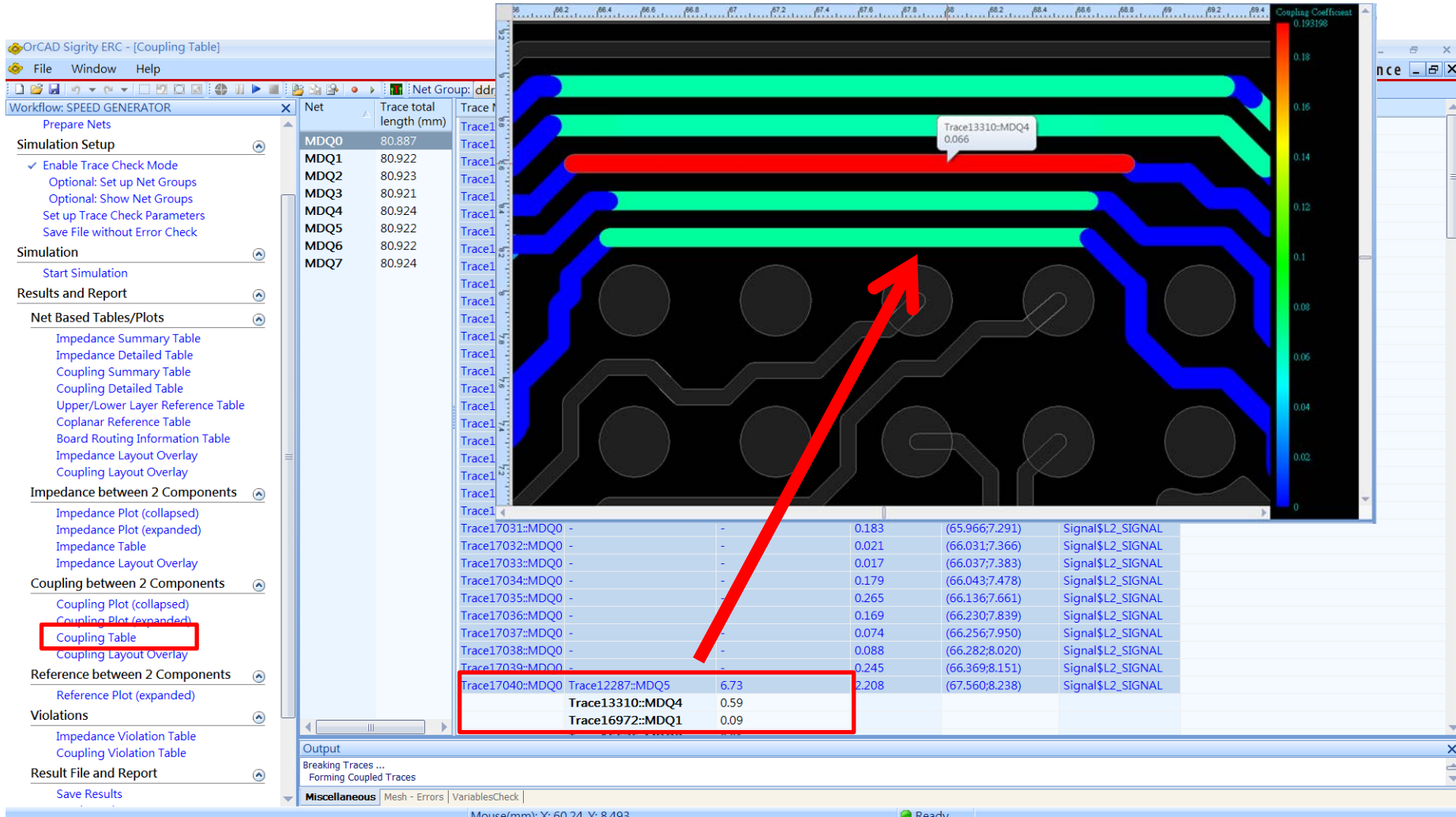


Trace Coupling Check

Cross probing helps to resolve issue intuitively

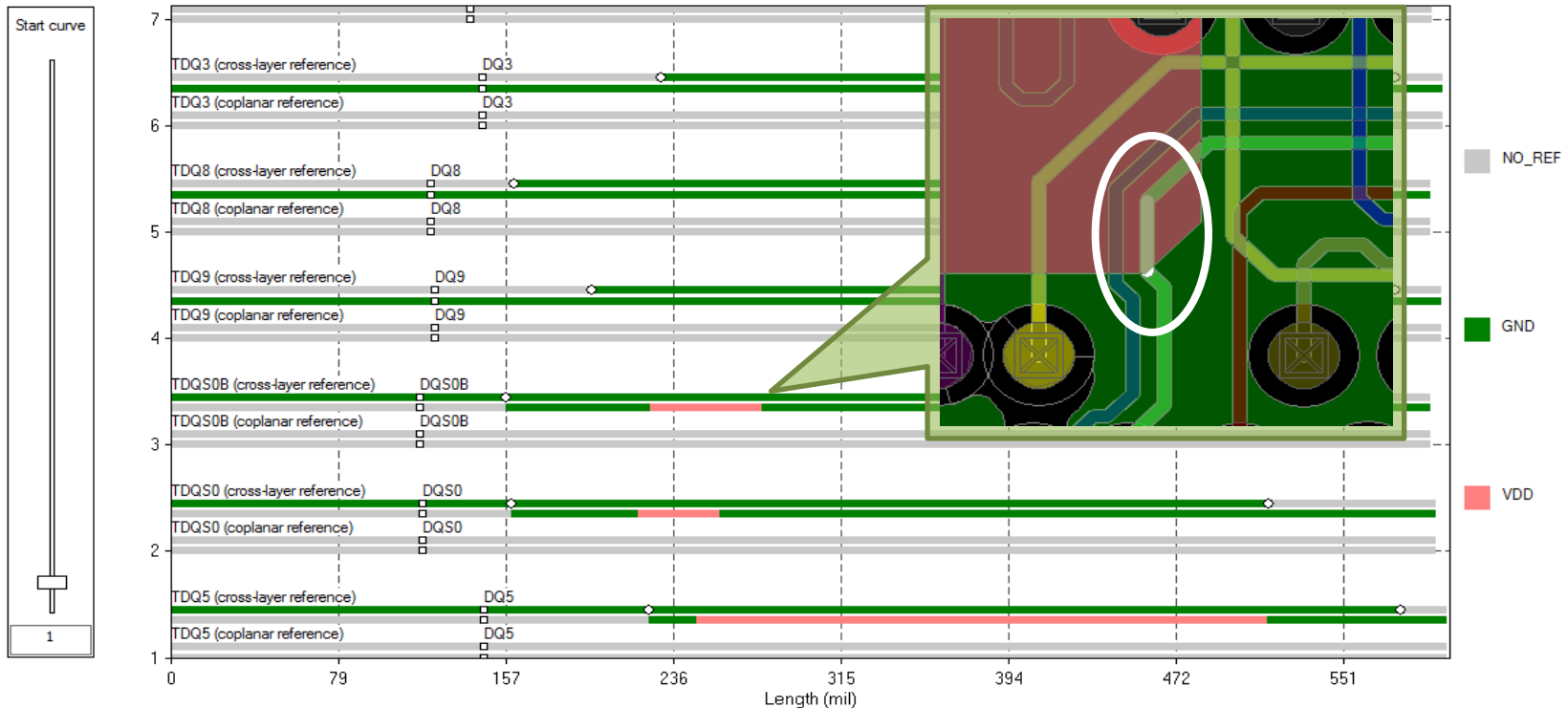


Trace Coupling Check



Trace Reference Check (Including co-planar)

Trace Reference Plot (expanded)



- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

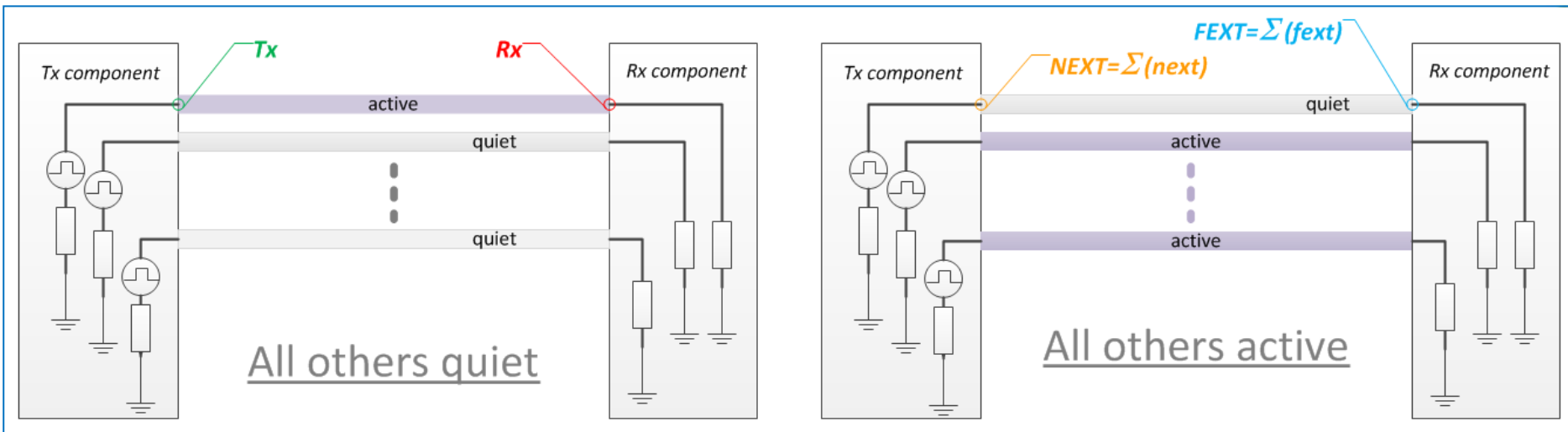
Signal Base Checker - SRC



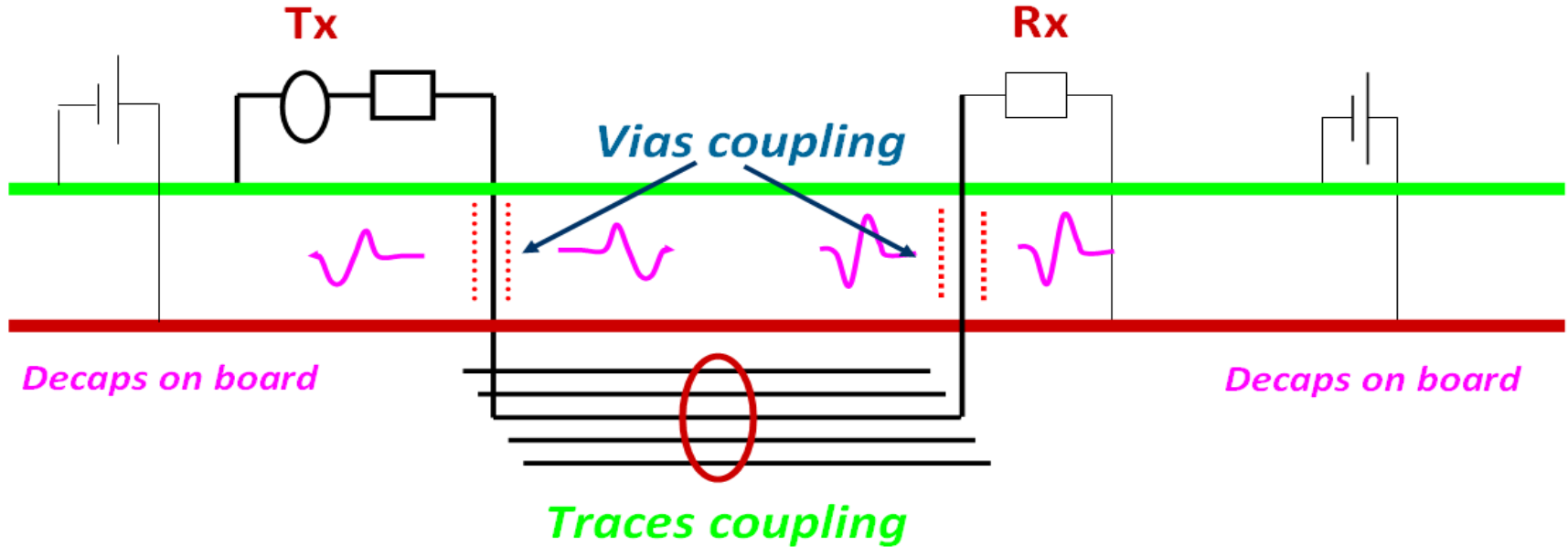
What is Sigrity SRC?

- OrCAD® Sigrity™ SRC is Macro, combined, net-level view in time-domain of impact due to ERC violations measured in mv&ps (no device model needed)
 - Setup considering termination impedance, data rate (pulse width, rise/fall time), and amplitude
 - Results with Tx/Rx/NEXT/FEXT waveforms, SI performance metrics
 - Organized to easy SI performance interpretation along with ERC
- Practical for board level check (setup, simulation, report)

<2min ~ 20min auto



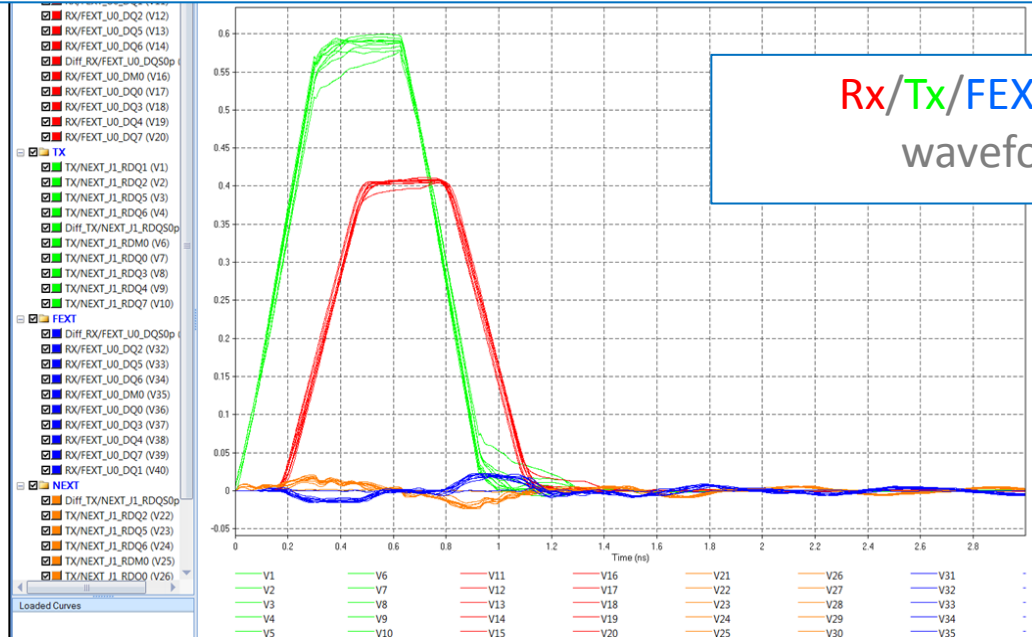
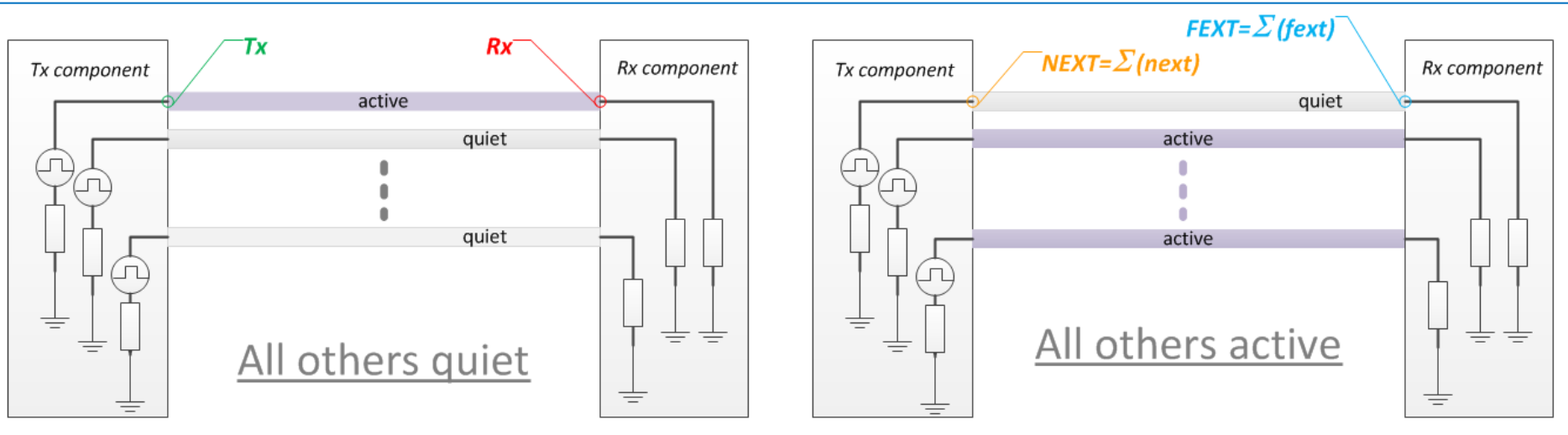
SI Channel Check



- Signal quality is affected by crosstalk among signals, EM coupling between signal and P/G planes and non-ideal return current path.
- The linear source and load are applied automatically for signal TD simulation
- Post process result waveforms (signal waveform, NEXT/FEXT waveforms) into signal to noise ratio for signal quality judgment



Time-domain Waveforms



Rx/Tx/FEXT/NEXT waveforms



Setup Models

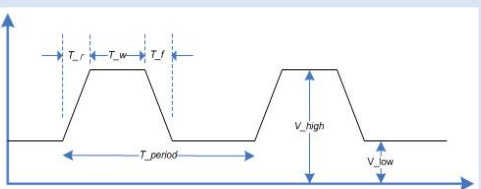
OrCAD Sigrity ERC - [DDR3_LRDIMM Layer View] | Set up SI Metrics Check Wizard

Select and enable nets for check simulation

Find component by name:

Net group names	Tx component	Net name	Rx component(s)	Rx component(s) populated	FIR filter	Pulse center
<input checked="" type="checkbox"/> d...	U100	M...	U1	U10,U2...	-	v-edge

Set up Tx/Rx Models

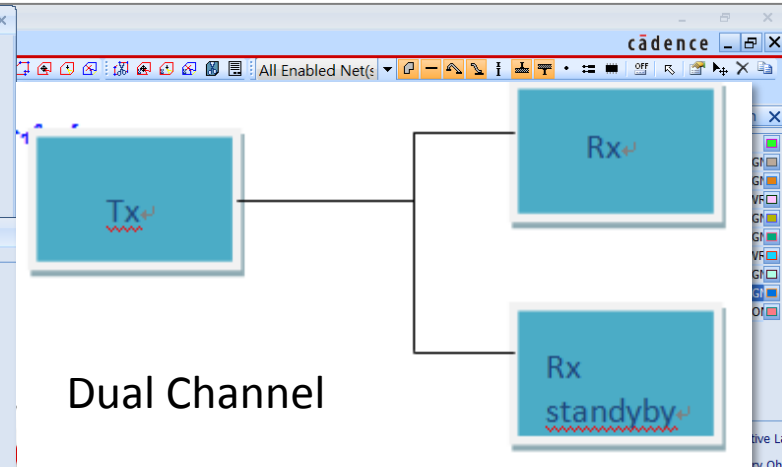


Import Tx/Rx Models | Export Tx/Rx Models

Interface and ckt type	Tx										Rx		Rx(Standby)			
	Tx_term type	R(ohm)	C(F)	V_low(V)	V_high(V)	Tdelay	T_r(s)	T_f(s)	T_w(s)	T_period(s)	Rx_term type	R(ohm)	C(F)	S/Rx_term type	(S)R(ohm)	(S)C(F)
ddr:SE	R	50	-	0	1	0p	100p	100p	525p	30n	R	50	-	R	50	-
ddr:Diff																

TX | RX | RX(Standby)

< 上一步(B) | 完成 | 取消



Net Color | Layer Color

Layer ... | Net M...

Import Net Groups | Net Groups Wizard | SI Metrics Wizard

Set up Simulation Option

OrCAD Sigrity ERC - [DDR3_LRDIMM Layer View]

File Edit View Mode Setup Tools Window Help

Workflow: SPEED GENERATOR

ERC - Trace Imp/Cpl/Ref Check

SRC - SI Metrics Check (Ideal P/G)

Layout Setup

- Load Layout File
- Check Stackup
- Prepare Nets

Set up SI Metrics Simulation

- Enable SI Metrics Check Mode
- Set up Net Groups
- Set up Models
- Set up Simulation Option**
- Save File with Error Check

Simulation

- Start Simulation

Result and Report

- Generate SI Metrics Check Report
- Save SI Metrics Check Report
- Load SI Metrics Check Results

Customize Workflow

Set up Simulation Option

- Level-1 (Single lines with ideal PDN; delay, loss, reflection effects)
- Level-2 (Coupled lines with ideal PDN; plus trace, via xtalk effects)
- Level-3 (Coupled lines with non-ideal PDN; plus return path and SSO effects)
- Level-4 (3DFEM model based; lack of reference cases) From SPEED2000

Transient Time Step (ps):

Coupling (%):

Rise Time (ps):

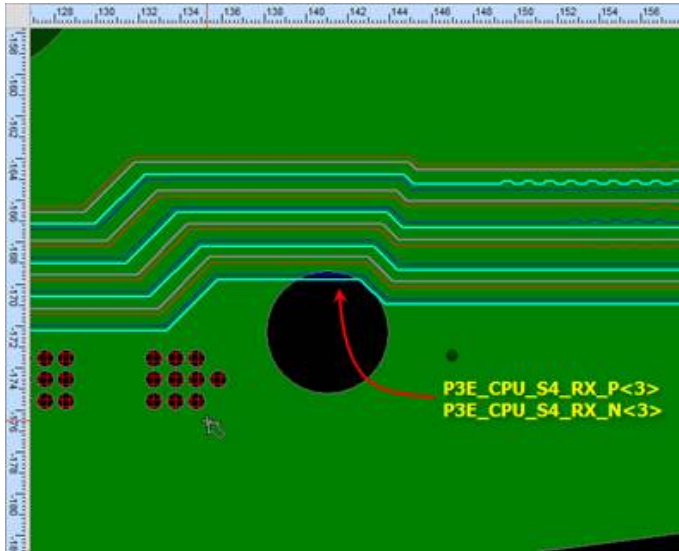
Sim Time:

Power-aware

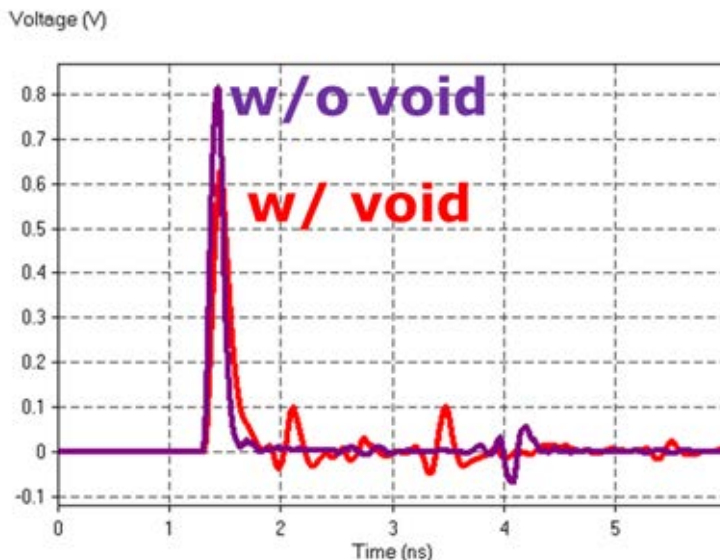
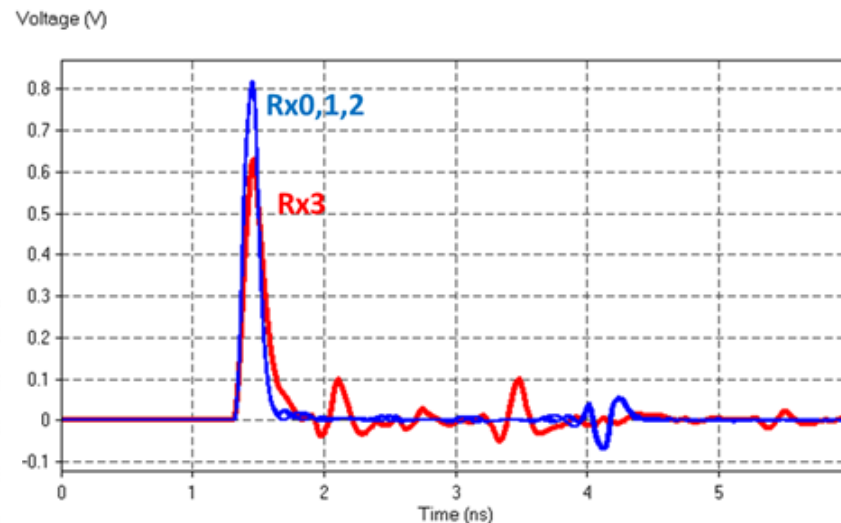
OK Cancel

Ver: 16.0.0.01291.0 000 Mouse(mm): X: -9.08, Y: 7.059 Ready

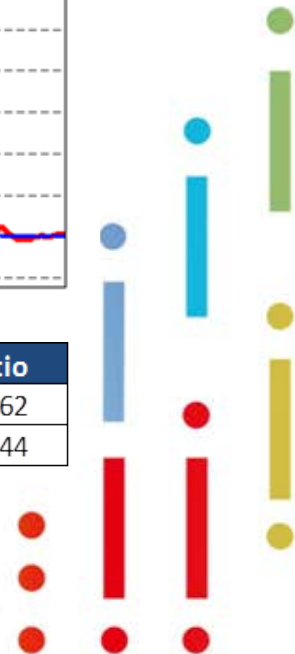
SI Channel Check



- An example shows the trace segment is over the void that causes impedance discontinuity and leads to worse signal quality



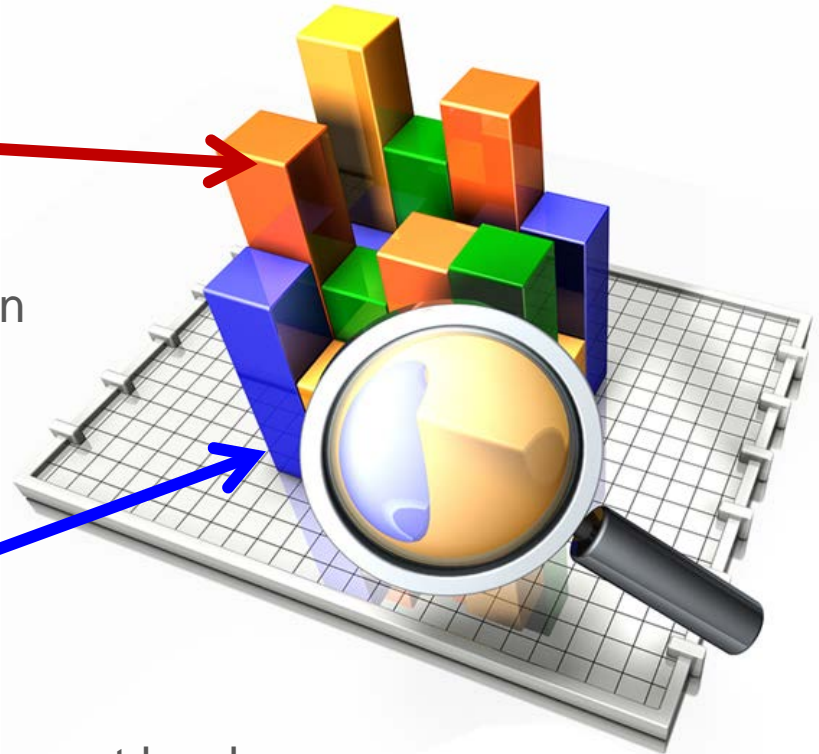
	INT_Sig	INT_ISI	INT_XTK	P-eye	P-ratio
RX3 w/ void	67.84	104.59	5.12	-41.87	0.62
RX3 w/o void	86.00	54.64	5.00	26.36	1.44



SRC Net-level View → ERC's Segment-level View

Sigrity™ SRG

- Layout SI macro view at net level
- All inclusive end results
- Shows what happened and its effect on performance



Sigrity™ ERC

- Layout SI micro level view at segment level
- Individual segmented results
- Shows why low performance happened and how to fix it



Summary

- **OrCAD® Sigrity™ ERC/SRC** fills the gap between layout designers and SI engineers
 - Expanded expertise
 - Using **same** tools
 - Measured by **same** units



Layout/Board designer -----> *SI engineer*

Layout tools -----> *Simulation tools*

Geometry domain (mil/mm) -----> *Electrical domain (mv, ps)*



Thank You

