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Getting Confidence
in Your Design Early!

Graser User Conference

Taipei

2016 7.14

跨界整合 翻轉設計

Graser User Conference Taipei

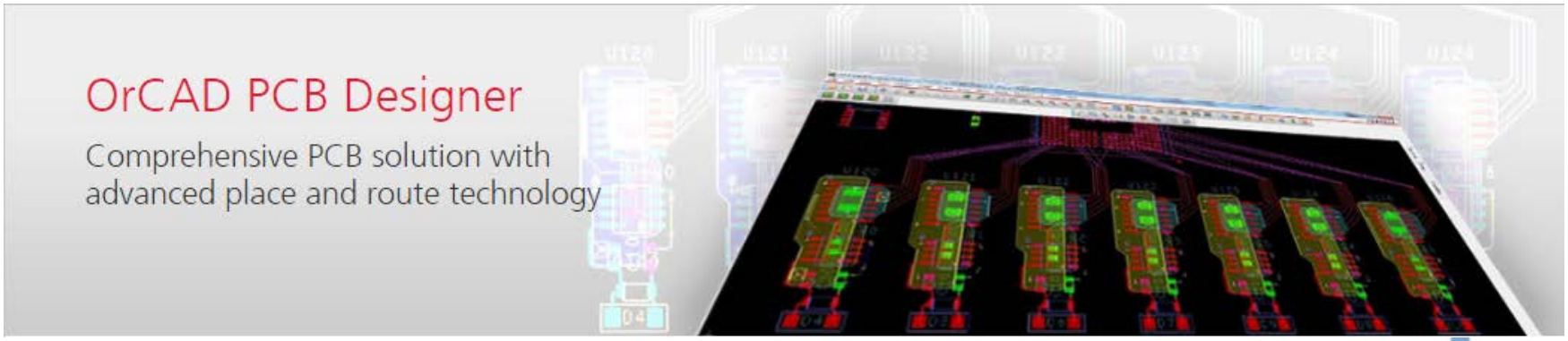
OrCAD® PCB Designer
佈線與訊號阻抗驗證

Mark Wu/ Graser

14 / July / 2016

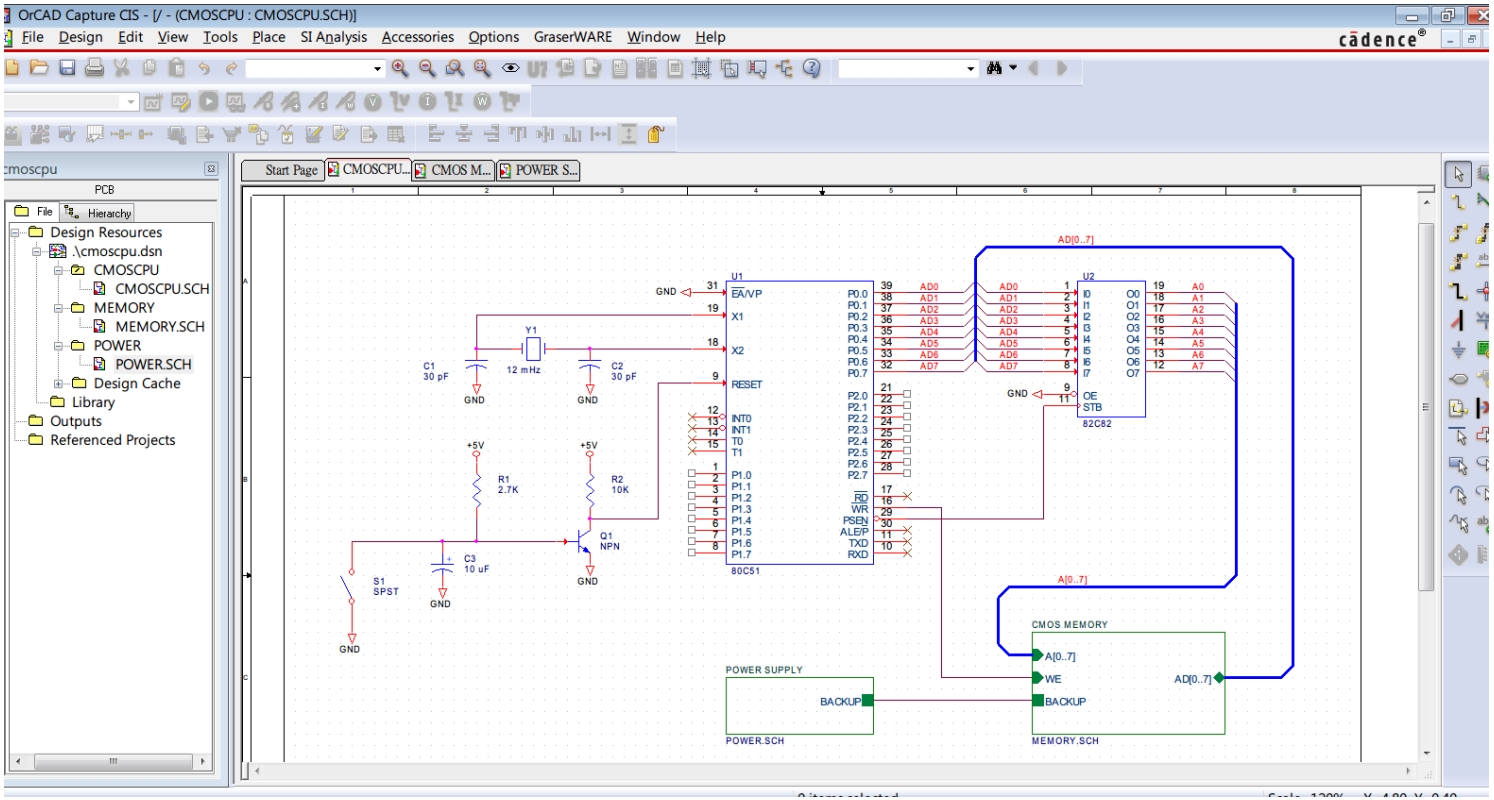
What's OrCAD PCB Designer?

- OrCAD® PCB Designer is powerful, tightly integrated PCB design technologies
  - Include Capture schematic
  - Constraint Manager setting
  - PCB editing and routing
  - Signal integrity and auto routing
  - Optional mixed-signal circuit simulation



OrCAD Capture CIS Support

- Powerful Schematic Entry
  - Streamline the creation of your more complex schematic designs with hierarchical and reuse design capabilities



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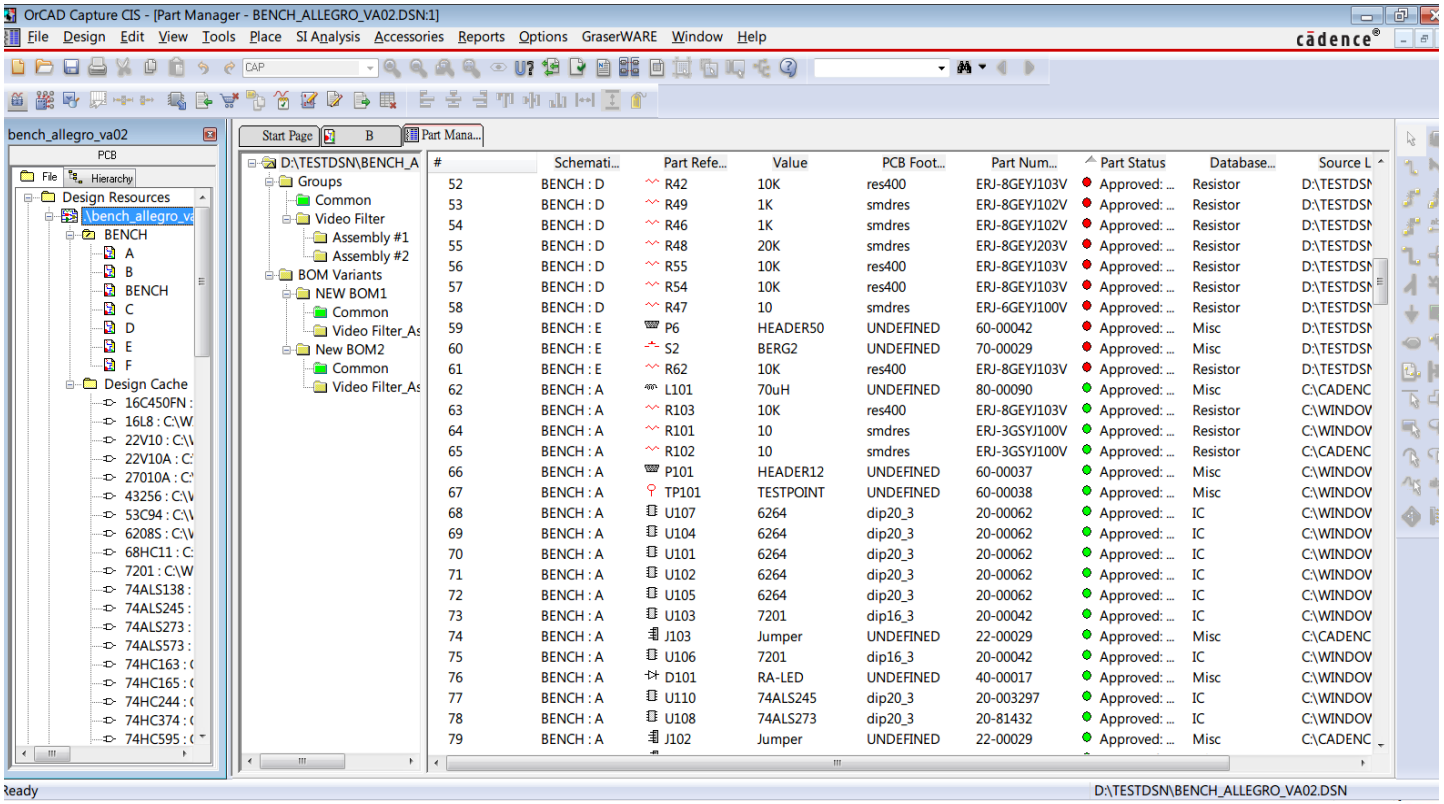
OrCAD Capture CIS Support

- Powerful part management
  - OrCAD® Capture CIS (Component Information System) provides easy access to your company's component databases and part information.



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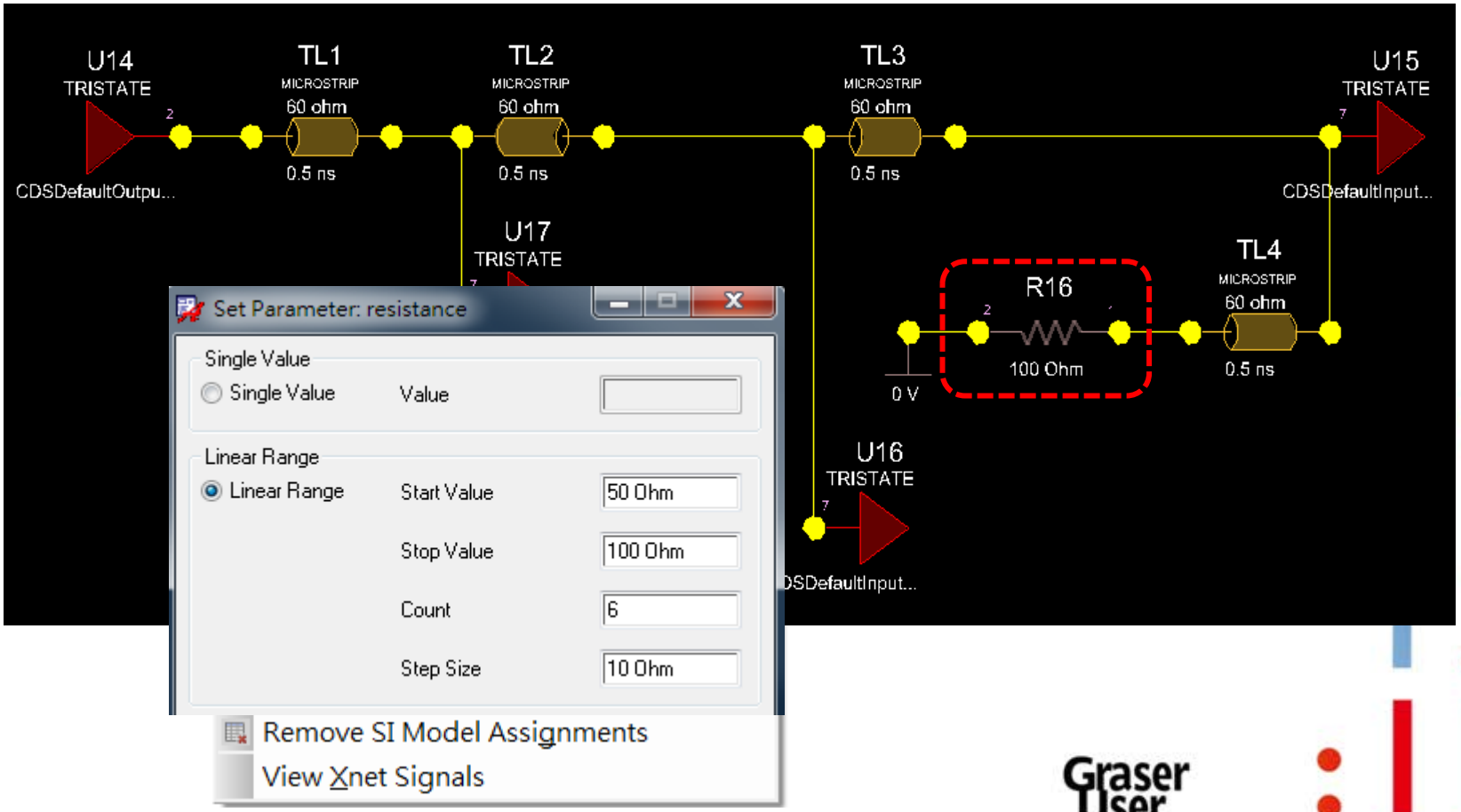
Pre-Simulation

- Easy to perform quick and accurate SI analysis on nets in OrCAD® PCB Designer. Impendence Control - Terminator



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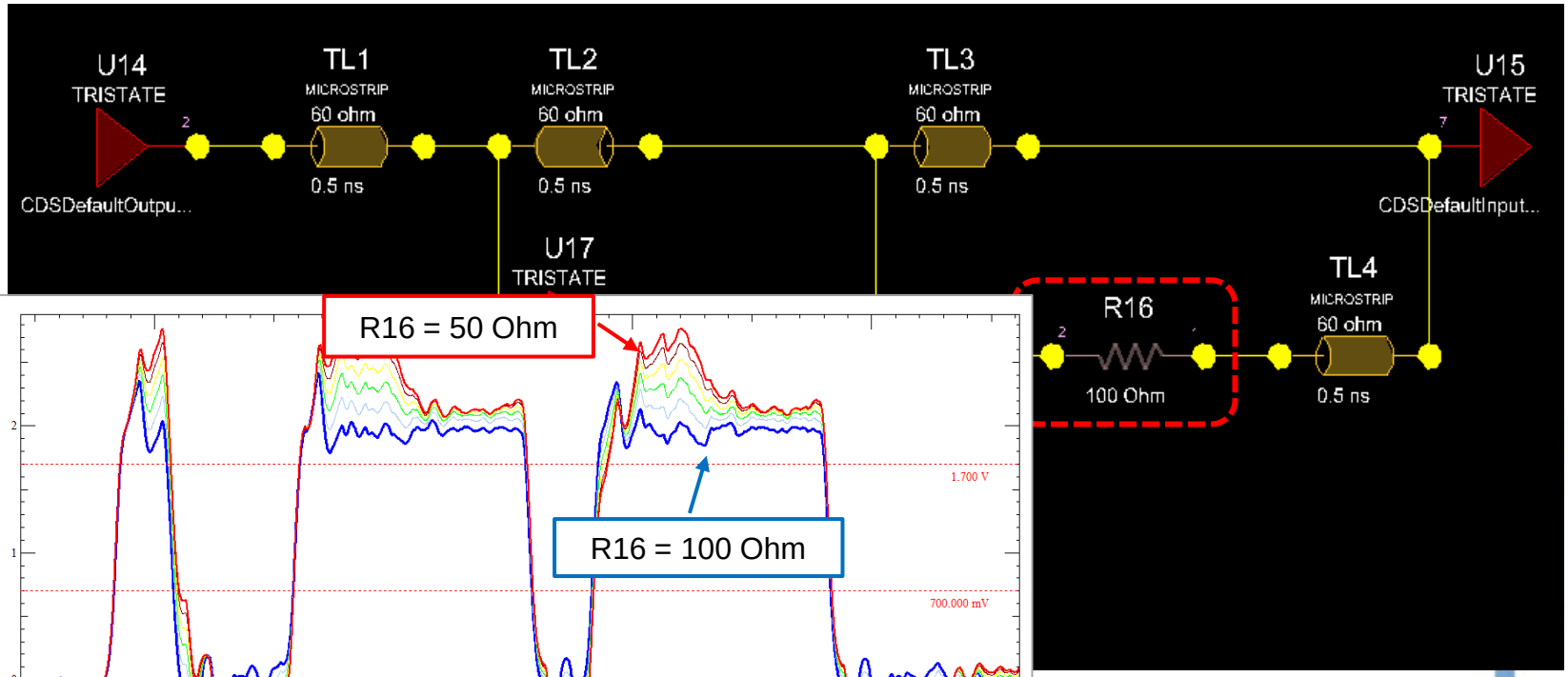

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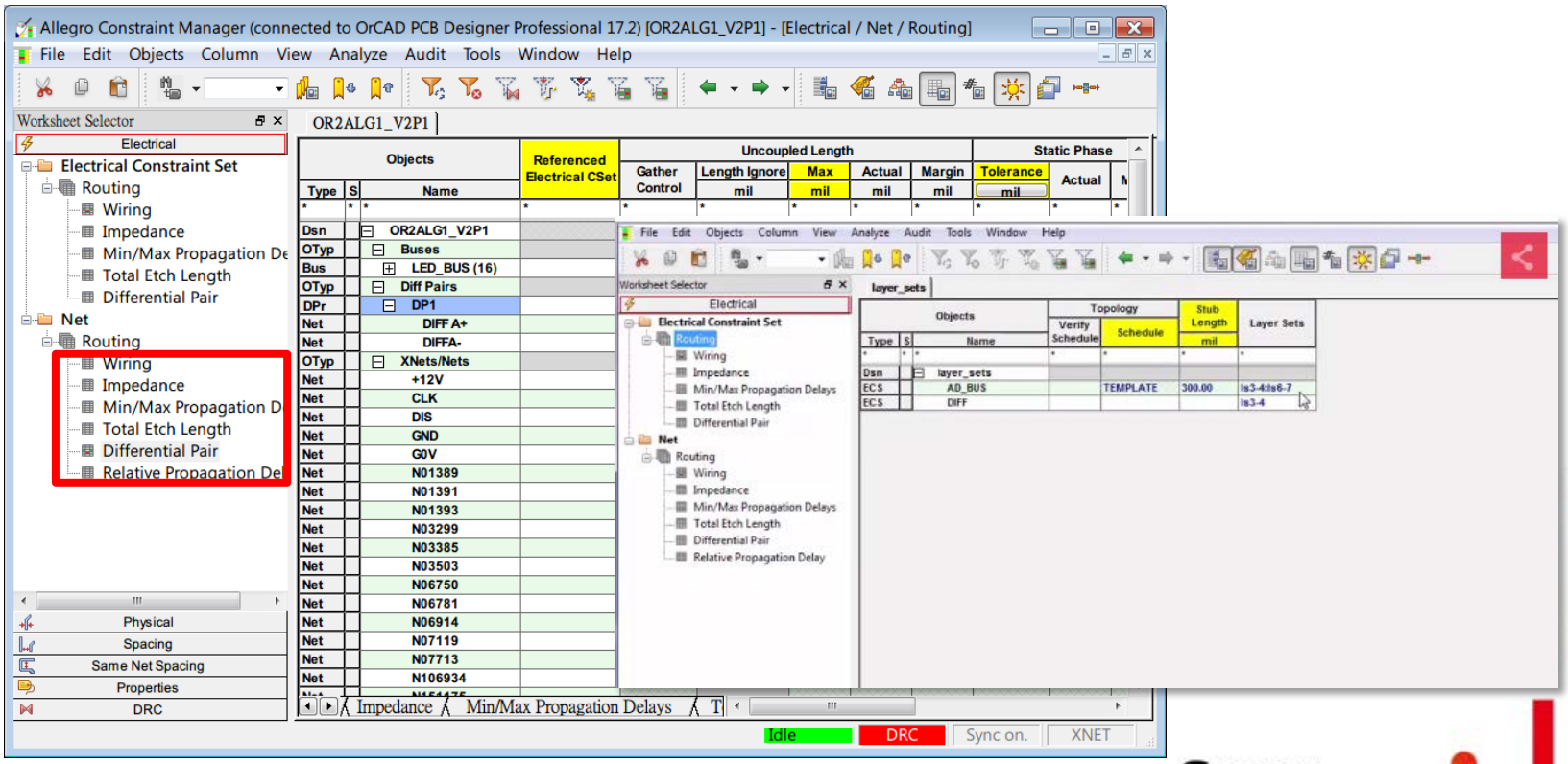
Constraint Setting

- Constraint Manager Setting
- Layer Set DRC and Routing
  - layer set functionality insures layer constrained nets are routed to wiring



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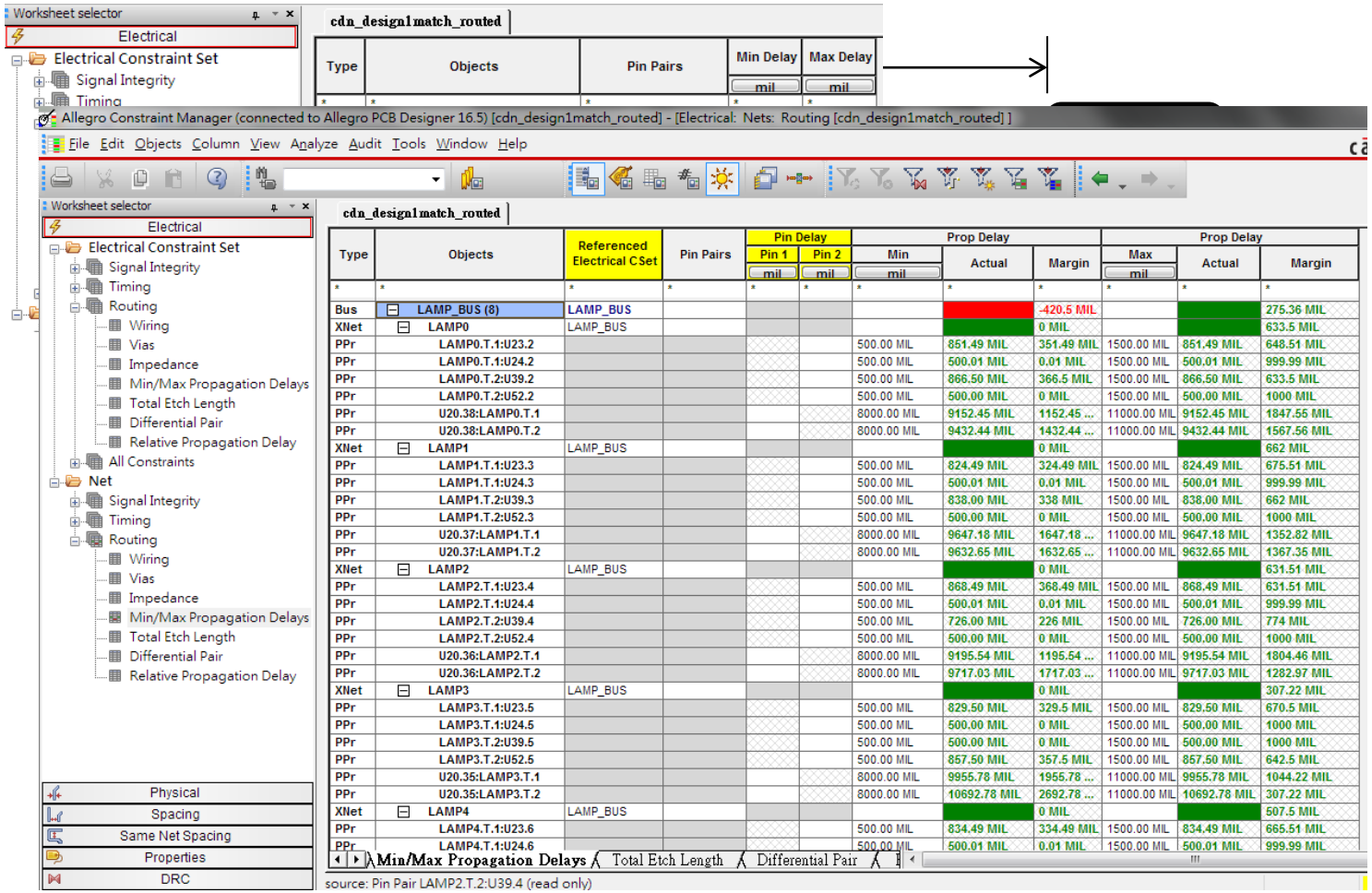
OrCAD PCB/CM - Min/Max Propagation Delay



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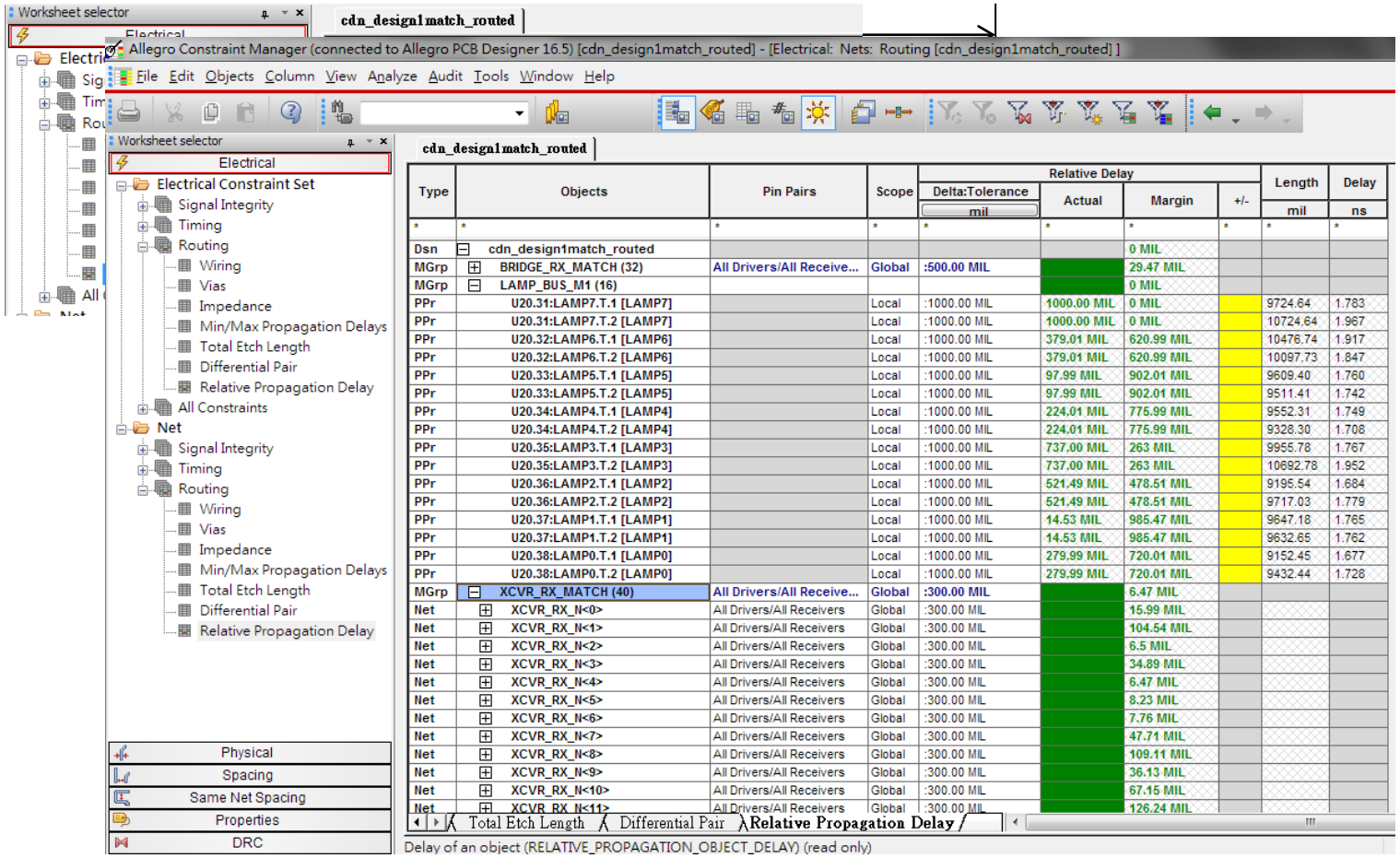
OrCAD PCB/CM - Relative Propagation Delay



Type	Objects	Pin Pairs	Scope	Relative Delay				Length	Delay
				Delta:Tolerance mil	Actual	Margin	+/-	mil	ns
*	*	*	*	*	*	*	*	*	*
Dsn	cdn_design1match_routed					0 MIL			
MGrp	BRIDGE_RX_MATCH (32)	All Drivers/All Receive...	Global	:500.00 MIL		29.47 MIL			
MGrp	LAMP_BUS_M1 (16)					0 MIL			
PPr	U20.31:LAMP7.T.1 [LAMP7]		Local	:1000.00 MIL	1000.00 MIL	0 MIL		9724.64	1.783
PPr	U20.31:LAMP7.T.2 [LAMP7]		Local	:1000.00 MIL	1000.00 MIL	0 MIL		10724.64	1.967
PPr	U20.32:LAMP6.T.1 [LAMP6]		Local	:1000.00 MIL	379.01 MIL	620.99 MIL		10476.74	1.917
PPr	U20.32:LAMP6.T.2 [LAMP6]		Local	:1000.00 MIL	379.01 MIL	620.99 MIL		10097.73	1.847
PPr	U20.33:LAMP5.T.1 [LAMP5]		Local	:1000.00 MIL	97.99 MIL	902.01 MIL		9609.40	1.760
PPr	U20.33:LAMP5.T.2 [LAMP5]		Local	:1000.00 MIL	97.99 MIL	902.01 MIL		9511.41	1.742
PPr	U20.34:LAMP4.T.1 [LAMP4]		Local	:1000.00 MIL	224.01 MIL	775.99 MIL		9552.31	1.749
PPr	U20.34:LAMP4.T.2 [LAMP4]		Local	:1000.00 MIL	224.01 MIL	775.99 MIL		9328.30	1.708
PPr	U20.35:LAMP3.T.1 [LAMP3]		Local	:1000.00 MIL	737.00 MIL	263 MIL		9955.78	1.767
PPr	U20.35:LAMP3.T.2 [LAMP3]		Local	:1000.00 MIL	737.00 MIL	263 MIL		10692.78	1.952
PPr	U20.36:LAMP2.T.1 [LAMP2]		Local	:1000.00 MIL	521.49 MIL	478.51 MIL		9195.54	1.684
PPr	U20.36:LAMP2.T.2 [LAMP2]		Local	:1000.00 MIL	521.49 MIL	478.51 MIL		9717.03	1.779
PPr	U20.37:LAMP1.T.1 [LAMP1]		Local	:1000.00 MIL	14.53 MIL	985.47 MIL		9647.18	1.765
PPr	U20.37:LAMP1.T.2 [LAMP1]		Local	:1000.00 MIL	14.53 MIL	985.47 MIL		9632.65	1.762
PPr	U20.38:LAMP0.T.1 [LAMP0]		Local	:1000.00 MIL	279.99 MIL	720.01 MIL		9152.45	1.677
PPr	U20.38:LAMP0.T.2 [LAMP0]		Local	:1000.00 MIL	279.99 MIL	720.01 MIL		9432.44	1.728
MGrp	XCVR_RX_MATCH (40)	All Drivers/All Receive...	Global	:300.00 MIL		6.47 MIL			
Net	XCVR_RX_N<0>	All Drivers/All Receivers	Global	:300.00 MIL		15.99 MIL			
Net	XCVR_RX_N<1>	All Drivers/All Receivers	Global	:300.00 MIL		104.54 MIL			
Net	XCVR_RX_N<2>	All Drivers/All Receivers	Global	:300.00 MIL		6.5 MIL			
Net	XCVR_RX_N<3>	All Drivers/All Receivers	Global	:300.00 MIL		34.89 MIL			
Net	XCVR_RX_N<4>	All Drivers/All Receivers	Global	:300.00 MIL		6.47 MIL			
Net	XCVR_RX_N<5>	All Drivers/All Receivers	Global	:300.00 MIL		8.23 MIL			
Net	XCVR_RX_N<6>	All Drivers/All Receivers	Global	:300.00 MIL		7.76 MIL			
Net	XCVR_RX_N<7>	All Drivers/All Receivers	Global	:300.00 MIL		47.71 MIL			
Net	XCVR_RX_N<8>	All Drivers/All Receivers	Global	:300.00 MIL		109.11 MIL			
Net	XCVR_RX_N<9>	All Drivers/All Receivers	Global	:300.00 MIL		36.13 MIL			
Net	XCVR_RX_N<10>	All Drivers/All Receivers	Global	:300.00 MIL		67.15 MIL			
Net	XCVR_RX_N<11>	All Drivers/All Receivers	Global	:300.00 MIL		126.24 MIL			

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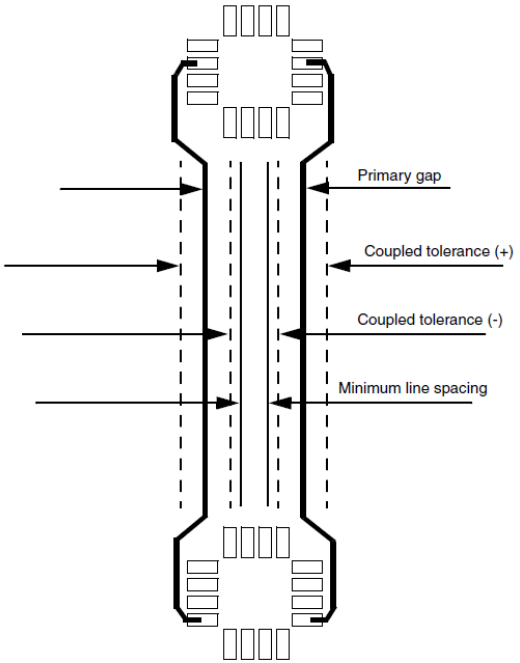
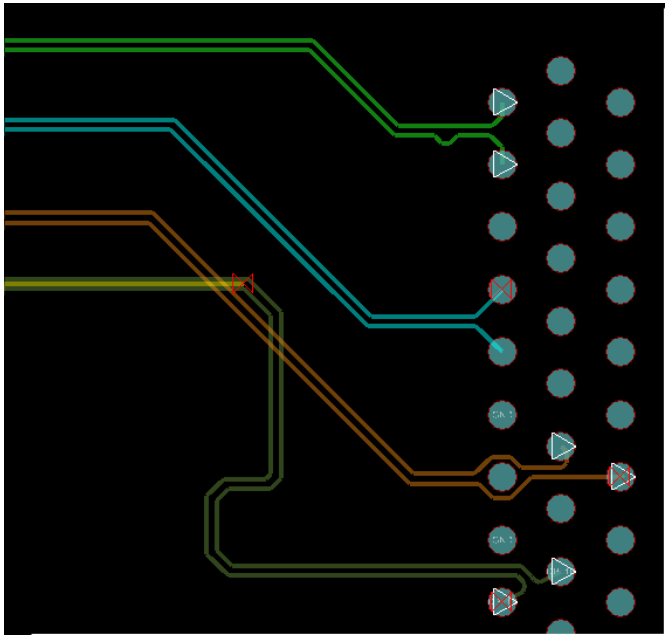
OrCAD PCB/CM - Differential Pair

Uncoupled Length					Static Phase			Min Line Spacing	Coupling Parameters					
Gather Control	Length Ignored	Max	Actual	Margin	Tolerance	Actual	Margin		Prim. Gap	Prim. Width	Neck Gap	Neck Width	(+)Tol.	(-)Tol.
	mil	mil	mil		mil			mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
							-60.71	0.00	0.00	5.00	0.00	0.00	0.00	0.00
Ignore		300.00			5 mil		-60.71	0.00	0.00	5.00	0.00	0.00	0.00	0.00
Ignore		300.00			5 mil		-36.98	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-5.220	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-40.32	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil			3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-22.16	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-12.36	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-60.71	3.80	6.00	6.00	3.90	3.40	0.10	0.10
Ignore		300.00			5 mil		-12.51	3.80	6.00	6.00	3.90	3.40	0.10	0.10





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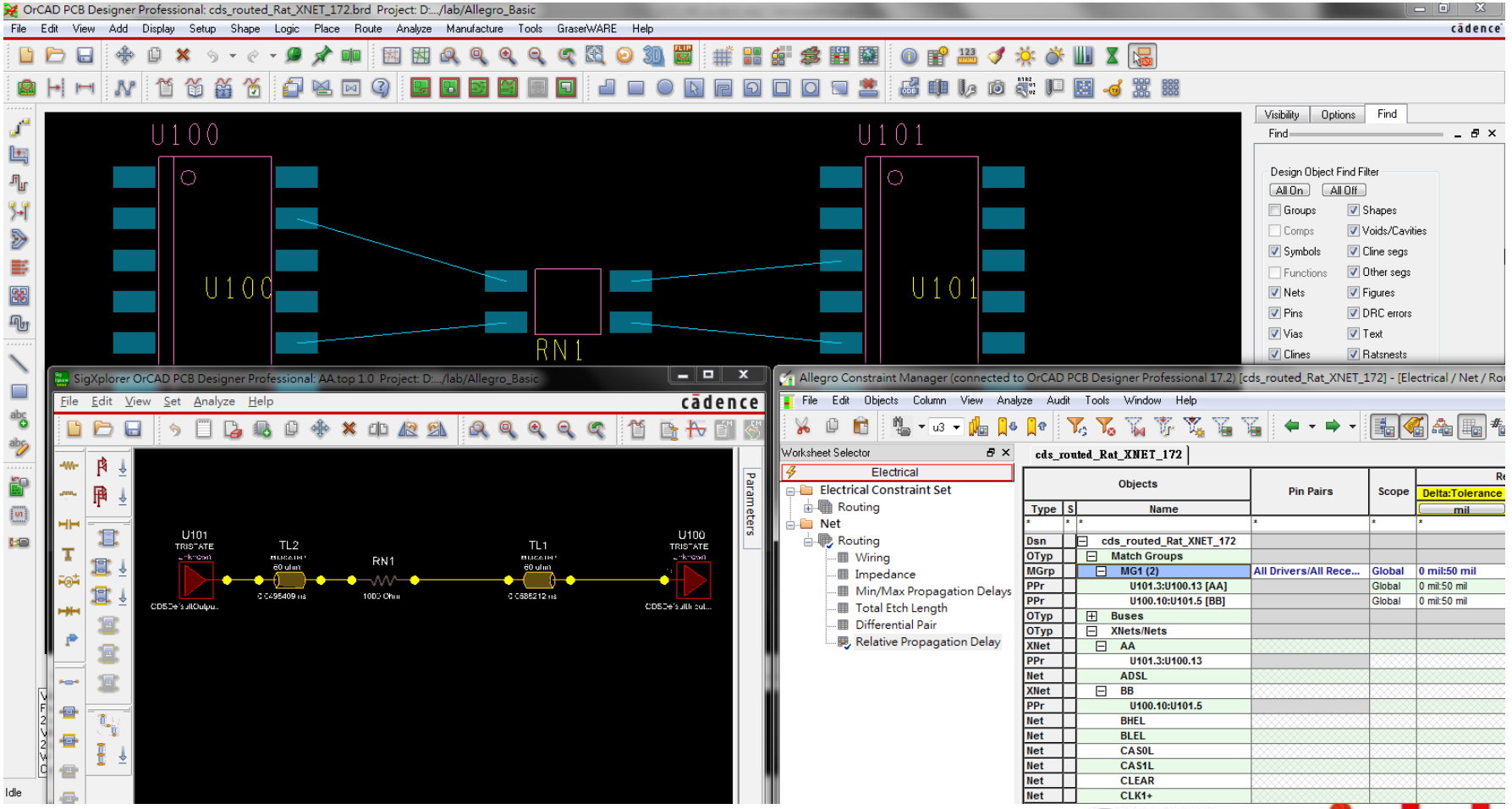
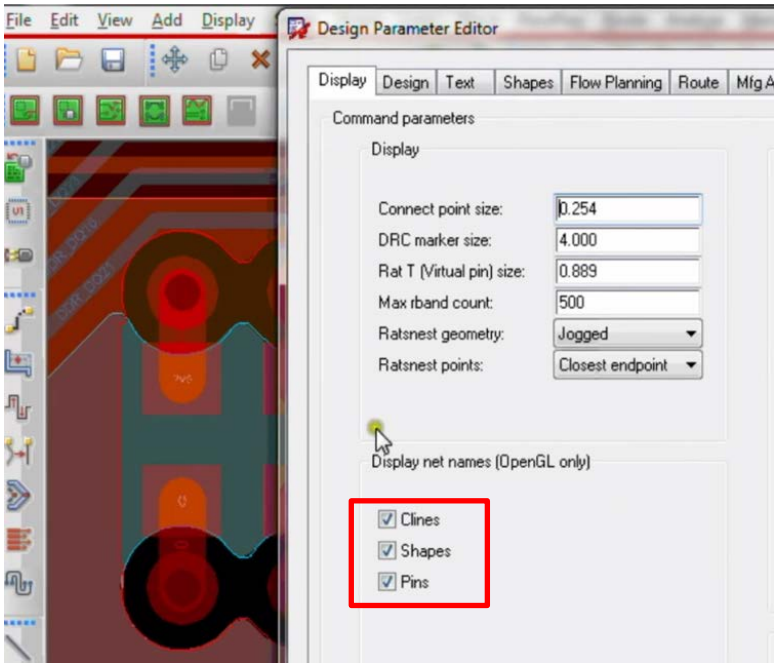
Support X-Net

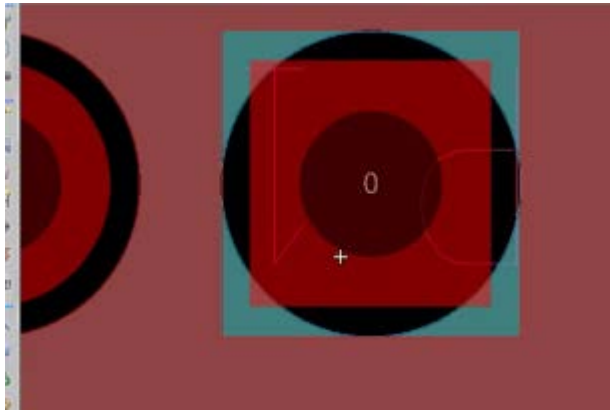
- eXtend Net

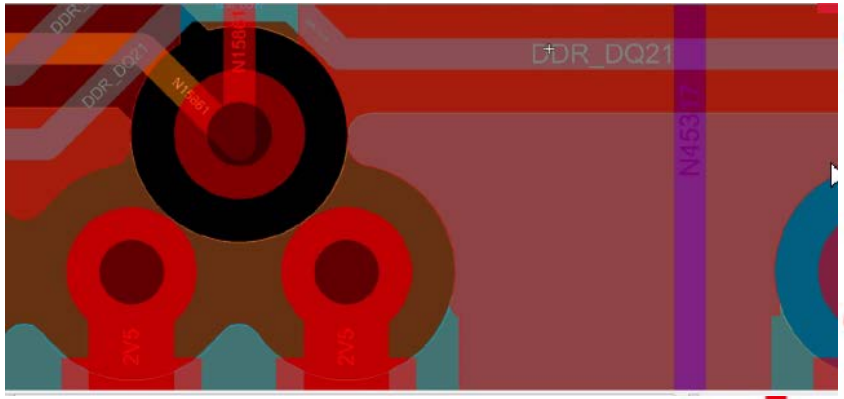


Embedded Net Names

- Set net name function to display so that the net names are shown.







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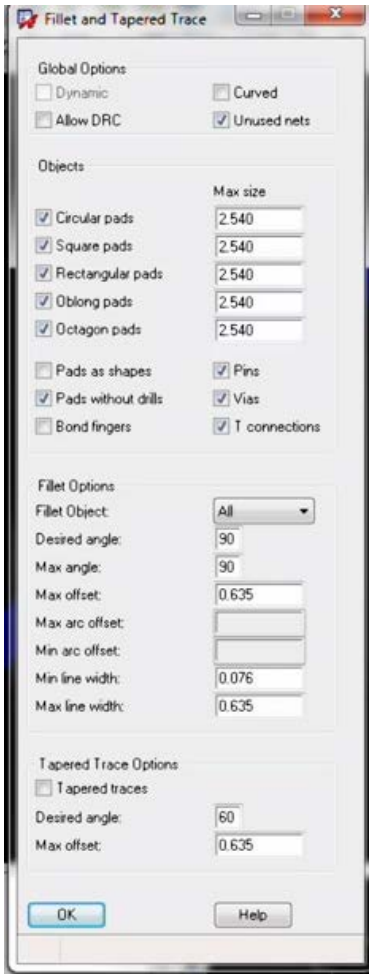
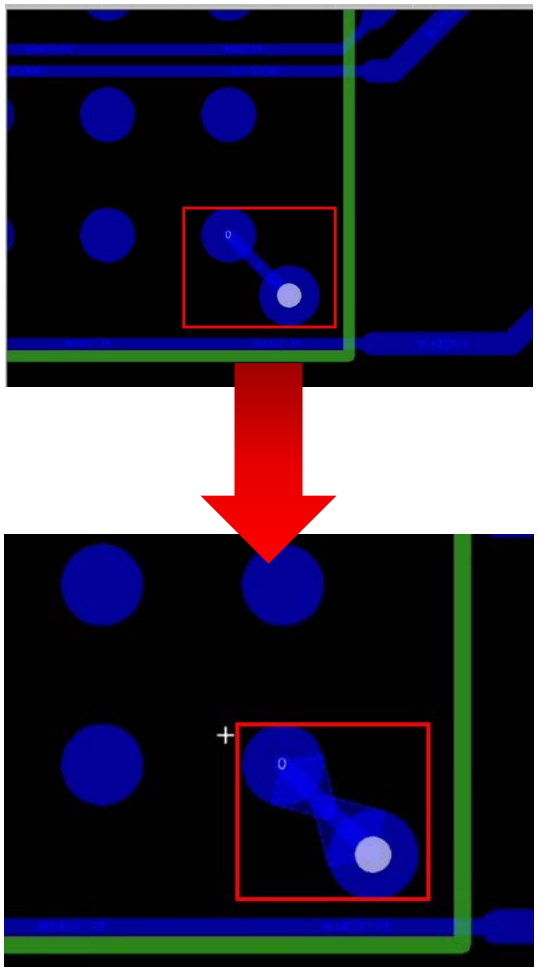
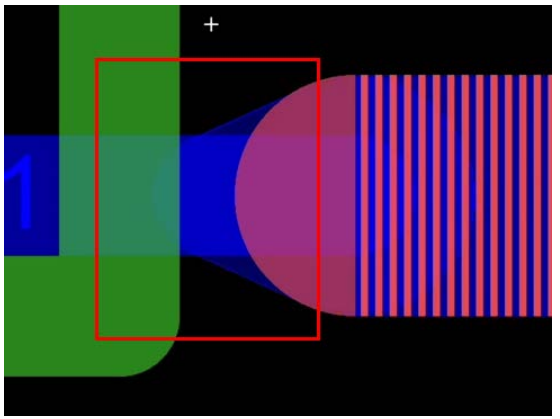
Fillet and Tapered Traces

- Use the Fillet Tapered Traces function

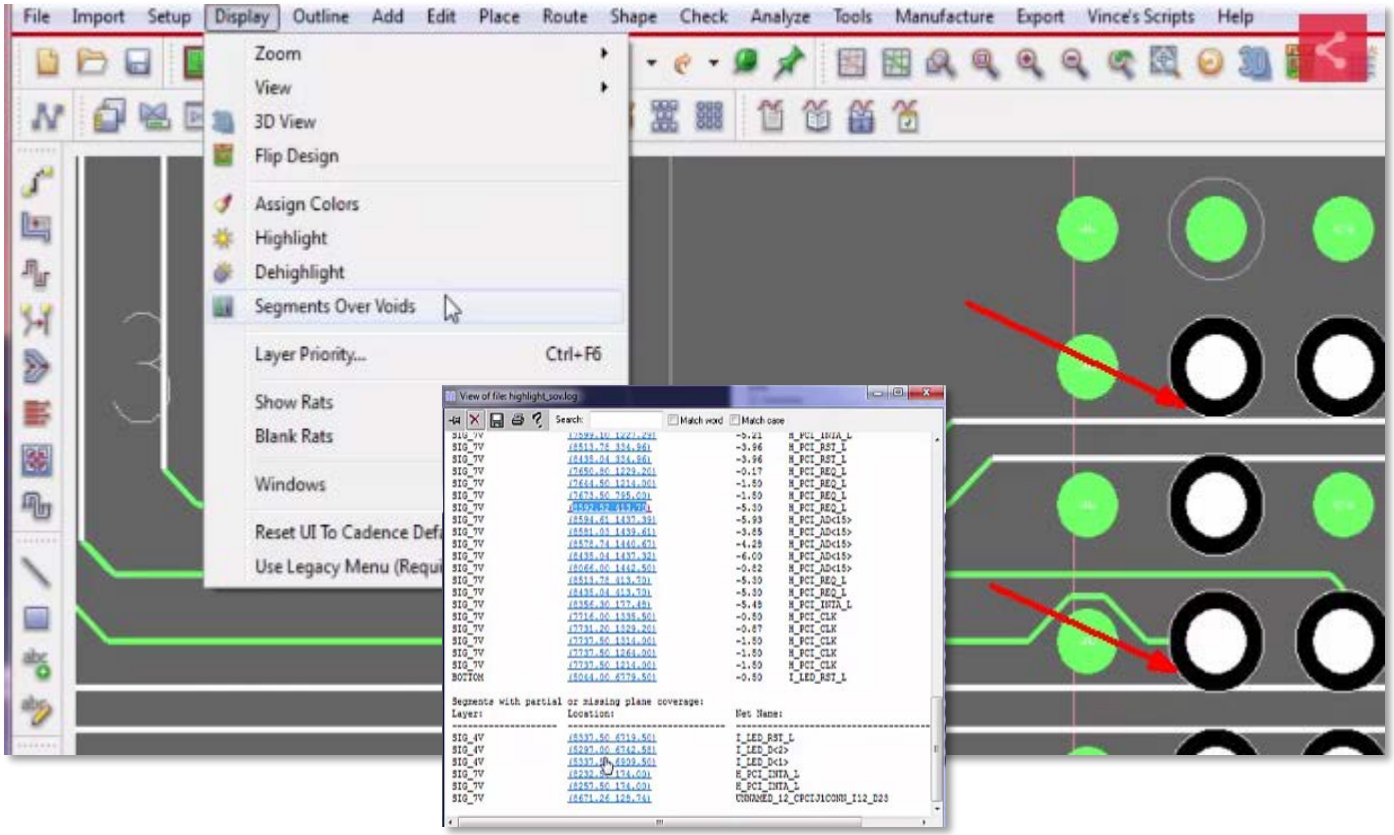






Segment Over Voids

- *Segment Over Voids* detects cline segments crossing adjacent plane layer voids.



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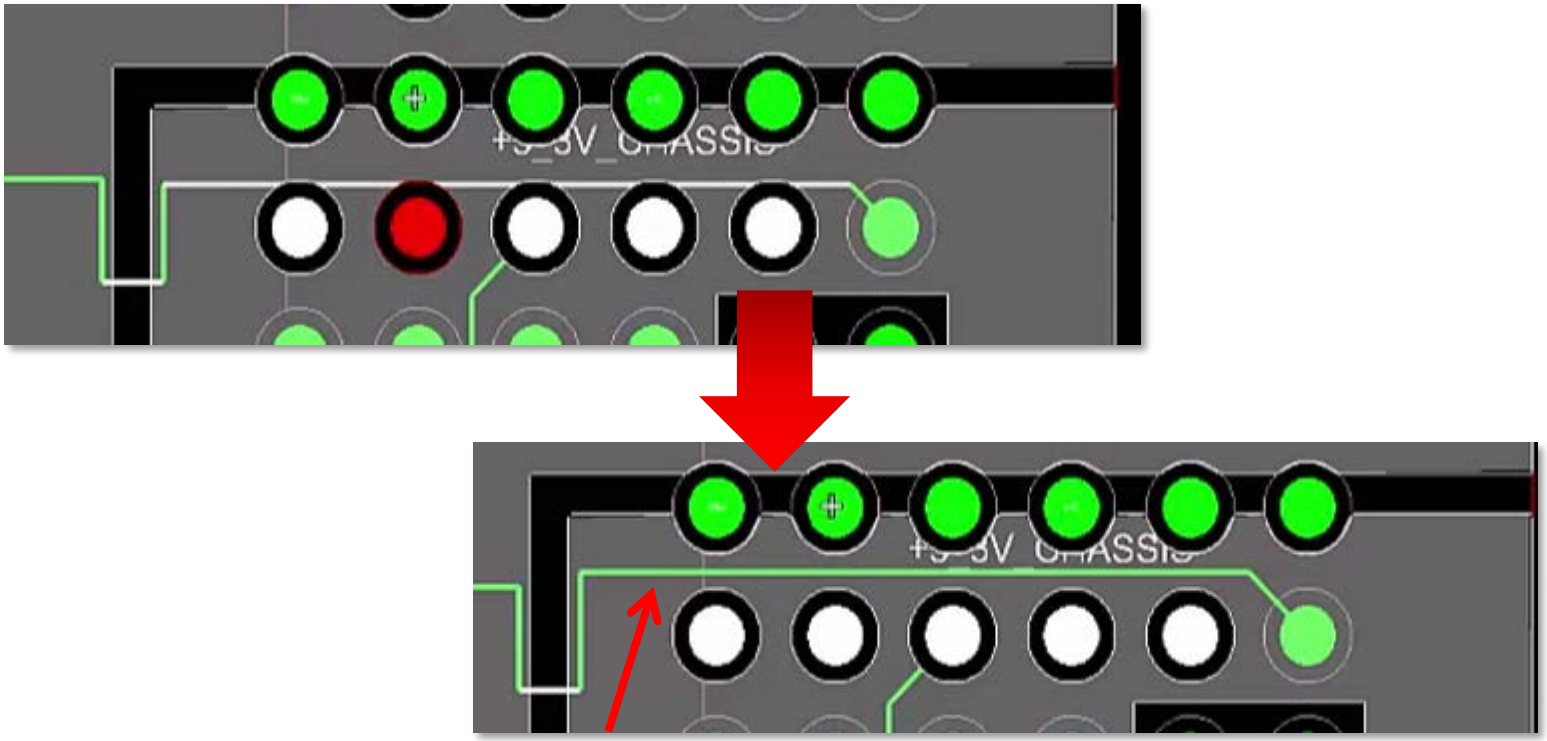
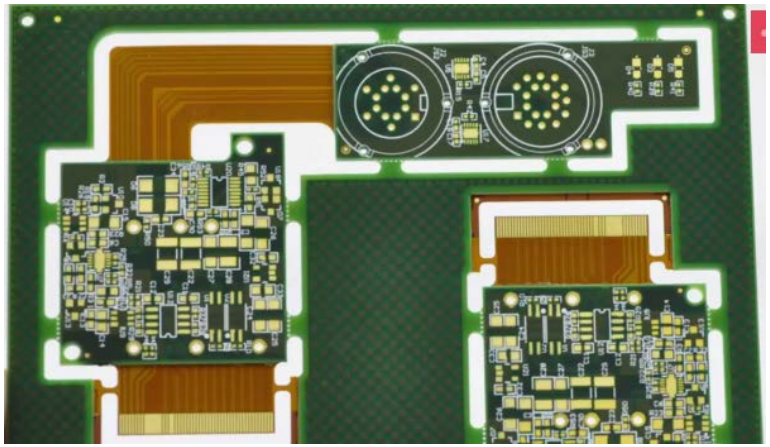
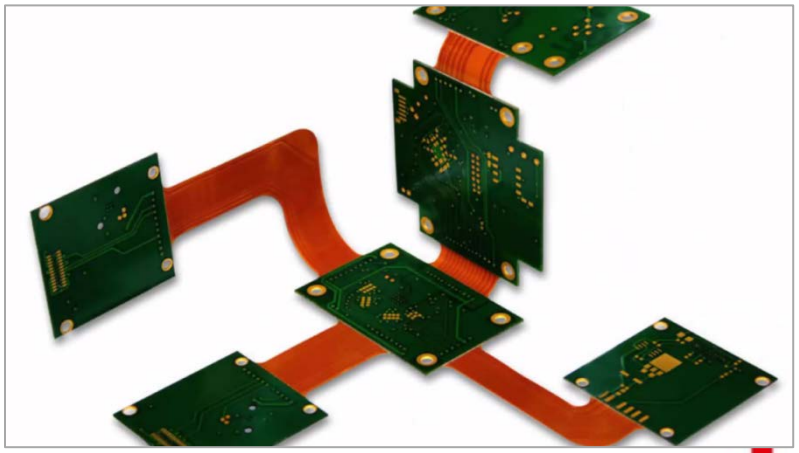


Flex and Rigid Flex Technologies

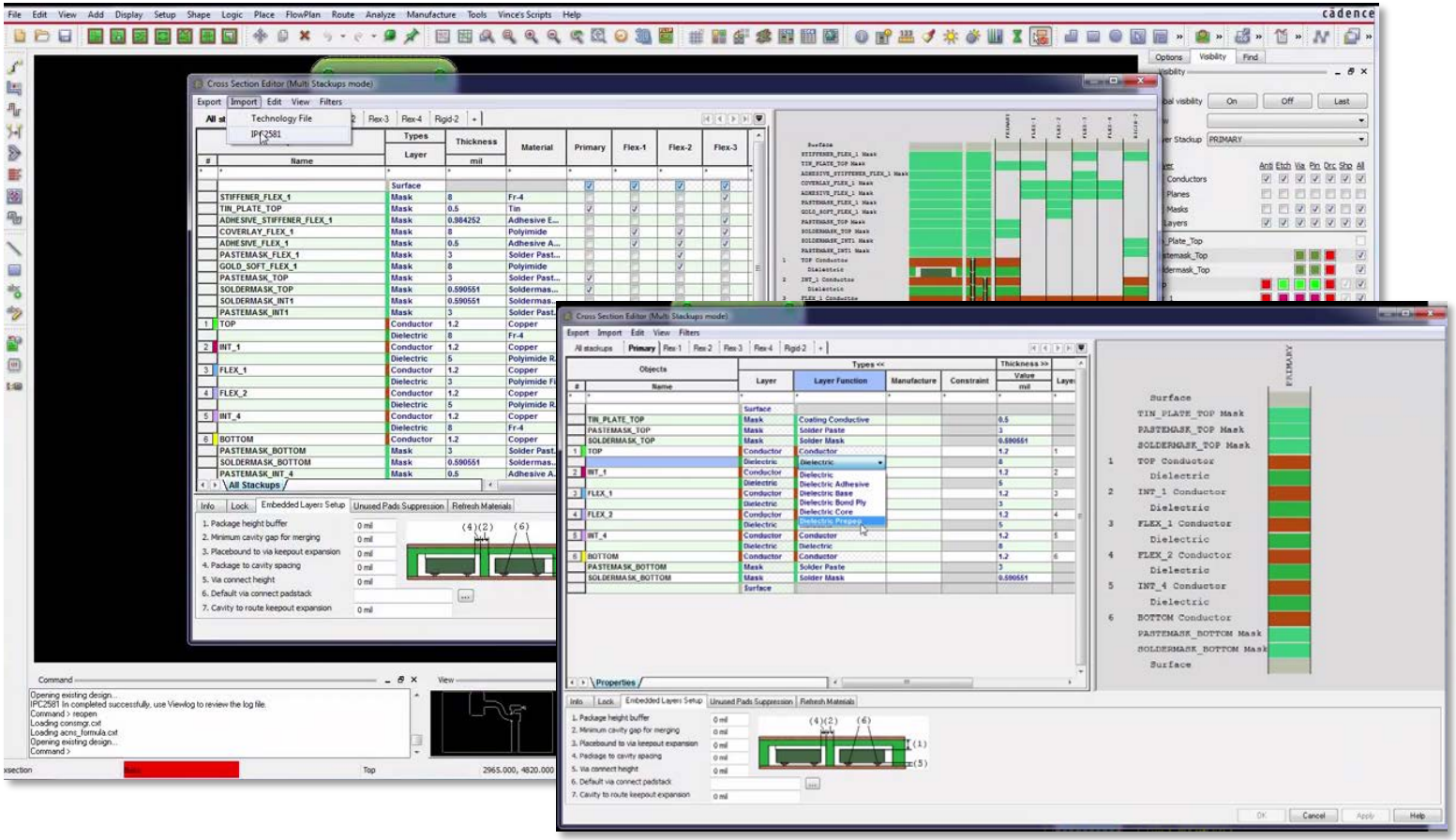
- To enable a faster and more efficient flex and rigid-flex design, capabilities for flex and rigid flex design to minimize design iterations. Key flex and rigid flex features include :
  - Stack-up by zone for flex and rigid-flex designs
  - Inter-layer checks for rigid-flex designs
  - Contour and arc-aware routing





Flex and Rigid Flex Technologies

- Layer Setting



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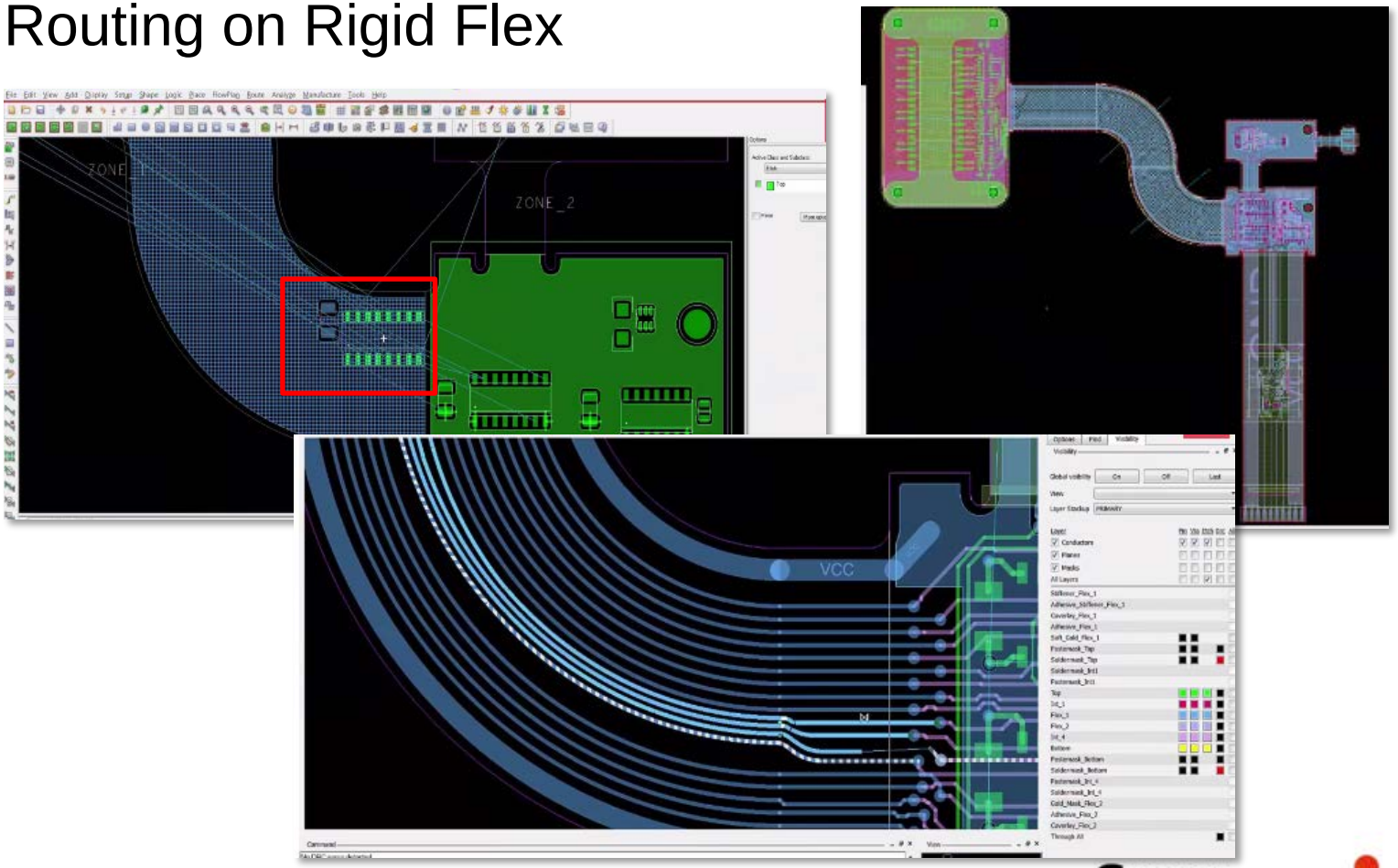
Flex and Rigid Flex Technologies

- Component place on Rigid Flex
- Routing on Rigid Flex



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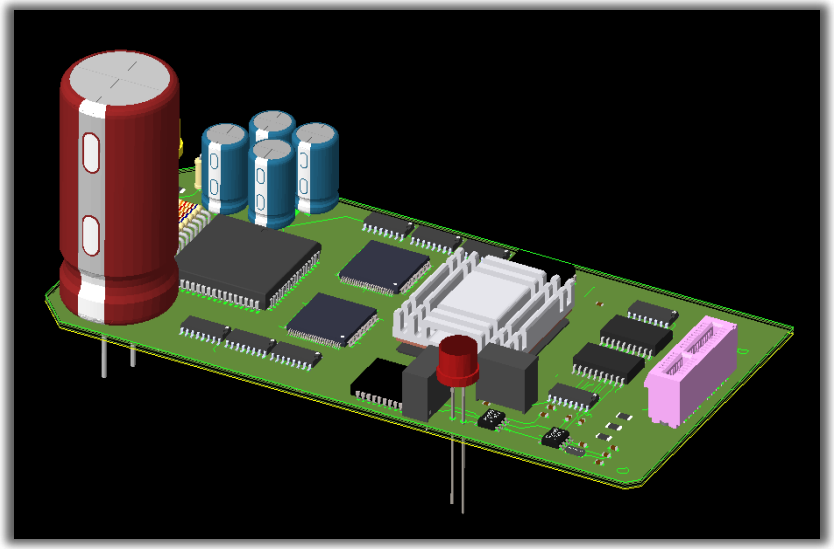
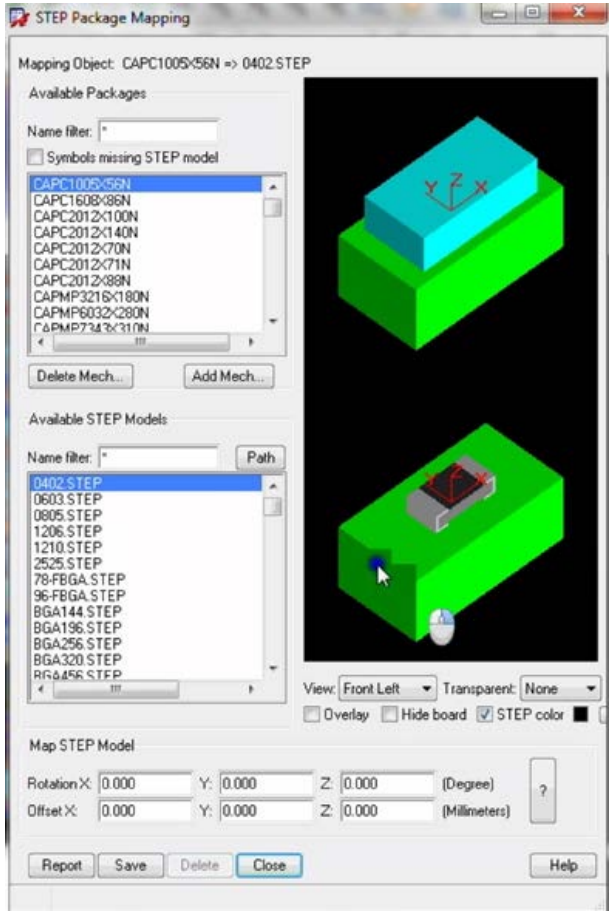
STEP Support - Mapping 3D Models

- Explore the ability to map and link a 3D STEP model to your components.





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OrCAD® Sigrity™ ERC / SRC Verification

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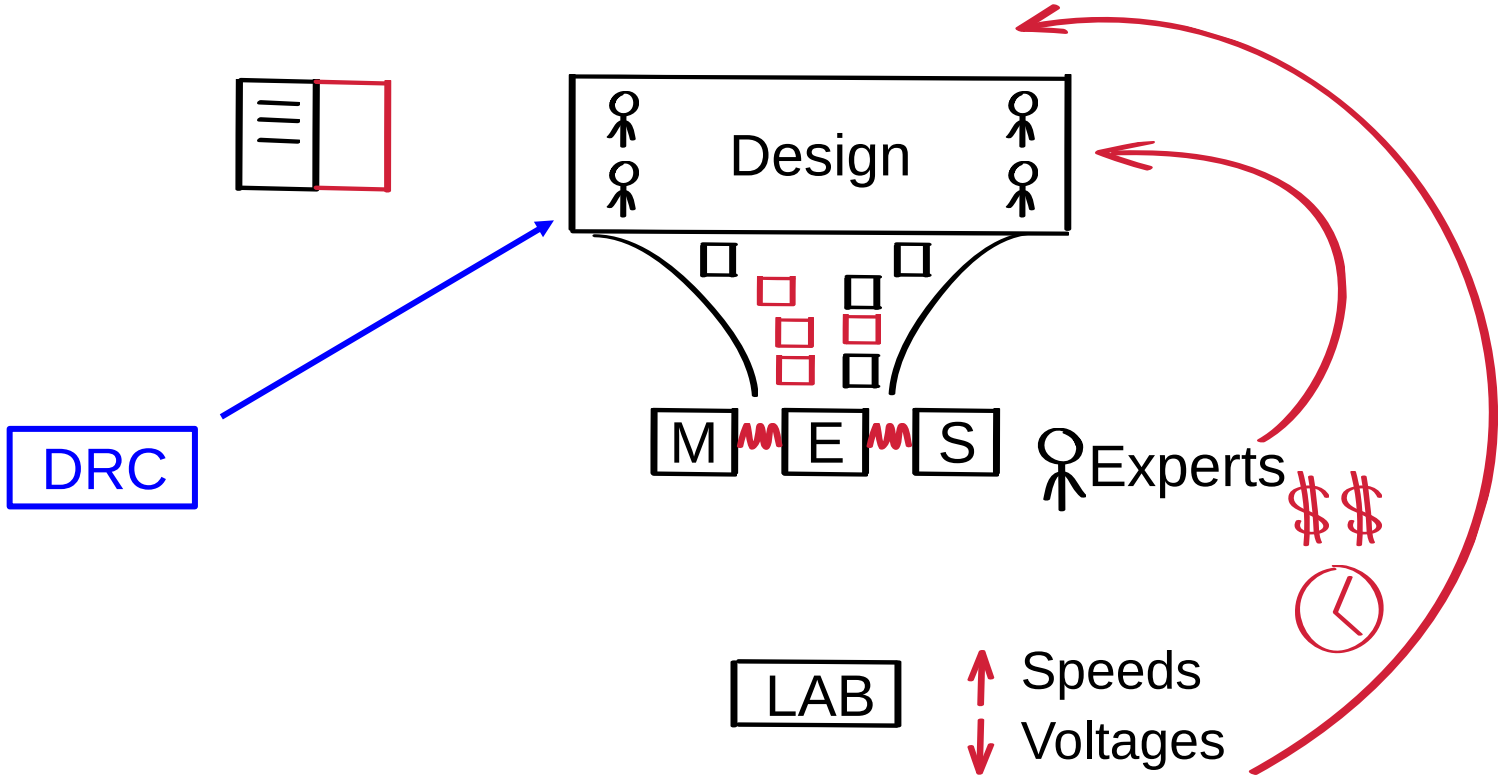
PCB Design Flow



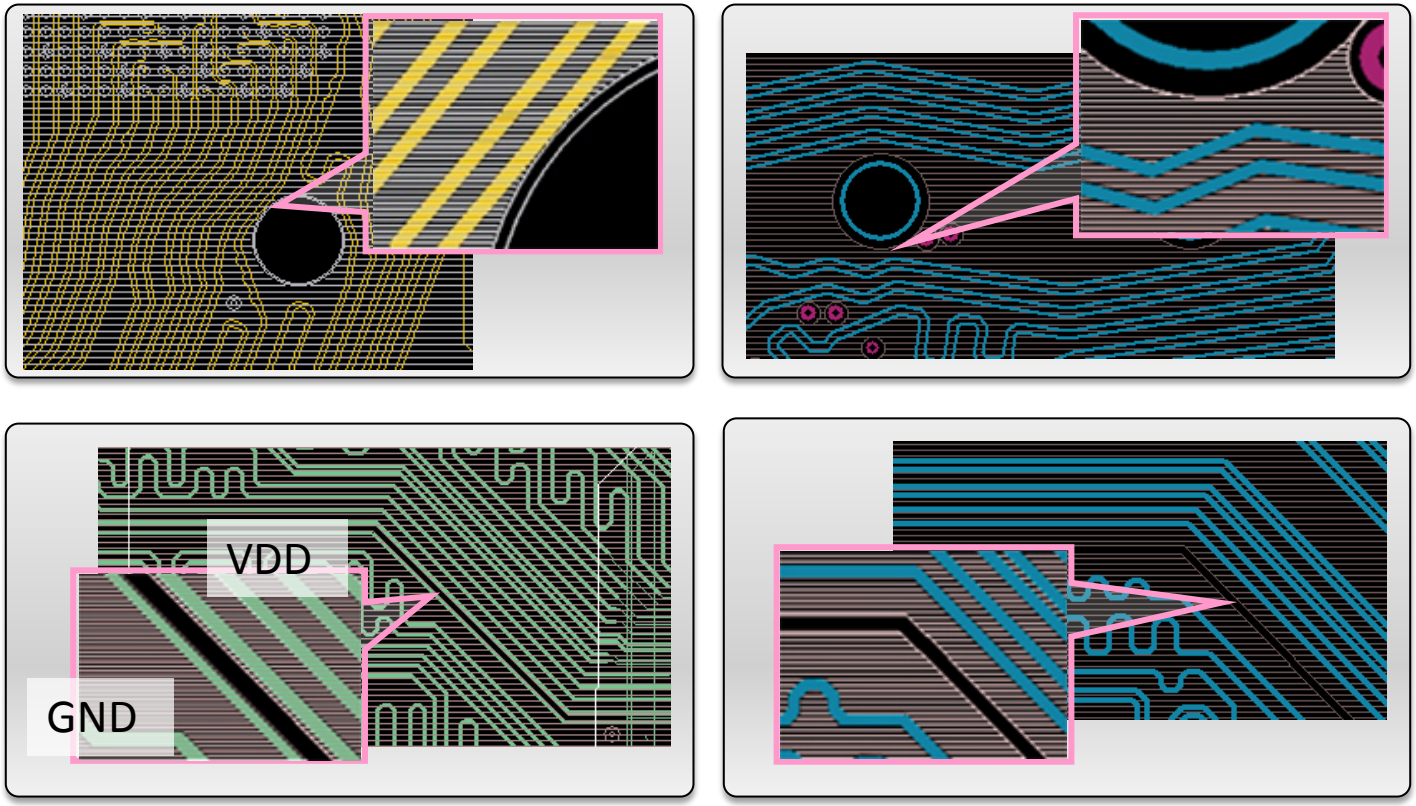
Signal and Power Chaos

Product Design Requirements

- Low Cost
- High Performance
- Shorter Design Phases
- First-Time Design Success!

Spacing Constraint Set

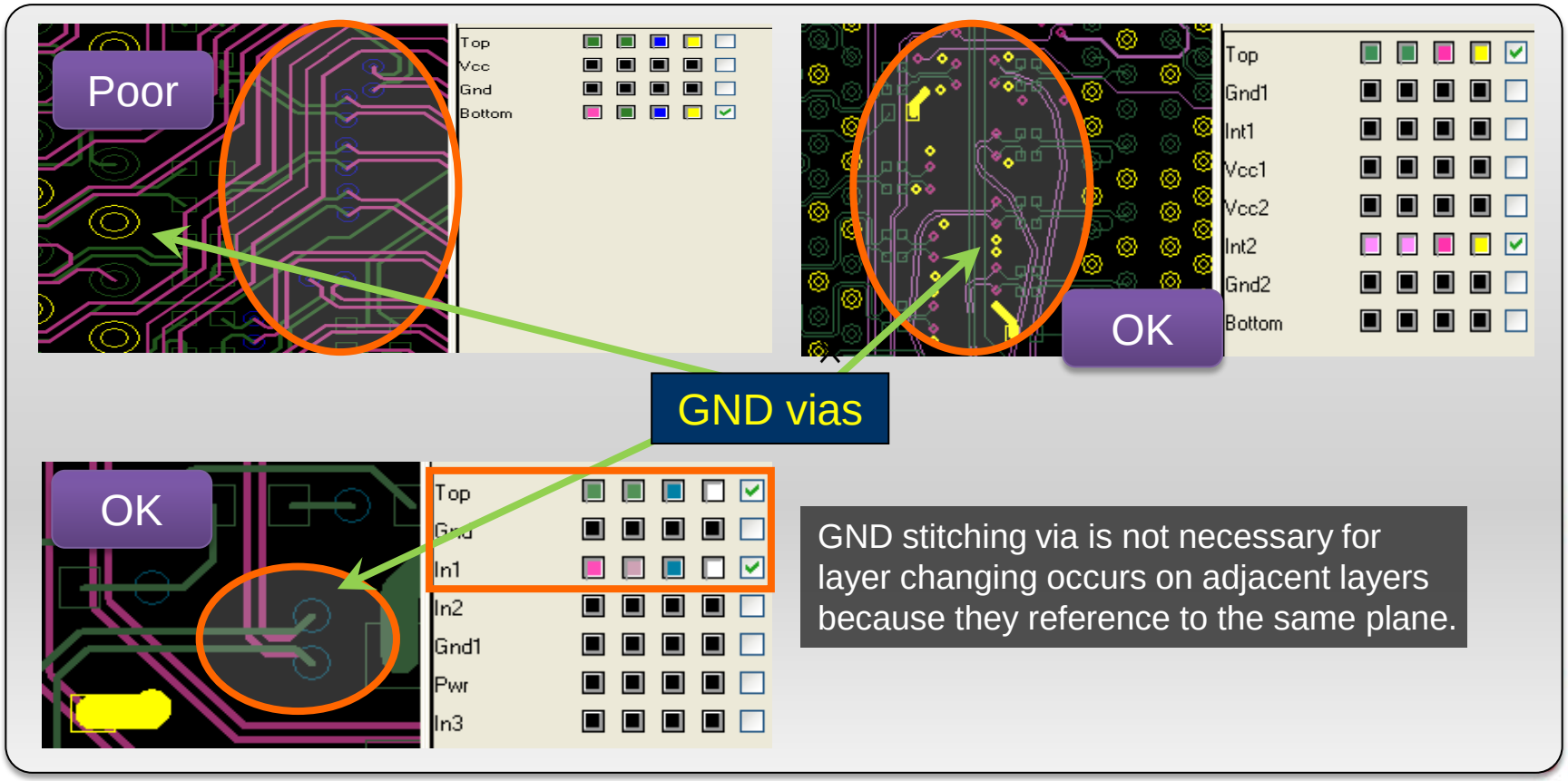
Reference Plane Spacing Clearance



- EMI
- Impedance mismatch

GND Stitching Vias

Return current path



- EMI
- Signal degradation

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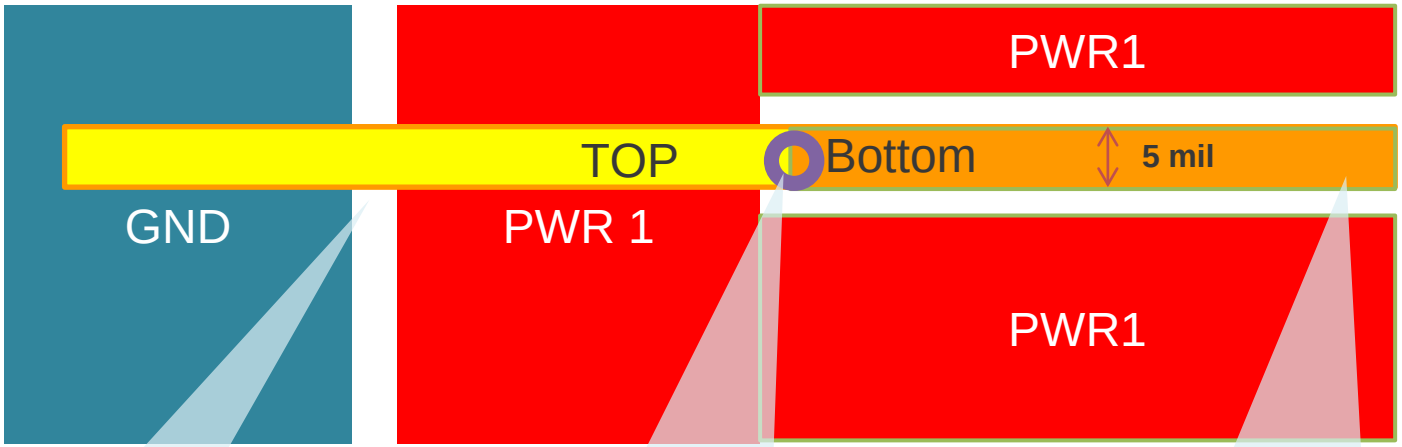
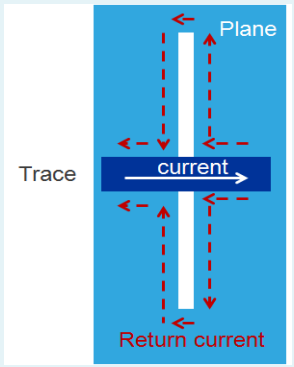
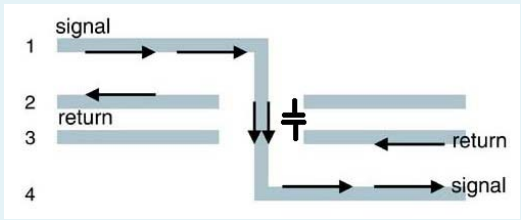
About SI – Impedance and Xtalk

- After pre-simulation, you set the trace width to be 5 mil in the constraint system to achieve the impedance you want. Of course, the following picture will show **no DRC** violation. **But if this is a 2-layers design and…**

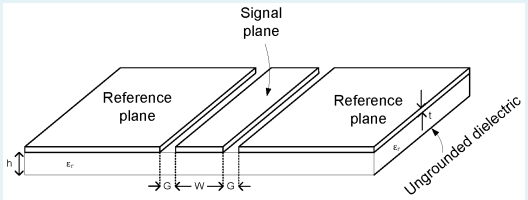




1. Reference change
2. Cross plane split



1. Layer Transistion



1. Coplarar reference

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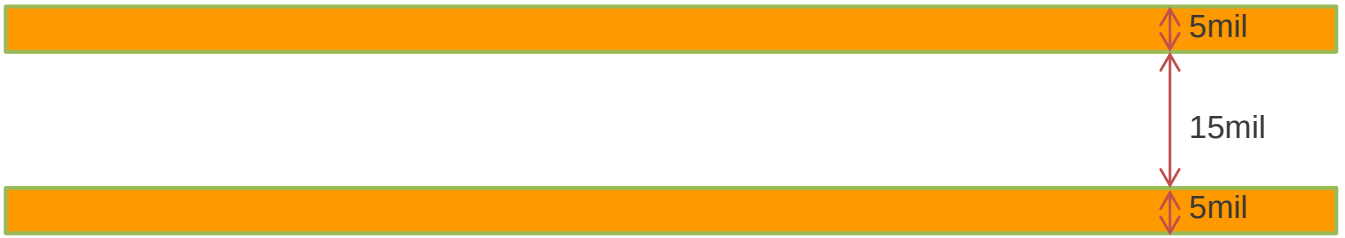
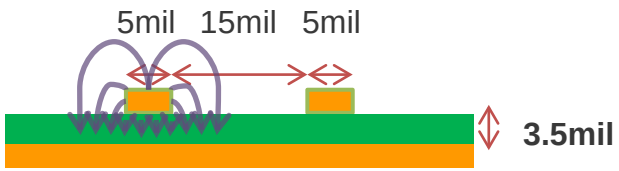
About SI – Impedance and Xtalk

- Talking about crosstalk, you probably follow the 3W rule – set the spacing between adjacent traces to 3 times the width of the trace as the following:



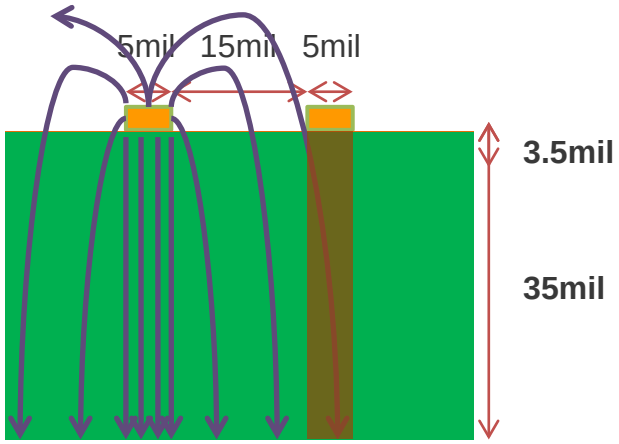
- The 3W rule may works well for the following structure:



No DRC violation ➡ No Xtalk issue

About SI – Impedance and Xtalk

- But if the stack-up looks like the following, will 3W rule still works well?



No DRC violation ➡ No Xtalk issue ?

Now, you're not satisfied with simply spacing constraint or the related **DRC** violation warning. You feel you probably need **simulation** or other way to tell you :

How Much the Coupling is

The gap between DRC and SI performance

- The gap between layout designers and SI engineers is huge
  - Have different design expertise
  - Using different tools
  - Measured by different units

Gap

Layout/Board designer

Layout tools

Geometry domain (mil/mm)

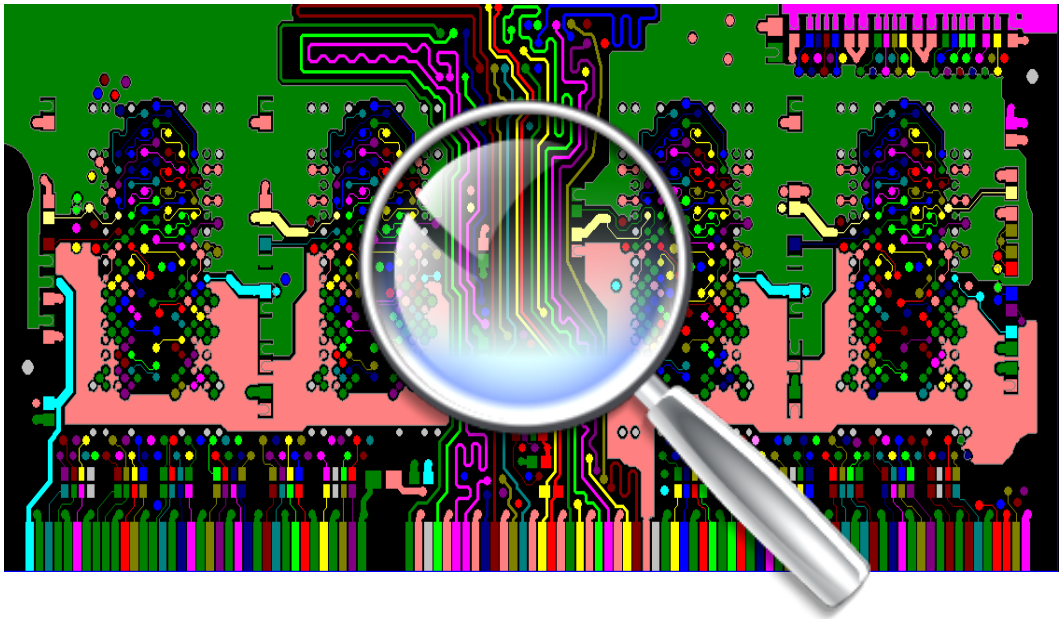
SI engineer

Simulation tools

Electrical domain (mv, ps)

Why Electrical Rule Check

- ERCs are better than DRCs for ‘signal quality’ validation
  - Goes beyond **MINIMUM-ACCEPTANCE, GEOMETRY-BASED** constraint validation
- PCB designers identify and address first-order signal quality issues

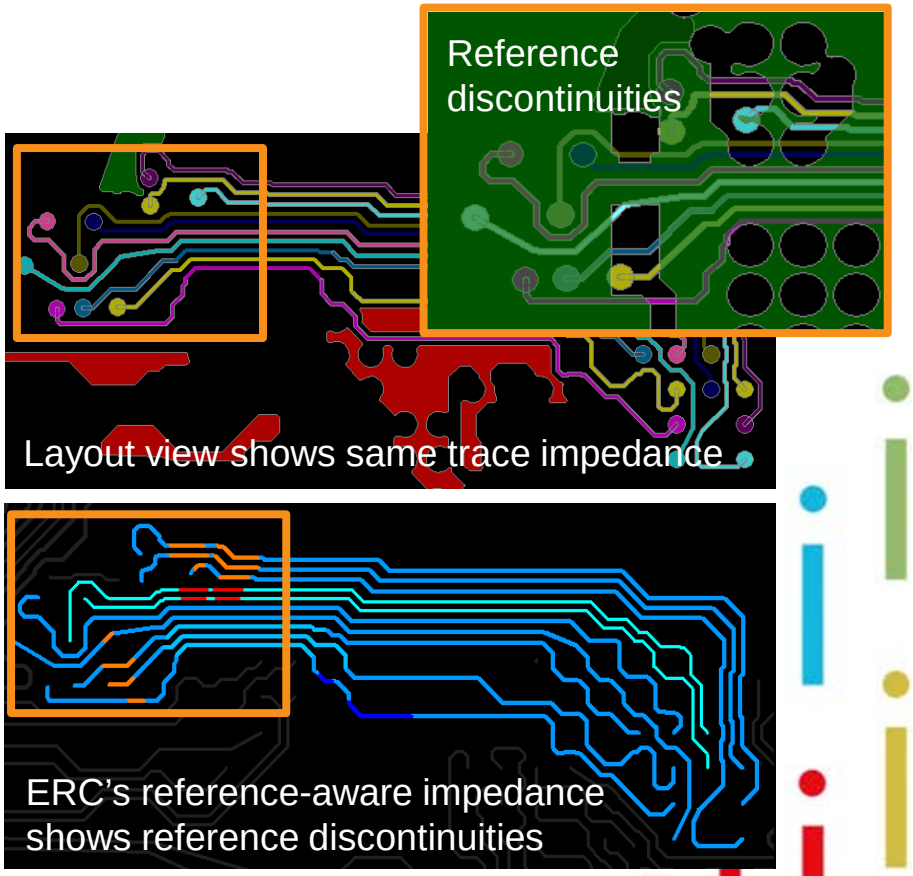


What is Sigrity ERC?

- OrCAD® Sigrity™ ERC is individual, segment-level view in geometry domain for PCB's SI performance with
  - Trace reference
  - Trace reference-aware impedance
  - Trace reference-aware coupling
  - Differential pair routing phase
  - # of vias and via locations, ….
  - Practical for board level check

    (setup, simulation, report)

    <2min 10-20min auto



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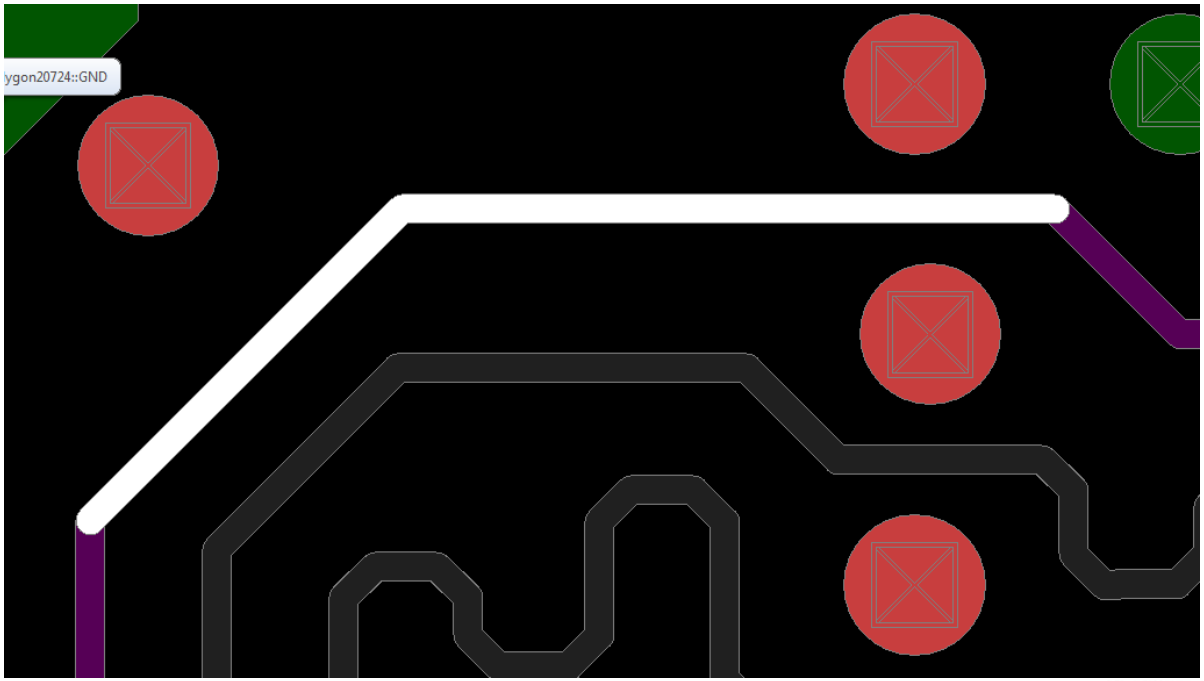
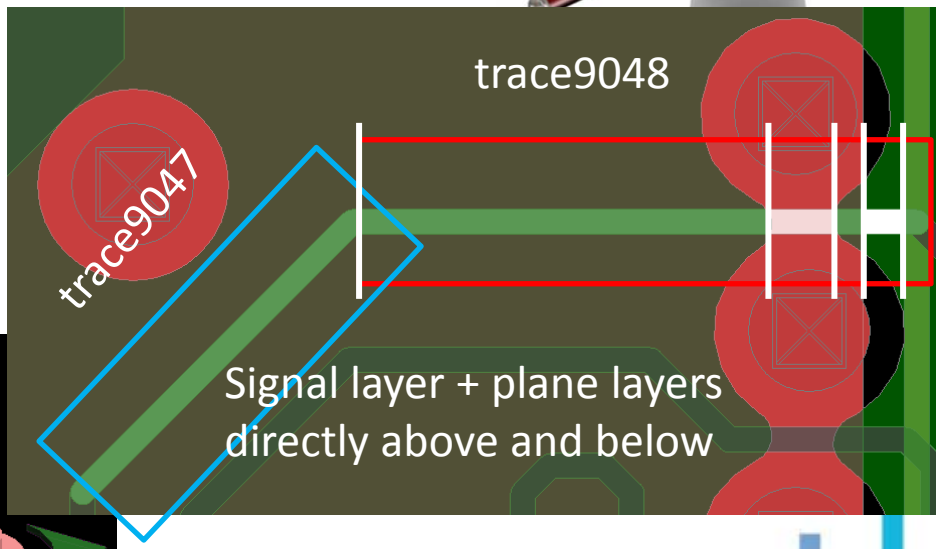
What is Sigrity ERC?

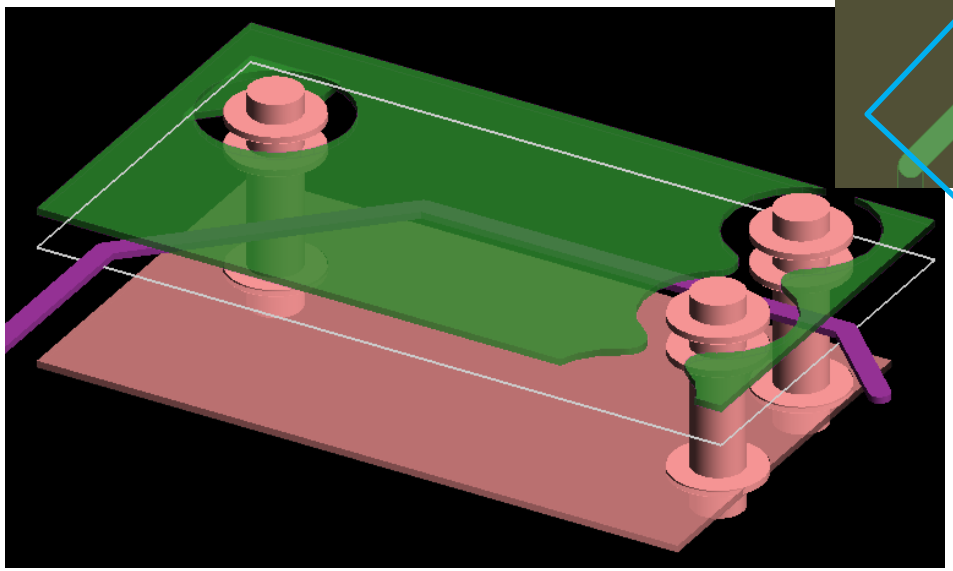
- DRC – Simplified impedance view
  Two trace segments example
  - 2 trace segments, same trace width, same impedance
  - You can also see trace segment length



What is Sigrity ERC?

- If you look close enough…
  Two trace segments example
  - **Trace9047:**
    one uniform impedance section
  - **Trace9048:**
    4 impedance sections





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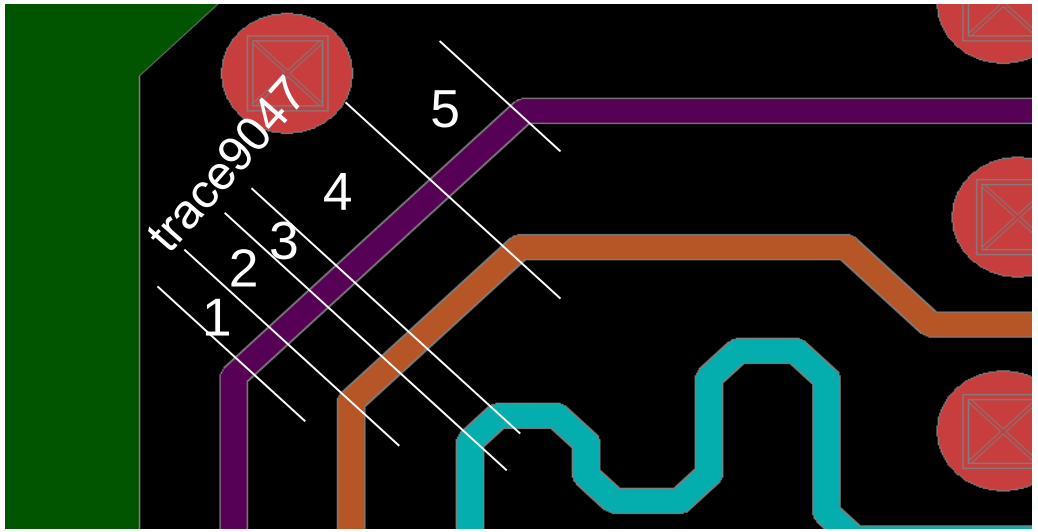
What is Sigrity ERC?

- Trace coupling
  - Trace9047 is one uniform impedance section
  - Trace9047 broken into 5 sections based on trace coupling
    - two no coupling sections (1 & 5)
    - two 2-line coupling sections (2 & 4)
    - one 3-line coupling section (3)

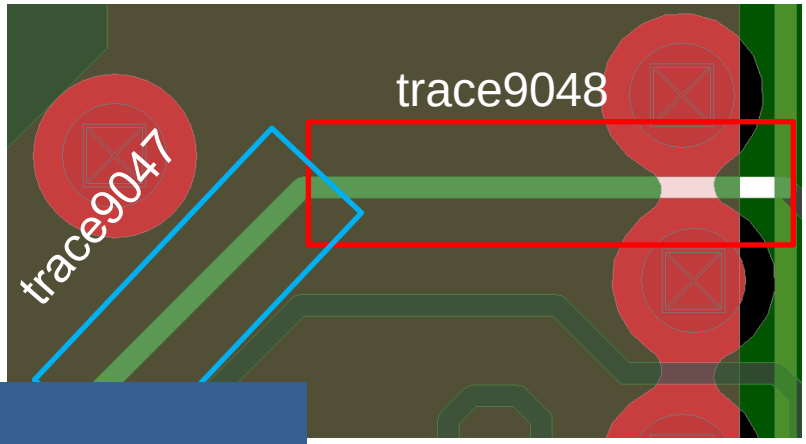
ERC results

Trace Name	Aggressor Trace Names	Coupling Coefficient (%)		Length (%)
Trace9047::DQ0	-	-	← 1	1.82
Trace9047::DQ0	Trace9024::DQ1	5.3	← 2	1.46
Trace9047::DQ0	Trace9024_Auto_190::DQ1	5.3	←3	1.16
	Trace8280::DQ4	0.6		
Trace9047::DQ0	Trace9024_Auto_191::DQ1	5.3	← 4	4.10
Trace9047::DQ0	-	-	← 5	3.04



What is Sigrity ERC?

- Trace upper / lower layer reference
  - Based on upper / lower layer references
    - Trace9047 → one section
    - Trace9048 → 5 sections



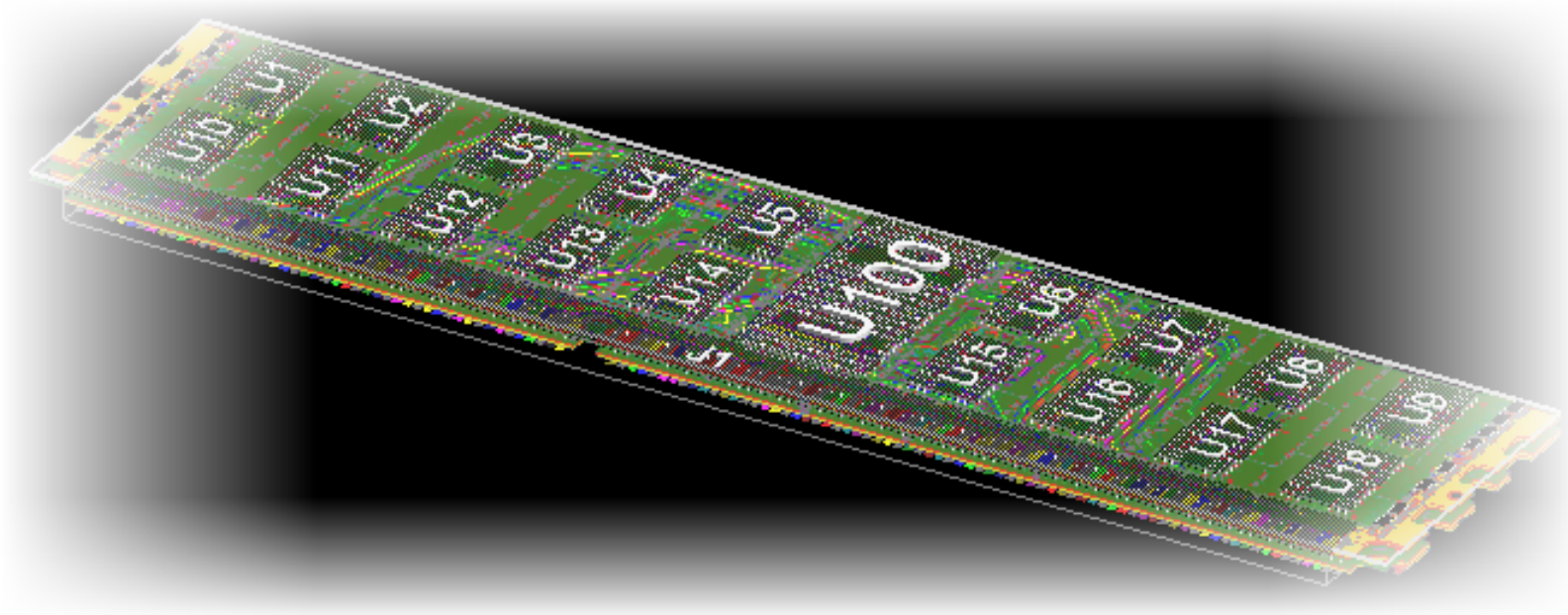
ERC results

Trace Name	Length (%)	Upper-lyr ref net name	Lower-lyr ref net name
Trace9047::DQ0	**11.58**	GND	**VDD**
Trace9048::DQ0	**12.74**	GND	**VDD**
Trace9048::DQ0	**1.78**	VDD	**VDD**
Trace9048::DQ0	**0.11**	-	**VDD**
Trace9048::DQ0	**0.89**	GND	**VDD**
Trace9048::DQ0	**1.66**	GND	**GND**

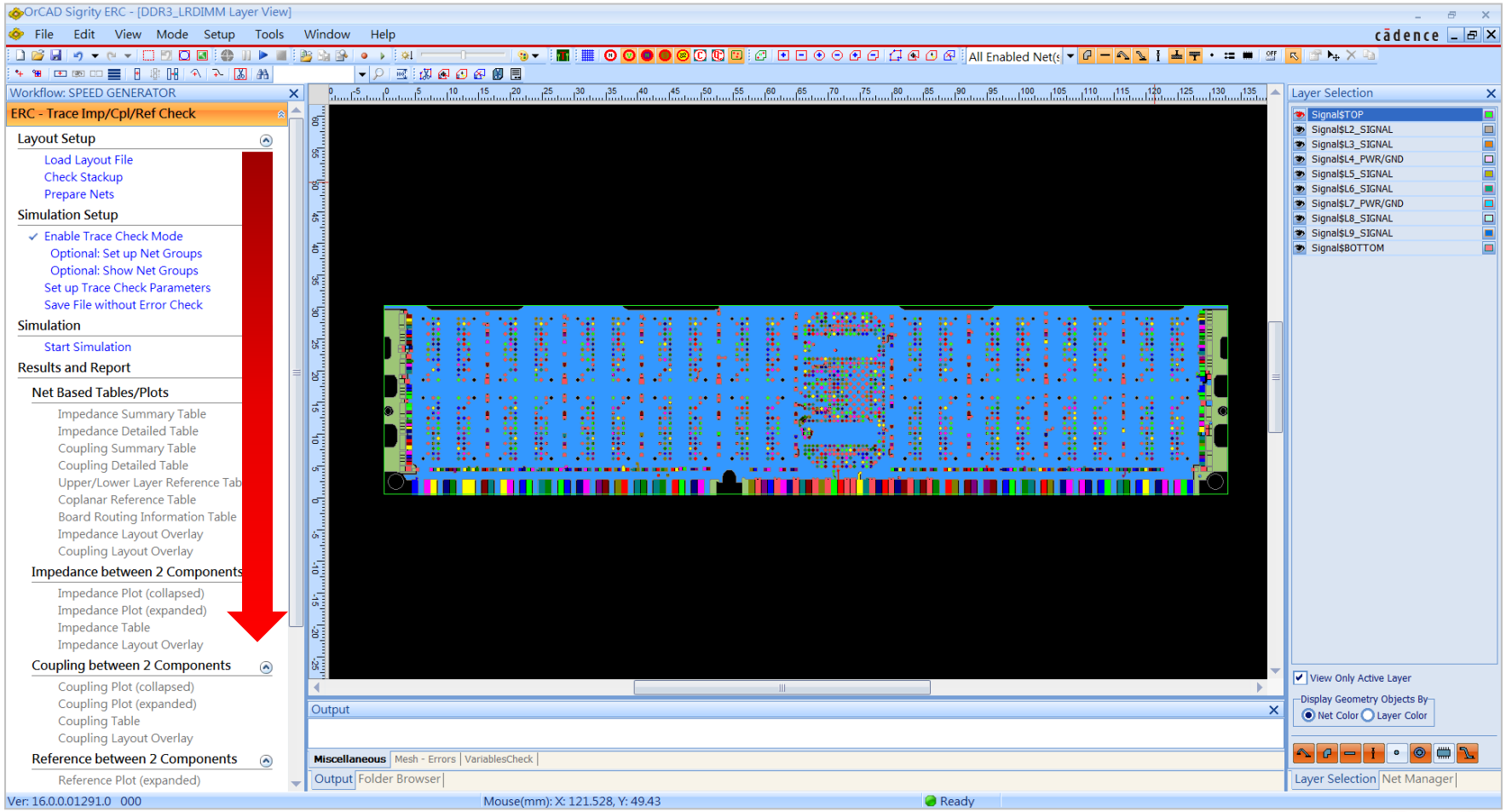
Note:
This is the reason why there are 5 impedance sections.

OrCAD ERC/SRC Checking Flow

- Example : DDR3 DIMM module
  - 1 buffer: U100
  - 36 DRAMs: U1 – U36
  - 10 layers



Easy Workflow



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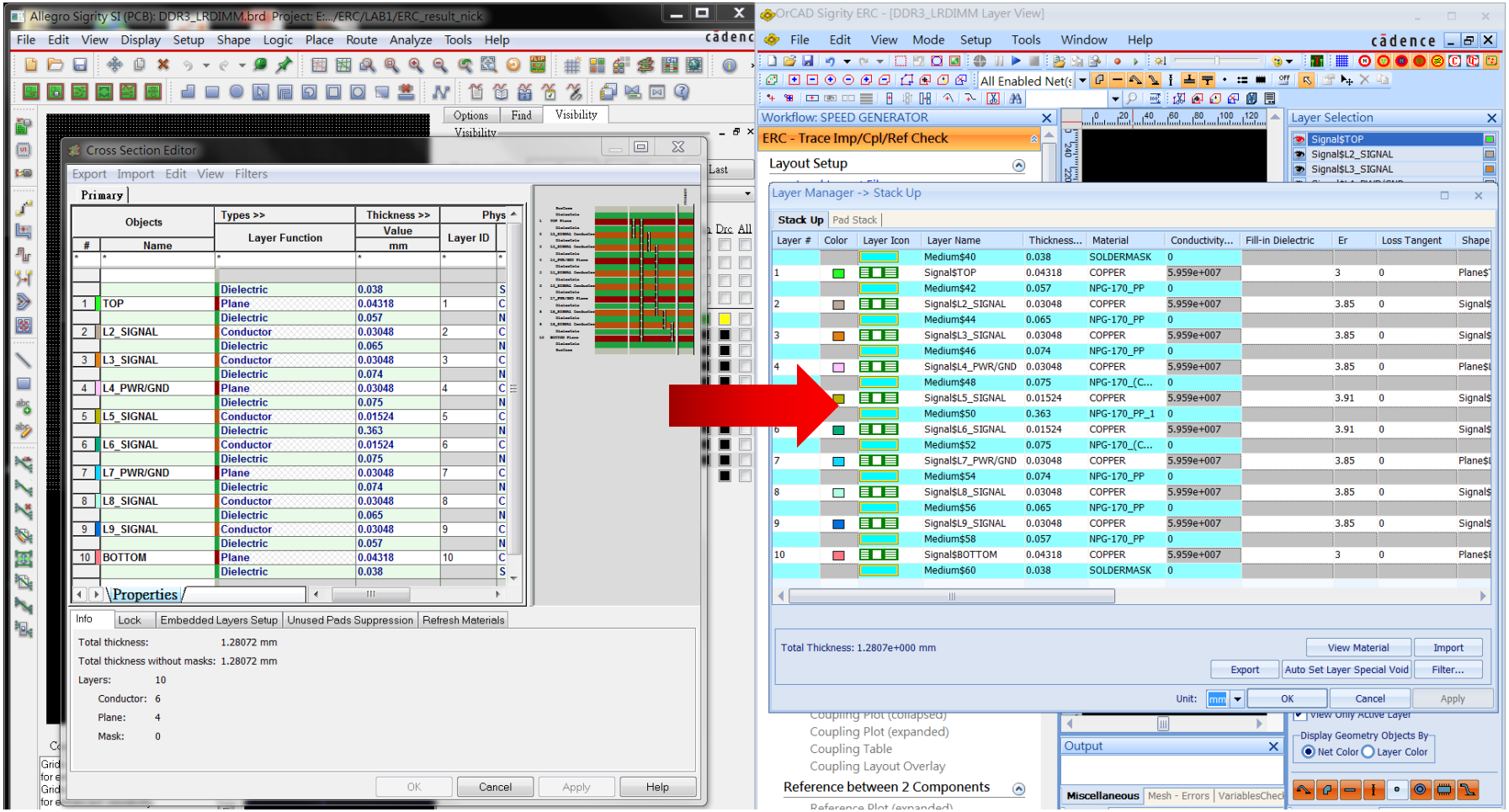
Check Stackup



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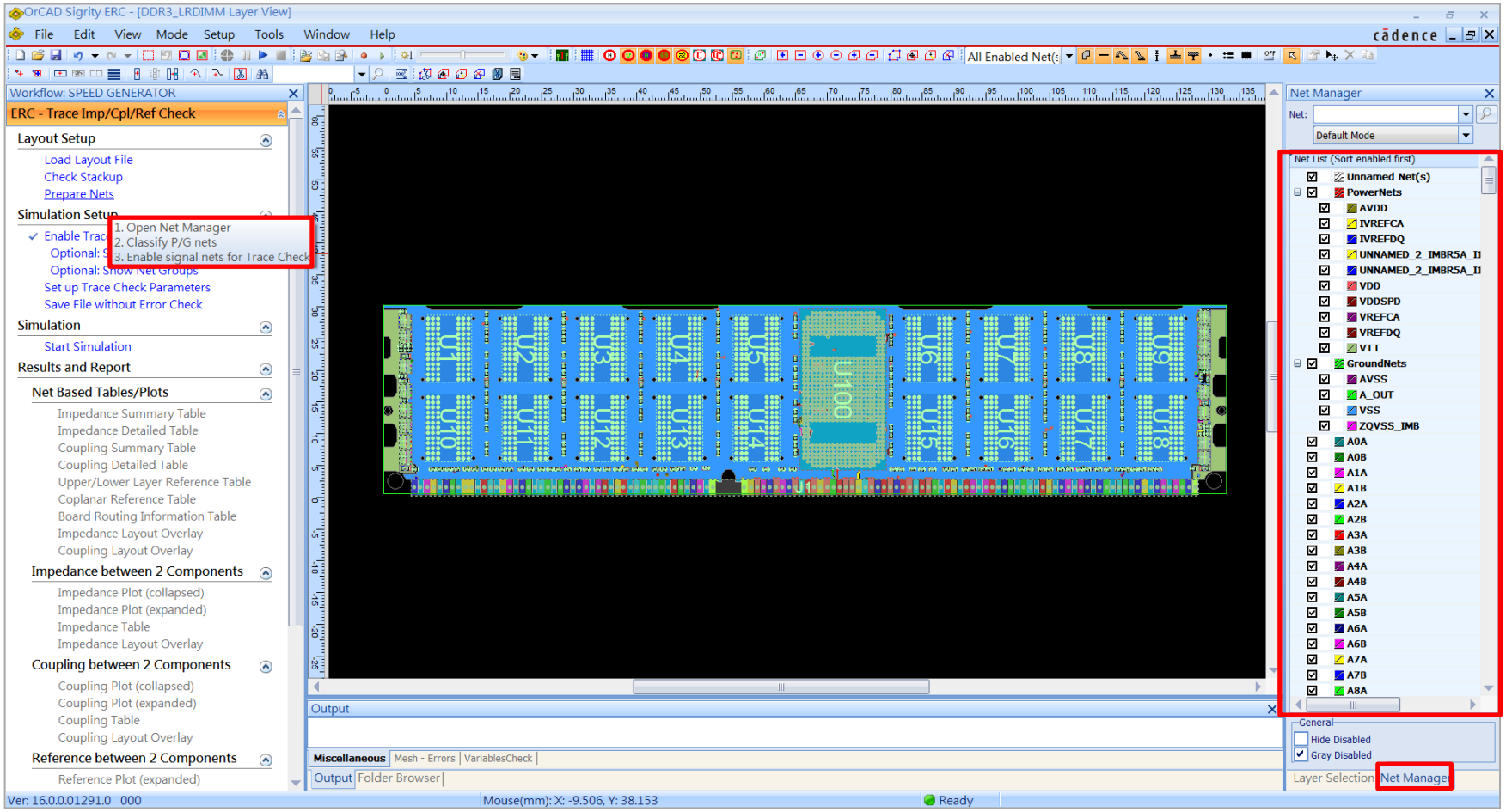
Classify Nets



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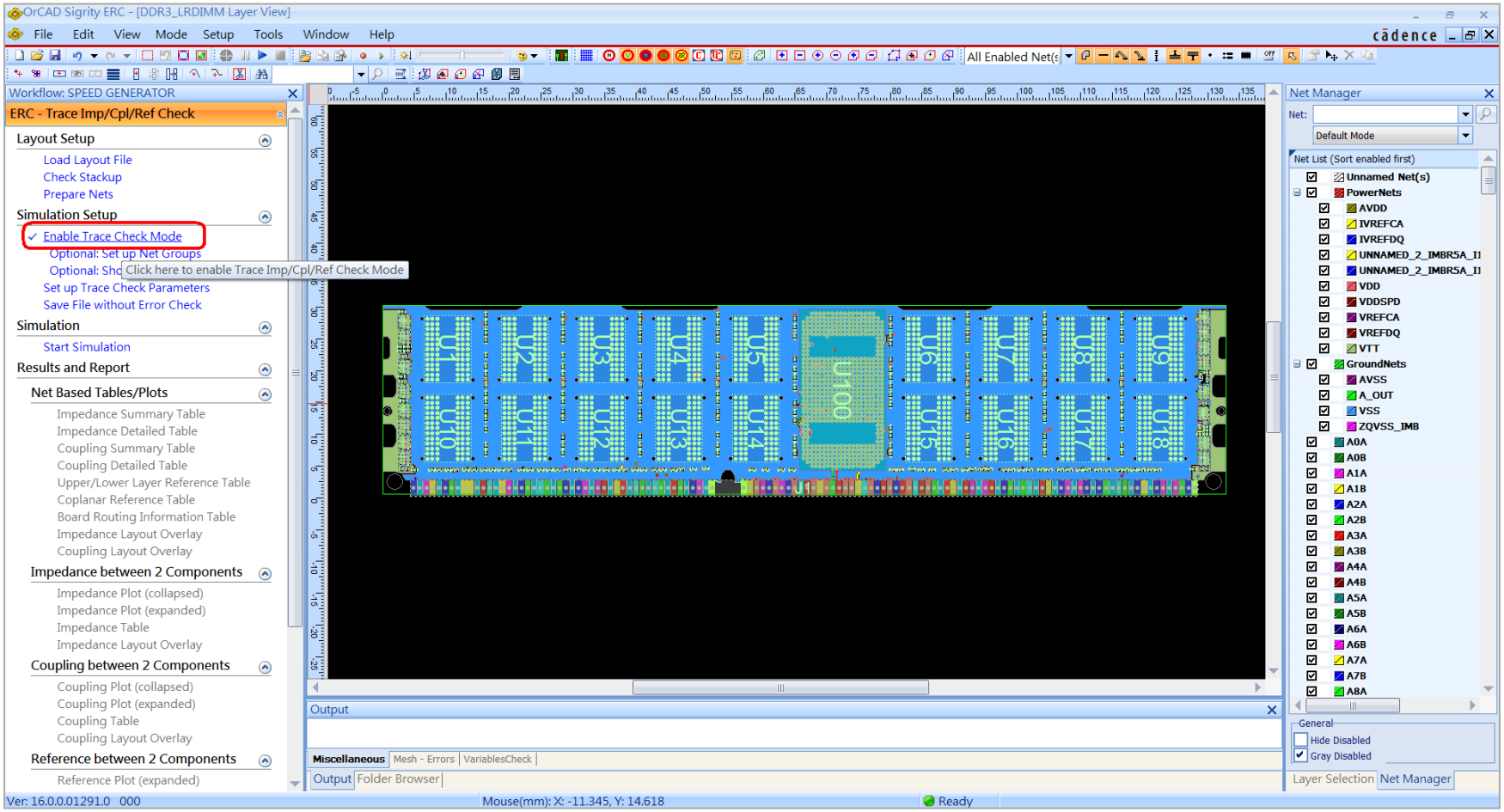
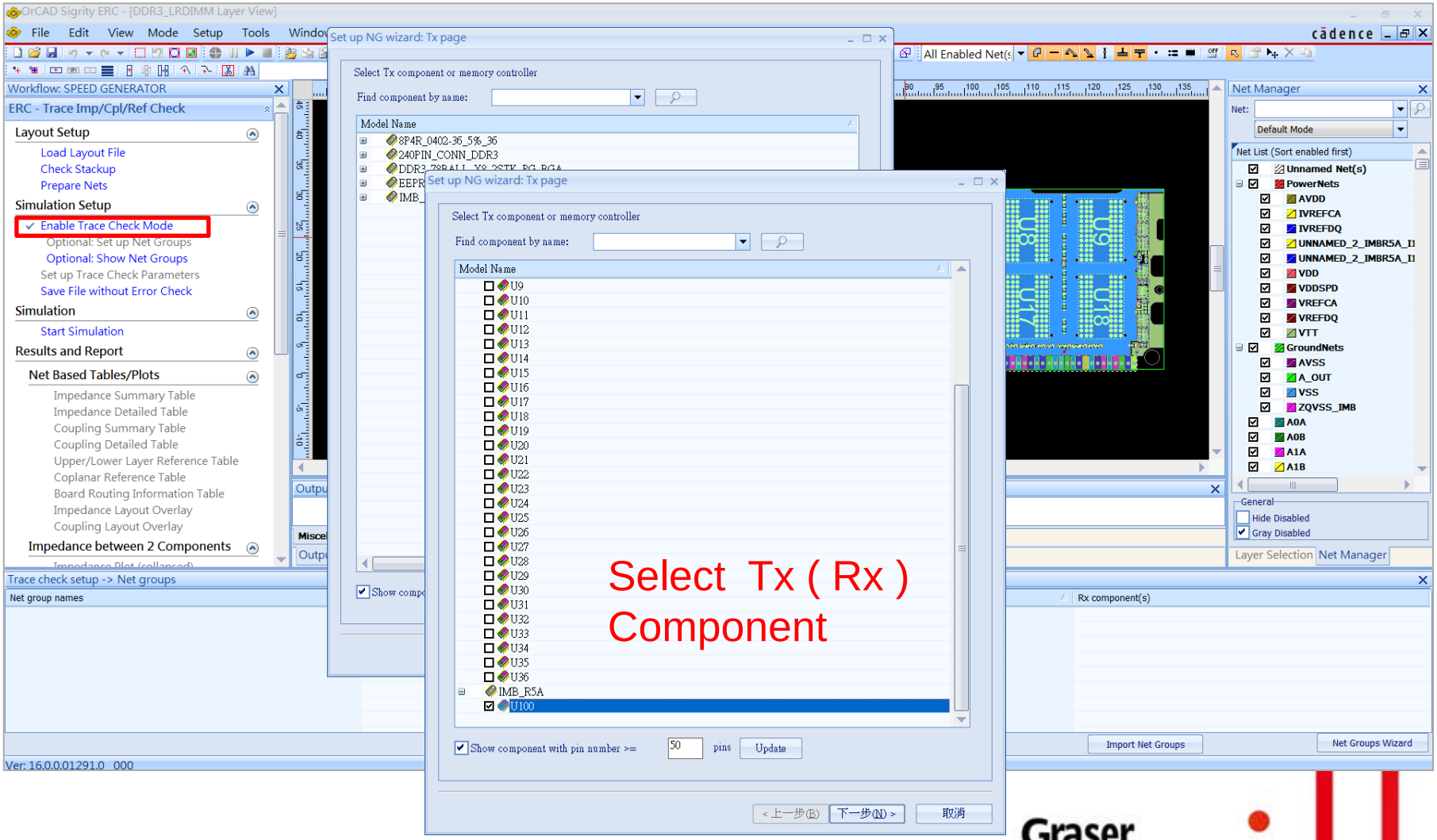
Enable Trace Check Mode



Nets Select Tx & Rx Components



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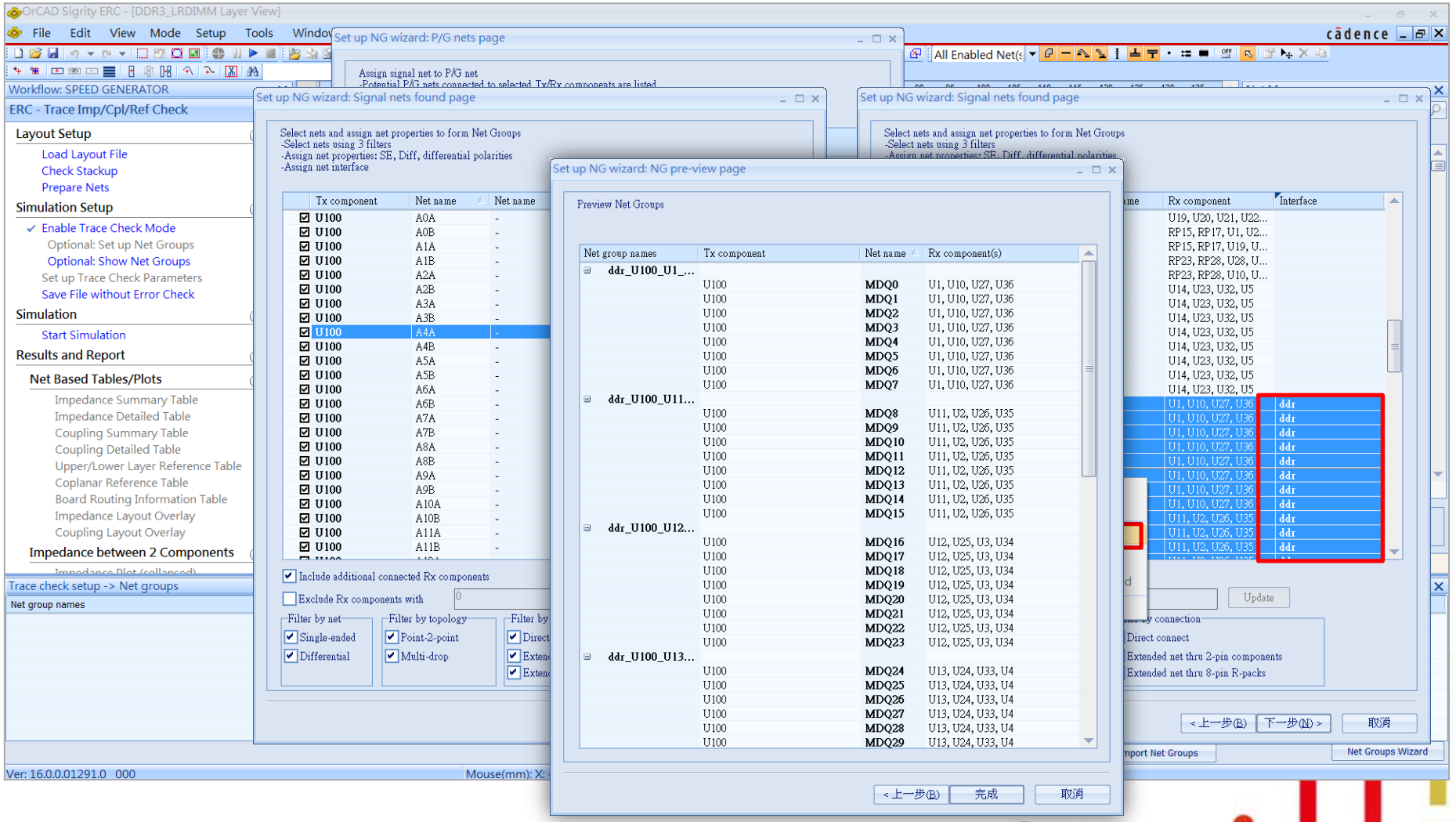
Set up Net Groups (Signal nets)



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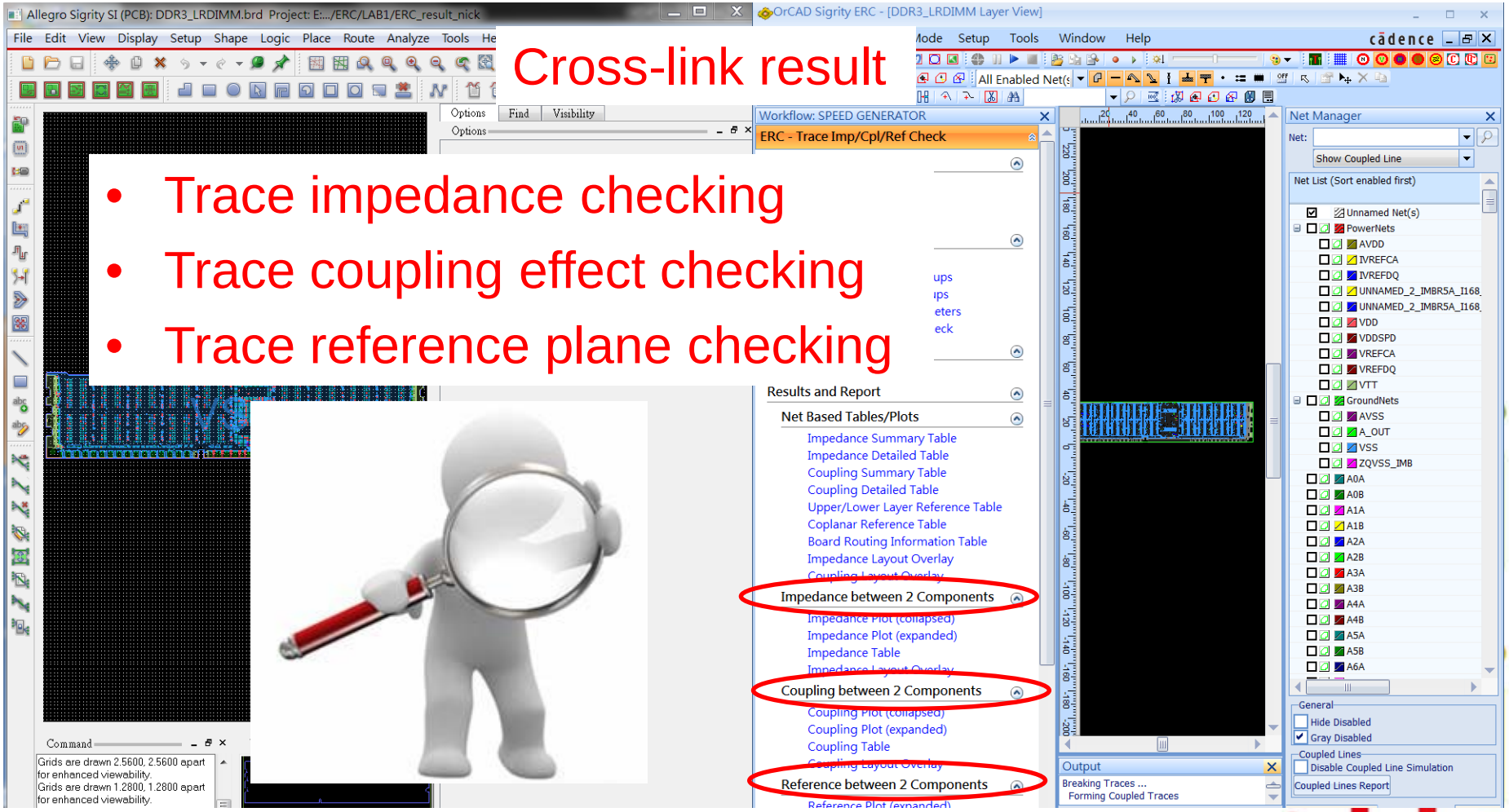
Simulation & View Result



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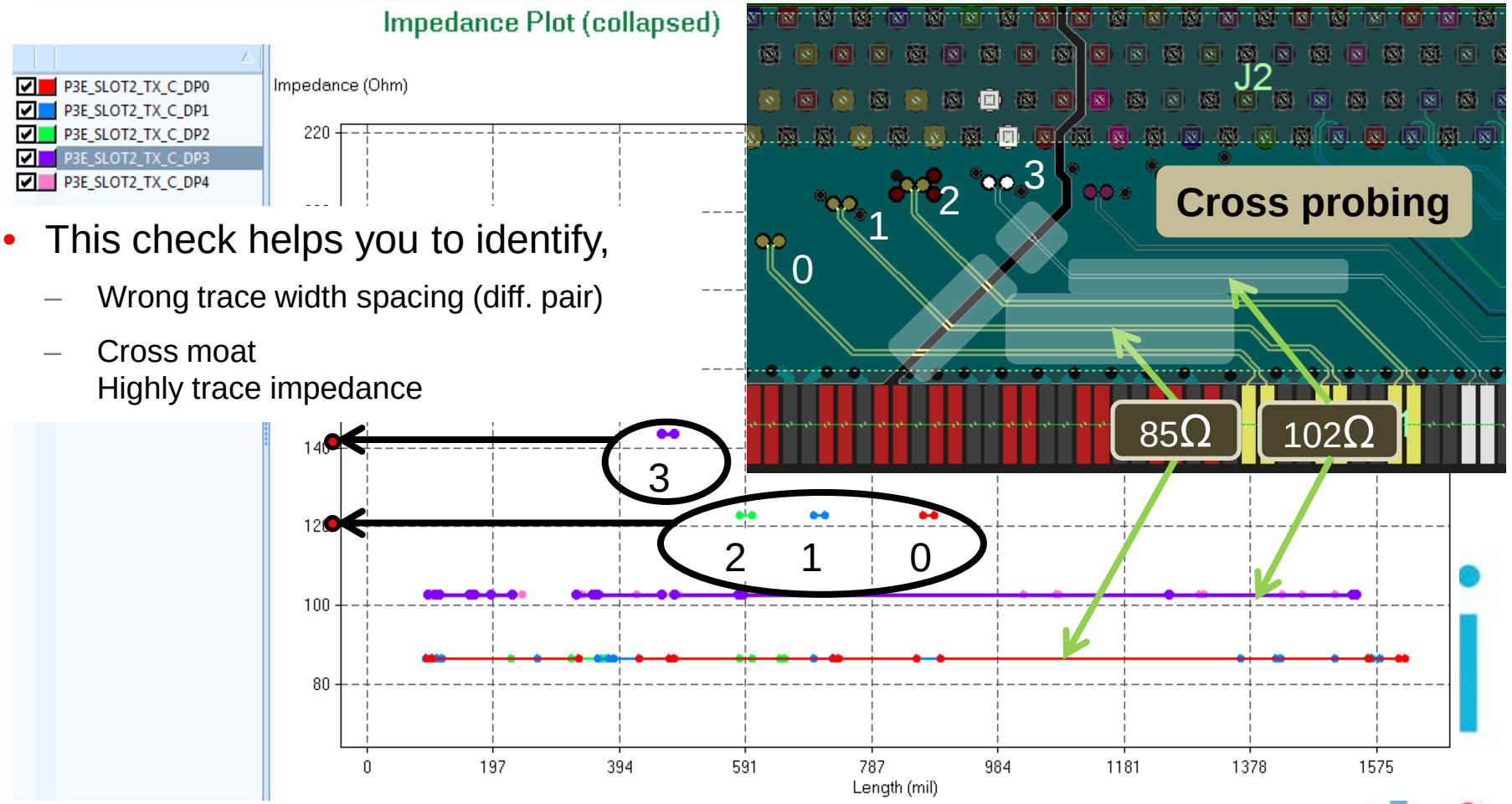
Trace Impedance Check



- This check helps you to identify,
  - Wrong trace width spacing (diff. pair)
  - Cross moat
    Highly trace impedance

- Visually or tabular result for trace impedance check that shows trace segments mismatch with target impedance.

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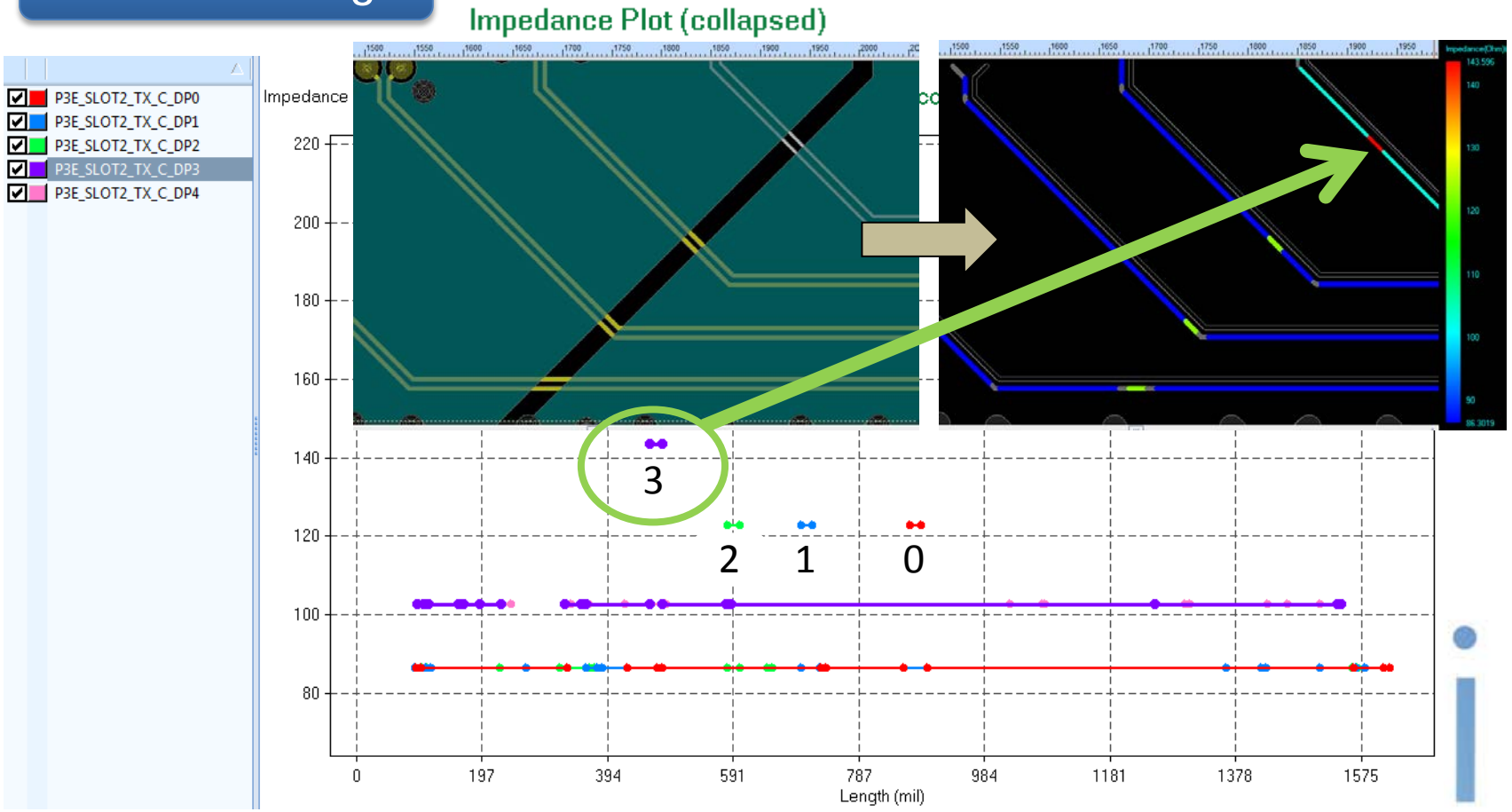
Trace Impedance Check

Cross Probing



- Cross probing allows you to identify defects quickly.

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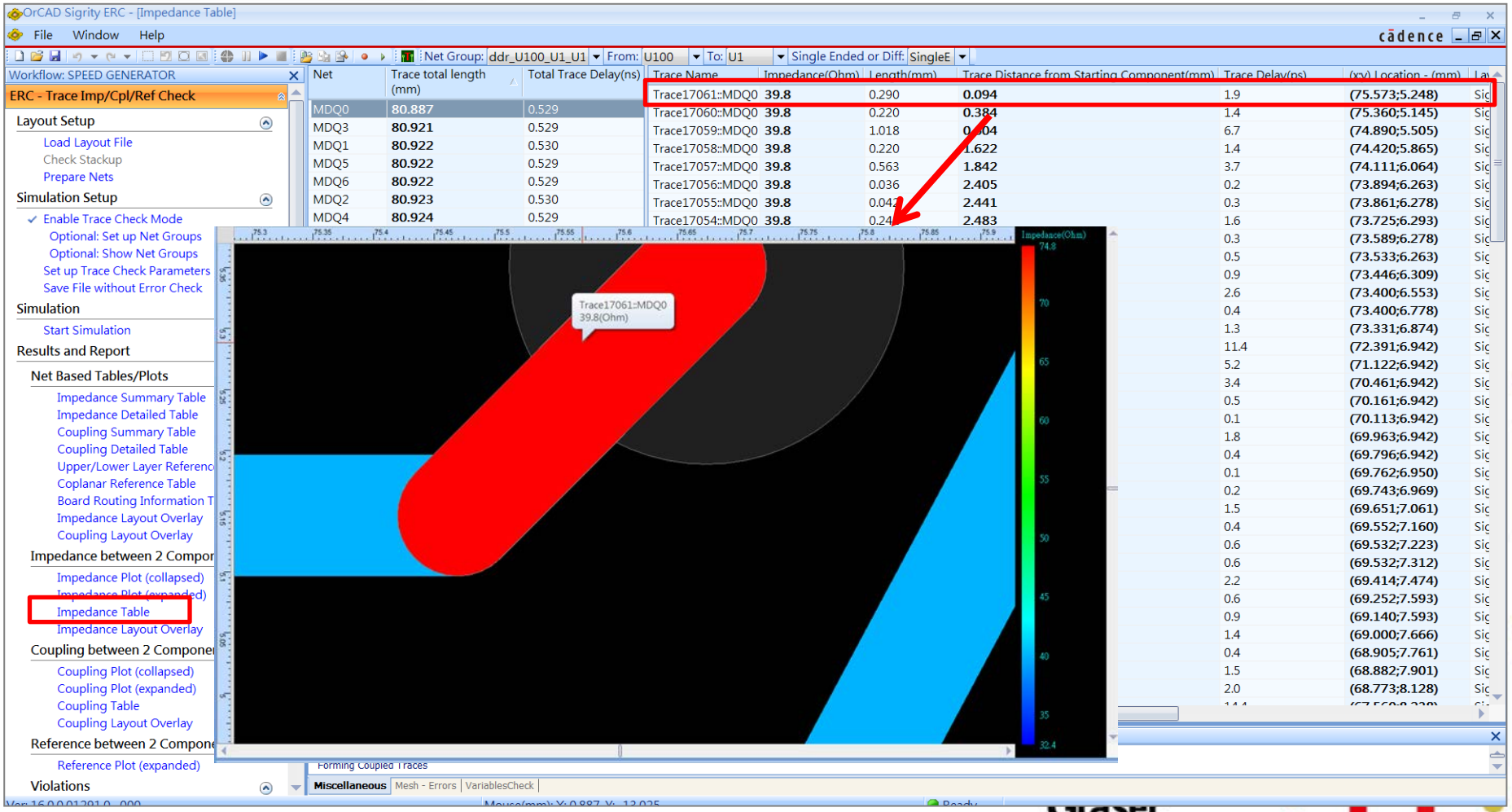
Trace Impedance Check

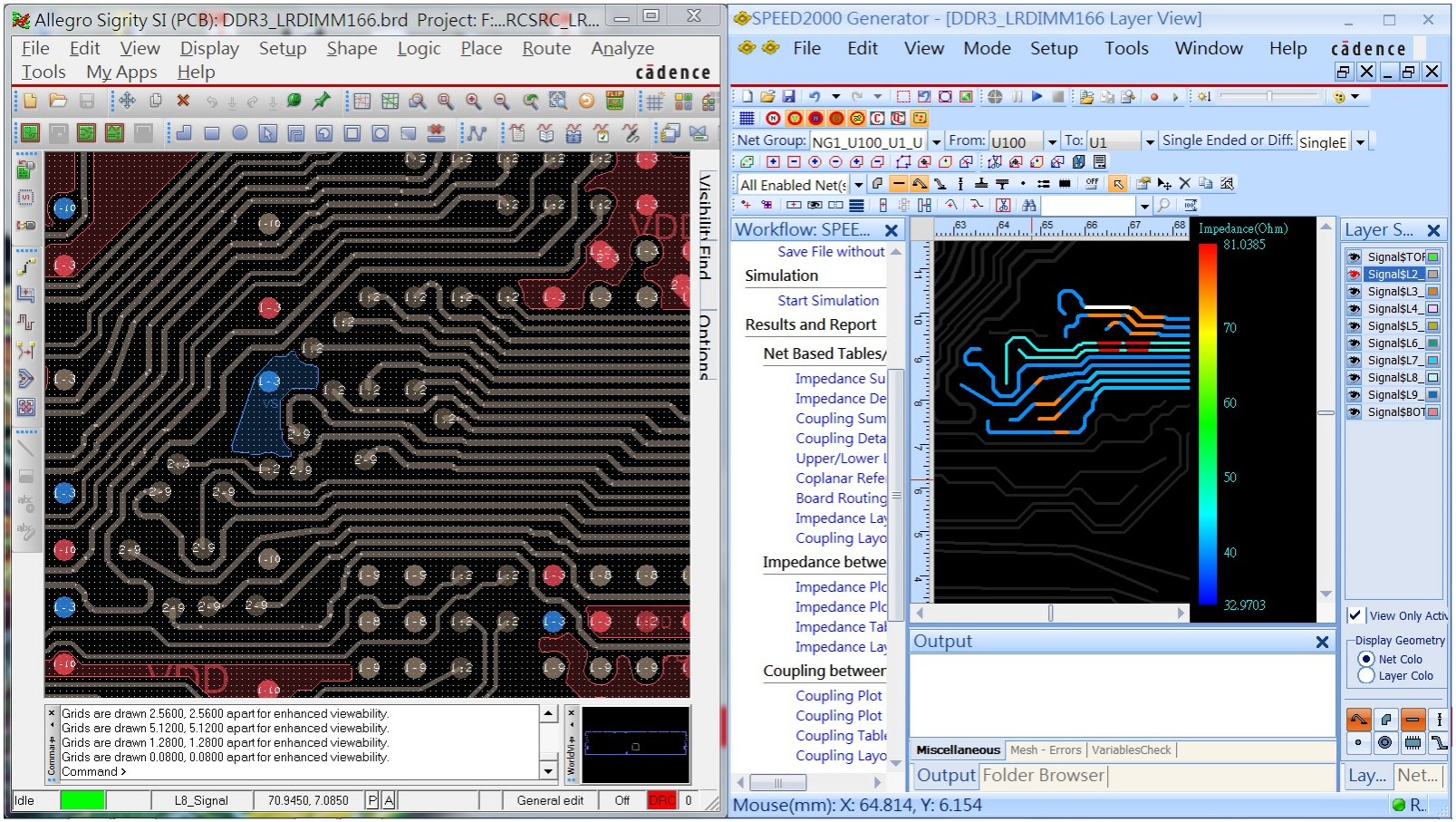
Tabular Results



Trace Impedance Check

Auto-Zoom in board

Impedance Layout Overlay



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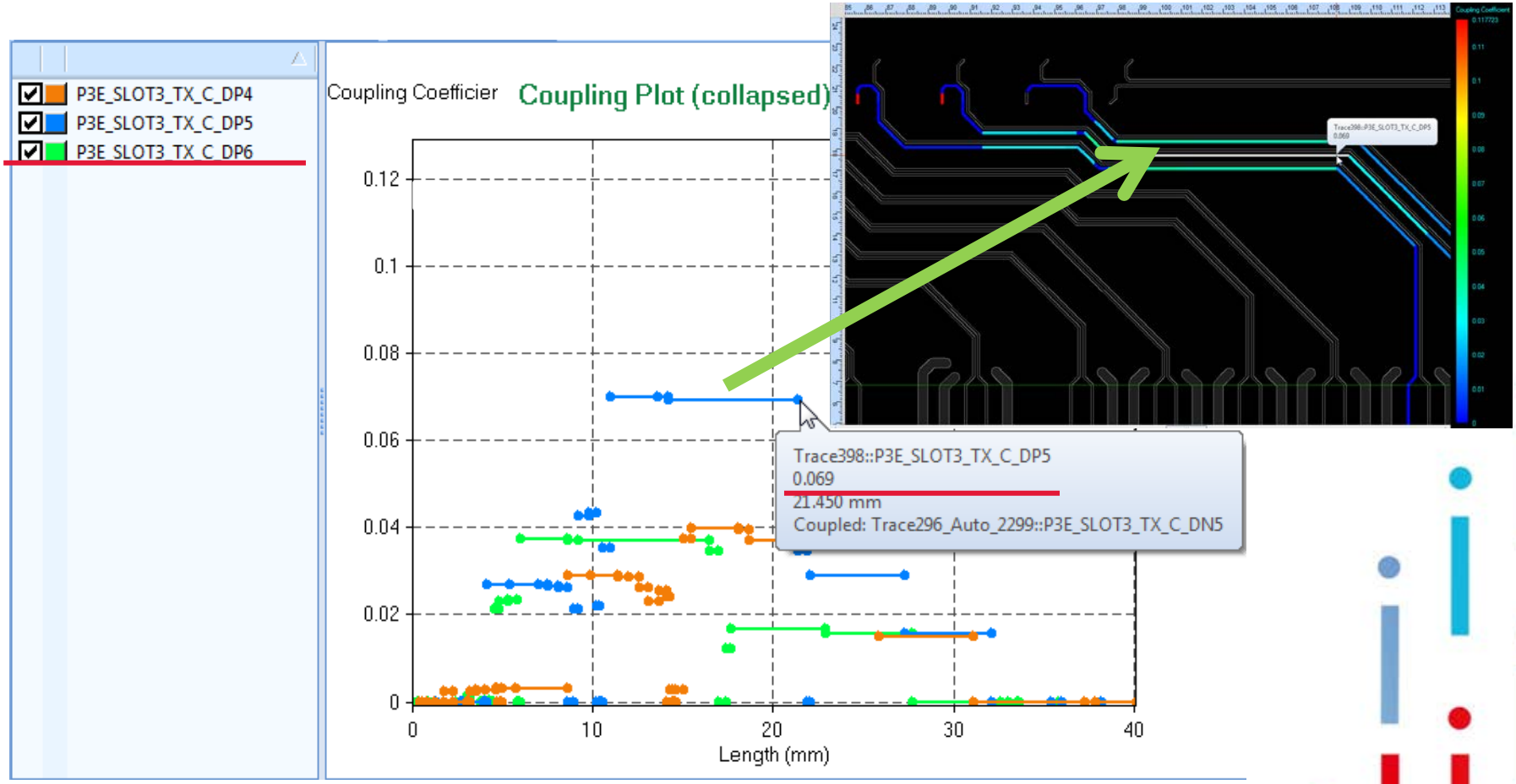
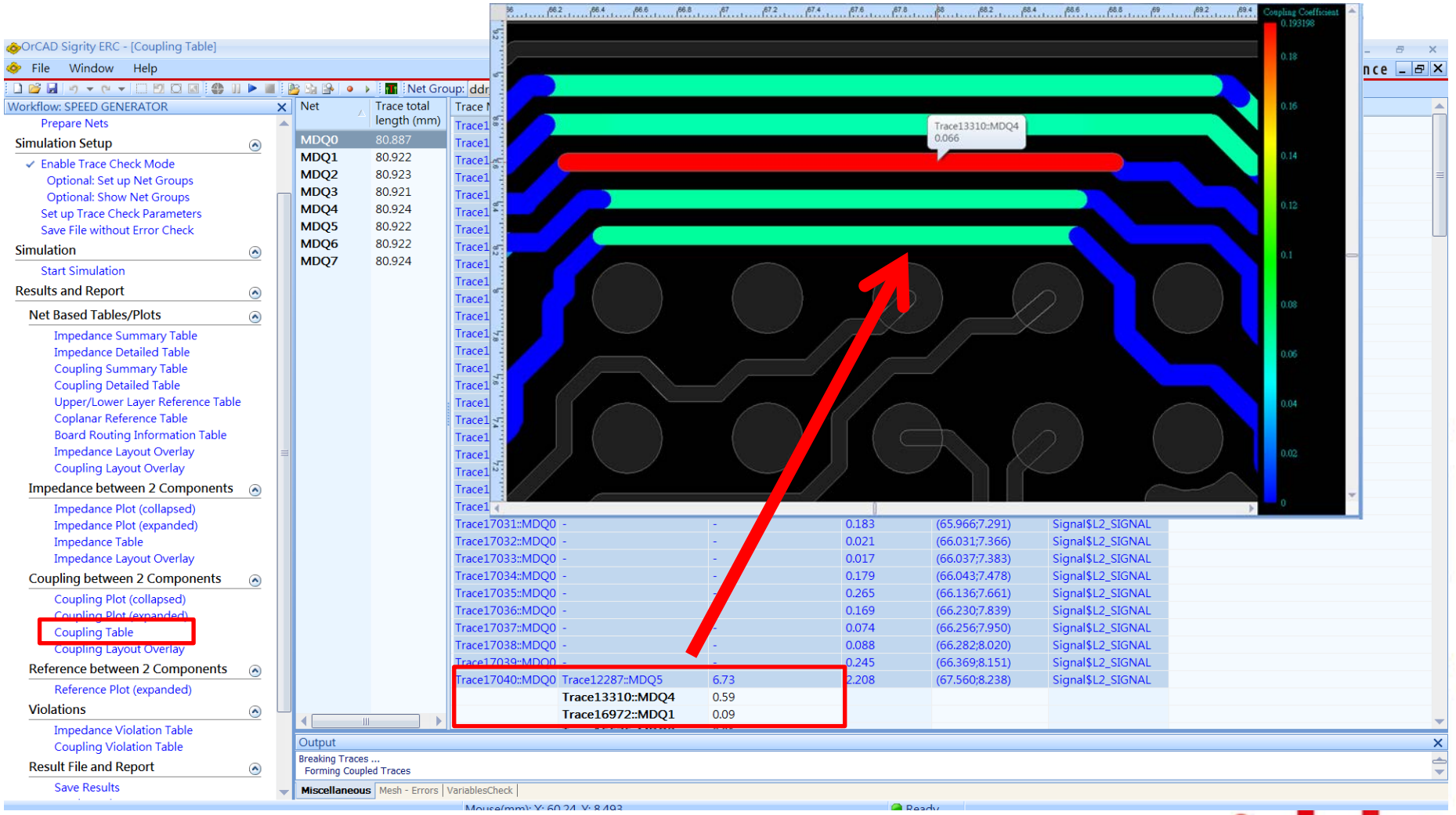
Trace Coupling Check

Cross probing helps to resolve issue intuitively



Trace Coupling Check



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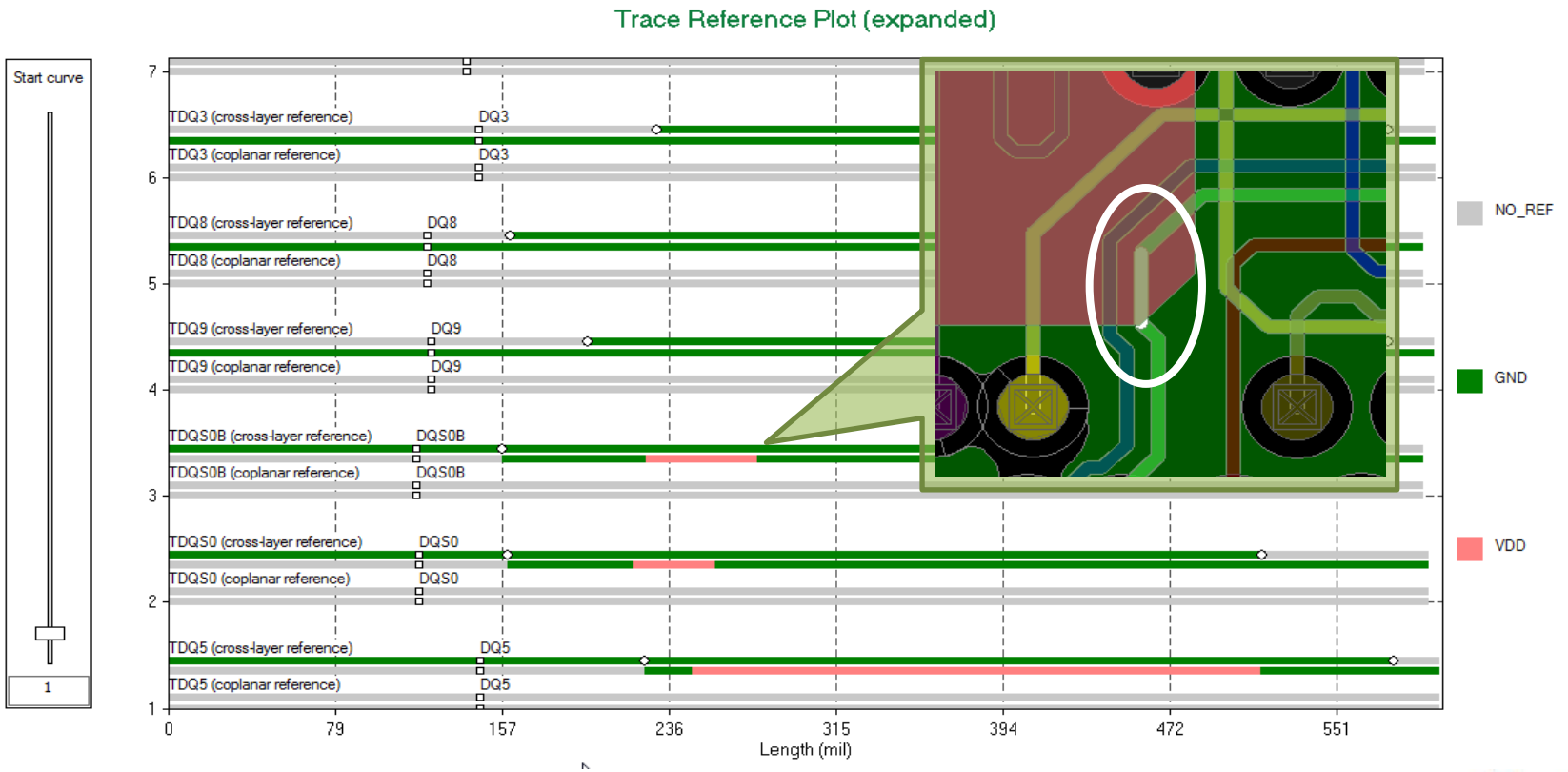
Trace Reference Check (Including co-planar)



- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

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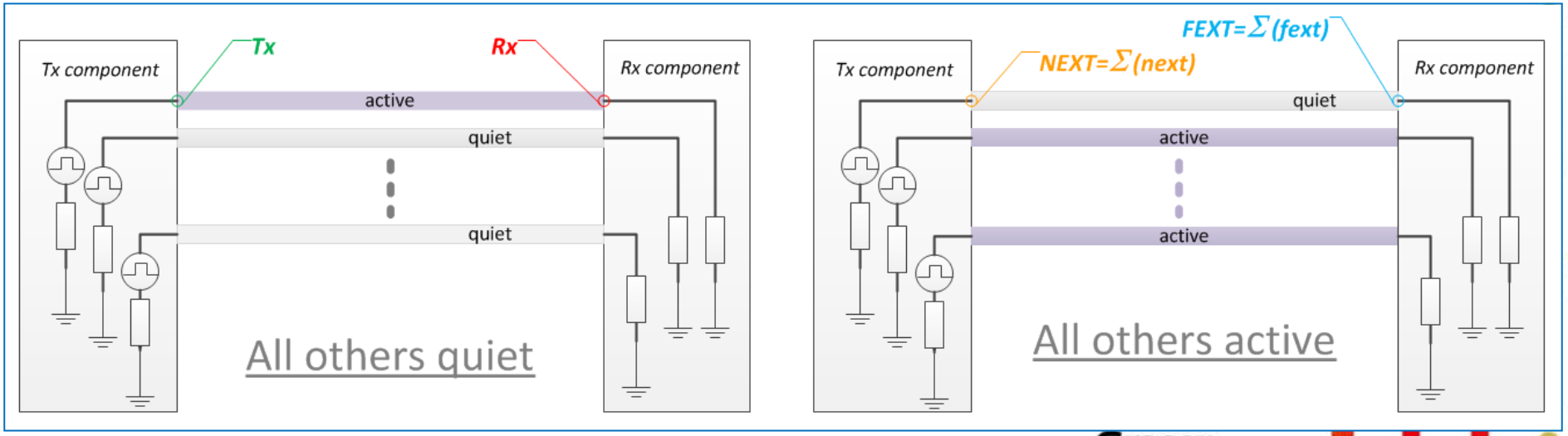
Signal Base Checker - SRC

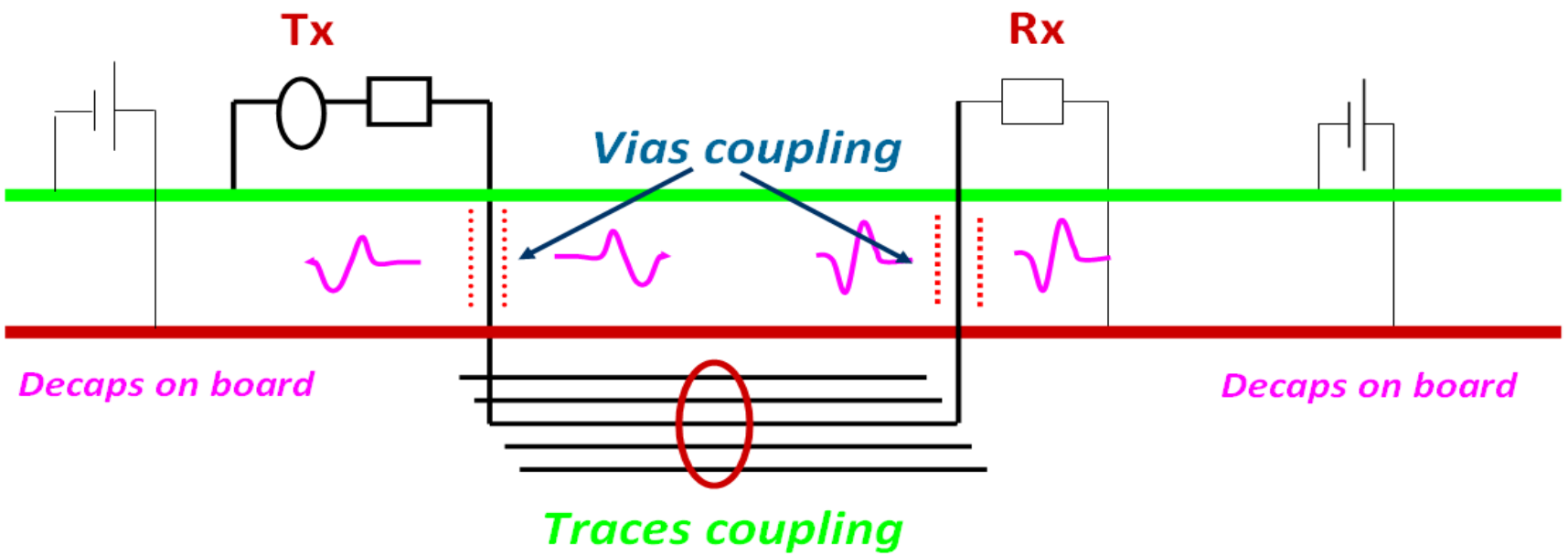
What is Sigrity SRC?

- OrCAD® Sigrity™ SRC is Macro, combined, net-level view in time-domain of impact due to ERC violations measured in mv&ps (no device model needed)
  - Setup considering termination impedance, data rate (pulse width, rise/fall time), and amplitude
  - Results with Tx/Rx/NEXT/FEXT waveforms, SI performance metrics
  - Organized to easy SI performance interpretation along with ERC
- Practical for board level check (setup, simulation, report)

<2min ~ 20min auto

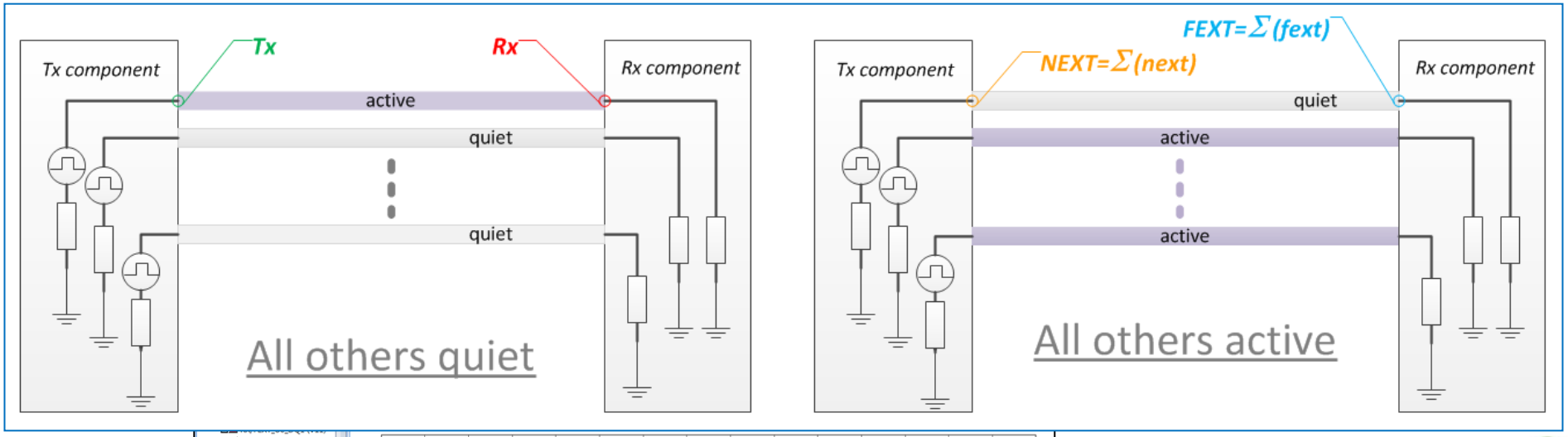


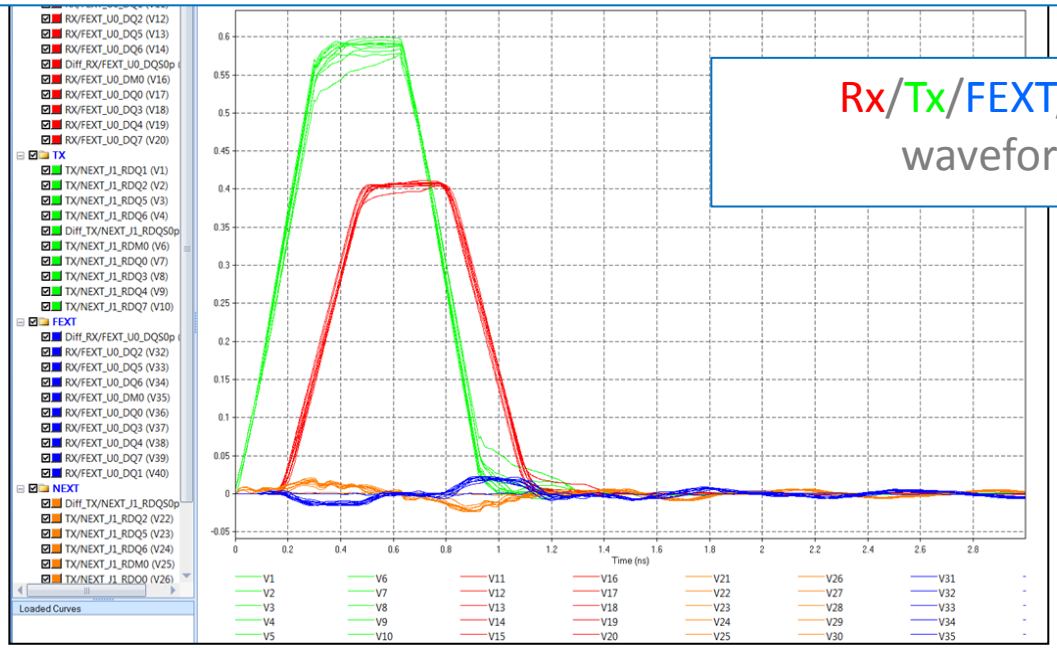
SI Channel Check



- Signal quality is affected by crosstalk among signals, EM coupling between signal and P/G planes and non-ideal return current path.
- The linear source and load are applied automatically for signal TD simulation
- Post process result waveforms (signal waveform, NEXT/FEXT waveforms) into signal to noise ratio for signal quality judgment

Time-domain Waveforms





Rx/Tx/FEXT/NEXT
waveforms

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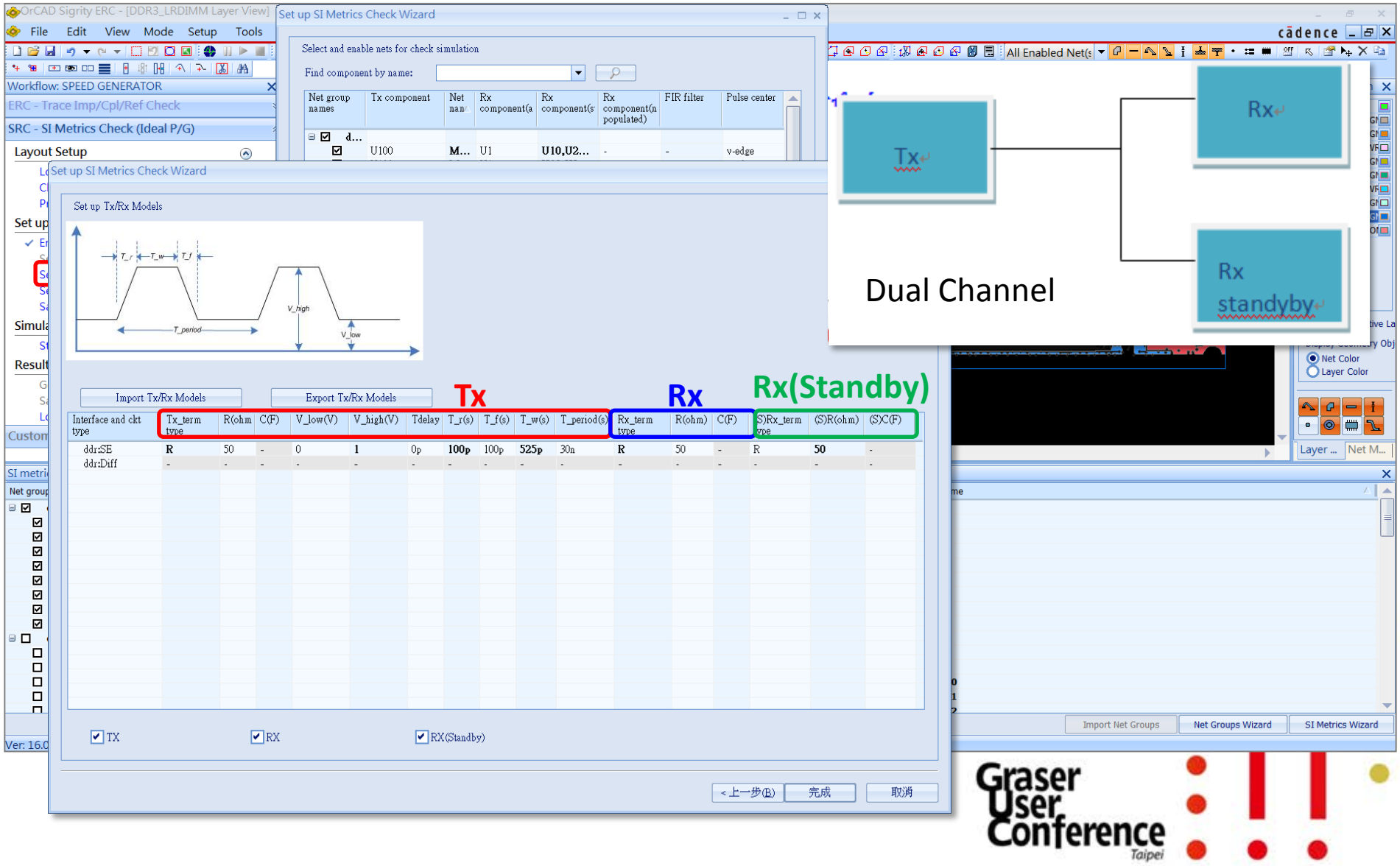
Setup Models



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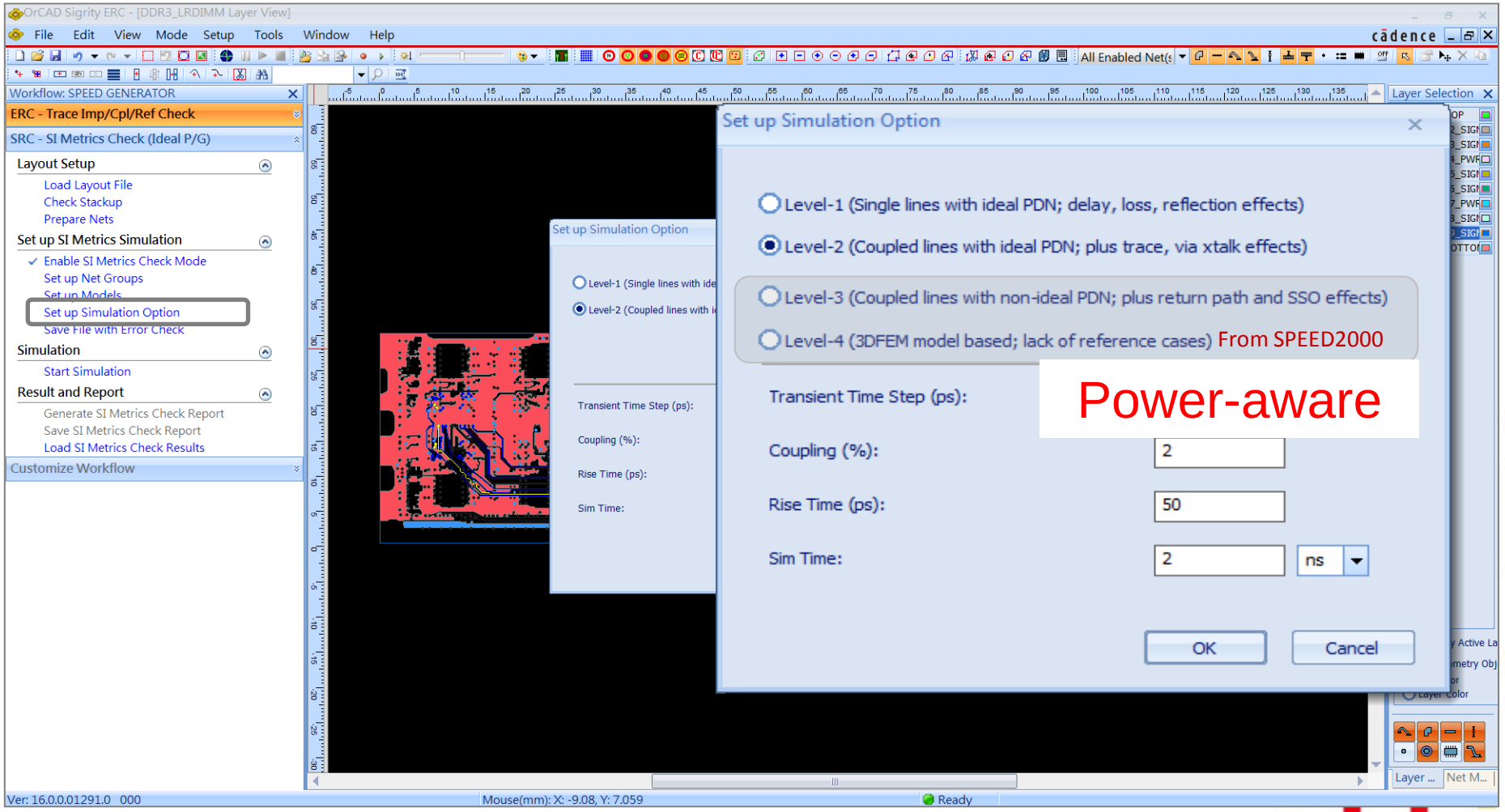
Set up Simulation Option



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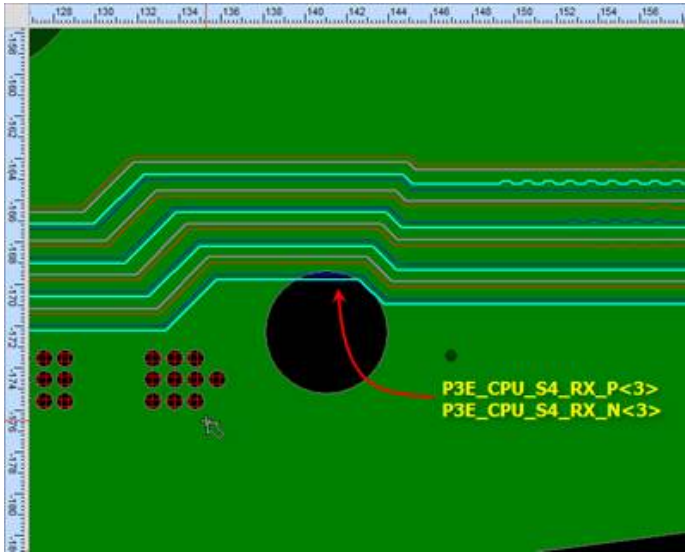
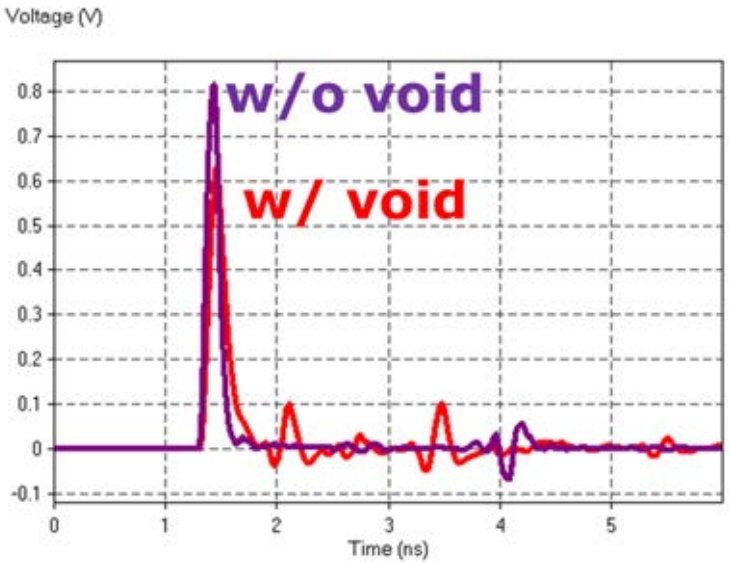
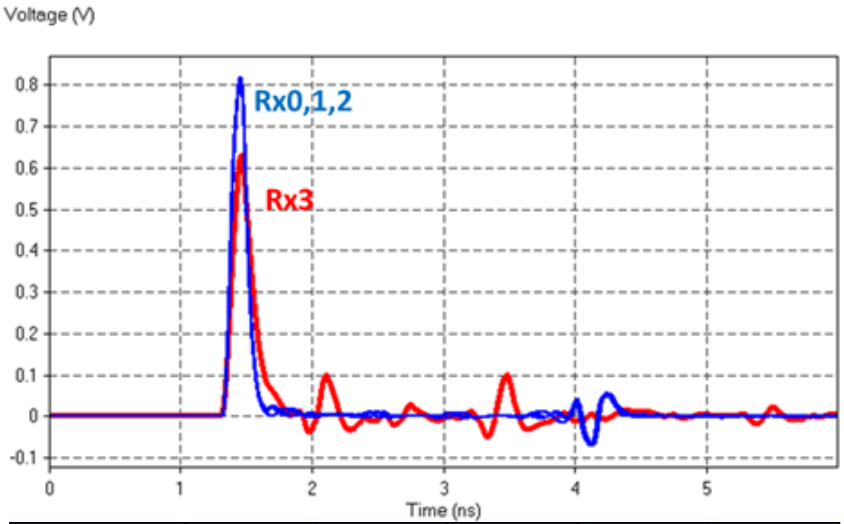
SI Channel Check



- An example shows the trace segment is over the void that causes impedance discontinuity and leads to worse signal quality





	INT_Sig	INT_ISI	INT_XTK	P-eye	P-ratio
RX3 w/ void	67.84	104.59	5.12	-41.87	0.62
RX3 w/o void	86.00	54.64	5.00	26.36	1.44

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SRC Net-level View → ERC's Segment-level View

Sigrity ™ SRC

- Layout SI macro view at net level
- All inclusive end results
- Shows what happened and its effect on performance

Sigrity ™ERC

- Layout SI micro level view at segment level
- Individual segmented results
- Shows why low performance happened and how to fix it

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Summary

- OrCAD® Sigrity™ ERC/SRC fills the gap between layout designers and SI engineers
  - Expanded expertise
  - Using same tools
  - Measured by same units

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Thank You