主辦 | Graser 協辦 | cadence

Getting Confidence
in Your Design Early!

Graser User Conference

Taipei

2016 7.14

跨界整合 翻轉設計

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系統級 FPGA 混合信號驗證

Paine Chuang/ Graser

14 / July / 2016

Agenda

- Overview
- Solution
- Implementation
- Successful Story
- Summary

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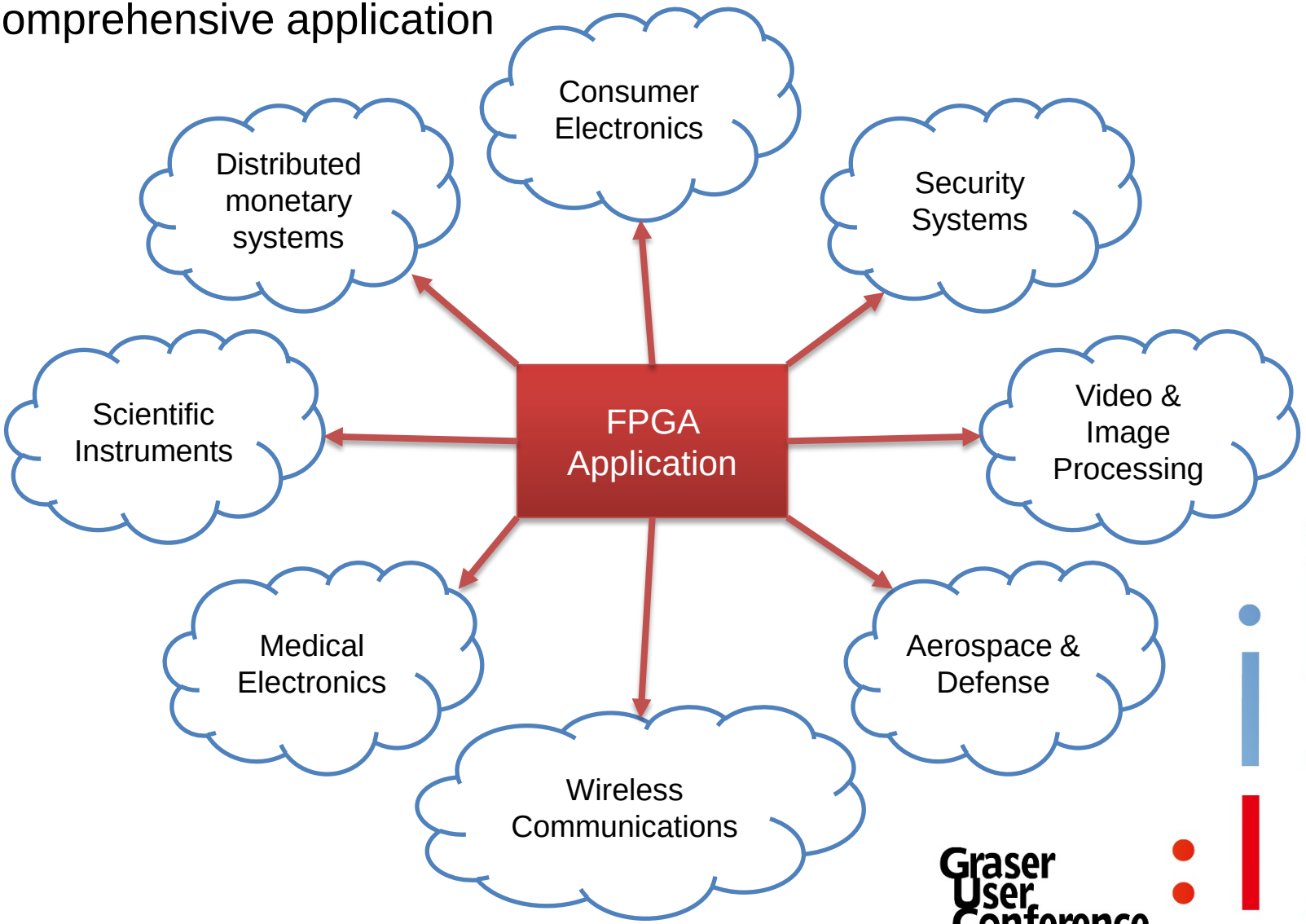
Overview

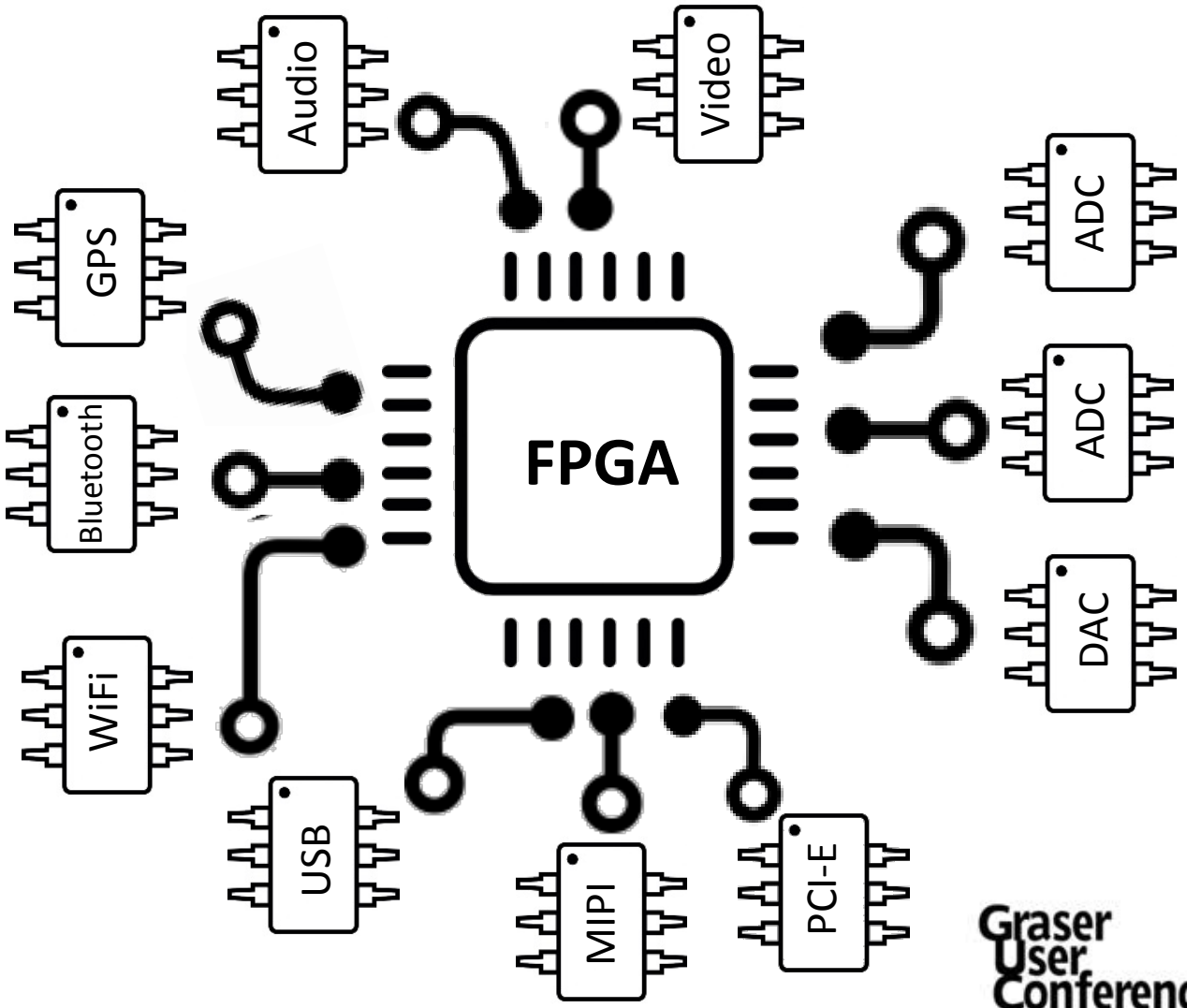
Overview - Application

- Comprehensive application



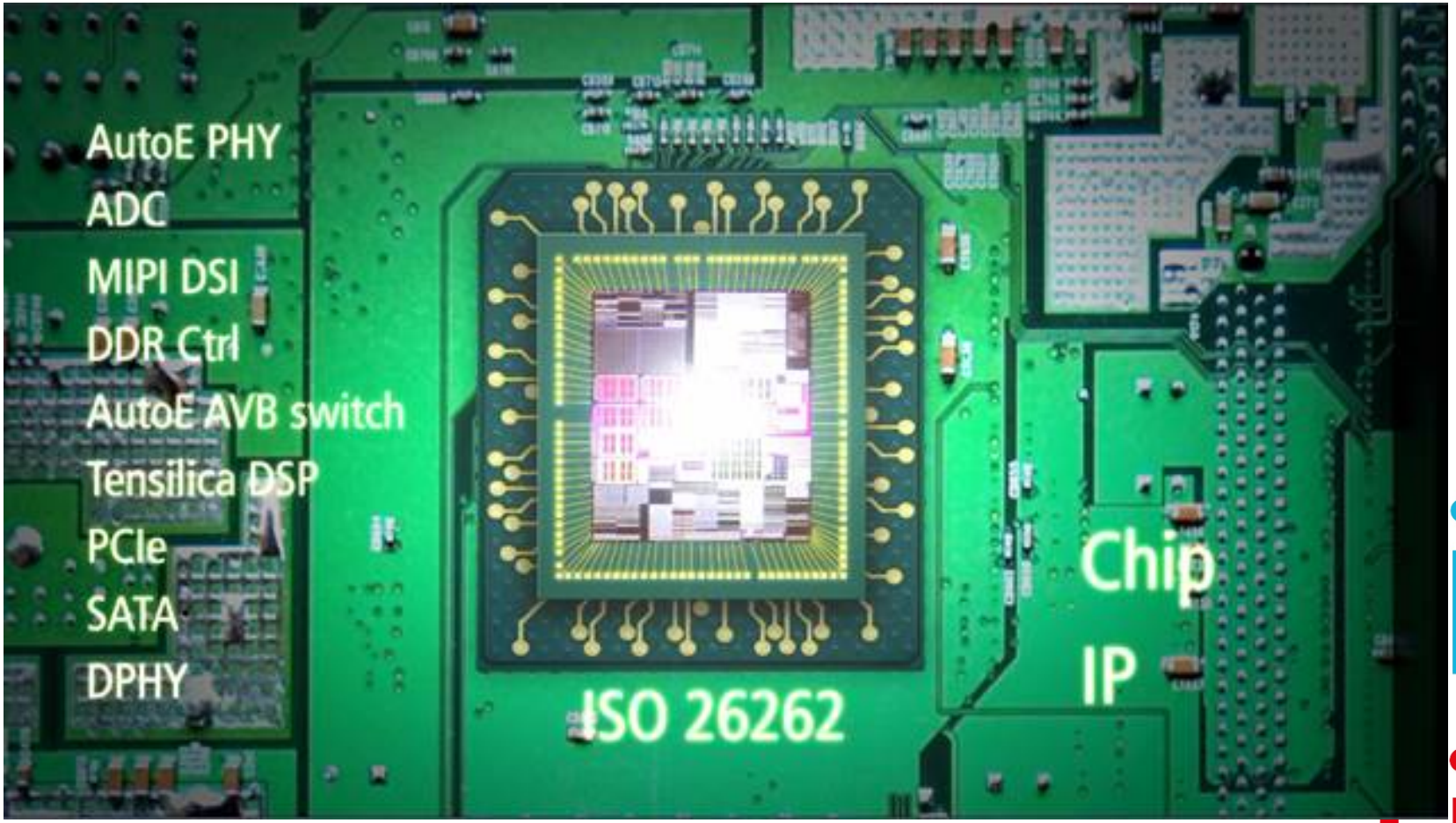
Overview - Chip

- What is the issue between Chip-level and Board-level?



Overview - Board

- What is the issue on Board-level?



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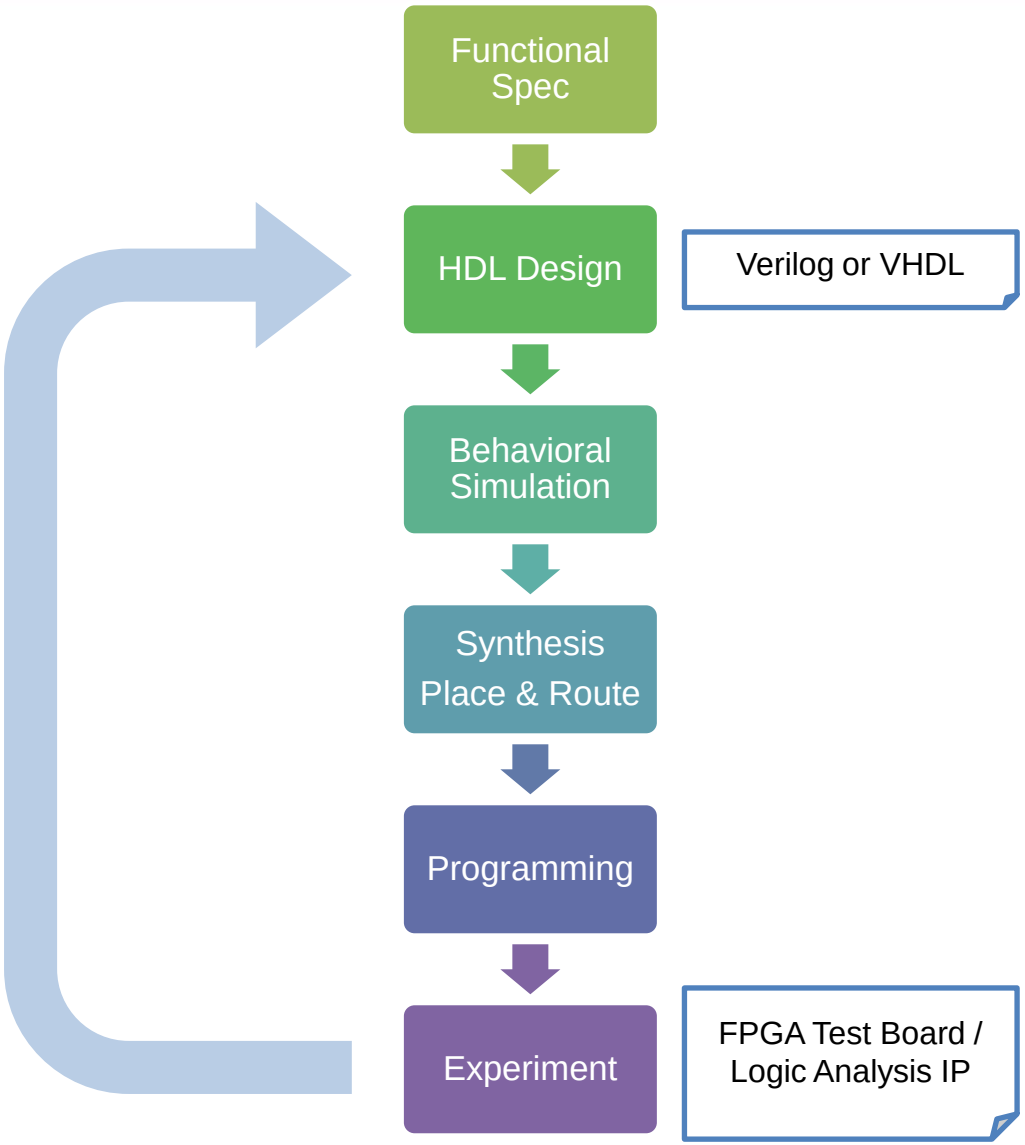
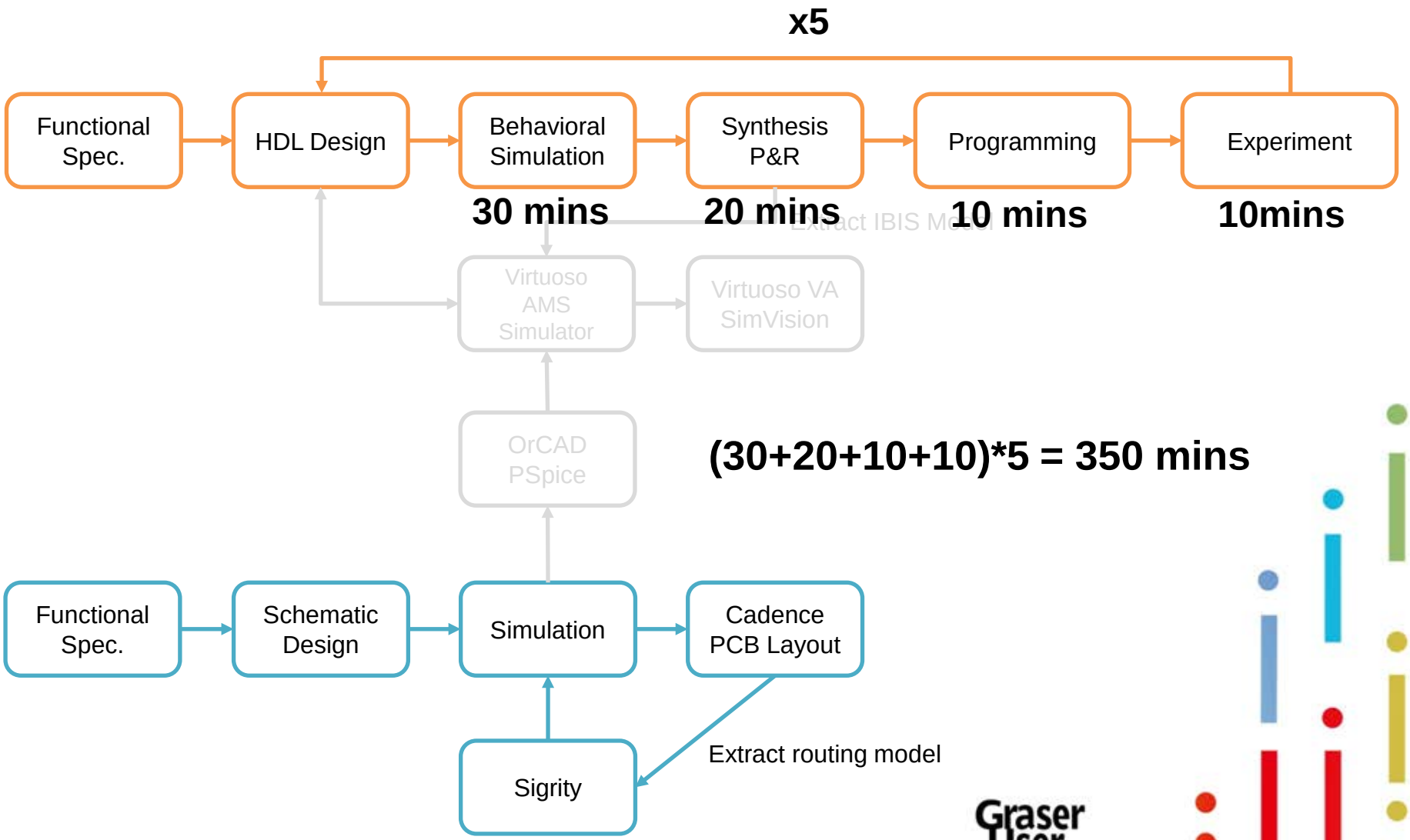
Mixed-Signal Solution

Traditional FPGA Design Flow

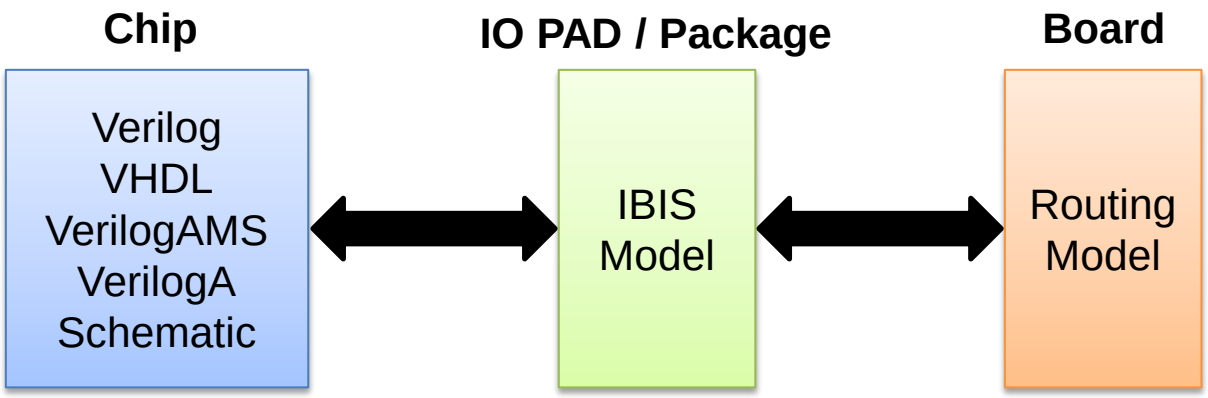


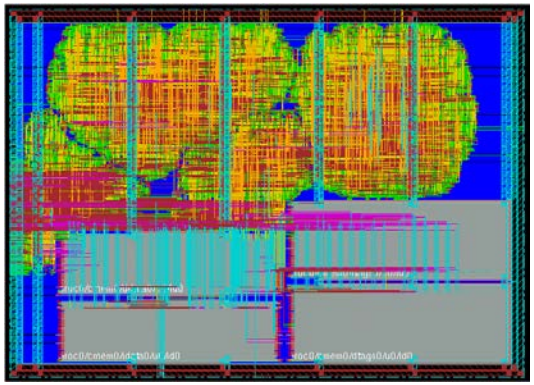
Traditional Flow for FPGA

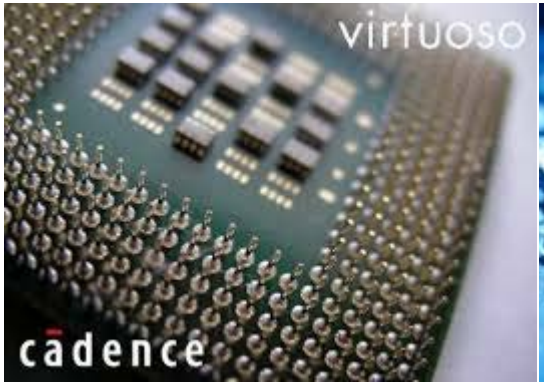


FPGA Mixed-Signal Solution

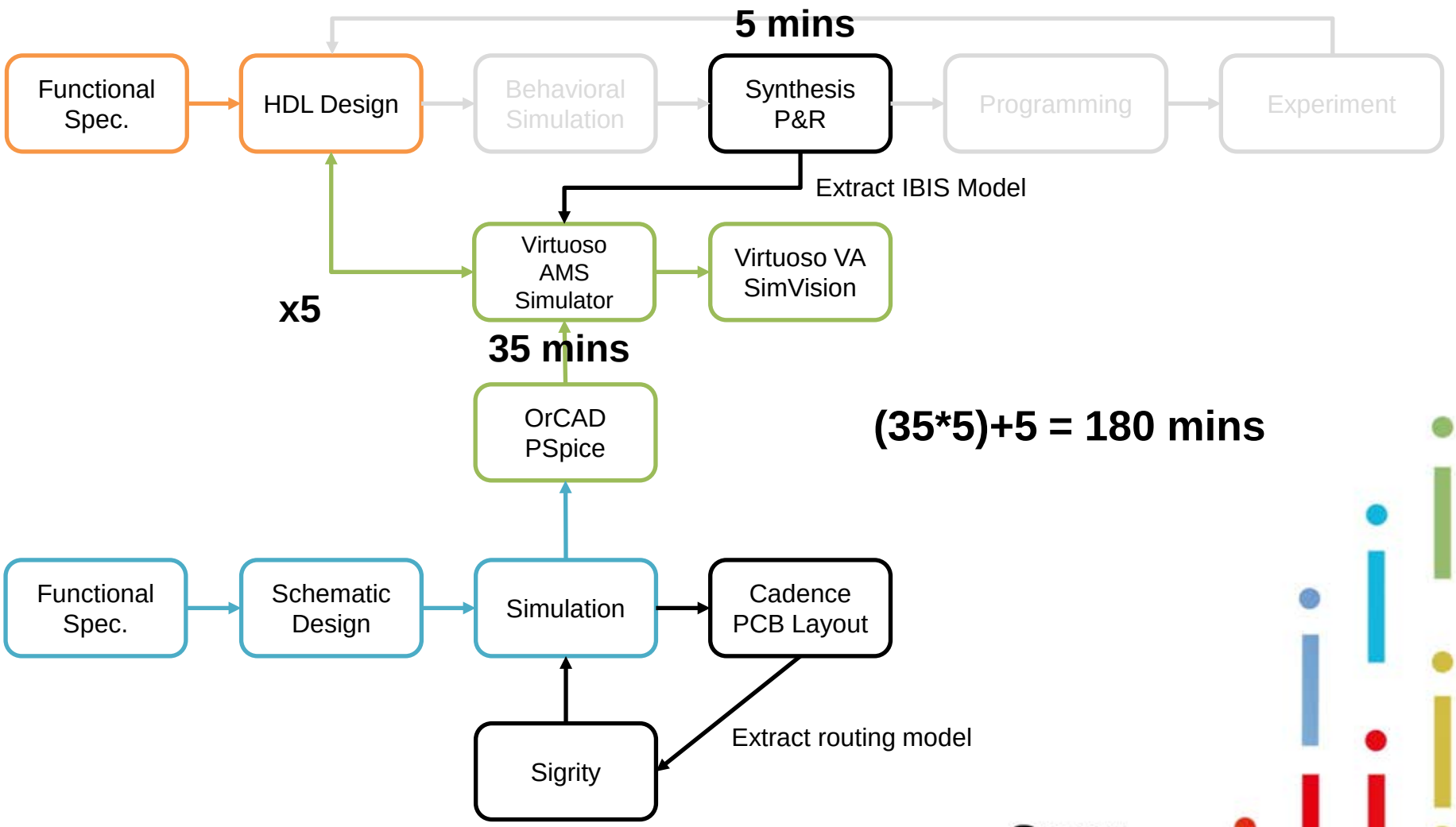
- Integrate with Chip, Package and Board level



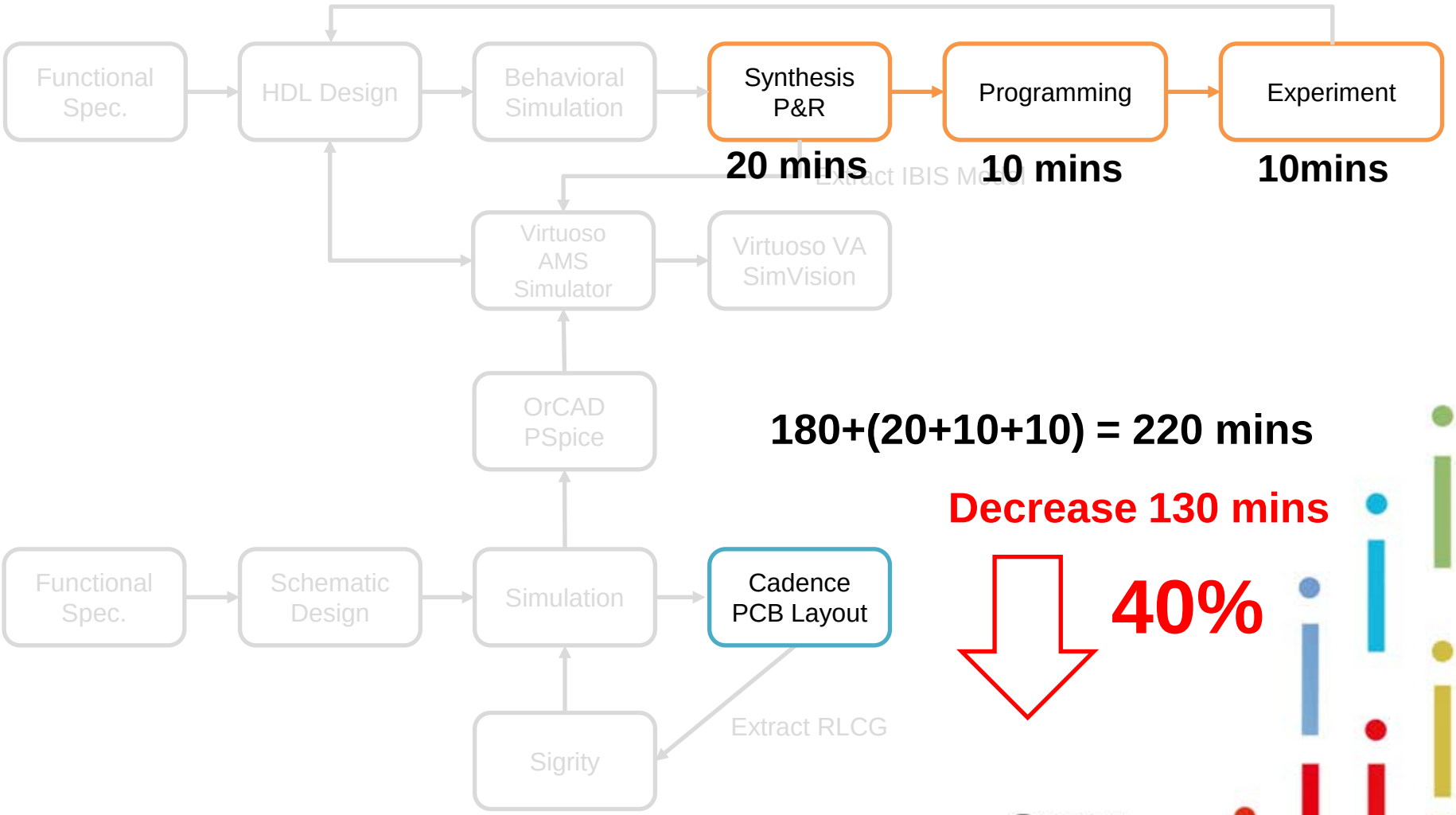




FPGA Mixed-Signal Simulation



Physical Flow



180+(20+10+10) = 220 mins

Decrease 130 mins

40%

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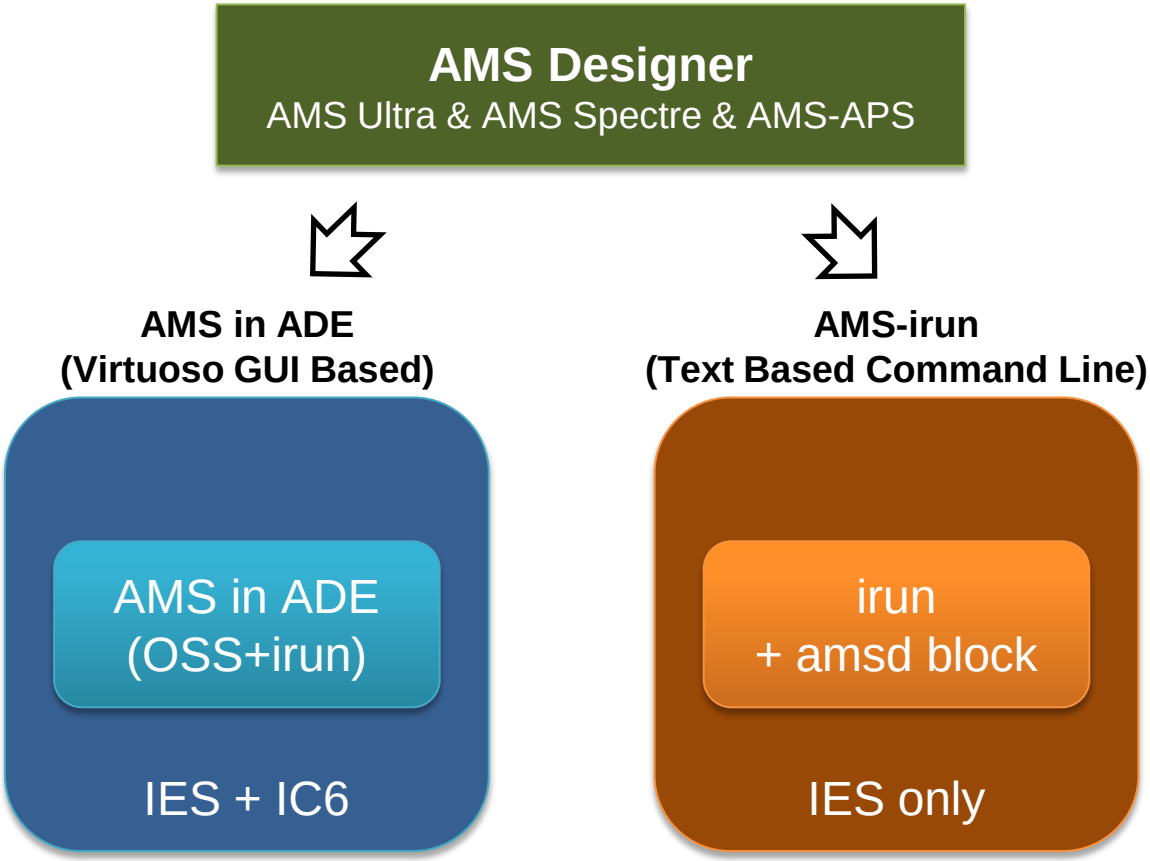
Implementation

Verification Methods

- What is the method for System-level AMS simulation?



Verification Flow in AVUM

IBIS Model

- IBIS File
- IBIS Pcell

Simulator

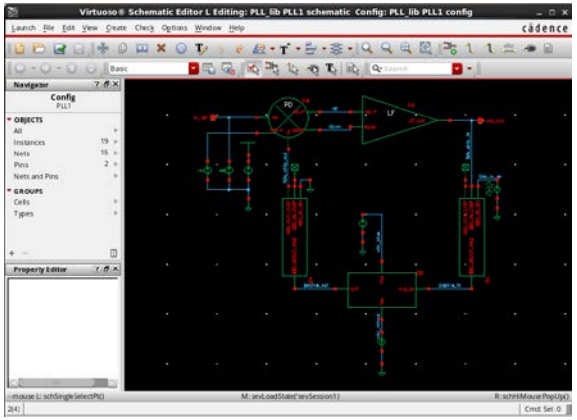
- Virtuoso AMSD

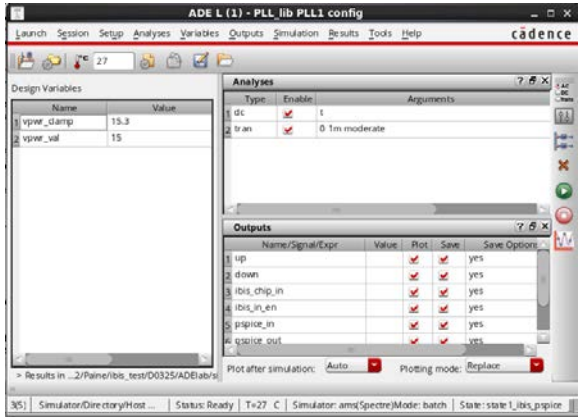
Virtuoso

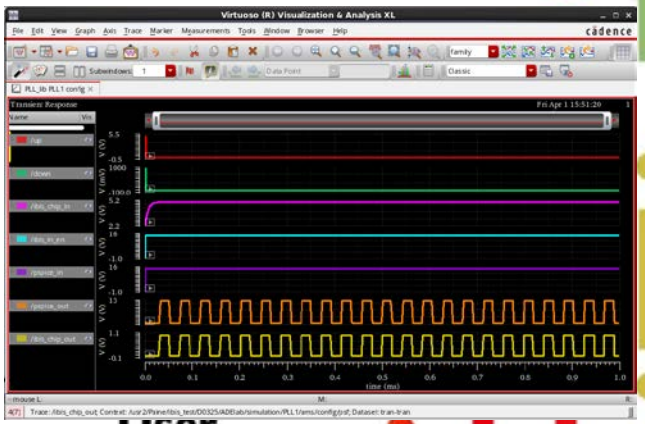
- Virtuoso SE
- HED
- ADE
- Virtuoso VA

Language

- Verilog
- Spice
- VerilogA
- PSpice
- VHDL
- VerilogAMS
- SystemVerilog

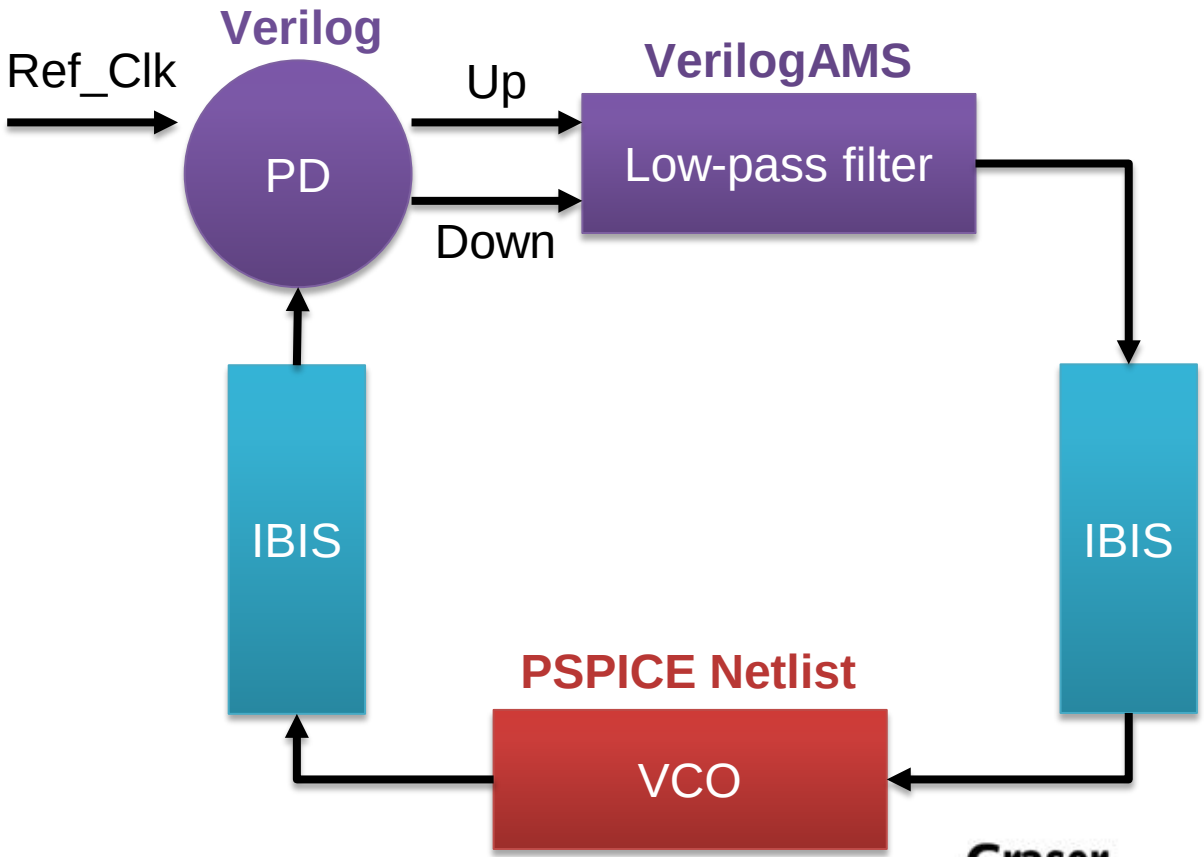




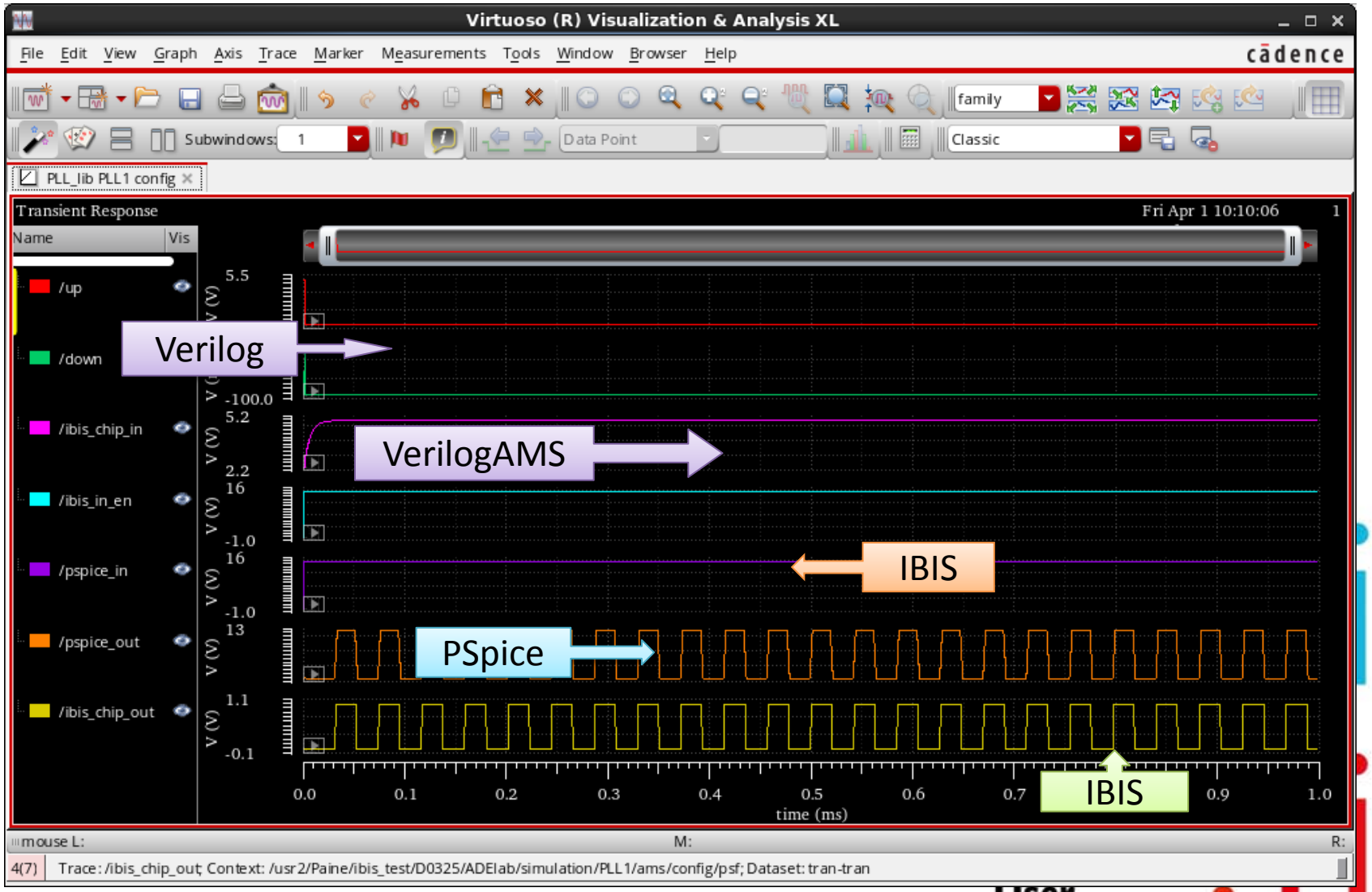


Verification Plan in AVUM

Virtuoso SE	HED	ADE	Virtuoso VA	IBIS Pcell	IBIS File
AMSD	Verilog	PSpice Netlist	VerilogAMS		



Verification Results in AVUM



Verification Flow in AIUM

Configuration

acf.scs

amscf.scs

Analog Simulator

Spectre

APS

IBIS Model

IBIS File

Digital Simulator

Incisive ES

SimVision

Language

Verilog

Spice

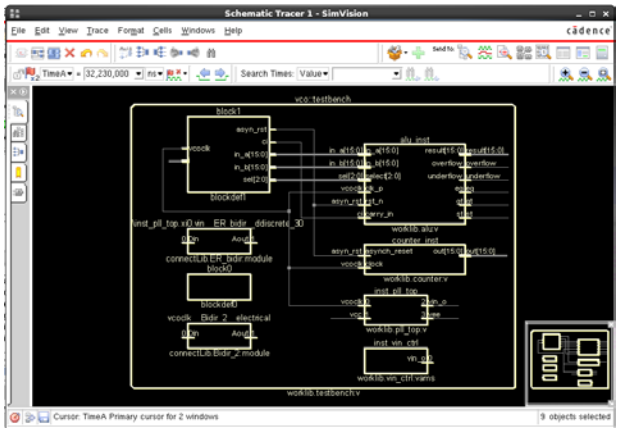
VerilogA

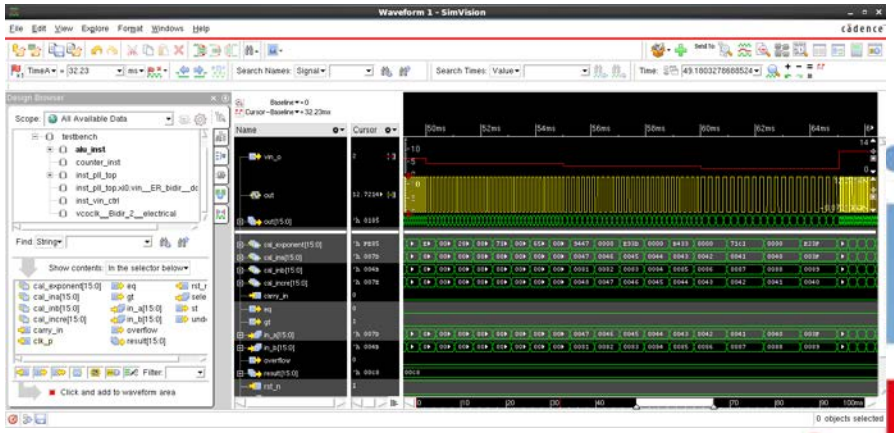
PSpice

VHDL

VerilogAMS

SystemVerilog





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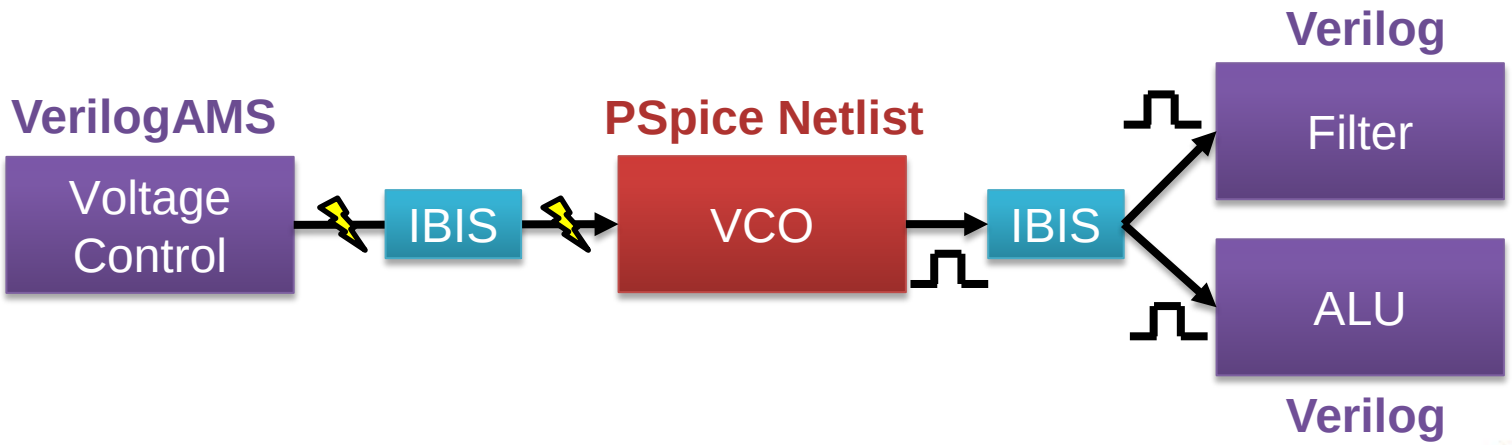
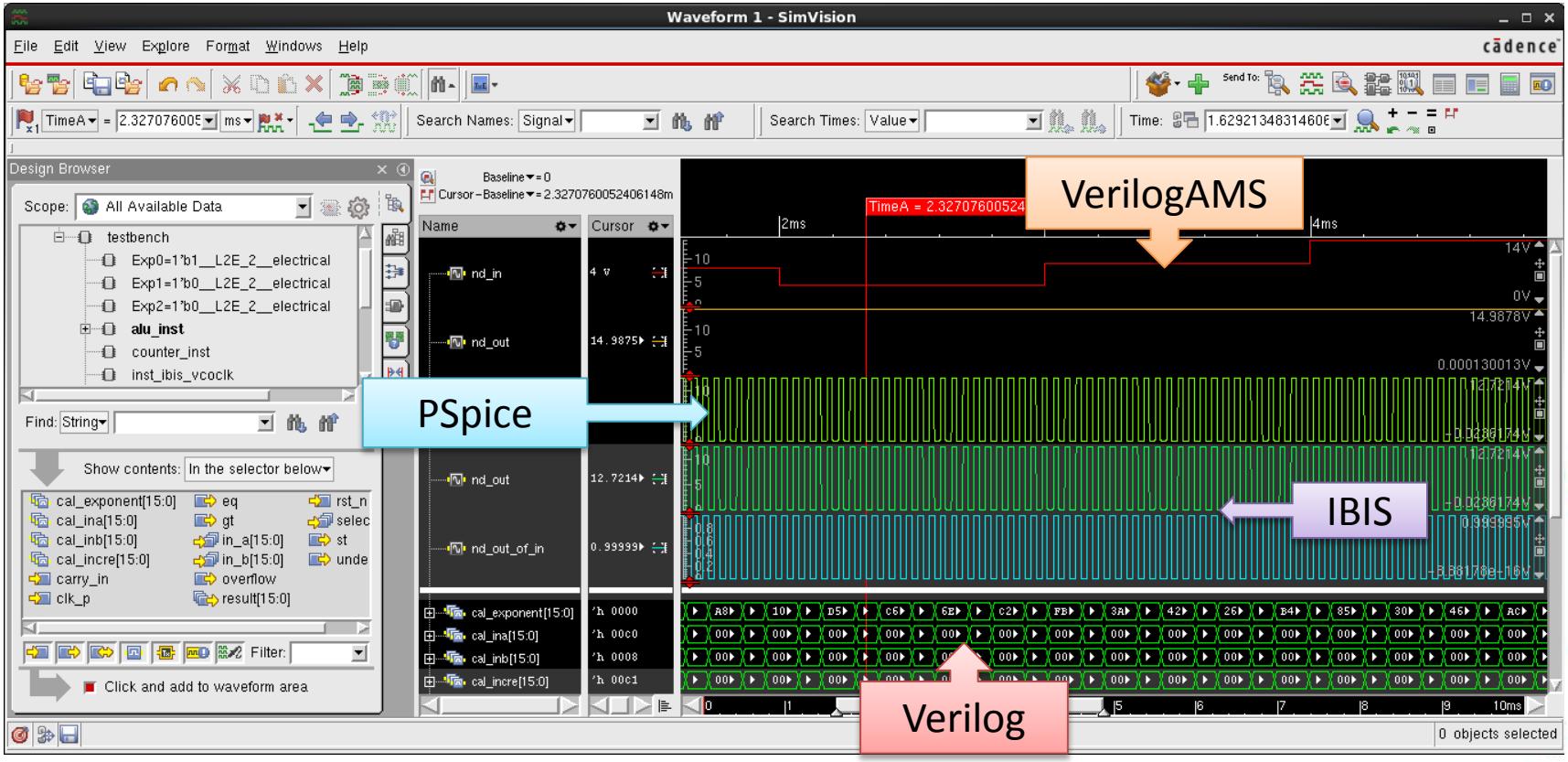
Verification Plan in AIUM

Incisive ES	acf.scs	amscf.scs	SimVision	Spectre	IBIS File
Verilog	VerilogAMS	PSpice Netlist	Spice		



Verification Results in AIUM



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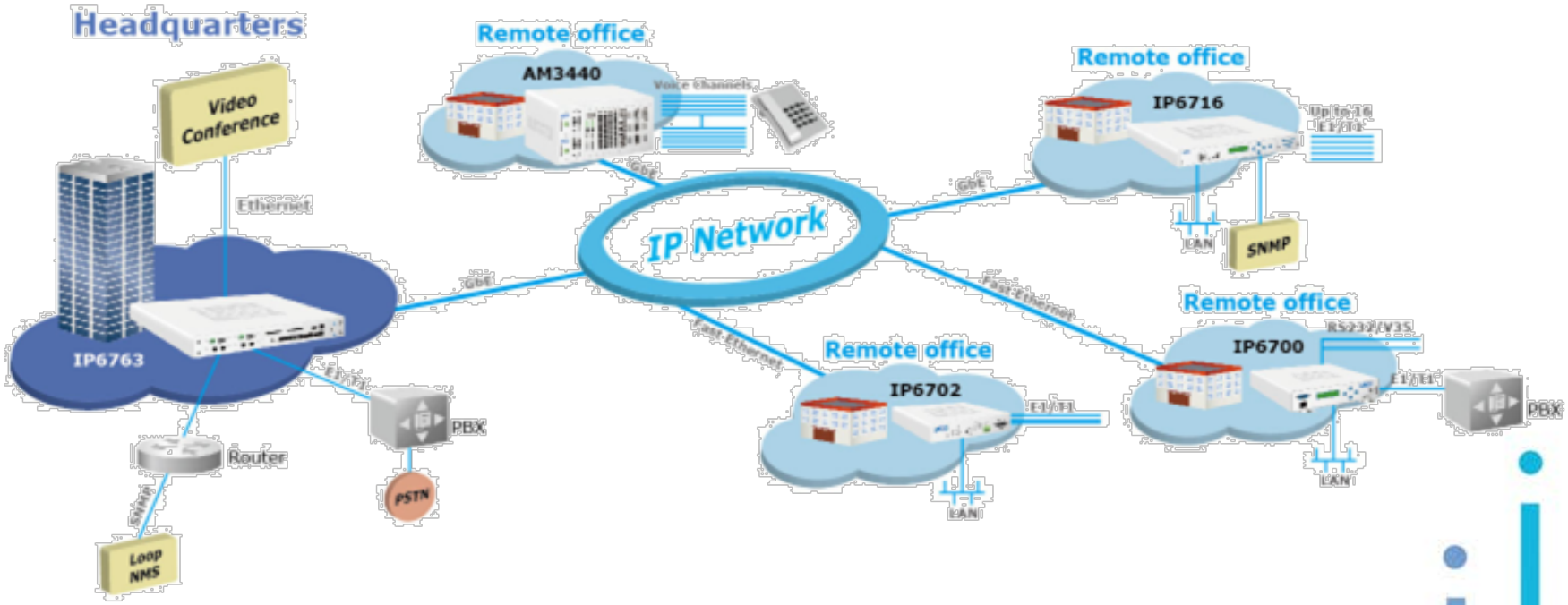
Successful Story

Application Field

- Network Application



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Application Field

- Video Application

Loop Telecom: Networking Devices for Transport, Switching, & Access

Application Focus: Video Surveillance

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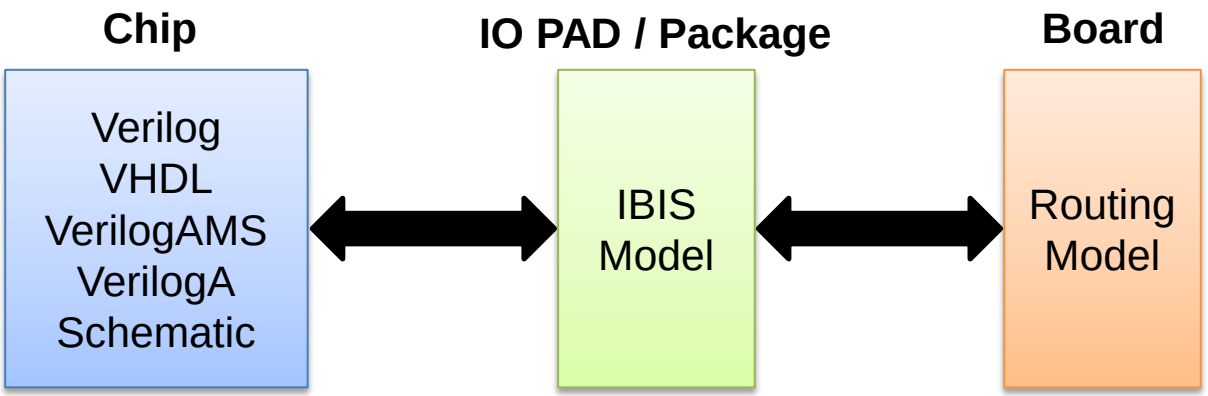
Summary

Summary

- Closely co-work between FPGA and PCB designer.
- Easily verify system design flow in AMS environment
- Reduce design cycle times and time-to-market



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Thank You!