

Getting Confidence  
in Your Design Early!

跨界整合 翻轉設計

# Graser User Conference

Taipei

2016  
7.14



# OrCAD PSpice 系統模擬驗證 與產業應用

Stacy Chen/ Graser

14 / July / 2016



# OrCAD PSpice System Solution and Industry Application

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- OrCAD® PSpice® Technologies
- OrCAD PSpice Virtual Prototyping Systems
- OrCAD PSpice Advanced Analysis
- Industry Application



# OrCAD PSpice Technologies



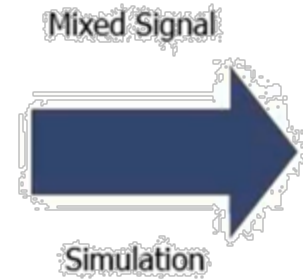
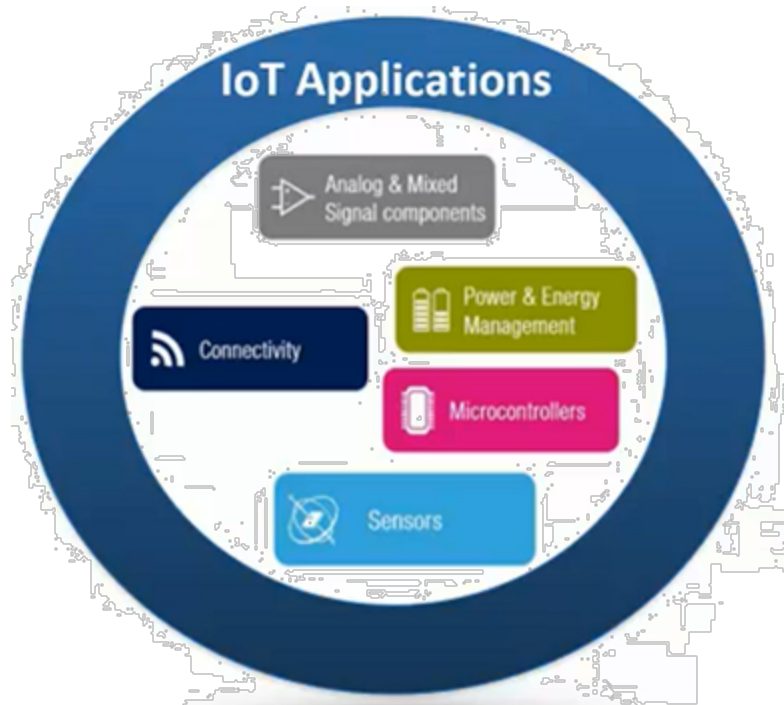
# Internet of Things

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# Internet of Things

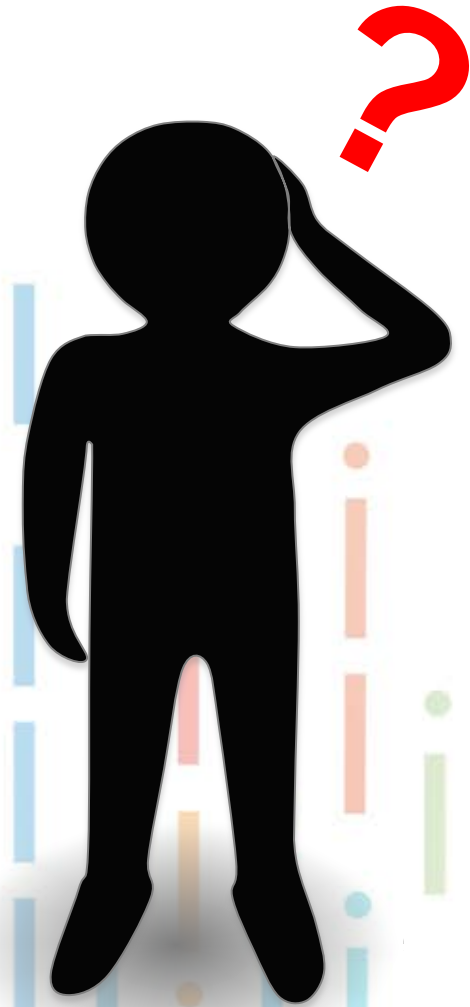
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IoT



# Challenges



Reduce errors

Increase reliability

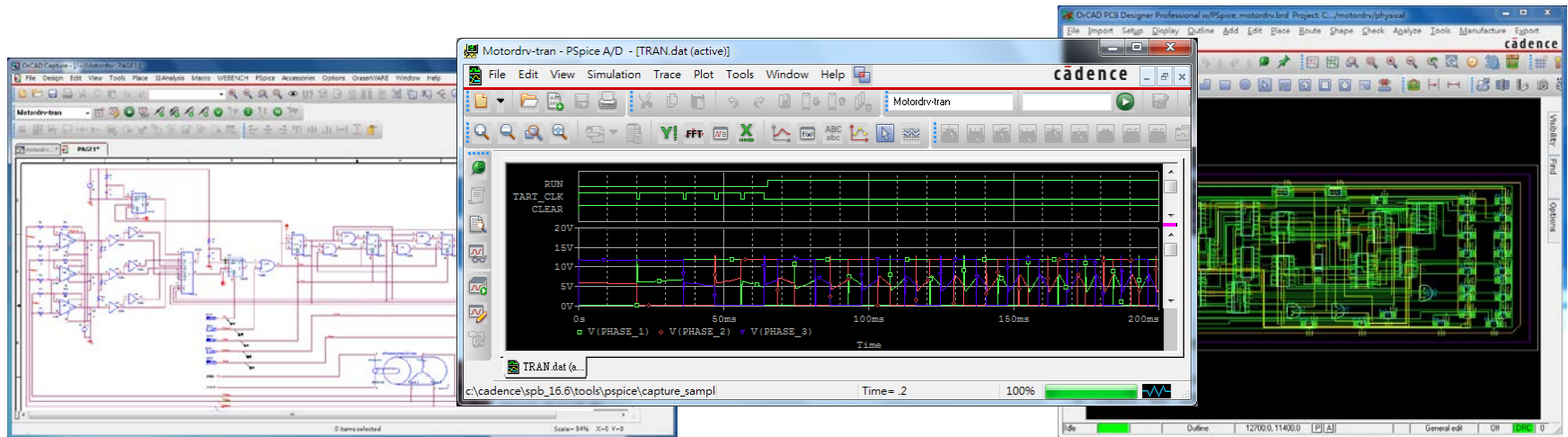
Model development

Increase Design Productivity



# OrCAD Design Solution

- Powerful and Widely Used Design Solution
  - Front-to-Back Integration
    - Fast and intuitive schematic design entry, OrCAD® Capture
    - **Mixed-signal simulator, OrCAD® PSpice®**
    - Comprehensive PCB solution, OrCAD® PCB Designer



Schematic  
OrCAD Capture



Simulation  
OrCAD PSpice



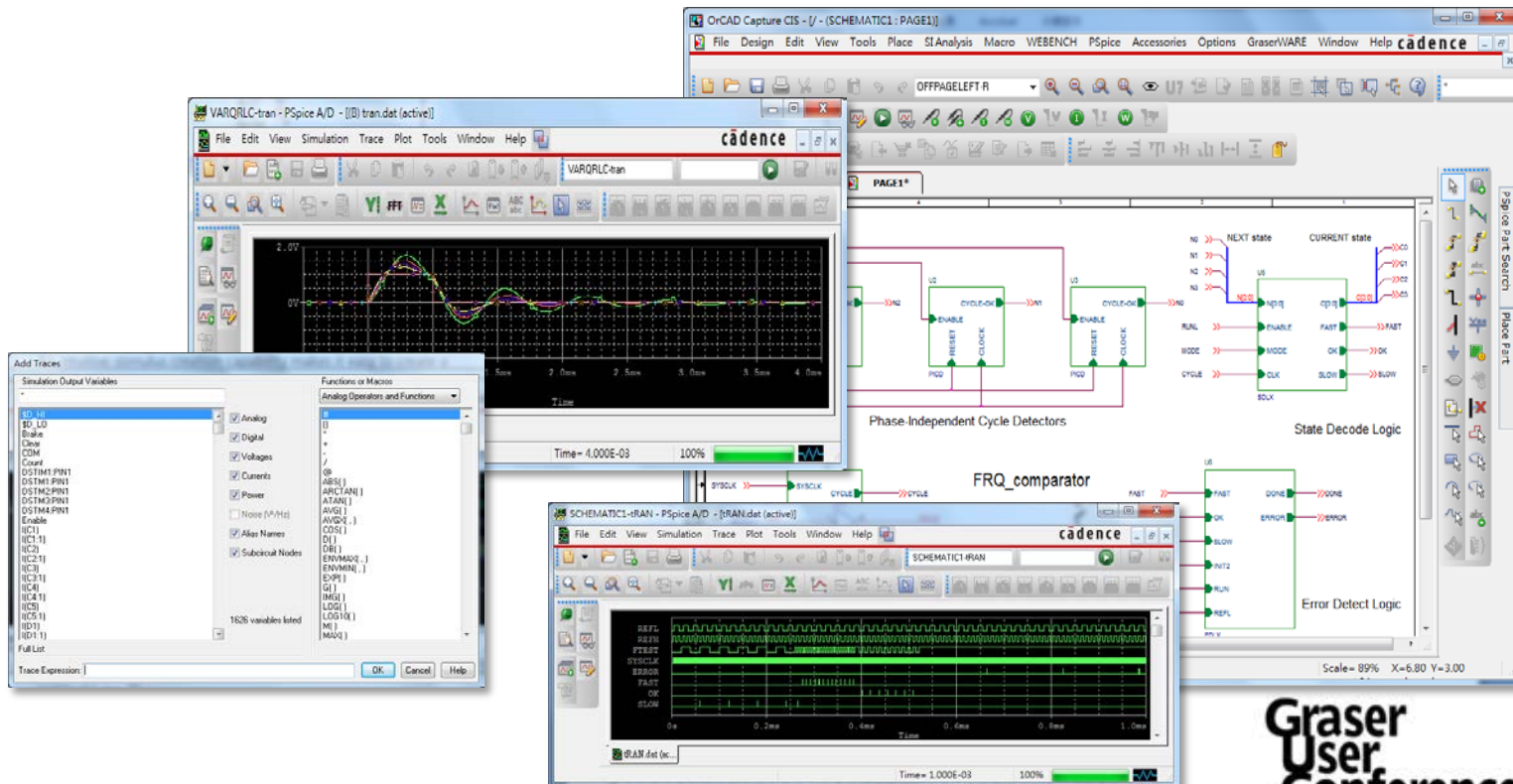
Layout  
OrCAD PCB Designer



# OrCAD PSpice

- Mixed-signal simulator

- Full integration with OrCAD® Capture improve productivity and data integrity.
- Powerful waveform viewing and post-processing expression support speed review and analysis without having to rerun simulations.



# OrCAD PSpice

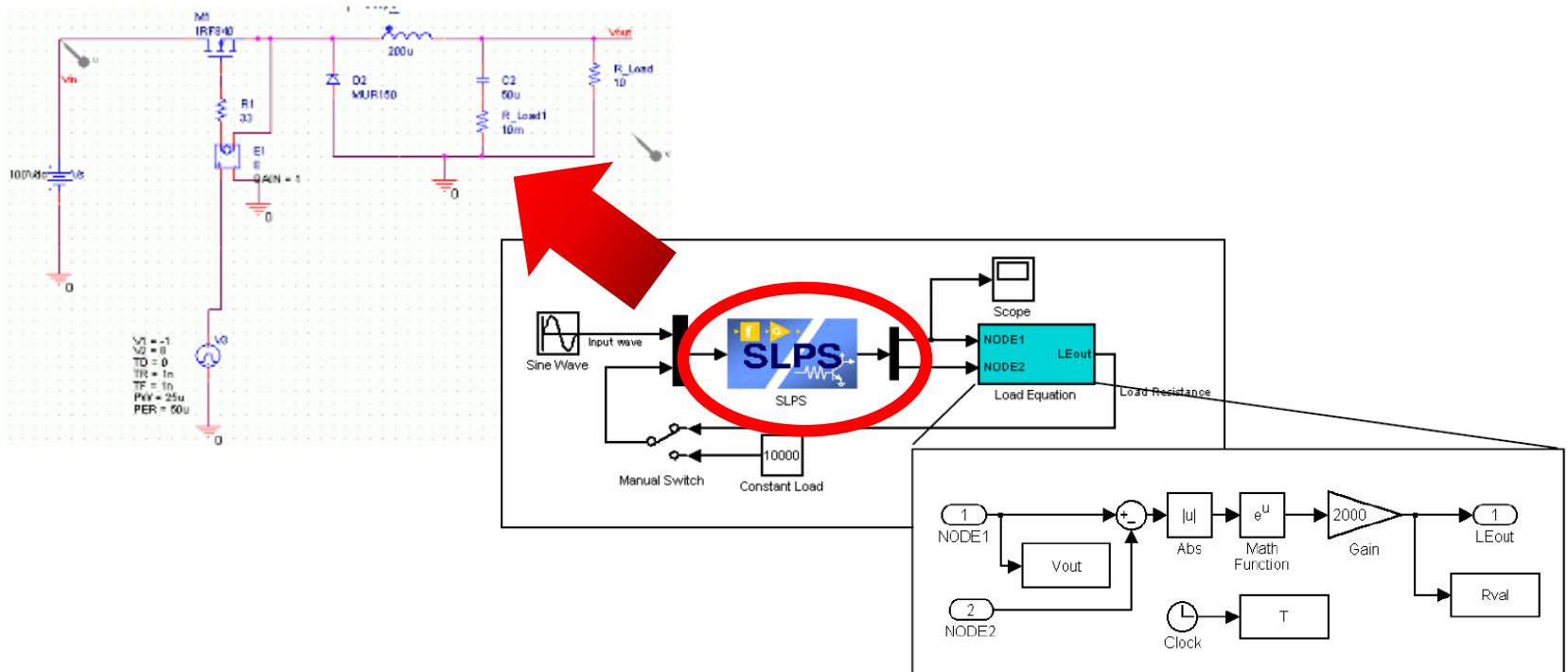
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- Mixed-signal simulator
  - Multi-vendor models, built-in mathematical functions, and behavioral modeling techniques.
  - Support multi-modeling type,
    - Algorithmic Models: Matlab/C/C++
    - System Models: SystemC
    - Digital Models with IO/Timing/Constraint
    - Digital Function Model
    - Verilog-A
    - PSpice® Behavioral Models

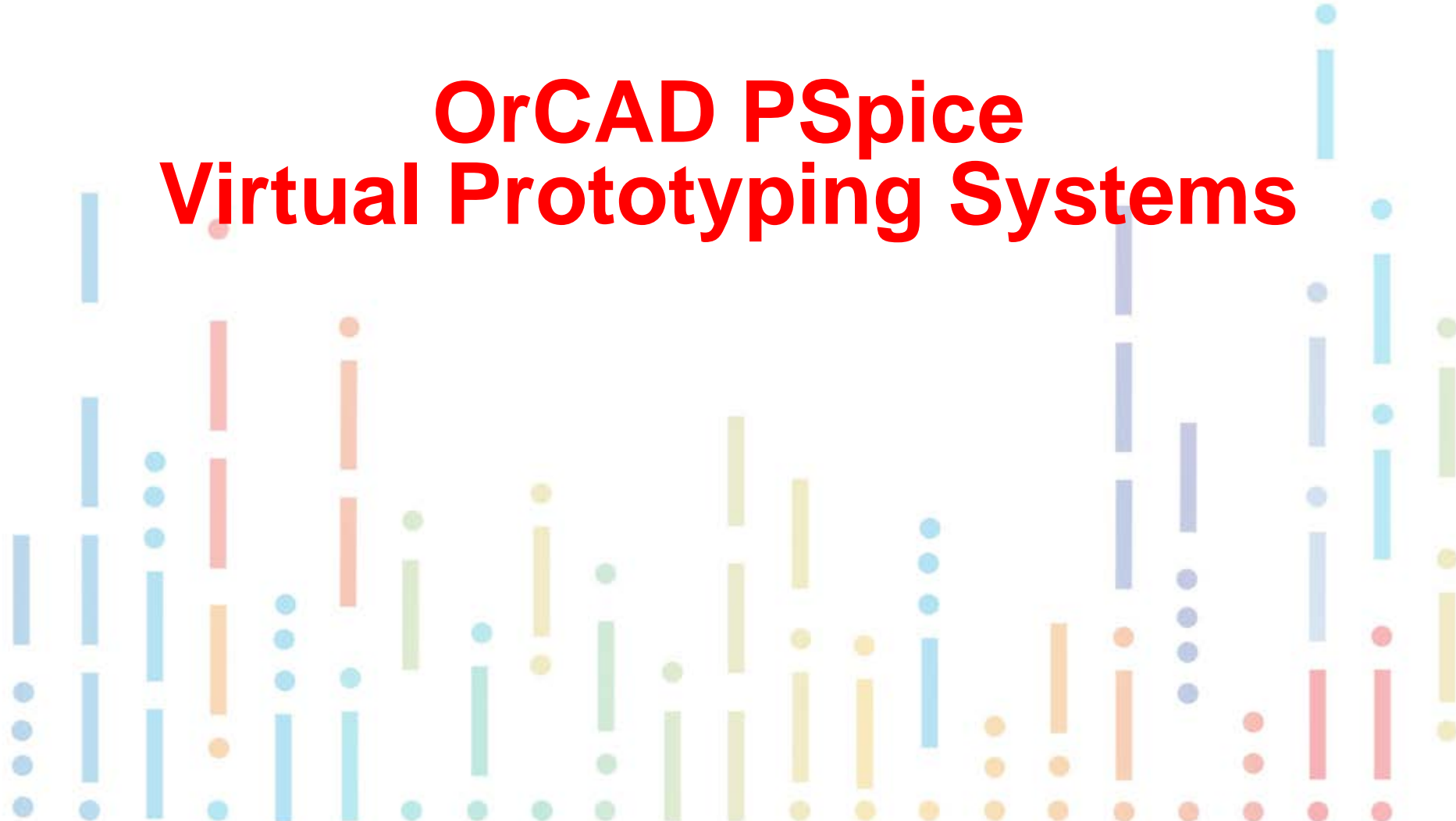


# OrCAD PSpice Mixed Domain Integration

- OrCAD® PSpice® w/ Matlab
  - Systems Simulation
  - Integration with MATLAB Simulink brings two industry-leading simulation tools, electromechanical systems & electrical, in a co-simulation environment.

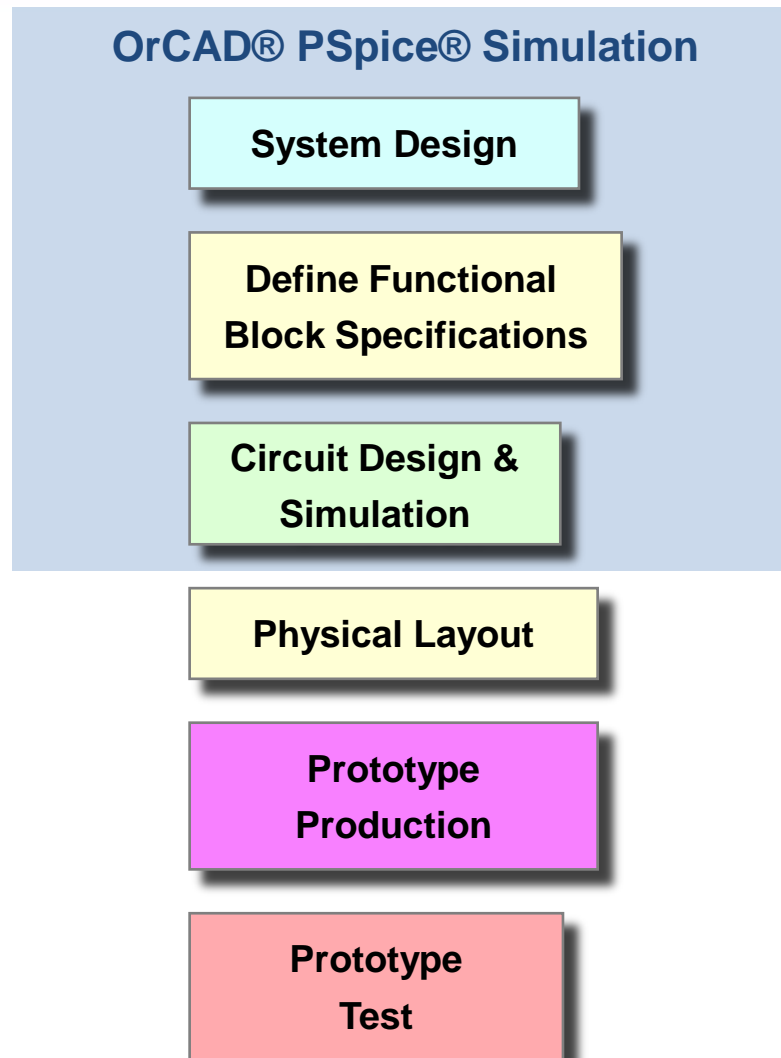


# OrCAD PSpice Virtual Prototyping Systems



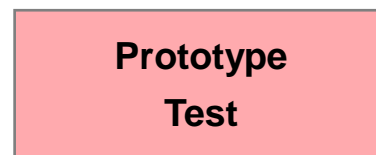
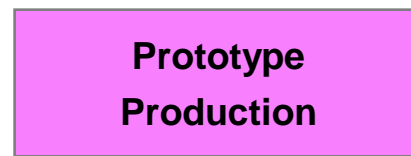
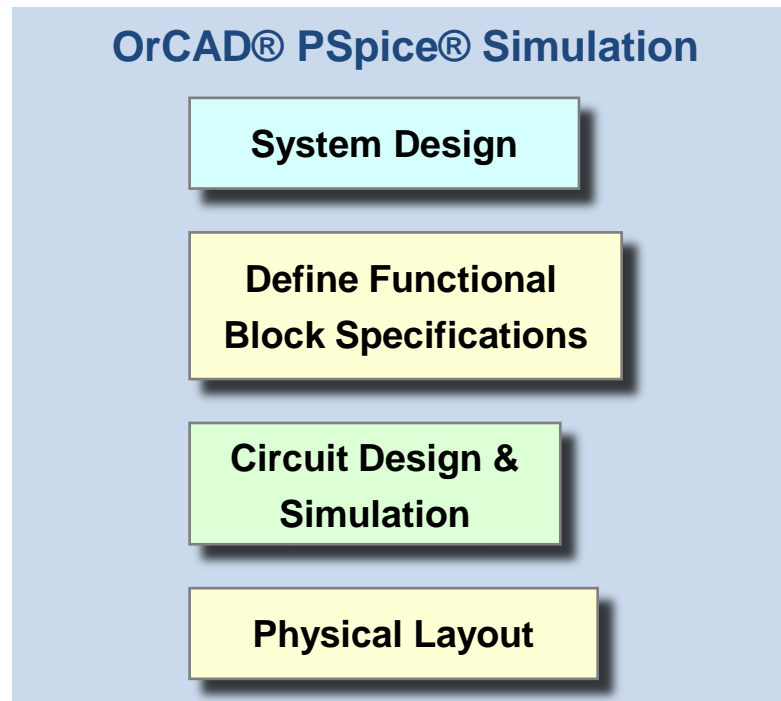
# OrCAD PSpice System Simulation Solution Flow

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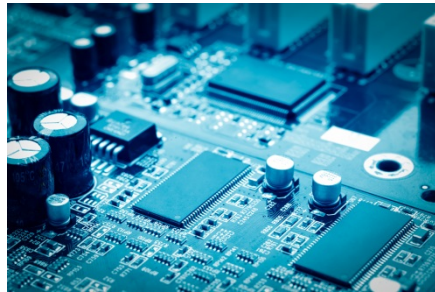


# OrCAD PSpice System Simulation Solution Flow

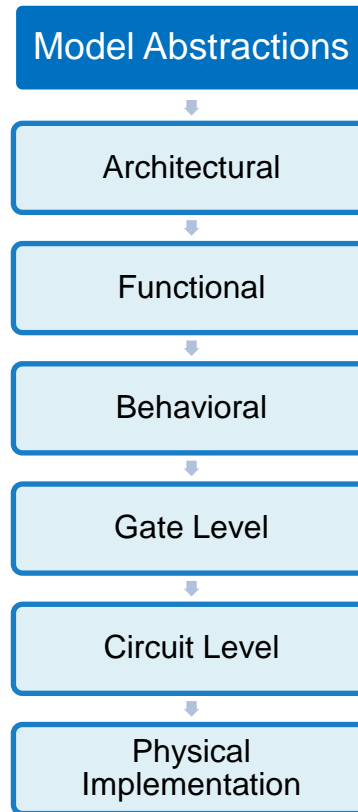
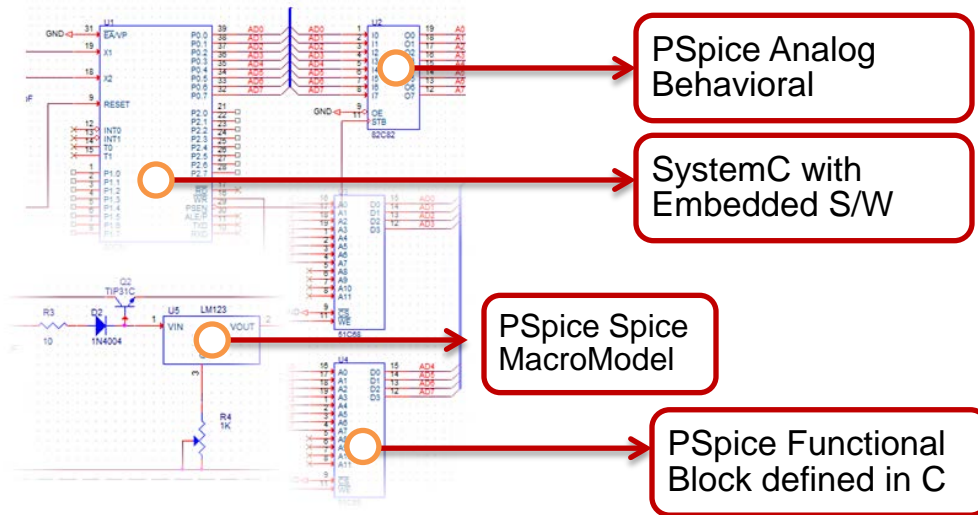
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# OrCAD PSpice Virtual Prototyping Systems



Components with different levels Abstraction Modeled in PSpice PCB simulation

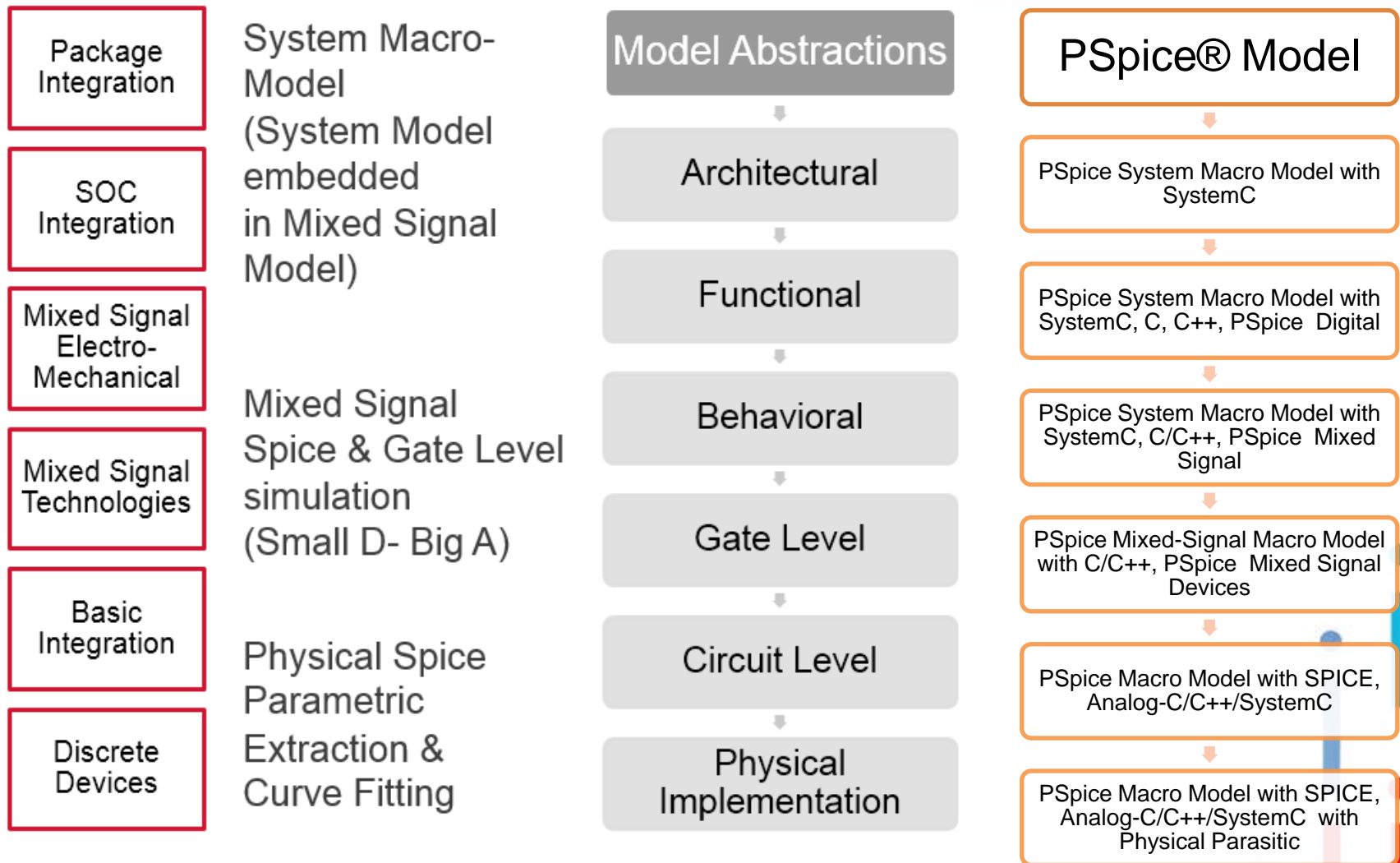


- **Multi-Level Block Abstractions**



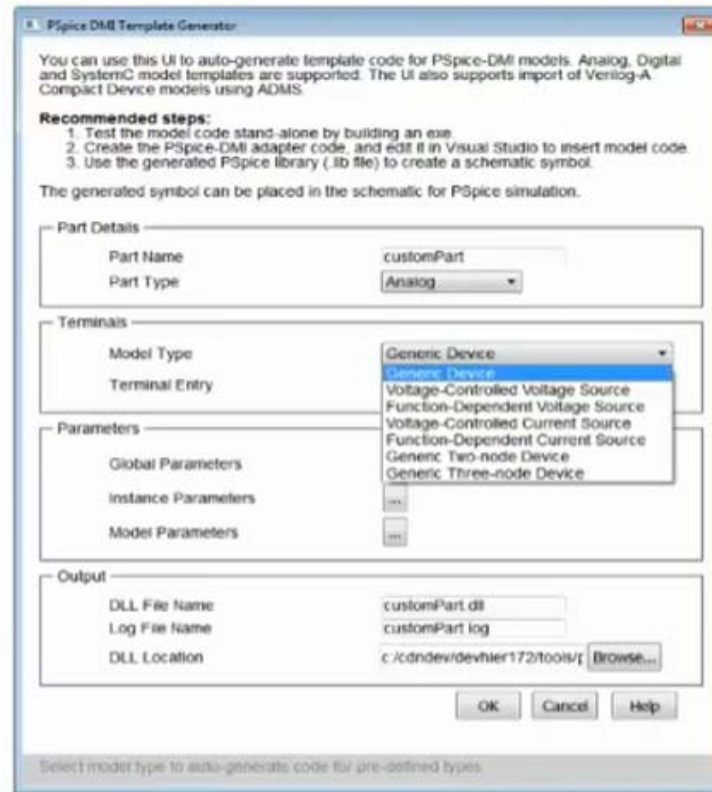
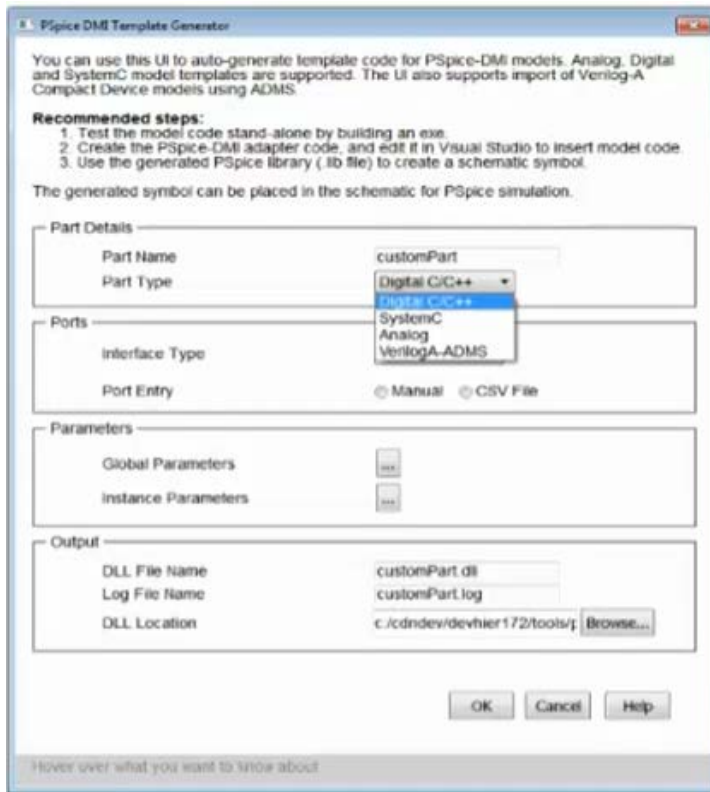


# OrCAD PSpice Virtual Prototyping Systems



# OrCAD PSpice Device Model Interface

- Generate PSpice® Adaptor code in PSpice Model Editor
  - Analog, Digital C/C++, SystemC and Verilog-A.



# OrCAD PSpice Simulation

- Create Model

PSpice® DMI

Microsoft Visual Studio Community 2013

Use this dialog-box to auto-generate DMI template code for the following PSpice-DMI models: Analog, Digital, and SystemC. The dialog-box also imports the Verilog-A Compact Device models using ADMS.

**Recommended steps:**

1. Test the model code stand-alone by building an exe.
2. Create the PSpice-DMI adapter code, and edit it in Visual Studio to insert model code.
3. Use the generated PSpice library (.lib file) to create a schematic symbol. The generated symbol can be placed in the schematic for PSpice simulation.

**Part Details**

Part Name: customPart  
Part Type: Digital C/C++

**Ports**

Interface Type: Port Entry

Port Entry: The csv file needs to follow the following syntax: <Port Name>, <Port Type: Input@O>, <Port Size>, <Initial Value>, <Port Description>. For example, IN1, INPUT, 1, X, Input Port 1 OUT, IO, 8, 0, IO Port 1

Global Paramet: IN1, INPUT, 1, X, Input Port 1  
Device Paramet: OUT, IO, 8, 0, IO Port 1

Select your CSV file here: D:\DMI\_Code\portv.csv

Port Name	Port Type	Port Size	Default Value	Port Description
CLK	INPUT	1	0	Clock
FB	INPUT	8	0	Feedback input
REF	INPUT	8	0	Reference input
PW	IO	1	0	Output Pulse Width

**Global Parameters**

Specify the global parameters which will be used by the device logic. These parameters need to be defined in the top-level schematic. DMI model will get their values from PSpice. Default value will be used to initialize the parameters in device constructor code.

Enter number of parameters: 2

Parameter Name	Parameter Type	Default Value	Parameter Description
PER	double	0	Period
D	double	0	Duty Cycle



```
REF[5]=pVectorStates[14].getLevel();
REF[6]=pVectorStates[15].getLevel();
REF[7]=pVectorStates[16].getLevel();
PW=pVectorStates[17].getLevel();

}

pspBits2Int(FB, FBInt, 8);
pspBits2Int(REF, REFInt, 8);
if (REFInt > FBInt && mD < 0.98) {
    mD += 0.001;
}
else if (REFInt < FBInt && mD > 0.02) {
    mD -= 0.01;
    fprintf(stderr, "Reducing DutyCycle\n");
}
if (mCurrentCLKCount <= 0) {
    mCurrentCLKCount = mPER;
}
if (mCurrentCLKCount > mD * mPER)
    mPWStatus = false;
else
    mPWStatus = true;

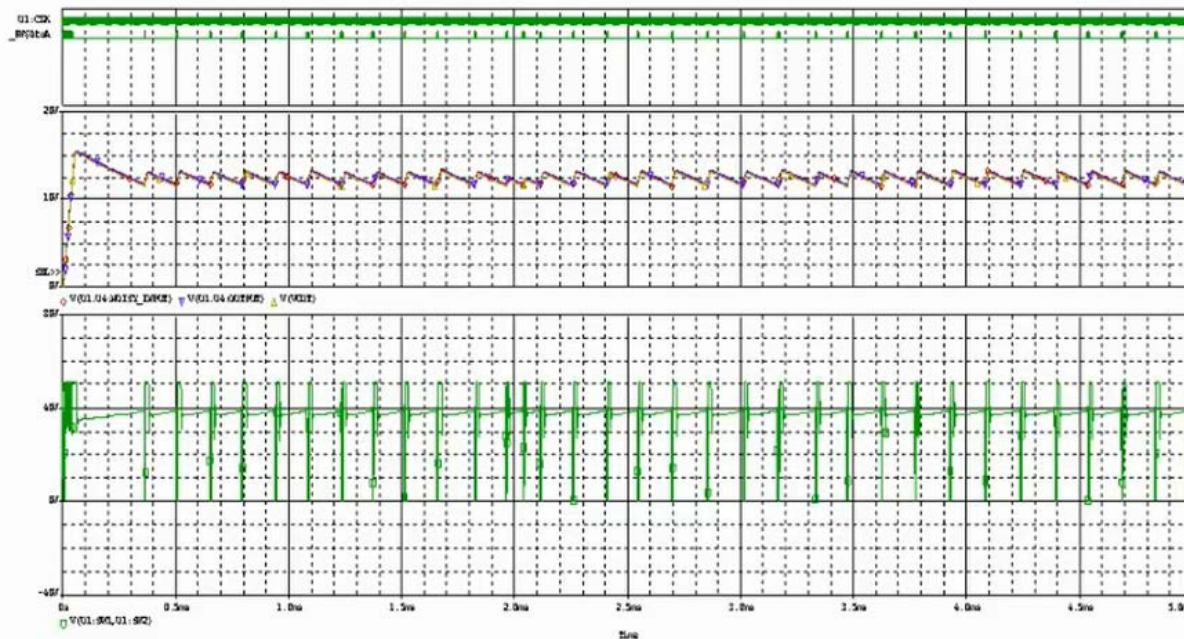
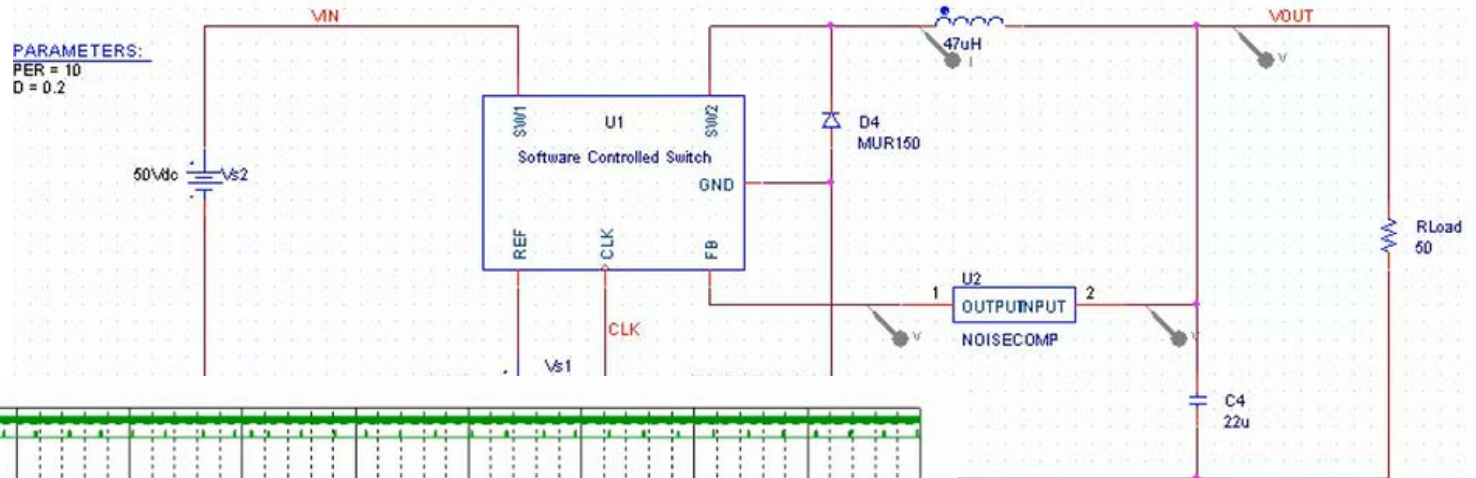
if (mPWStatus == true && (int)PW != 1){
    PW = pspBit::HI;
}
else if (mPWStatus == false && (int)PW != 0) {
    PW = pspBit::LO;
}

// LOGIC TO BE IMPLEMENTED BY USER
```

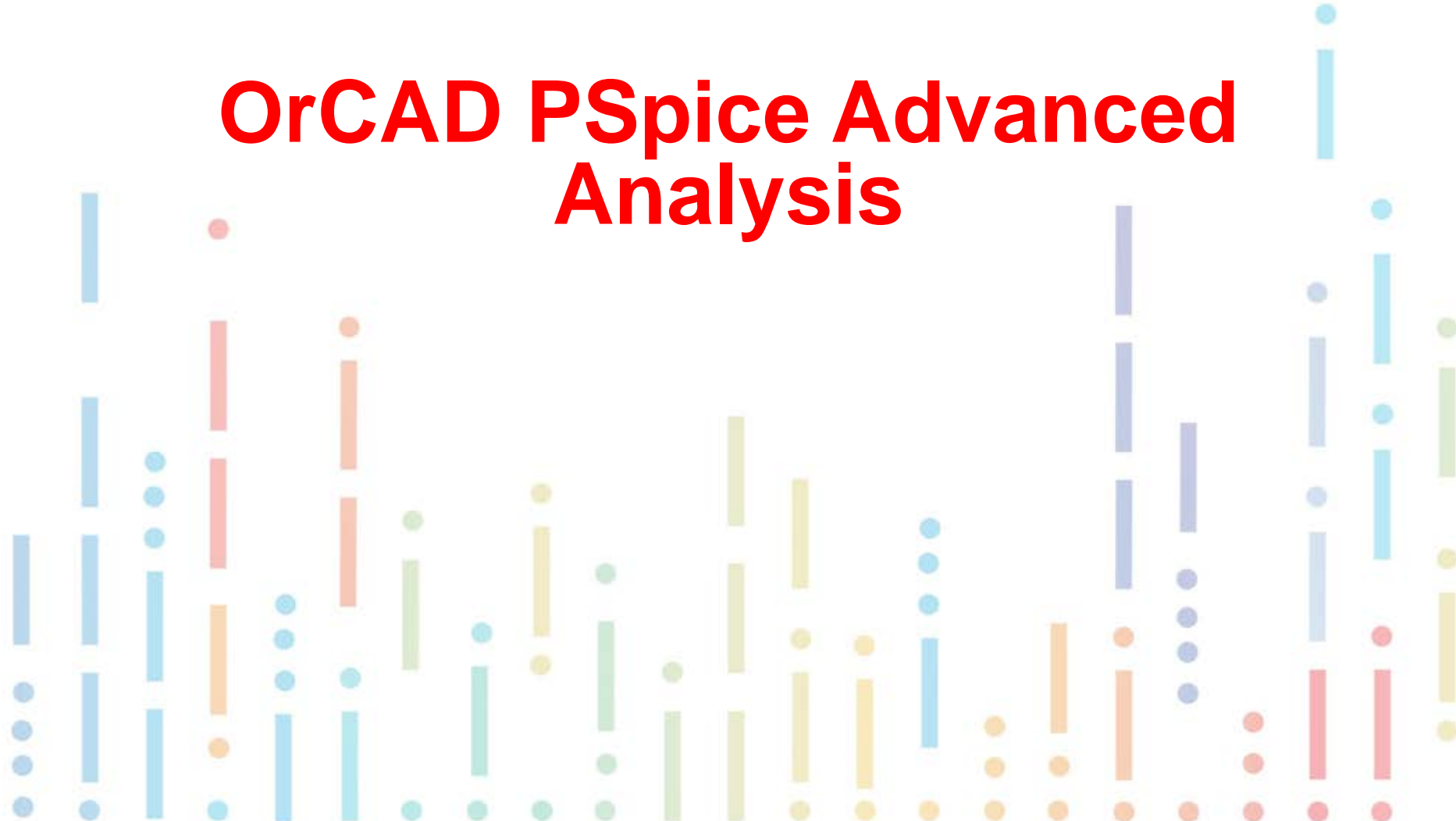


# OrCAD PSpice Simulation

- Result



# OrCAD PSpice Advanced Analysis





# Powerful Advanced Analysis

- Combine OrCAD® PSpice® A/D functionality with the powerful Advanced Analysis environment.

The image displays several screenshots from the Cadence Advanced Analysis software interface, illustrating its capabilities:

- Monte Carlo Analysis:** A screenshot titled "Probability Density Graph (Runs: 1 to 100)" shows a histogram of bandwidth values. Below the graph is a table of statistical information:
 

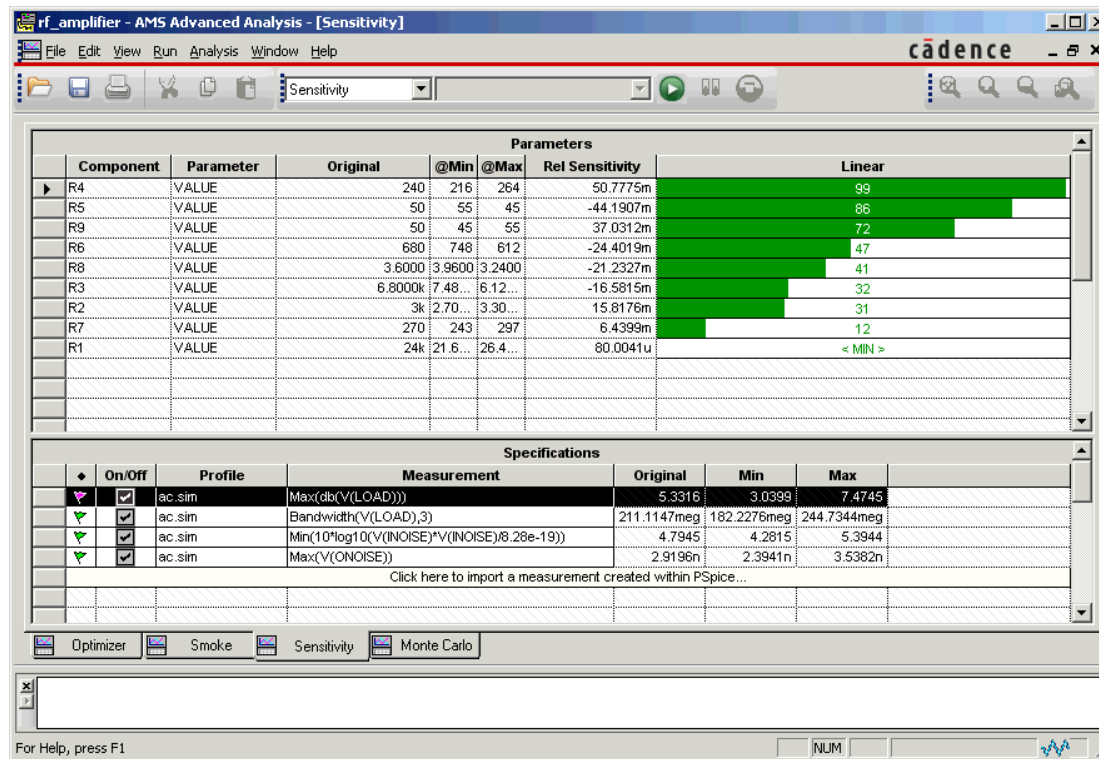
Measurement	Cursor Min	Cursor Max	Yield	Mean	Std Dev	3 Sigma
BW (LOAD)	9.306k	11.300k	100%	9.384k	425.314m	110k
Max(V(Load))	138.067mV	162.294mV	100%	150.675mV	4.7029mV	100%
Min(V(Load))	3.793n	4.596n	100%	4.152n	1.767151n	100%
Max(V(Noise))	3.8653n	4.7338n	100%	4.330n	201.3921p	100%
- Sensitivity Analysis:** A screenshot titled "Sensitivity" shows a table of parameters and their sensitivities:
 

Component	Parameter	Original	@Min	@Max	Rel Sensitivity	Linear
R4	VALUE	240	216	264	50.7775m	90
R5	VALUE	50	55	45	-44.1907m	90
R6	VALUE	50	45	55	37.6032m	72
R7	VALUE	680	748	612	-24.4013m	47
R8	VALUE	38000	36000	40000	-21.2305m	32
R3	VALUE	6.8000k	7.48	6.12	-15.5255m	41
R2	VALUE	3k	2.7	3.3	16.8175m	31
R1	VALUE	370	341	397	4.4338m	12
R11	VALUE	24	21.6	26.4	80.000Hz	<100%
- Error Graph:** A screenshot titled "Error Graph" shows a line graph of error percentage versus run number. Below the graph is a table of specifications:
 

On/Off	Profile	Measurement	Min	Max	Error
On	ac sim	Max(V(Load))	138.067mV	162.294mV	7.44%
On	ac sim	BW(Bandwidth(V(Load)))	9.306k	11.300k	21.147mV
On	ac sim	Min(V(Noise))	3.793n	4.596n	4.7945%
On	ac sim	Max(V(Noise))	3.8653n	4.7338n	2.9186%
- Transient Analysis:** A screenshot shows a transient analysis plot of current I(N) versus time. The plot shows a sharp peak followed by a decay. The time axis ranges from 0 to 300 ns.
- Parameter Tables:** Several screenshots show tables for parameters, discrete tables, and specifications, providing detailed data for various components and measurements.

# Sensitivity Analysis

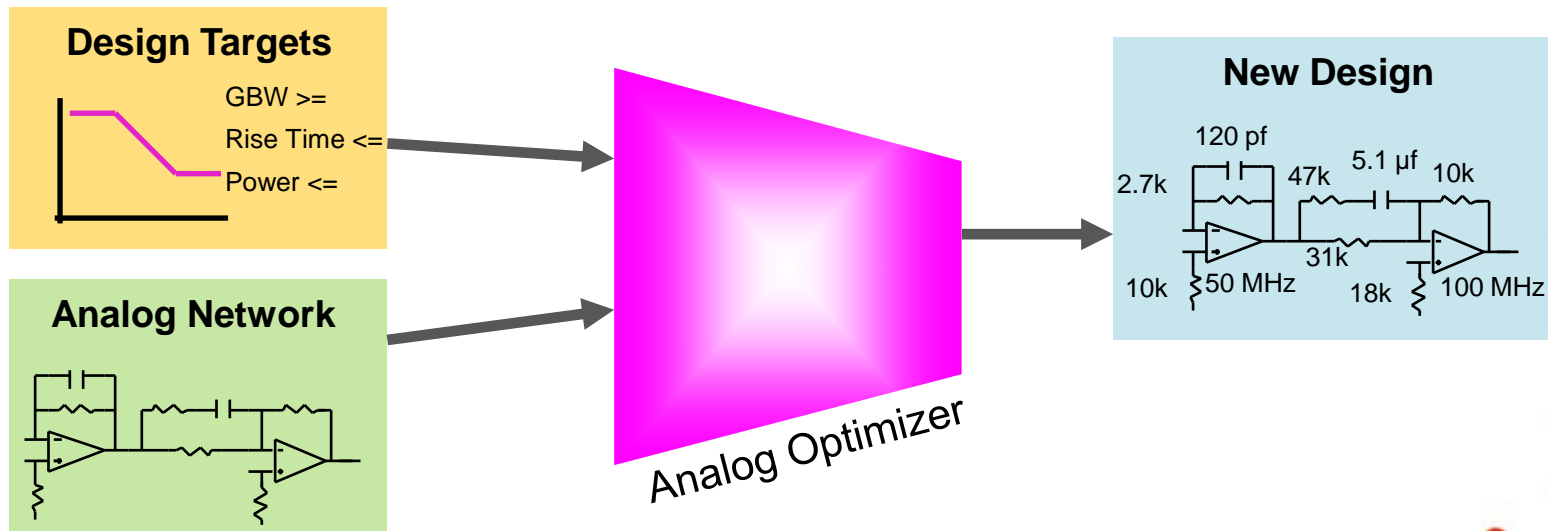
- **Easily identify** components impacting key circuit goals and specs.
- **Estimate worst case** performance of the circuit given the device tolerances.
- Identify components whose tolerance does not matter.
  - **Reduce cost** by choosing components with relaxed tolerance.





# Circuit Optimization

- Engineer specifies the Circuit Topology and the desired goals.
- **Optimizer does the rest.** It calculates the optimum component values to use to meet the desired goals.
  - One of the **most powerful** analysis tool.
  - Identify components impacting key circuit goals.
  - Identify designs goals and **optimize your design** to meet/beat these goals.
  - Design goals examples: Gain, BW, Overshoot, Pd, Ripple.
  - Design goals can be described as a waveform or Specification.



# Optimizer

- Finds optimum combination of component values; automatically simulates, evaluates results, and adjusts component values to reach performance requirements.
- Can be used to retarget an existing design at new goals.
  - To meet requirements of newer circuits.
  - To meet regional requirements.
- Saves time for engineers by taking over the often “mindless” task of final optimization
- Can optimize to a set of goal functions and/or a set of curves.



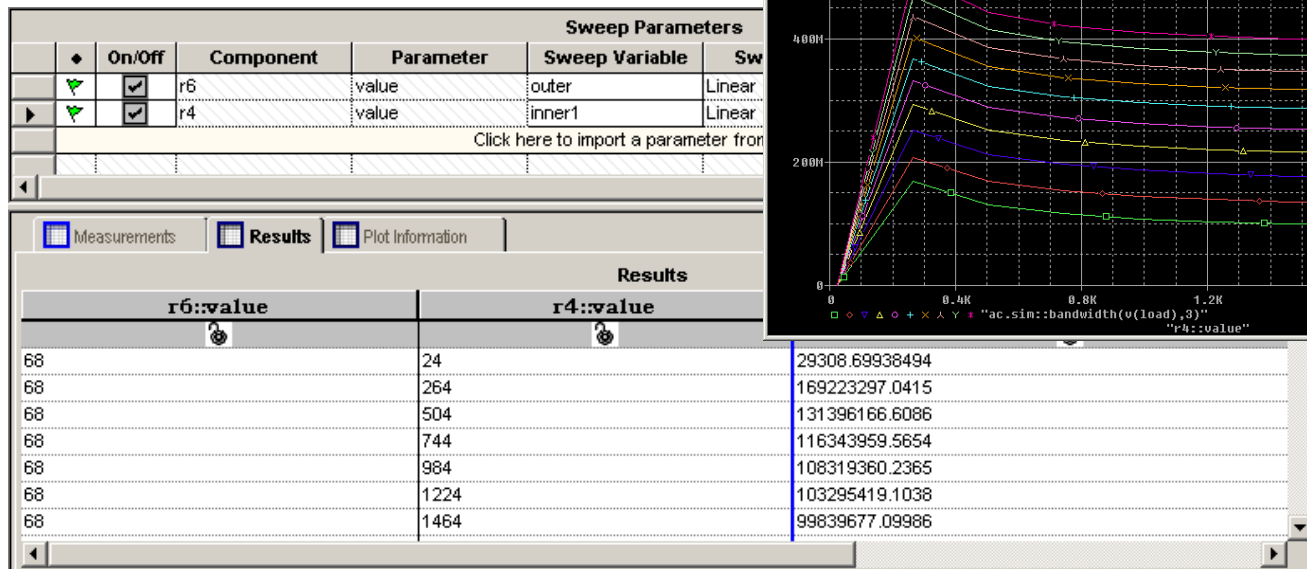
# Smoke

- Checks components to see if they are approaching or exceeding their recommended **safe operating limits**.
- Allows users to **specify their own derating criteria** to ensure components are not stressed, or exceed safe operating limits.
- **Determines a part's performance under various stresses** and environmental conditions.
- Helps in **thermal design** aspect of electronics circuit.
- Calculate **Peak, Avg.** and **RMS** power.
- **Cross-probe** to automatically find listed parts in the **schematic**.

Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Values	% Max
XG1	VCE	Average	12	50	6	8.1262	136
XG1	VCE	Peak	12	50	6	8.1422	136
XG1	VCE	RMS	12	50	6	8.1202	136
XG1	PCM	Average	197.7143m	75	148.2857m	77.7422m	39
XG1	PCM	Peak	197.7143m	75	148.2857m	74.7285m	38
XG1	PCM	RMS	197.7143m	75	148.2857m	74.7607m	38
XG1	TJ	Average	200	100	200	95.0288	48
XG1	TJ	Peak	200	100	200	92.3892	47
XG1	TJ	RMS	200	100	200	92.4156	47
RB	PCM	Average	250m	38	96.688m	40.4885m	42
RB	PCM	Peak	250m	38	96.688m	40.4885m	42
RB	PCM	RMS	250m	38	96.688m	40.4885m	42
XG2	VCE	Average	40	50	20	7.6077	39
XG2	VCE	Peak	40	50	20	7.6077	39
XG2	VCE	RMS	40	50	20	7.6077	39
XG1	VCB	Average	20	100	20	7.3391	37
XG1	VCB	Peak	20	100	20	7.3568	37
XG1	VCB	RMS	20	100	20	7.3392	37
XG1	VCB	Average	25000	100	25000	767.0403m	31
RB	TB	Average	200	100	200	59.3500	30
RB	TB	Peak	200	100	200	59.3500	30
RB	TB	RMS	200	100	200	59.3988	30
XG1	IC	Average	50m	80	40m	9.5771m	24
C4	CV	Average	50	90	45	10.6377	24
C4	CV	Peak	50	90	45	10.6377	24
C4	CV	RMS	50	90	45	10.6377	24
XG1	IC	Average	50m	80	40m	9.1877m	23
XG1	IC	RMS	50m	80	40m	9.1918m	23

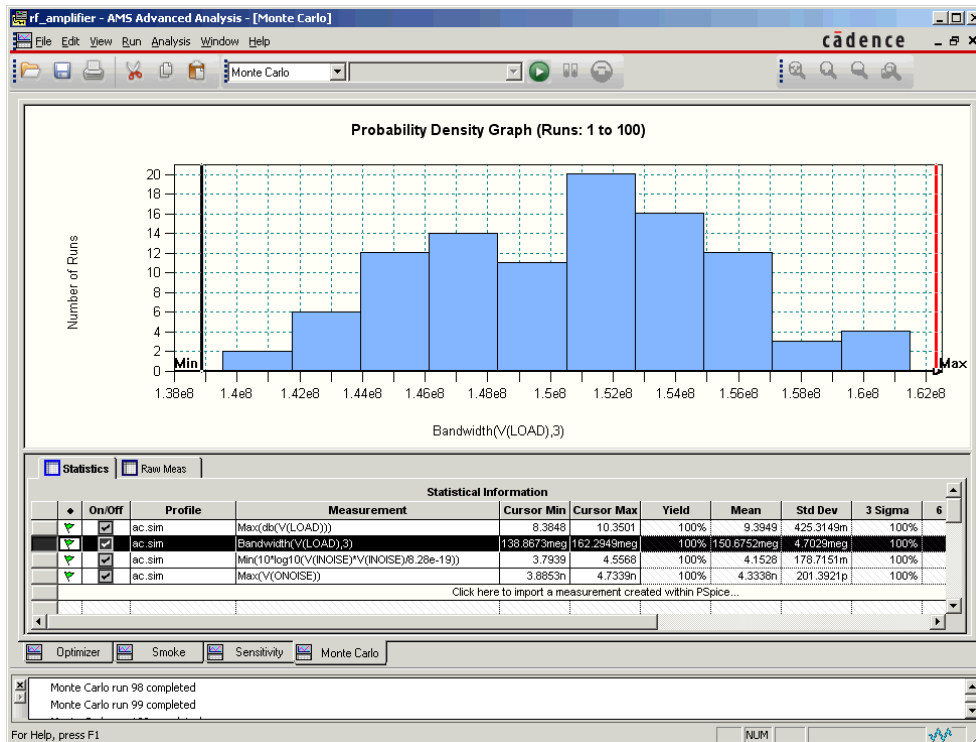
# Parametric

- **Sweep** multiple (nested) parameters.
- Quickly view results and create families of curves.
- **Ensure** there is **no unusual circuit behavior** while sweeping the component values.



# Monte Carlo

- Calculate Yield before going into manufacturing.
- Produce circuit performance statistics due to device variations.
- Set specification minimum and maximum, and estimate production yield before going to production.
- View graphical results as probability density histogram, or as cumulative distribution function.

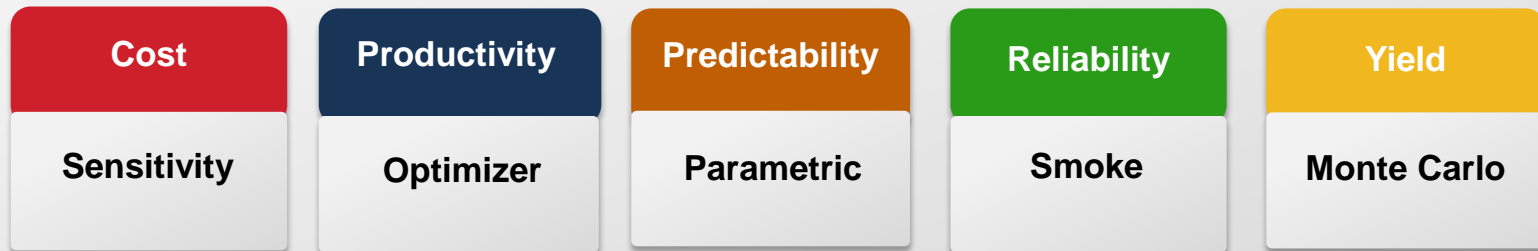


# OrCAD PSpice Advanced Analysis

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- Help customers optimize their design while maintaining their cost and yield.

## OrCAD® PSpice® Advanced Analysis



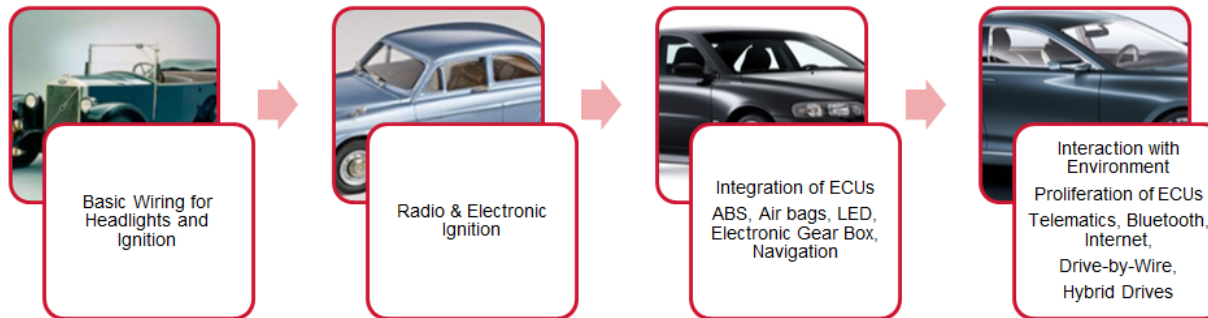
# Industry Application





# Automotive

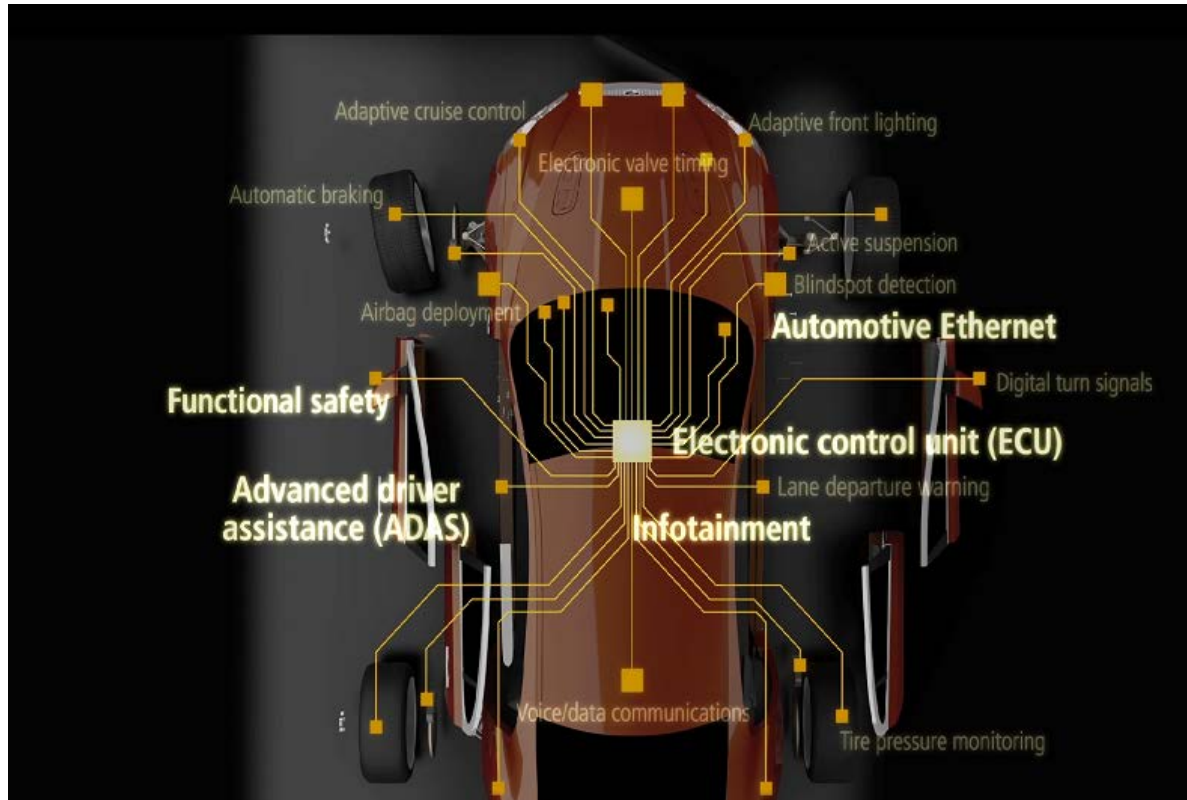
- Automotive Engineering Design Challenges



- Systems Modeling
- ECU Logic Authoring
- Power Electronics
- Multi-Domain Mixed Signal Control Systems
- Sensors
- Network Enabled
- Embedded Software

# Automotive

- Automotive Engineering Design Challenges



- Systems Modeling
- ECU Logic Authoring
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- Multi-Domain Mixed Signal Control Systems
- Sensors
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# Automotive

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- **Customer Key Challenges**
  - Evaluate electronic interfaces for compatibility and robustness against various automotive conditions.
  - Identify and fix problem before Hardware Freeze.
- **Adopt OrCAD® PSpice® Solution**
  - OrCAD PSpice
  - OrCAD PSpice Advanced Analysis
  - OrCAD PSpice SLPS



# Automotive

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- OrCAD® PSpice® Technology
  - Steady State Analysis
  - Transient Analysis
  - System Analysis/Subsystem Analysis
  - Simulate to identify below Failures
    - Short to battery
    - Short to ground
    - Jump start
    - Ground shift conditions
    - Reverse Battery condition
  - Worst Case Analysis
  - Monte Carlo Analysis
  - DC Sweep, Parametric Sweep, Temperature Sweep
  - Smoke Analysis



# Automotive

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- Results

- Quickly identified stress on electronics components at different conditions.
- Evaluated Power dissipation.
- Simulated ECU subsystem with other automotive electronic subsystems.
- Detected supplier design problems and vehicle interface error earlier on.
  - Saving time and money.
- Met the rigorous quality and reliability standards.



# Power Electronics



# Power Electronics

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- **Customer Key Challenges**

- High power = hard to characterize accurately in the lab.
- Requires special models for transformer(nonlinear magnetic), power semiconductors.
- Component stress.
- Power electronics designers that need PCB routing effects included in their simulation.

- **Adopt Cadence® Solution**

- OrCAD® PSpice®
- OrCAD PSpice Advanced Analysis
- Cadence® Sigrity™ solution





# Power Electronics

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## Cadence Solution

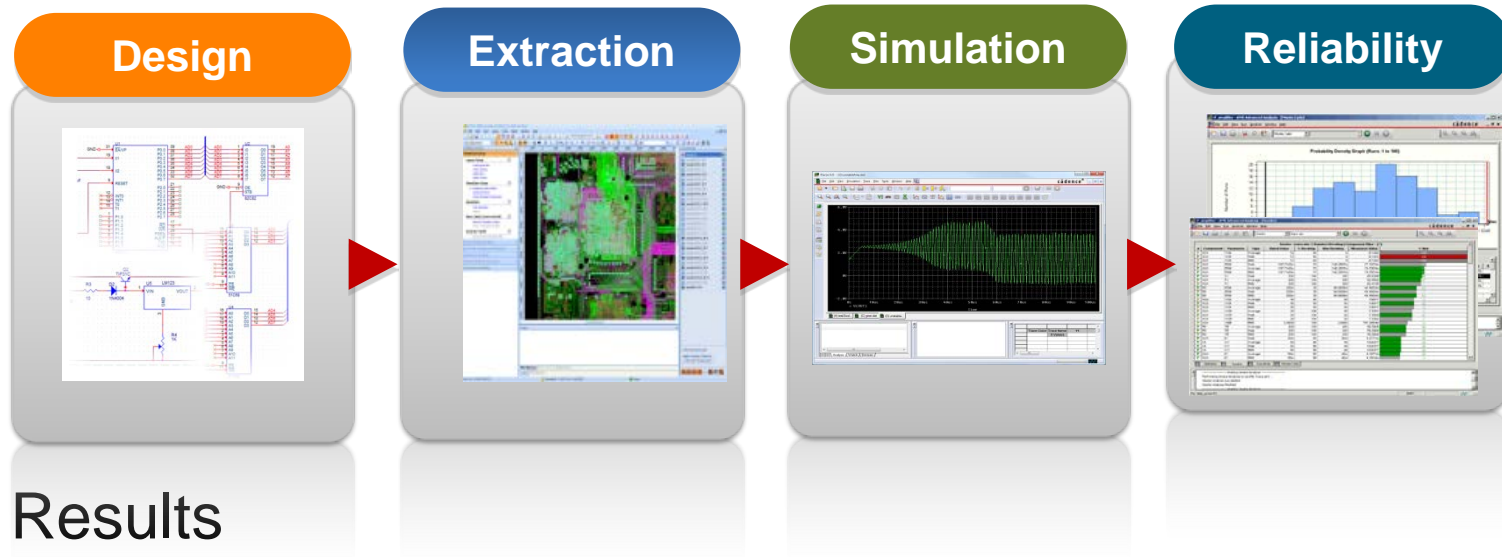
- **OrCAD® PSpice® Technology**
  - Allows mixed-signal simulation and system level analysis capabilities across different levels of abstraction.
  - Core loss calculator.
  - Ease of access to Industry's most comprehensive set of accurate data from manufacturers, which are included in more than 33,000 simulation-ready PSpice models.
  - PSpice Modeling Apps for Voltage Controlled Oscillators (VCOs), Piece-Wise Linear Sources (PWLs), PWMs, Transformers and several others simplify modeling
  - Smoke Analysis.
  - Monte Carlo Analysis
- **Cadence® Sigrity™ Technology**
  - Extract PCB routing effects.
    - Power electronics designers can simulate early validating design requirements are met.



# Power Electronics

- Cadence® Solution

- OrCAD® PSpice® and Cadence® Sigrity™



- Results

- OrCAD PSpice verifies component stress.
- Meet Time To Market targets.
  - Faster development process.
  - OrCAD PSpice delivers accurate results enabled First-Time-Right Design.

# System Simulation Solution

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- Summary

- **Increase Design Productivity** by automating the design process using the PSpice Optimizer. Produce more optimized circuits than humans.
- **Reduce errors** from re-entering the schematics when going from schematic to layout.
- **Increase reliability** of the design by using the advanced analyses package. Reduce the number of costly Field Failures.
- Excellent **Model development** capability Large analog/mixed level components in standard library.



**Thank You**

