ERC and SRC Applications In Practical PCB Design Process

Cliff Lin

2016/07/06

ADLINK

Building Forward Together

Abstract

- **Overview**
- ERC (Electrical Rule Check)
- SRC (Simulation Rule Check)
- Applications
- Summary

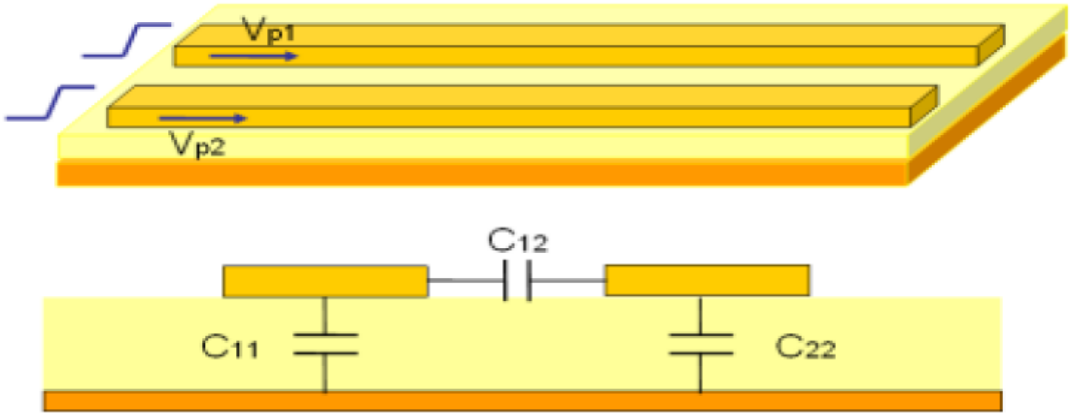
Overview

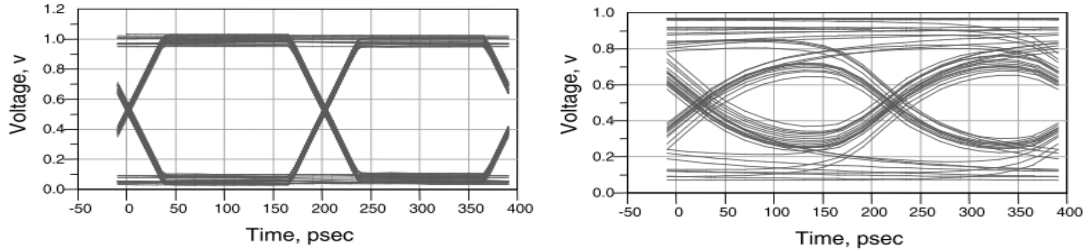
- No models required : easy to run by PCB layout designers
- Detects impedance discontinuities of routed PCB signals
- Detects excessive coupling between routed PCB signals
- Integrated with OrCAD PCB Designer for easy modification of problem signals

Theoretical Background

ERC

Coupling is defined with **Near-ended Crosstalk** as a victim.





Eye diagrams of a 5-Gbps pseudorandom bit stream. Left: little loss. Right: same bit pattern when there is a lot of loss, showing the collapse of the eye diagram, and increased jitter, indicated by the widening of the cross-over regions.

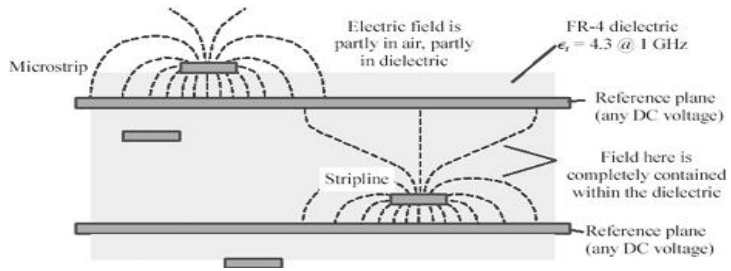
1. Radiative loss
2. Coupling to adjacent traces
3. Impedance mismatches ★
4. Conductor loss
5. Dielectric loss

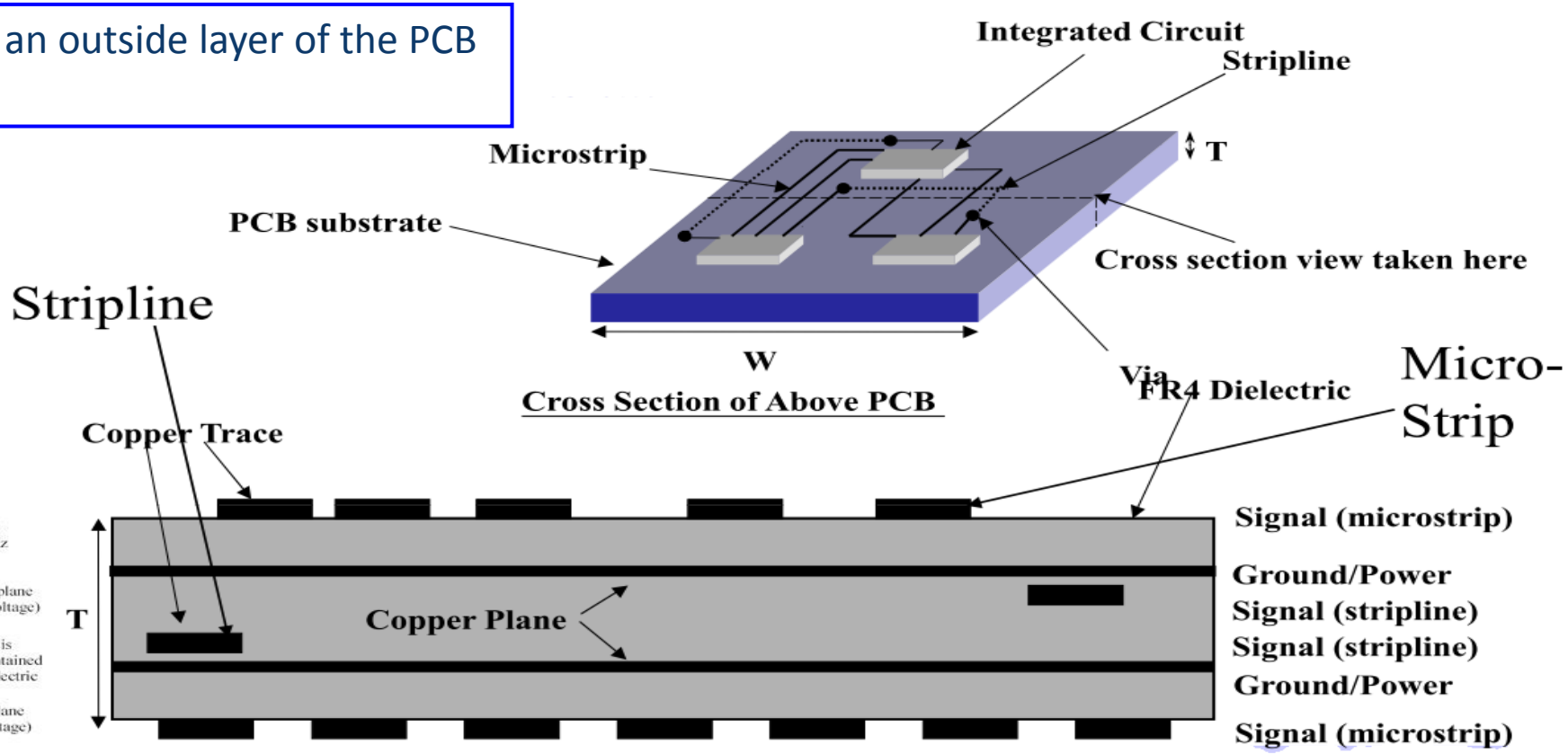
⇒

Reflection noise
Crosstalk noise
Power and ground noise

Impedance Discontinuities

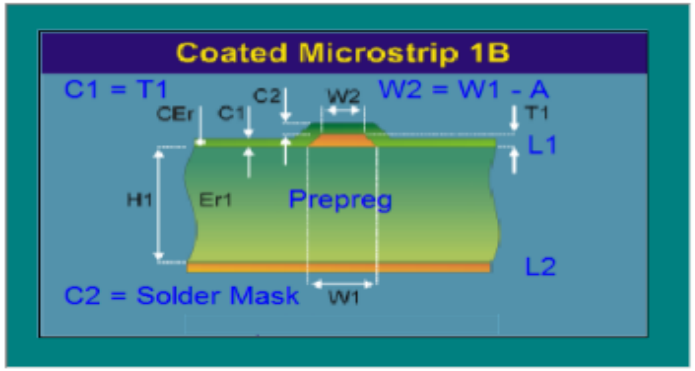
A microstrip is typically routed on an outside layer of the PCB and has only one reference plane.

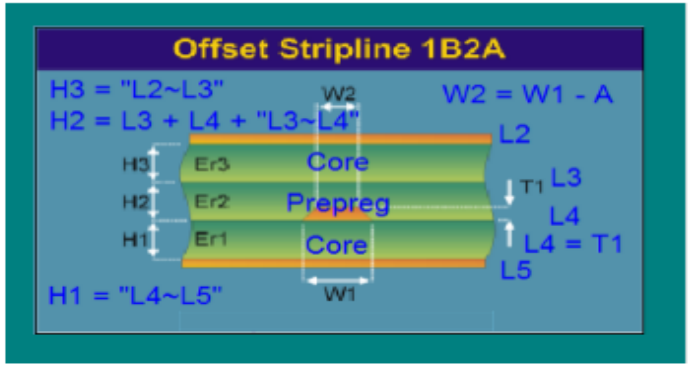


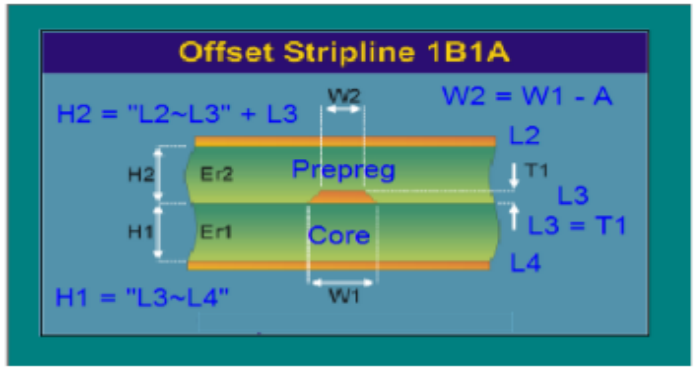


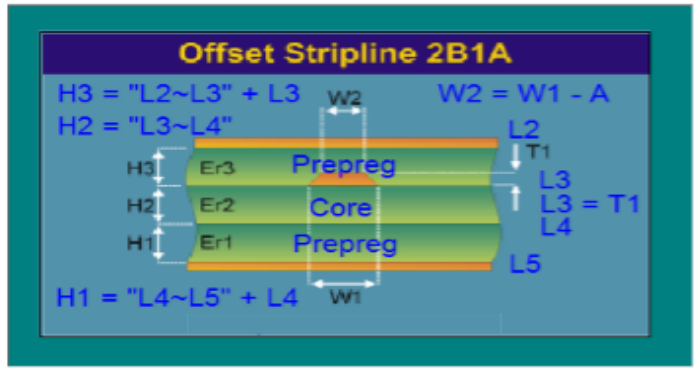
A stripline is routed on an inside layer and has two reference planes.

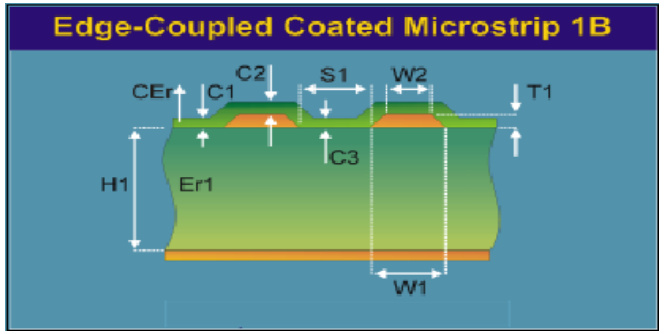
Impedance Discontinuities

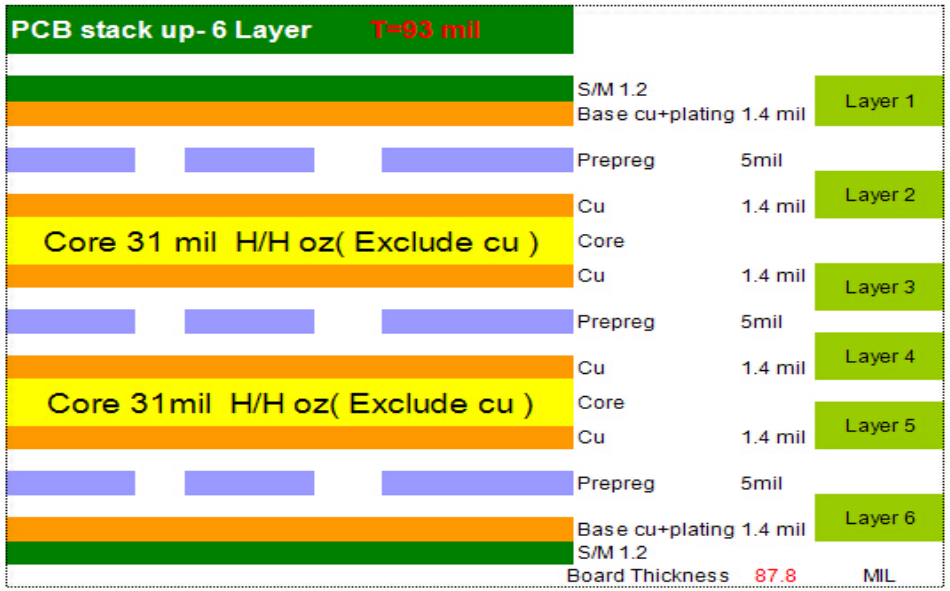




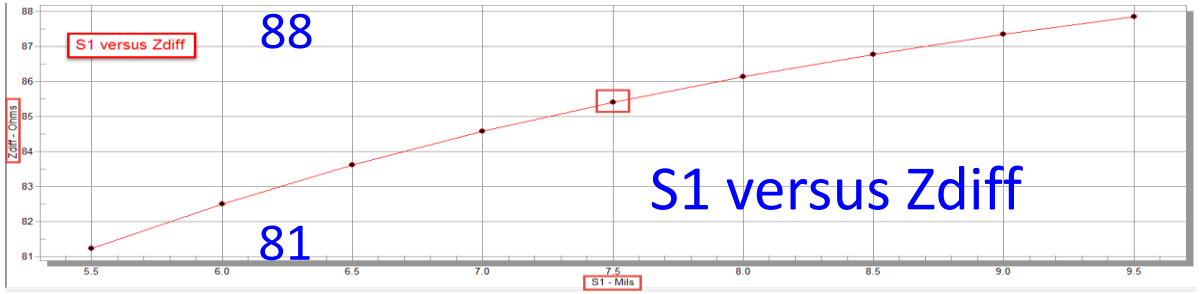


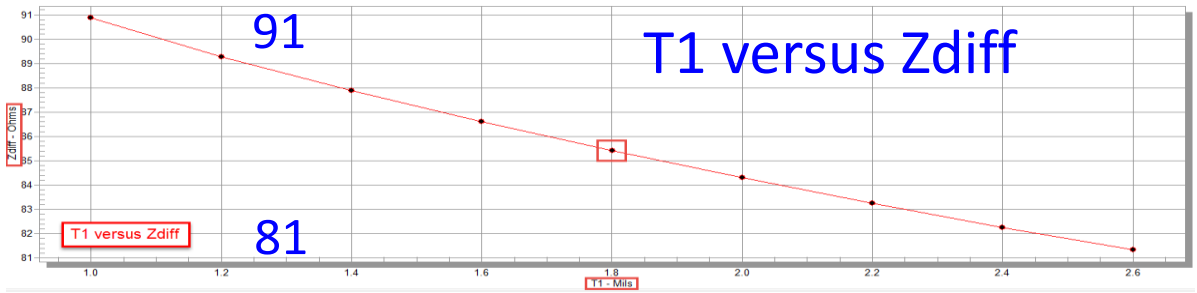


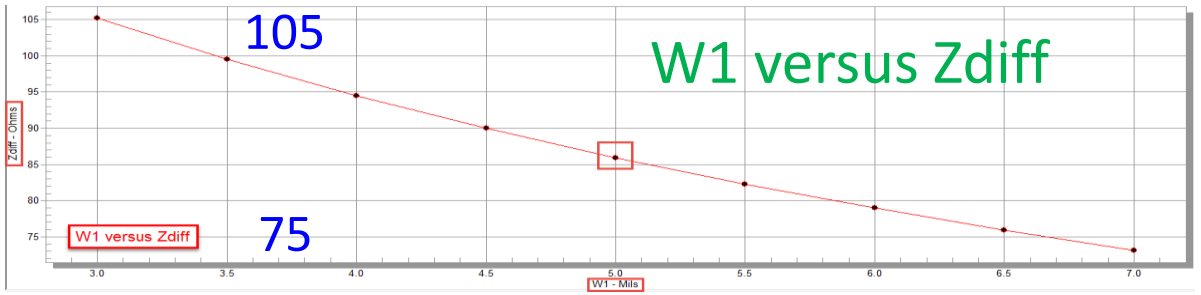


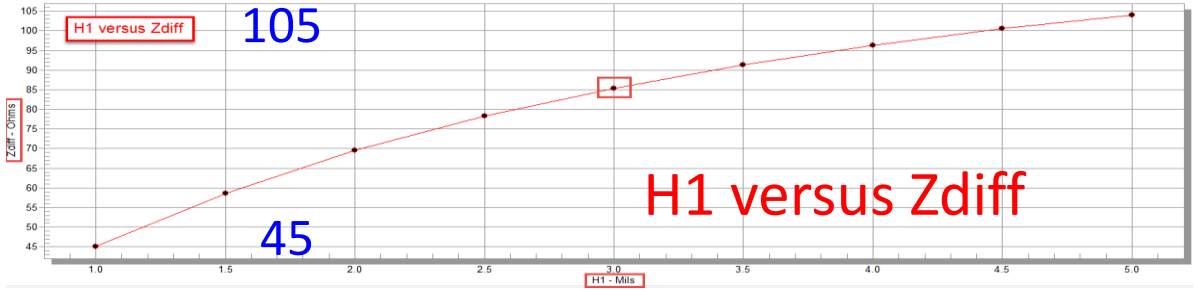


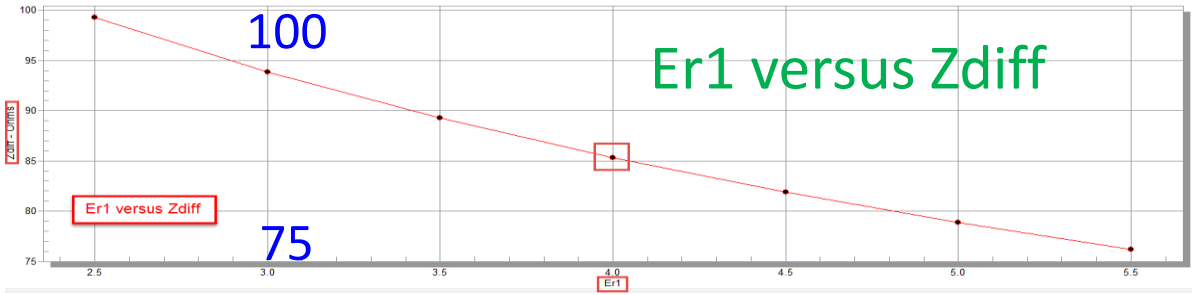
Impedance Discontinuities

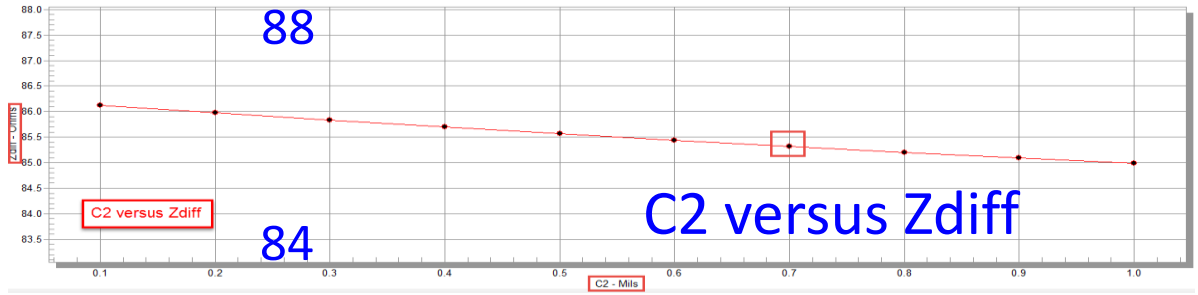




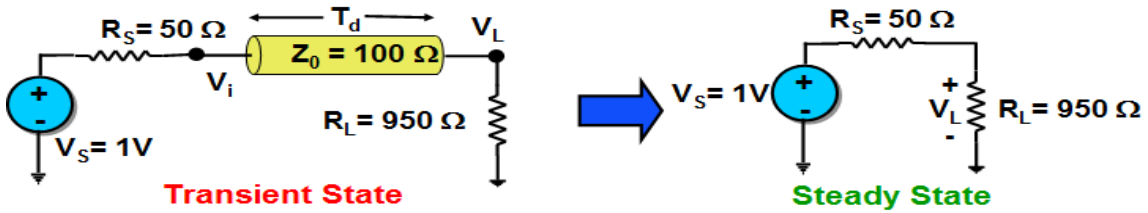








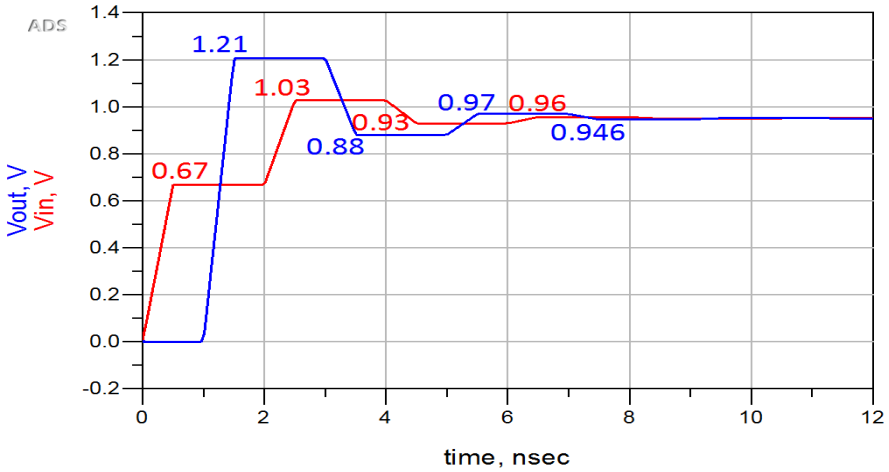
Impedance Discontinuities

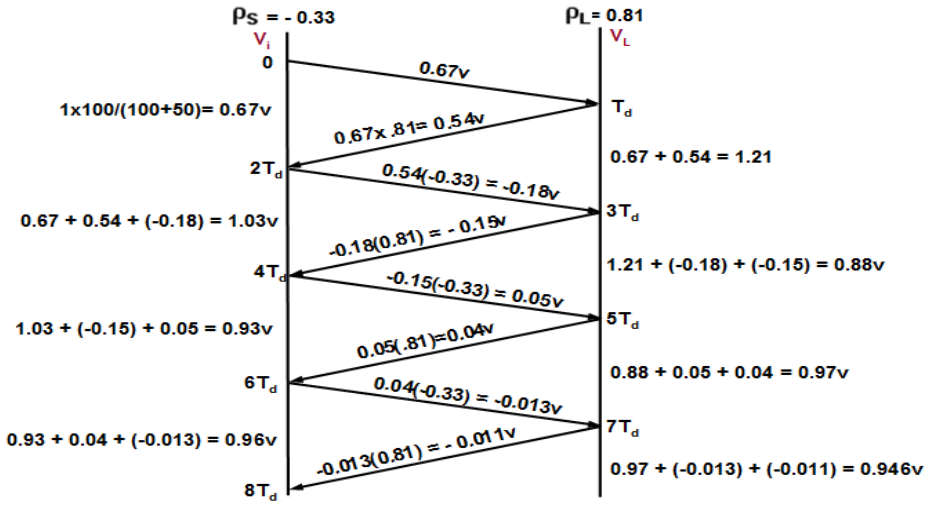


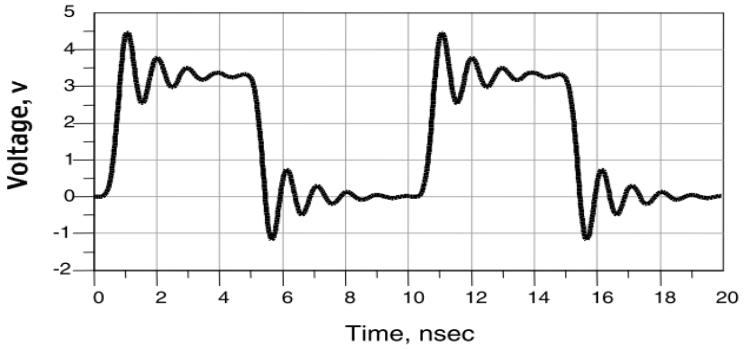
$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} = \frac{50 - 100}{50 + 100} = -0.33$$

$$\rho_L = \frac{R_L - Z_0}{R_L + Z_0} = \frac{950 - 100}{950 + 100} = 0.81$$

$$V_{L\text{-Steady}} = \frac{R_L}{R_S + R_L} V_S = \frac{950}{50 + 950} 1V = 0.95\ V$$







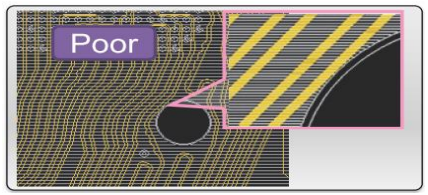
"Ringing" noise at the receiver end of a 1-inch-long controlled-impedance interconnect created because of impedance mismatches and multiple reflections at the ends of the line.

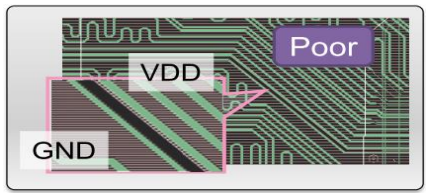
Impedance Discontinuities

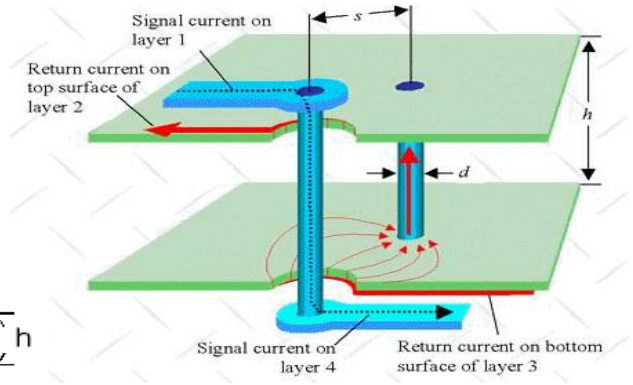
Even if a circuit board is designed with controlled-impedance interconnects, there is still the opportunity for a signal to see an impedance discontinuity from such features as:

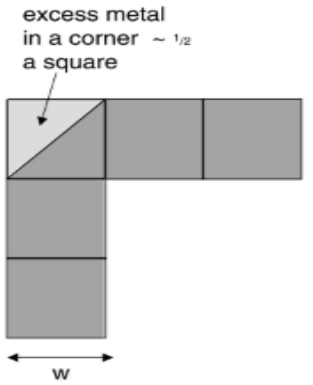
1. The ends of the line
2. A package lead
3. An input-gate capacitance
4. A via between signal layers
5. A corner
6. A stub
7. A branch
8. A test pad
9. A gap in the return path
10. A neck down in a via field
11. A crossover

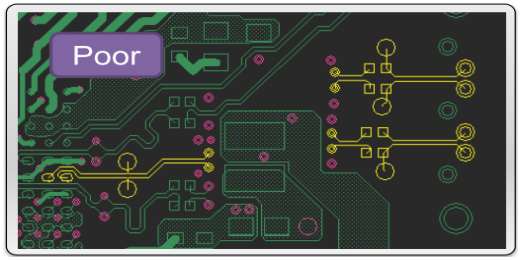
Unless otherwise specified, as a rough rule of thumb, the reflection noise level should be kept to less than 10% of the voltage swing. For a 3.3-v signal, this is 330 mV of noise.

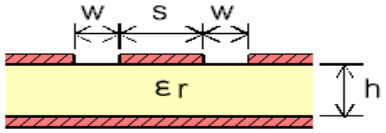




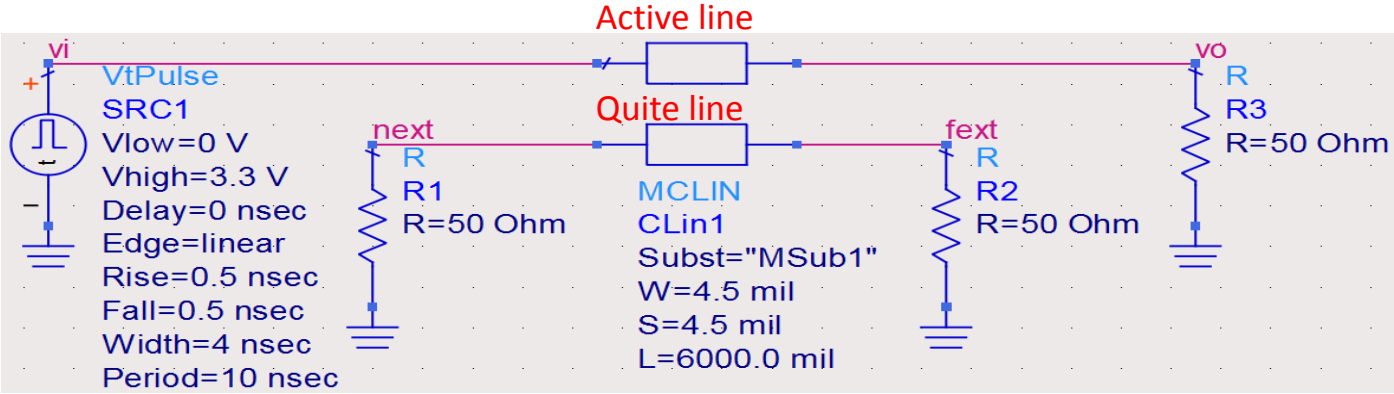


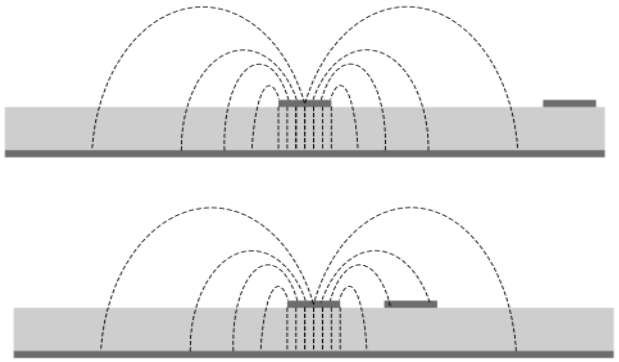




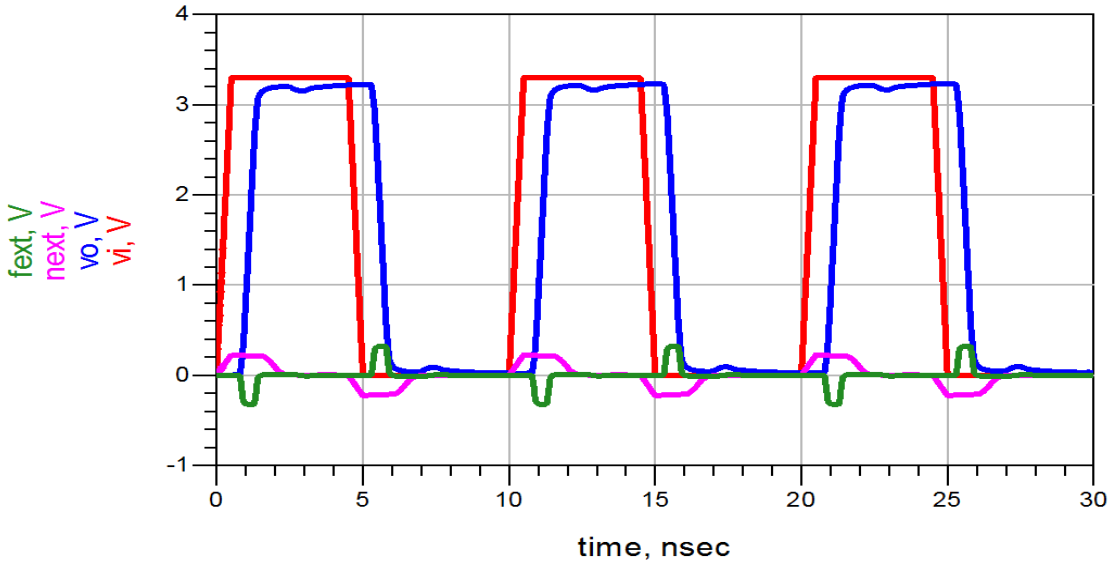


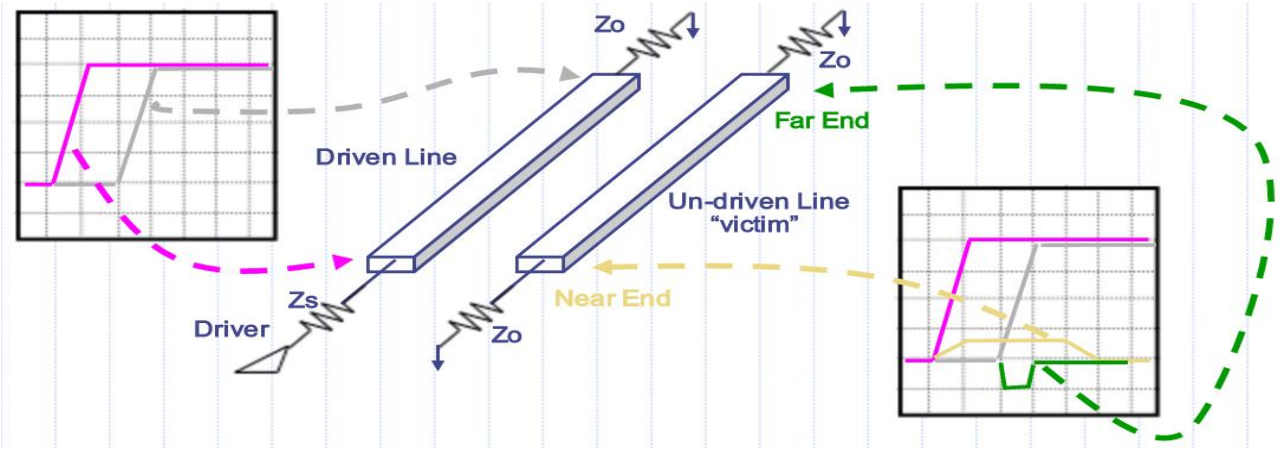
Excessive Coupling



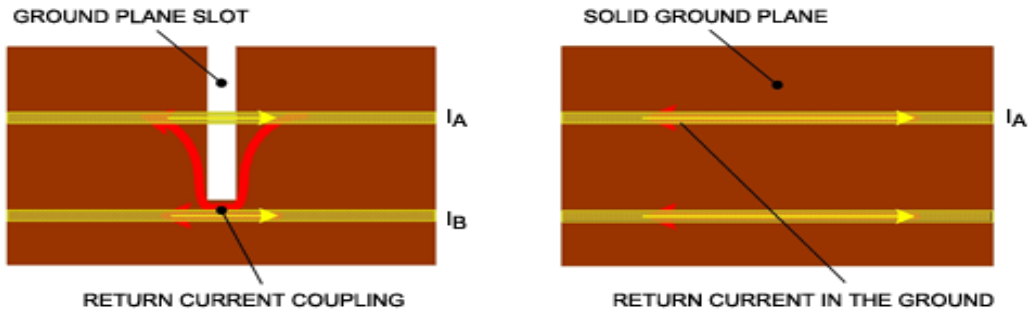


Fringe fields near a signal line. When a second trace is far away, there is little fringe-field coupling and little cross talk. When the second net is in the vicinity of the fringe fields, there can be excessive coupling and cross talk.





Excessive Coupling



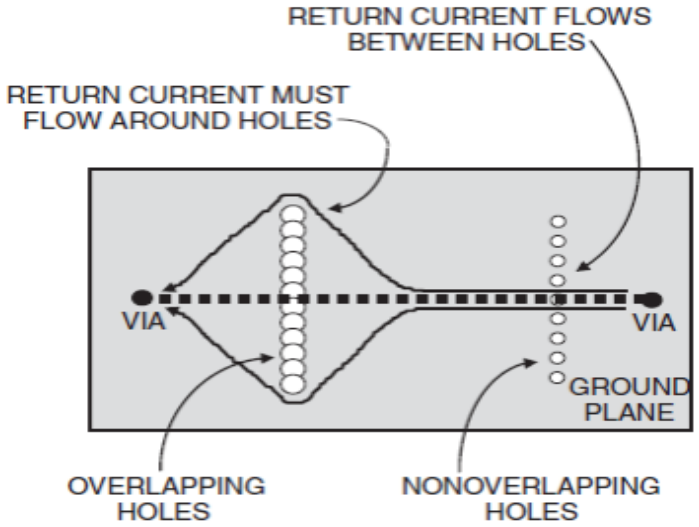
$$\text{Len}_{sat} = \frac{1}{2} \times RT \times v \sim RT \times 3 \frac{\text{inch}}{\text{nanosecond}}$$

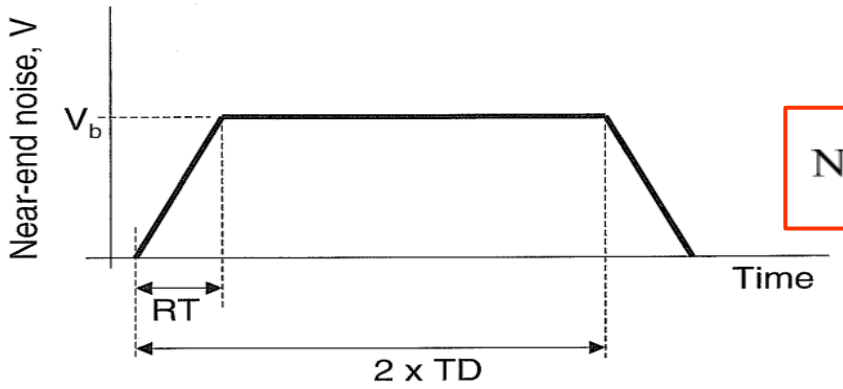
where:

Len_{sat} = the saturation length for near-end cross talk, in inches

RT = the rise time of the signal in nsec

v = the speed of the signal down the active line in inches/nsec



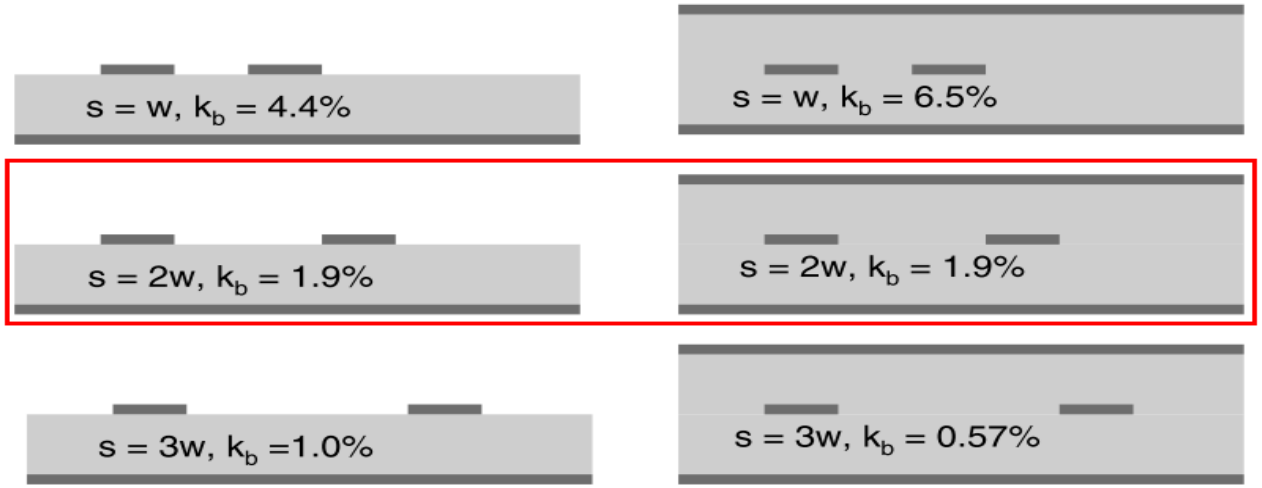


$$NEXT = \frac{V_b}{V_a} = k_b = \frac{1}{4}\left(\frac{C_{mL}}{C_L} + \frac{L_{mL}}{L_L}\right)$$

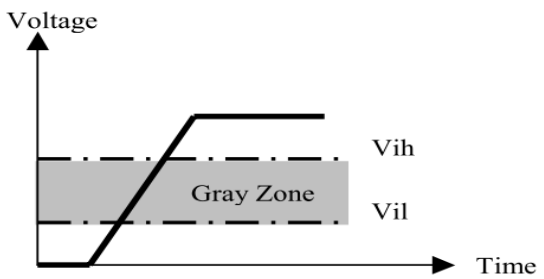
Near-end cross-talk voltage signature when the signal is a linear ramp.

Excessive Coupling

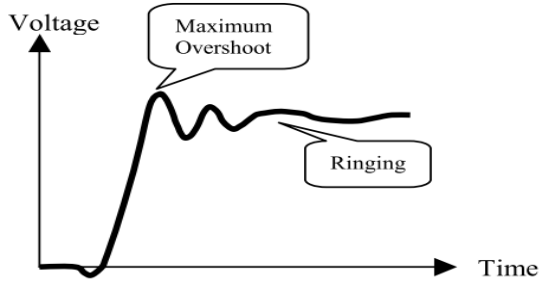
5-mil-wide 50 ohm line in microstrip and stripline



Near-end cross-talk coefficients for microstrip and stripline for a few specific spacings. These are handy rules of thumb to remember.



Ideal waveform at the receiving gate.

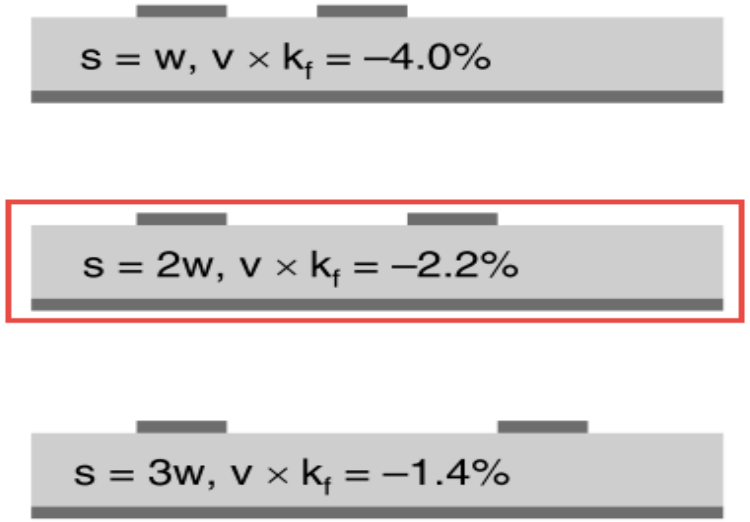


Real waveform at the receiving gate.

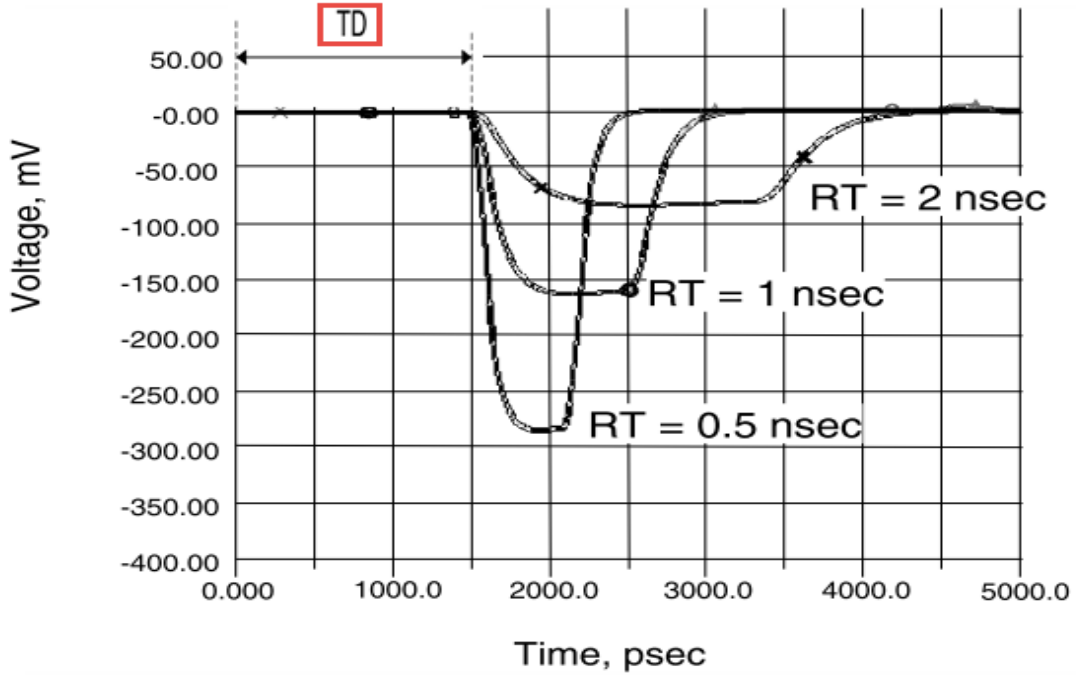
In single-ended systems, the maximum amount of crosstalk to design for, from all sources, should be less than about 5% of the signal swing. In high speed serial links, a safe value for the maximum crosstalk to design for should be less than -50dB, or 0.3%.

Excessive Coupling

5-mil-wide 50 ohm line in microstrip



Simple rules of thumb for estimating the far-end cross talk for a pair of coupled 50-Ohm microstrips in FR4 for different spacings.



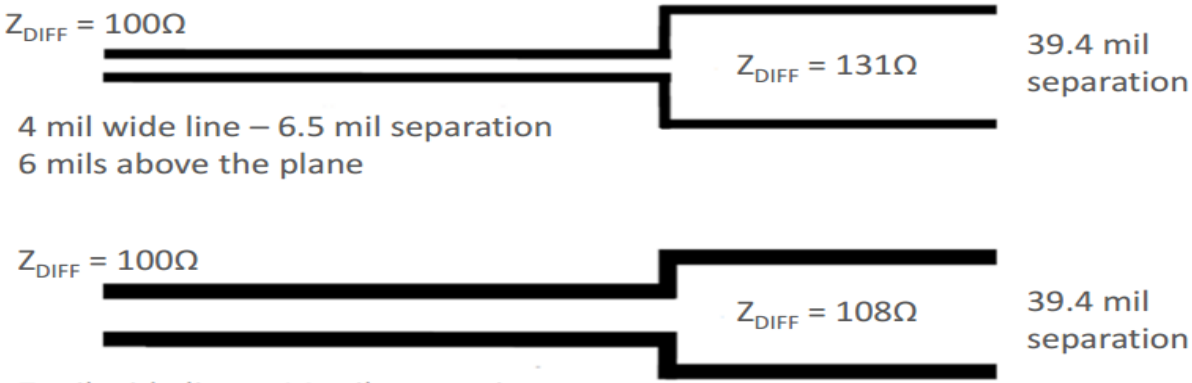
Far-end noise between two 50-Ohm microstrips in FR4 with 5-mil line and space, for the case of three different signal rise times, but the same 10-inch-long coupled length.

$$FEXT = \frac{V_f}{V_a} = \frac{Len}{RT} \times k_f = \frac{Len}{RT} \times \frac{1}{2v} \times \left(\frac{C_{mL}}{C_L} - \frac{L_{mL}}{L_L}\right)$$

Excessive Coupling

Non-Interleaved

Interleaved

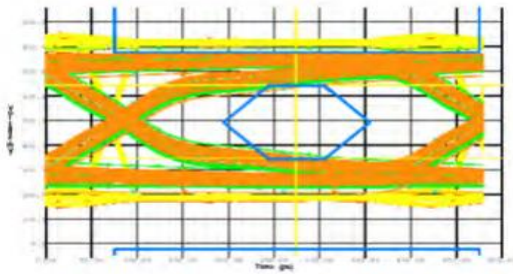


Interleaved mode is implemented on microstrip when FEXT is more significant than NEXT.

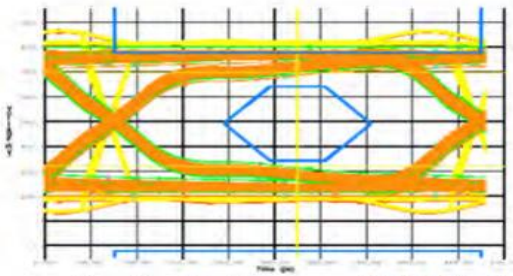
On the other hand, non-interleaved routing is implemented stripline when NEXT is more significant than FEXT.

[Signal Integrity Challenges and Design Practices on a Mobile Platform]

24” long microstrip traces example



4 mil wide traces – 3.125Gb/S



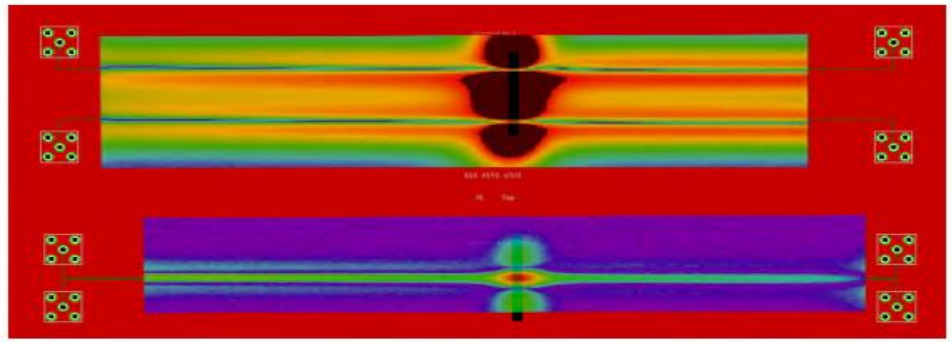
7 mil wide traces – 3.125Gb/S

Excessive Coupling

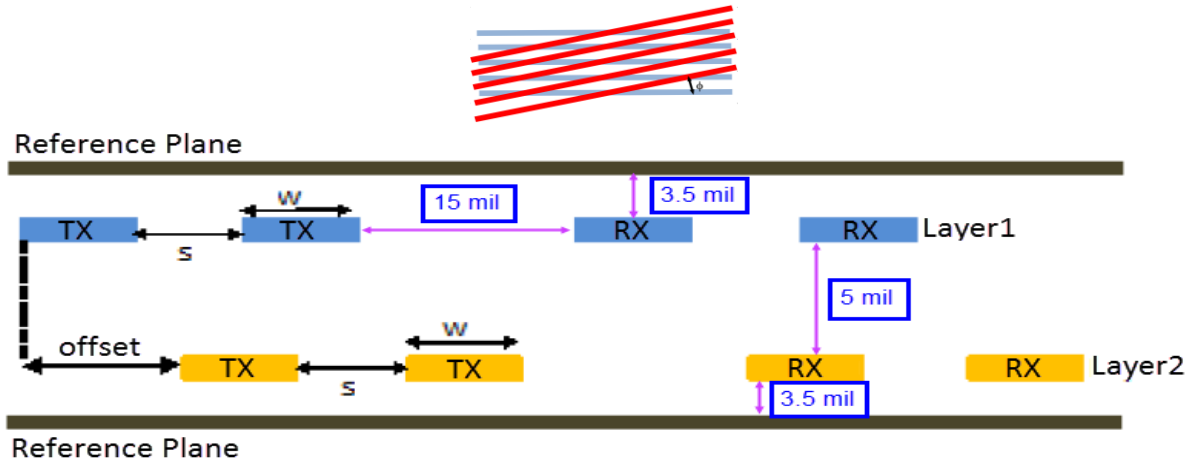
When loss is important, loosely coupled differential pairs should be used.

When interconnect density and noise immunity are important, tightly coupled differential pairs should be used.

With no overriding constraint, loose coupling with a spacing equal to twice the trace width offers a reasonable compromise in providing the lowest loss at the highest interconnect density.



Loosely coupled vs. Tightly coupled differential pair with gap in return path



For high frequency application, using low DF solder mask can help to decrease the microstrip insertion loss significantly, ~10% improvement when comparing the traditional solder mask.

The optimum coating thickness for decreasing far-end noise will depend on all the geometry features and dielectric constants.

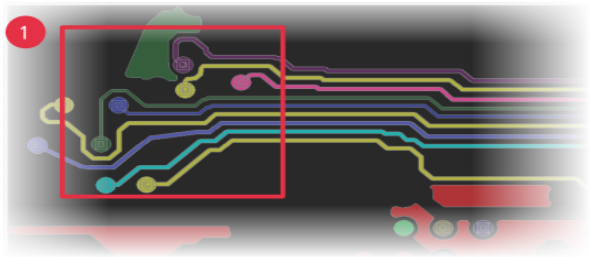
Abstract

- Overview
- **ERC (Electrical Rule Check)**
- SRC (Simulation Rule Check)
- Applications
- Summary

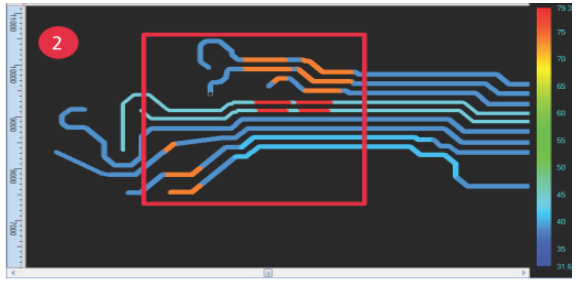
About ERC

ERC-based signal quality checks analyze at the individual, segment-level view in the geometry domain for signal quality, including:

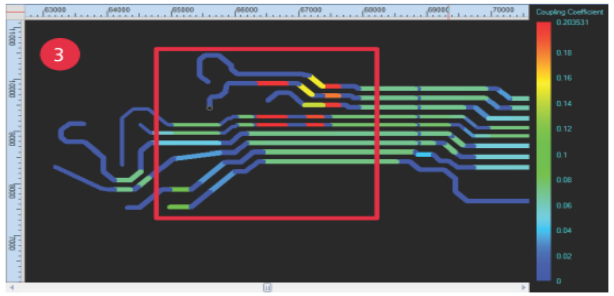
- Trace reference
- Trace reference-aware impedance
- Trace reference-aware coupling
- Differential pair routing phase
- Number of vias and via locations



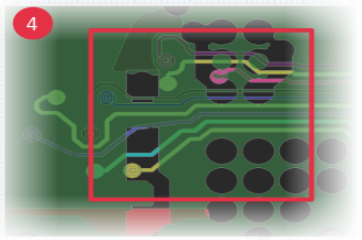
Layout view shows same trace impedance



OrCAD Sigrity ERC reference-aware impedance shows reference discontinuities



OrCAD Sigrity ERC reference-aware coupling shows increased coupling



…due to voids on reference planes

All analysis is organized for easy signal performance interpretation by the PCB layout designer, NOT the signal integrity (SI) expert.

About ERC

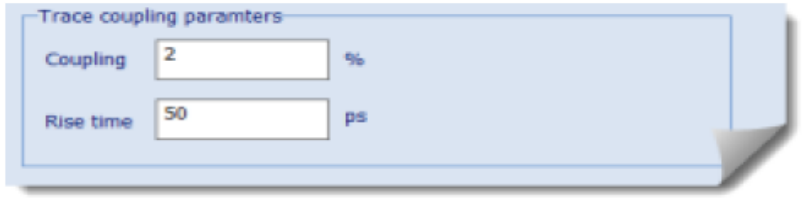
Trace coupling parameters

You can set up trace coupling parameters for the impedance/coupling/reference check. The trace coupling parameters will be used as a threshold. The trace couplings below this threshold will be ignored.

In order for trace coupling to be included,

- The trace near end coupling coefficients must be larger than the given value, and
- The coupled trace segment length must be longer than the NEXT saturation length. The saturation length is calculated using the rise time as

$L_{saturation} = t_r * v$ 0.5 * Trise * V



The smaller the coupling % and rise time thresholds, the more trace segments will be considered as coupled lines. This results in a longer simulation time.

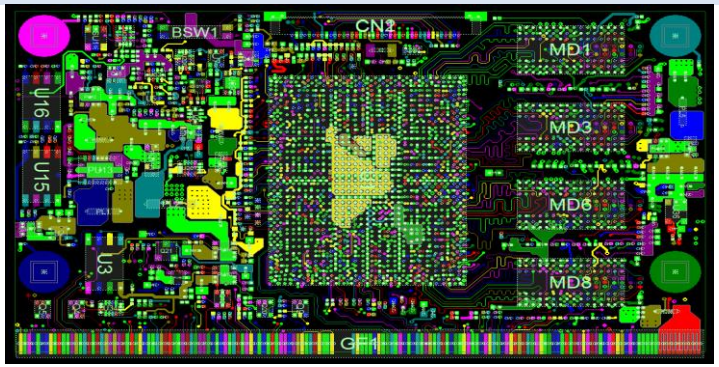
About ERC

Sigrity BrdExtractor

Settings

Translate MIXED layer to: Plane or Signal

- [x] Allow patches on signal layers
- [x] Distinguish shapes of different nets by color
- [ ] Add pseudo plane(s) if lack of plane or patch
- [x] Append net name to objects
- [x] Include elements with no net names
- [ ] Create component model names based upon component part nu
- [x] Remove non-functional pads
- [x] Translate antipads as voids
- [ ] Translate only voltage nets
- [x] Treat pad on dielectric layer as drill
- [ ] Use "Board Geometry > Design Outline" for outline
- [ ] Generate via if padstack drill size is zero
- [ ] Calculate via plating using "Drill/Slot symbol" values
- [ ] Metal layer thickness as plating thickness



ERC - Trace Imp/Cpl/Ref Check

Layout Setup

Load Layout File
Check Stackup
Prepare Nets

Simulation Setup

✓ Enable Trace Check Mode
Optional: Set up Net Groups
Optional: Show Net Groups
Set up Trace Check Parameters
Save File without Error Check

Simulation

Technology	Data rate	Fastest rise time	Scope BW
Ethernet 10base-T	10 Mbps	30 ns	600 MHz
Ethernet 100base-T	100 Mbps	3 ns	600 MHz
Ethernet 1000base-T	250 Mbps x 4	1.2 ns	1 GHz
USB 2.0	480 Mbps	300 ps	2.5 G
USB 3.0	5 Gbps	50 ps	12 GHz
DDR1	400 MT/s	500 ps	2 GHz
DDR2	1066 MT/s	250 ps	4 GHz
DDR3	2133 MT/s	100 ps	8 GHz
DDD4	3200 MT/s	75 ps	12 GHz
GDDR5	8 Gbps	30 ps	16 GHz
SATA 3G	3 Gbps	67 ps	12 GHz
SATA 6G	6 Gbps	33 ps	16 GHz
SAS-2	6 Gbps	42 ps	16 GHz
SAS-3	12 Gbps	21 ps	30 GHz
16G FibreChannel	14.025 Gbps	24 ps	35 GHz
HDMI 1.4	3.4 Gbps	50 ps	8 GHz
DisplayPort 1.2	5.4 Gbps	50 ps	13 GHz

Impedance/Coupling Check Option

- [x] Impedance
- [x] Coupling Coefficient

Trace coupling paramters

Coupling 2 %

Rise time 100 ps

Nets Selection Option

- ( ) Check all signal nets(enable all signal nets)
- (•) Check all enabled signal nets

Notes: Go to Net Manager to enable nets for Trace Check

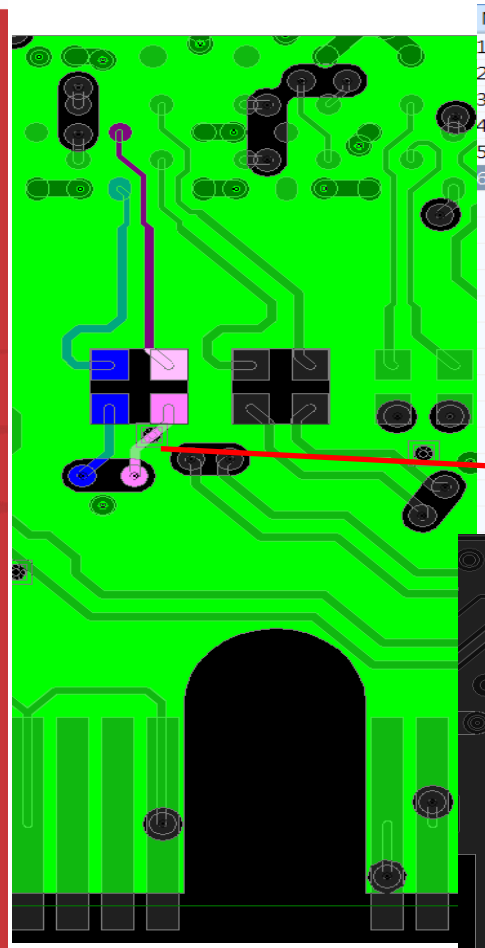
- ( ) Check by NetGroup

Notes:
1.Detailed and interactive results are available with Check by NetGroup.
2.A pair of extended nets are reported as one signal.

Coplanar Traces

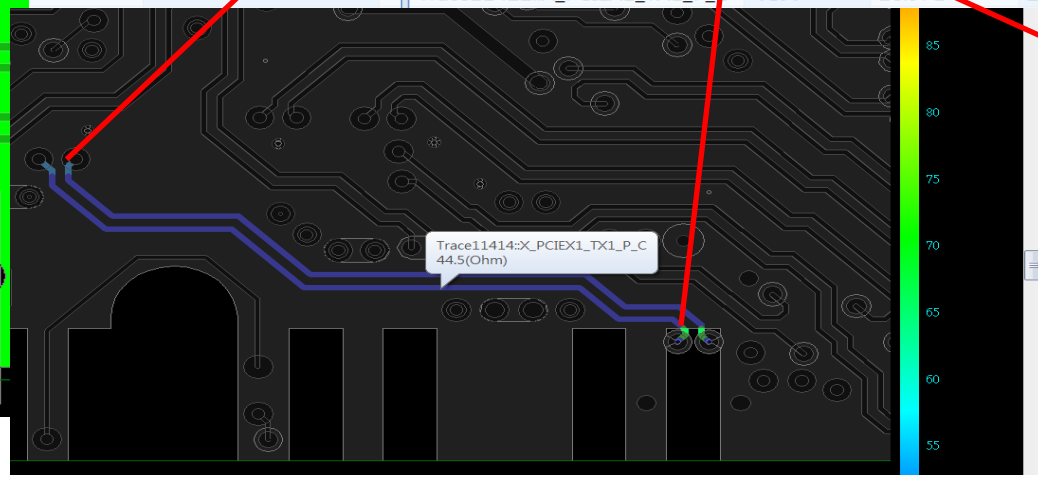
- [x] Detect and model the coplanar traces

About ERC

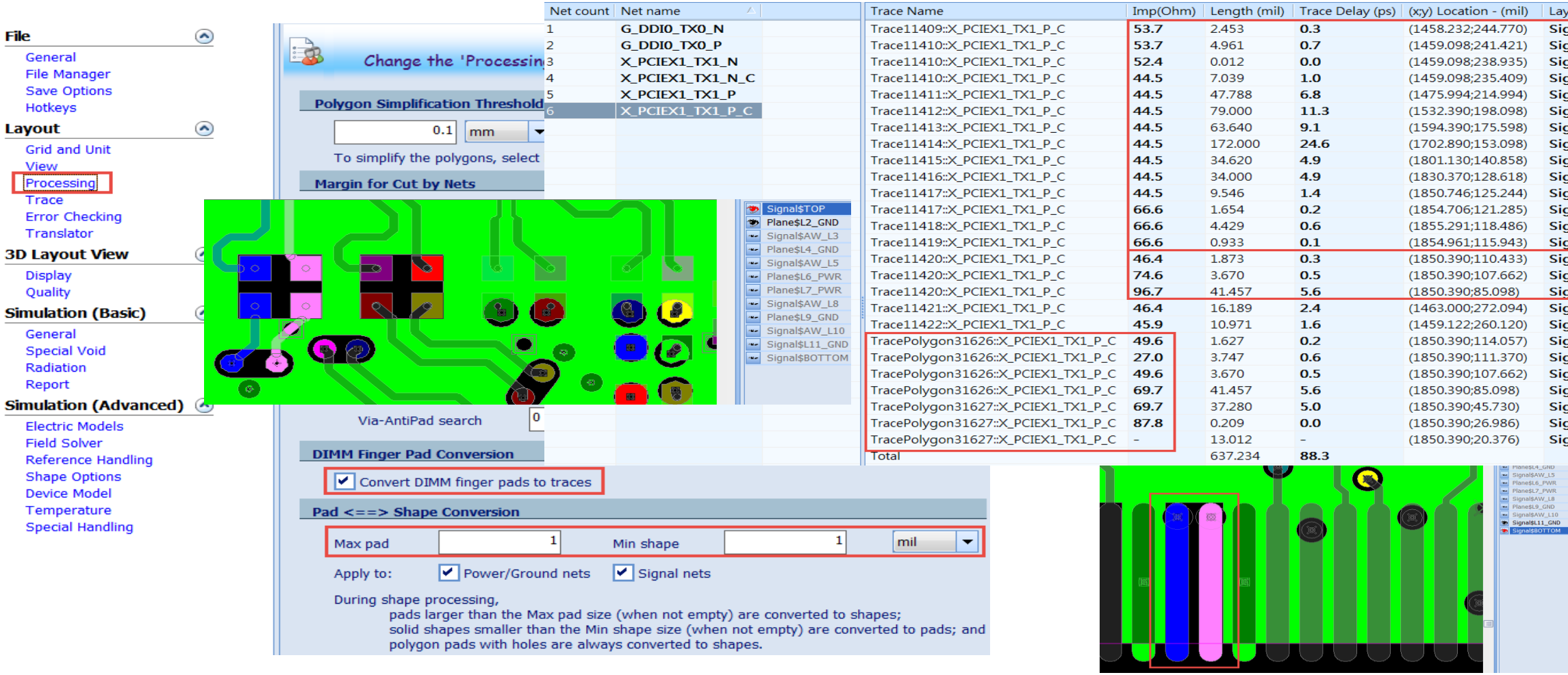


Net count	Net name
1	G_DDI0_TX0_N
2	G_DDI0_TX0_P
3	X_PCIEX1_TX1_N
4	X_PCIEX1_TX1_N_C
5	X_PCIEX1_TX1_P
6	X_PCIEX1_TX1_P_C

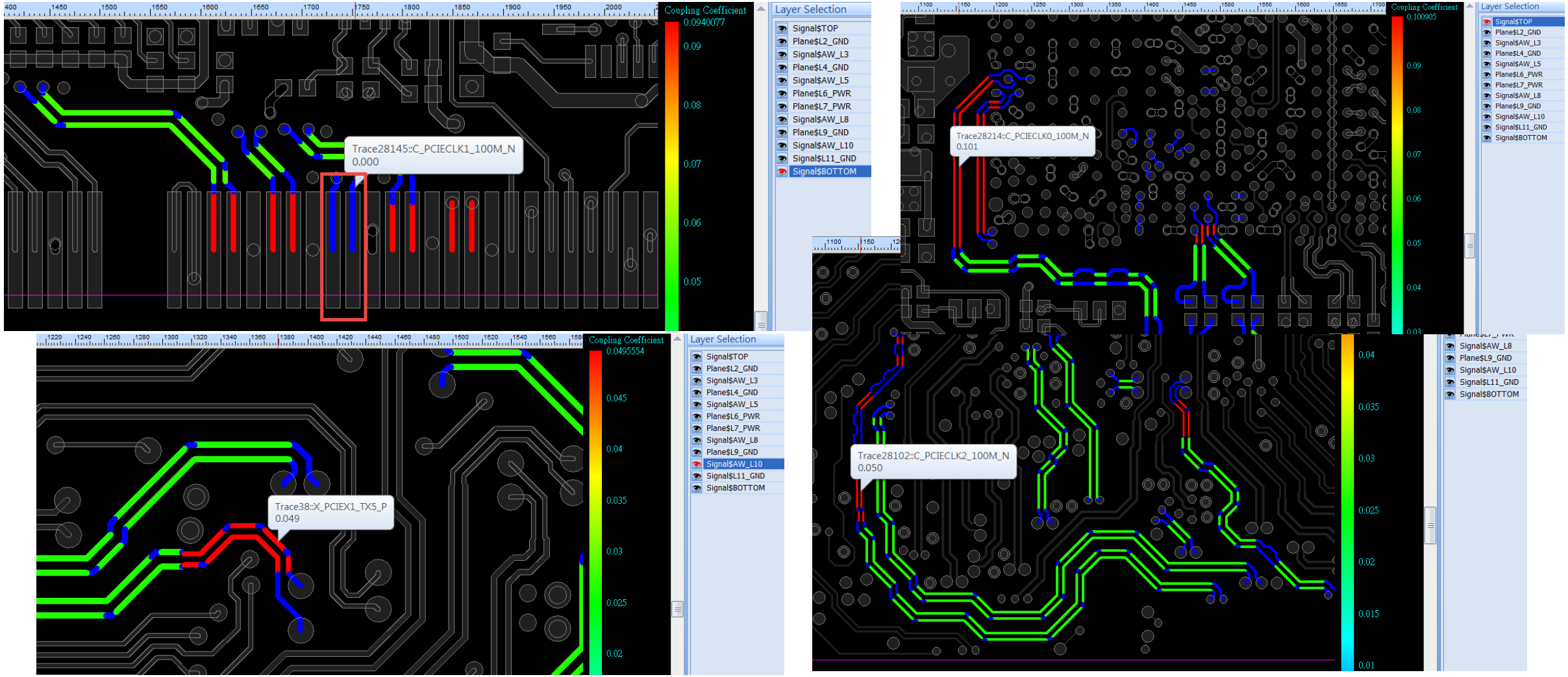
Trace Name	Imp(Ohm)	Length (mil)	Trace Delay (ps)	(x;y) Location - (mil)	Layer	R (mOhm)	L (nH)	C (pF)
Trace11409::X_PCIEX1_TX1_P_C	53.7	11.453	1.6	(1455.049;247.951)	Signal$AW_L10	1.652	0.088	0.030
Trace11410::X_PCIEX1_TX1_P_C	53.7	4.961	0.7	(1459.098;241.421)	Signal$AW_L10	0.716	0.038	0.013
Trace11410::X_PCIEX1_TX1_P_C	52.4	0.012	0.0	(1459.098;238.935)	Signal$AW_L10	0.002	0.000	0.000
Trace11410::X_PCIEX1_TX1_P_C	44.5	7.039	1.0	(1459.098;235.409)	Signal$AW_L10	1.015	0.045	0.023
Trace11411::X_PCIEX1_TX1_P_C	44.5	47.788	6.8	(1475.994;214.994)	Signal$AW_L10	6.894	0.303	0.153
Trace11412::X_PCIEX1_TX1_P_C	44.5	79.000	11.3	(1532.390;198.098)	Signal$AW_L10	11.396	0.502	0.254
Trace11413::X_PCIEX1_TX1_P_C	44.5	63.640	9.1	(1594.390;175.598)	Signal$AW_L10	9.180	0.404	0.204
Trace11414::X_PCIEX1_TX1_P_C	44.5	172.000	24.6	(1702.890;153.098)	Signal$AW_L10	24.812	1.092	0.552
Trace11415::X_PCIEX1_TX1_P_C	44.5	34.620	4.9	(1801.130;140.858)	Signal$AW_L10	4.994	0.220	0.111
Trace11416::X_PCIEX1_TX1_P_C	44.5	34.000	4.9	(1830.370;128.618)	Signal$AW_L10	4.905	0.216	0.109
Trace11417::X_PCIEX1_TX1_P_C	44.5	9.546	1.4	(1850.746;125.244)	Signal$AW_L10	1.377	0.061	0.031
Trace11417::X_PCIEX1_TX1_P_C	66.6	1.654	0.2	(1854.706;121.285)	Signal$AW_L10	0.239	0.016	0.004
Trace11418::X_PCIEX1_TX1_P_C	66.6	4.429	0.6	(1855.291;118.486)	Signal$AW_L10	0.639	0.042	0.009
Trace11419::X_PCIEX1_TX1_P_C	66.6	5.058	0.7	(1853.503;114.483)	Signal$AW_L10	0.730	0.048	0.011
Trace11419::X_PCIEX1_TX1_P_C	44.5	1.874	0.3	(1851.052;112.033)	Signal$AW_L10	0.270	0.012	0.006
Trace11420::X_PCIEX1_TX1_P_C	46.4	1.873	0.3	(1850.390;110.433)	Signal$BOTTOM	0.162	0.013	0.006
Trace11420::X_PCIEX1_TX1_P_C	96.7	45.127	6.1	(1850.390;86.933)	Signal$BOTTOM	3.908	0.594	0.063
Trace11421::X_PCIEX1_TX1_P_C	46.4	24.189	3.5	(1463.000;276.094)	Signal$TOP	2.095	0.164	0.076
Trace11422::X_PCIEX1_TX1_P_C	46.4	16.971	2.5	(1457.000;258.000)	Signal$TOP	1.469	0.115	0.054
						76.453	3.971	1.709



About ERC


File
General
File Manager
Save Options
Hotkeys
Layout
Grid and Unit
View
Processing
Trace
Error Checking
Translator
3D Layout View
Display
Quality
Simulation (Basic)
General
Special Void
Radiation
Report
Simulation (Advanced)
Electric Models
Field Solver
Reference Handling
Shape Options
Device Model
Temperature
Special Handling
Change the 'Processin
Polygon Simplification Threshold
0.1
mm
To simplify the polygons, select
Margin for Cut by Nets
Via-AntiPad search
0
DIMM Finger Pad Conversion
Convert DIMM finger pads to traces
Pad <==> Shape Conversion
Max pad
1
Min shape
1
mil
Apply to:
Power/Ground nets
Signal nets
During shape processing,
pads larger than the Max pad size (when not empty) are converted to shapes;
solid shapes smaller than the Min shape size (when not empty) are converted to pads; and
polygon pads with holes are always converted to shapes.
Net count
Net name
1 G_DDI0_TX0_N
2 G_DDI0_TX0_P
3 X_PCIEX1_TX1_N
4 X_PCIEX1_TX1_N_C
5 X_PCIEX1_TX1_P
6 X_PCIEX1_TX1_P_C
Signal$TOP
Plane$L2_GND
Signal$AW_L3
Plane$L4_GND
Signal$AW_L5
Plane$L6_PWR
Plane$L7_PWR
Signal$AW_L8
Plane$L9_GND
Signal$AW_L10
Signal$L11_GND
Signal$BOTTOM
Trace Name | Imp(Ohm) | Length (mil) | Trace Delay (ps) | (x;y) Location - (mil) | Layer
Trace11409::X_PCIEX1_TX1_P_C | 53.7 | 2.453 | 0.3 | (1458.232;244.770) | Signal$AW_L10
Trace11410::X_PCIEX1_TX1_P_C | 53.7 | 4.961 | 0.7 | (1459.098;241.421) | Signal$AW_L10
Trace11410::X_PCIEX1_TX1_P_C | 52.4 | 0.012 | 0.0 | (1459.098;238.935) | Signal$AW_L10
Trace11410::X_PCIEX1_TX1_P_C | 44.5 | 7.039 | 1.0 | (1459.098;235.409) | Signal$AW_L10
Trace11411::X_PCIEX1_TX1_P_C | 44.5 | 47.788 | 6.8 | (1475.994;214.994) | Signal$AW_L10
Trace11412::X_PCIEX1_TX1_P_C | 44.5 | 79.000 | 11.3 | (1532.390;198.098) | Signal$AW_L10
Trace11413::X_PCIEX1_TX1_P_C | 44.5 | 63.640 | 9.1 | (1594.390;175.598) | Signal$AW_L10
Trace11414::X_PCIEX1_TX1_P_C | 44.5 | 172.000 | 24.6 | (1702.890;153.098) | Signal$AW_L10
Trace11415::X_PCIEX1_TX1_P_C | 44.5 | 34.620 | 4.9 | (1801.130;140.858) | Signal$AW_L10
Trace11416::X_PCIEX1_TX1_P_C | 44.5 | 34.000 | 4.9 | (1830.370;128.618) | Signal$AW_L10
Trace11417::X_PCIEX1_TX1_P_C | 44.5 | 9.546 | 1.4 | (1850.746;125.244) | Signal$AW_L10
Trace11417::X_PCIEX1_TX1_P_C | 66.6 | 1.654 | 0.2 | (1854.706;121.285) | Signal$AW_L10
Trace11418::X_PCIEX1_TX1_P_C | 66.6 | 4.429 | 0.6 | (1855.291;118.486) | Signal$AW_L10
Trace11419::X_PCIEX1_TX1_P_C | 66.6 | 0.933 | 0.1 | (1854.961;115.943) | Signal$AW_L10
Trace11420::X_PCIEX1_TX1_P_C | 46.4 | 1.873 | 0.3 | (1850.390;110.433) | Signal$BOTTOM
Trace11420::X_PCIEX1_TX1_P_C | 74.6 | 3.670 | 0.5 | (1850.390;107.662) | Signal$BOTTOM
Trace11420::X_PCIEX1_TX1_P_C | 96.7 | 41.457 | 5.6 | (1850.390;85.098) | Signal$BOTTOM
Trace11421::X_PCIEX1_TX1_P_C | 46.4 | 16.189 | 2.4 | (1463.000;272.094) | Signal$TOP
Trace11422::X_PCIEX1_TX1_P_C | 45.9 | 10.971 | 1.6 | (1459.122;260.120) | Signal$TOP
TracePolygon31626::X_PCIEX1_TX1_P_C | 49.6 | 1.627 | 0.2 | (1850.390;114.057) | Signal$BOTTOM
TracePolygon31626::X_PCIEX1_TX1_P_C | 27.0 | 3.747 | 0.6 | (1850.390;111.370) | Signal$BOTTOM
TracePolygon31626::X_PCIEX1_TX1_P_C | 49.6 | 3.670 | 0.5 | (1850.390;107.662) | Signal$BOTTOM
TracePolygon31626::X_PCIEX1_TX1_P_C | 69.7 | 41.457 | 5.6 | (1850.390;85.098) | Signal$BOTTOM
TracePolygon31627::X_PCIEX1_TX1_P_C | 69.7 | 37.280 | 5.0 | (1850.390;45.730) | Signal$BOTTOM
TracePolygon31627::X_PCIEX1_TX1_P_C | 87.8 | 0.209 | 0.0 | (1850.390;26.986) | Signal$BOTTOM
TracePolygon31627::X_PCIEX1_TX1_P_C | - | 13.012 | - | (1850.390;20.376) | Signal$BOTTOM
Total | | 637.234 | 88.3 |

About ERC


Coupling Coefficient
0.0940077
0.09
0.08
0.07
0.06
0.05
Trace28145::C_PCIECLK1_100M_N
0.000
Layer Selection
Signal$TOP
Plane$L2_GND
Signal$AW_L3
Plane$L4_GND
Signal$AW_L5
Plane$L6_PWR
Plane$L7_PWR
Signal$AW_L8
Plane$L9_GND
Signal$AW_L10
Signal$L11_GND
Signal$BOTTOM
Coupling Coefficient
0.100905
0.09
0.08
0.07
0.06
0.05
0.04
0.03
Trace28214::C_PCIECLK0_100M_N
0.101
Coupling Coefficient
0.0495554
0.045
0.04
0.035
0.03
0.025
0.02
Trace38::X_PCIEX1_TX5_P
0.049
Trace28102::C_PCIECLK2_100M_N
0.050
0.04
0.035
0.03
0.025
0.02
0.015
0.01

About ERC

Is trace-to-trace coupling included in impedance calculation?

No.

Can trace impedance be determined only thru co-planar cooupling?

For traces without reference planes, they may depend on the ground shapes on the same layer as signal return. Trace check impedance cannot be determined using co-planar coupling.

Are differential trace impedance and coupling check results available?

Starting from ASI 16.61, differential impedance and coupling are available. In order to get differential trace check results, differential nets need to be classified when forming net groups.

Is trapezoidal cross-section considered in the trace check?

Yes. You should use workflow step **Check Stackup** to set up trapezoidal angles.

About ERC

Is via impedance/coupling included in the trace check?

No.

Is via delay calculated in the trace check?

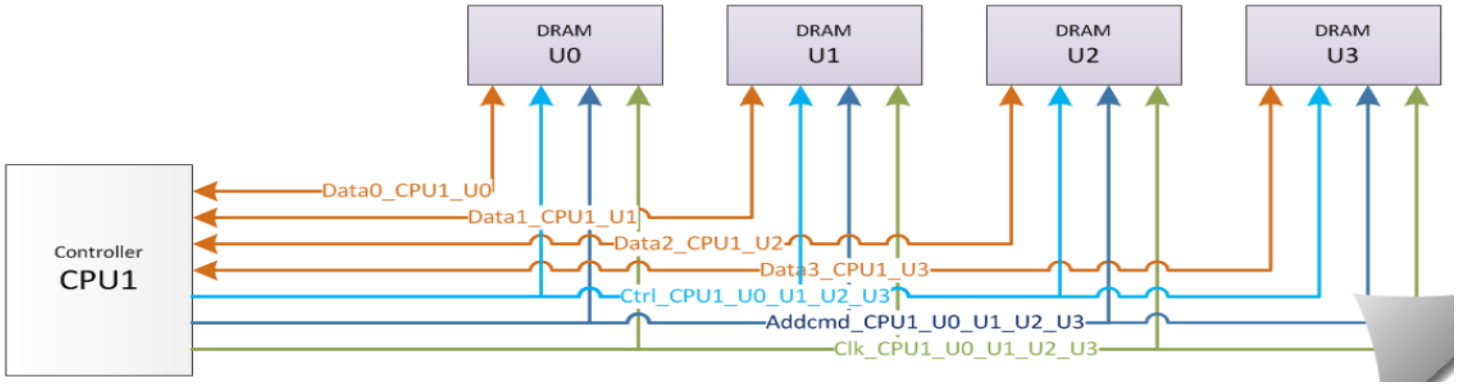
No.

Is coupling between different net groups included

If multiple net groups are included in one trace check simulation, couplings among nets in all net groups are included.

Is coupling for not enabled nets included?

No.



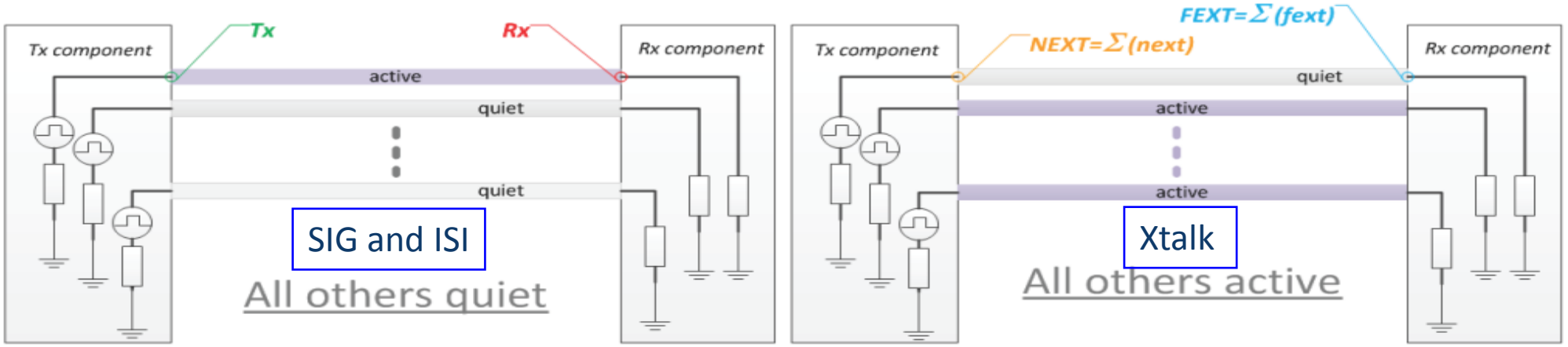
Abstract

- Overview
- ERC (Electrical Rule Check)
- **SRC (Simulation Rule Check)**
- Applications
- Summary

About SRC

This net-level PCB layout checking engine is based on time-domain simulation (device simulation models are not needed), and considers:

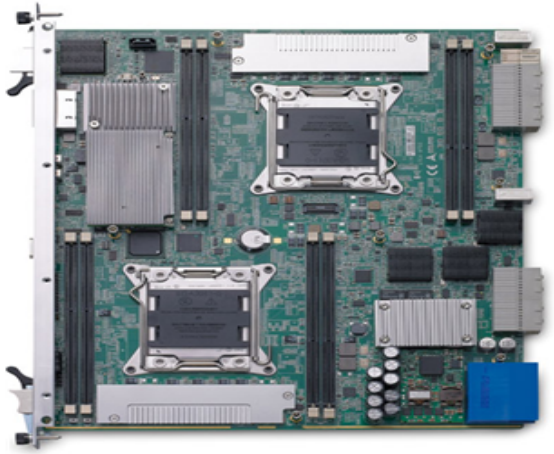
- Loss
- Delay
- Reflections
- Trace couplings
- Via coupling



After SRC simulation, TX, RX, NEXT (near end xtalk), and FEXT (far end xtalk) waveforms are available, as well as SI metrics calculated using RX and FEXT waveforms as signal quality indicators.

About SRC

Generic
TX Buffer Model



Transmission line and via model extracted from layout

Generic
RX Buffer Model

Sigrity SRC

Compare the check result to the data from success design

Pulse Responses

SI Metrics

Sigrity SRC

- Layout SI macro view at net level
- All inclusive end results
- Shows what happened and its effect on performance

"Channel Checking"
or "Channel Quality Comparison"

About SRC

$Int\_sig = \int_{t_1}^{t_2} \lvert Rx(t) \rvert dt$	Higher channel loss will decrease the SIG. Trace length, dielectric loss, and conductive loss will all increase the channel loss. *The higher SIG, the better signal integrity is.* ▲
$Int\_ISI = \int_{0}^{t_1} \lvert Rx(t) \rvert dt + \int_{t_2}^{t_{max}} \lvert Rx(t) \rvert dt$	Loss and impedance discontinuity will both increase the "ISI" (Intersymbol interference). *The larger the ISI, the worse signal integrity is.* ▼
$Int\_xtk = \sum \int_{0}^{t_{max}} \lvert fext_i(t) \rvert dt$	Far-end crosstalk is calculated by including all the other signals which is included in the simulation. *The larger FEXT, the worse signal integrity is.* ▼
$SN\_difference = (Int\_sig) - (Int\_ISI) - (Int\_xtk)$	*The larger* **value** *, the better signal integrity is.* ▲
$SN\_ratio = \frac{Int\_sig}{(Int\_ISI) + (Int\_xtk)}$	The concept is similar to SNR (signal-to-noise ratio) *The larger* **value** *, the better signal integrity is.* ▲

About SRC

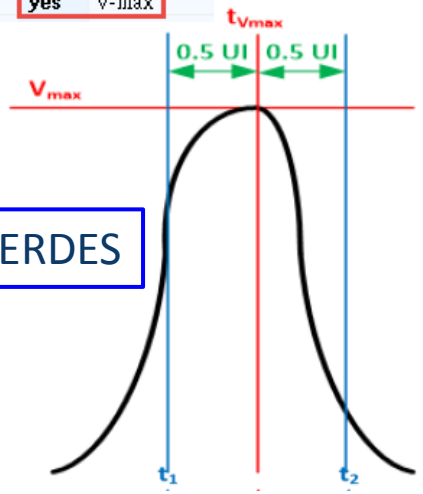
Net group names	Tx component	Net name	Passive component	Net name	Passive component	Net name	Rx component(active)	Rx component(standby)	Rx component(not populated)	FIR filter	Pulse center
PCIEX1_TX_PCH1_CN3											
	PCH1	X_PCIEX1_1_TX_N_C	C27	X_PCIEX1_1_TX_N	-	-	CN3	-	-	yes	v-max
	PCH1	X_PCIEX1_1_TX_P_C	C26	X_PCIEX1_1_TX_P	-	-	CN3	-	-	yes	v-max
	PCH1	X_PCIEX1_2_TX_N_C	C25	X_PCIEX1_2_TX_N	-	-	CN3	-	-	yes	v-edge
	PCH1	X_PCIEX1_2_TX_P_C	C24	X_PCIEX1_2_TX_P	-	-	CN3	-	-	yes	v-max
	PCH1	X_PCIEX1_3_TX_N_C	C23	X_PCIEX1_3_TX_N	-	-	CN3	-	-	yes	v-max
	PCH1	X_PCIEX1_3_TX_P_C	C22	X_PCIEX1_3_TX_P	-	-	CN3	-	-	yes	v-max

Net group names	Tx component	Net name	Rx component(active)	Rx component(standby	Rx component(not populated)	FIR filter	Pulse center
PCIEX1_RX_CN3_PCH1							
	CN3	X_PCIEX1_1_RX_N	PCH1	-	-	yes	v-max
	CN3	X_PCIEX1_1_RX_P	PCH1	-	-	yes	v-max
	CN3	X_PCIEX1_2_RX_N	PCH1	-	-	yes	v-max
	CN3	X_PCIEX1_2_RX_P	PCH1	-	-	yes	v-max
	CN3	X_PCIEX1_3_RX_N	PCH1	-	-	yes	v-max
	CN3	X_PCIEX1_3_RX_P	PCH1	-	-	yes	v-max

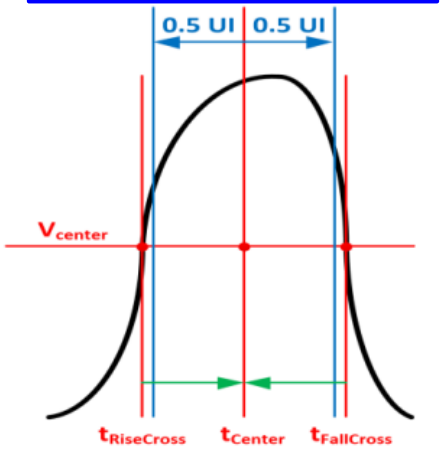
FIR filter is recommended to be enabled for SERDES link SI Metrics Check. When FIR is applied:

- Coefficient is calculated for each net by forcing the first post curser 0
- The pulse is balanced and centered, making the SI Metrics more reasonable (Otherwise, the pulse is not centered, causing large ISI noise)

SERDES

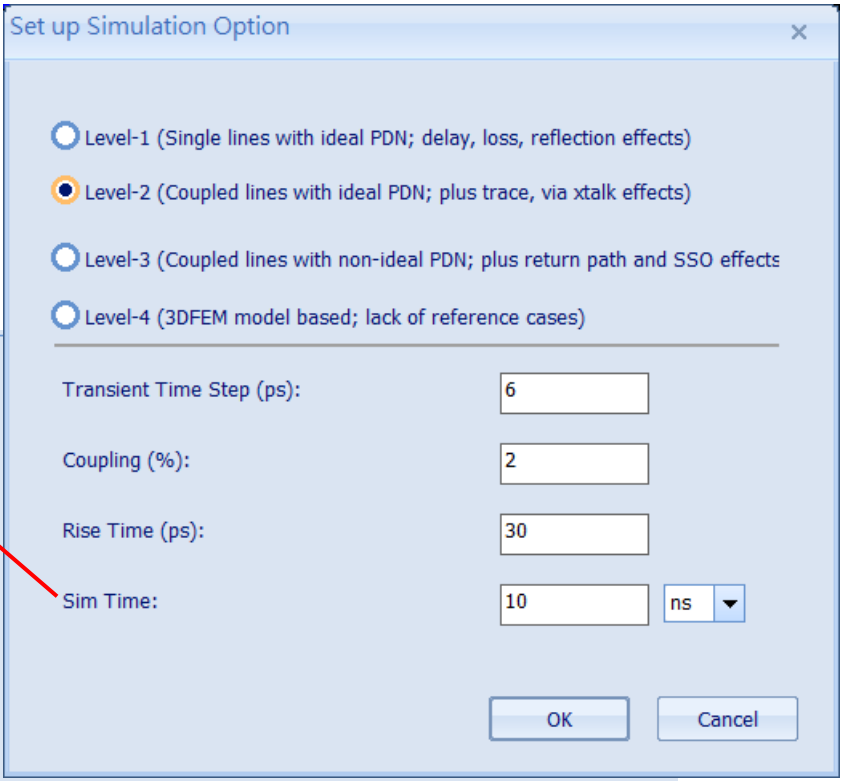


DDR, Single-ended

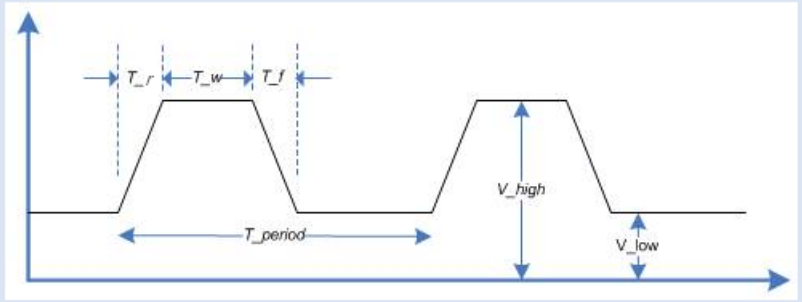


About SRC

20 ns is typical for SRC analysis whereas something shorter, 5 – 10 ns may be used for a quicker debug run.



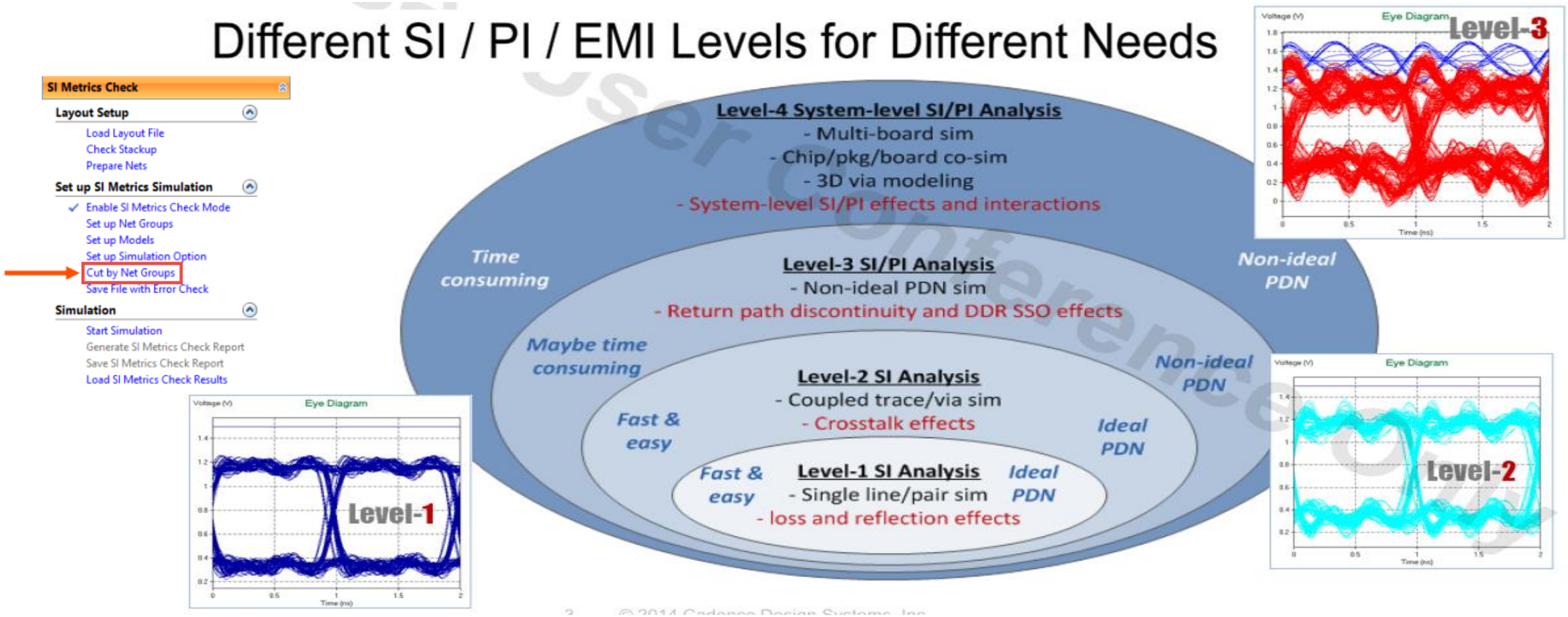
Set up Tx/Rx Models



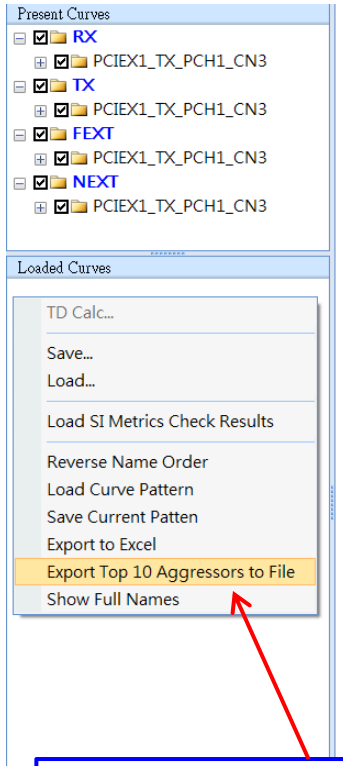
Import Tx/Rx Models Export Tx/Rx Models

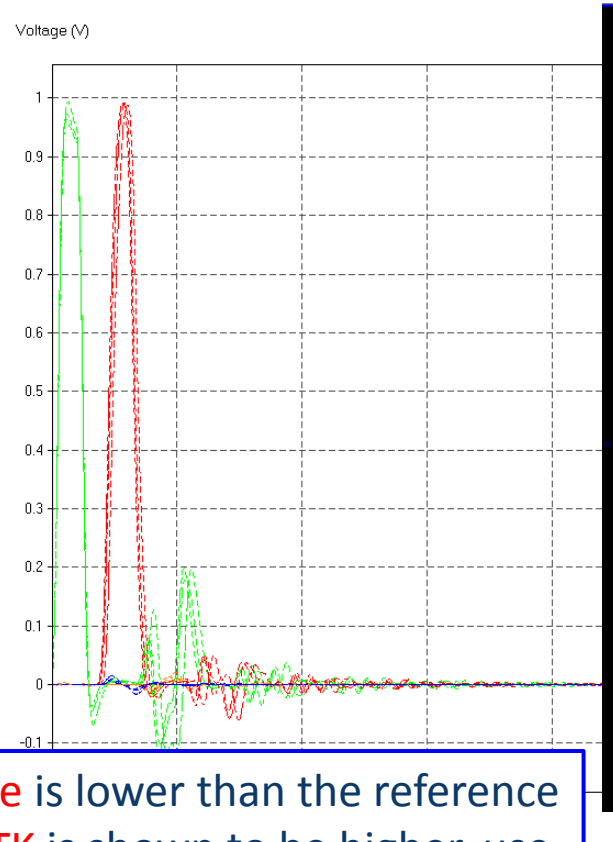
Interface and ckt type	Tx_term type	R(ohm)	C(F)	V_low(V)	V_high(V)	Tdelay	T_r(s)	T_f(s)	T_w(s)	T_period(s)	Rx_term type	R(ohm	C(F)	(S)Rx_term type	(S)R(ohm)	(S)C(F)
PCIEX1_RX:SE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PCIEX1_RX:Diff	**Parallel RC**	50	**1p**	0	**1**	0p	**60p**	60p	**140p**	1e+012p	**Parallel RC**	50	**1p**	-	-	-
PCIEX1_TX:SE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PCIEX1_TX:Diff	**Parallel RC**	50	**1p**	0	**1**	0p	**60p**	60p	**140p**	1e+012p	**Parallel RC**	50	**1p**	-	-	-

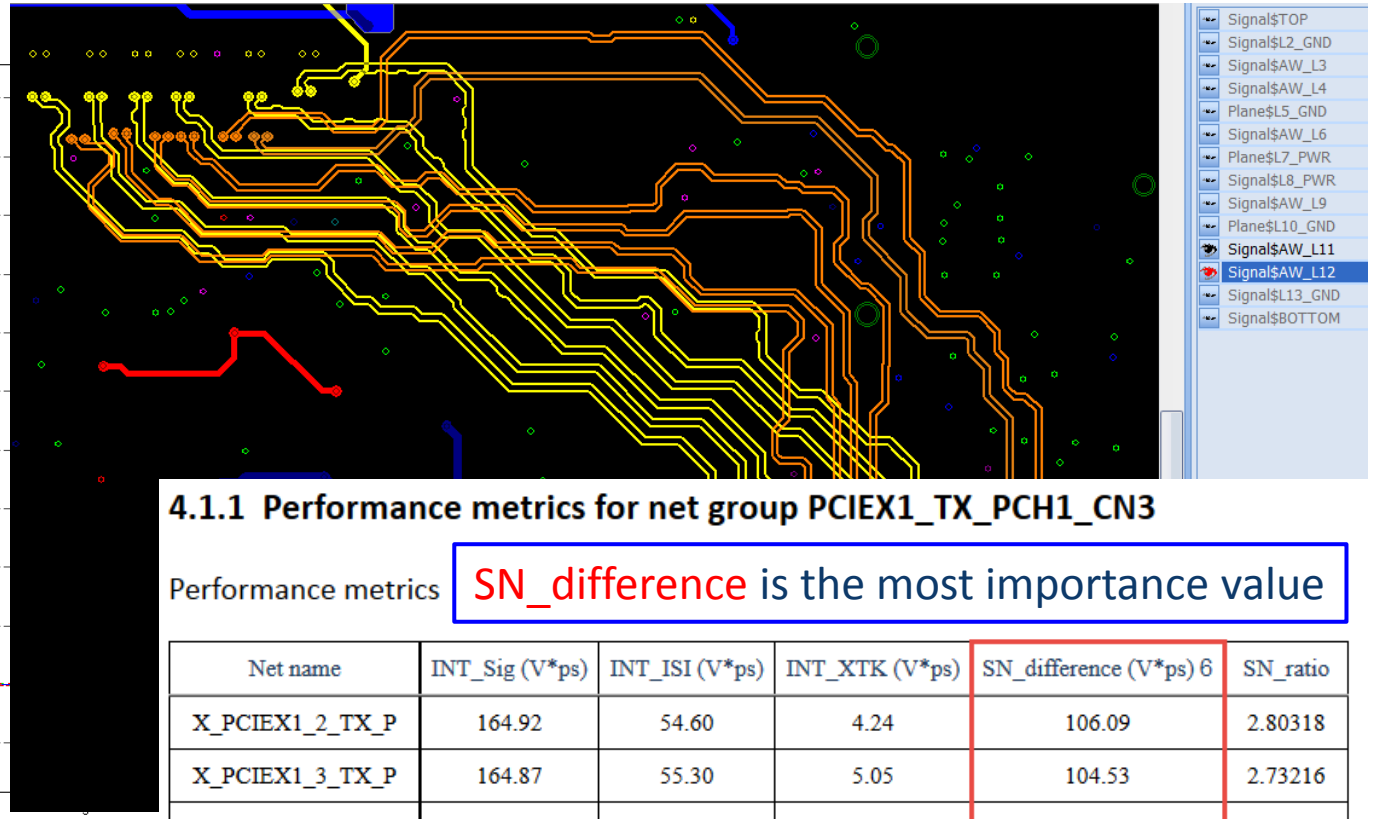
About SRC


Different SI / PI / EMI Levels for Different Needs
SI Metrics Check
Layout Setup
Load Layout File
Check Stackup
Prepare Nets
Set up SI Metrics Simulation
Enable SI Metrics Check Mode
Set up Net Groups
Set up Models
Set up Simulation Option
Cut by Net Groups
Save File with Error Check
Simulation
Start Simulation
Generate SI Metrics Check Report
Save SI Metrics Check Report
Load SI Metrics Check Results
Level-4 System-level SI/PI Analysis
- Multi-board sim
- Chip/pkg/board co-sim
- 3D via modeling
- System-level SI/PI effects and interactions
Time consuming
Non-ideal PDN
Level-3 SI/PI Analysis
- Non-ideal PDN sim
- Return path discontinuity and DDR SSO effects
Maybe time consuming
Non-ideal PDN
Level-2 SI Analysis
- Coupled trace/via sim
- Crosstalk effects
Fast & easy
Ideal PDN
Fast & easy
Level-1 SI Analysis
- Single line/pair sim
- loss and reflection effects
Ideal PDN
Eye Diagram
Level-3
Eye Diagram
Level-1
Eye Diagram
Level-2

About SRC







If SN_difference is lower than the reference and the INT_XTK is shown to be higher, use this file to quickly identify and mitigate XTK causes.

4.1.1 Performance metrics for net group PCIEX1_TX_PCH1_CN3

Performance metrics — SN_difference is the most importance value

Net name	INT_Sig (V*ps)	INT_ISI (V*ps)	INT_XTK (V*ps)	SN_difference (V*ps) 6	SN_ratio
X_PCIEX1_2_TX_P	164.92	54.60	4.24	106.09	2.80318
X_PCIEX1_3_TX_P	164.87	55.30	5.05	104.53	2.73216
X_PCIEX1_0_TX_P	162.16	60.84	2.66	98.66	2.55389
X_PCIEX1_4_TX_P	164.37	68.95	0.59	94.83	2.36362
X_PCIEX1_1_TX_P	163.37	60.27	9.45	93.65	2.34312
X_PCIEX1_5_TX_P	162.62	71.33	0.48	90.82	2.26478

About SRC

Using SRC for design that is “out of guideline”:

1. Check the layout by checking electrical performance instead of layout rules.

2. Locate the weakest signal(s) and fix it/them.

3. Check if the next revision of board does have improvement.

4. Understand the risk of current design based on other project(s).

5. Perform quick “what-if” type analysis on an actual implementation.

Good reference design selection:

1. Current version of the design

2. An exiting working design

Abstract

- Overview
- ERC (Electrical Rule Check)
- SRC (Simulation Rule Check)
- **Applications**
- Summary

Applications

With easy setup and fast simulation, ERC enables practical first-order screening of electrical issues before handing off to SI experts for final check.

- ERC → SRC → Simulation:

✓ Use ERC to screen layout and identify the worst case for further SRC or SI analysis

✓ Use SRC to evaluate the SI impact of design rule violations and investigate tradeoffs

- SRC → ERC:

✓ Use ERC to find out how to fix SI problems shown in SRC or SI simulations

- Compare ERC and SRC results with known-good reference design and the part of the design that has been fully analyzed.

Applications

General SI Simulation	Trace Impedance/ Coupling Check	SI Performance Metrics Check	DDR Simulation	Time-domain PDN Simulation
Mainstream SI *L1/L2 for fast sim* Easy to setup; Sim runs fast Waveforms & measurements	Geometry based Trace impedance, coupling & reference check for entire board or net groups Results tables; Results plots; Layout overlay; Layout x-probing	Simulation based *L1/L2 for fast sim* *L3 for non-ideal PDN* Loss, reflection, xtalk check, typically by net groups Waveforms; Xtalk v_max & v_min	Layout-based DDR simulation *L1/L2 for fast sim* *L3 for SSO* No s-parameter model needed for on-board DRAMs Waveforms & measurements	Layout-based TD PDN sim PDN chip-pkg-board co-sim with *-Voltus die mode* *- XcitePI IO model with die grid* Voltage / current distributions; dynamic noise propagation

Potential power noise path check (Treat target power as signal and use SRC):

→ A 3-pin “Source” should be created at the source of the potential noise. Typically at the output of the Voltage Regulator Module (VRM) inductor.

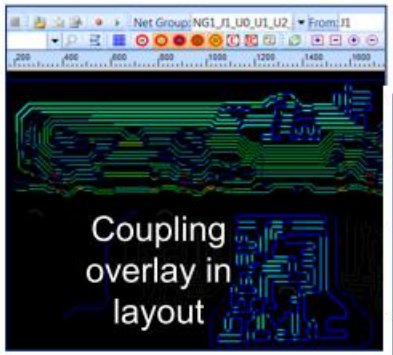
→ A 3-pin “Sink” should be created where the current will be consumed.

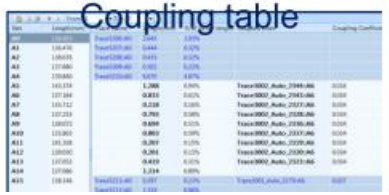
→ These devices will be used as transmit and receive components in the Net Group setup page.

Abstract

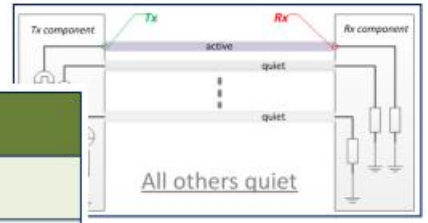
- Overview
- ERC (Electrical Rule Check)
- SRC (Simulation Rule Check)
- Applications
- **Summary**

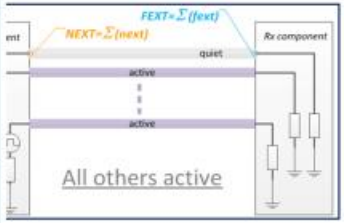
Summary

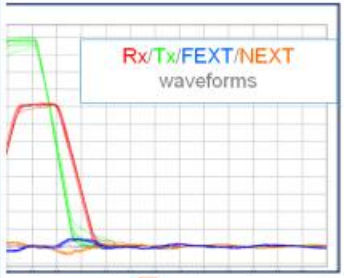




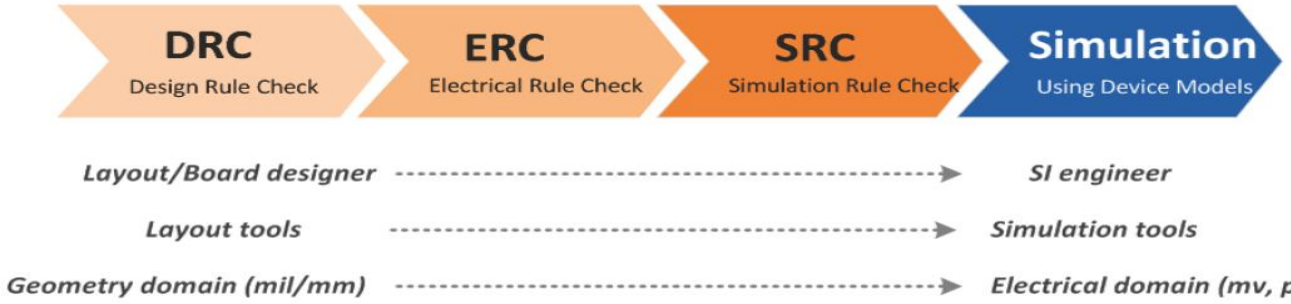
	ERC Electrical rule check	SRC Simulation rule check
	Trace Impedance/Coupling Check	SI Metrics Check
	Geometry-based	Simulation-based
	Micro, individual, segment-level view (coupling %, Ω & mm)	Macro, combined net-level, view (mv & ps)
	Options Check all nets Check selected nets Check nets in net groups	Options Level-1 simulation Level-2 simulation Level-3 simulation
	Results Coupling coefficient Impedance Trace reference Summary & detailed tables Expanded & collapsed plots Layout overlay Layout cross probing HTML report	Results Waveforms: Tx / Rx / NEXT / FEXT v_min & v_max SI performance metrics HTML report







Summary



- DRC's alone cannot validate the interconnects electrical characteristics.

– Examples: signals crossing split or different reference planes causing impedance changes.

- ERC: Segment-level view to shows why low performance happened and how to fix it .

- SRC: Net-level view to shows what happened and its effect on performance.

- ERC/SRC designed for use by the PCB layout designer, not the signal integrity (SI) expert.

– SI Expert can focus on other complex problems such as "**stackup design**", "**design guide creation**", "**constraint setting**", "**risk assessment proposal**", "**design improvement**", "**suggestion/solution/explanation for customers**".

– The possibility in catching something which might be missed in the traditional layout review is valuable, which may decrease the effort in the validation phase.


ADLINK
TECHNOLOGY INC.