# Accelerate your Power Delivery Network Simulation Analysis

**Nick Chiu**

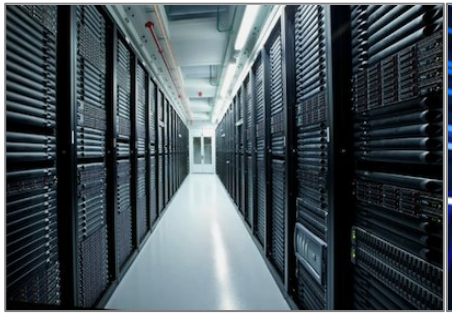
July, 2016

# > COMPANY FACTS


| | |
|---|---|
| Established Date : | May 3rd, 1996 |
| Company Founder/ CEO : | Michael Liang |
| HQ Address : | No. 152, Section 4th, Linghang N. Road ,<br>Dayuan District, Taoyuan city 337, Taiwan |

# >COMPLETE PRODUCT LINES FOR VARIOUS MARKETS

## Target Vertical Markets

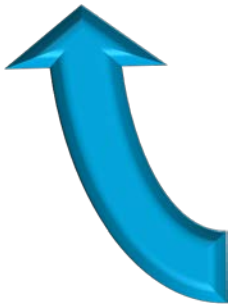


Cloud Data Center

Networking Security

Broadcasting

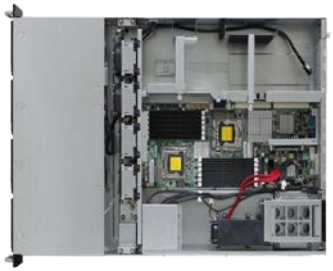
Industrial PC



Storage Solution

Rackmount Enclosure

Server Barebone



Storage Controller Design

Server Board Design

# Outline

- DC IR-drop Analysis Solutions
- Integrated DC Solutions
- Integrated AC Solutions
- Case Improved efficiency compared
- Summary

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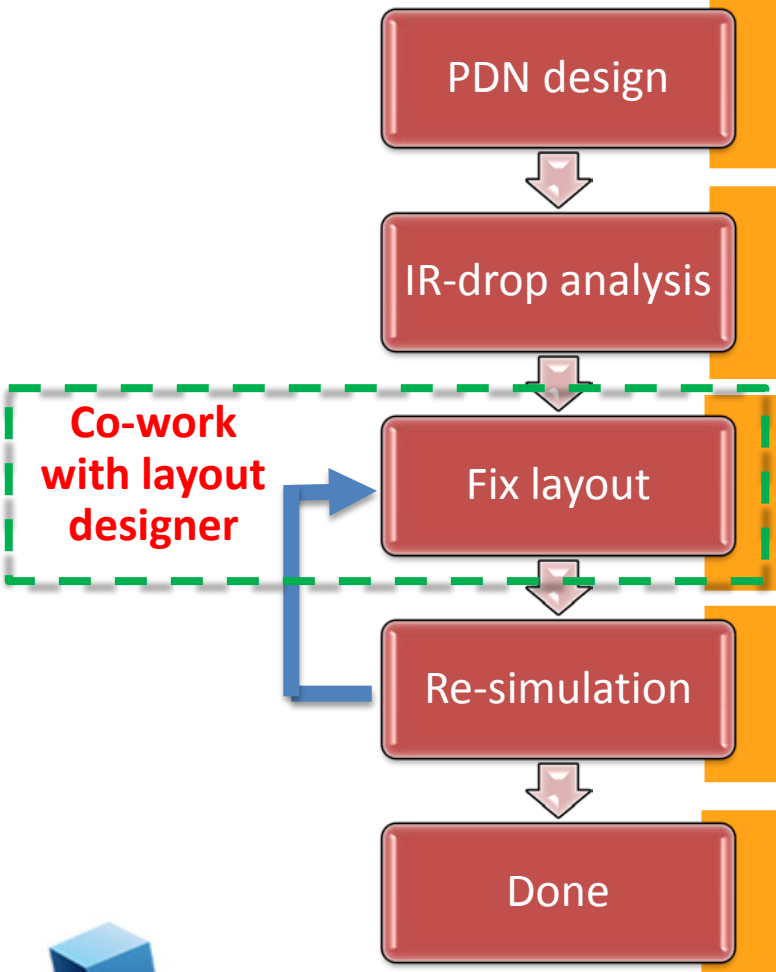
# DC IR-drop Analysis Solutions

## DC IR-drop design flow




- Following IPC specifications, considered a temperature rise to calculate current carrying capacity need copper cross-sectional area and via hole size.
- Check power consumption meet requirements

- PWR/GND nets classification
- Set up VRMs, Sinks, Discretes
- Set up Thermal parameters

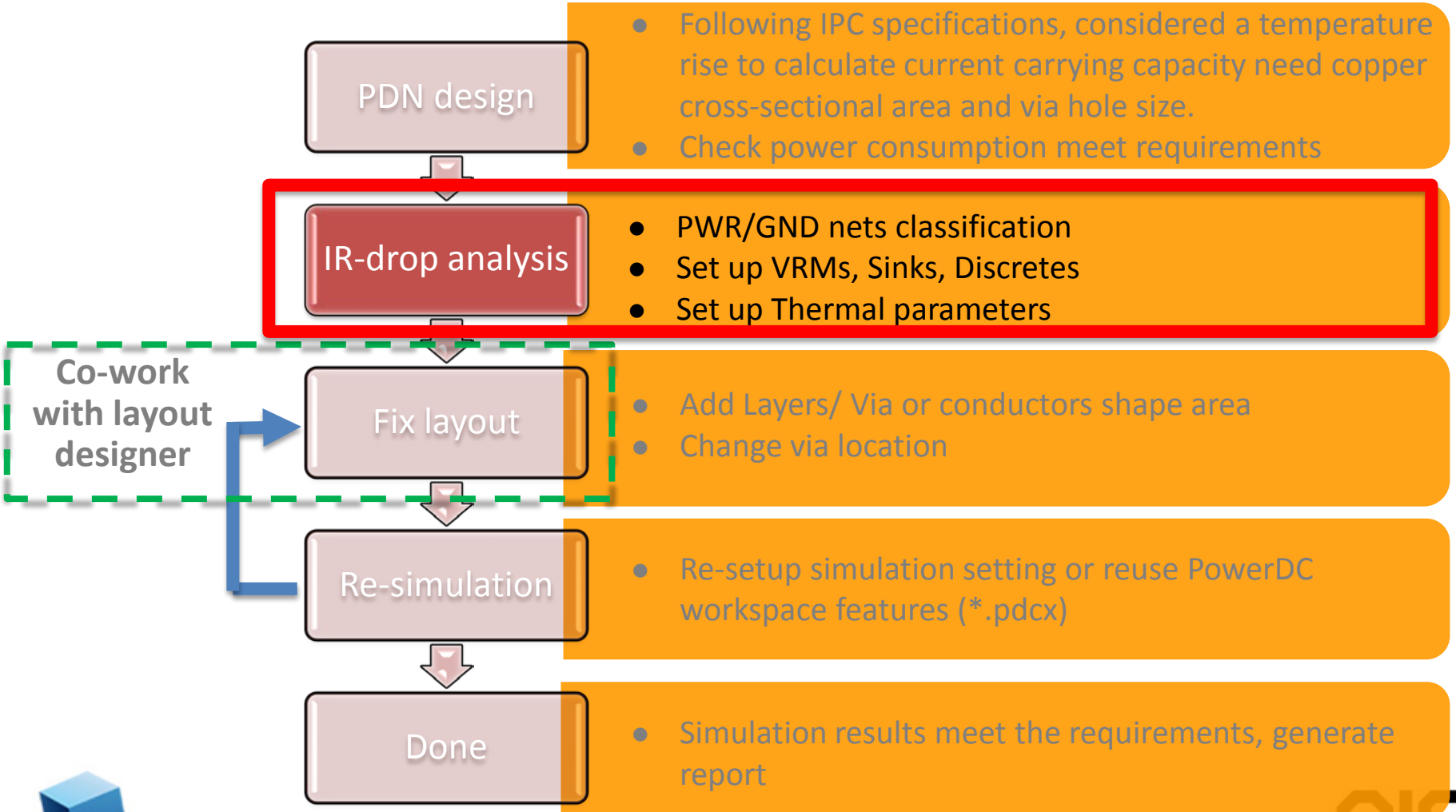
- Add Layers/ Via or conductors shape area
- Change via location

- Re-setup simulation setting or reuse PowerDC workspace features (*.pdcx)

- Simulation results meet the requirements, generate report

# DC IR-drop Analysis Solutions

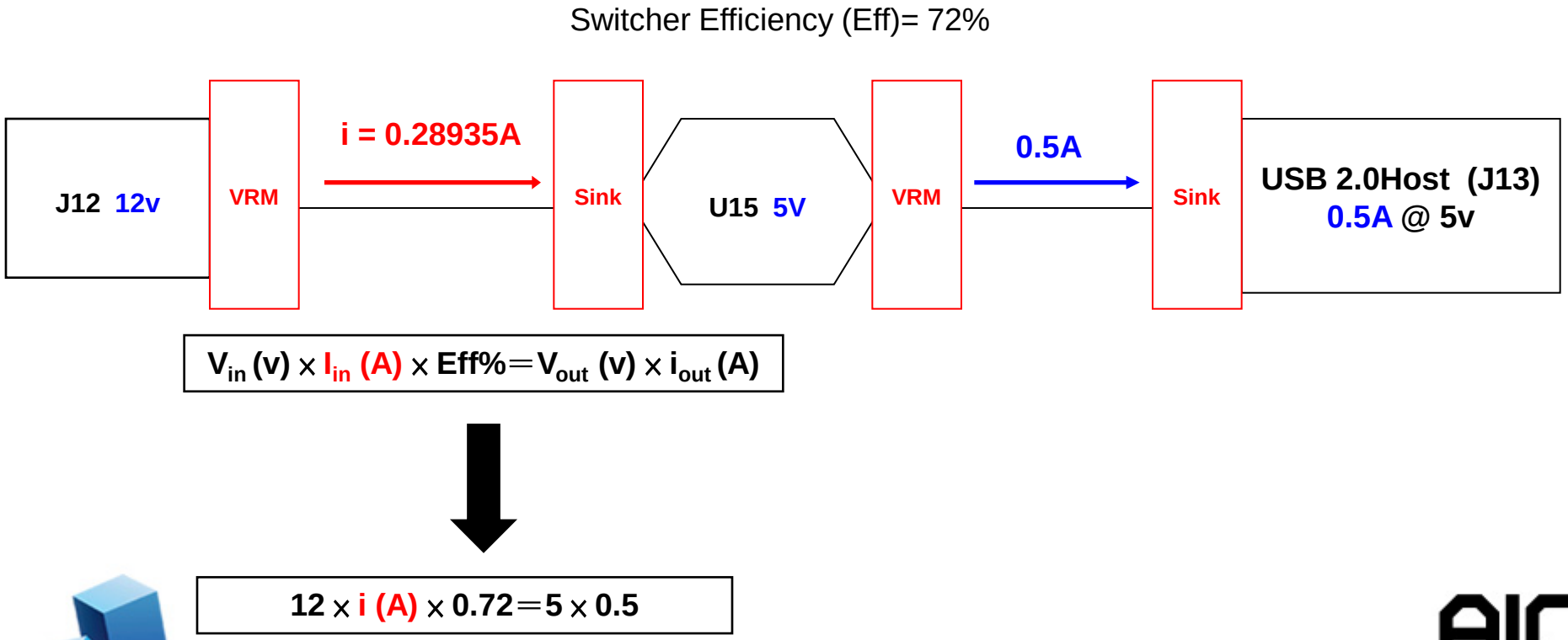
## Initial DC analysis



# DC IR-drop Analysis Solutions

## Your DC analysis is correct in setup?

- Set up VRMs, Sinks device and sense pin.
- Relationship of voltage switch and interconnect.

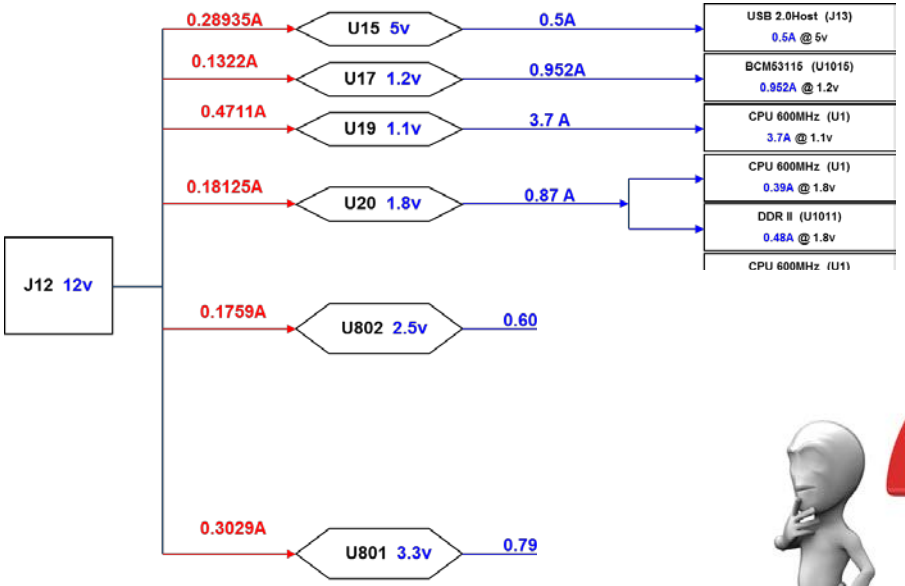


# DC IR-drop Analysis Solutions

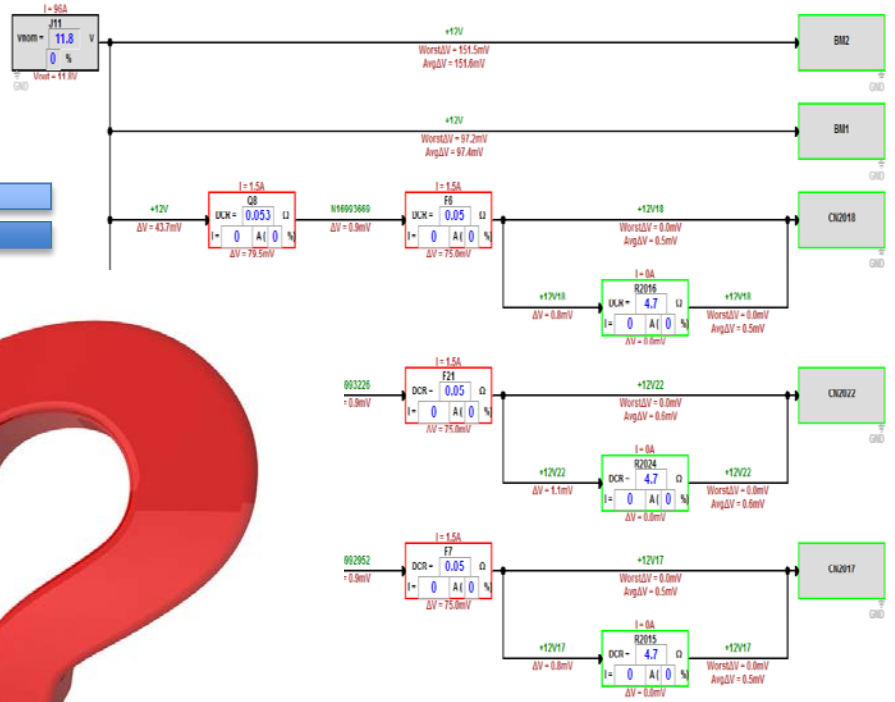
## Your DC analysis is correct in setup?

- Correct DC block diagram in simulation.

Your DC Analysis Block Diagram

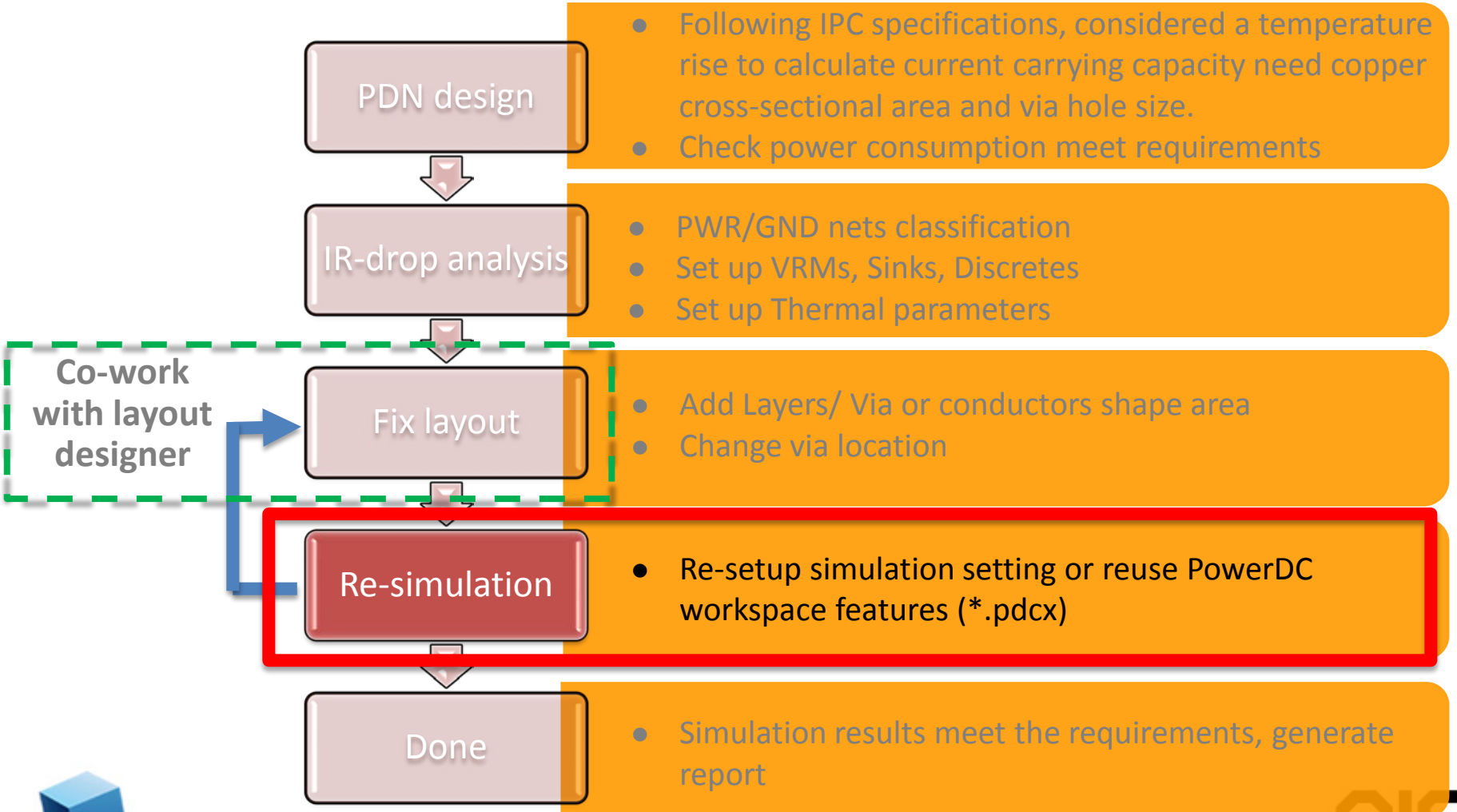



DC Analysis Block Diagram simulation result



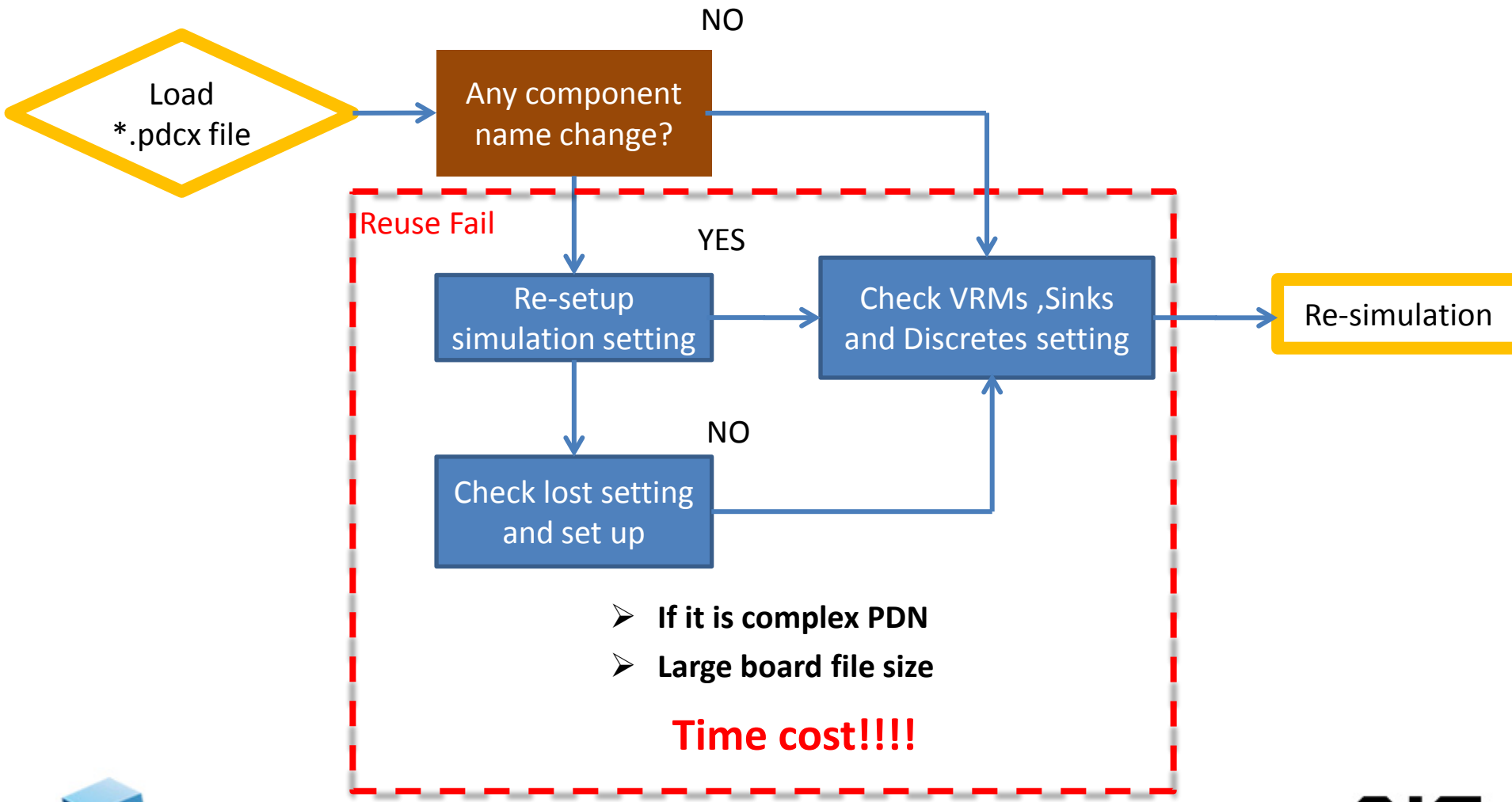
# DC IR-drop Analysis Solutions

## Re-simulation



# DC IR-drop Analysis Solutions

## Reuse PowerDC workspace feasibility?



# DC IR-drop Analysis Solutions

## When complex Power Delivery Network Simulation Analysis…

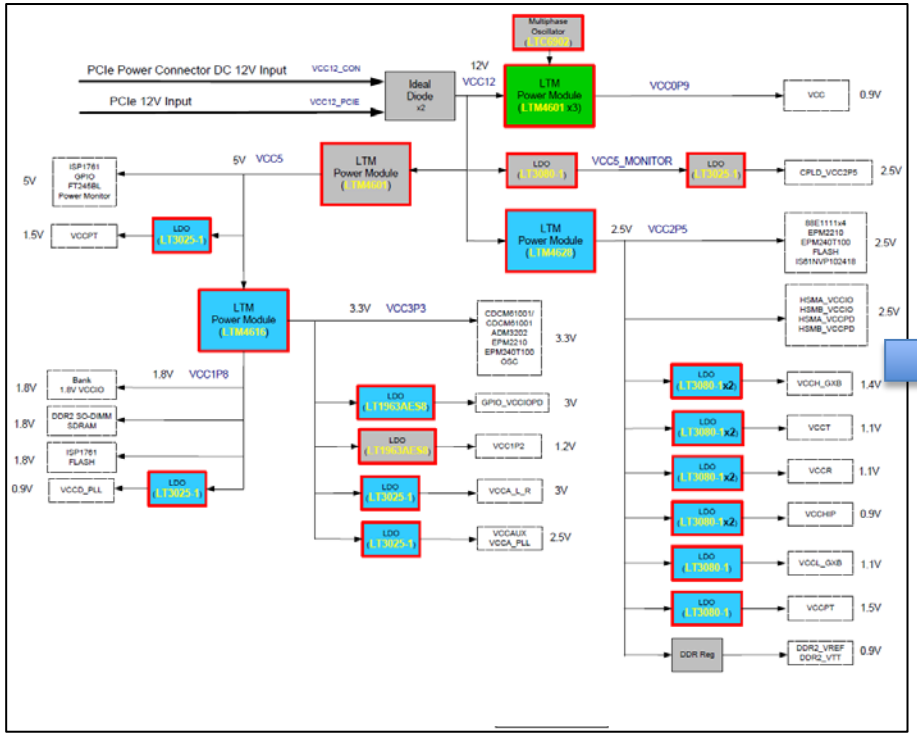
- Complicated set of VRMs and Sinks.
- Power rail interconnections
- Correct DC analysis block diagram
- Reuse PowerDC workspace features

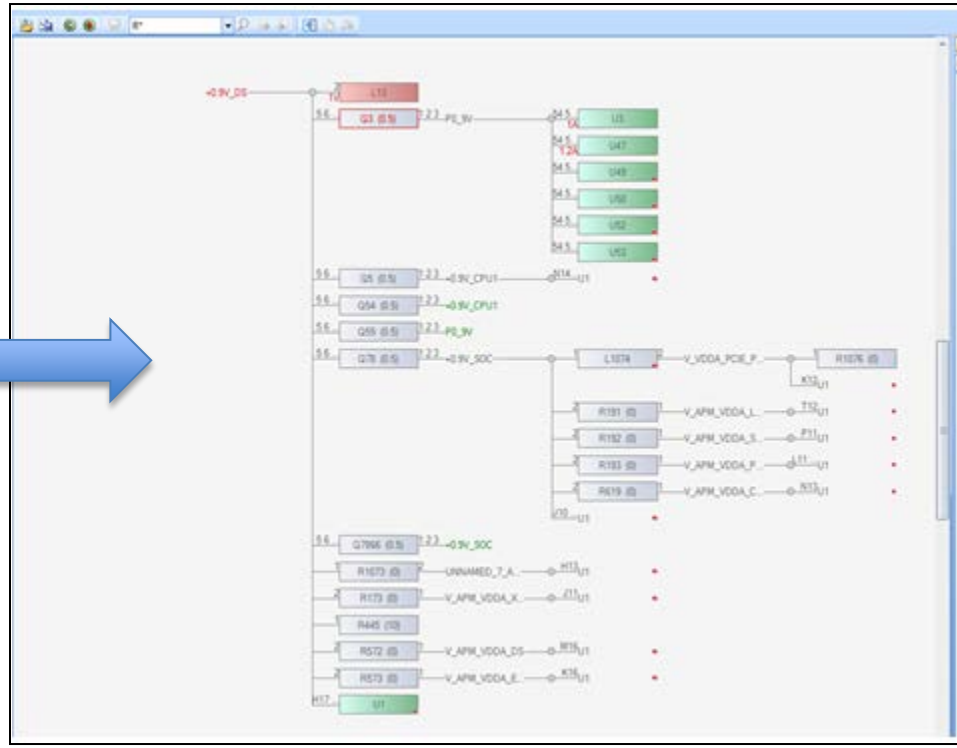
**Spend the most time of DC analysis and correct simulation confirmed**

# DC IR-drop Analysis Solutions

## Power Tree concept

- Describe on your PDN block diagram



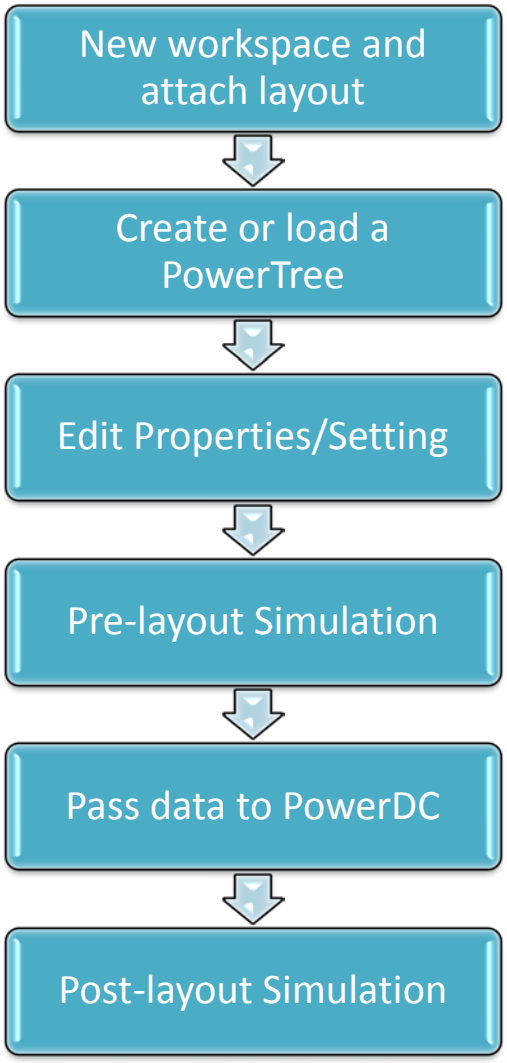
# DC IR-drop Analysis Solutions

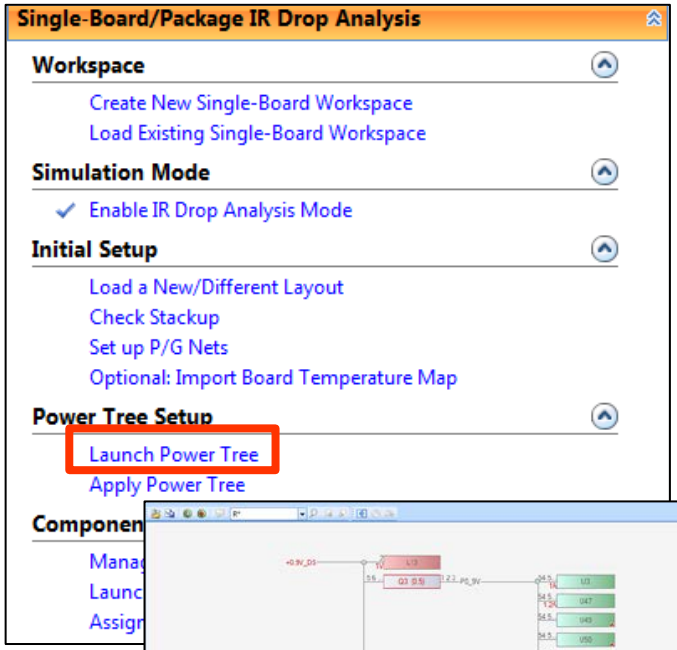
## What's Power Tree can help?

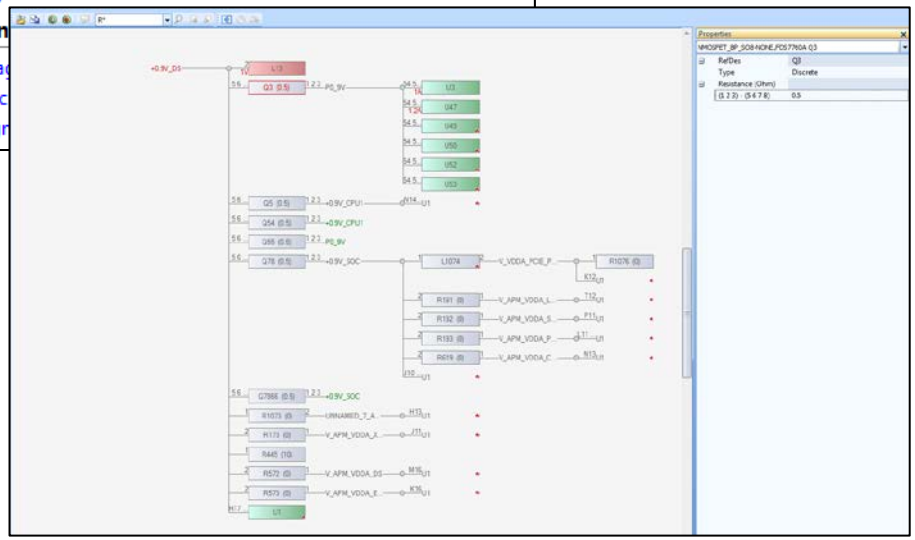
- Power Tree is a tool for early power estimation
- Power Tree is a visualization tool for the schematic data
- Power Tree is used to extract power topologies from net list
- Power Tree is used to help setting automation
- Power Tree is used to help setting reuse

# DC IR-drop Analysis Solutions

## Power Tree Based DC Auto Setup Flow



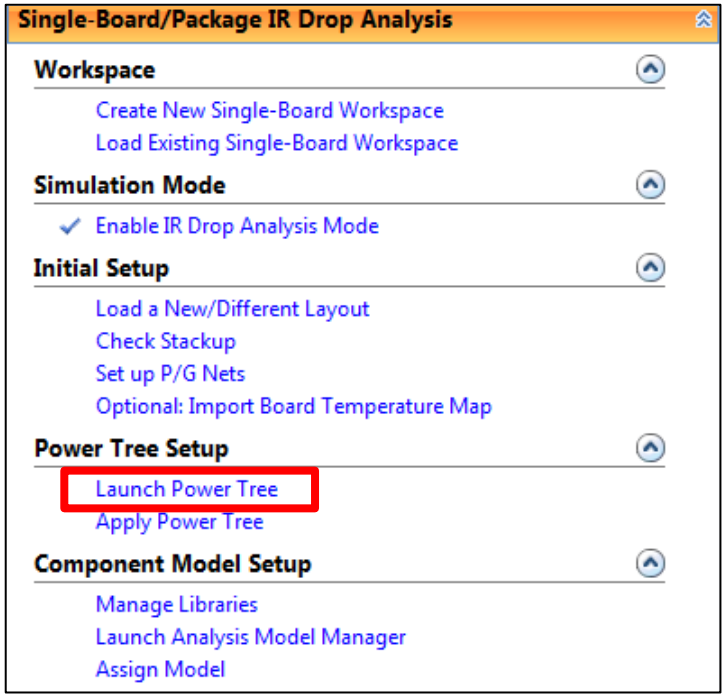



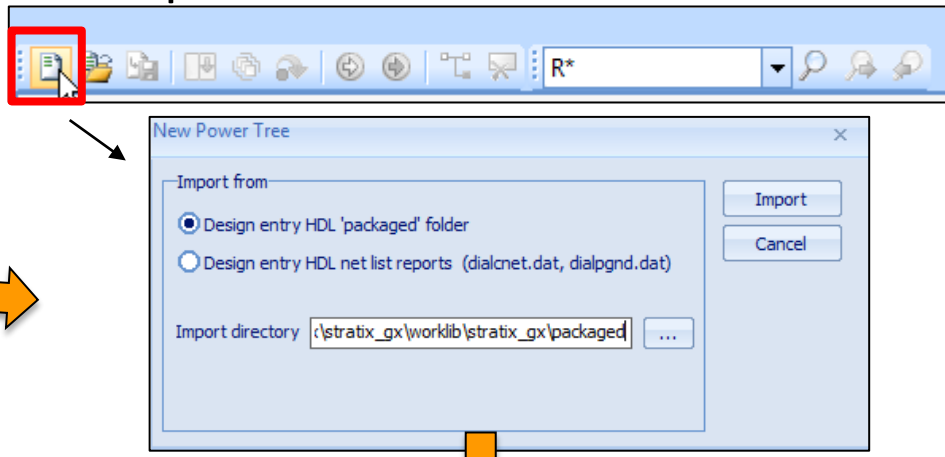
# DC IR-drop Analysis Solutions

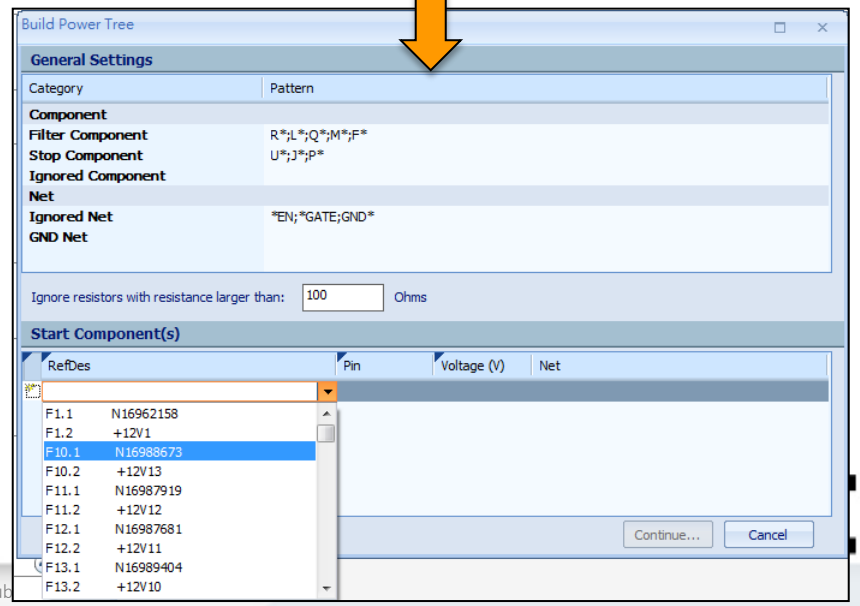
## Power Tree Generation

- "Launch Power Tree" in workflow




- Import netlist files



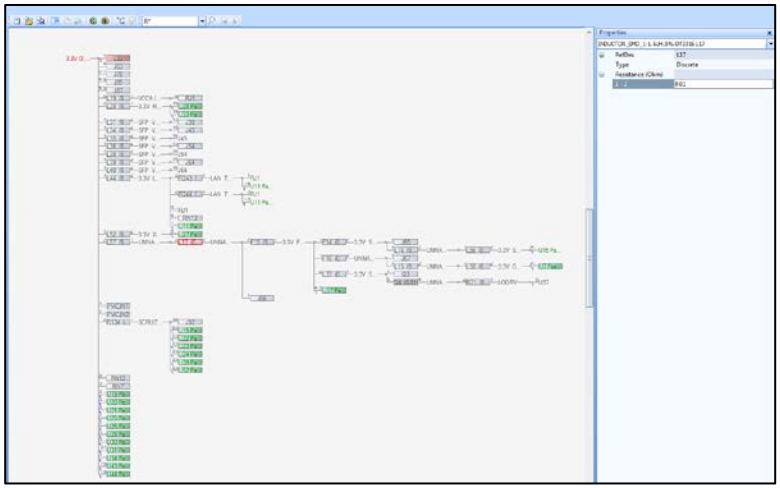



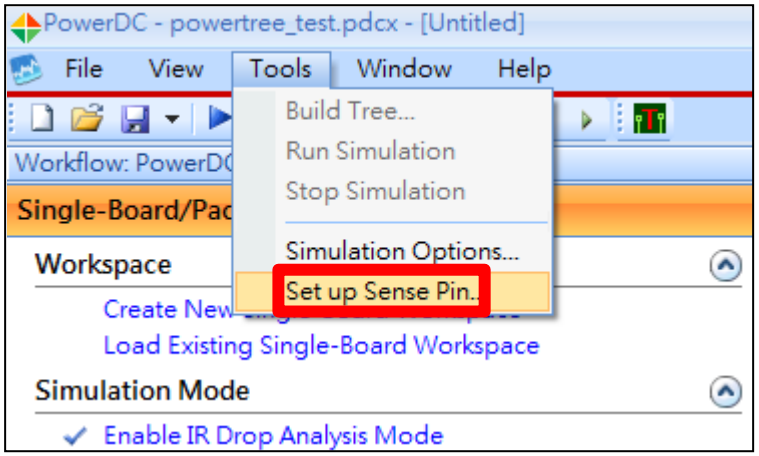

- Pick the starting component pin
- Select through pins for through components if any

# DC IR-drop Analysis Solutions

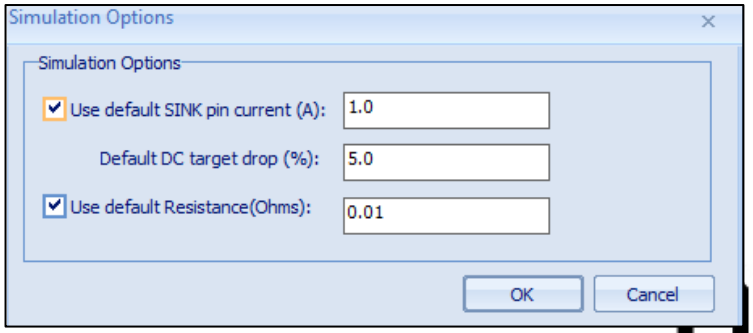
## Property Editing in Power Tree

- Double click a component to edit properties
  - Sink current/discrete comp resistance/sense pin





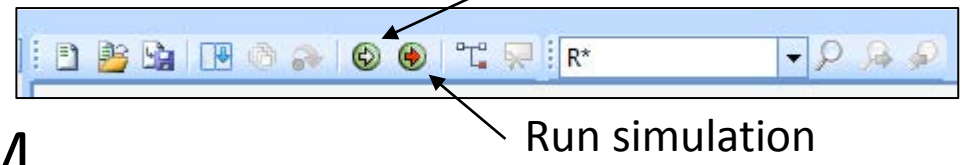

- Default settings for all others
  - Tools->Simulation Options…

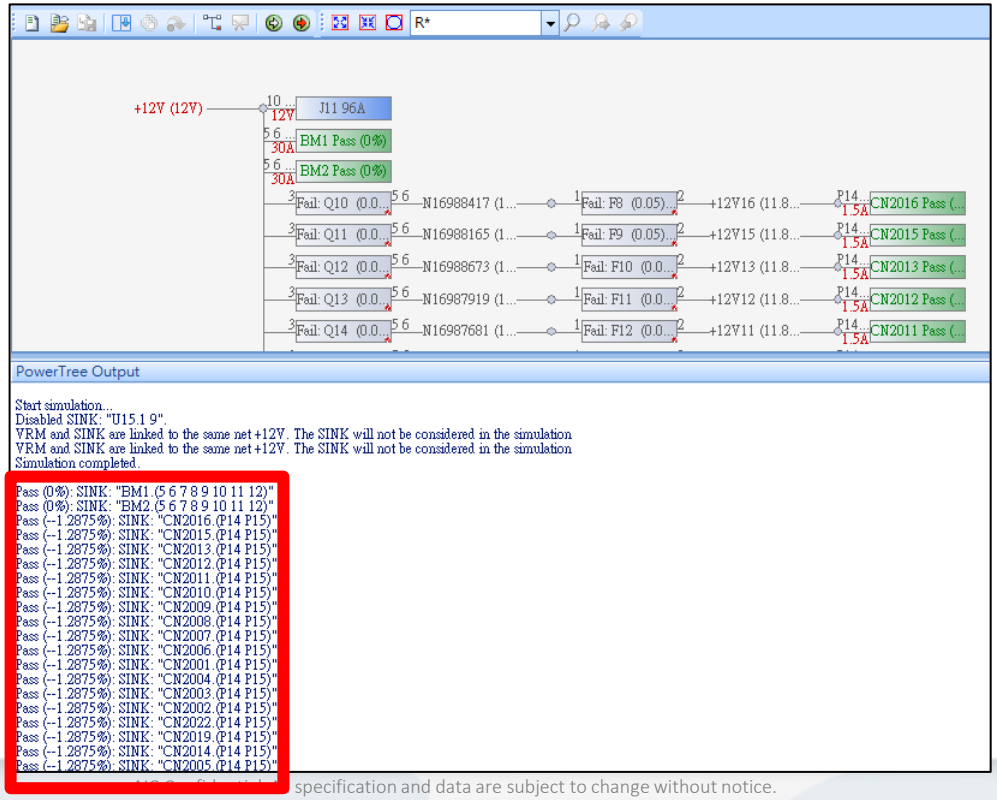


# DC IR-drop Analysis Solutions

## DC Analysis in Power Tree (Pre-simulation)

- Results will mark on the power tree
- Check discrete current
- Check total current for VRM

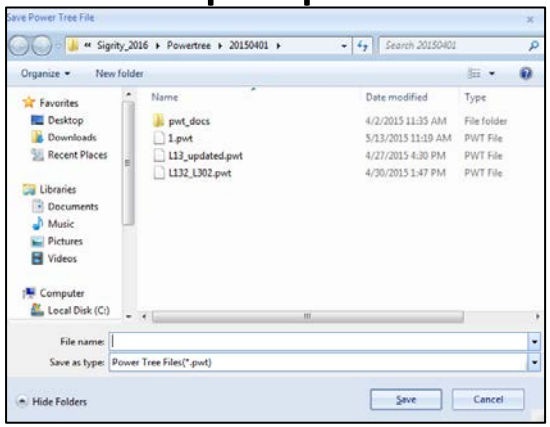


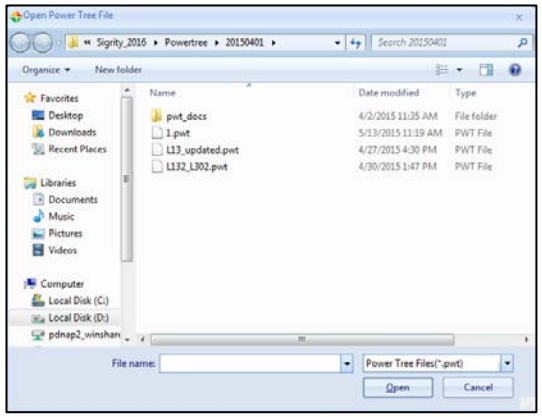
# DC IR-drop Analysis Solutions

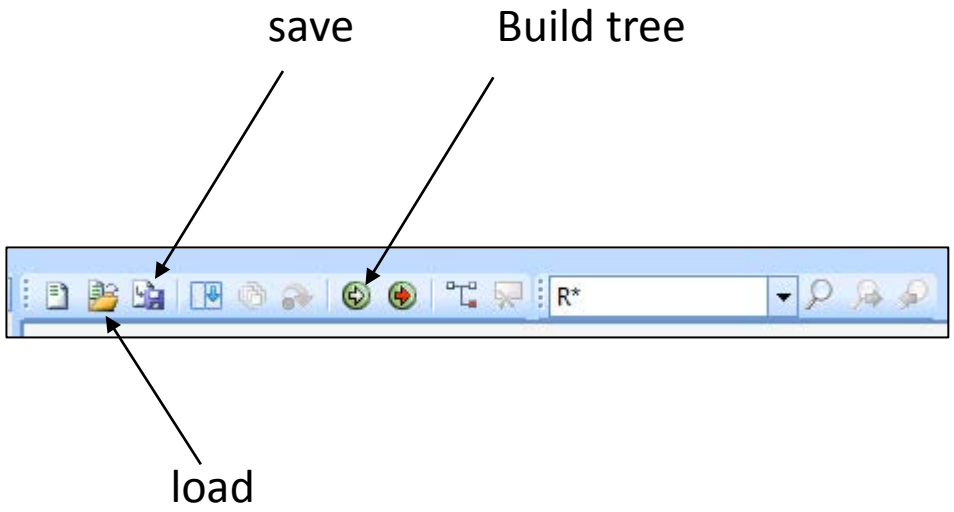
## Save/Load Power Tree Files

- Save a power tree file
  - Both properties and topologies are saved




- Load a power tree file

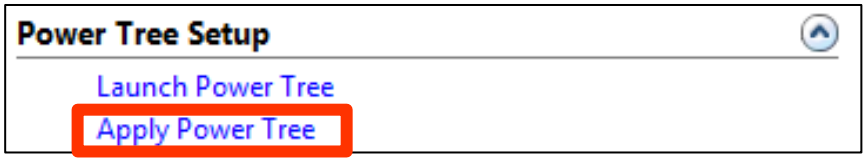


# DC IR-drop Analysis Solutions

## Pass Power Tree Data to PowerDC

- Attach layout to PowerDC
  - Matching with the schematic (Power tree)
- “Apply PowerTree” in workflow
- Select proper ground nets
- After the assignment, check workspace



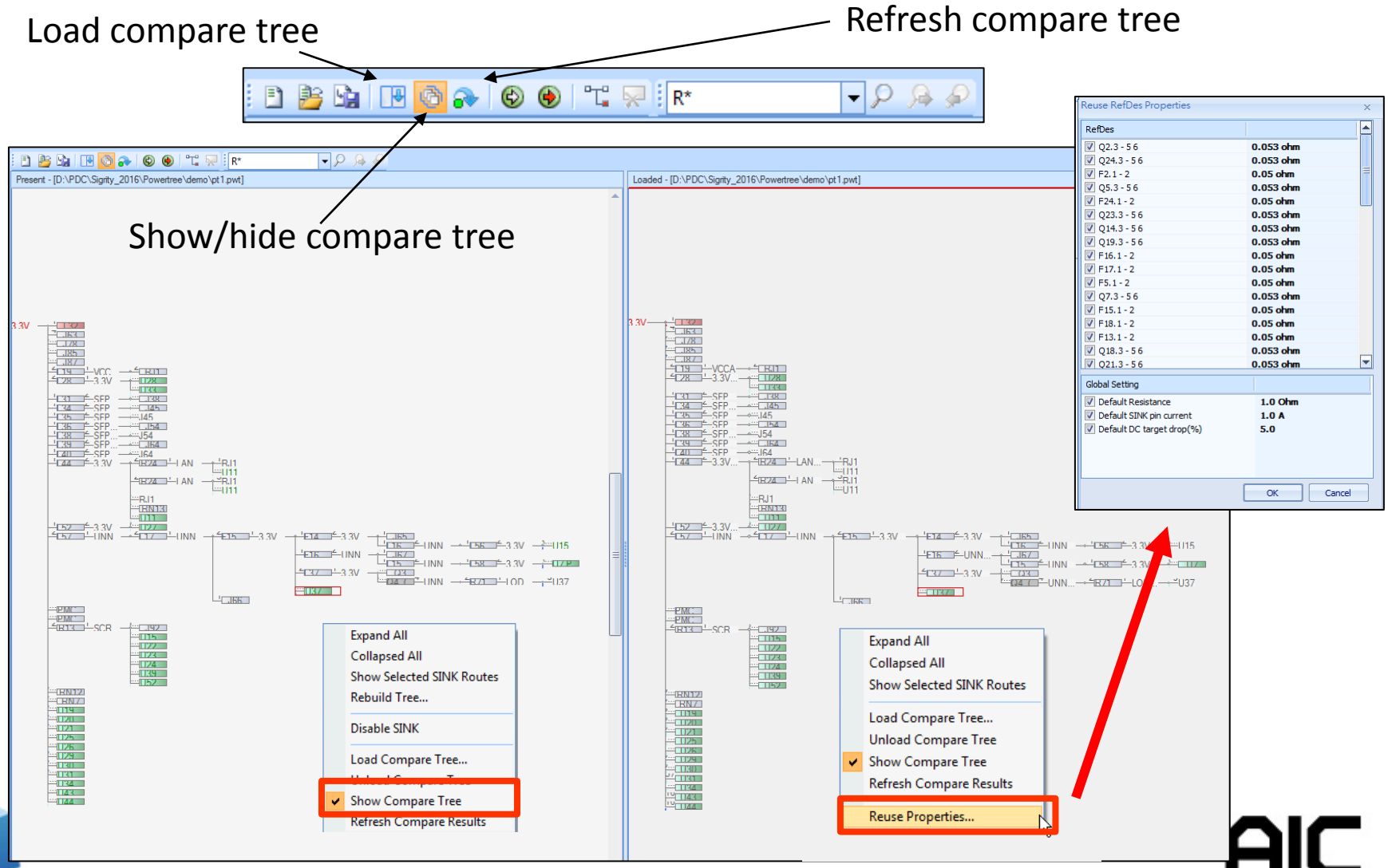

Voltage Drop Analysis Setup -> Set up Sinks

Assign | Tolerance Unit: %

| | Sink Name | Model | Nominal Voltage (V) | Power/Ground Net | Upper Tolerance(+%) | Lower Tolerance(-%) | P/F Mode | Current (A) | Cu |
|---|---|---|---|---|---|---|---|---|---|
| ☑ | SINK_U30_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U31_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U34_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U43_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U44_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U28_3_3V_R... | Equal Current | 3.3 | 3_3V_RS232_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U33_3_3V_R... | Equal Current | 3.3 | 3_3V_RS232_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U20_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U19_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |
| ☑ | SINK_U21_3_3V_GND | Equal Current | 3.3 | 3_3V_GND | 5 | 5 | Average | 1 | |

# DC IR-drop Analysis Solutions

## Compare Two Power Trees



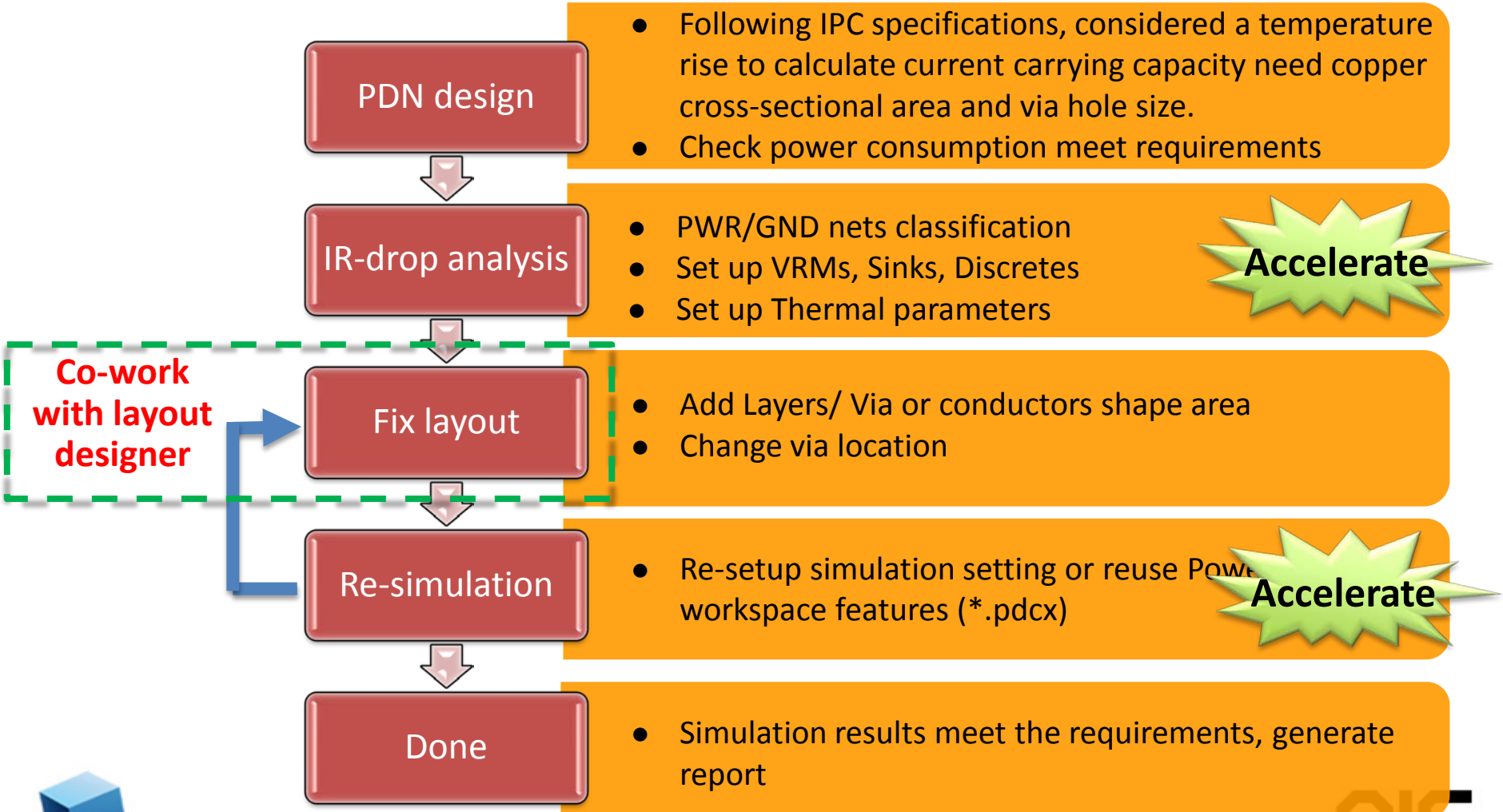
# DC IR-drop Analysis Solutions

## What Power Tree Will Do?

- Power topology extraction from schematic data in graphic diagrams
- Editing/creating properties in Power Tree
- Help to select/group proper power/ground nets analysis
- Circuit simulation in Power Tree
- Passing properties from PowerTree to PowerDC for settings reuse
- Saving/Loading Power Tree
- Comparing two Power Trees
- Auto net classification

# DC IR-drop Analysis Solutions

## Power Tree Accelerate



# DC IR-drop Analysis Solutions

## Using Power Tree acceleration

- In complex PDN for ten power rail simulation analysis

| DC IR-drop analysis | Item | Not used | Using Power Tree | Features |
|---|---|---|---|---|
| IR-drop analysis | Set up VRMs, Sinks, Discretes, Sense pin | 60 min | 30 min | Extract power topologies from netlist and circuit simulation (setting automation) |
| | Interconnections | 10 min | | |
| | Check DC analysis block diagram | 10 min | | |
| Re-simulation | Reuse PowerDC workspace | 20 min | 10 min | Compare Two Power Trees |

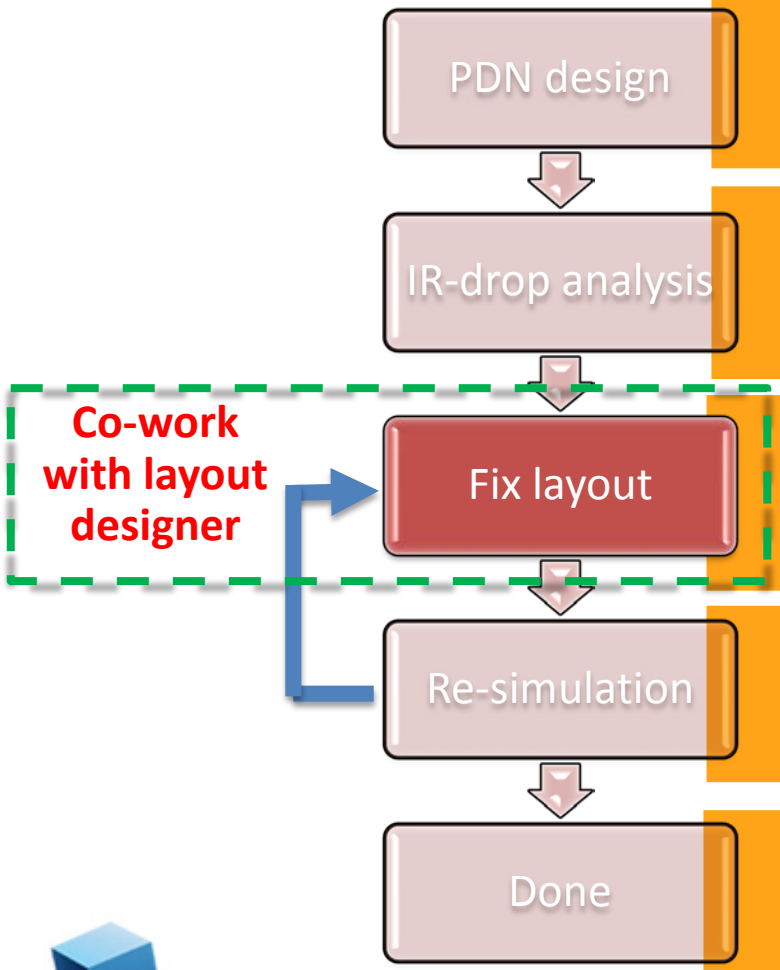
**Reduce half the time costs ⬇**
**Simulation correctness ⬆**

# Outline

- Challenges for PCB Designers
- DC IR-drop Analysis Solutions
- Integrated DC Solutions
- Integrated AC Solutions
- Case Improved efficiency compared
- Summary

# Integrated DC Solutions

## Innovative Solution for PCB Designers and PI Engineers




- Following IPC specifications, considered a temperature rise to calculate current carrying capacity need copper cross-sectional area and via hole size.
- Check power consumption meet requirements

- PWR/GND nets classification
- Set up VRMs, Sinks, Discretes
- Set up Thermal parameters

Accelerate

- Add Layers/ Via or conductors shape area
- Change via location

- Re-setup simulation setting or reuse Pow workspace features (*.pdcx)

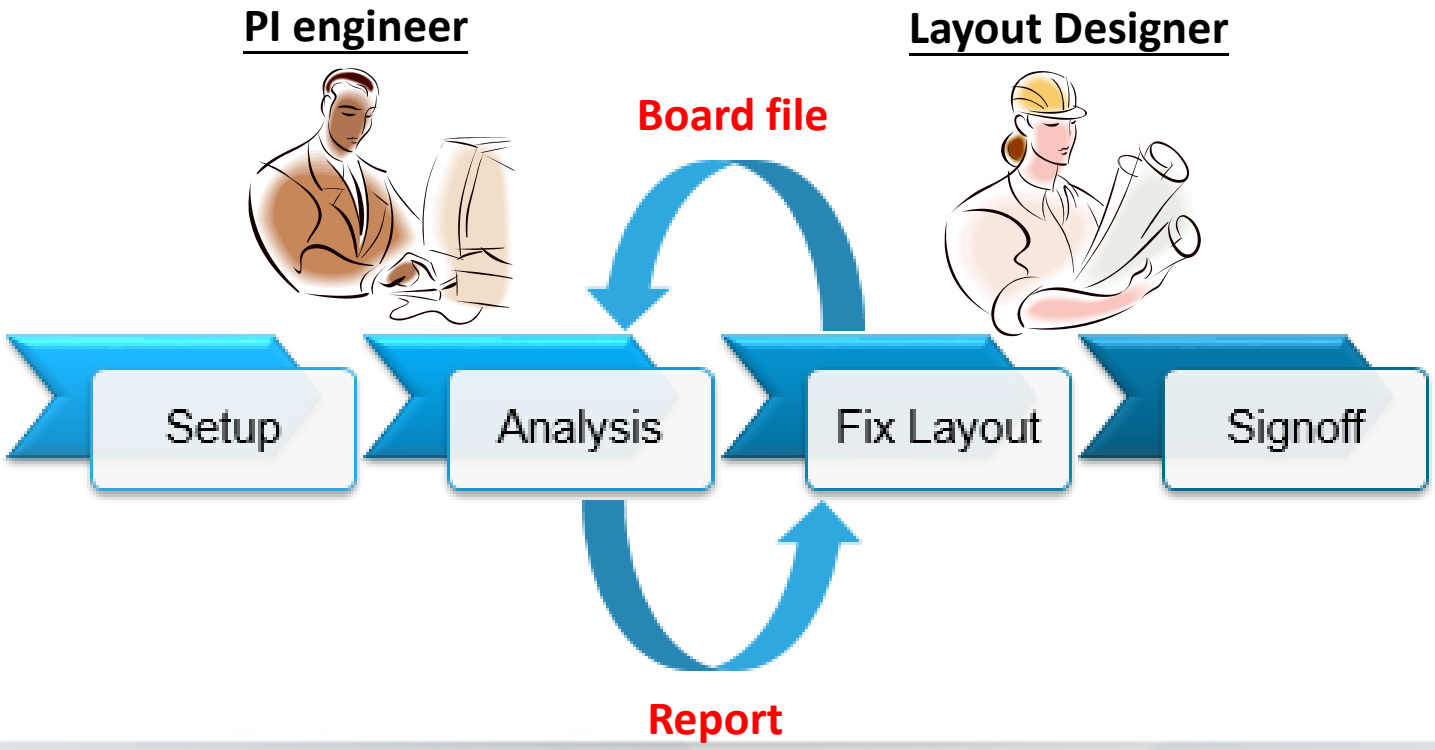
Accelerate

- Simulation results meet the requirements, generate report

# Integrated DC Solutions

## Co-work with layout designer

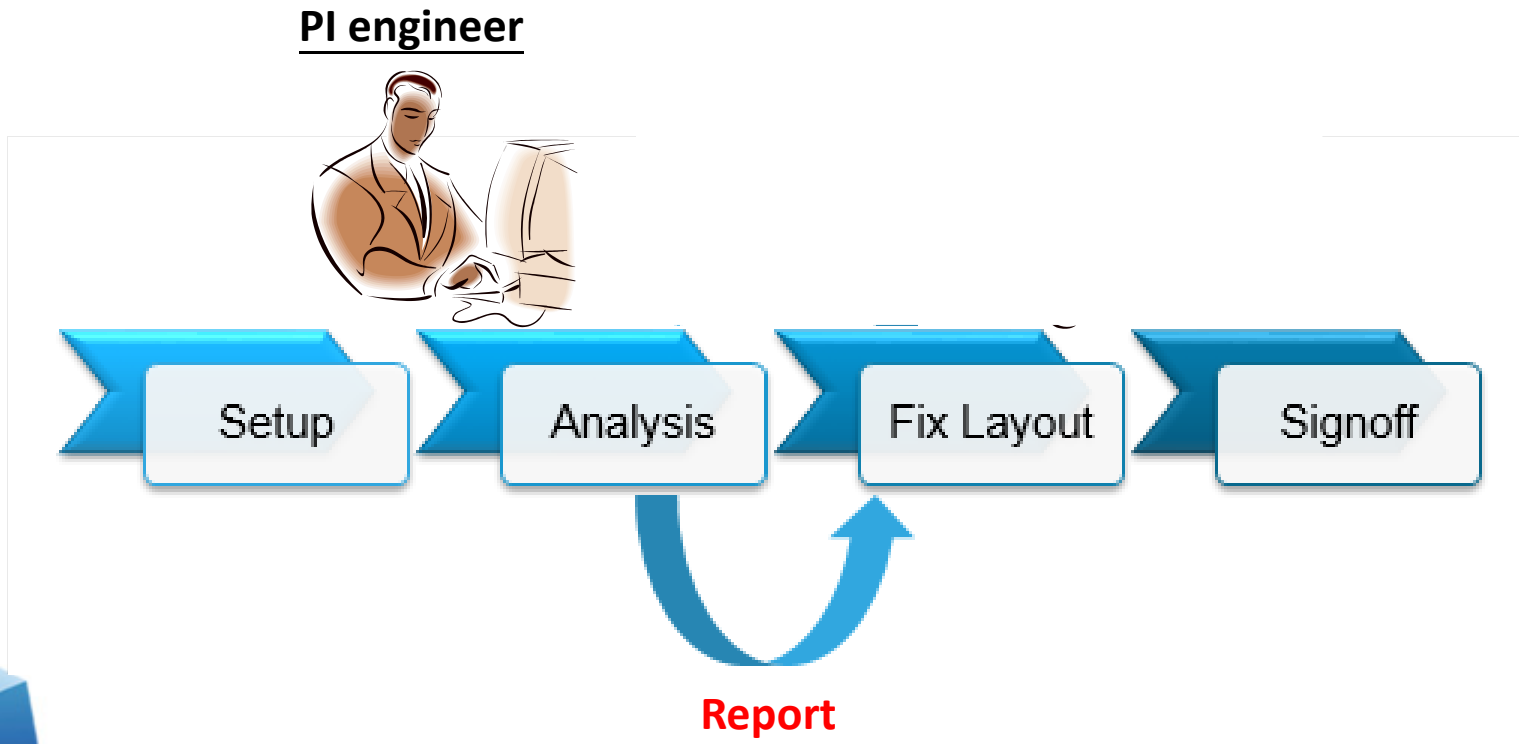
- For typical enterprise customers, the DC design and analysis flow is as below
  - Communication and efficiency issue



# Integrated DC Solutions

## Gap in layout modify

- After modified board file need to verification simulation.
- Modified board gap with the PI engineer suggestion.



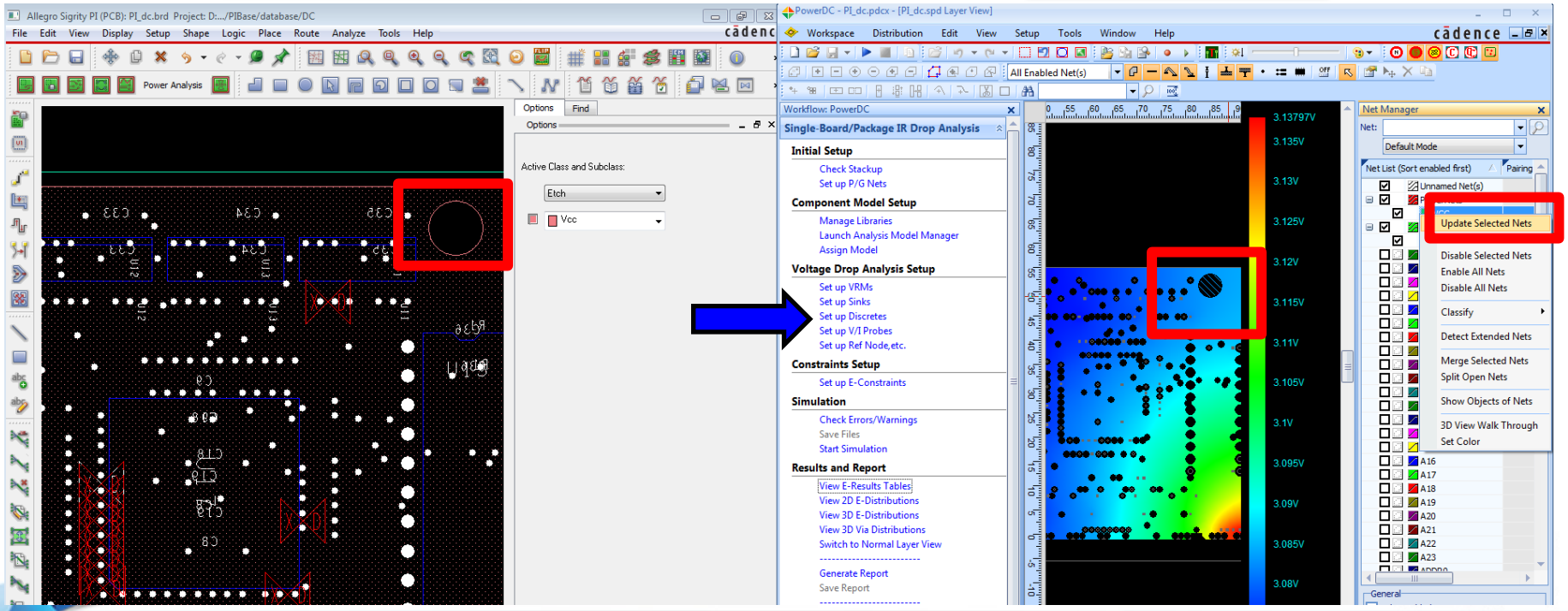
# Integrated DC Solutions

## Cross probing between layout design and analysis results

- Layout incremental update support
- Allegro layout change is dynamically updated to PDC-Lite
  - Update Selected Nets

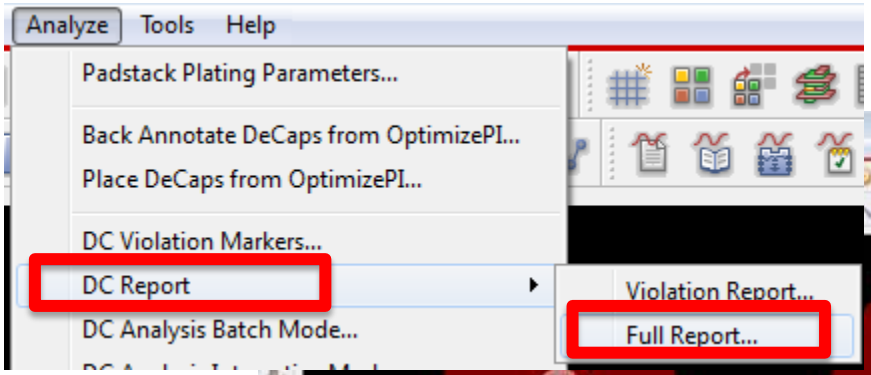
PI Base

PowerDC



# Integrated DC Solutions

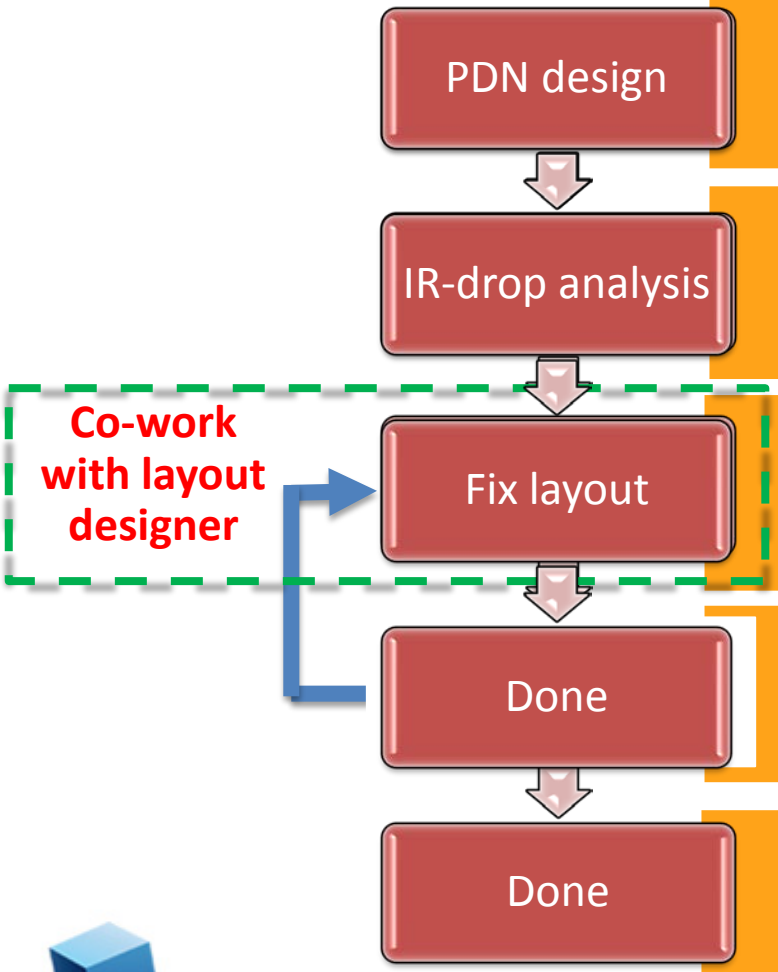
- Load a PowerDC report in PI Base
  - Check violations
  - Fix layout problems




PI Base

# DC IR-drop Analysis Solutions

## DC Accelerate solutions

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Accelerate

- Add Layers/ Via or conductors shape area
- Change via location

Accelerate

- Re-setup simulation setting or reuse Power workspace features (*.pdcx)

Accelerate

- Simulation results meet the requirements, generate report

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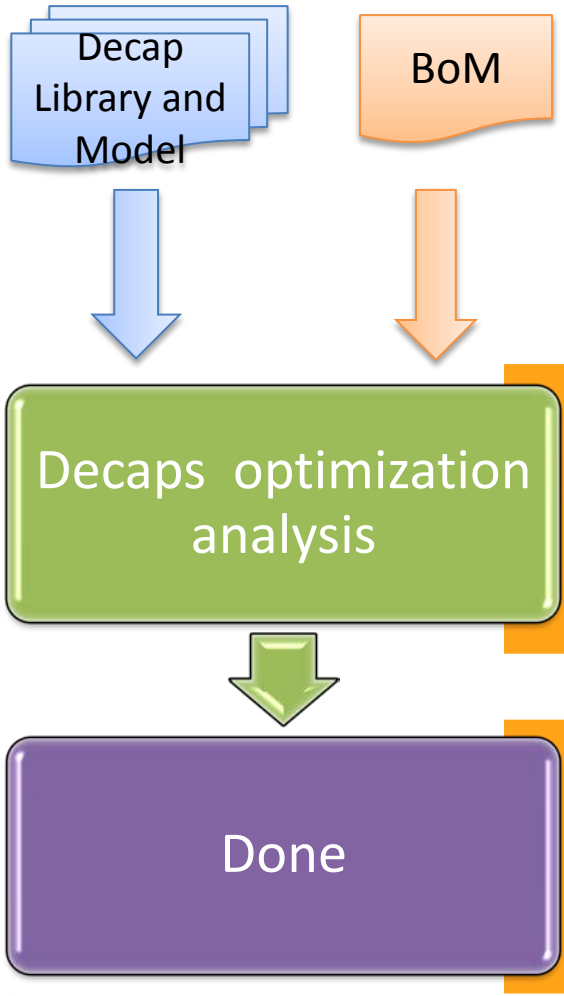
# Integrated AC Solutions

## Decoupling capacitor optimization

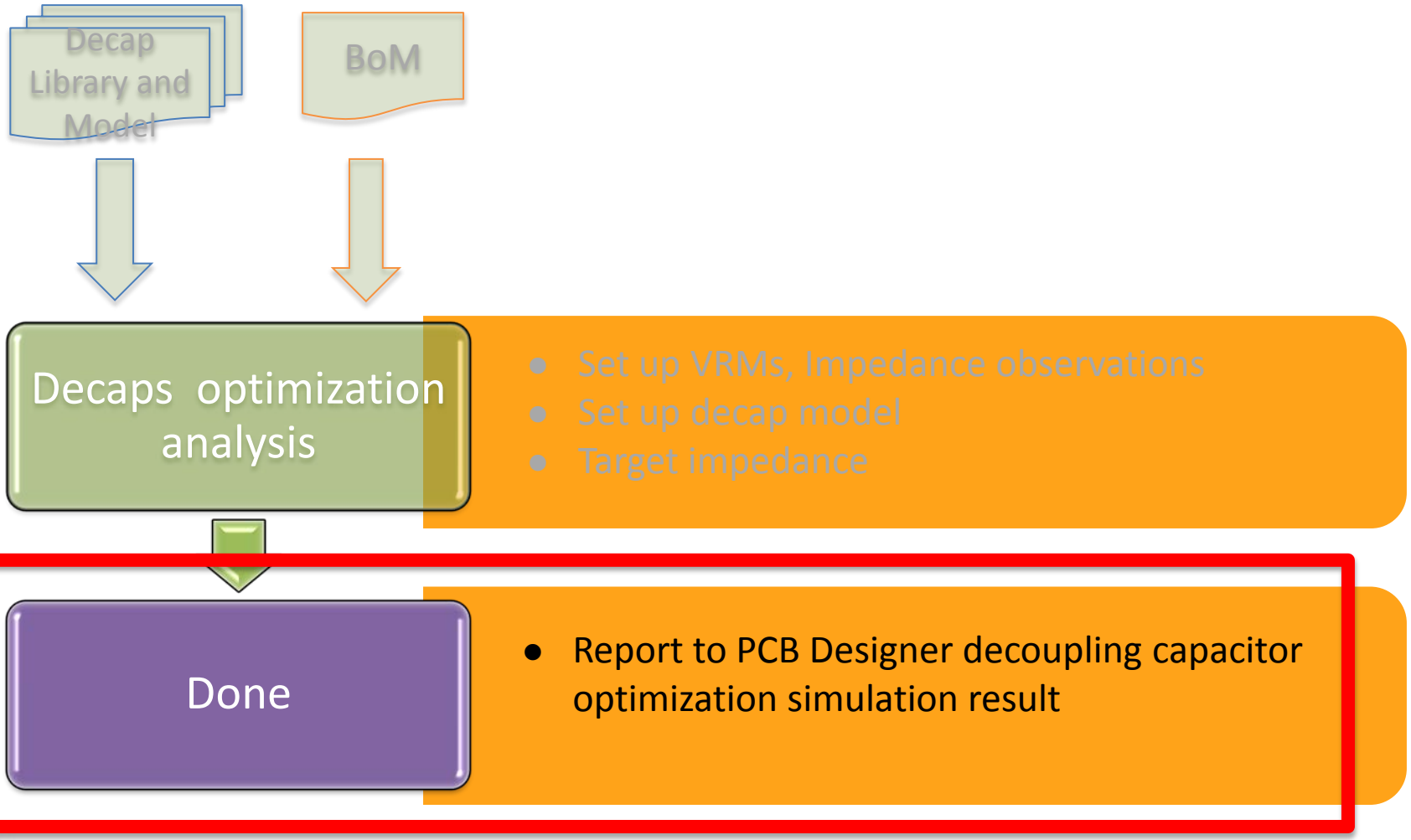



- Set up VRMs, Impedance observations
- Set up decap model
- Target impedance

- Report to PCB Designer decoupling capacitor optimization simulation result

# Integrated AC Solutions

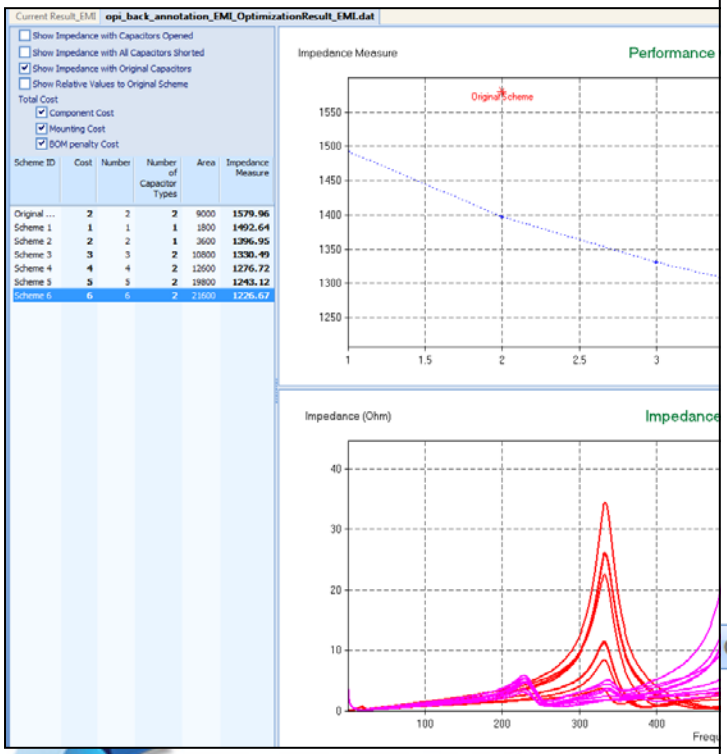
## Decoupling capacitor optimization

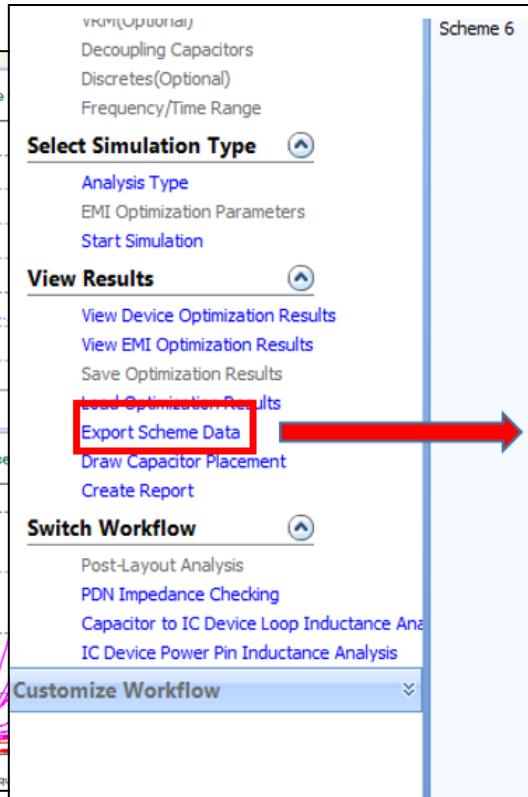


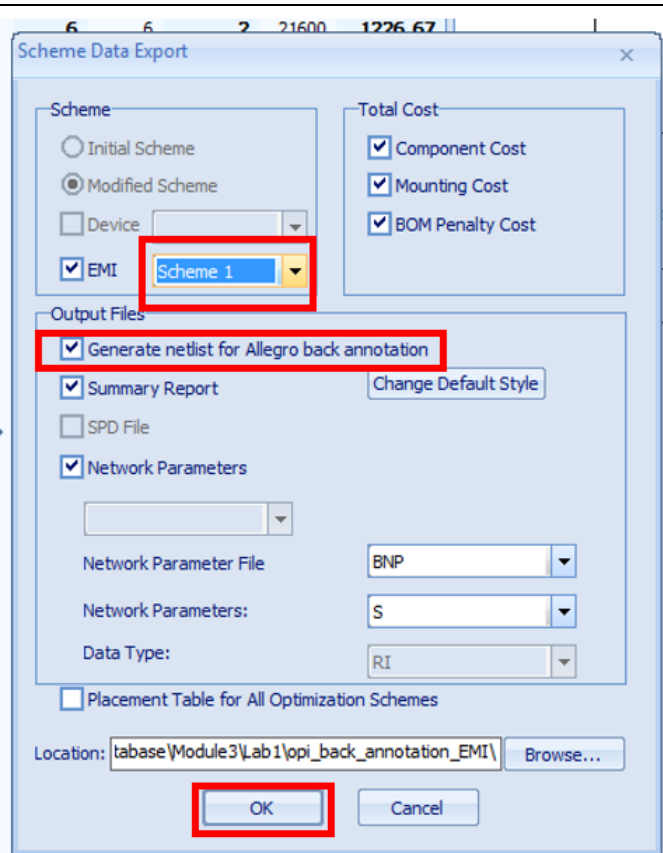
# Integrated AC Solutions

## Decap Back-annotation

- Decap Optimization in OptimizePI
  - Simulation in OPI
  - Export scheme data



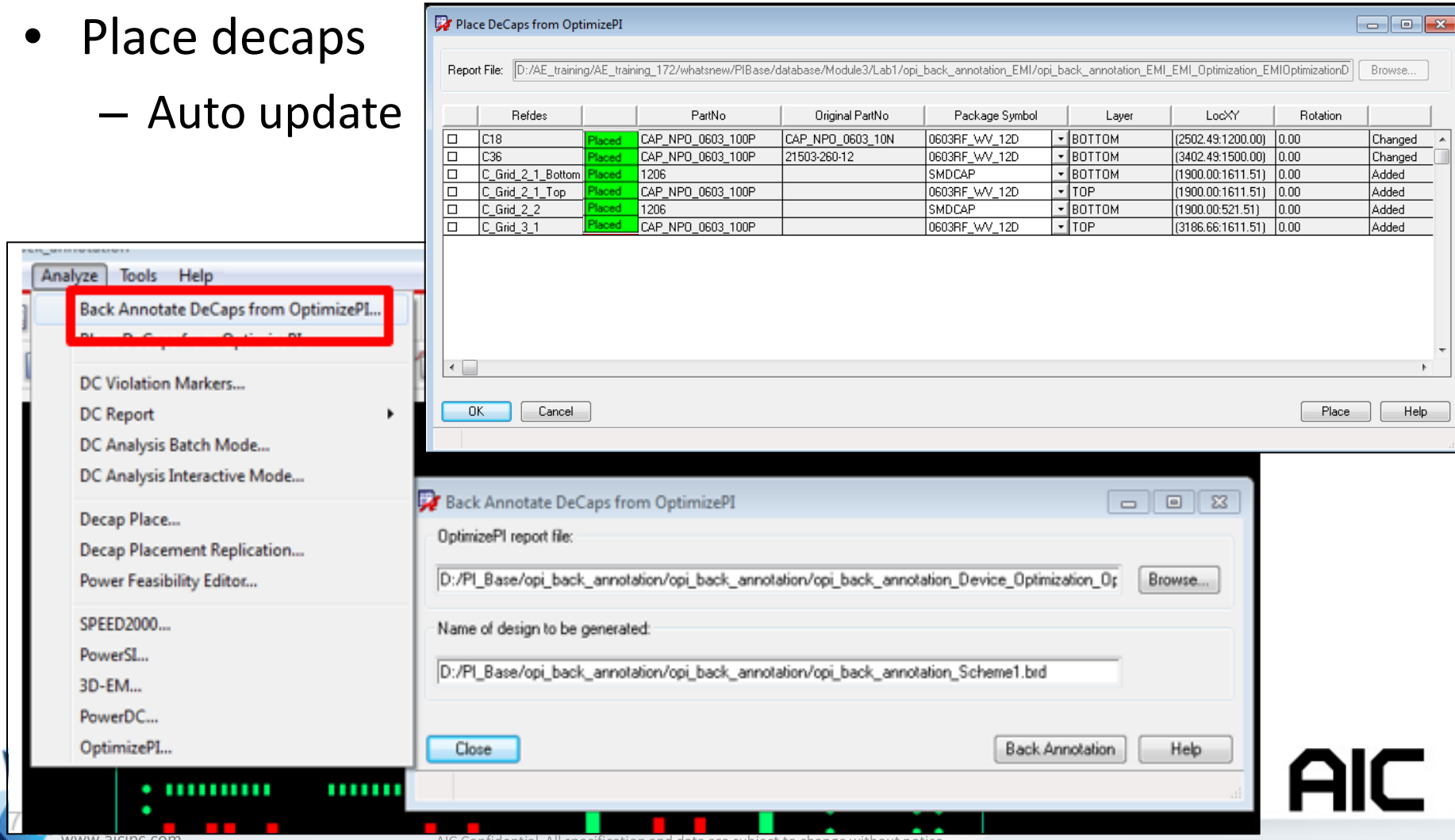



# Integrated AC Solutions

## Decap Back-annotation

- Use the original brd file
- Place decaps
  - Auto update



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# Case improved efficiency compared

- In complex  PDN case for ten power rail simulation analysis

| PDN analysis simulation | Item | Before | Accelerate solution |
|---|---|---|---|
| DC IR-drop analysis | Initial IR-drop analysis | 80 min | 30 min |
| | Fix layout | Half day | 10 min |
| | Re-simulation | 20 min | ~~10 min~~ |
| AC decaps optimization analysis | Place decaps | 20 min | 10 min |

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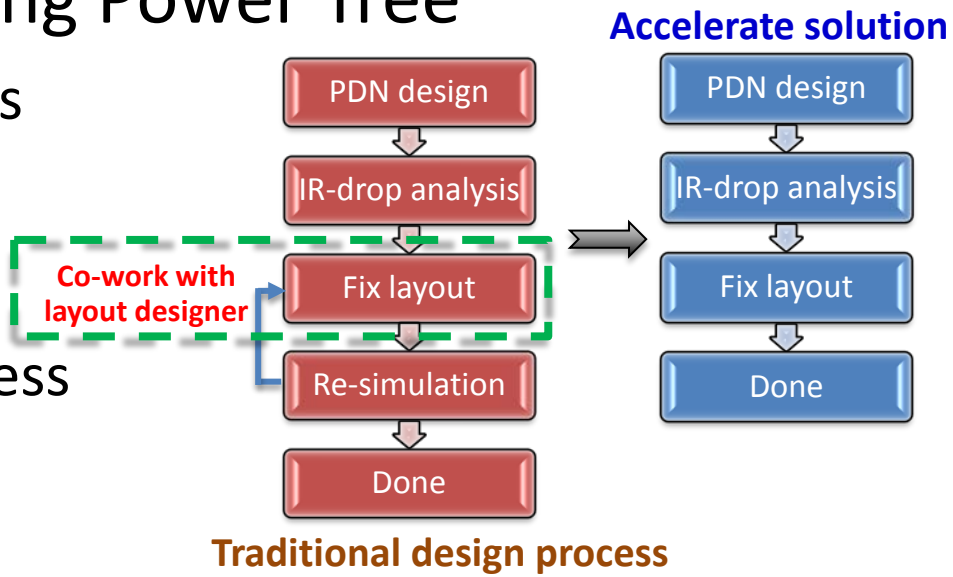
# Summary

- Accelerate DC analysis using Power Tree
  - Reduce nearly 50% time costs
  - Extract power topologies
  - setting automation
  - Increase simulation correctness




- Integrated Solutions
  - Reduce communication issues
  - Reduce modify layout version
  - Increasing the overall efficiency of the PDN design

# Thank you !