



Accelerate your Power Delivery Network Simulation Analysis

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> COMPANY FACTS



Established Date : May 3rd, 1996

Company Founder/ CEO : Michael Liang

HQ Address : No. 152, Section 4th, Linghang N. Road ,
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> COMPLETE PRODUCT LINES FOR VARIOUS MARKETS

Target Vertical Markets



Cloud Data Center



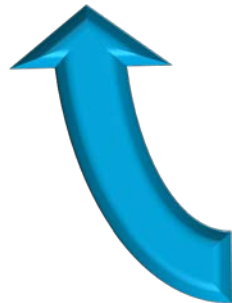
Networking Security



Broadcasting



Industrial PC



Storage Solution



Storage Controller Design

Rackmount Enclosure



Server Board Design

Server Barebone



Outline

- DC IR-drop Analysis Solutions
- Integrated DC Solutions
- Integrated AC Solutions
- Case Improved efficiency compared
- Summary



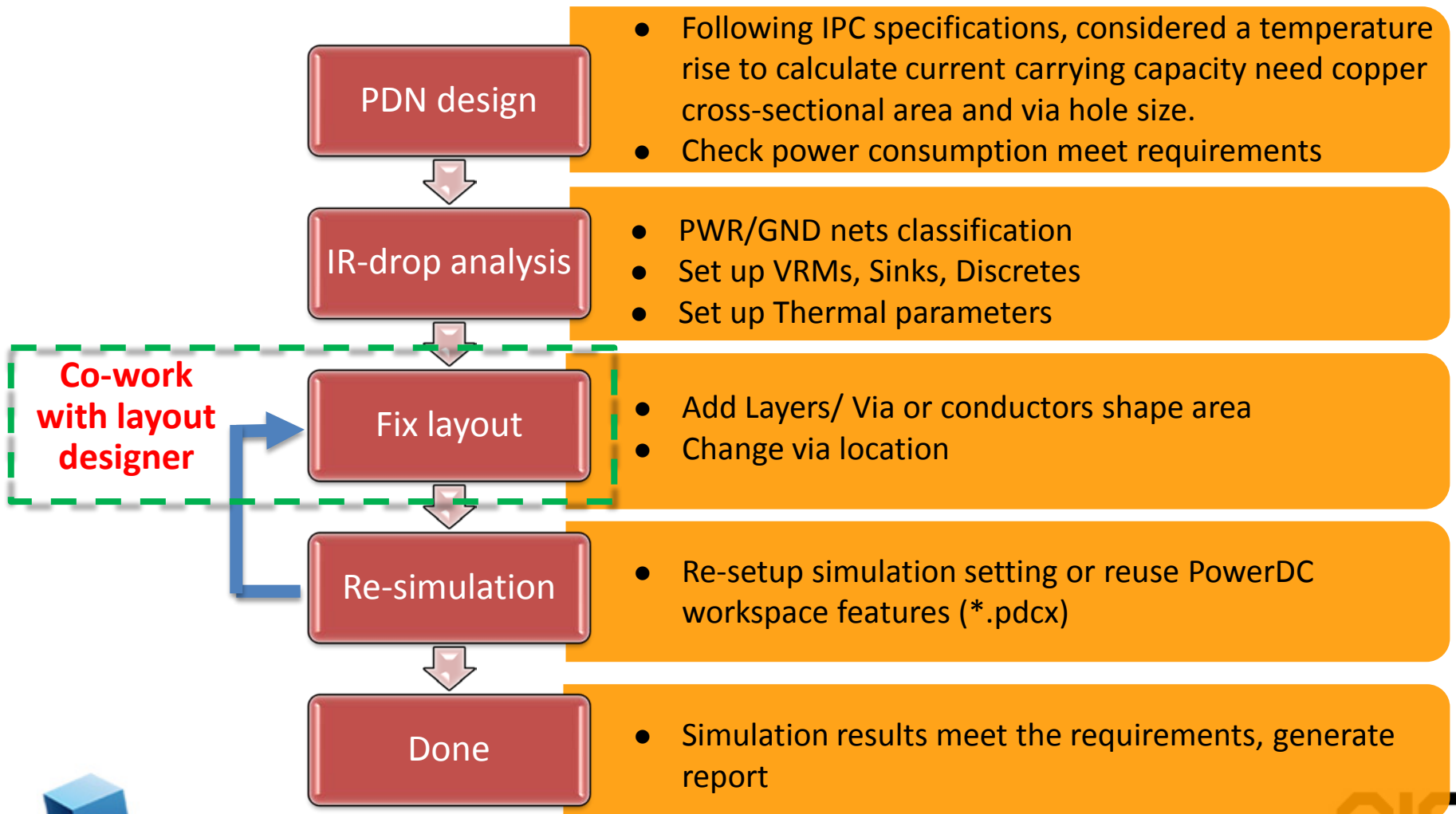
Outline

- DC IR-drop Analysis Solutions
- Integrated DC Solutions
- Integrated AC Solutions
- Case Improved efficiency compared
- Summary



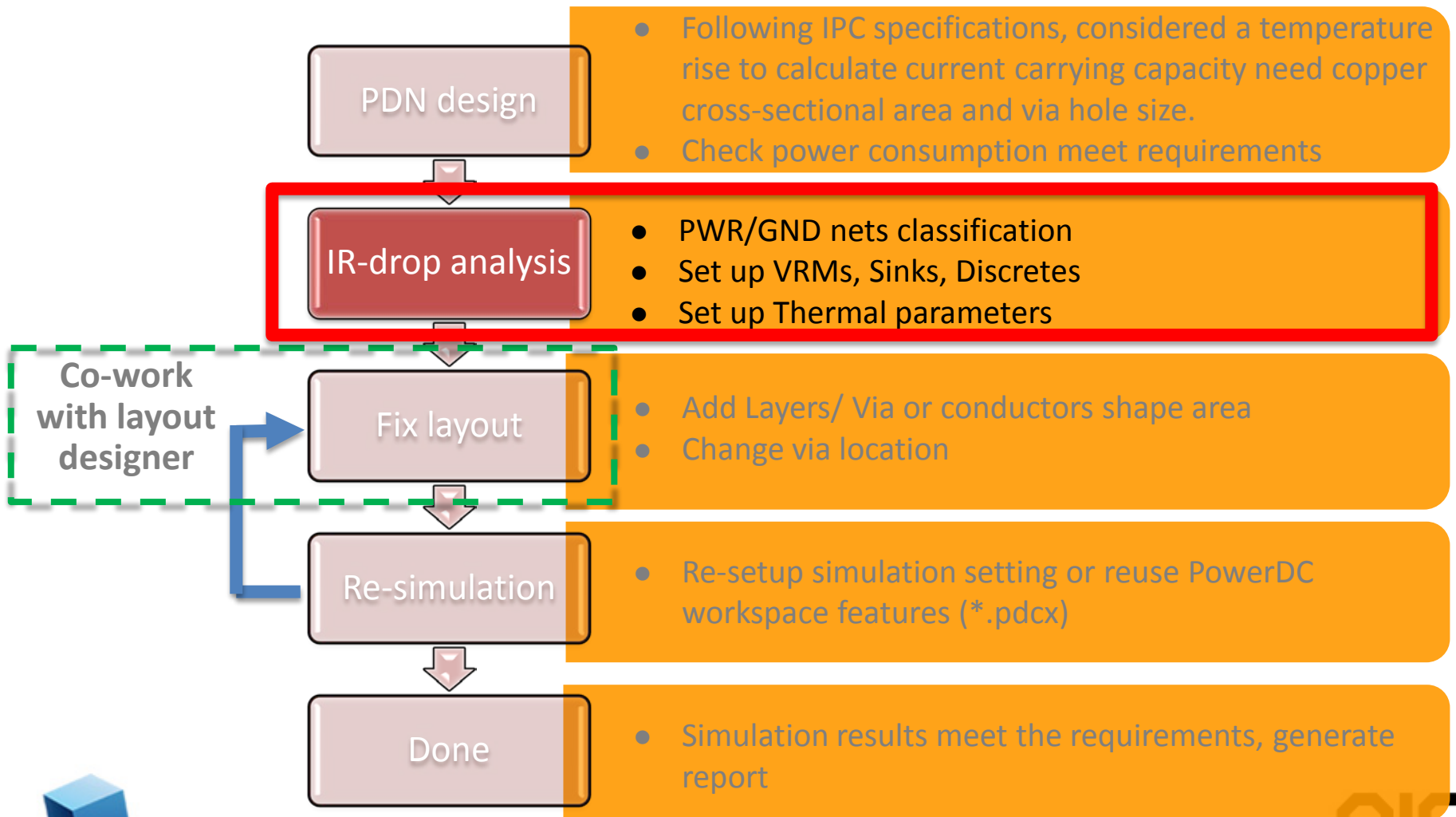
DC IR-drop Analysis Solutions

DC IR-drop design flow



DC IR-drop Analysis Solutions

Initial DC analysis

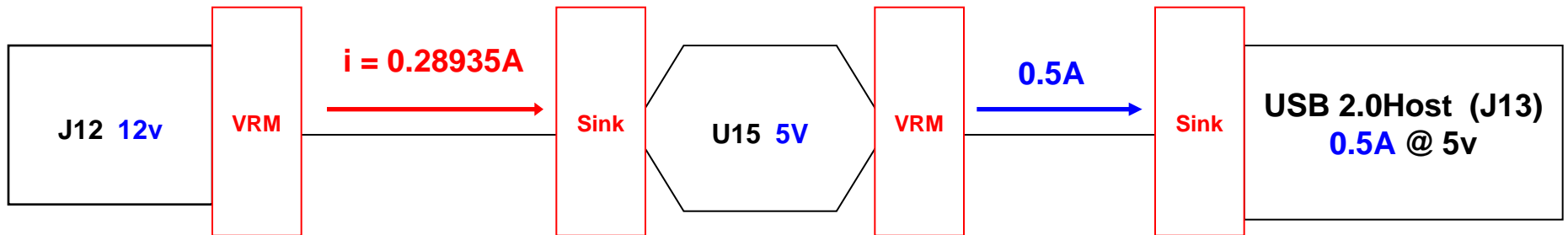


DC IR-drop Analysis Solutions

Your DC analysis is correct in setup?

- Set up VRMs, Sinks device and sense pin.
- Relationship of voltage switch and interconnect.

Switcher Efficiency (Eff)= 72%



$$V_{in} (v) \times I_{in} (A) \times \text{Eff}\% = V_{out} (v) \times i_{out} (A)$$



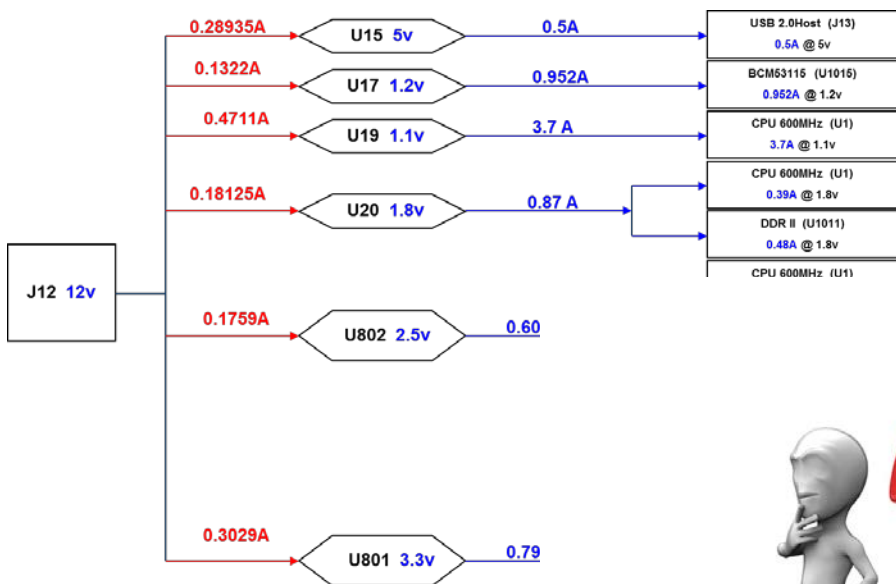
$$12 \times i (A) \times 0.72 = 5 \times 0.5$$

DC IR-drop Analysis Solutions

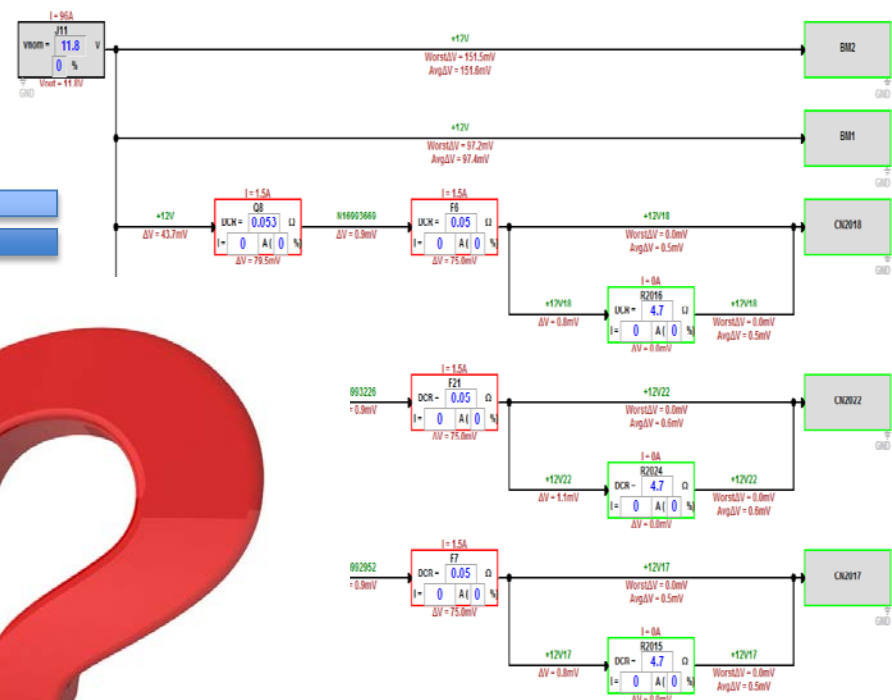
Your DC analysis is correct in setup?

- Correct DC block diagram in simulation.

Your DC Analysis Block Diagram

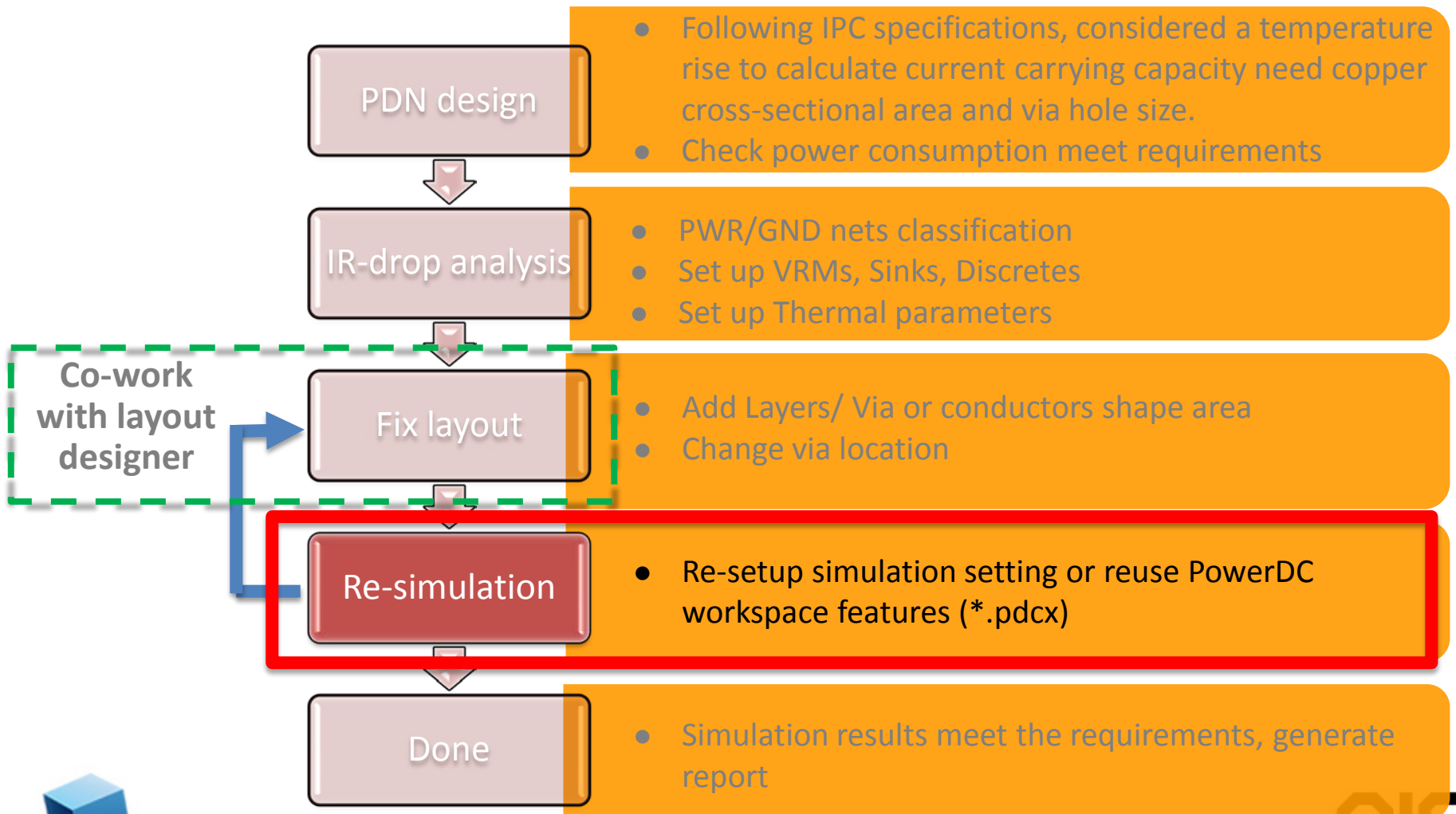


DC Analysis Block Diagram simulation result



DC IR-drop Analysis Solutions

Re-simulation



DC IR-drop Analysis Solutions

Reuse PowerDC workspace feasibility?

NO

Load
*.pdcx file

Any component
name change?

Reuse Fail

YES

Re-setup
simulation setting

Check VRMs ,Sinks
and Discretes setting

Re-simulation

NO

Check lost setting
and set up

- If it is complex PDN
- Large board file size

Time cost!!!!

AIC

DC IR-drop Analysis Solutions

When complex Power Delivery Network Simulation Analysis...

- Complicated set of VRMs and Sinks.
- Power rail interconnections
- Correct DC analysis block diagram
- Reuse PowerDC workspace features

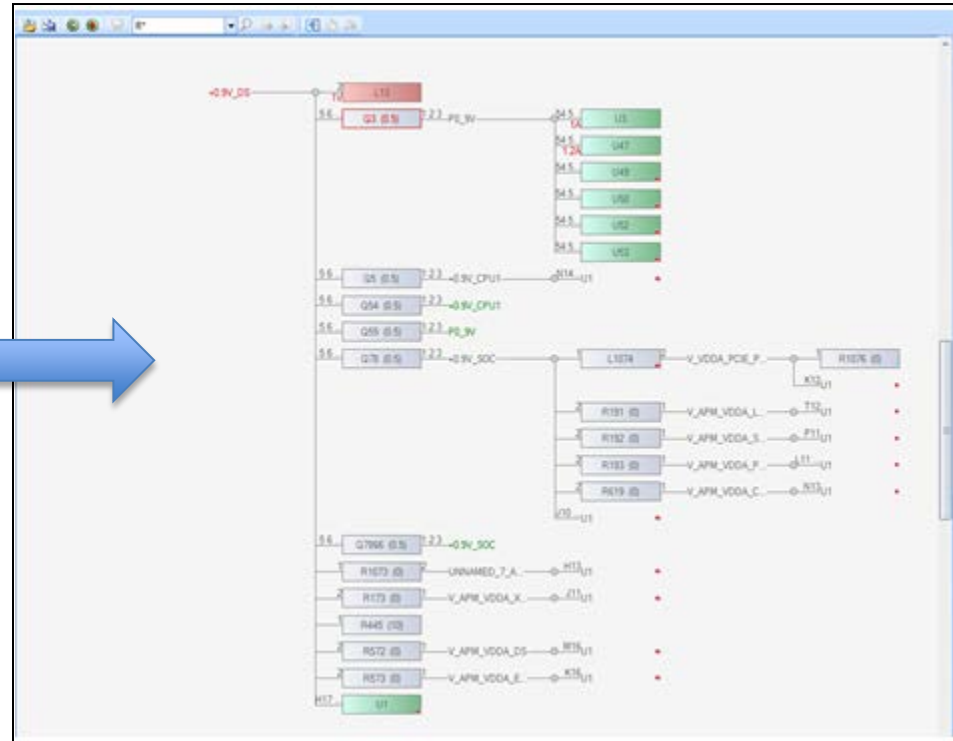
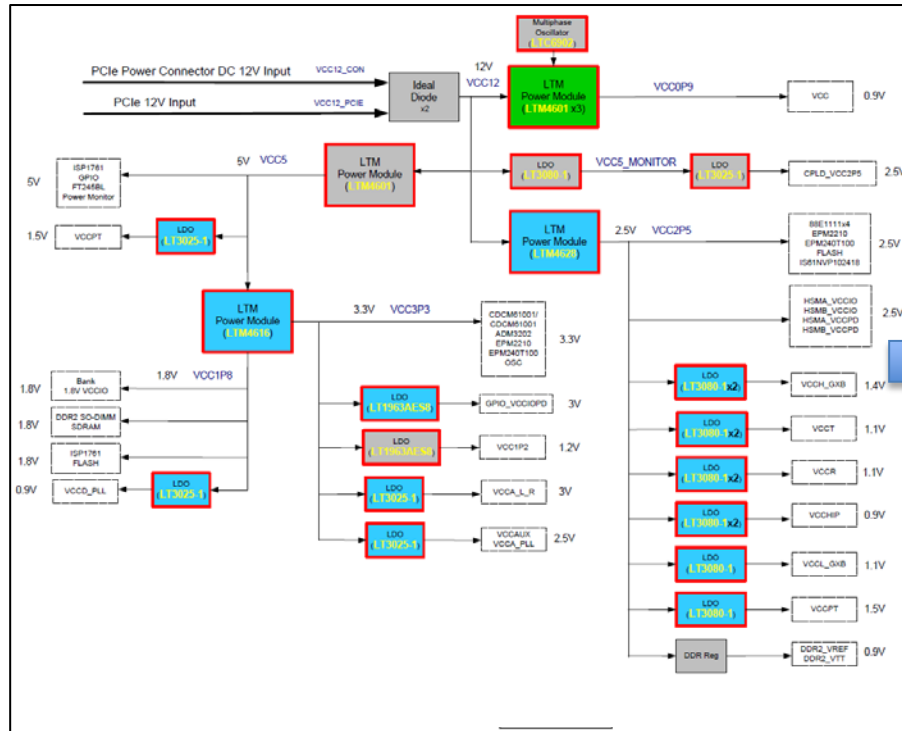
**Spend the most time of DC analysis
and correct simulation confirmed**



DC IR-drop Analysis Solutions

Power Tree concept

- Describe on your PDN block diagram



DC IR-drop Analysis Solutions

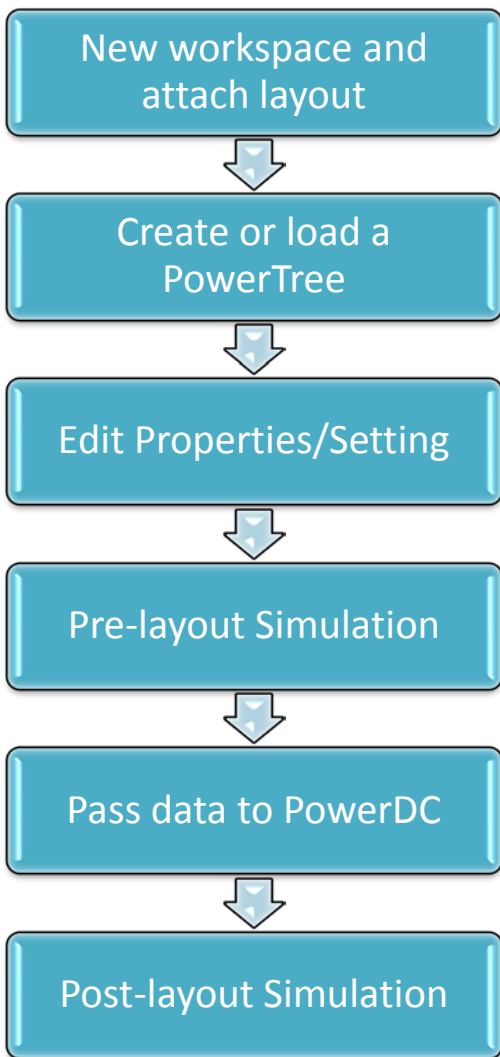
What's Power Tree can help?

- Power Tree is a tool for early power estimation
- Power Tree is a visualization tool for the schematic data
- Power Tree is used to extract power topologies from net list
- Power Tree is used to help setting automation
- Power Tree is used to help setting reuse



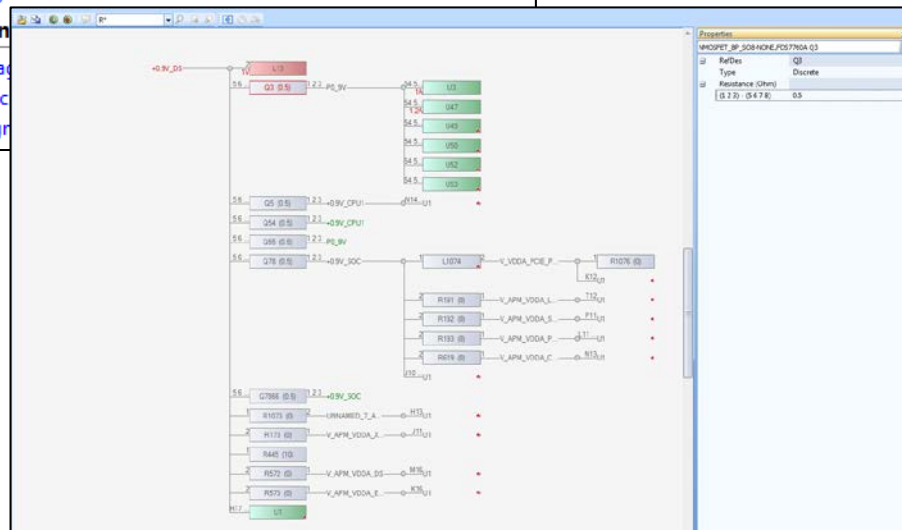
DC IR-drop Analysis Solutions

Power Tree Based DC Auto Setup Flow



Single-Board/Package IR Drop Analysis

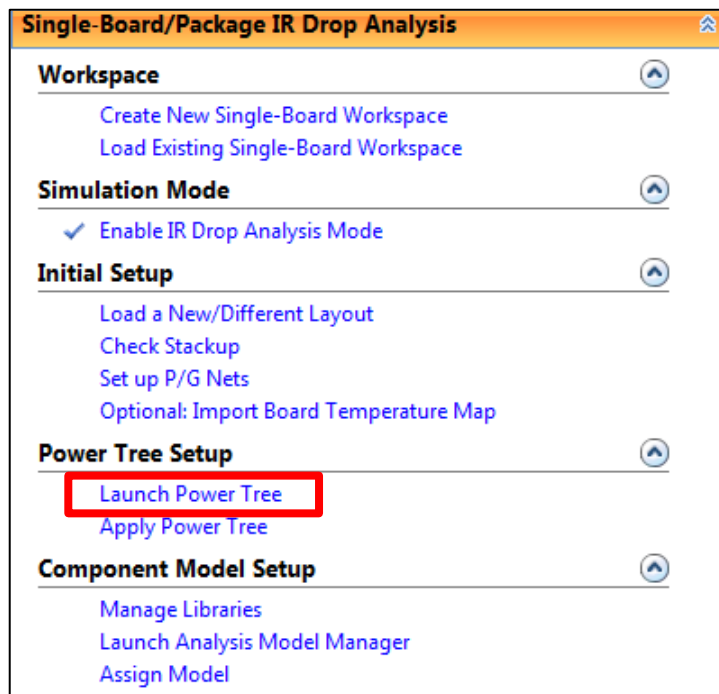
- Workspace**
 - Create New Single-Board Workspace
 - Load Existing Single-Board Workspace
- Simulation Mode**
 - ✓ Enable IR Drop Analysis Mode
- Initial Setup**
 - Load a New/Different Layout
 - Check Stackup
 - Set up P/G Nets
 - Optional: Import Board Temperature Map
- Power Tree Setup**
 - Launch Power Tree**
 - Apply Power Tree
- Component**
 - Manage
 - Launch
 - Assign



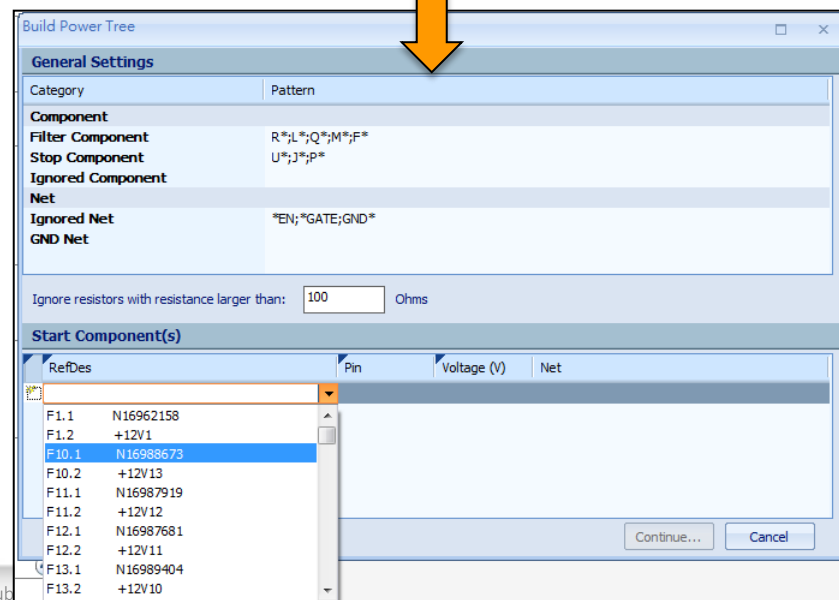
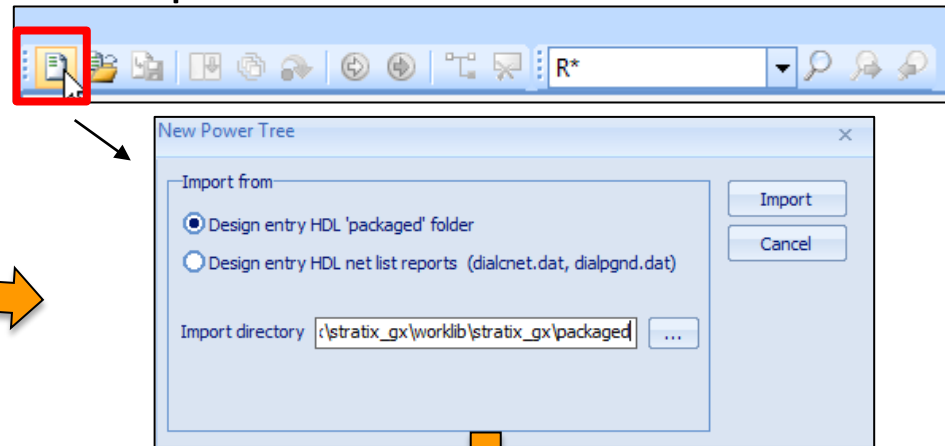
DC IR-drop Analysis Solutions

Power Tree Generation

- “Launch Power Tree” in workflow



- Import netlist files

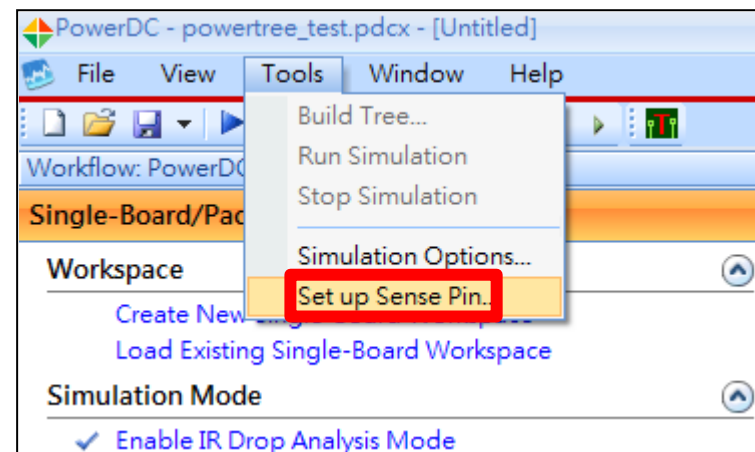
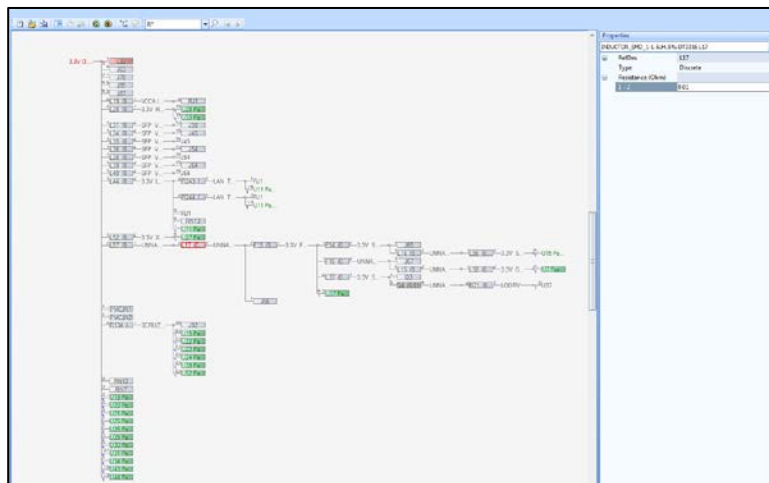


- Pick the starting component pin
- Select through pins for through components if any

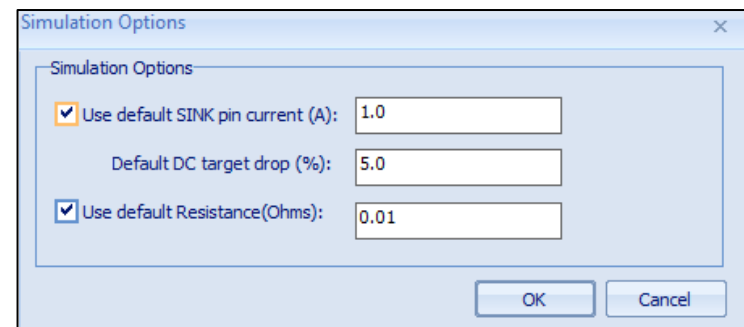
DC IR-drop Analysis Solutions

Property Editing in Power Tree

- Double click a component to edit properties
 - Sink current/discrete comp resistance/sense pin



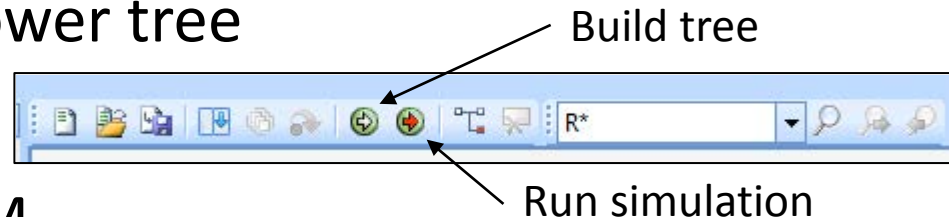
- Default settings for all others
 - Tools->Simulation Options...



DC IR-drop Analysis Solutions

DC Analysis in Power Tree (Pre-simulation)

- Results will mark on the power tree
- Check discrete current
- Check total current for VRM



The screenshot shows the 'PowerTree Output' window. The top part displays a hierarchical power tree starting with a +12V source, branching into two bus bars (BM1 and BM2), and then into various regulators (Q10-Q14) and their outputs (F8-F12). The bottom part shows the simulation output text, which is partially highlighted with a red box. The text indicates that the simulation passed for all sinks and components.

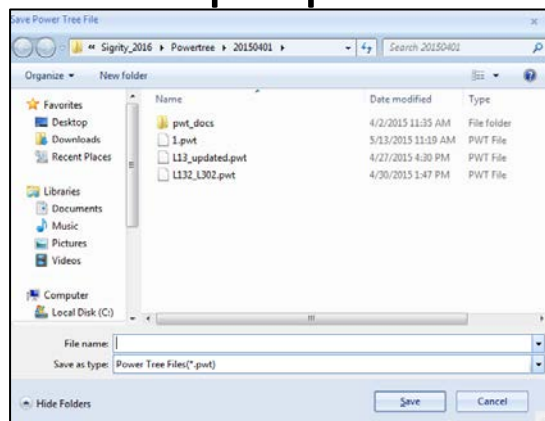
```
Start simulation...
Disabled SINK: "U15.1.9".
VRM and SINK are linked to the same net+12V. The SINK will not be considered in the simulation
VRM and SINK are linked to the same net+12V. The SINK will not be considered in the simulation
Simulation completed.

Pass (0%): SINK: "BM1 (5 6 7 8 9 10 11 12)"
Pass (0%): SINK: "BM2 (5 6 7 8 9 10 11 12)"
Pass (-1.2875%): SINK: "CN2016 (P14 P15)"
Pass (-1.2875%): SINK: "CN2015 (P14 P15)"
Pass (-1.2875%): SINK: "CN2013 (P14 P15)"
Pass (-1.2875%): SINK: "CN2012 (P14 P15)"
Pass (-1.2875%): SINK: "CN2011 (P14 P15)"
Pass (-1.2875%): SINK: "CN2010 (P14 P15)"
Pass (-1.2875%): SINK: "CN2009 (P14 P15)"
Pass (-1.2875%): SINK: "CN2008 (P14 P15)"
Pass (-1.2875%): SINK: "CN2007 (P14 P15)"
Pass (-1.2875%): SINK: "CN2006 (P14 P15)"
Pass (-1.2875%): SINK: "CN2001 (P14 P15)"
Pass (-1.2875%): SINK: "CN2004 (P14 P15)"
Pass (-1.2875%): SINK: "CN2003 (P14 P15)"
Pass (-1.2875%): SINK: "CN2002 (P14 P15)"
Pass (-1.2875%): SINK: "CN2022 (P14 P15)"
Pass (-1.2875%): SINK: "CN2019 (P14 P15)"
Pass (-1.2875%): SINK: "CN2014 (P14 P15)"
Pass (-1.2875%): SINK: "CN2005 (P14 P15)"
```

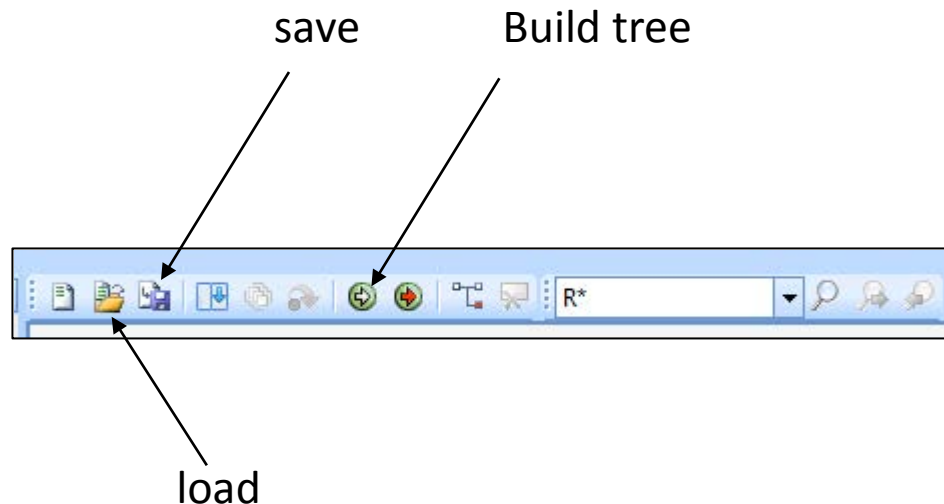
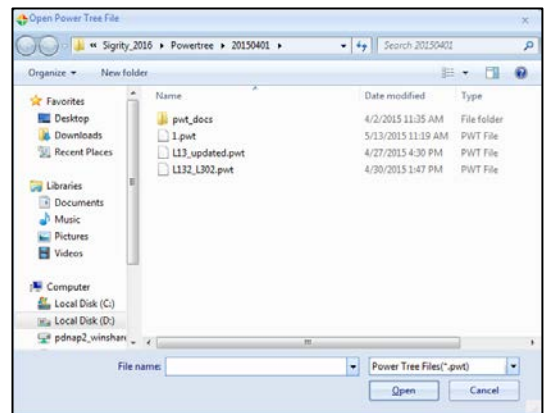
DC IR-drop Analysis Solutions

Save/Load Power Tree Files

- Save a power tree file
 - Both properties and topologies are saved



- Load a power tree file



DC IR-drop Analysis Solutions

Pass Power Tree Data to PowerDC

- Attach layout to PowerDC
 - Matching with the schematic (Power tree)
- “Apply PowerTree” in workflow
- Select proper ground nets
- After the assignment, check workspace



Voltage Drop Analysis Setup -> Set up Sinks

	Sink Name	Model	Nominal Voltage (V)	Power/Ground Net	Upper Tolerance(+%)	Lower Tolerance(-%)	P/F Mode	Current (A)	Current (A)
<input checked="" type="checkbox"/>	SINK_U30_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U31_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U34_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U43_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U44_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U28_3_3V_R...	Equal Current	3.3	3_3V_RS232_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U33_3_3V_R...	Equal Current	3.3	3_3V_RS232_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U20_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U19_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1
<input checked="" type="checkbox"/>	SINK_U21_3_3V_GND	Equal Current	3.3	3_3V_GND	5	5	Average	1	1

DC IR-drop Analysis Solutions

Compare Two Power Trees

Load compare tree

Refresh compare tree



Show/hide compare tree

The screenshot shows two side-by-side windows displaying power trees. The left window is titled 'Present' and the right is 'Loaded'. Both show a hierarchical tree of components like resistors, capacitors, and connectors. A context menu is open over the left tree, and another is open over the right tree. A 'Reuse Properties...' button is highlighted in the right menu, with a red arrow pointing to a 'Reuse RefDes Properties' dialog box on the right side of the screen.

Expand All
Collapsed All
Show Selected SINK Routes
Rebuild Tree...
Disable SINK
Load Compare Tree...
Unload Compare Tree
Show Compare Tree
Refresh Compare Results

Expand All
Collapsed All
Show Selected SINK Routes
Load Compare Tree...
Unload Compare Tree
Show Compare Tree
Refresh Compare Results
Reuse Properties...

RefDes	
<input checked="" type="checkbox"/> Q2.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> Q24.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> F2.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> Q5.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> F24.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> Q23.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> Q14.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> Q19.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> F16.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> F17.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> F5.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> Q7.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> F15.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> F18.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> F13.1 - 2	0.05 ohm
<input checked="" type="checkbox"/> Q18.3 - 5.6	0.053 ohm
<input checked="" type="checkbox"/> Q21.3 - 5.6	0.053 ohm

Global Setting

<input checked="" type="checkbox"/> Default Resistance	1.0 Ohm
<input checked="" type="checkbox"/> Default SINK pin current	1.0 A
<input checked="" type="checkbox"/> Default DC target drop(%)	5.0

OK Cancel



DC IR-drop Analysis Solutions

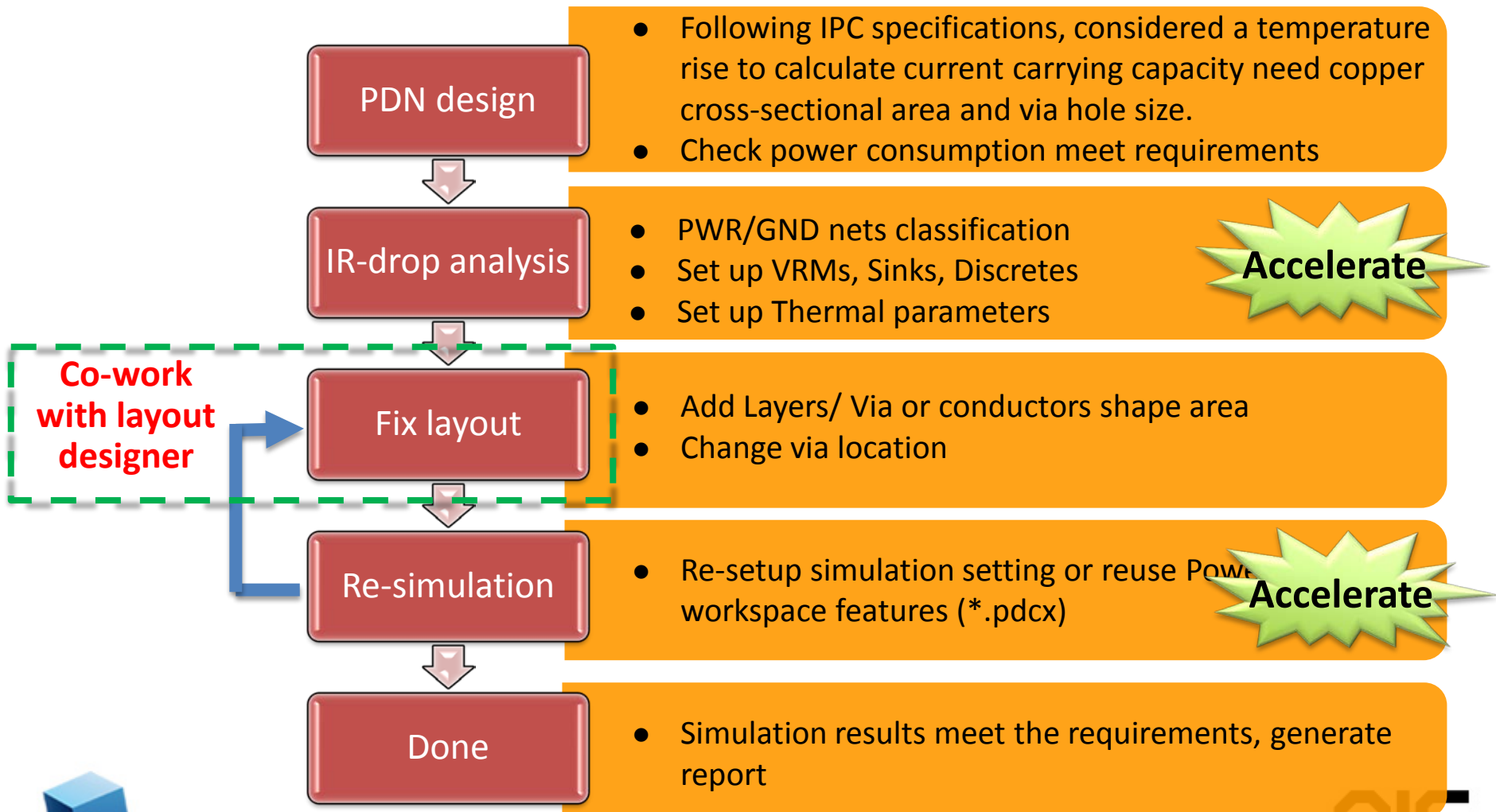
What Power Tree Will Do?

- Power topology extraction from schematic data in graphic diagrams
- Editing/creating properties in Power Tree
- Help to select/group proper power/ground nets analysis
- Circuit simulation in Power Tree
- Passing properties from PowerTree to PowerDC for settings reuse
- Saving/Loading Power Tree
- Comparing two Power Trees
- Auto net classification



DC IR-drop Analysis Solutions

Power Tree Accelerate



DC IR-drop Analysis Solutions

Using Power Tree acceleration

- In complex PDN for ten power rail simulation analysis

DC IR-drop analysis	Item	Not used	Using Power Tree	Features
IR-drop analysis	Set up VRMs, Sinks, Discretes, Sense pin	60 min	30 min	Extract power topologies from netlist and circuit simulation (setting automation)
	Interconnections	10 min		
	Check DC analysis block diagram	10 min		
Re-simulation	Reuse PowerDC workspace	20 min	10 min	Compare Two Power Trees

Reduce half the time costs ↓
Simulation correctness ↑

AIC

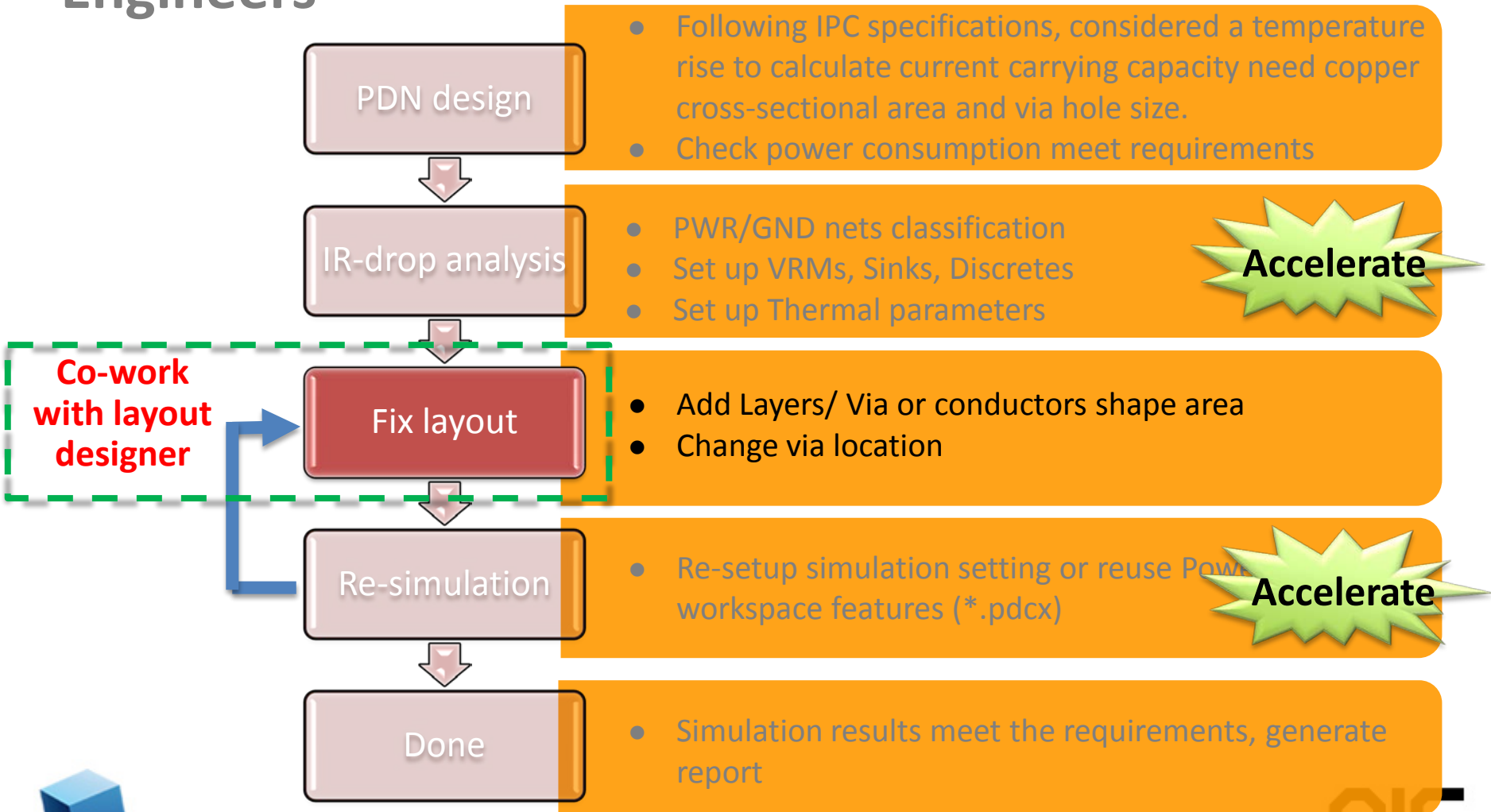
Outline

- Challenges for PCB Designers
- DC IR-drop Analysis Solutions
- **Integrated DC Solutions**
- Integrated AC Solutions
- Case Improved efficiency compared
- Summary



Integrated DC Solutions

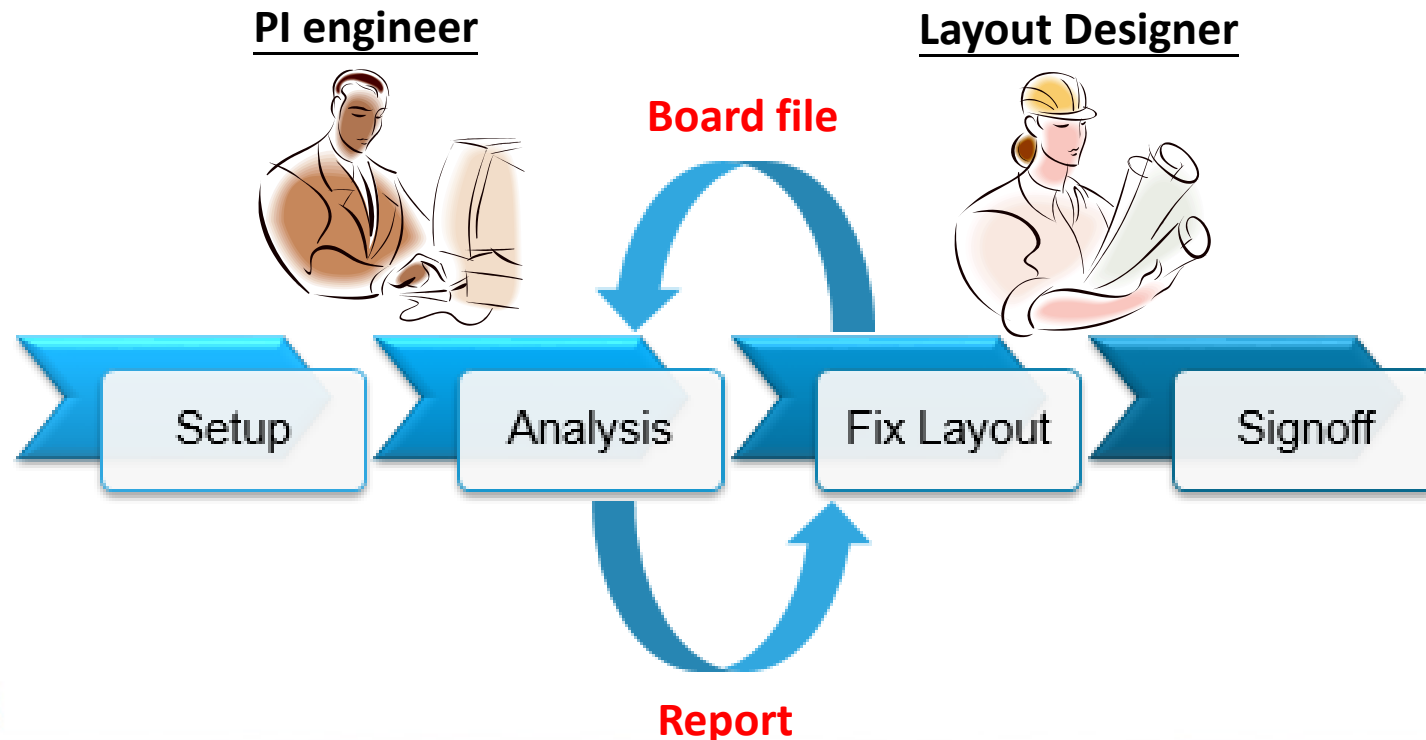
Innovative Solution for PCB Designers and PI Engineers



Integrated DC Solutions

Co-work with layout designer

- For typical enterprise customers, the DC design and analysis flow is as below
 - Communication and efficiency issue



Integrated DC Solutions

Gap in layout modify

- After modified board file need to verification simulation.
- Modified board gap with the PI engineer suggestion.

PI engineer



Report

Integrated DC Solutions

Cross probing between layout design and analysis results

- Layout incremental update support
- Allegro layout change is dynamically updated to PDC-Lite
 - Update Selected Nets

PI Base

PowerDC

The image displays two software windows side-by-side. The left window is Allegro PCB Editor, showing a PCB layout with a red box highlighting a circular feature. The right window is PowerDC, showing a color-coded IR drop analysis plot with a red box highlighting a corresponding feature. A blue arrow points from the red box in the layout to the red box in the analysis plot. The PowerDC window also shows a 'Net Manager' panel with a red box around the 'Update Selected Nets' button.

Allegro Sigrity PI (PCB): PI_dc.brd Project: D:\...PIBase/database/DC

PowerDC - PI_dc.pdcx - [PI_dc.spd Layer View]

Workflow PowerDC

Single-Board/Package IR Drop Analysis

Initial Setup

- Check Stackup
- Set up P/G Nets

Component Model Setup

- Manage Libraries
- Launch Analysis Model Manager
- Assign Model

Voltage Drop Analysis Setup

- Set up VRMs
- Set up Sinks
- Set up Discretes
- Set up V/I Probes
- Set up Ref Node, etc.

Constraints Setup

- Set up E-Constraints

Simulation

- Check Errors/Warnings
- Save Files
- Start Simulation

Results and Report

- View E-Results Tables
- View 2D E-Distributions
- View 3D E-Distributions
- View 3D Via Distributions
- Switch to Normal Layer View

Generate Report

- Save Report

Net Manager

- Update Selected Nets
- Disable Selected Nets
- Enable All Nets
- Disable All Nets
- Classify
- Detect Extended Nets
- Merge Selected Nets
- Split Open Nets
- Show Objects of Nets
- 3D View Walk Through
- Set Color

Integrated DC Solutions

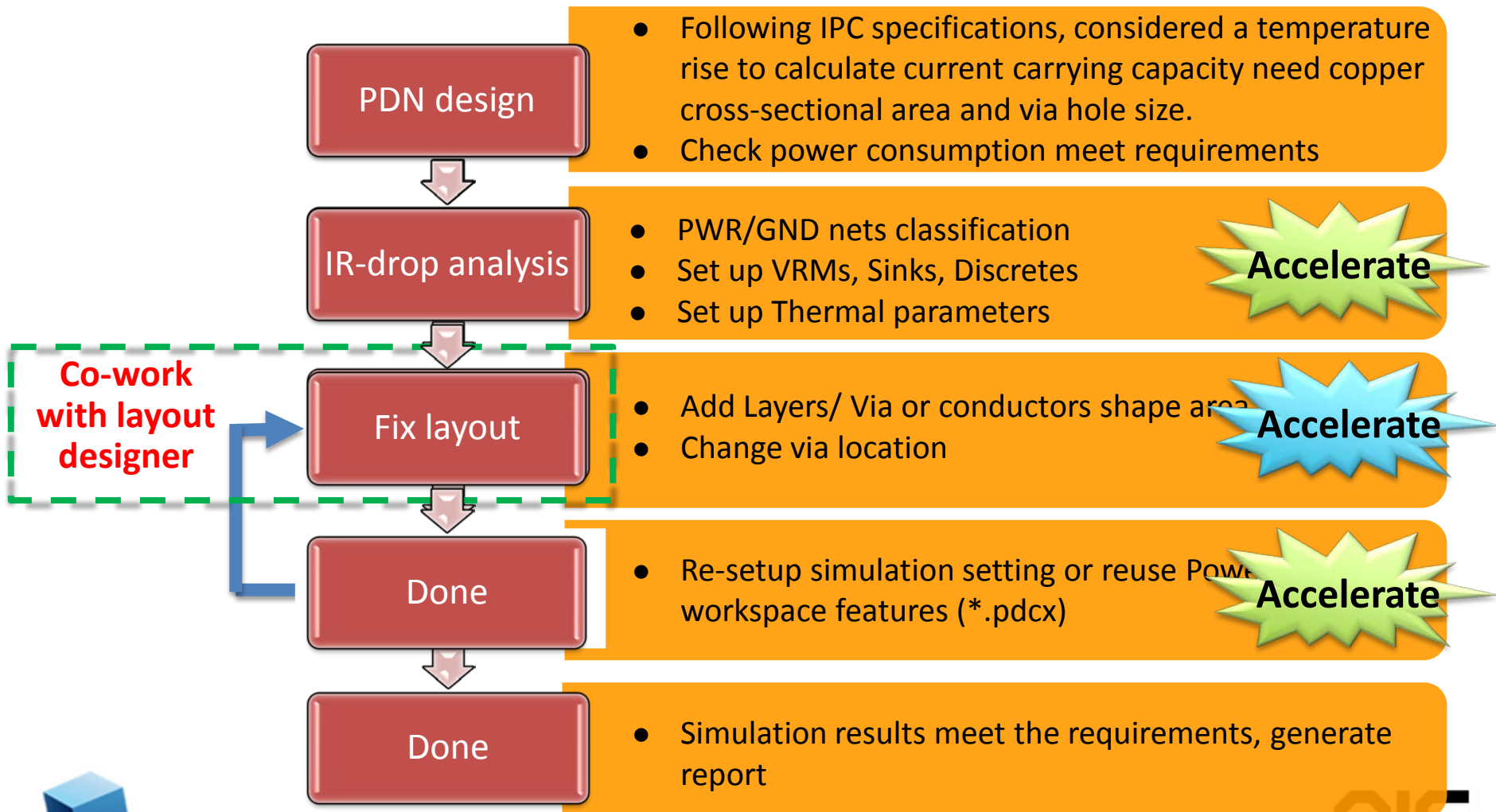
- Load a PowerDC report in PI Base
 - Check violations
 - Fix layout problems

The screenshot shows the Cadence software interface. The 'Analyze' menu is open, with 'DC Report' and 'Full Report...' highlighted in red boxes. A red box labeled 'PI Base' is positioned above a table of trace data. A blue arrow points from the 'Full Report...' option to the table.

Trace Name	Location(mm_min,mm_max)	Current Value	Actual Current Density(A/mm ²)
Trace17GND	(80.325000,0.000000,59.690000,0.615000)	925.936	2190.86
Trace17GND	(80.325000,0.000000,59.690000,0.615000)	925.936	2172.8
Trace100GND	(81.595000,0.000000,60.960000,0.615000)	925.936	2164.56
Trace114GND	(87.310000,-1.905000,67.945000,-2.540000)	925.936	2149.09
Trace110GND	(87.310000,0.635000,67.310000,-1.905000)	925.936	2149.09
Trace106GND	(82.230000,0.455000,62.230000,-1.905000)	925.936	2144.1
Trace107GND	(82.230000,-1.905000,62.965000,-2.540000)	925.936	2144.1
Trace112GND	(86.675000,0.000000,66.040000,0.615000)	925.936	2139.39
Trace110GND	(85.405000,0.000000,64.770000,0.635000)	925.936	2131.98
Trace104GND	(85.500000,-1.905000,64.135000,-2.540000)	925.936	2129.48
Trace103GND	(85.500000,0.635000,63.500000,-1.905000)	925.936	2129.48
Trace89VCC	(88.265000,-2.540000,87.630000,-1.905000)	925.936	2012.66
Trace89VCC	(87.630000,-1.905000,87.630000,0.615000)	925.936	2012.66
Trace71VCC	(89.535000,0.000000,88.900000,0.635000)	925.936	1969.99
Trace73VCC	(90.170000,-1.905000,90.805000,-2.540000)	925.936	1942.84
Trace72VCC	(90.170000,0.635000,90.170000,-1.905000)	925.936	1942.84
Trace77VCC	(91.440000,-1.905000,91.440000,0.615000)	925.936	1923.08
Trace78VCC	(92.075000,-2.540000,91.440000,-1.905000)	925.936	1923.08
Trace85VCC	(95.885000,-2.540000,95.250000,-1.905000)	925.936	1920.36
Trace86VCC	(95.250000,-1.905000,95.250000,0.635000)	925.936	1920.36
Trace79VCC	(92.710000,-1.905000,93.345000,-2.540000)	925.936	1912.04
Trace78VCC	(92.710000,0.635000,92.710000,-1.905000)	925.936	1912.04
Trace81VCC	(93.980000,0.635000,93.980000,-1.905000)	925.936	1910.63
Trace82VCC	(93.980000,-1.905000,94.615000,-2.540000)	925.936	1910.63

DC IR-drop Analysis Solutions

DC Accelerate solutions



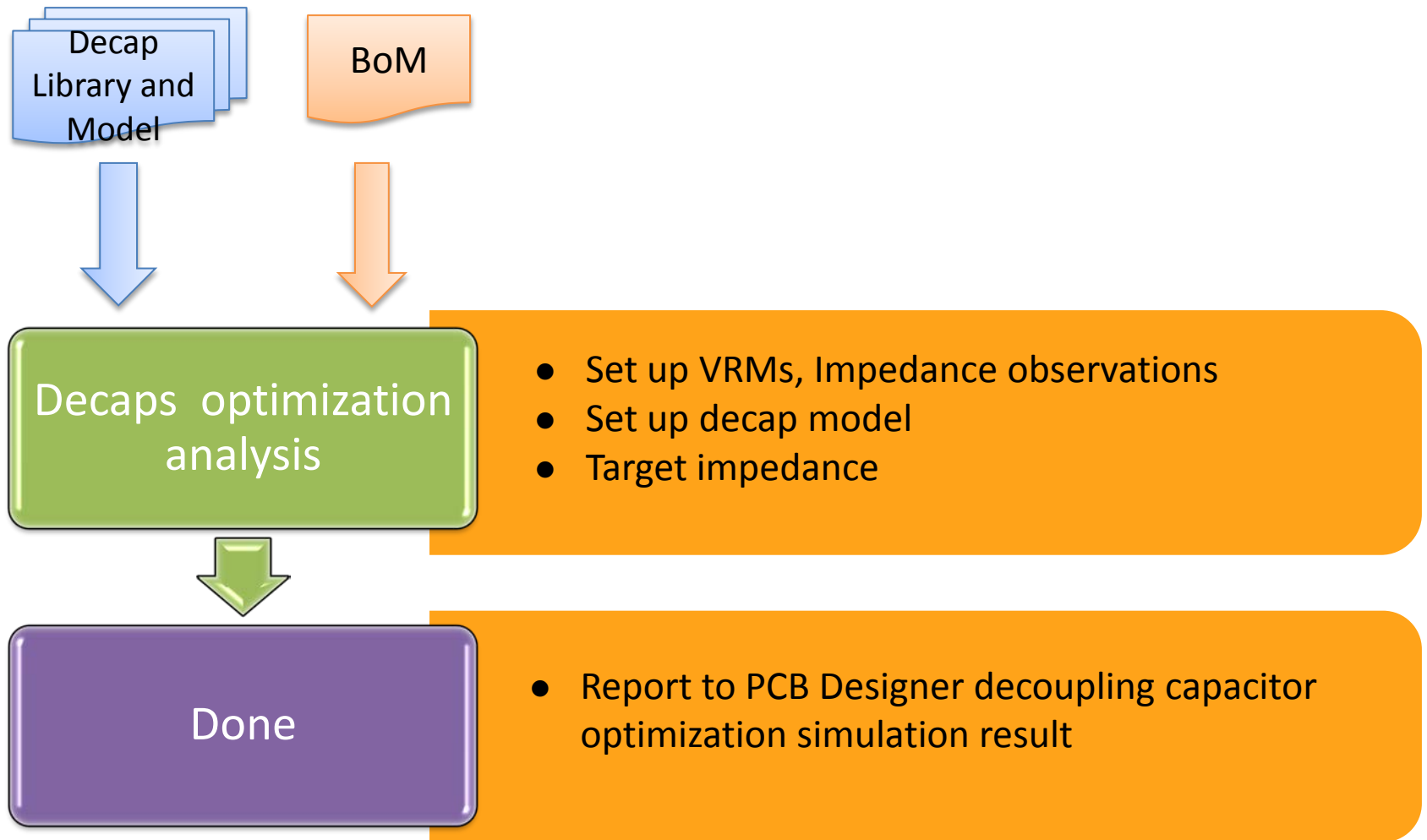
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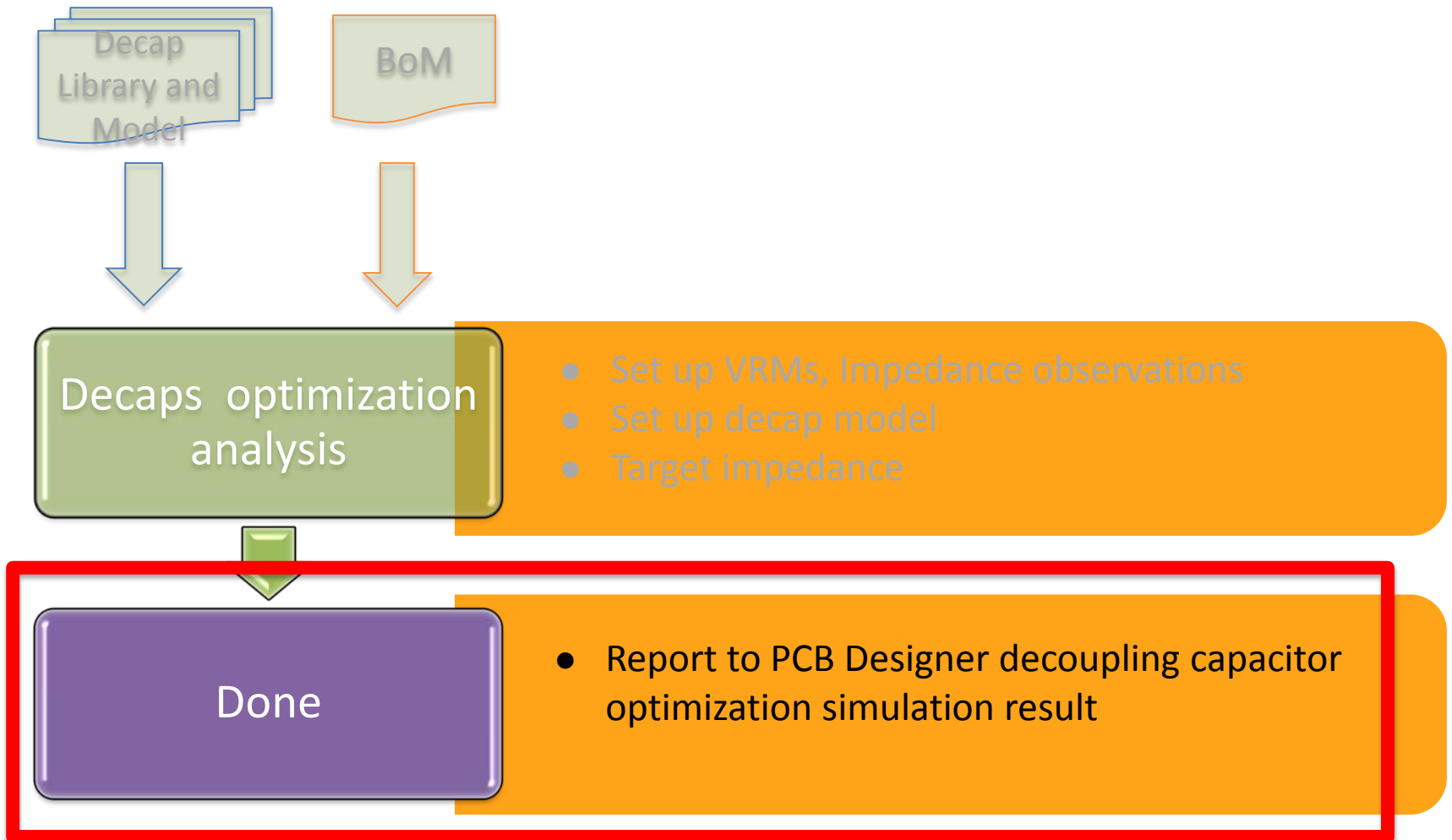
Integrated AC Solutions

Decoupling capacitor optimization



Integrated AC Solutions

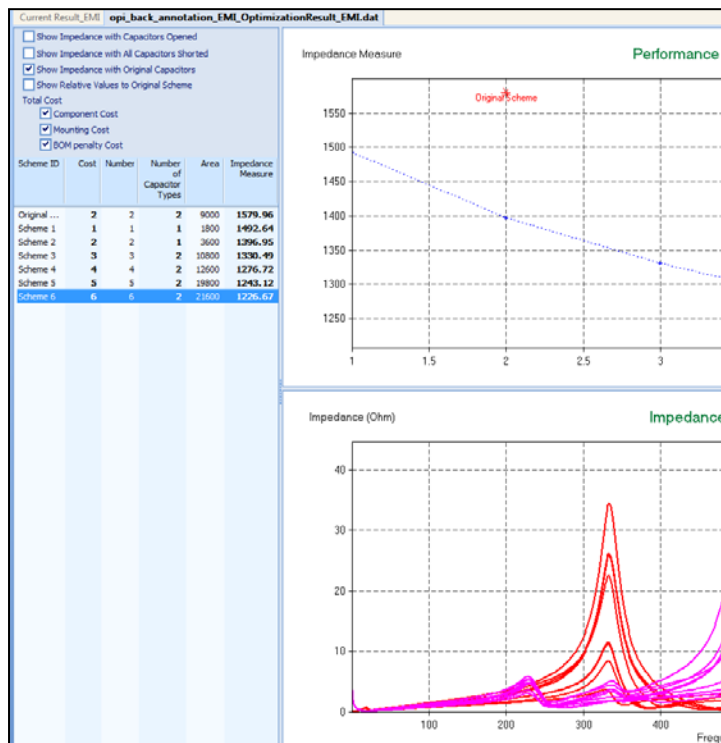
Decoupling capacitor optimization



Integrated AC Solutions

Decap Back-annotation

- Decap Optimization in OptimizePI
 - Simulation in OPI
 - Export scheme data



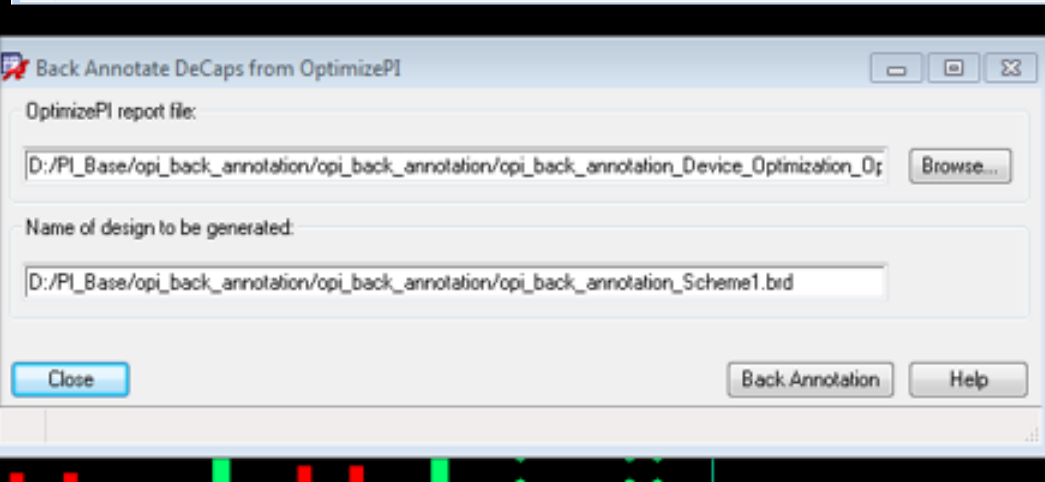
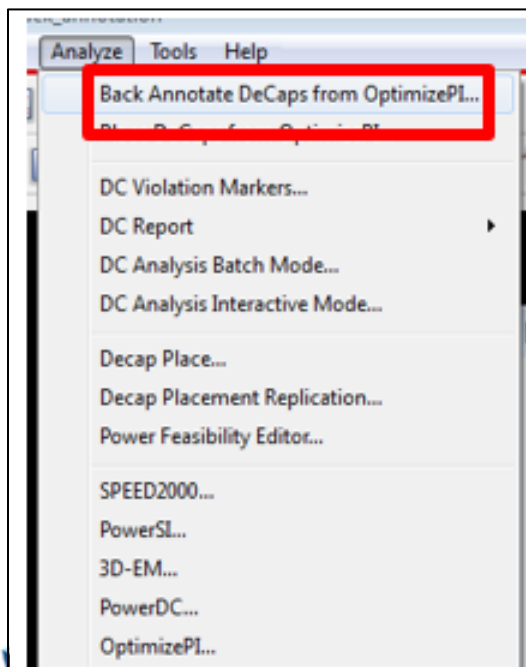
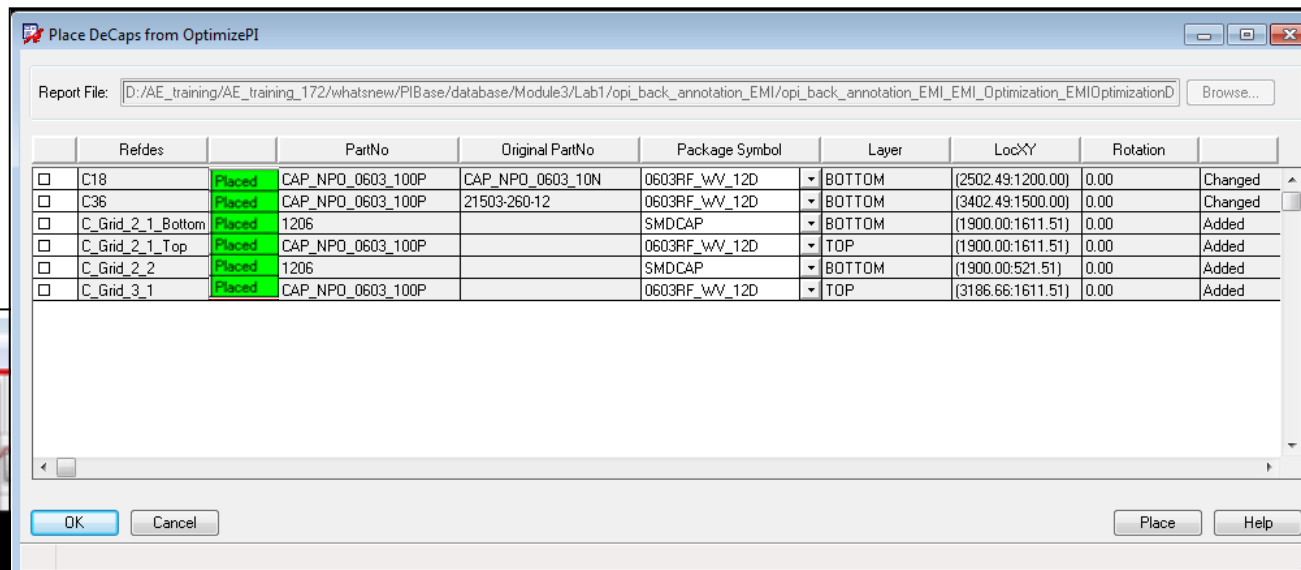
The screenshot shows the 'View Results' section of the OptimizePI workflow. The 'Export Scheme Data' option is highlighted with a red box, and a red arrow points from it towards the 'Scheme Data Export' dialog box.

The screenshot shows the 'Scheme Data Export' dialog box. The 'Generate netlist for Allegro back annotation' checkbox is checked and highlighted with a red box. The 'Scheme 1' dropdown menu is also highlighted with a red box. The 'OK' button at the bottom is also highlighted with a red box.

Integrated AC Solutions

Decap Back-annotation

- Use the original brd file
- Place decaps
 - Auto update



AIC

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Case improved efficiency compared

- In complex PDN case for ten power rail simulation analysis

PDN analysis simulation	Item	Before	Accelerate solution
DC IR-drop analysis	Initial IR-drop analysis	80 min	30 min
	Fix layout	Half day	10 min
	Re-simulation	20 min	10 min
AC decaps optimization analysis	Place decaps	20 min	10 min



Outline

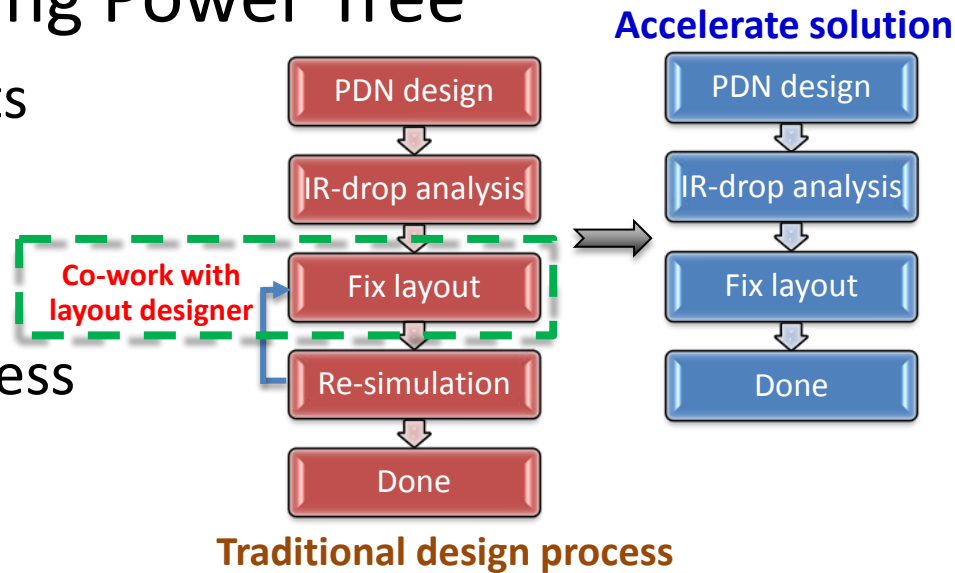
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Summary

- Accelerate DC analysis using Power Tree

- Reduce nearly 50% time costs
- Extract power topologies
- setting automation
- Increase simulation correctness



- Integrated Solutions

- Reduce communication issues
- Reduce modify layout version
- Increasing the overall efficiency of the PDN design



Thank you !

