

阻抗匹配與訊號耦合檢查

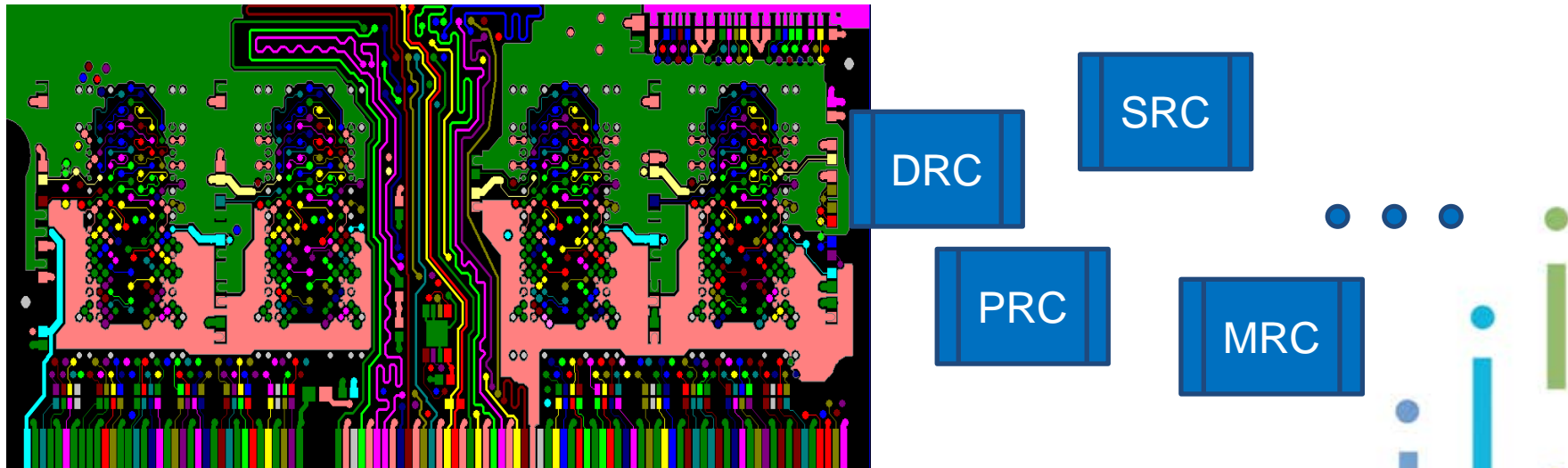
Eric Chen/ Graser

14 / July / 2016



DRC/MRC/...?

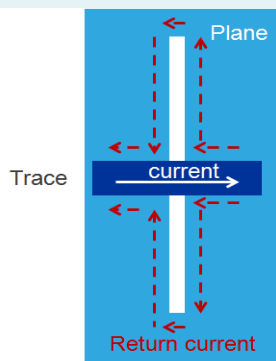
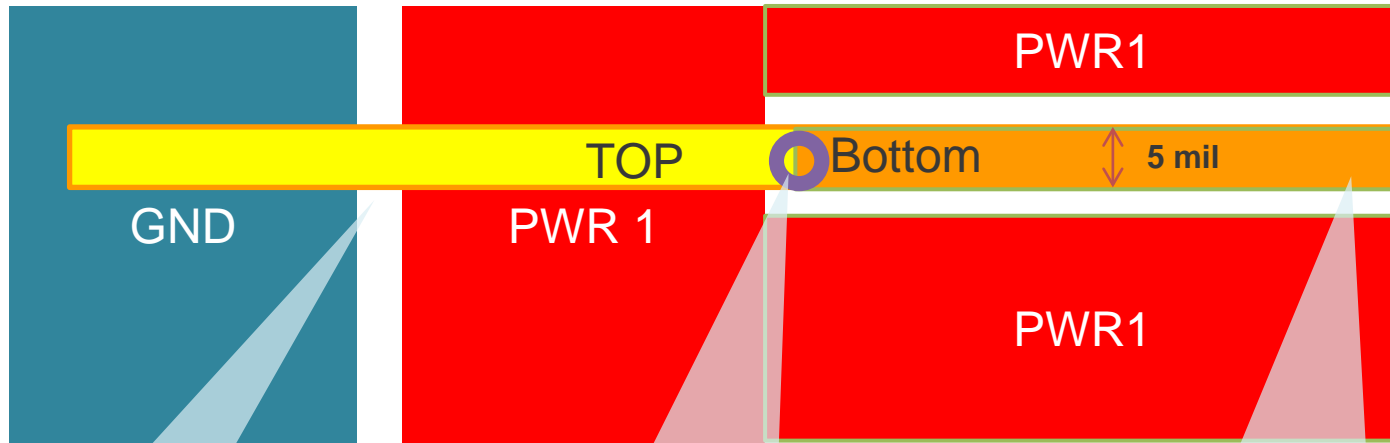
- A bunch of design rules need to implement in your design
- To check and verify layout rules, to meet design requirements



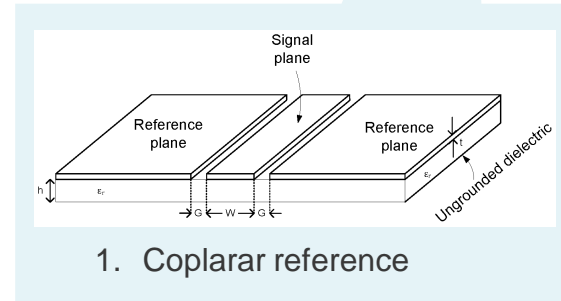
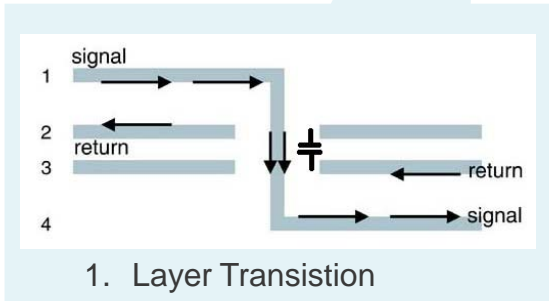
But! How about Layout Quality ?

About SI – Z0 and Xtalk

- Talk about impedance Z0, let's see the following case :
 - After simulation, you set the trace width to be 5 mil in the constraint system to achieve the impedance you want. Of course, the following picture will show **no DRC** violation. **But if this is a 2-layers design and...**



1. Reference change
2. Cross plane split

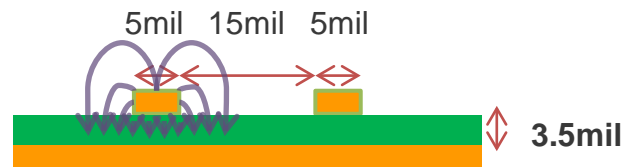


About SI – Z0 and Xtalk

- Talking about crosstalk, you probably follow the 3W rule – set the spacing between adjacent traces to 3 times the width of the trace as the following:



- The 3W rule may work well for the following structure:

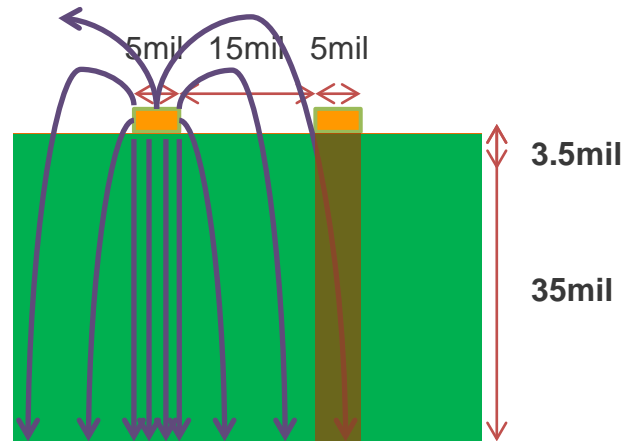


No DRC violation → No Xtalk issue



About SI – Z0 and Xtalk

- But if the stack-up looks like the following, will 3W rule still works well?



No DRC violation → **No Xtalk issue** ?

Now, you're not satisfied with simply spacing constraint or the related **DRC** violation warning. You feel you probably need **simulation** or other way to tell you :

How Much the Coupling is



The gap between DRC and SI performance

- The gap between layout designers and SI engineers is huge
 - Have different design expertise
 - Using different tools
 - Measured by different units



Layout/Board designer

Layout tools

Geometry domain (mil/mm)



SI engineer

Simulation tools

Electrical domain (mv, ps)



OrCAD Sigrity ERC/SRC Checking Flow

BRD
MCM
SiP
ASC
ODB++

Coupling Detailed Table
Upper/Lower Layer Reference Table
Coplanar Reference Table

Impedance between 2 Components
Impedance Plot (collapsed)
Impedance Plot (expanded)
Impedance Table
Impedance Overlay in Layout

Coupling between 2 Components

開啟舊檔

名稱	修改日期
最近的位置	
Desktop - 捷徑	
桌面	
OneDrive	
hicloud Box(e)	
媒體庫	
Subversion	
文件	
音樂	
視訊	
圖片	
DDR3_LRDIMM_SIMetrics	2015/6/9 上午 10...
DDR3_LRDIMM_Trace	2015/6/8 下午 06...
ERC_DDR3_LRDIMM_DataNG_Trace	2015/6/12 下午 0...
SRC_DDR3_LRDIMM_DataNG_SIMetrics	2015/6/8 下午 06...
Trace_Pad_Library	2015/6/9 上午 10...
DDR3_LRDIMM	2015/6/9 上午 10...
ERC_DDR3_LRDIMM_DataNG	2015/6/12 下午 0...
SRC_DDR3_LRDIMM_DataNG	2015/3/5 上午 06...

名稱(N): DDR3_LRDIMM SPEED2000 Files (*.spd;*.dxf;*.brd)

開啟舊檔(O) 取消

ERC

SRC

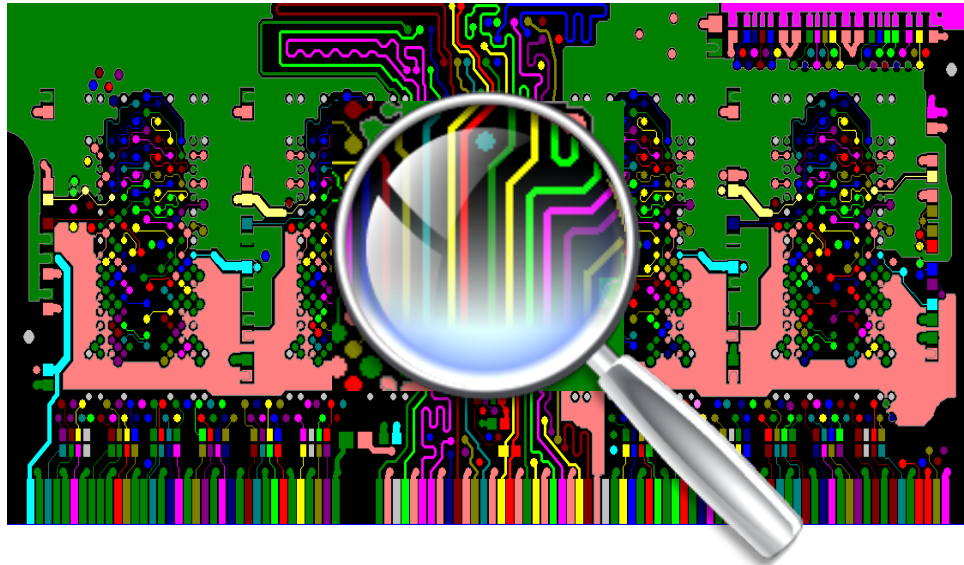
View Only Active Layer
Display Geometry Objects By
 Net Color Layer Color

Layer Selection | Net Manager

Ver-15.0.3.05011 S002 (Trace impedance/coupling check) Mouse(mm): X: 138.982, Y: -21.865 Ready

Why Electrical Rule Check

- ERCs are better than DRCs for 'signal quality' validation
 - Goes beyond **MINIMUM-ACCEPTANCE, GEOMETRY-BASED** constraint validation
- PCB designers identify and address first-order signal quality issues



OrCAD Sigrity ERC

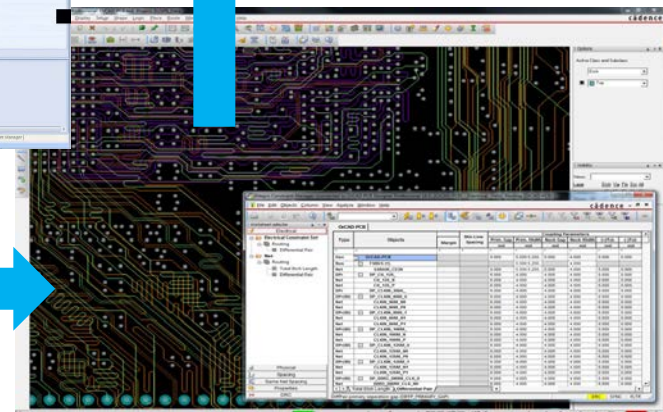
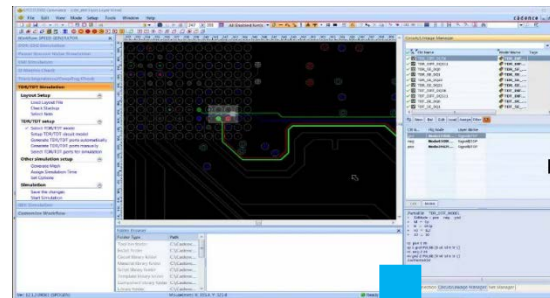
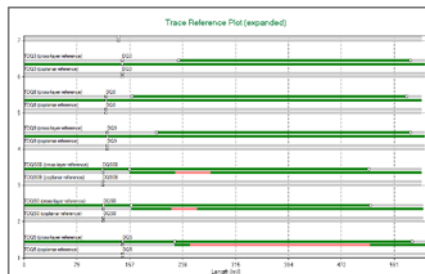
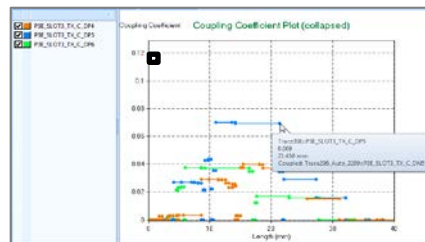
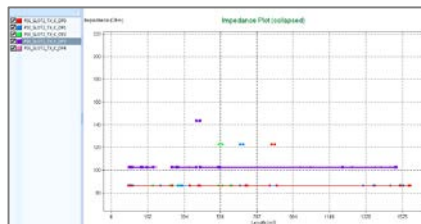
- A comprehensive set of electrical signal quality checks for PCB enabling the PCB designer to make needed changes before more extensive and exhaustive analysis is performed

OrCAD Sigrity ERC

Electrical Rules Analysis

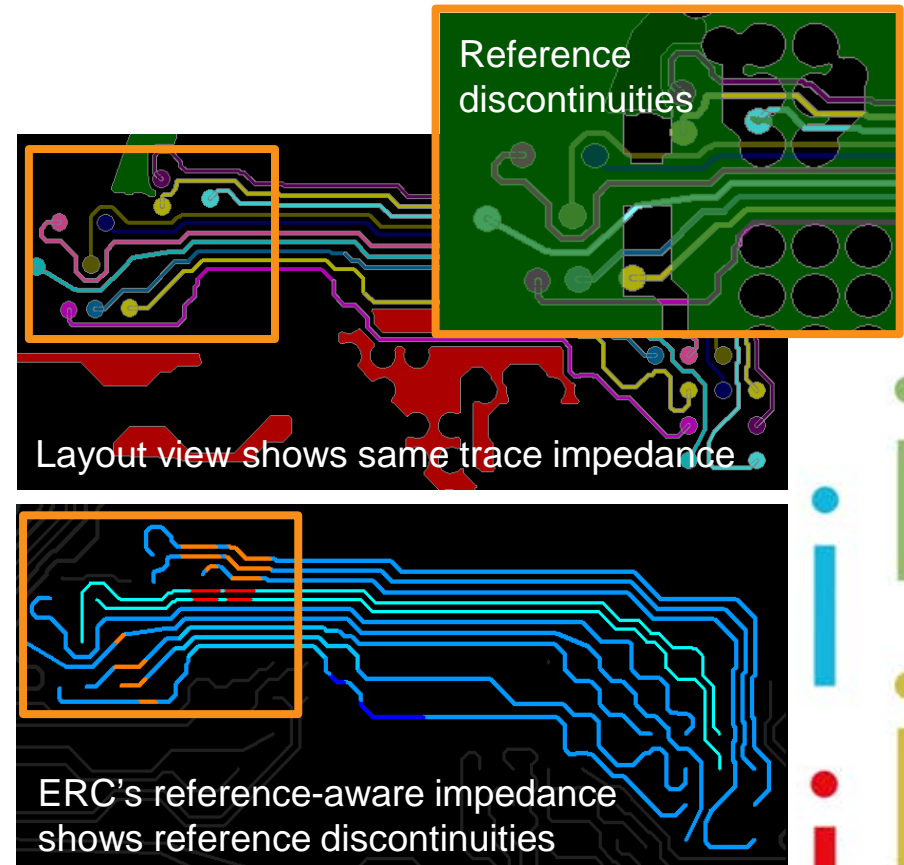
DRCs / ERCs

OrCAD PCB Board



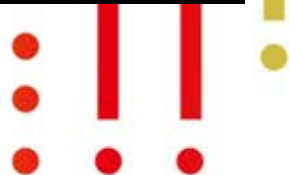
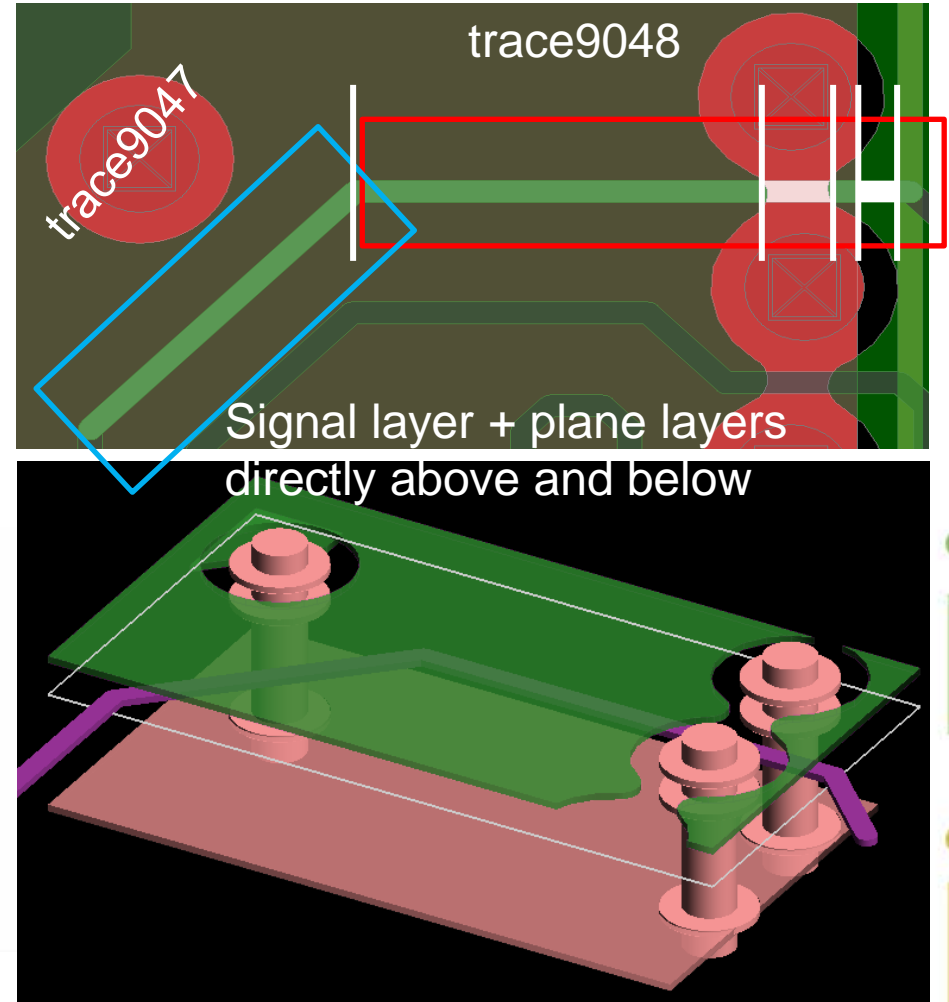
What is Sigrity ERC?

- Sigrity ERC is individual, segment-level view in geometry domain for PCB's SI performance with
 - Trace reference
 - Trace reference-aware impedance
 - Trace reference-aware coupling
 - Differential pair routing phase
 - # of vias and via locations,
 - Practical for board level check (setup, simulation, report)



What is Sigrity ERC?

- If you look close enough...
Two trace segments example
 - **Trace9047:**
one uniform impedance section
 - **Trace9048:**
4 impedance sections



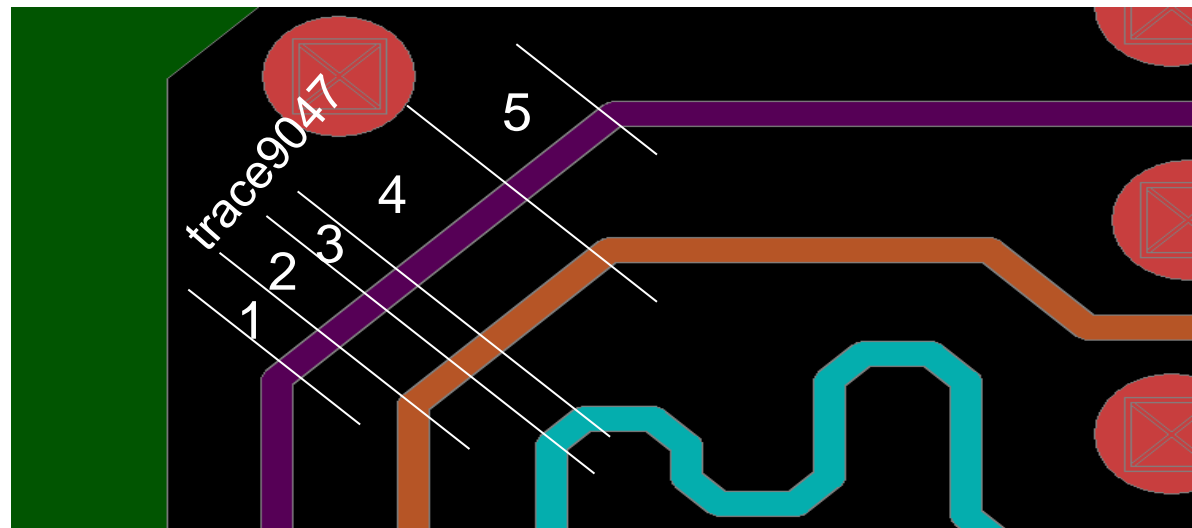
What is Sigridy ERC?

- ERC – Trace coupling

Two trace segments
example

- Trace9047 is one uniform impedance section
- Trace9047 broken into 5 sections based on trace coupling
 - two no coupling sections (1 & 5)
 - two 2-line coupling sections (2 & 4)
 - one 3-line coupling section (3)

ERC results			
Trace Name	Aggressor Trace Names	Coupling Coefficient (%)	Length (%)
Trace9047::DQ0	-	-	← 1 1.82
Trace9047::DQ0	Trace9024::DQ1	5.3	← 2 1.46
Trace9047::DQ0	Trace9024_Auto_190::DQ1	5.3	← 3 1.16
	Trace8280::DQ4	0.6	
Trace9047::DQ0	Trace9024_Auto_191::DQ1	5.3	← 4 4.10
Trace9047::DQ0	-	-	← 5 3.04



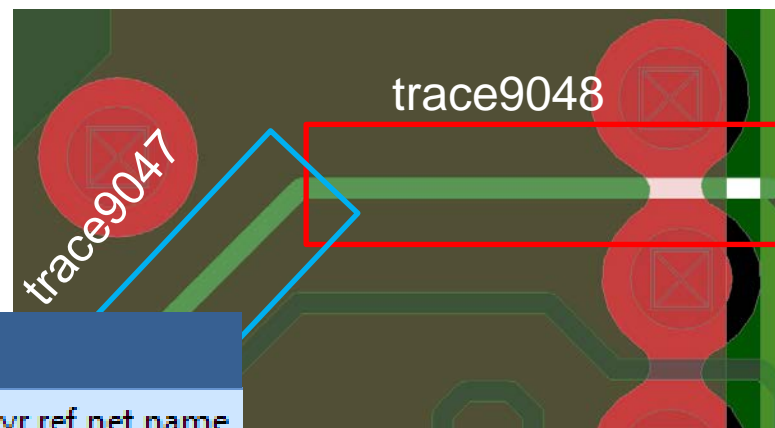
What is Sigrity ERC?

- ERC – Trace upper / lower layer reference

Two trace segments example

– Based on upper / lower layer references

- Trace9047 → one section
- Trace9048 → 5 sections



ERC results

Trace Name	Length (%)	Upper-lyr ref net name	Lower-lyr ref net name
Trace9047::DQ0	11.58	GND	VDD
Trace9048::DQ0	12.74	GND	VDD
Trace9048::DQ0	1.78	VDD	VDD
Trace9048::DQ0	0.11	-	VDD
Trace9048::DQ0	0.89	GND	VDD
Trace9048::DQ0	1.66	GND	GND

*Note:
This is the reason why
there are 5
impedance sections.*



Trace Impedance Check

- P3E_SLOT2_TX_C_DP0
- P3E_SLOT2_TX_C_DP1
- P3E_SLOT2_TX_C_DP2
- P3E_SLOT2_TX_C_DP3
- P3E_SLOT2_TX_C_DP4

Impedance (Ohm)

220

140

120

100

80

0

197

394

591

787

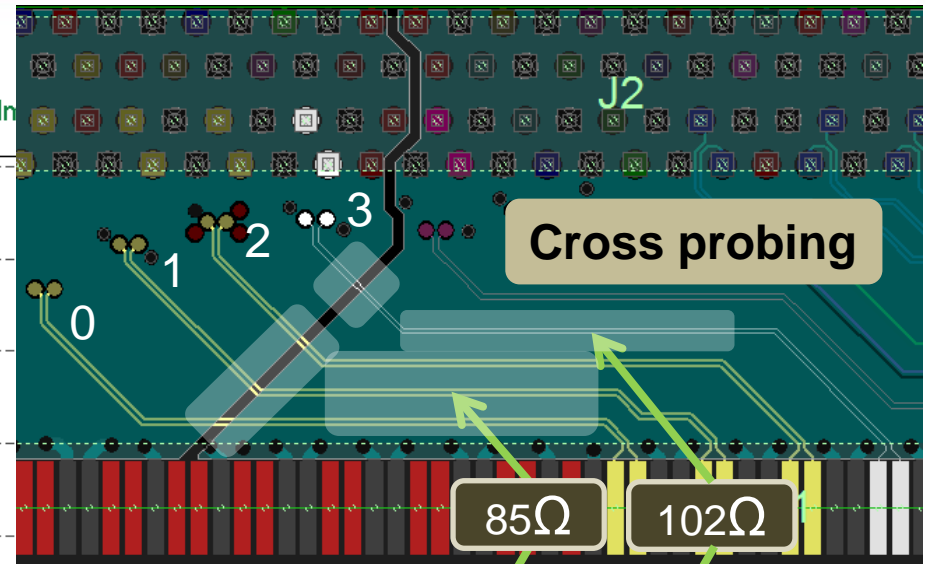
984

1181

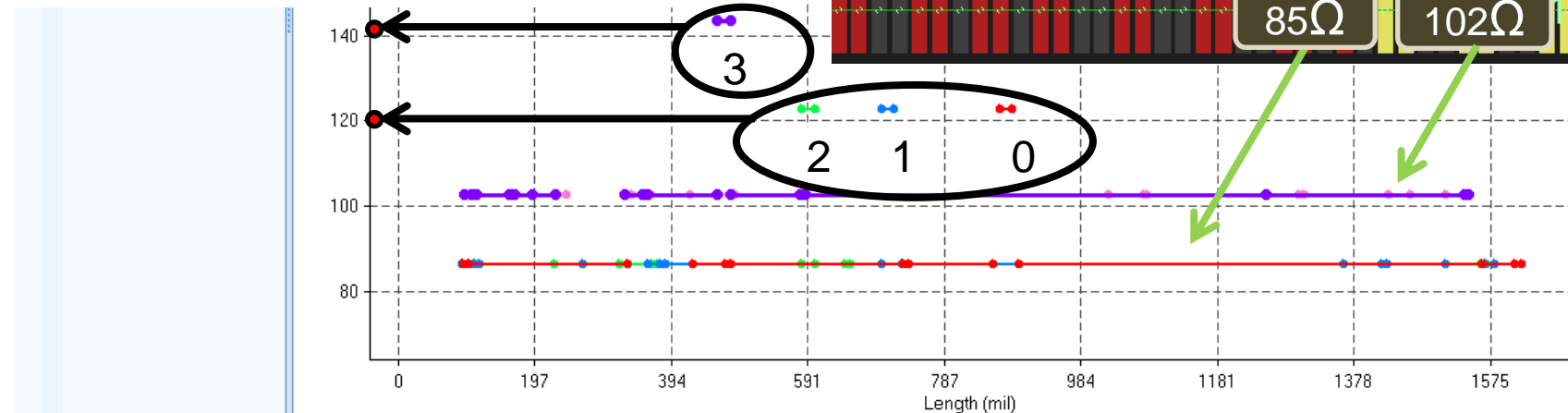
1378

1575

Length (mil)



- This check helps you to identify,
 - Wrong trace width spacing (diff. pair)
 - Cross moat
 - Highly trace impedance

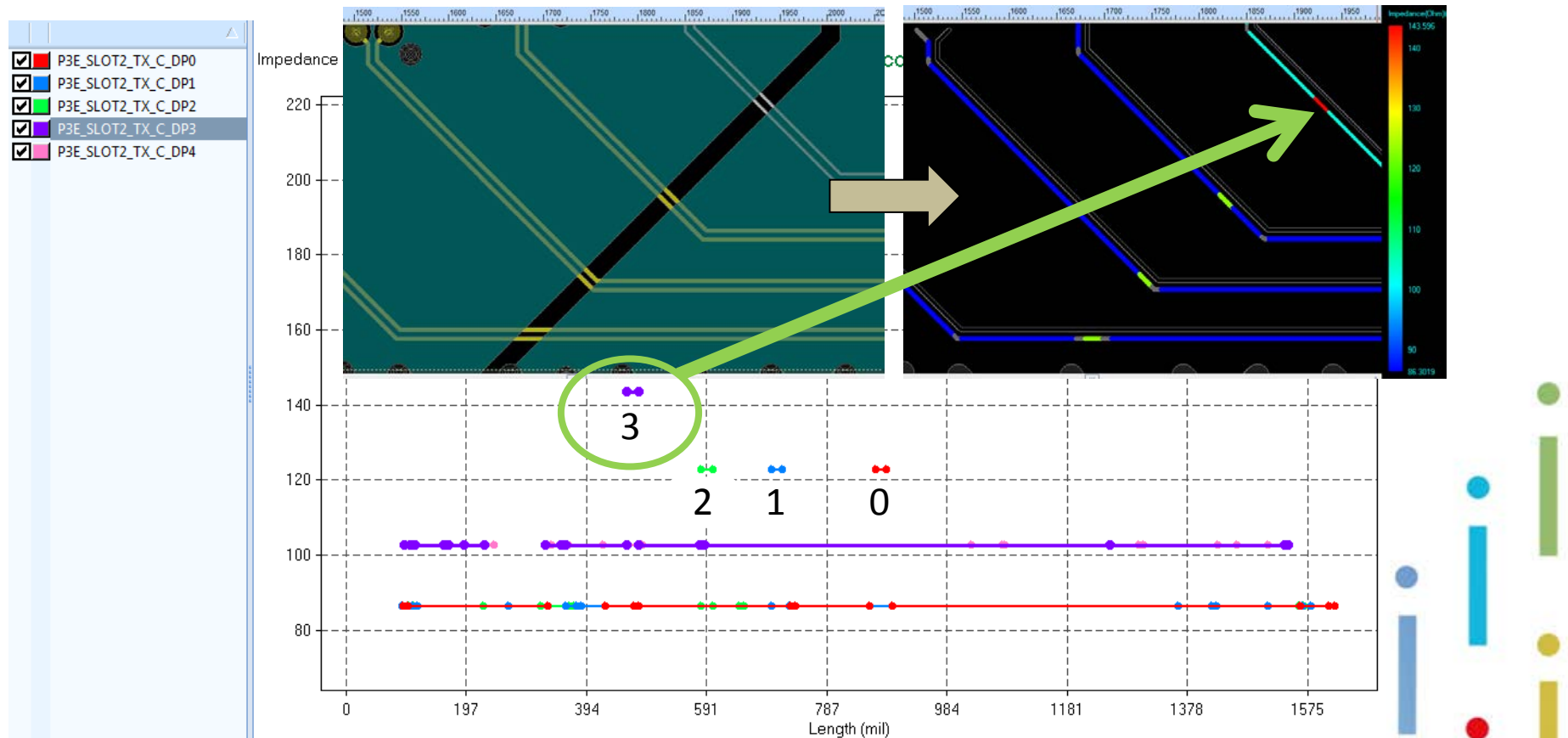


- Visually or tabular result for trace impedance check that shows trace segments mismatch with target impedance.



Trace Impedance Check

Cross Probing

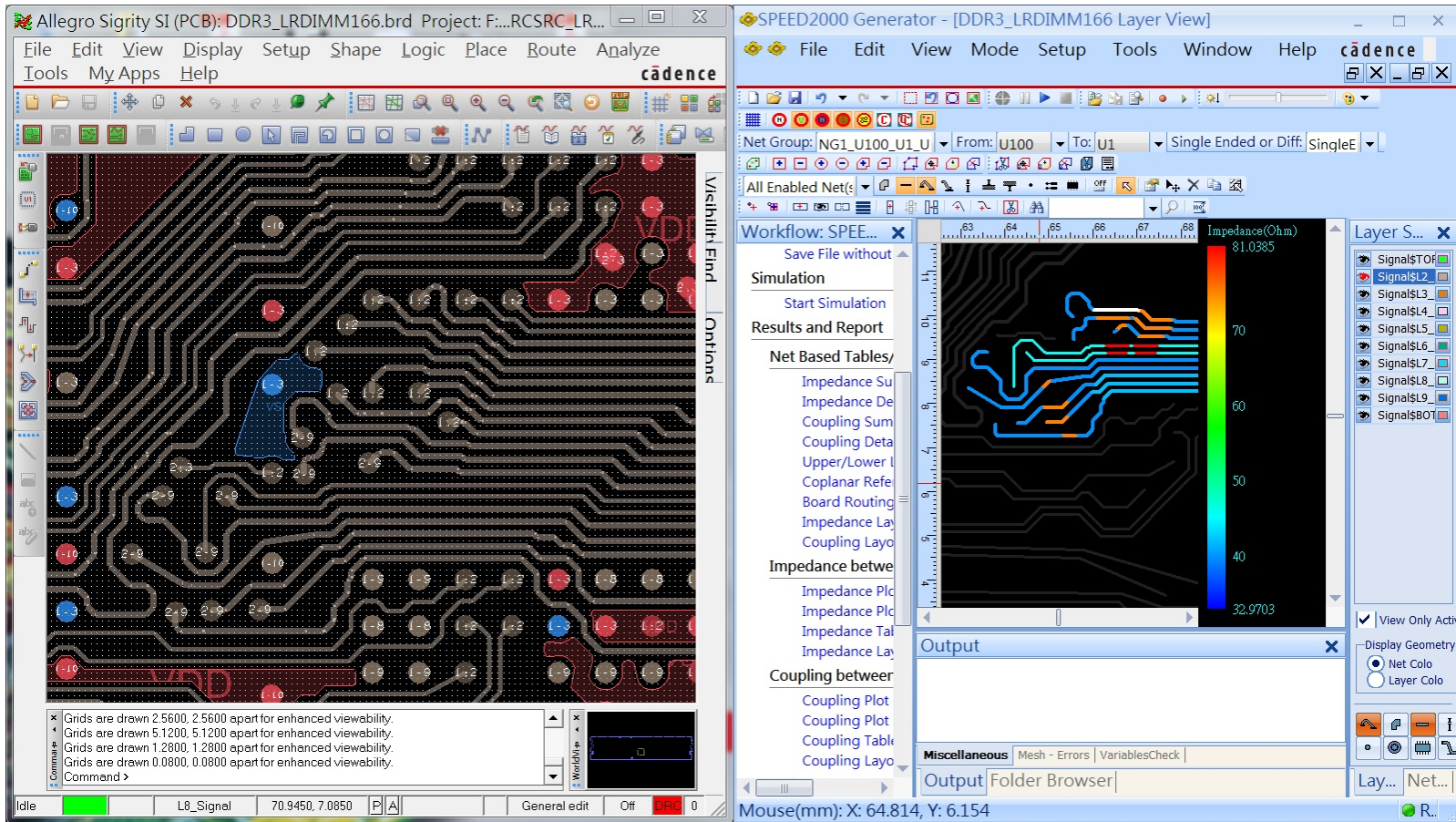


- Cross probing allows you to identify defects quickly.



Trace Impedance Check

Cross Probing



- Auto-Zoom in board .

Trace Impedance Check

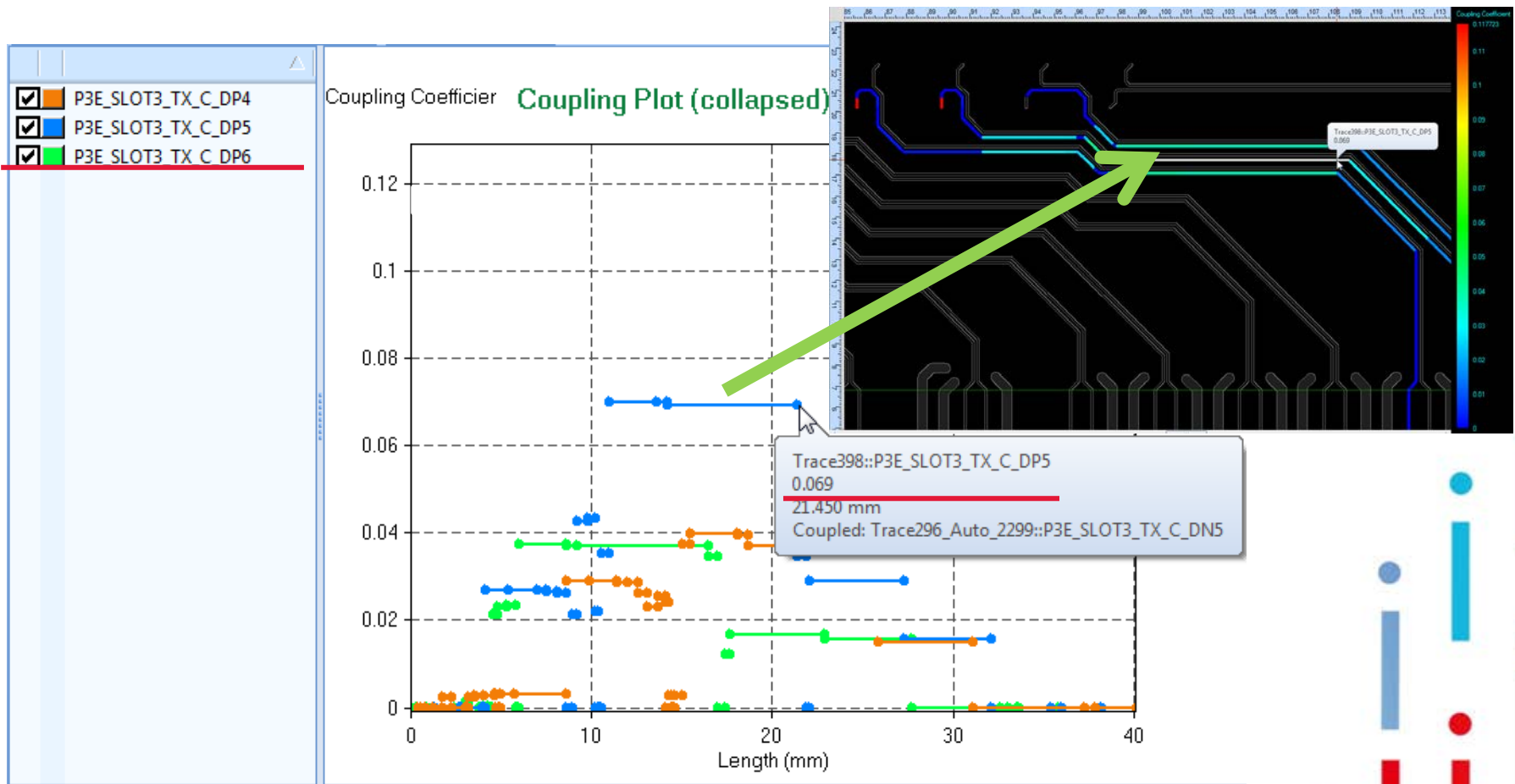
Tabular Results

Net count	Net name	No. of segments without	No. of trace reference discontinuities	No. of vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)	Dominant Impedance (Ohm)	Dominant Imp Length (%)	Trace total length (mil)	Trace delay(ns)
1	P3E_SLOT2_TX_C_DN0	1	3	2	144.946	56.449	56.449	92.921	1633.158	0.233
2	P3E_SLOT2_TX_C_DN1	1	3	2	144.946	56.449	56.449	93.168	1583.722	0.225
3	P3E_SLOT2_TX_C_DN2	1	3	2	144.946	56.449	56.449	93.186	1575.168	0.224
4	P3E_SLOT2_TX_C_DN3	1	3	2	153.005	63.836	63.836	93.074	1549.678	0.220
5	P3E_SLOT2_TX_C_DN4	1	1	2	63.836	63.836	63.836	94.228	1513.121	0.214
6	P3E_SLOT2_TX_C_DP0	1	3	2	144.946	56.449	56.449	92.923	1633.643	0.233
7	P3E_SLOT2_TX_C_DP1	1	3	2	144.946	56.449	56.449	93.221	1583.404	0.225
8	P3E_SLOT2_TX_C_DP2	1	3	2	144.946	56.449	56.449	93.184	1574.865	0.224
9	P3E_SLOT2_TX_C_DP3	1	3	2	153.005	63.836	63.836	93.059	1546.528	0.219
10	P3E_SLOT2_TX_C_DP4	1	1	2	63.836	63.836	63.836	94.221	1511.225	0.214
11	P3E_SLOT3_TX_C_DN0	1	1	1	56.449	56.449	56.449	94.142	1490.958	0.211

- Cross moat?
- Any trace segment mismatch? Cross moat?
- Too much breakout neck length?
- Too much MS/SL routing difference in a group?
- The same trace length means the same trace delay?
- Routing on MS/SL has different trace delay.

Trace Coupling Check

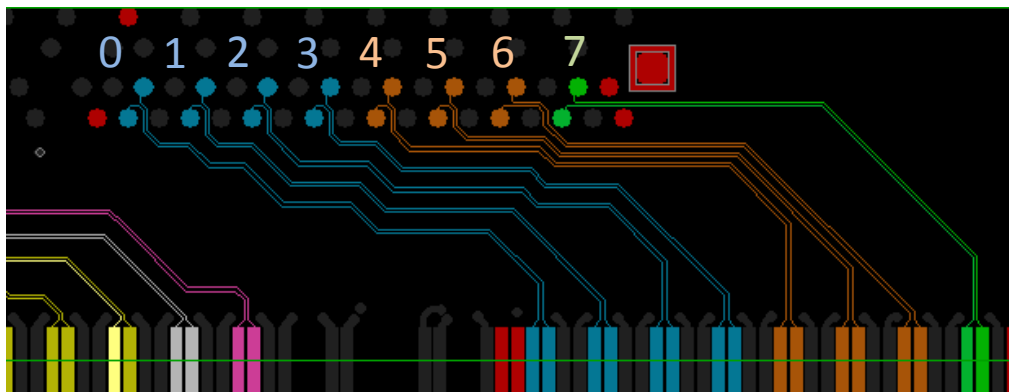
Cross probing helps to resolve issue intuitively



Trace Coupling Check

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
1	P3E_SLOT2_TX_C_DP0-P3E_SLOT2_TX_C_DN0	P3E_SLOT2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
2	P3E_SLOT2_TX_C_DP1-P3E_SLOT2_TX_C_DN1	P3E_SLOT2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
3	P3E_SLOT2_TX_C_DP2-P3E_SLOT2_TX_C_DN2	P3E_SLOT2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
4	P3E_SLOT2_TX_C_DP3-P3E_SLOT2_TX_C_DN3	P3E_SLOT2_TX_C_DN2	0.125%	36.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.125%	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

18X

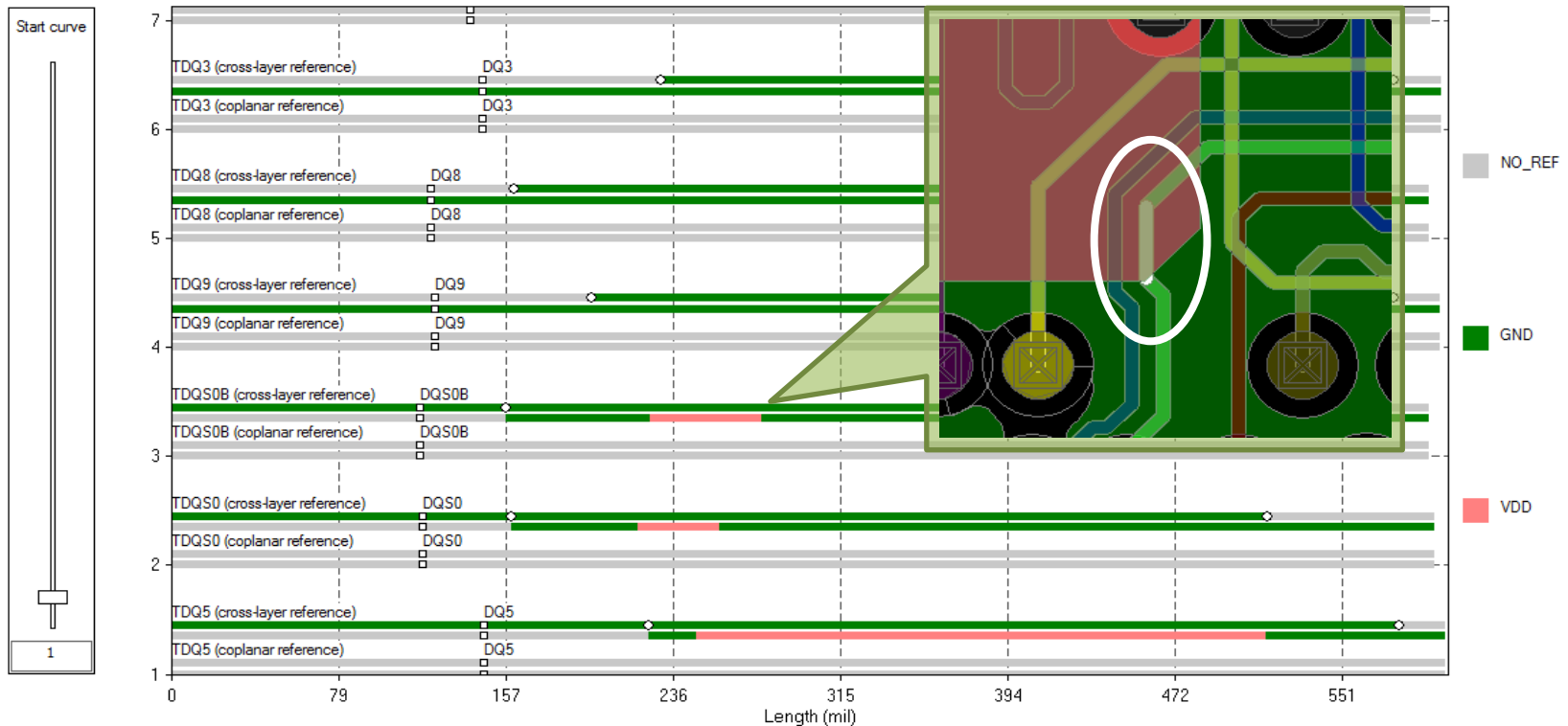


Through this test, you will see,

- Tight coupling pairs
- Max coupling aggressor
- Dangerous vs. safe coupling
→ **18X** (= 2.81% / 0.156%)

Trace Reference Check (Including co-planar)

Trace Reference Plot (expanded)



- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer



OrCAD Sigrity ERC/SRC Checking Flow

BRD
MCM
SiP
ASC
ODB++

Coupling Detailed Table
Upper/Lower Layer Reference Table
Coplanar Reference Table

Impedance between 2 Components
Impedance Plot (collapsed)
Impedance Plot (expanded)
Impedance Table
Impedance Overlay in Layout

Coupling between 2 Components

開啟資料夾

名稱	修改日期
最近的位置	
Desktop - 捷徑	
桌面	
OneDrive	
hicloud Box(e)	
媒體庫	
Subversion	
文件	
音樂	
視訊	
圖片	
DDR3_LRDIMM_SIMetrics	2015/6/9 上午 10...
DDR3_LRDIMM_Trace	2015/6/8 下午 06...
ERC_DDR3_LRDIMM_DataNG_Trace	2015/6/12 下午 0...
SRC_DDR3_LRDIMM_DataNG_SIMetrics	2015/6/8 下午 06...
Trace_Pad_Library	2015/6/9 上午 10...
DDR3_LRDIMM	2015/6/9 上午 10...
ERC_DDR3_LRDIMM_DataNG	2015/6/12 下午 0...
SRC_DDR3_LRDIMM_DataNG	2015/3/5 上午 06...

標籤名稱(N): DDR3_LRDIMM

SPEED2000 Files (*.spd;*.dxf;*.brd)

開啟資料夾(O) 取消

ERC

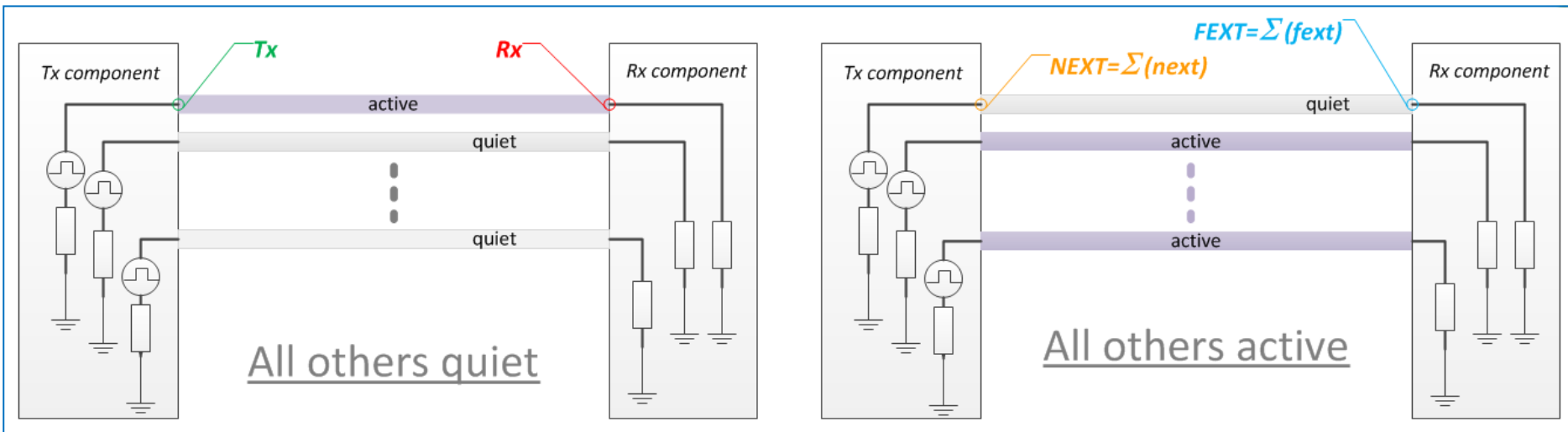
SRC

Ver-15.0.3.05011 S002 (Trace impedance/coupling check) Mouse(mm): X: 138.982, Y: -21.865 Ready

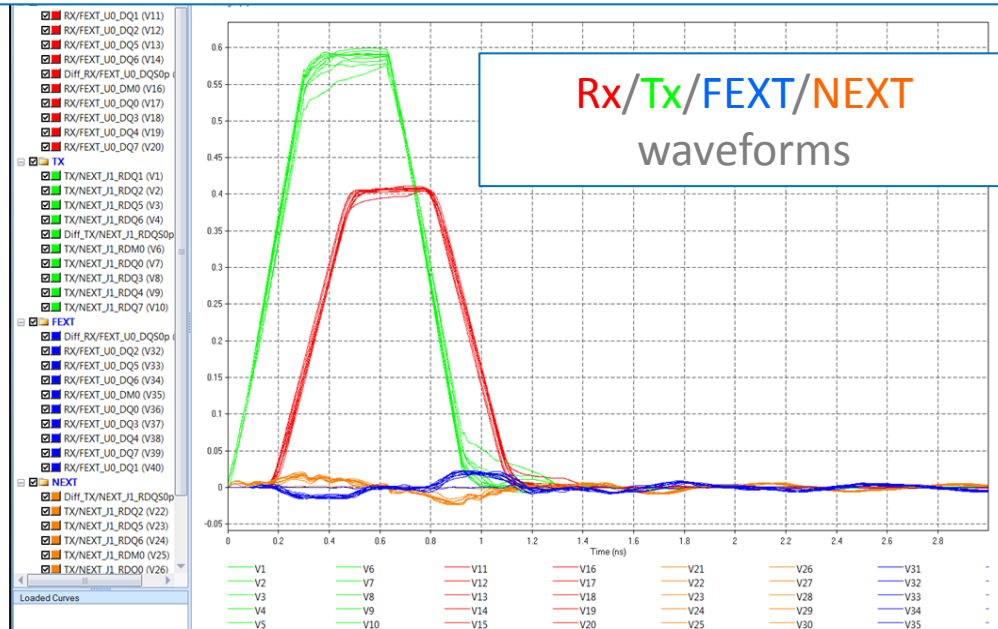
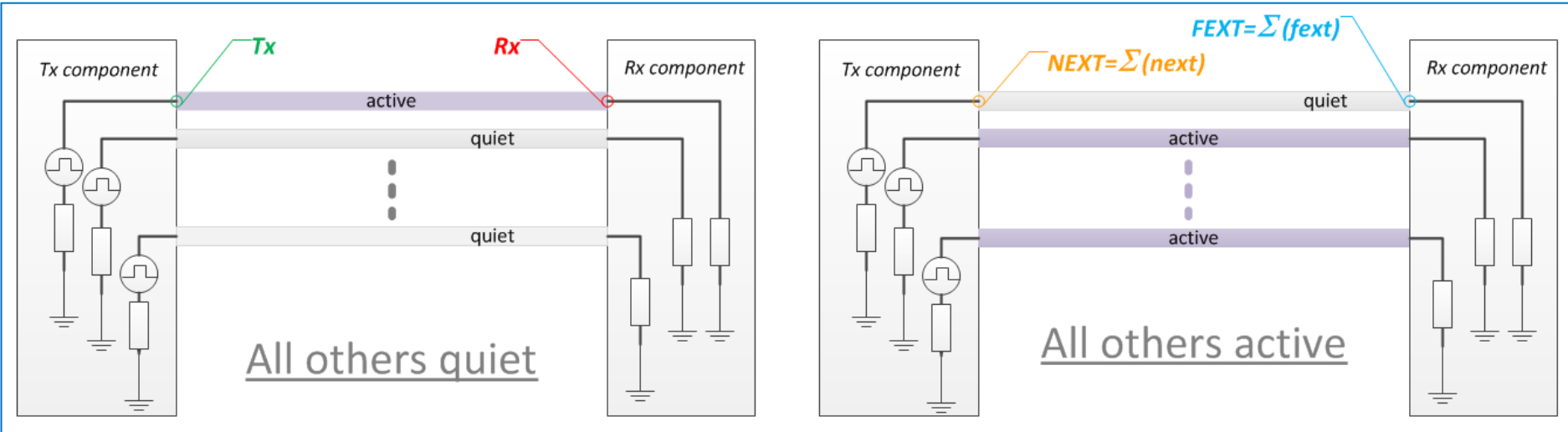
What is Sigrity SRC?

- Sigrity SRC is Macro, combined, net-level view in time-domain of impact due to ERC violations measured in mv & ps (no device model needed)
 - Setup considering termination impedance, data rate (pulse width, rise/fall time), and amplitude
 - Results with Tx/Rx/NEXT/FEXT waveforms, SI performance metrics
 - Organized to easy SI performance interpretation along with ERC
- Practical for board level check (setup, simulation, report)

<2min ~ 20min auto



Time-domain waveforms SRC – SI Metrics Check



SRC Setup

- Device models are not needed
- Voltage pulse as stimulus, users can specify
 - Amplitude
 - Data rate (pulse width, rise/fall time)
 - Termination

Set up SI Metrics Check Wizard

Set up Tx/Rx Models

Import Tx/Rx Models Export Tx/Rx Models

Interface and ckt type	Tx_term type	R(ohm)	C(F)	V_low(V)	V_high(V)	Tdelay(s)	T_r(s)	T_f(s)	T_w(s)	T_period(s)	Rx_term type	R(ohm)	C(F)	(S)Rx_term type	(S)R(ohm)	(S)C(F)
NG1:SE	R	40	-	0	1	0p	100p	100p	525p	30n	R	40	-	R	5000	-
NG1:Diff	R	40	-	0	0.5	0p	100p	100p	525p	30n	R	40	-	R	5000	-

Set up Simulation Option

Level-1 (Single lines with ideal PDN; delay, loss, reflection effects)
 Level-2 (Coupled lines with ideal PDN; plus trace, via xtalk effects)
 Level-3 (Coupled lines with non-ideal PDN; plus return path and SSO effects)
 Level-4 (3DFEM model based; lack of reference cases) From SPEED2000

Transient Time Step (ps):

Coupling (%):

Rise Time (ps):

Sim Time: ns

OK Cancel

Net-level Performance Ranking *SRC – SI metrics check*

Net name	INT_Sig (V*ps)	INT_ISI (V*ps)	INT_XTK (V*ps)	SN_difference (V*ps)	SN_ratio
DQ19	287.97	22.96	3.7	261.31	10.8029
DQ17	288.15	22.79	3.12	262.24	11.1223
DM2	286.52	24.21	3.04	259.28	10.5156
DQS2_P	206.59	104.05	0	102.54	1.98541
DQ20	286.71	23.94	3.14	259.63	10.5871
DQ21	288.2	22.68	5.43	260.09	10.2522
DQ16	286.51	24.21	0	262.3	11.834
DQ22	286.46	24.06	1.6	260.8	11.1639
DQ18	286.47	24.12	0	262.34	11.8752
DQ23	286.65	24.13	7.81	254.71	8.97519

← Ranking by SI Metrics

Net name	NEXT Vmax (mv)	NEXT Vmin (mv)	NEXT pk-2-pk (mv)	FEXT Vmax (mv)	FEXT Vmin (mv)	FEXT pk-2-pk (mv)
DM1	0	0	0	0	0	0
DQ10	0	0	0	0	0	0
DQ11	0	0	0	0	0	0
DQ9	19	-18	37	14	-15	29
DQ12	17	-15	32	16	-16	32
DQ8	2	-2	5	3	-3	6
DQ14	0	0	0	0	0	0
DQS1_P	0	0	0	0	0	0
DQ15	17	-16	33	13	-13	27
DQ13	19	-18	37	14	-14	29

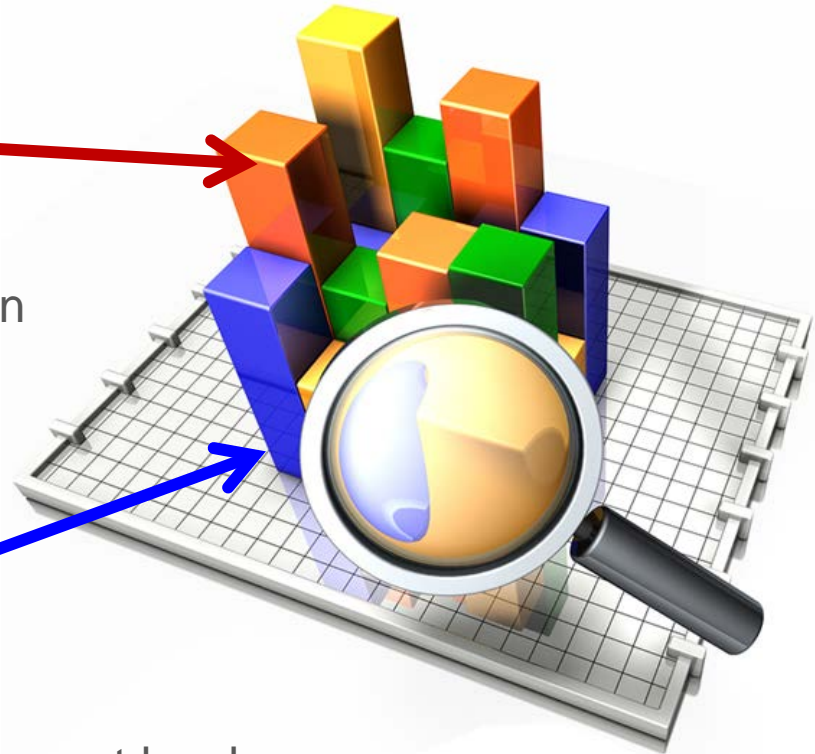
← Ranking by xtalk levels



SRC Net-level View → ERC's Segment-level View

Sigrity SRC

- Layout SI macro view at net level
- All inclusive end results
- Shows what happened and its effect on performance



Sigrity ERC

- Layout SI micro level view at segment level
- Individual segmented results
- Shows why low performance happened and how to fix it



Summary

- **Sigrity ERC/SRC** fills the gap between layout designers and SI engineers
 - Expanded expertise
 - Using **same** tools
 - Measured by **same** units



Layout/Board designer -----> *SI engineer*

Layout tools -----> *Simulation tools*

Geometry domain (mil/mm) -----> *Electrical domain (mv, ps)*



PCB 製造之 DFM 解決方案

Eric Chen / Graser

14 / July / 2016

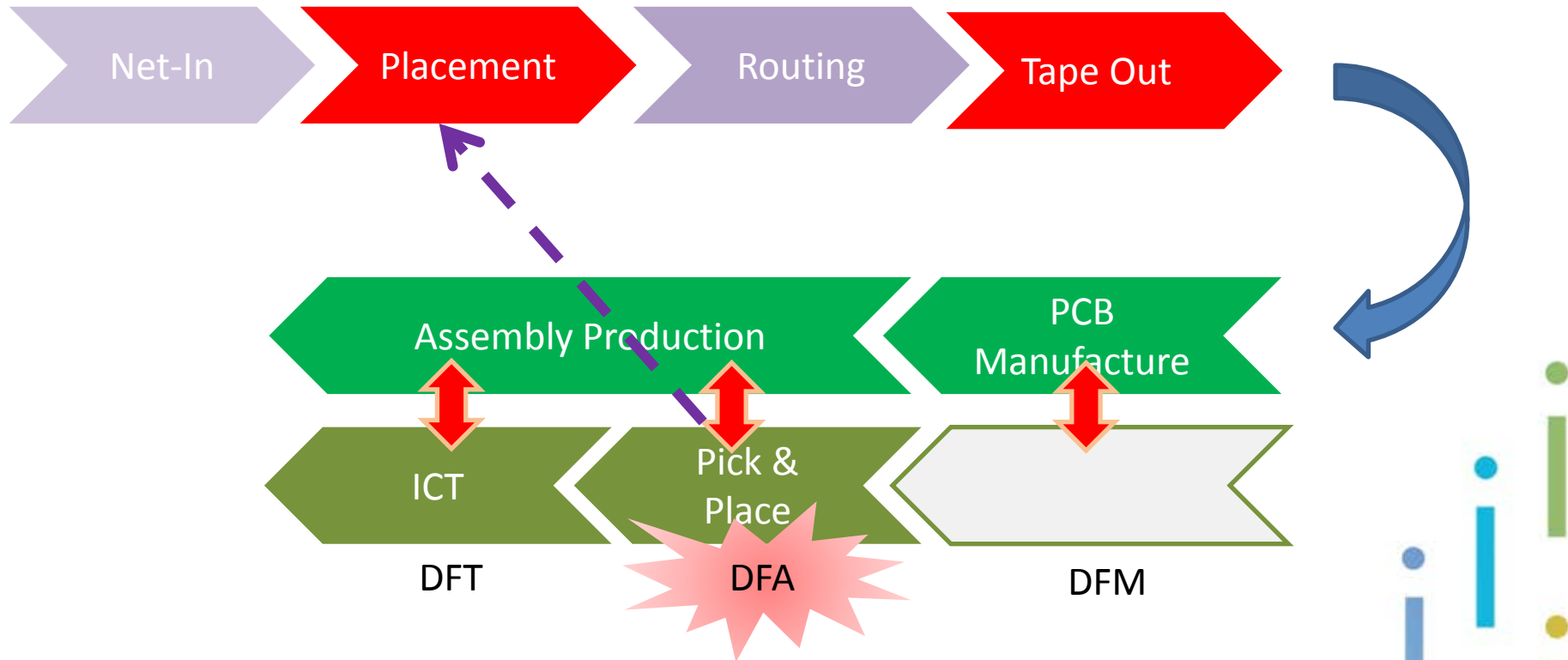


Topic

1. Review Design Flow
2. Review production issue from PCB manufacture & Assembly line.
3. What we have in Allegro PCB Designer?



What we need DFX Checker

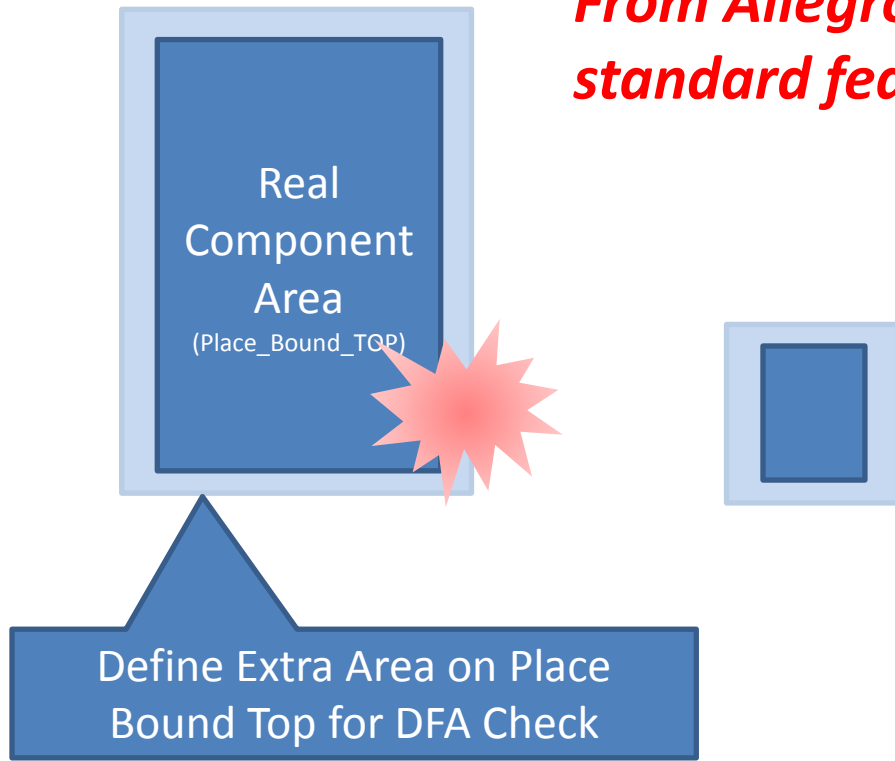


Design for Assembly Check



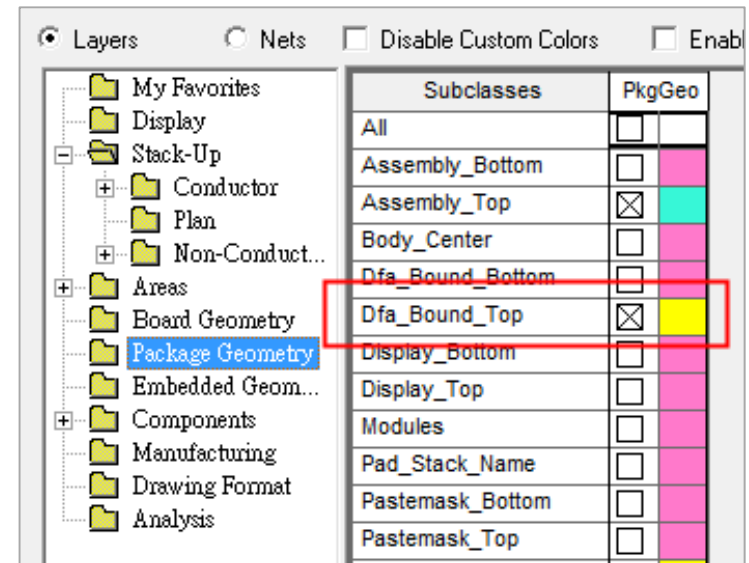
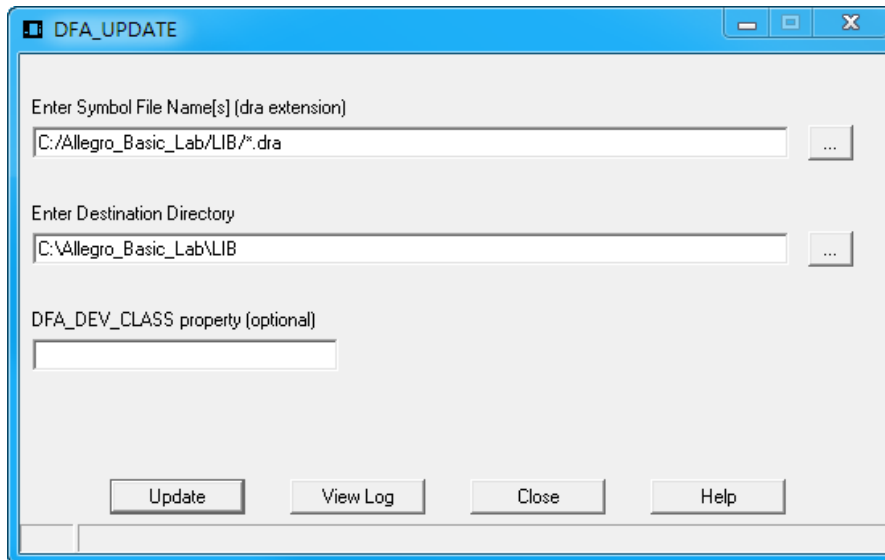
Allegro DFA Constraint

From Allegro® V16.5 , the DFA check is standard feature in Allegro PCB Designer.



Allegro DFA Constraint

- Define DFA_Bound_Top/Bottom
- Define Correct area
- Classify DFA Class or add DFA_Bound_Top/Bottom, when you needed.



Define DFA Spreadsheet Editor & Rule

- Edit / Constraint / DFA Constraint Spreadsheet

DFA Constraints Dialog - External DFA Table: Untitled

File Edit

DRC mode

- On
- Off
- Batch

S:S E:E S:E E:S

Column Row Column Row Column Row Column Row

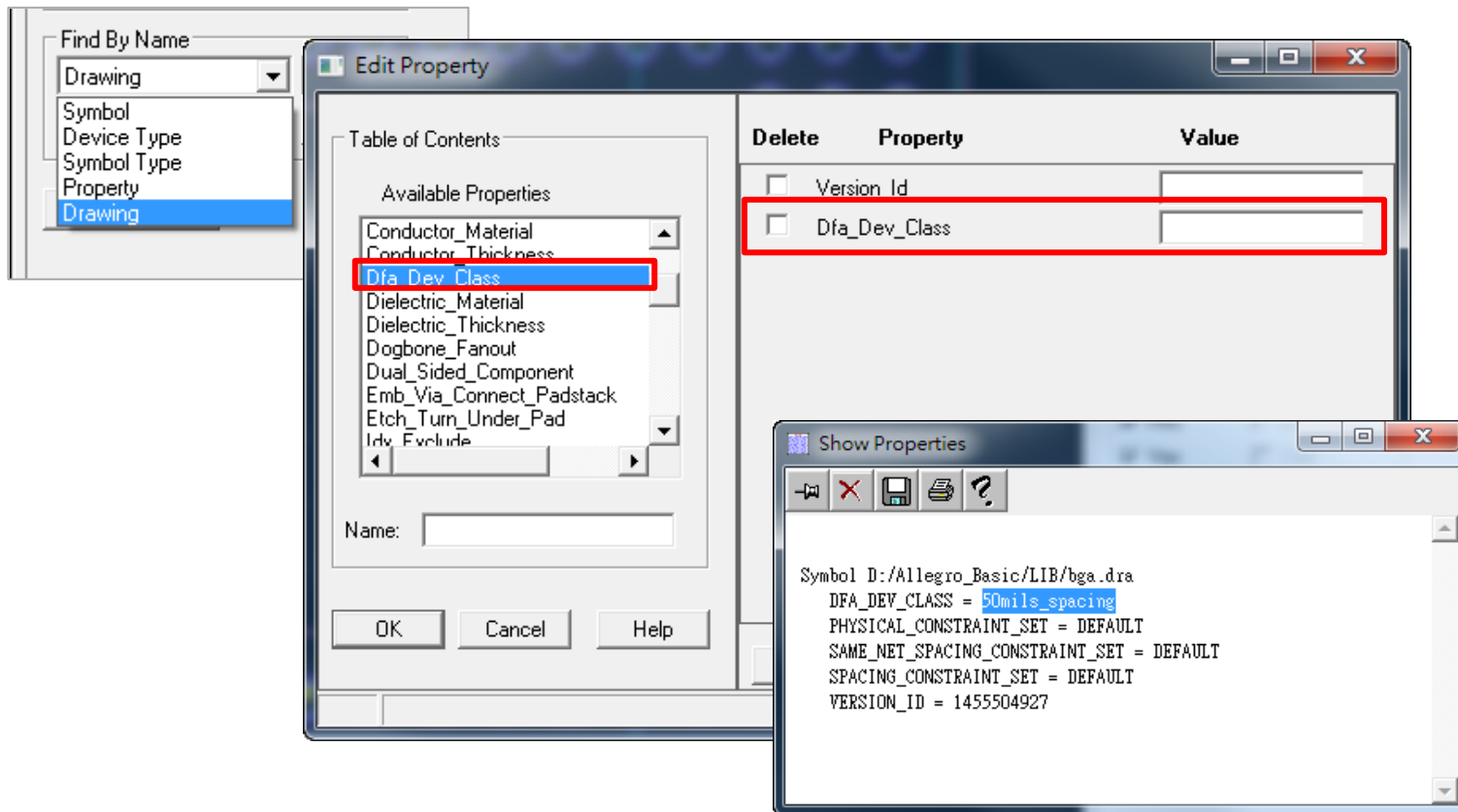
DFA spreadsheet format: (Side to Side):(End to End):(Side to End):(End to Side)

Default: 50:100:50:50 Apply to selected cells Mils Read only

	CONN_DIP_	DIP8	DIP14	DIP16	LED-DIP150	RES1130	SMDCAP	SMDRES	SOIC24
CONN_DIP_2	100								
DIP8	60	60							
DIP14	50:100:50:50	50:100:50:50	50:100:50:50						
DIP16	50:100:50:50	50:100:50:50	50:100:50:50	50:100:50:50					

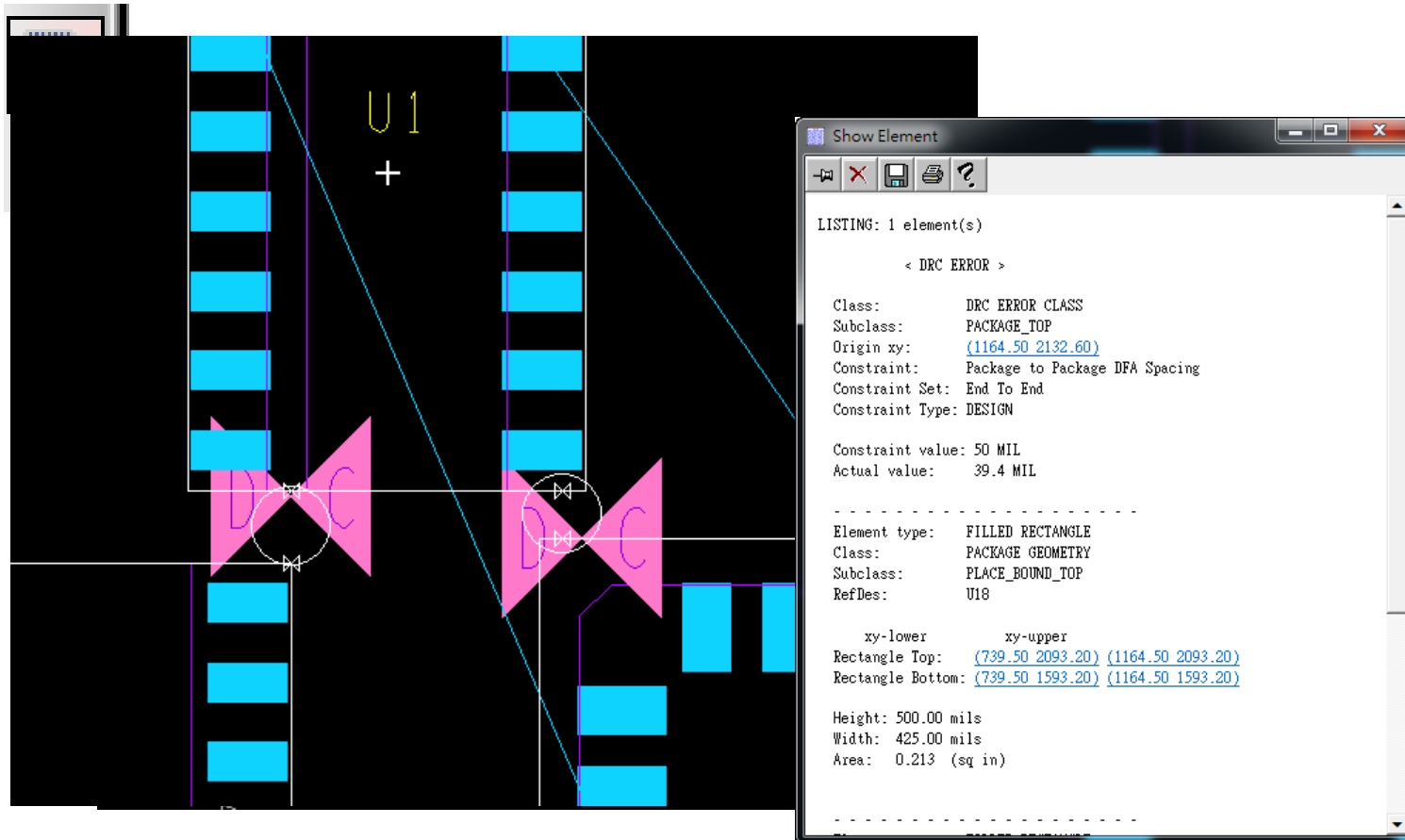
Define DFA Device Class

- Using DFA Update to classify DFA Class
- Edit Drawing property



DFA DRC Marker

- DFA Clearance Control



The DFM Solution for PCB Manufacture



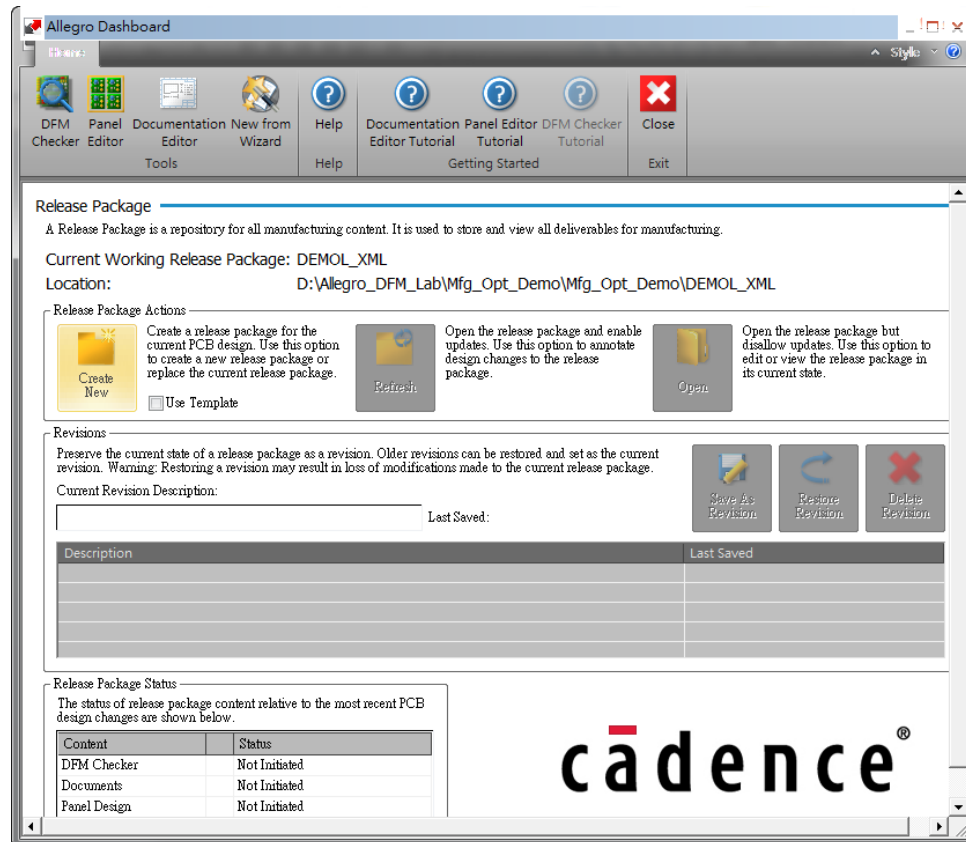
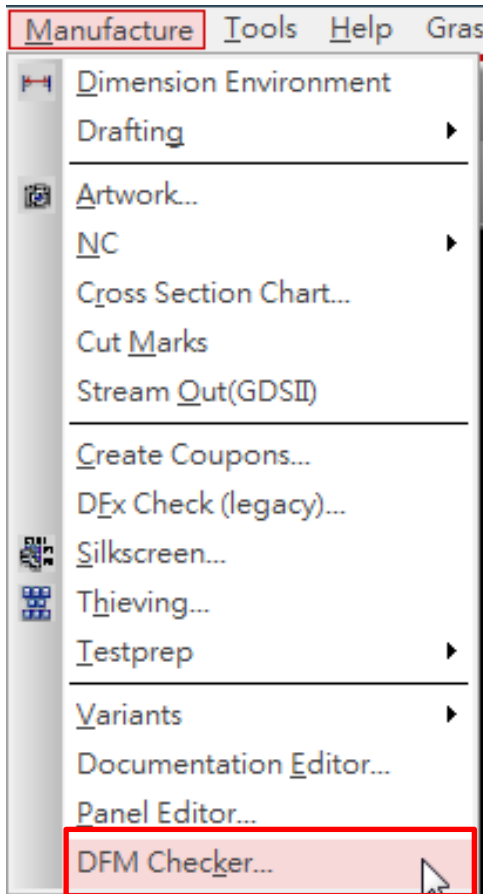
Why do we need to do DFM check?

1. Make sure manufacture date is correct and good for PCB manufacture.
2. Vision same as PCB Factory.
3. Identify problems early , reduce re-work probability.



Allegro PCB Manufacturing Option

- 16.6 S045 or later



DFM Check Rules

- Features

	Check Category	Data category
Etch	Logic	Netlist compare
	Graphic Check	Signal layer
		Power plane
Non-Etch	Graphic Check	Solder mask
		Silkscreen
		Paste mask
		NC data
Analysis	Statistics	Analysis Report



DFM Check Rules

- **Netlist Compare**
 - Import External Netlist, Extract CAM Netlist, Run Netlist Compare
- **Signal Layer**
 - Track to Track, Track to Pad, Pad to Pad, Pad to Drill, Minimum Track, Minimum Pad, Unplated Drills to Copper, Plated Drills to Copper, Copper to One-Up-Border, Redundant Pads, Plated Drills without Pads, Pads without Drills, Antennas, Minimum Gap, Minimum Width, Acid Traps, Copper Slivers, Pin Holes
- **Positive Plane**
 - Plated Drills to Copper, Unplated Drills to Copper, Pads to Drills, Acid Traps, Copper Slivers, Pin Holes, Minimum Gap, Minimum Width
- **Negative Plane**
 - Plated Drills to Copper, Unplated Drills to Copper, Pads to Drills, Copper to One-Up-Border, Isolated Thermal, Starved Thermal, Thermal Conflict, Tie Width



DFM Check Rules

- **Soldermask**
 - Pad to Mask, Drill to Mask, Mask Slivers, Soldermask Bridge, Pin Holes, Soldermask to Track, Missing Soldermask
- **Silkscreen**
 - Silkscreen to Soldermask, Minimum Soldermask Width
- **NC Data Layer**
 - Overlapping Hits, Coincidental Hits, Redundant Hits, Drill to Drill, Imploded Arcs, Imploded Path, Mill Tab Errors
- **Pastemask**
 - Pastemask on Through Holes, Missing Pastemask on SMD Pads, Missing Soldermask for Pastemask Pads, Pastemask to Copper clearance
- **Design Analyzer**
 - Design Analysis reporting, including User Parameter specifications, Calculated design analysis and customized output formatting.



Netlist Compare

Property	Value
<input checked="" type="checkbox"/> Preprocess Optimization 0 - Optimization Preprocess	
<input checked="" type="checkbox"/> Netlist Compare 1 - Netlist Compare	
Name	Netlist Compare 1
Actions	Import, Extract, Run
<input type="checkbox"/> Details	
<input checked="" type="checkbox"/> Import External Netlist	
File name	...
Netlist type	IPC-D-356A
<input checked="" type="checkbox"/> Extract CAM Netlist	
<input type="checkbox"/> Allow CAM nets without pads	
<input type="checkbox"/> Allow Single Point CAM net	
<input type="checkbox"/> Treat Neg Planes as Single CAM net (no splits in Plane)	
<input checked="" type="checkbox"/> Run Netlist Compare	
<input type="checkbox"/> Ignore Extra External Nets at CAM Points	
<input type="checkbox"/> Ignore Missing External Nets for CAM Nets	
<input checked="" type="checkbox"/> Signal Layer 2 - Signal Layer check	
<input checked="" type="checkbox"/> Negative Plane 3 - Negative Plane check	

Checks Constraints Areas Results

Specific external Netlist file(IPC-D-356 format)

可選擇IPC-D-356或 IPC-D-356A



Constraint Region Check

The image shows a software interface for configuring constraint regions. On the left, a tree view shows the hierarchy: Electrical > Physical > Spacing > Spacing Constraint Set > Net > Net Class-Class > Region. The 'Region' folder is selected.

The main table lists constraints for the 'POWER-REGION' region. The 'Line To' section is expanded to show specific values for various constraint types.

Objects			Line To									
Type	S	Name	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bond Finger	Hole
			mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		demol	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	8.0000
Rgn		POWER-REGION	8.0000	8.0000	6.0000	8.0000	8.0000	8.0000	10.0000	10.0000	5.0000	10.0000

The bottom table shows the configuration for the 'POWER-REGION_Outer_Electrical - Signal Layer check'.

POWER-REGION_Outer_Electrical - Signal Layer check	
Name	POWER-REGION_Outer_Electrical
Layers	[Outer Electrical]
Drill Layers	[All NC]
Checks	TT, TC, CC, TP, CP, CPCP, SMSM, VV, LV, W, THTH, SMV, SMLV, SMTH, VTH, LVTH, DTHC, DT...
Shape/Size Filter	
NC Tool Filter	
Area	POWER-REGION_All_Electrical
<input type="checkbox"/> Auto Fix Errors	
Details	
<input checked="" type="checkbox"/> Board Outline spacing	
<input checked="" type="checkbox"/> Copper spacing (Different Nets)	
<input checked="" type="checkbox"/> TT - Track to Track	8.000000
<input checked="" type="checkbox"/> TC - Track to Copper	10.000000
<input checked="" type="checkbox"/> CC - Copper to Copper	12.000000
<input checked="" type="checkbox"/> TP - Track to Pad	10.000000
<input checked="" type="checkbox"/> CP - Copper to Pad	10.000000
<input checked="" type="checkbox"/> Pad spacing	
<input checked="" type="checkbox"/> Drill spacing	
<input checked="" type="checkbox"/> Annular Ring	

Arrows indicate the mapping of values from the top table to the bottom table:

- Red arrow: Line (8.0000) to TT (8.000000)
- Blue arrow: Test Via (10.0000) to TC (10.000000)
- Red arrow: Shape (10.0000) to CC (12.000000)
- Blue arrow: Bond Finger (5.0000) to TP (10.000000)
- Red arrow: Hole (10.0000) to CP (10.000000)



Results & Cross Probing

Allegro PCB Designer (was Performance L): demo.lbrd Project: D:\Mfg_Opt_Demo

File Edit View Add Display Setup Shape Logic Place FlowPlan Route Analyze Manufacture Tools Help GraserWARE ADIVA Interface cadence

Refresh Constraints
Cross Probe
PCB Integration

DRC error "Externally Determined Violation" Bottom
Constraint value: 5.0000
Actual value: 4.9843 mils

Zoom to errors in PCB
Lock Layer Visibility
Hide Validated Errors
Error Chart
Stream List

demoL - Advanced Streams DFM

Id	Distance	Layer	X1	Y1	X2	Y2	Min Dist	Validated	Com...
8	14.1421	L5:LYR4_(VCC)	3755.0000	-325.0000	3765.0000	-335.0000	15.0000	<input type="checkbox"/>	

MW - Minimum Width - 1 Errors, 0 Hidden

Id	Min Width	Layer	X	Y	Max Size	Max Noise	Validated	Comm...
9	4.9843	L7:BOTTOM	-56.4680	1047.0661	5.0000	50	<input type="checkbox"/>	

Solder Mask Layer 4 - 2606 Errors, 0 Hidden

SMDM - SMD to Mask (Annular Ring) - 464 Errors, 0 Hidden

Id	Dist...	Layer	Layer	X1	Y1	X2	Y2	Pad S...	S/M ...	Min ...	Validated	Com...
10	2.5000	L10:SOLD...	L1:TOP	822.5...	1862....	822.5...	1865....	55.00...	50.00...	3.0000	<input type="checkbox"/>	
11	2.5000	L10:SOLD...	L1:TOP	822.5...	1912....	822.5...	1915....	55.00...	50.00...	3.0000	<input type="checkbox"/>	
12	2.5000	L10:SOLD...	L1:TOP	822.5...	1912....	822.5...	1915....	55.00...	50.00...	3.0000	<input type="checkbox"/>	

Summary

- Embedded Systems Design , Easy to Use.
- Cross Probing between Checker and Allegro® / OrCAD® PCB Designer

**Confirm the correctness of the information
before sending to your partner.
Ensure smooth production.**



New Exchange Format IPC-2581

- Generic Requirements for Printed Board
- Assembly Products Manufacturing Description Data and Transfer Methodology

Name	Full	Design			Fabrication			Assembly			Test			
		1	2	3	1	2	3	1	2	3	1	2	3	
Hierarchical layer/stack instance files	█		█											
Hierarchical conductor routing files	█		█											
BOM (Components and Materials)	█	█	█	█	█	█	█	█	█	█		█	█	
AVL (Components and Materials)	█		█	█		█	█	█	█	█			█	█
Component Packages	█	█	█	█			█	█	█	█			█	█
Land Patterns	█		█	█			█		█	█			█	█
Device Descriptions	█	█	█	█					█	█			█	█
Component Descriptions	█	█	█	█				█	█	█			█	█
Soldermask ; Solder Paste Legend Layers	█			█	█	█	█	█	█	█			█	█
Drilling and Routing Layers	█			█	█	█	█	█	█	█			█	█
Documentation Layers	█	█	█	█	█	█	█	█	█	█			█	█
Net List	█	█	█	█			█	█	█	█			█	█
Outer Copper Layers	█			█	█	█	█	█	█	█			█	█
Inner Layers	█			█	█	█	█	█	█	█			█	█
Miscellaneous Image Layers	█		█	█			█	█	█	█			█	█
DFX Analysis	█	█	█	█	█	█	█	█	█	█			█	█



New Exchange Format IPC-2581

- Using IPC-2581 data format
 - All artwork film record must be defined
 - IPC-2581 Layer mapping must be defined



Ravel Rule Checker

Does Traditional Design Rule Checker Enough?

Now You Can Self-development it .

A New DFM Rule Checker - Ravel Rule Check



Ravel Rule Checker

The screenshot displays the 'DFM Ravel Rules GUI' window. On the left, a menu bar includes 'Manufacture', 'Tools', and 'Help'. Below it, a list of manufacturing tools is shown, with 'Setup RAVEL Rules in CM...' highlighted by a red box. The main window is divided into two panes: 'PCBRules' and 'UserDefinedRules'. The 'UserDefinedRules' pane shows a tree view of rule categories, with 'Text to exposed PinPad Spacing on Top Layer' selected and highlighted by a red box. A red arrow points from this rule to a preview image of a PCB layout showing pinpads. Another red arrow points from the same rule to a table of constraints. The table has two columns: 'Constraint Name' and 'Value(mils)'. The first row is highlighted with a red box and contains the text 'MIN_TXT_TO_EXP_PINPAD_TOP_D' and the value '1'. At the bottom of the window, the 'Apply' button is highlighted with a red box.

Constraint Name	Value(mils)
MIN_TXT_TO_EXP_PINPAD_TOP_D	1

RAVEL DRC Overview

Advantages

- Rapid development of custom DRC upon demand
- Reduced DRC implementation effort
 - RAVEL DRC language is specialized for expressing design rules in PCB and SiP
 - Does not require knowledge of SKILL or C/C++ programming languages
 - Does not require knowledge of Allegro® PCB/SiP database

Case 1: 2 rules	C/C++	RAVEL
Lines of code	1200	80
Effort	10 days	2 hours

Case 2: 4 rules	SKILL	RAVEL
Lines of code	1540	470
Effort	15 days	3 days

- Reduced DRC maintenance effort
 - RAVEL rules are independent of database
 - RAVEL rules are independent of SPB software release
 - All dependencies are built into RAVEL DRC engine



Thank You!

