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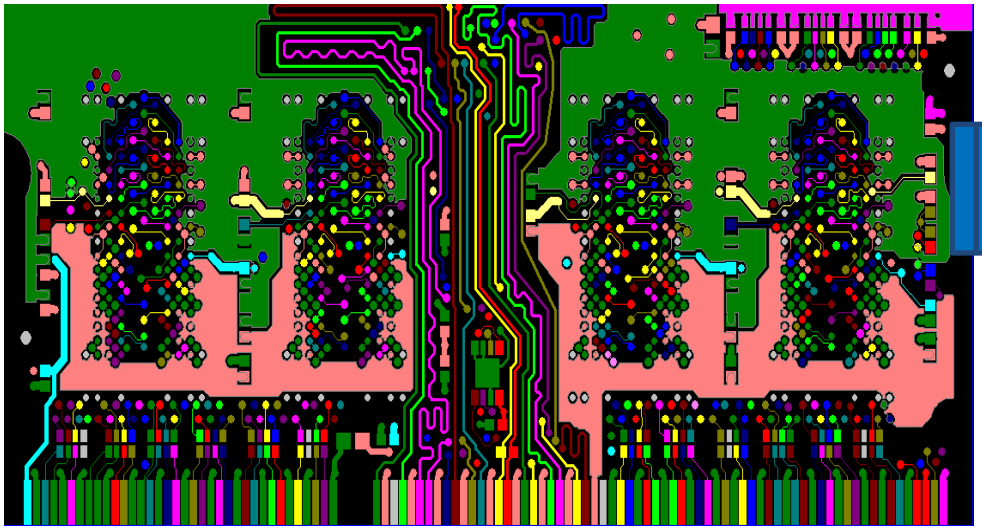
阻抗匹配與訊號偶合檢查

Eric Chen/ Graser

14 / July / 2016

DRC/MRC/…?

- A bunch of design rules need to implement in your design
- To check and verify layout rules, to meet design requirements



DRC

SRC

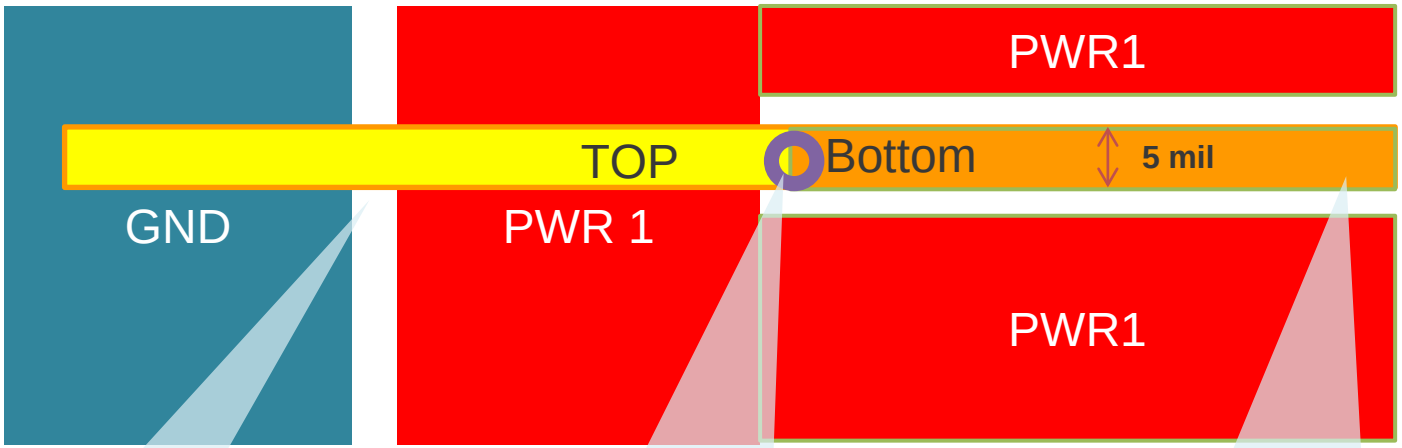
PRC

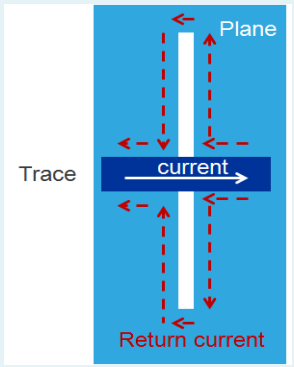
MRC

But! How about Layout Quality ?

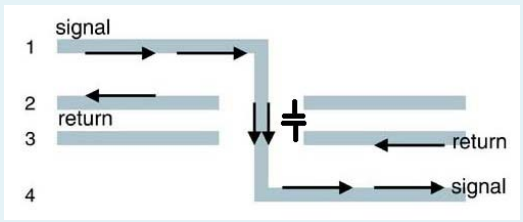
About SI – Z0 and Xtalk

- Talk about impedance Z0, let's see the following case :
  - After simulation, you set the trace width to be 5 mil in the constraint system to achieve the impedance you want. Of course, the following picture will show **no DRC** violation. **But if this is a 2-layers design and…**

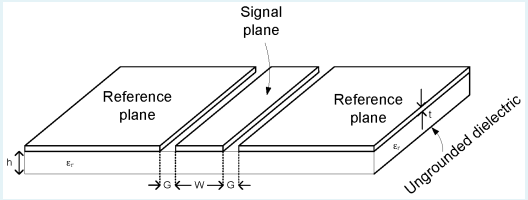




1. Reference change
2. Cross plane split



1. Layer Transistion



1. Coplarar reference

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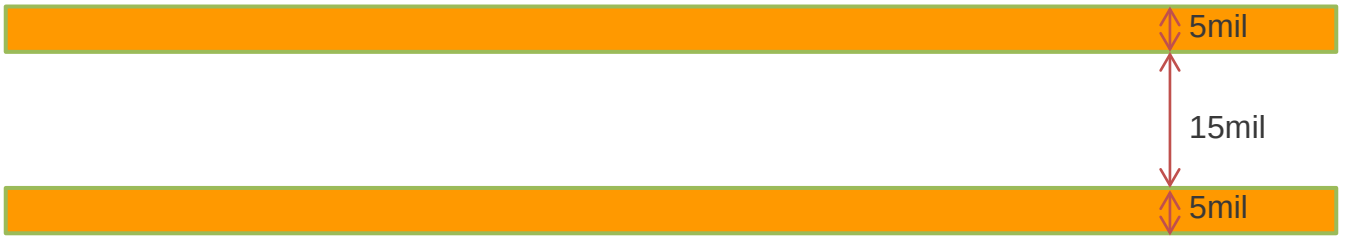
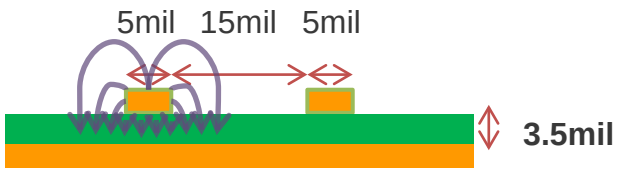
About SI – Z0 and Xtalk

- Talking about crosstalk, you probably follow the 3W rule – set the spacing between adjacent traces to 3 times the width of the trace as the following:



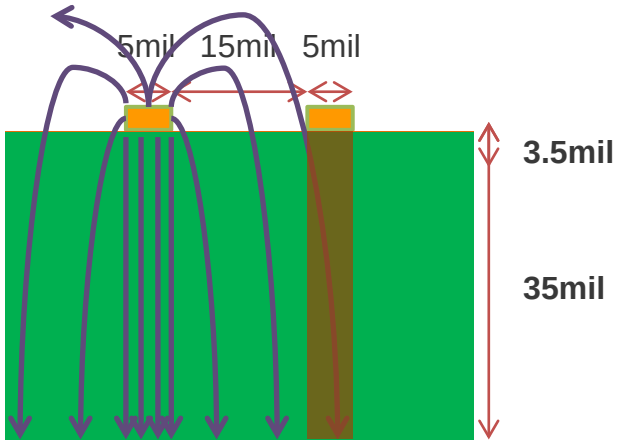
- The 3W rule may works well for the following structure:



No DRC violation ➡ No Xtalk issue

About SI – Z0 and Xtalk

- But if the stack-up looks like the following, will 3W rule still works well?



No DRC violation ➡ No Xtalk issue ?

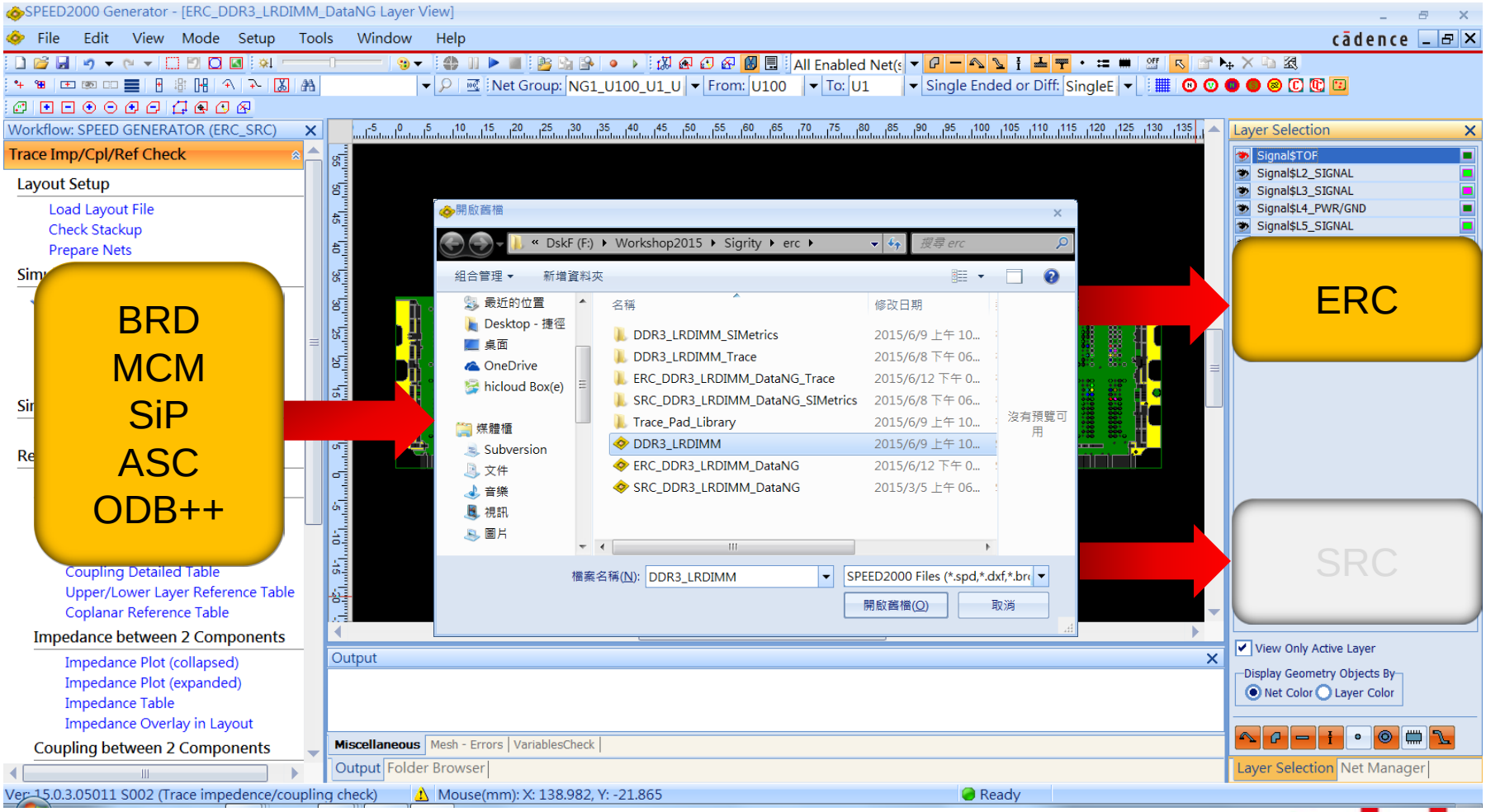
Now, you're not satisfied with simply spacing constraint or the related **DRC** violation warning. You feel you probably need **simulation** or other way to tell you :

How Much the Coupling is

The gap between DRC and SI performance

- The gap between layout designers and SI engineers is huge
  - Have different design expertise
  - Using different tools
  - Measured by different units

OrCAD Sigrity ERC/SRC Checking Flow



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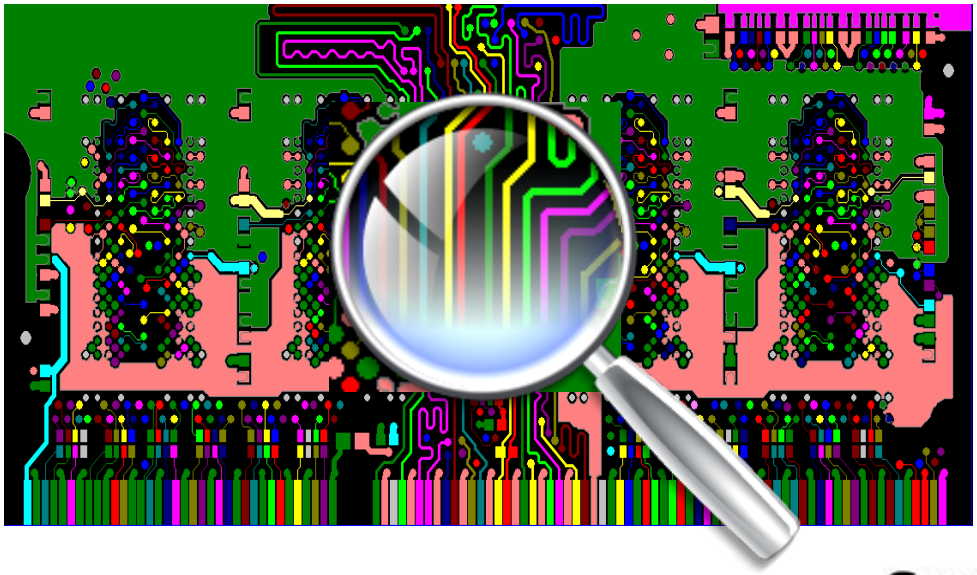
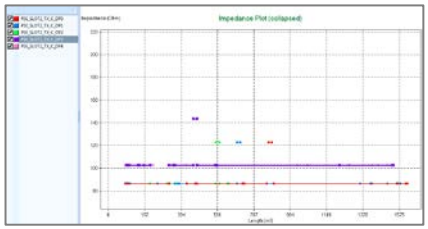
Why Electrical Rule Check

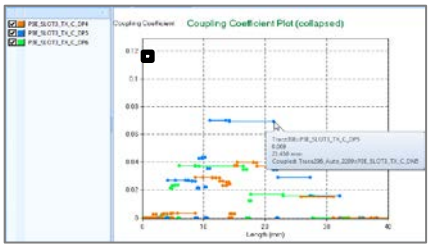
- ERCs are better than DRCs for ‘signal quality’ validation
  - Goes beyond **MINIMUM-ACCEPTANCE, GEOMETRY-BASED** constraint validation
- PCB designers identify and address first-order signal quality issues

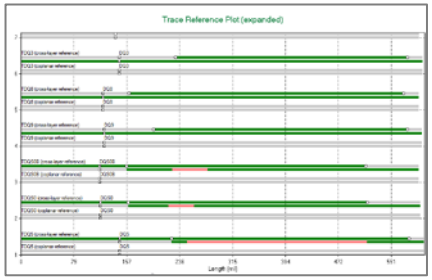


OrCAD Sigrity ERC

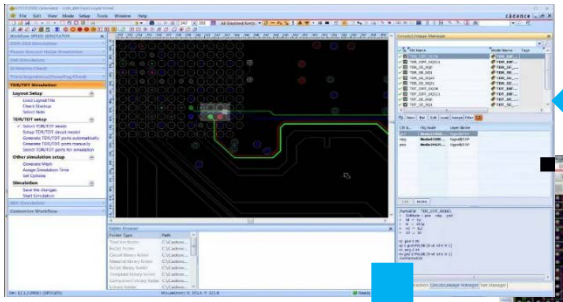
- A comprehensive set of electrical signal quality checks for PCB enabling the PCB designer to make needed changes before more extensive and exhaustive analysis is performed





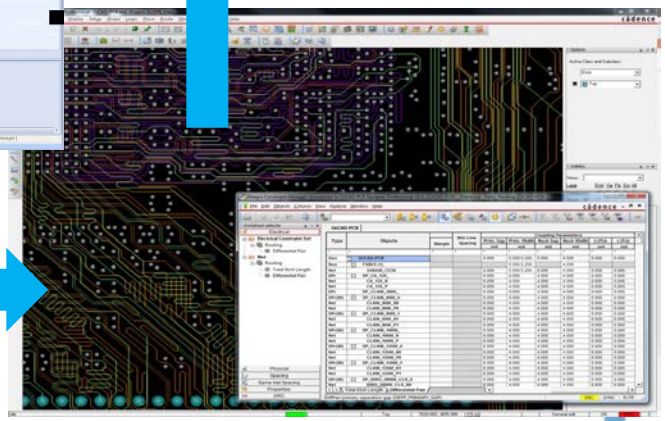


OrCAD Sigrity ERC



Electrical Rules Analysis

DRCs / ERCs



OrCAD PCB Board

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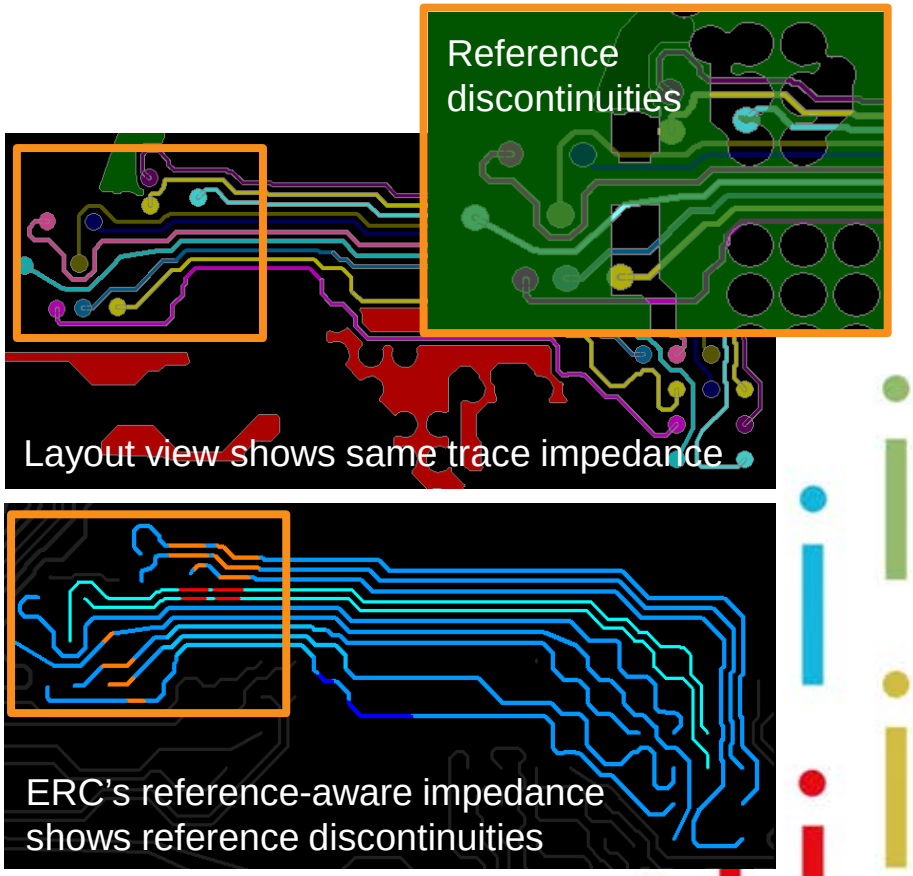
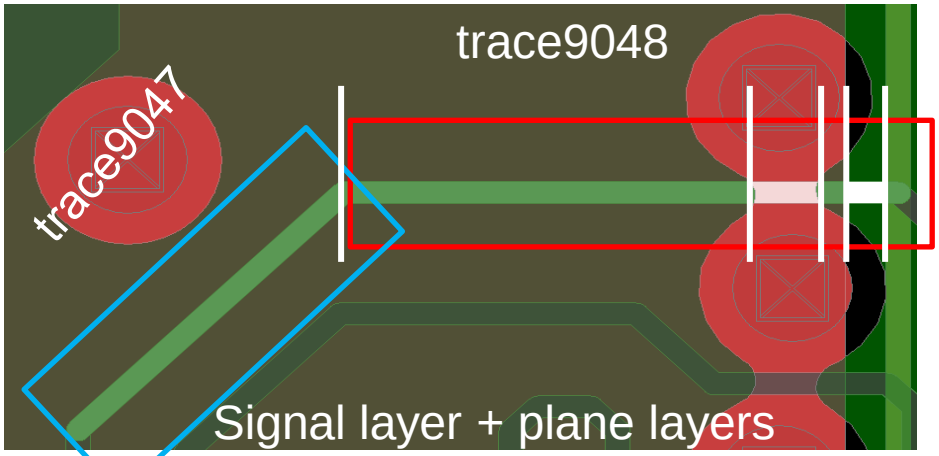
What is Sigrity ERC?

- Sigrity ERC is individual, segment-level view in geometry domain for PCB's SI performance with
  - Trace reference
  - Trace reference-aware impedance
  - Trace reference-aware coupling
  - Differential pair routing phase
  - # of vias and via locations, ….
  - Practical for board level check (setup, simulation, report)



What is Sigrity ERC?

- If you look close enough…
  Two trace segments example
  - **Trace9047:**
    one uniform impedance section
  - **Trace9048:**
    4 impedance sections



What is Sigrity ERC?

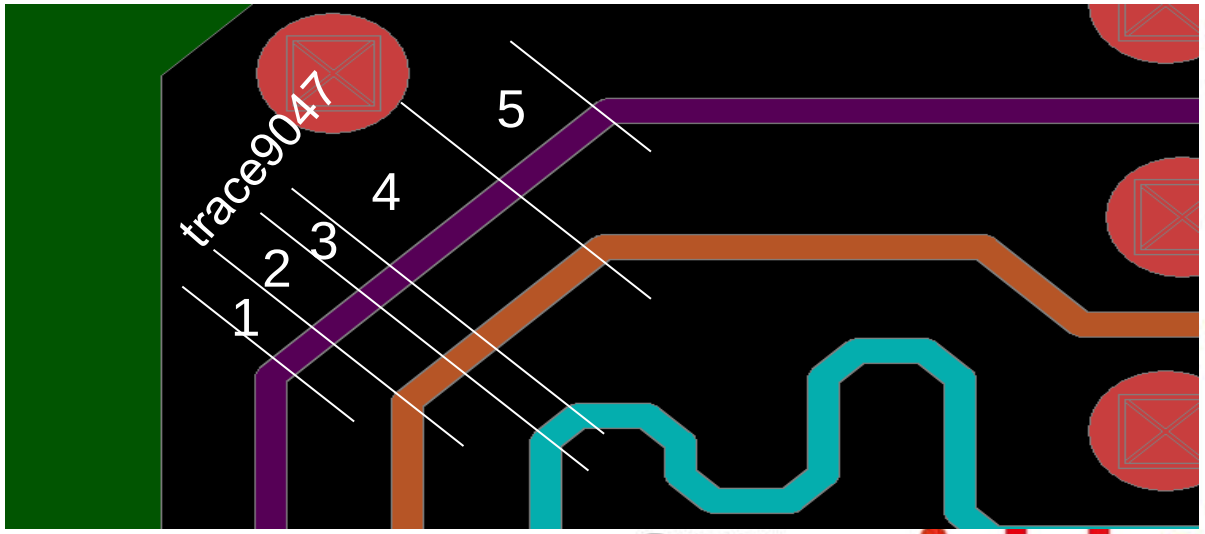
- ERC – Trace coupling

  Two trace segments example

  - Trace9047 is one uniform impedance section
  - Trace9047 broken into 5 sections based on trace coupling
    - two no coupling sections (1 & 5)
    - two 2-line coupling sections (2 & 4)
    - one 3-line coupling section (3)

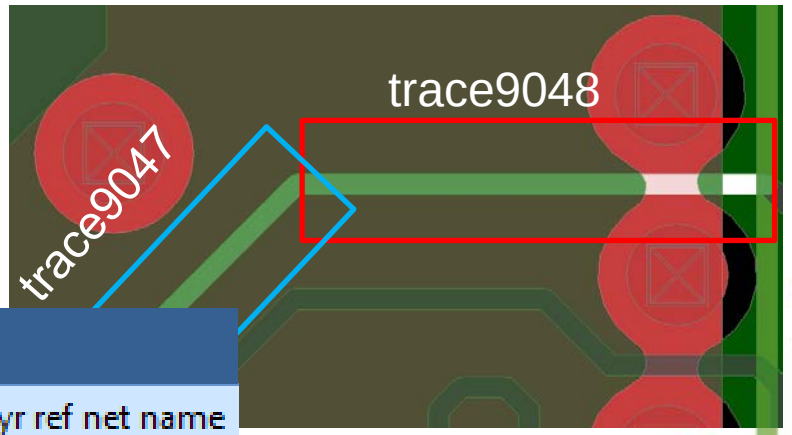
ERC results

Trace Name	Aggressor Trace Names	Coupling Coefficient (%)	Length (%)
Trace9047::DQ0	-	- ← 1	1.82
Trace9047::DQ0	Trace9024::DQ1	5.3 ← 2	1.46
Trace9047::DQ0	Trace9024_Auto_190::DQ1	5.3 ←3	1.16
	Trace8280::DQ4	0.6	
Trace9047::DQ0	Trace9024_Auto_191::DQ1	5.3 ← 4	4.10
Trace9047::DQ0	-	- ← 5	3.04



What is Sigrity ERC?

- ERC – Trace upper / lower layer reference
  Two trace segments example
  - Based on upper / lower layer references
    - Trace9047 → one section
    - Trace9048 → 5 sections

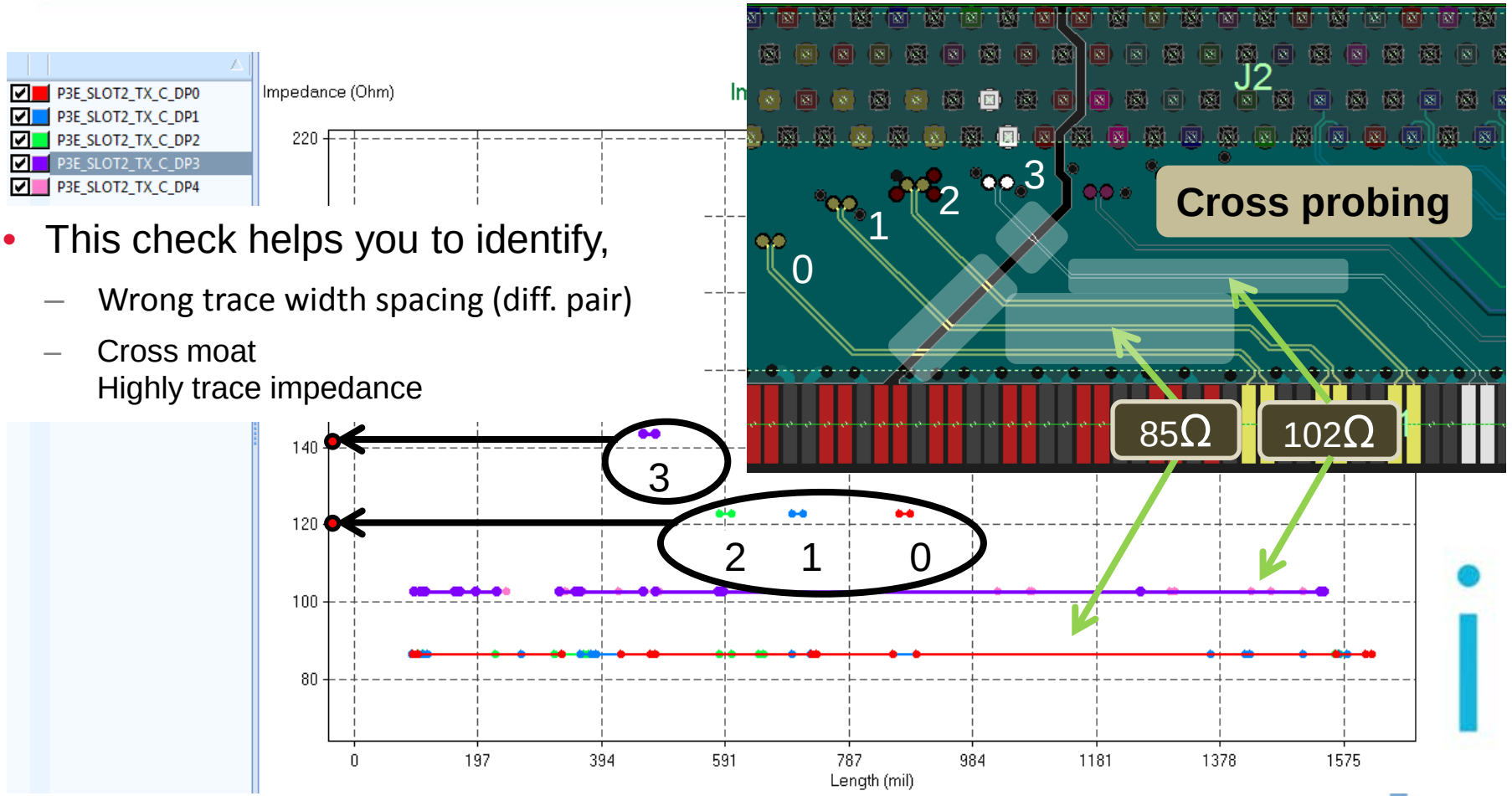


ERC results

Trace Name	Length (%)	Upper-lyr ref net name	Lower-lyr ref net name
Trace9047::DQ0	**11.58**	GND	**VDD**
Trace9048::DQ0	**12.74**	GND	**VDD**
Trace9048::DQ0	**1.78**	VDD	**VDD**
Trace9048::DQ0	**0.11**	-	**VDD**
Trace9048::DQ0	**0.89**	GND	**VDD**
Trace9048::DQ0	**1.66**	GND	**GND**

Note:
This is the reason why there are 5 impedance sections.

Trace Impedance Check

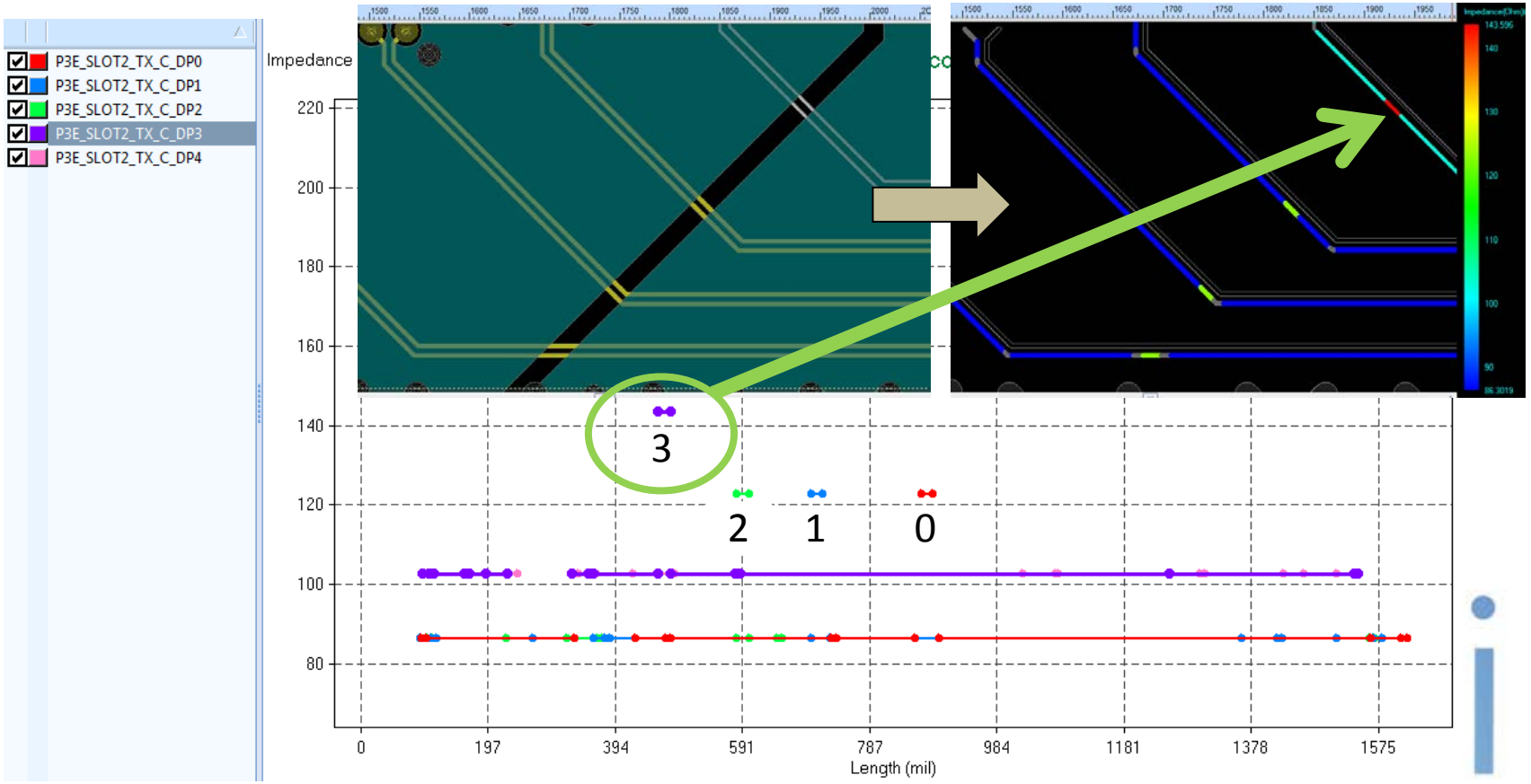


- This check helps you to identify,
  - Wrong trace width spacing (diff. pair)
  - Cross moat
    Highly trace impedance

- Visually or tabular result for trace impedance check that shows trace segments mismatch with target impedance.

Trace Impedance Check

Cross Probing



- Cross probing allows you to identify defects quickly.

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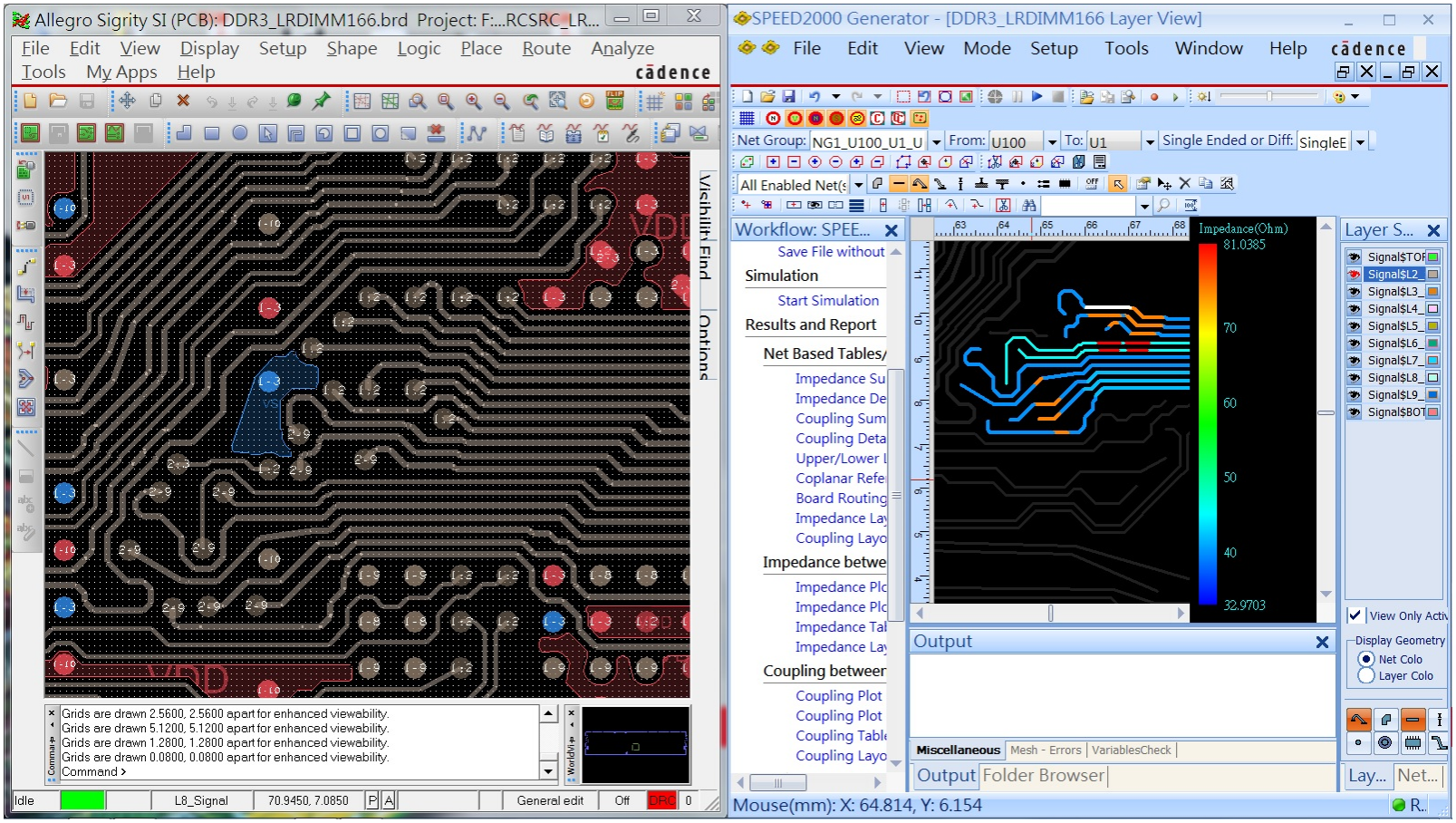
Trace Impedance Check

Cross Probing



- Auto-Zoom in board .

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Trace Impedance Check

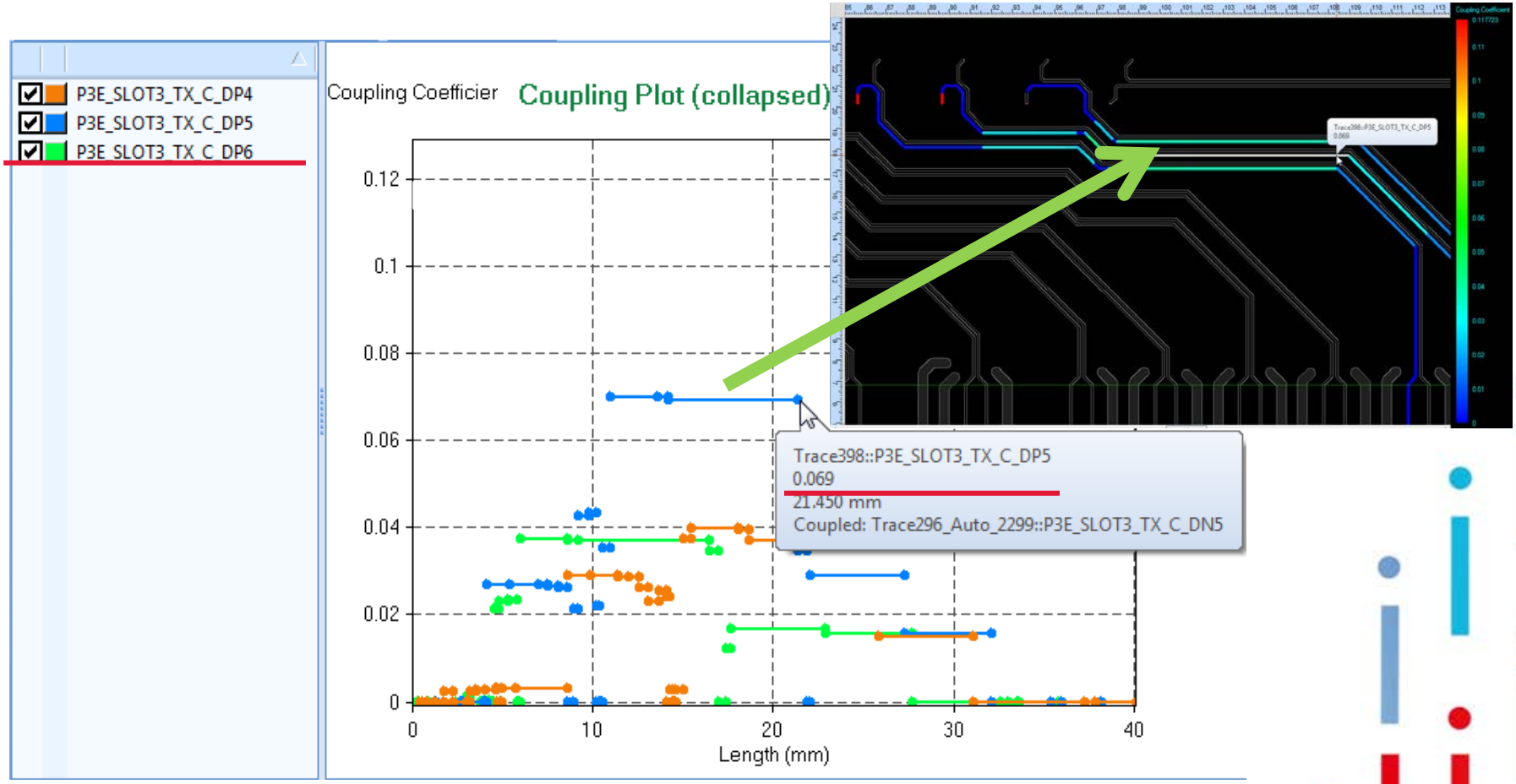
Tabular Results

Net count	Net name	No. of segments without	No. of trace reference discontinuities	No. of vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)	Dominant Impedance (Ohm)	Dominant Imp Length (%)	Trace total length (mil)	Trace delay(ns)
1	**P3E_SLOT2_TX_C_DN0**	1	**3**	2	**144.946**	56.449	**56.449**	92.921	**1633.158**	0.233
2	**P3E_SLOT2_TX_C_DN1**	1	**3**	2	**144.946**	56.449	**56.449**	93.168	**1583.722**	0.225
3	**P3E_SLOT2_TX_C_DN2**	1	**3**	2	**144.946**	56.449	**56.449**	93.186	**1575.168**	0.224
4	**P3E_SLOT2_TX_C_DN3**	1	**3**	2	**153.005**	63.836	**63.836**	93.074	**1549.678**	0.220
5	**P3E_SLOT2_TX_C_DN4**	1	**1**	2	**63.836**	63.836	**63.836**	94.228	**1513.121**	0.214
6	**P3E_SLOT2_TX_C_DP0**	1	**3**	2	**144.946**	56.449	**56.449**	92.923	**1633.643**	0.233
7	**P3E_SLOT2_TX_C_DP1**	1	**3**	2	**144.946**	56.449	**56.449**	93.221	**1583.404**	0.225
8	**P3E_SLOT2_TX_C_DP2**	1	**3**	2	**144.946**	56.449	**56.449**	93.184	**1574.865**	0.224
9	**P3E_SLOT2_TX_C_DP3**	1	**3**	2	**153.005**	63.836	**63.836**	93.059	**1546.528**	0.219
10	**P3E_SLOT2_TX_C_DP4**	1	**1**	2	**63.836**	63.836	**63.836**	94.221	**1511.225**	0.214
11	**P3E_SLOT3_TX_C_DN0**	1	**1**	1	**56.449**	56.449	**56.449**	94.142	**1490.958**	0.211
										0.208
										0.217
										0.209
										0.225
										0.214
										0.203
										0.212
										0.212
										0.209
										0.217
										0.210
										0.225
										0.214
										0.203
										0.212

- Cross moat?
- Any trace segment mismatch? Cross moat?
- Too much breakout neck length?
- Too much MS/SL routing difference in a group?
- The same trace length means the same trace delay?
- Routing on MS/SL has different trace delay.

Trace Coupling Check

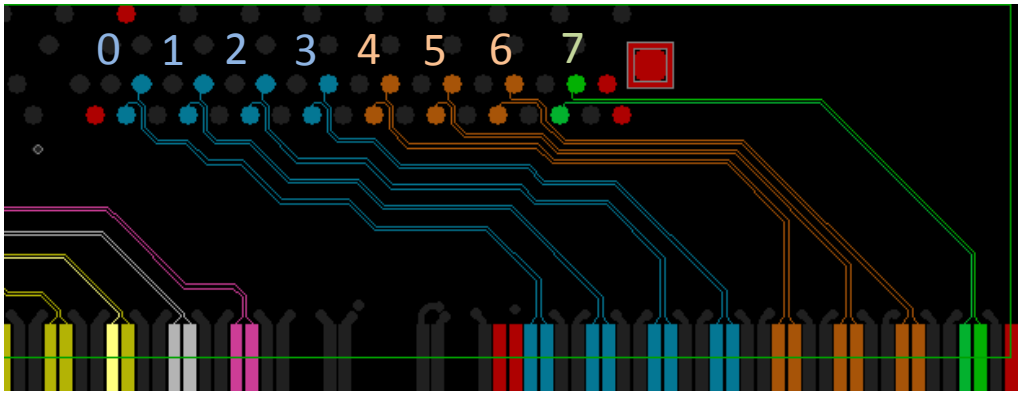
Cross probing helps to resolve issue intuitively



Trace Coupling Check

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
1	P3E_SLOT2_TX_C_DP0-P3E_SLOT2_TX_C_DN0	P3E_SLOT2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
2	P3E_SLOT2_TX_C_DP1-P3E_SLOT2_TX_C_DN1	P3E_SLOT2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
3	P3E_SLOT2_TX_C_DP2-P3E_SLOT2_TX_C_DN2	P3E_SLOT2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
4	P3E_SLOT2_TX_C_DP3-P3E_SLOT2_TX_C_DN3	P3E_SLOT2_TX_C_DN2	0.125%	36.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.[illegible]	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

18X



Through this test, you will see,

- Tight coupling pairs
- Max coupling aggressor
- Dangerous vs. safe coupling
  → **18X** (= 2.81% / 0.156%)

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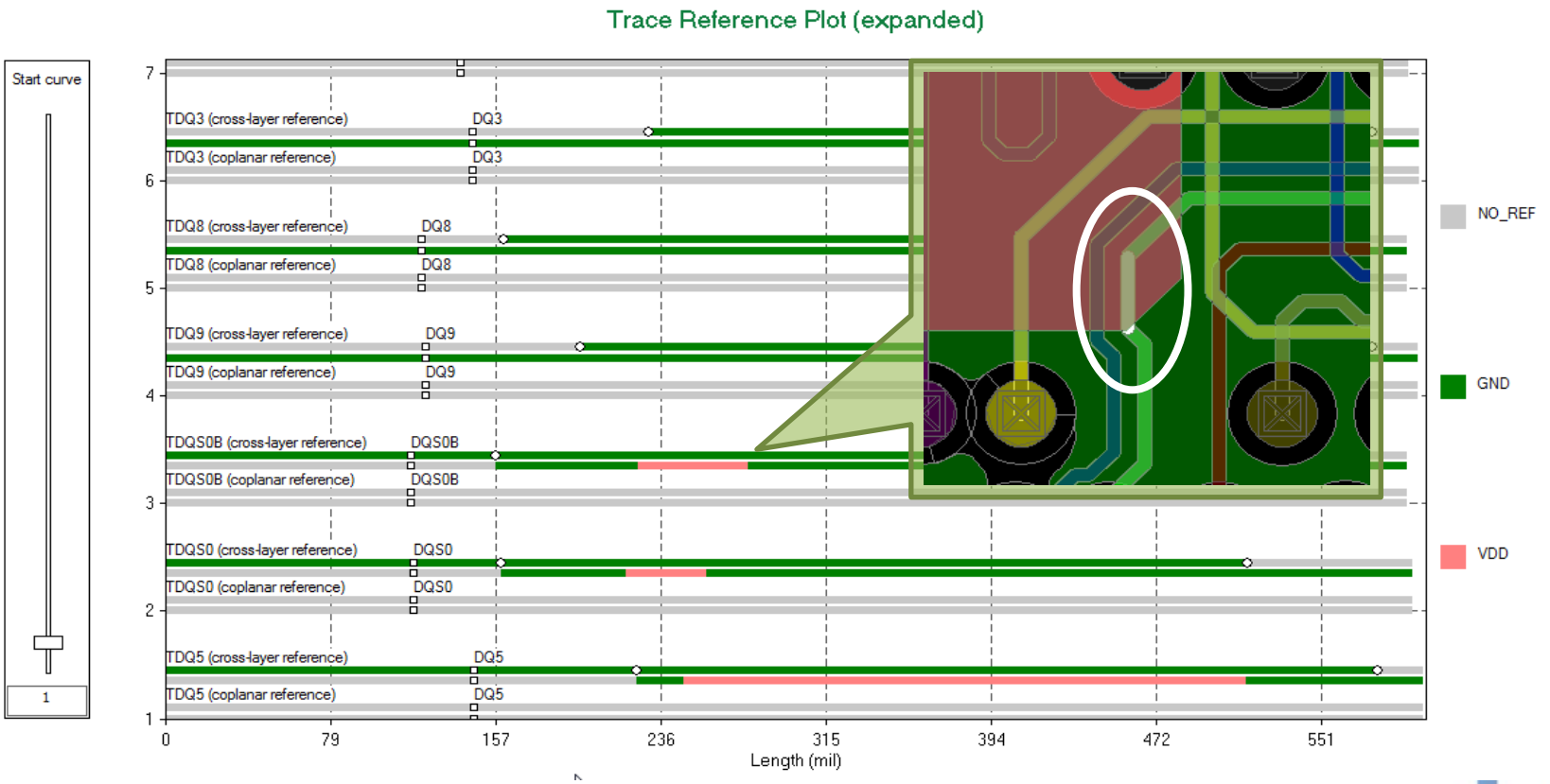
Trace Reference Check (Including co-planar)



- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

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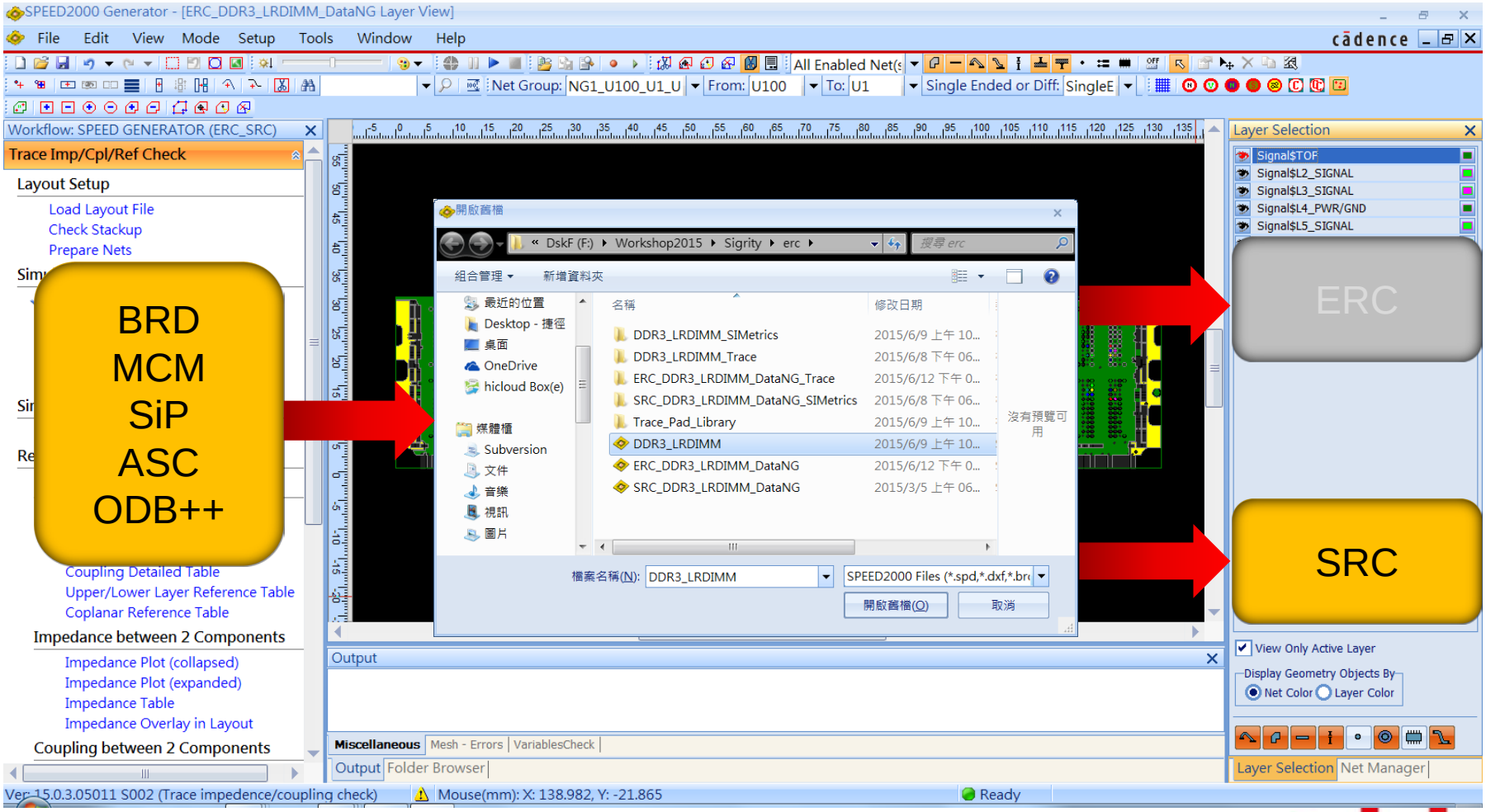
OrCAD Sigrity ERC/SRC Checking Flow



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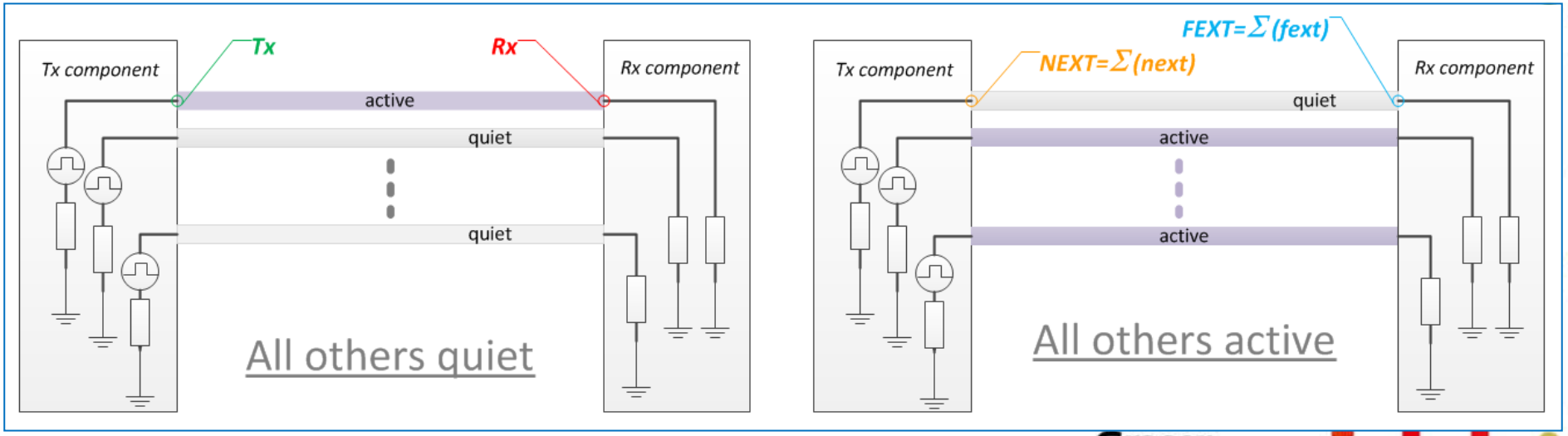
What is Sigrity SRC?

- Sigrity SRC is Macro, combined, net-level view in time-domain of impact due to ERC violations measured in mv & ps (no device model needed)
  - Setup considering termination impedance, data rate (pulse width, rise/fall time), and amplitude
  - Results with Tx/Rx/NEXT/FEXT waveforms, SI performance metrics
  - Organized to easy SI performance interpretation along with ERC
- Practical for board level check (setup, simulation, report)

<2min ~ 20min auto



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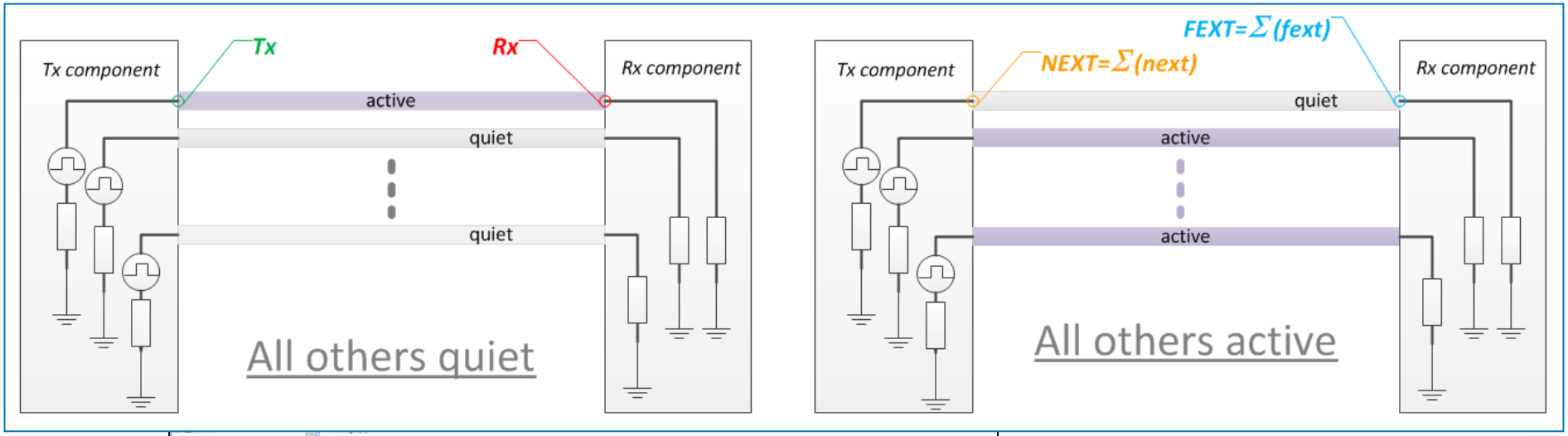
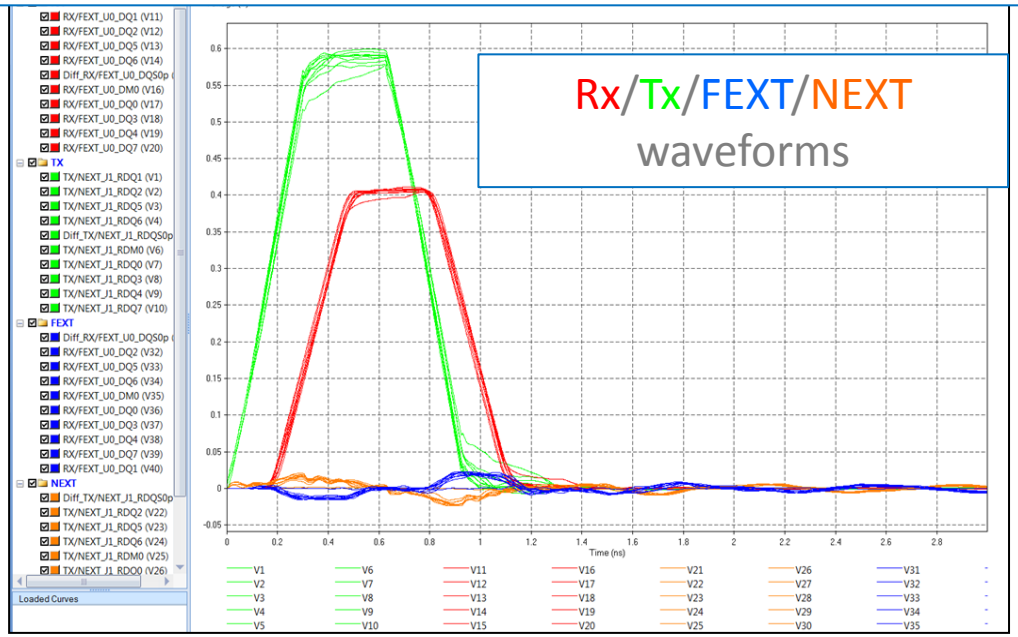
Time-domain waveforms *SRC – SI Metrics Check*





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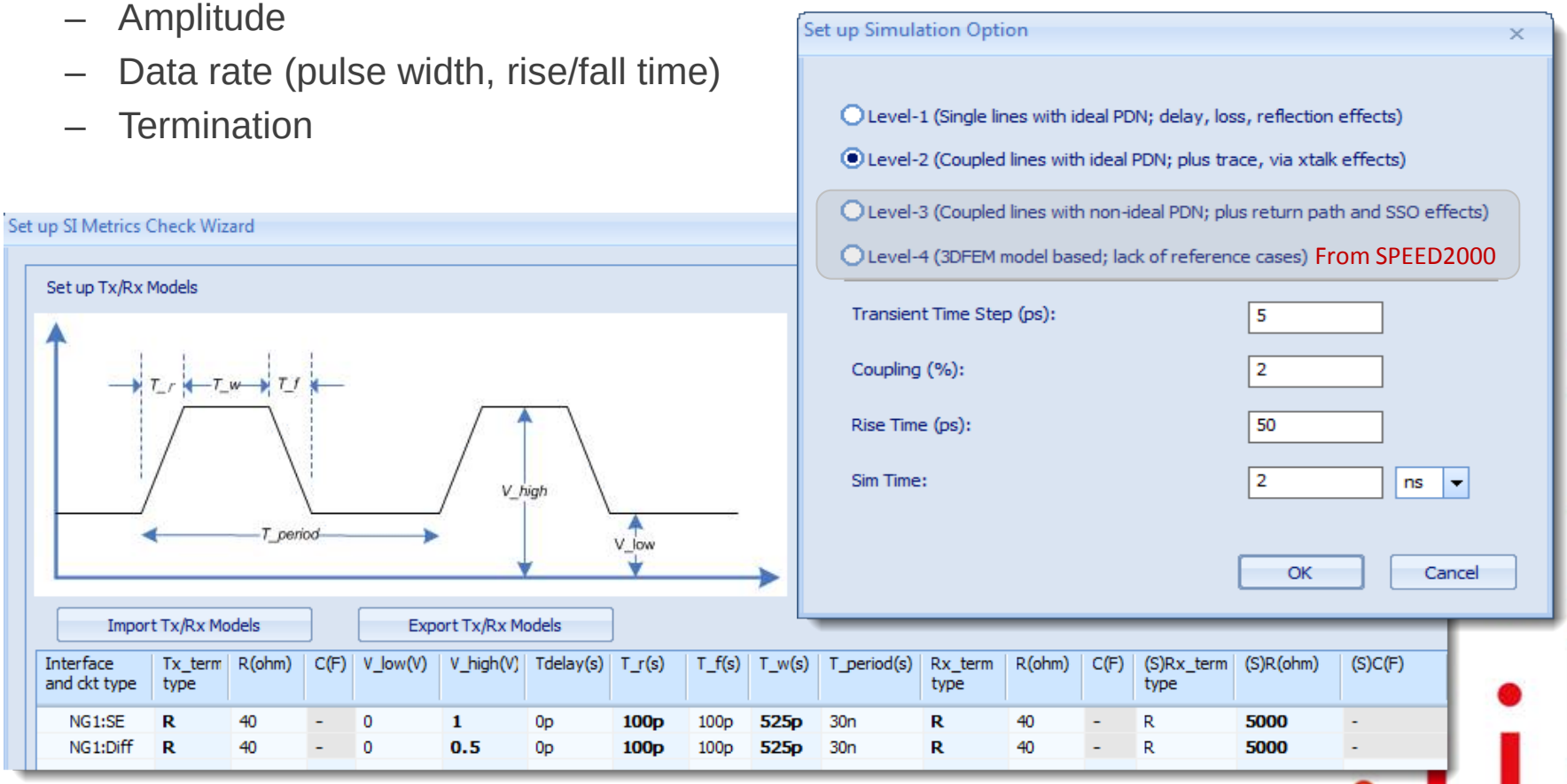
SRC Setup

- Device models are not needed
- Voltage pulse as stimulus, users can specify
  - Amplitude
  - Data rate (pulse width, rise/fall time)
  - Termination



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Net-level Performance Ranking *SRC – SI metrics check*

Net name	INT_Sig (V*ps)	INT_ISI (V*ps)	INT_XTK (V*ps)	SN_difference (V*ps)	SN_ratio
DQ19	287.97	22.96	3.7	261.31	10.8029
DQ17	288.15	22.79	3.12	262.24	11.1223
DM2	286.52	24.21	3.04	259.28	10.5156
DQS2_P	206.59	104.05	0	102.54	1.98541
DQ20	286.71	23.94	3.14	259.63	10.5871
DQ21	288.2	22.68	5.43	260.09	10.2522
DQ16	286.51	24.21	0	262.3	11.834
DQ22	286.46	24.06	1.6	260.8	11.1639
DQ18	286.47	24.12	0	262.34	11.8752
DQ23	286.65	24.13	7.81	254.71	8.97519

← Ranking by SI Metrics

Net name	NEXT Vmax (mv)	NEXT Vmin (mv)	NEXT pk-2-pk (mv)	FEXT Vmax (mv)	FEXT Vmin (mv)	FEXT pk-2-pk (mv)
DM1	0	0	0	0	0	0
DQ10	0	0	0	0	0	0
DQ11	0	0	0	0	0	0
DQ9	19	-18	37	14	-15	29
DQ12	17	-15	32	16	-16	32
DQ8	2	-2	5	3	-3	6
DQ14	0	0	0	0	0	0
DQS1_P	0	0	0	0	0	0
DQ15	17	-16	33	13	-13	27
DQ13	19	-18	37	14	-14	29

← Ranking by xtalk levels

SRC Net-level View → ERC's Segment-level View

Sigrity SRC

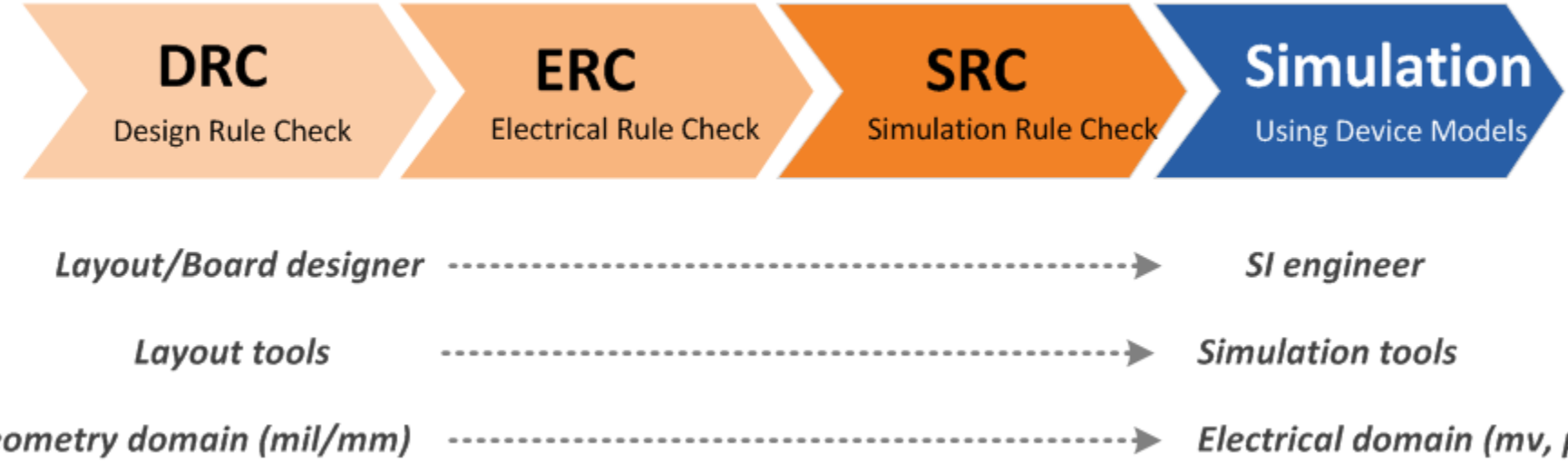
- Layout SI macro view at net level
- All inclusive end results
- Shows what happened and its effect on performance

Sigrity ERC

- Layout SI micro level view at segment level
- Individual segmented results
- Shows why low performance happened and how to fix it

Summary

- Sigrity ERC/SRC fills the gap between layout designers and SI engineers
  - Expanded expertise
  - Using same tools
  - Measured by same units



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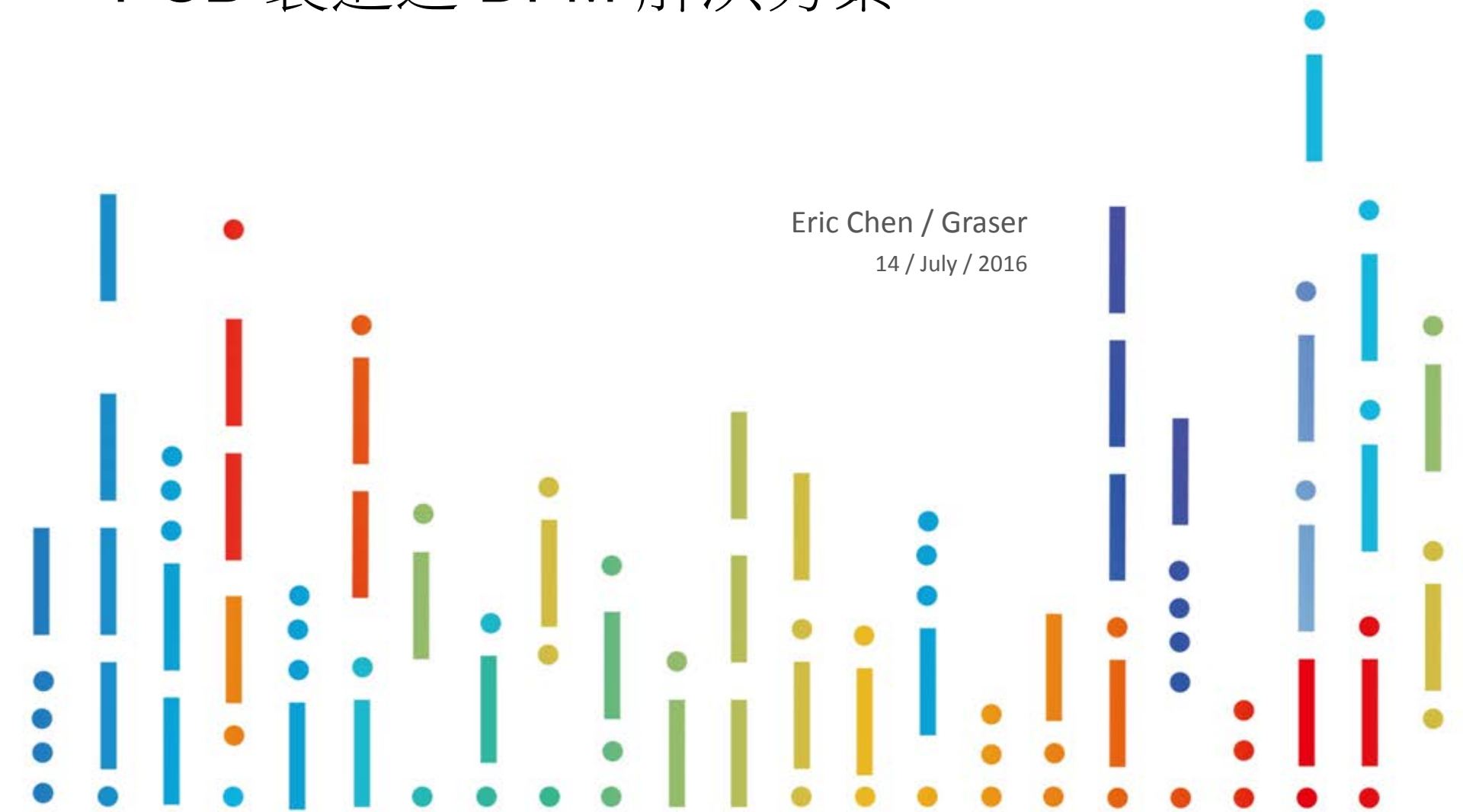
PCB 製造之 DFM 解決方案

Eric Chen / Graser

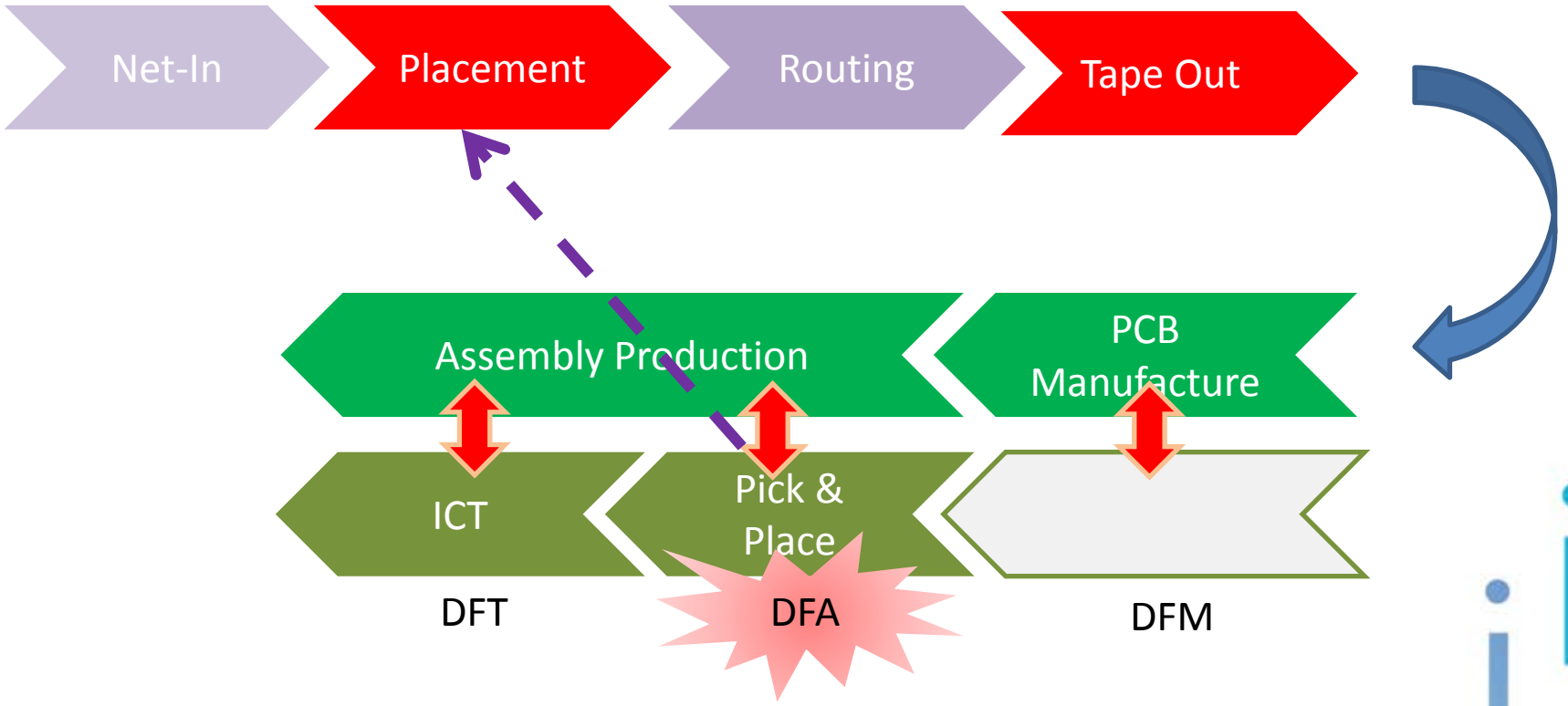
14 / July / 2016



Topic

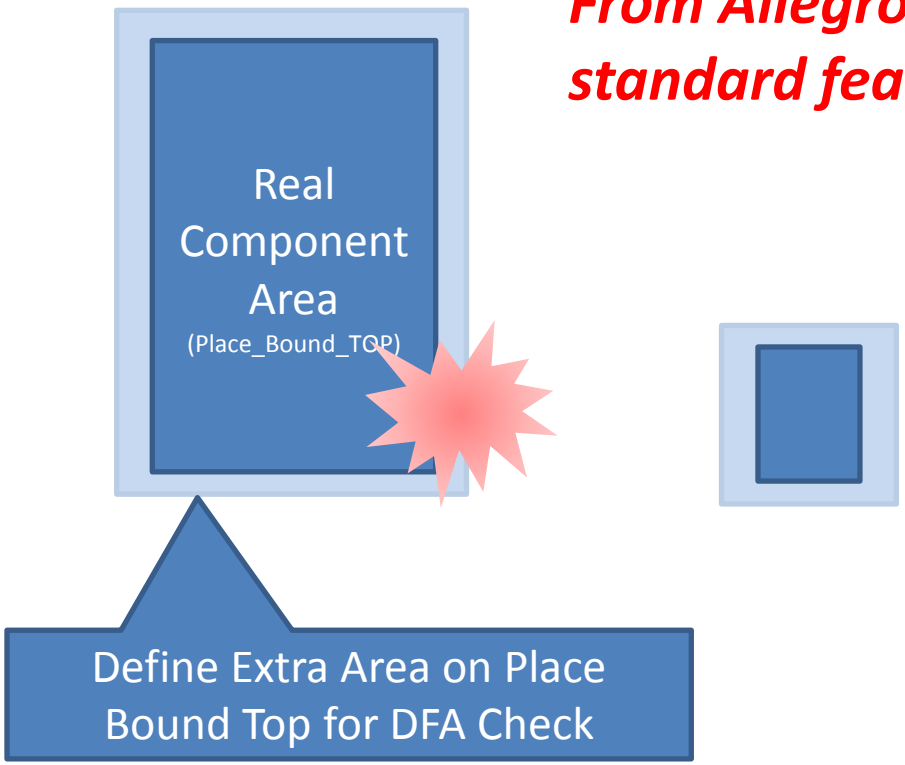
1. Review Design Flow
2. Review production issue from PCB manufacture & Assembly line.
3. What we have in Allegro PCB Designer?

What we need DFx Checker



Design for Assembly Check

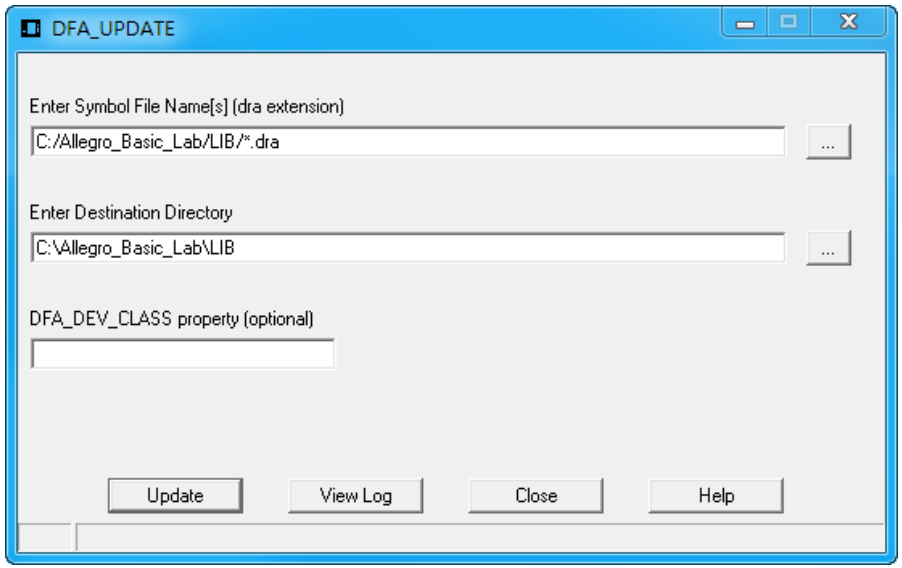
Allegro DFA Constraint

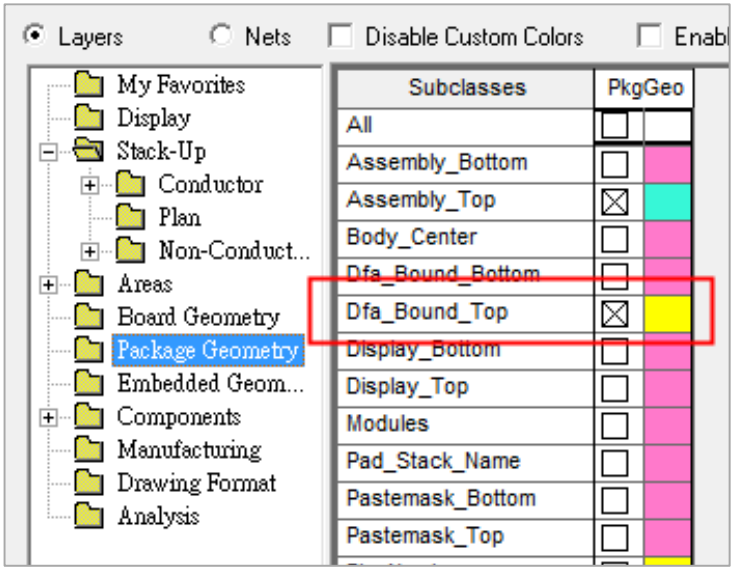


From Allegro® V16.5 , the DFA check is standard feature in Allegro PCB Designer.

Allegro DFA Constraint

- Define DFA_Bound_Top/Bottom
- Define Correct area
- Classify DFA Class or add DFA_Bound_Top/Bottom, when you needed.





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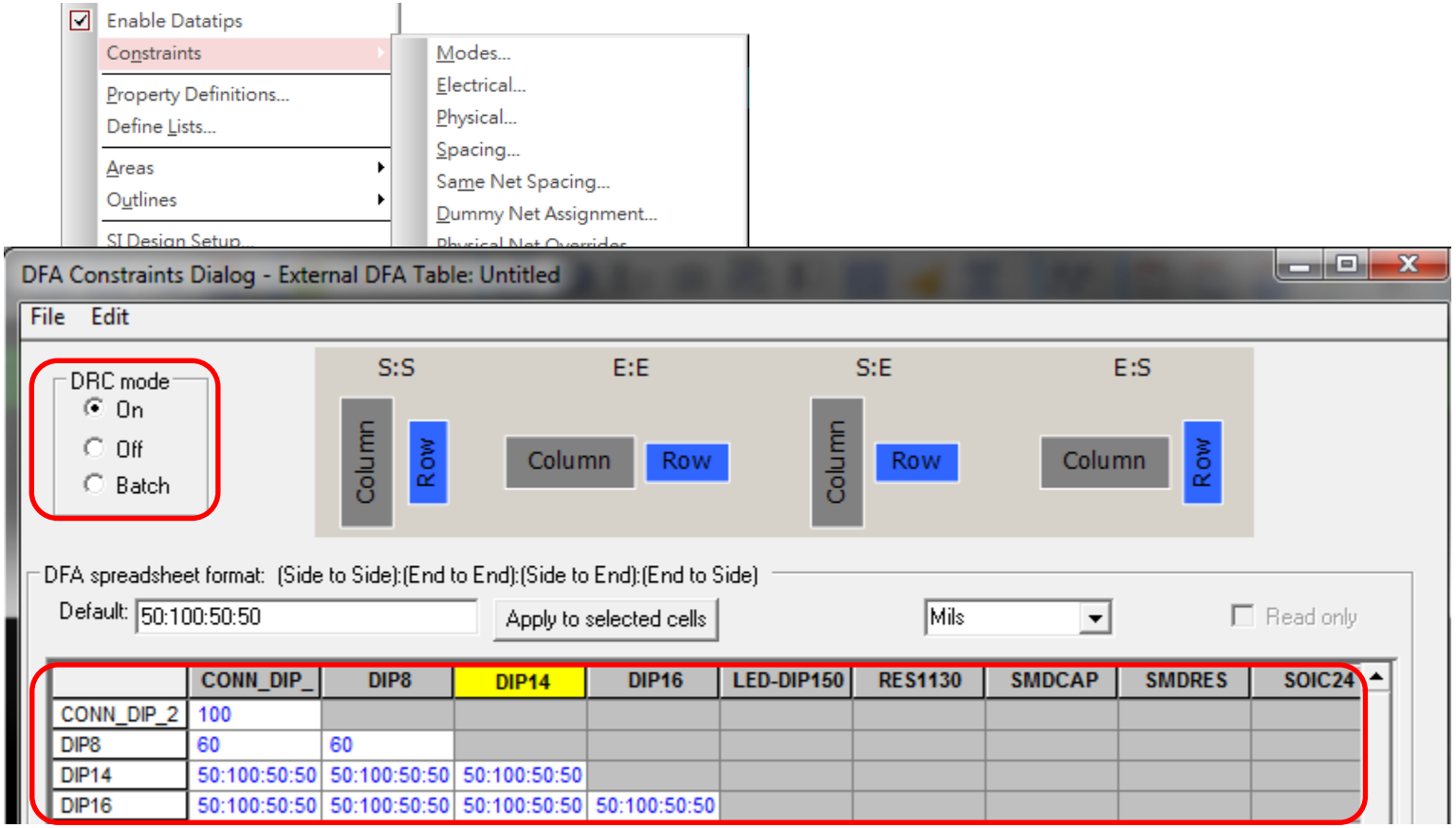
Define DFA Spreadsheet Editor & Rule

- Edit / Constraint / DFA Constraint Spreadsheet



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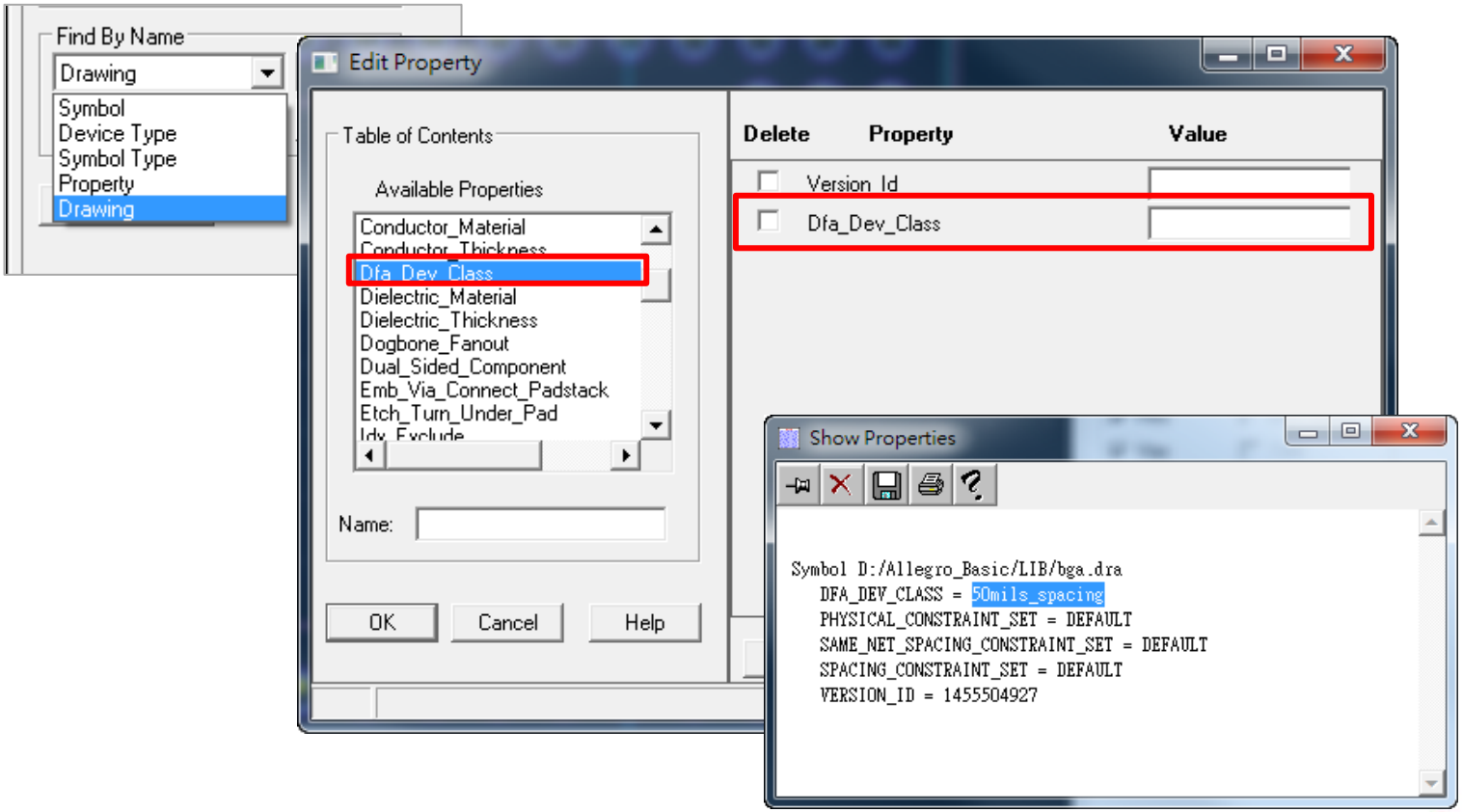
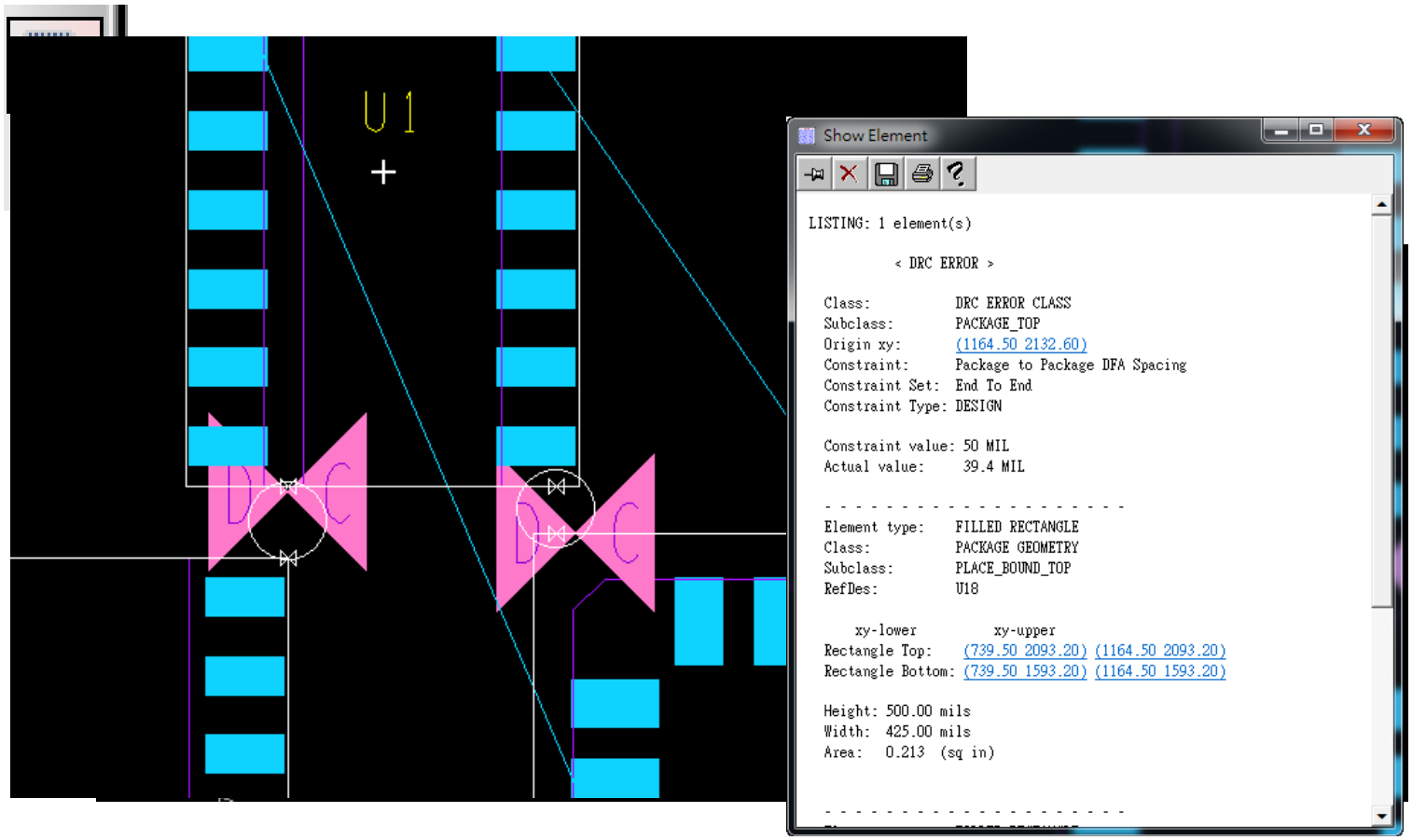
Define DFA Device Class

- Using DFA Update to classify DFA Class
- Edit Drawing property



DFA DRC Marker

- DFA Clearance Control



The DFM Solution for PCB Manufacture

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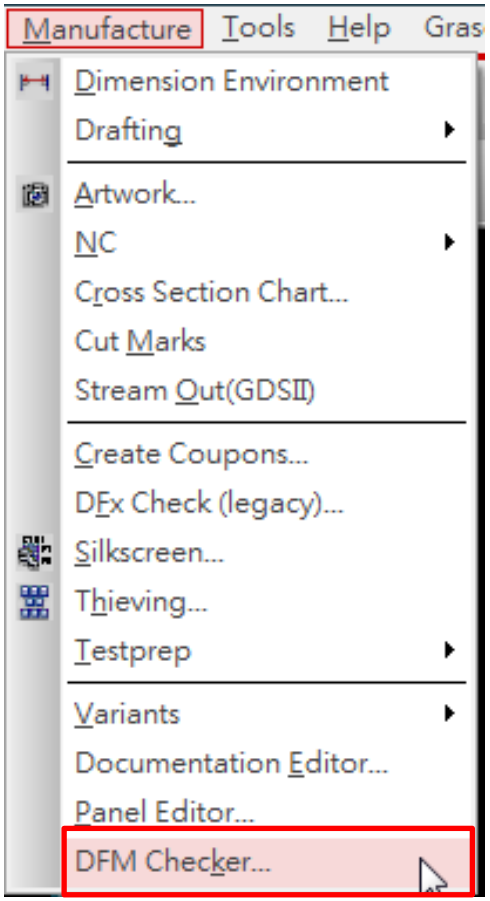
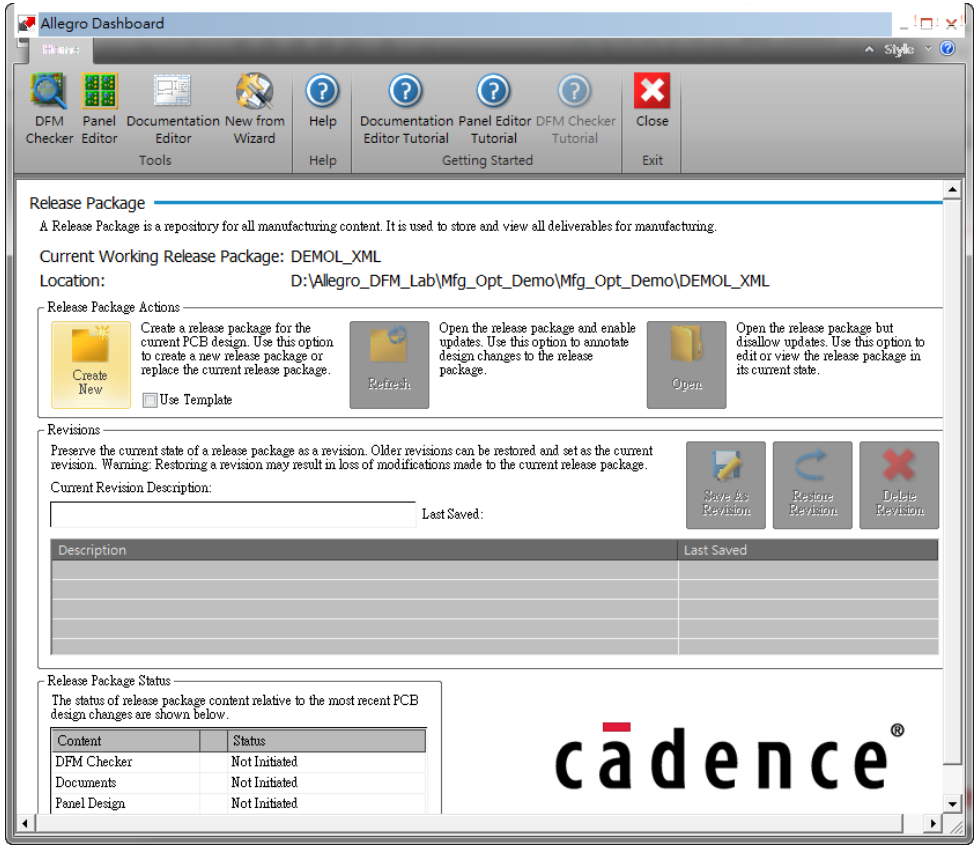
Why do we need to do DFM check?

1. Make sure manufacture date is correct and good for PCB manufacture.
2. Vision same as PCB Factory.
3. Identify problems early , reduce re-work probability.

Allegro PCB Manufacturing Option

- 16.6 S045 or later





DFM Check Rules

- Features

	Check Category	Data category
Etch	Logic	Netlist compare
	Graphic Check	Signal layer
		Power plane
Non-Etch	Graphic Check	Solder mask
		Silkscreen
		Paste mask
		NC data
Analysis	Statistics	Analysis Report

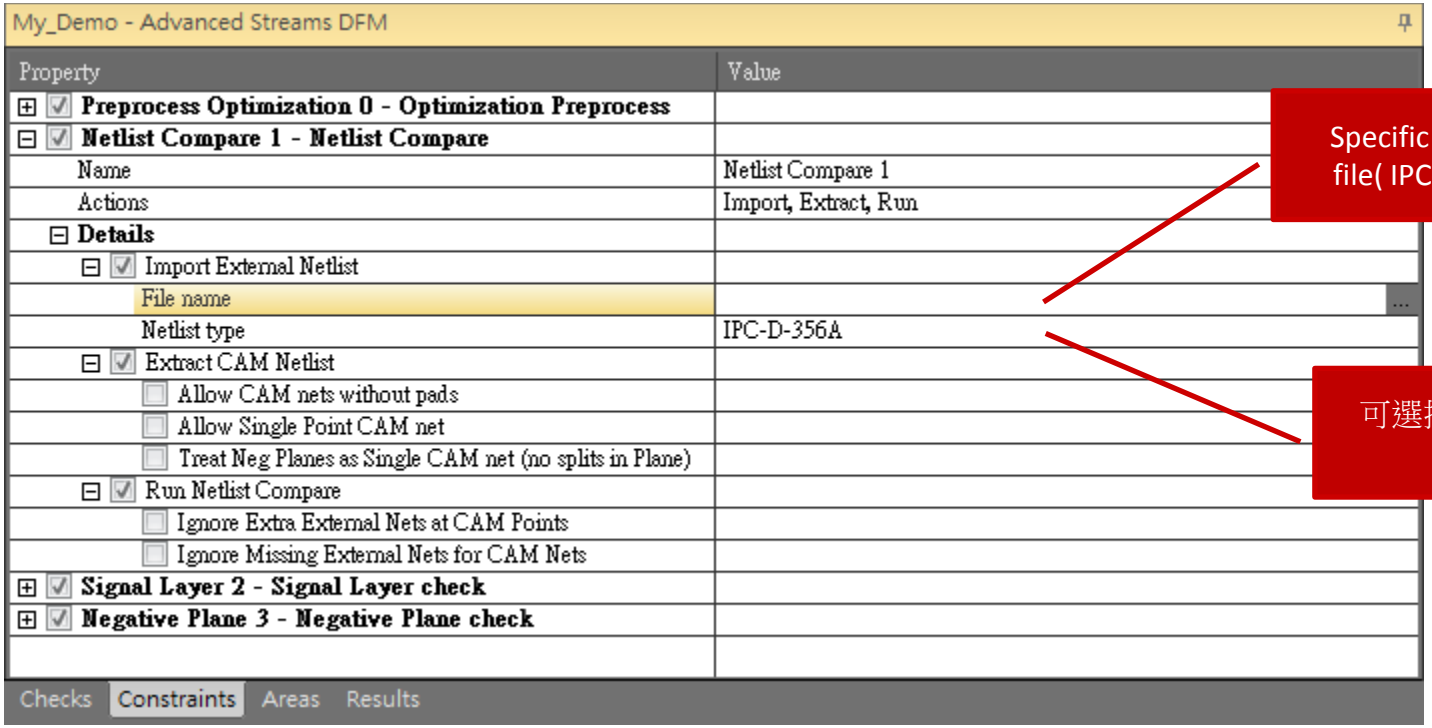
DFM Check Rules

- Netlist Compare
  - Import External Netlist, Extract CAM Netlist, Run Netlist Compare
- Signal Layer
  - Track to Track, Track to Pad, Pad to Pad, Pad to Drill, Minimum Track, Minimum Pad, Unplated Drills to Copper, Plated Drills to Copper, Copper to One-Up-Border, Redundant Pads, Plated Drills without Pads, Pads without Drills, Antennas, Minimum Gap, Minimum Width, Acid Traps, Copper Slivers, Pin Holes
- Positive Plane
  - Plated Drills to Copper, Unplated Drills to Copper, Pads to Drills, Acid Traps, Copper Slivers, Pin Holes, Minimum Gap, Minimum Width
- Negative Plane
  - Plated Drills to Copper, Unplated Drills to Copper, Pads to Drills, Copper to One-Up-Border, Isolated Thermal, Starved Thermal, Thermal Conflict, Tie Width

DFM Check Rules

- Soldermask
  - Pad to Mask, Drill to Mask, Mask Slivers, Soldermask Bridge, Pin Holes, Soldermask to Track, Missing Soldermask
- Silkscreen
  - Silkscreen to Soldermask, Minimum Soldermask Width
- NC Data Layer
  - Overlapping Hits, Coincidental Hits, Redundant Hits, Drill to Drill, Imploded Arcs, Imploded Path, Mill Tab Errors
- Pastemask
  - Pastemask on Through Holes, Missing Pastemask on SMD Pads, Missing Soldermask for Pastemask Pads, Pastemask to Copper clearance
- Design Analyzer
  - Design Analysis reporting, including User Parameter specifications, Calculated design analysis and customized output formatting.

Netlist Compare



Specific external Netlist file(IPC-D-356 format)

可選擇IPC-D-356或 IPC-D-356A

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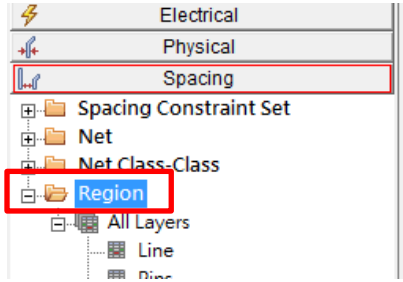
Constraint Region Check



Objects			Referenced Spacing CSet	Line To									
Type	S	Name		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bond Finger	Hole
				mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*		*	*	*	*	*	*	*	*	*	*	*	*
Dsn		demoL	DEFAULT	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	8.0000
Rgn		POWER-REGION	POWER NETS	8.0000	8.0000	6.0000	8.0000	8.0000	8.0000	10.0000	10.0000	5.0000	10.0000

POWER-REGION_Outer_Electrical - Signal Layer check	
Name	POWER-REGION_Outer_Electrical
Layers	[Outer Electrical]
Drill Layers	[All NC]
Checks	TT, TC, CC, TP, CP, CPCP, SMSM, VV, LVLV, THTH, SMV, SMLV, SMTH, VTH, LVTH, DTHC, DT...
Shape/Size Filter	
NC Tool Filter	
Area	POWER-REGION_All_Electrical
Auto Fix Errors	
Details	
Board Outline spacing	
Copper spacing (Different Nets)	
TT - Track to Track	8.000000
TC - Track to Copper	10.000000
CC - Copper to Copper	12.000000
TP - Track to Pad	10.000000
CP - Copper to Pad	10.000000
Pad spacing	
Drill spacing	
Annular Ring	

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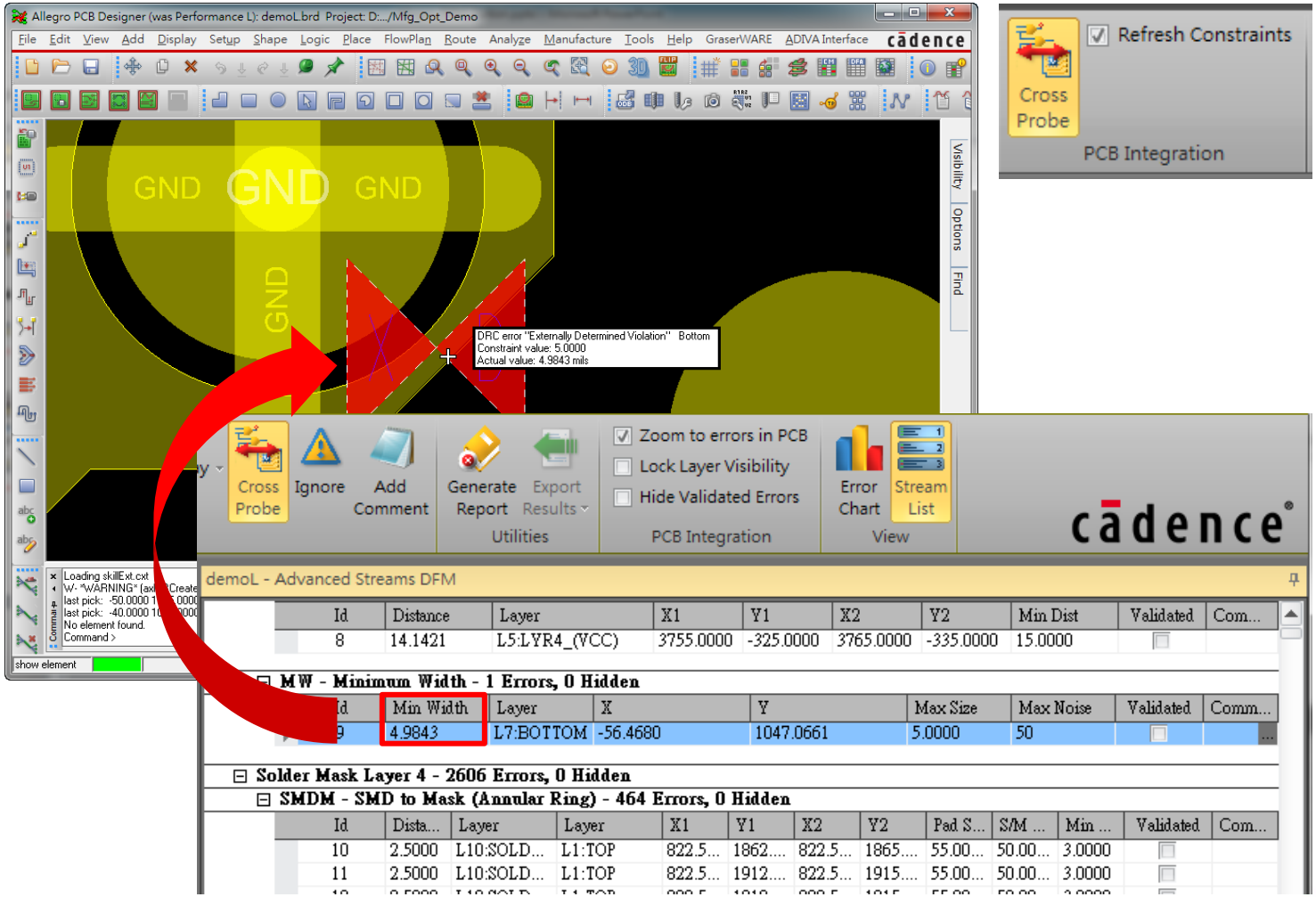
Results & Cross Probing



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Summary

- Embedded Systems Design , Easy to Use.
- Cross Probing between Checker and Allegro® / OrCAD® PCB Designer

Confirm the correctness of the information before sending to your partner.
Ensure smooth production.

New Exchange Format IPC-2581

- Generic Requirements for Printed Board
- Assembly Products Manufacturing Description Data and Transfer Methodology

Name	Full	Design			Fabrication			Assembly			Test		
		1	2	3	1	2	3	1	2	3	1	2	3
Hierarchical layer/stack instance files													
Hierarchical conductor routing files													
BOM (Components and Materials)													
AVL (Components and Materials)													
Component Packages													
Land Patterns													
Device Descriptions													
Component Descriptions													
Soldermask ; Solder Paste Legend Layers													
Drilling and Routing Layers													
Documentation Layers													
Net List													
Outer Copper Layers													
Inner Layers													
Miscellaneous Image Layers													
DFX Analysis													

New Exchange Format IPC-2581

- Using IPC-2581 data format
  - All artwork film record must be defined
  - IPC-2581 Layer mapping must be defined

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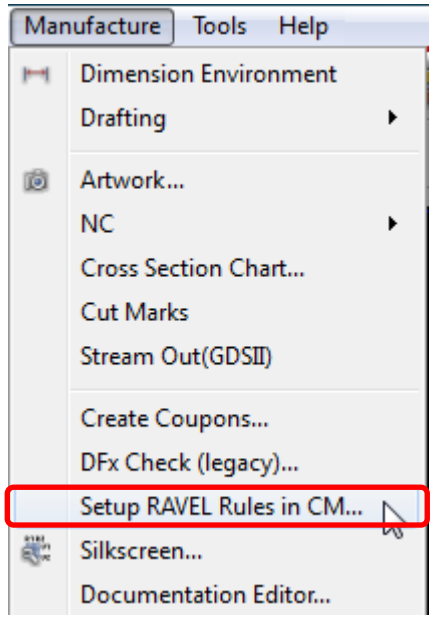
Ravel Rule Checker

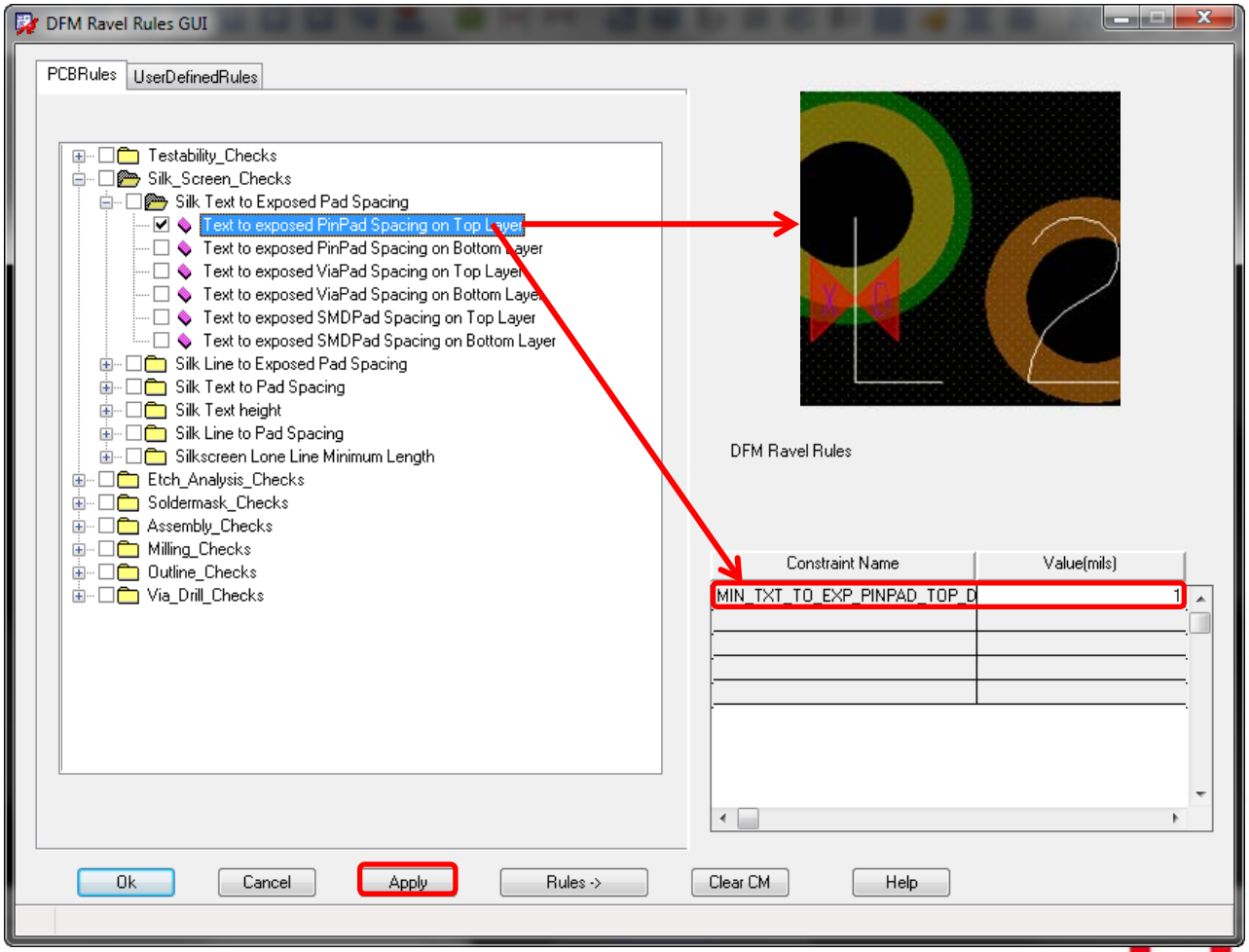
Does Traditional Design Rule Checker Enough?

Now You Can Self-development it .

A New DFM Rule Checker - Ravel Rule Check

Ravel Rule Checker





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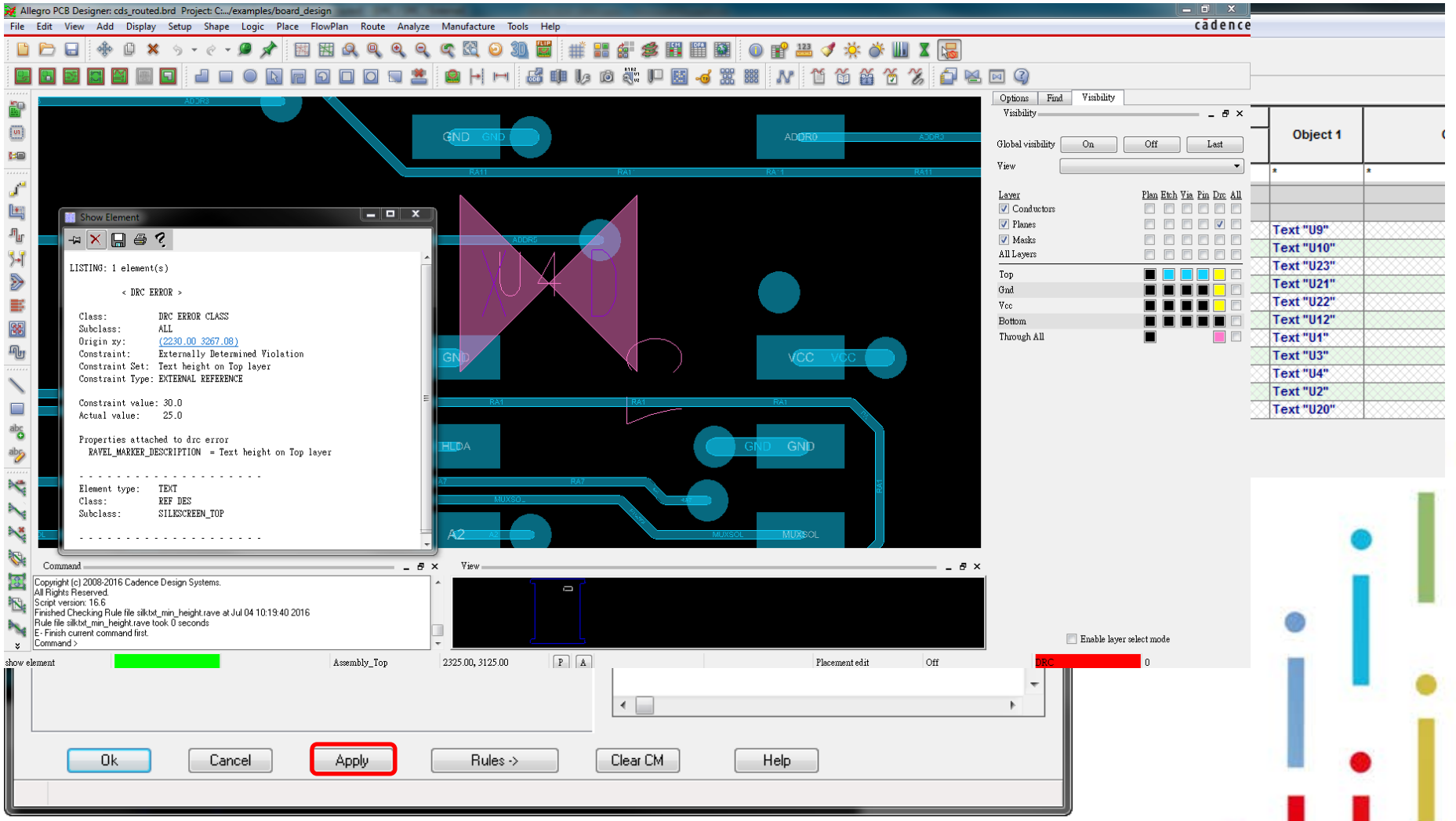
Ravel Rule Checker



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RAVEL DRC Overview

Advantages

- Rapid development of custom DRC upon demand
- Reduced DRC implementation effort
  - RAVEL DRC language is specialized for expressing design rules in PCB and SiP
  - Does not require knowledge of SKILL or C/C++ programming languages
  - Does not require knowledge of Allegro® PCB/SiP database

Case 1: 2 rules	C/C++	RAVEL
Lines of code	1200	80
Effort	10 days	2 hours

Case 2: 4 rules	SKILL	RAVEL
Lines of code	1540	470
Effort	15 days	3 days

- Reduced DRC maintenance effort
  - RAVEL rules are independent of database
  - RAVEL rules are independent of SPB software release
  - All dependencies are built into RAVEL DRC engine

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Thank You!