Package RLC Extraction and Assessment Solution

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Agenda

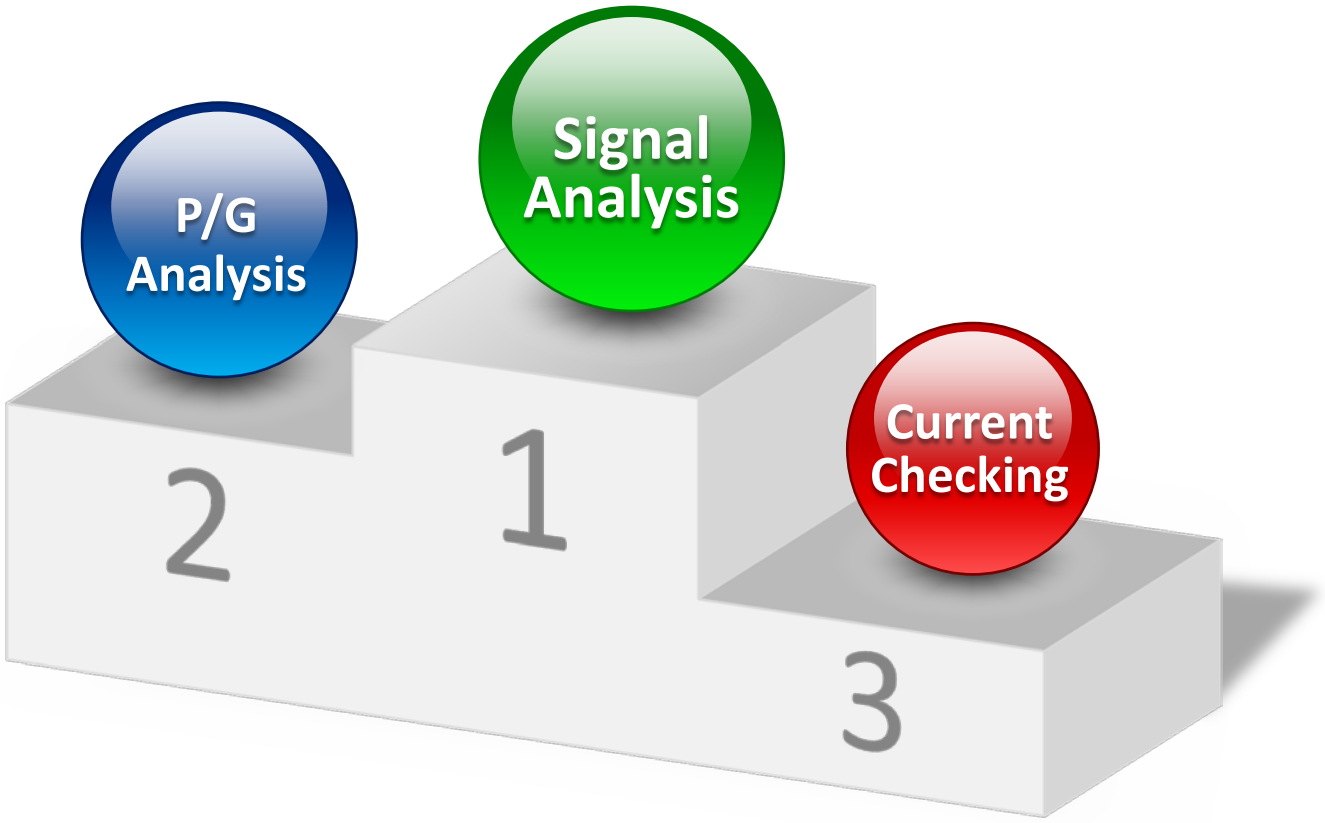
The XtractIM Electrical Performance Assessment functions

How to use XtractIM applications

1. Wirebond BGA RLC applications
2. Leadframe PKG RLC applications
3. Automation

Summary

EPA (Electrical Performance Assessment)

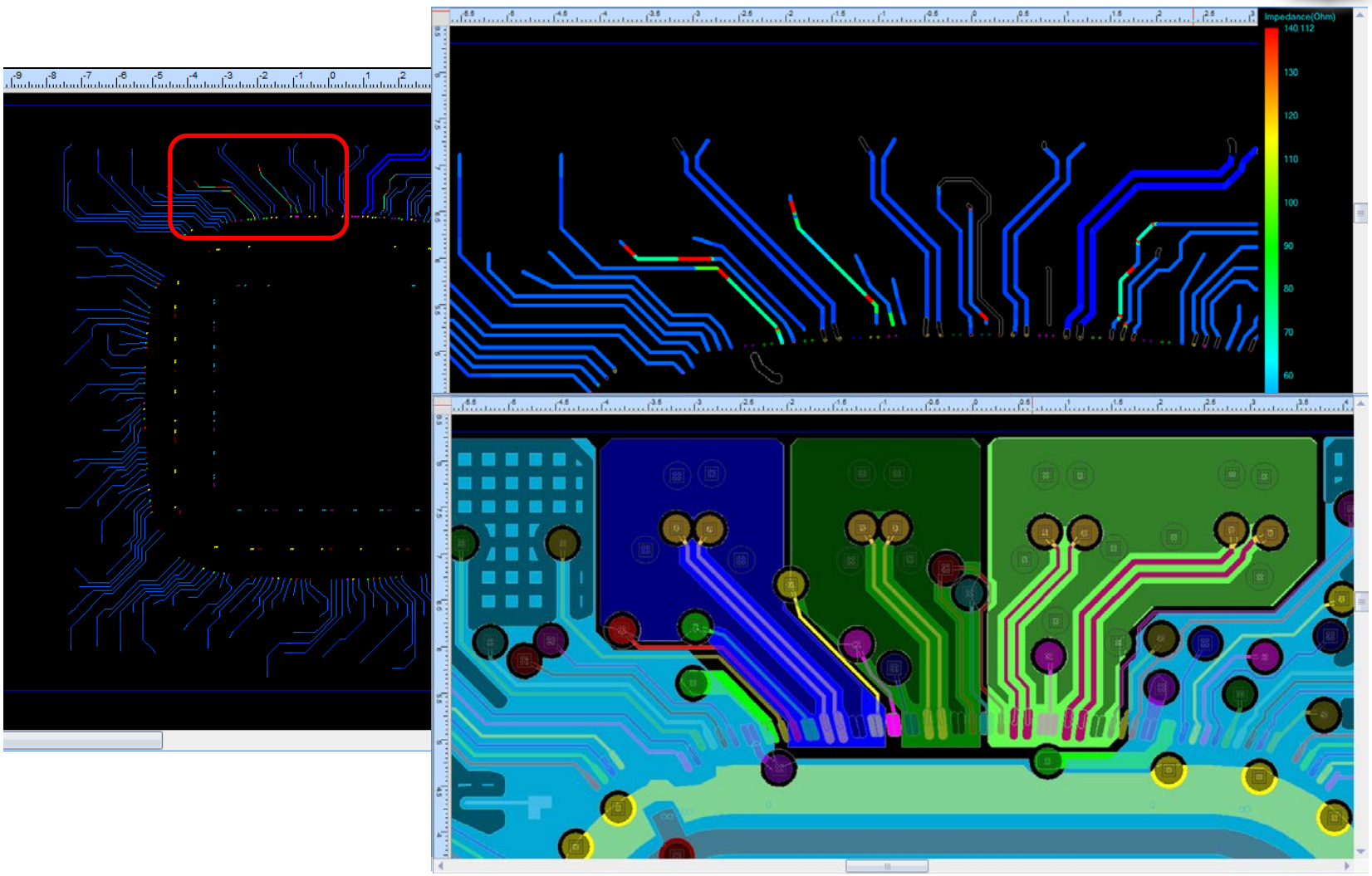


Three major functions that XIM EPA can support.

1. Signal analysis for signal integrity (SI)
2. P/G analysis for power integrity (PI)
3. Current checking for power integrity (PI)

Application1 – Impedance check

Signal Analysis



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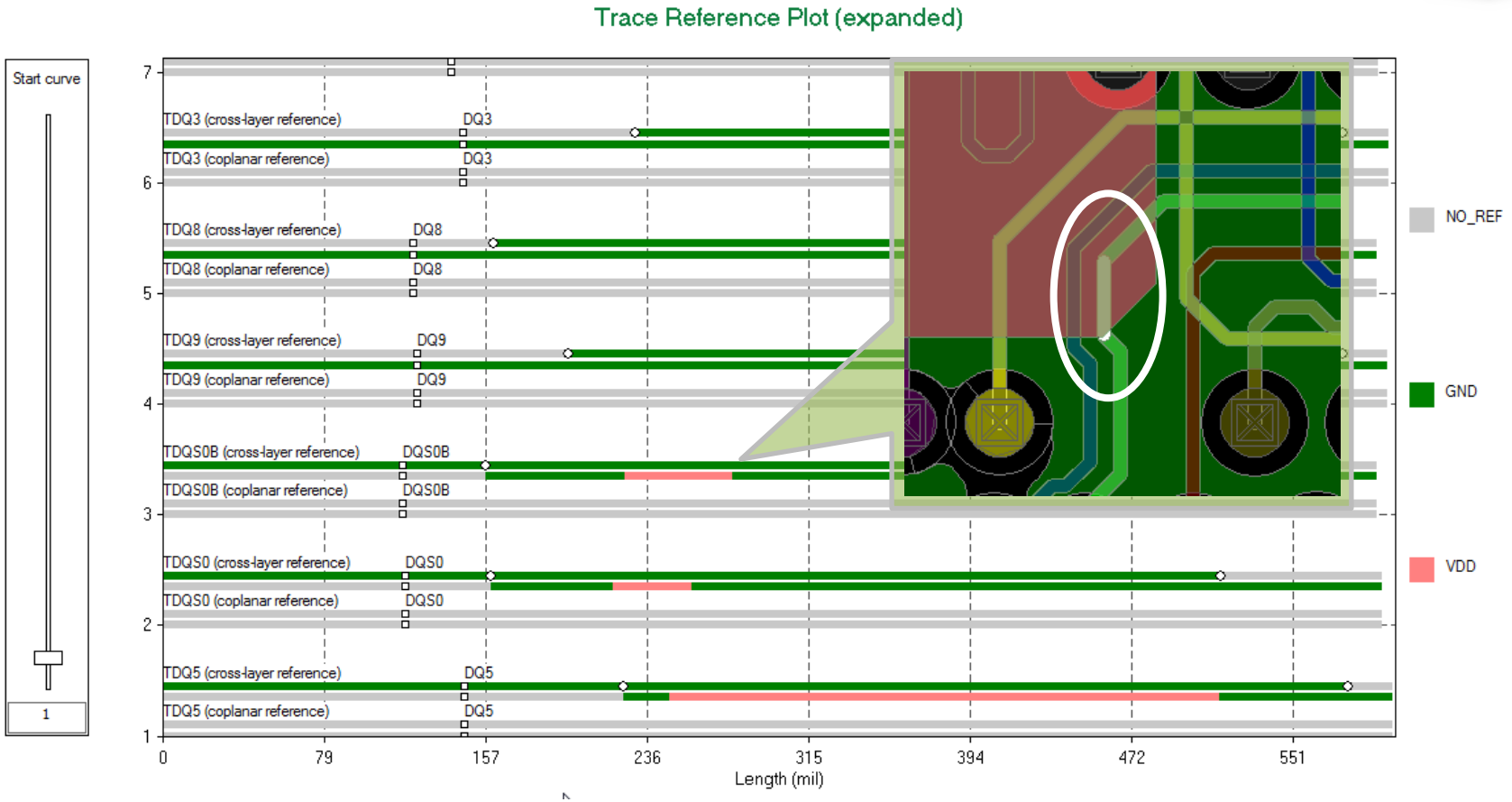
Application1 – Impedance check

Signal Analysis



- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

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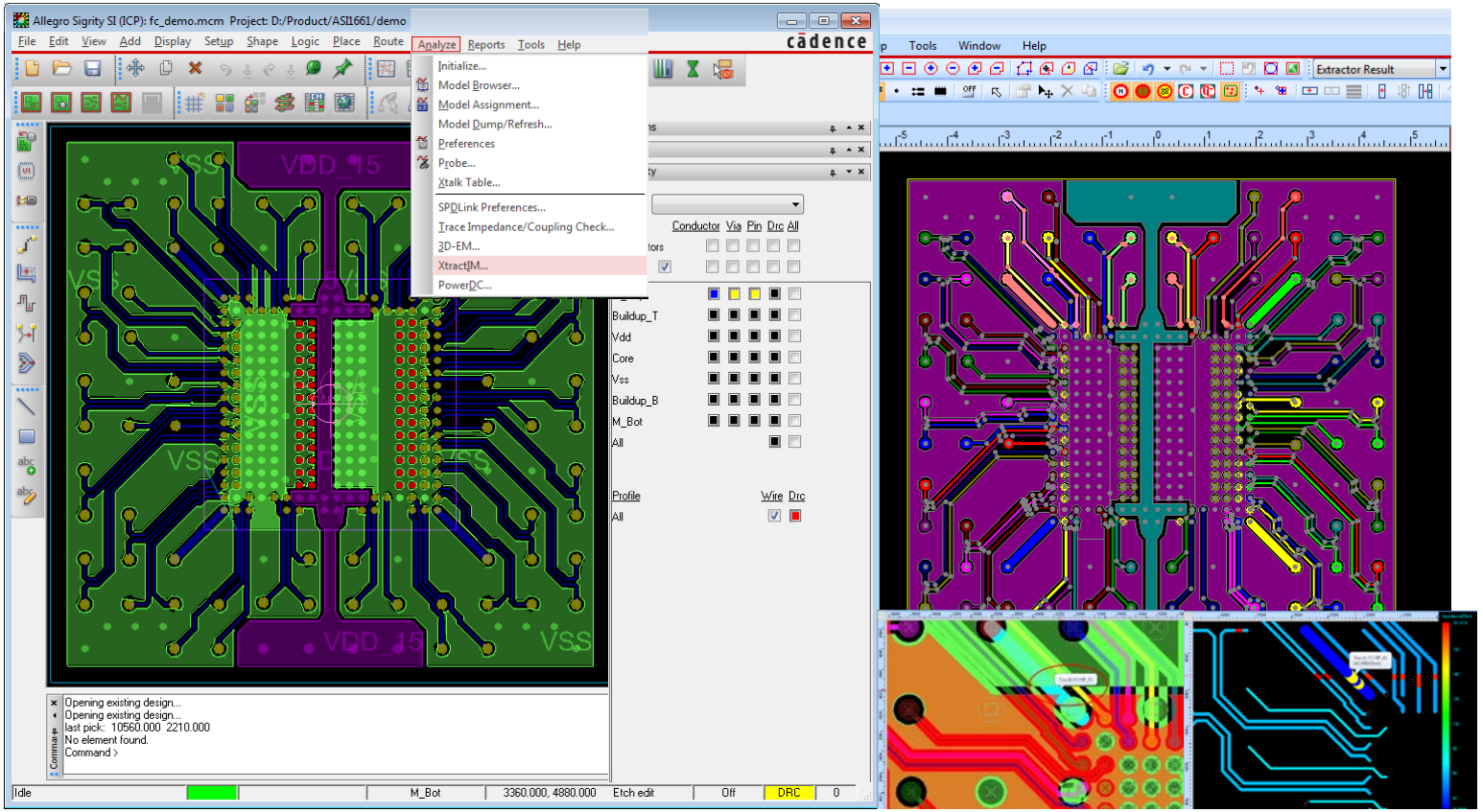
Application1 – Impedance check

Signal Analysis

APD →ASI →XtractIM Integration Flow



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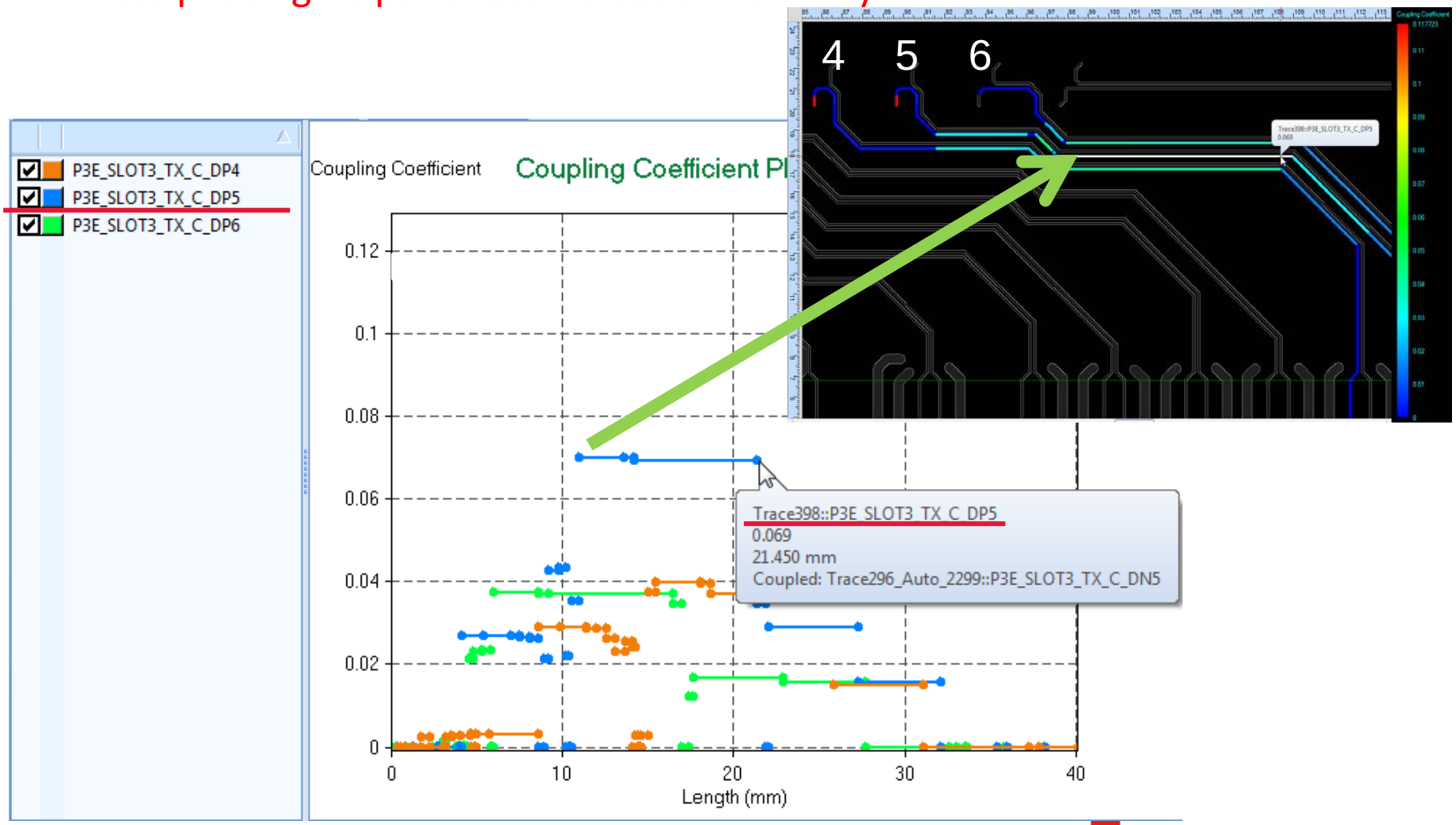
Application2 – Net Coupling Check

Signal Analysis

- Cross probing helps to resolve issue intuitively



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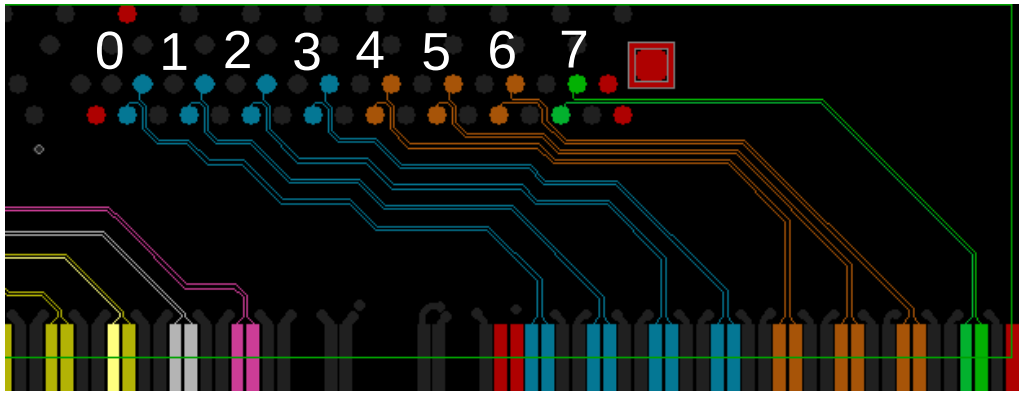
Application2 – Net Coupling Check

Signal Analysis

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
1	P3E_SLOT2_TX_C_DP0-P3E_SLOT2_TX_C_DN0	P3E_SLOT2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
2	P3E_SLOT2_TX_C_DP1-P3E_SLOT2_TX_C_DN1	P3E_SLOT2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
3	P3E_SLOT2_TX_C_DP2-P3E_SLOT2_TX_C_DN2	P3E_SLOT2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
4	P3E_SLOT2_TX_C_DP3-P3E_SLOT2_TX_C_DN3	P3E_SLOT2_TX_C_DN2	0.125%	36.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.125%	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

18X



Through this test, you will see,

- Tight coupling pairs
- Max coupling aggressor
- Dangerous vs. safe coupling
  → **18X**(= 2.81% / 0.156%)

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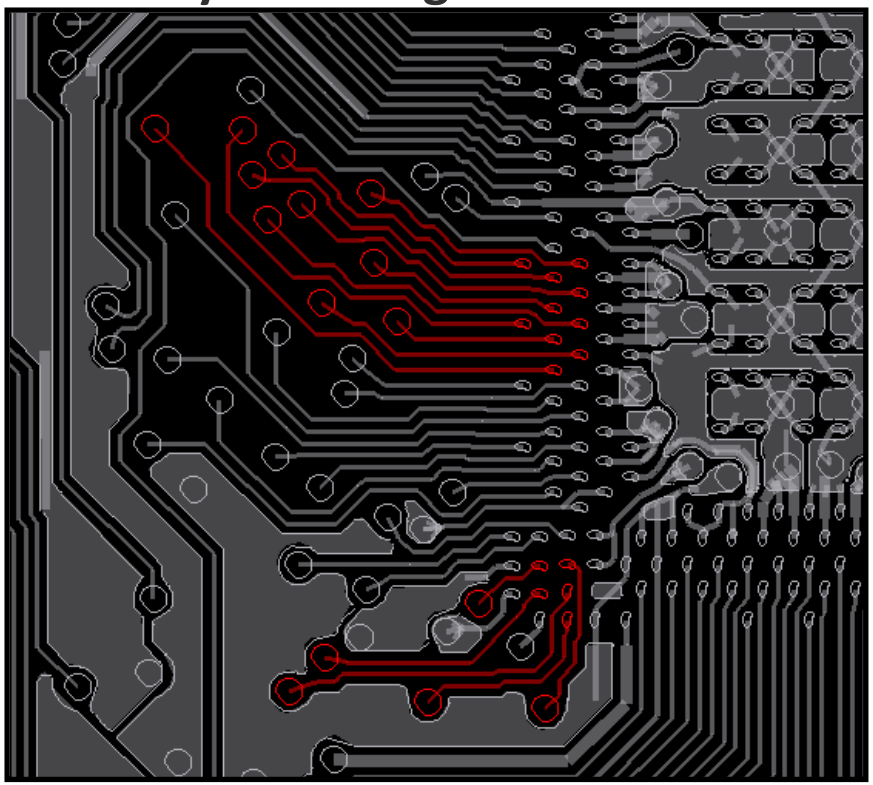
Application3 – Net Delay/Skew Check

Signal Analysis

Memory Bus Design



Net Length/Delay Summary

Net	Total trace length(...	Total trace delay(ns)
SDRAM_ADDR...	1.340	0.008
SDRAM_ADDR...	1.817	0.012
SDRAM_ADDR...	1.981	0.013
SDRAM_ADDR...	2.251	0.014
SDRAM_ADDR...	2.841	0.018
SDRAM_ADDR...	5.228	0.031
SDRAM_ADDR...	5.241	0.031
SDRAM_ADDR...	5.265	0.032
SDRAM_ADDR...	5.391	0.034
SDRAM_ADDR...	5.527	0.032
SDRAM_ADDR...	5.693	0.036
SDRAM_ADDR...	5.860	0.037
SDRAM_ADDR...	5.872	0.037
SDRAM_ADDR...	6.034	0.037
SDRAM_ADDR...	6.601	0.041

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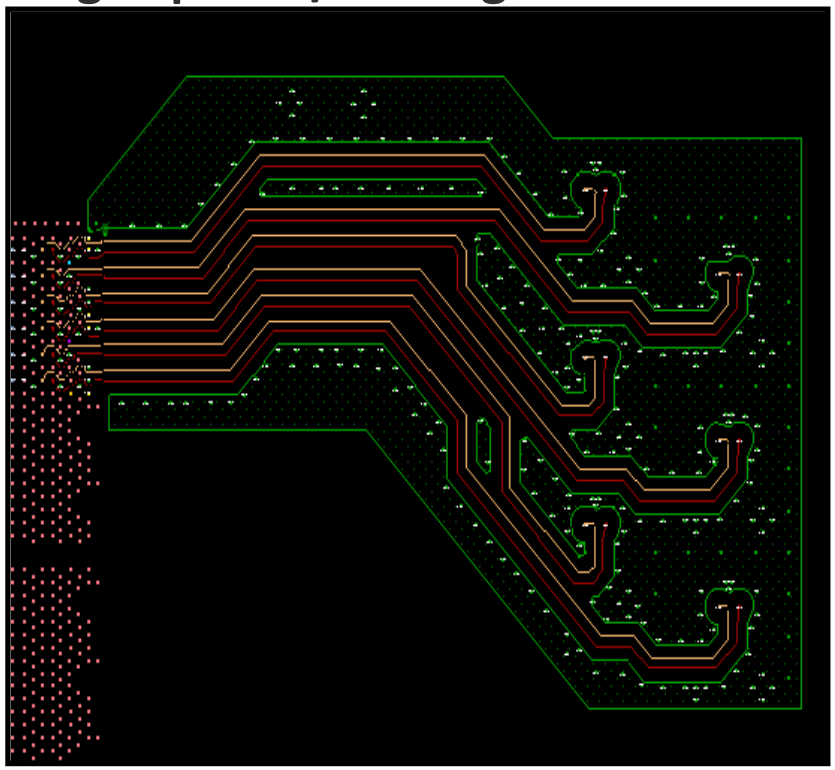
Application4 – RLC Check

Signal Analysis

High Speed I/O Design



Quick RLC Extraction

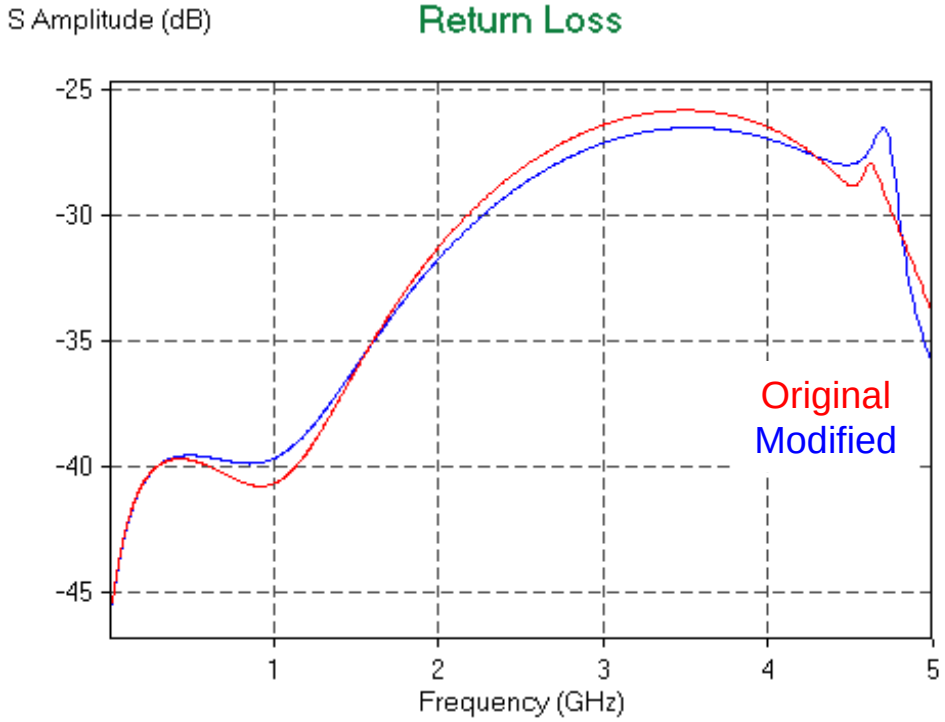
Power Net	Ref Groun...	L(nH)	C(pF)
1F_TX_0_N	VSS	5.5377	1.8513
1F_TX_0_P	VSS	5.5519	1.8704
1F_TX_1_N	VSS	4.7291	1.5823
1F_TX_1_P	VSS	4.7043	1.5878
1F_TX_2_N	VSS	5.1236	1.7420
1F_TX_2_P	VSS	5.1206	1.7351
1F_TX_3_N	VSS	4.4588	1.5081
1F_TX_3_P	VSS	4.4402	1.5160
1F_TX_4_N	VSS	4.9430	1.6869
1F_TX_4_P	VSS	4.9231	1.6848
1F_TX_5_N	VSS	4.2315	1.4292
1F_TX_5_P	VSS	4.2369	1.4276

Application5 – S-parameter Check

Signal Analysis

1F_TX_0 (Insertion loss)

1F_TX_0 (Return loss)



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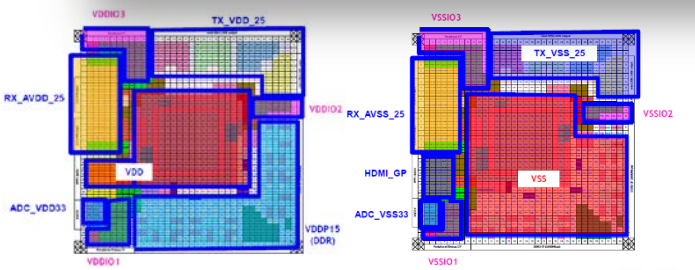
Application6 - PWR/GND Couple

P/G Analysis

Power Net	Ref Ground Net	L(nH)	C(pF)
EVDD18_TX	EVSS18_TX	0.0872	51.6027
VCCK	GNDK	0.1999	50.2715
VDDA12_VBO	VSSA12_VBO	0.5152	8.2681
VCCIO	GNDK	0.5342	1.8993
VCCIO18_EPI	EVSS18_TX	0.6679	2.5377
VDDQ	VSSQ	0.7138	8.6293
VDDA33_VBO	VSSA12_VBO	1.0993	1.9119
VDD2	VSSQ	1.3505	1.1996
EVDD18_PLL1	EVSS18_TX	1.5725	0.4981
EVDD18_PLL7	EVSS18_TX	1.5808	0.5554
EVDD18_PLL8	EVSS18_TX	1.5986	0.5181
EVDD18_LDOPLL7	EVSS18_TX	1.7999	0.4061
EVDD18_LDOPLL6	EVSS18_TX	1.8451	0.4020
EVDD18_LDOPLL8	EVSS18_TX	1.8834	0.5537
VDDCA	EVSS18_TX	2.0899	0.2757
EVDD18_PLL6	EVSS18_TX	2.1077	0.6014
EVDD18_LDOPLL4	EVSS18_TX	2.1681	0.5882



- Check if the reference is correct or not in current design.
- Check if inductance passes spec or not.

	Ref Ground Net	L(nH)	C(pF)
	EVSS18_TX	0.0872	51.6027
	GNDK	0.1999	50.2715
	VSSA12_VBO	0.5152	8.2681
	GNDK	0.5342	1.8993
	EVSS18_TX	0.6679	2.5377
	VSSQ	0.7138	8.6293
	VSSA12_VBO	1.0993	1.9119
	VSSQ	1.3505	1.1996
EVDD18_PLL7	EVSS18_TX	1.5808	0.5554
EVDD18_PLL8	EVSS18_TX	1.5986	0.5181
EVDD18_LDOPLL7	EVSS18_TX	1.7999	0.4061
EVDD18_LDOPLL6	EVSS18_TX	1.8451	0.4020
EVDD18_LDOPLL8	EVSS18_TX	1.8834	0.5537
VDDCA	EVSS18_TX	2.0899	0.2757
EVDD18_PLL6	EVSS18_TX	2.1077	0.6014
EVDD18_LDOPLL4	EVSS18_TX	2.1681	0.5882
VDD18_PLLEPI	EVSS18_TX	2.3472	0.4330

Ground Net	L(nH)
EVSS18_TX	2.08988
VSS	2.10294
GNDK	2.12942
VSSQ	2.36701
GNDIO	2.39219
VSSCA	2.58214
VSSIO18_EPI	2.60306
VSSA12_VBO	2.78448
VSSA33_VBO	2.874
EVSS18_PLL1	3.70874
EVSS18_LDOPLL6	3.8871
EVSS18_LDOPLL7	3.89717
EVSS18_LDOPLL8	4.0381
EVSS18_PLL8	4.07865
EVSS18_PLL7	4.13481
EVSS18_LDOPLL1	4.14524
EVSS18_PLL6	4.16143
EVSS18_LDOPLL4	4.34497

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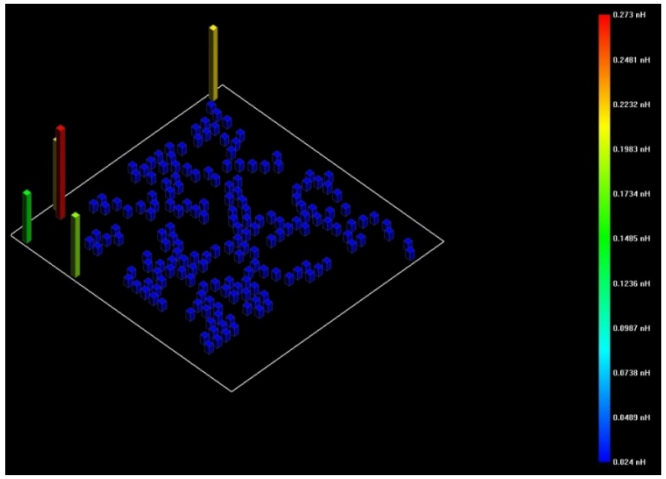
P/G Analysis

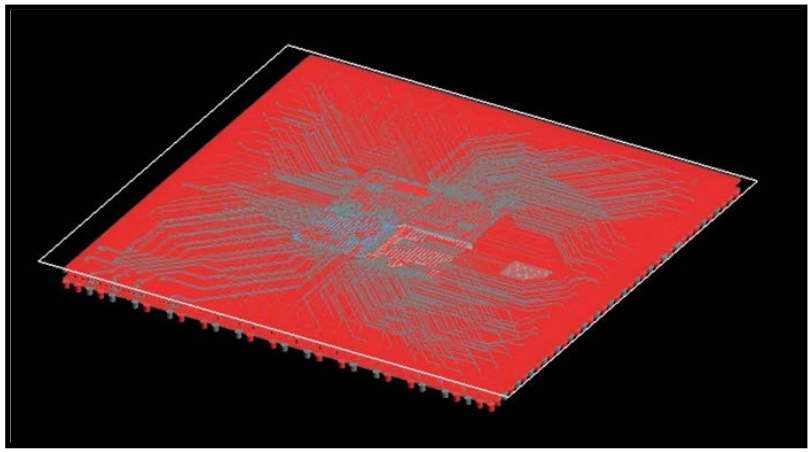
Application7 – PDN Performance

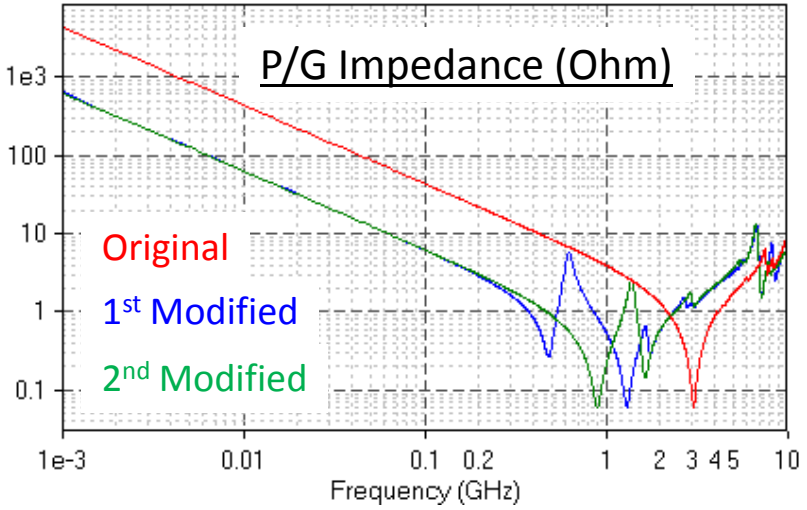
Per Pin Inductance:



Pin NodeName	Self L(nH)	Total L(nH)	R(mOhm)
Node022704!!2_VSS::VSS	0.024	3.807	3.020
Node022705!!3_VSS::VSS	0.024	3.807	2.985
Node022706!!4_VSS::VSS	0.024	3.807	3.709
Node022707!!5_VSS::VSS	0.024	3.807	3.004
Node022708!!6_VSS::VSS	0.024	3.807	3.028
Node022709!!7_VSS::VSS	0.024	3.807	3.056
Node022710!!8_VSS::VSS	0.024	3.807	3.087
Node022711!!9_VSS::VSS	0.024	3.807	2.887
Node022712!!10_VSS::VSS	0.024	3.807	3.168
Node022714!!12_VSS::VSS	0.024	3.807	2.921
Node022715!!13_VSS::VSS	0.024	3.807	3.151
Node022716!!14_VSS::VSS	0.024	3.807	3.317
Node022717!!15_VSS::VSS	0.024	3.807	4.638
Node022718!!16_VSS::VSS	0.024	3.807	3.608
Node022721!!19_VSS::VSS	0.024	3.807	3.062

Impedance Extractions:





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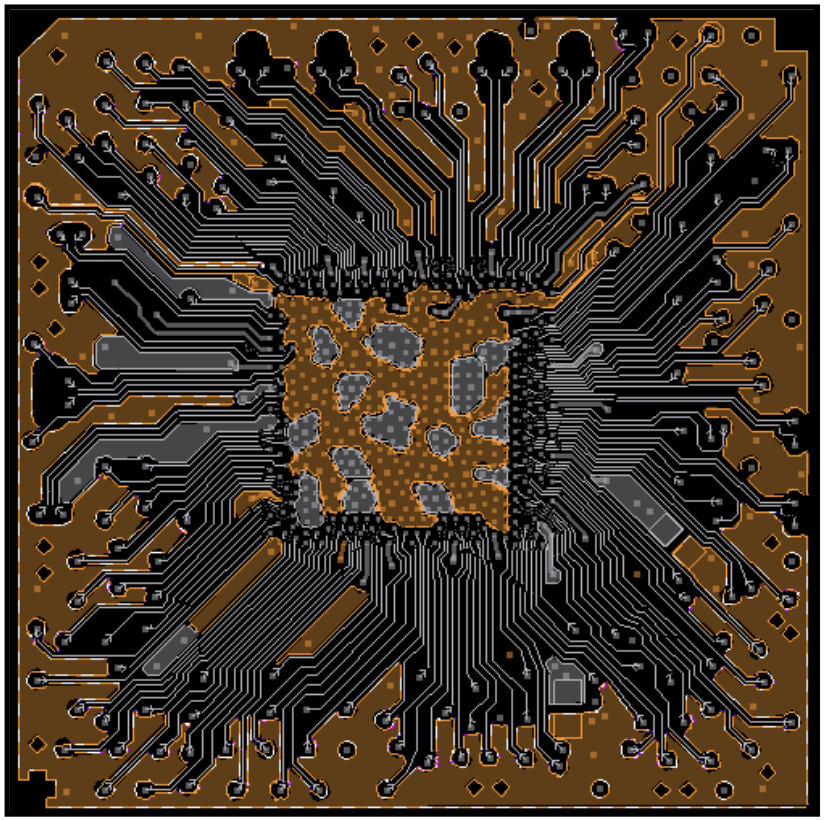
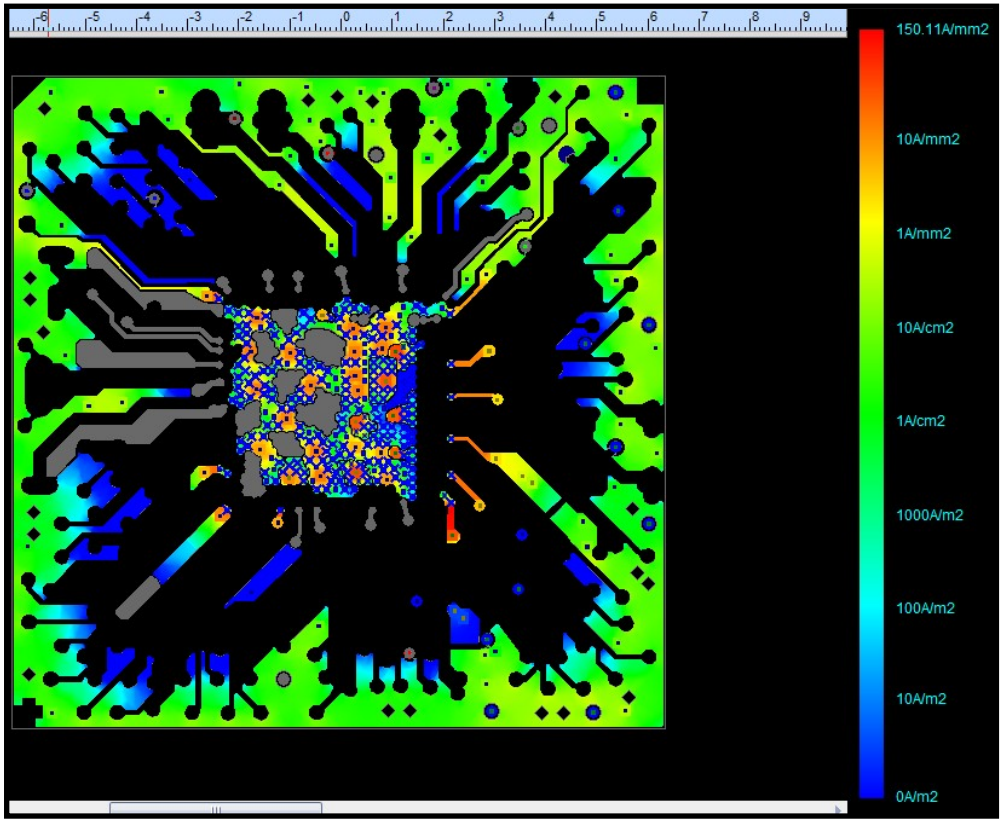
Application8 – Current Density

Current Checking

- PDN design optimization through current density





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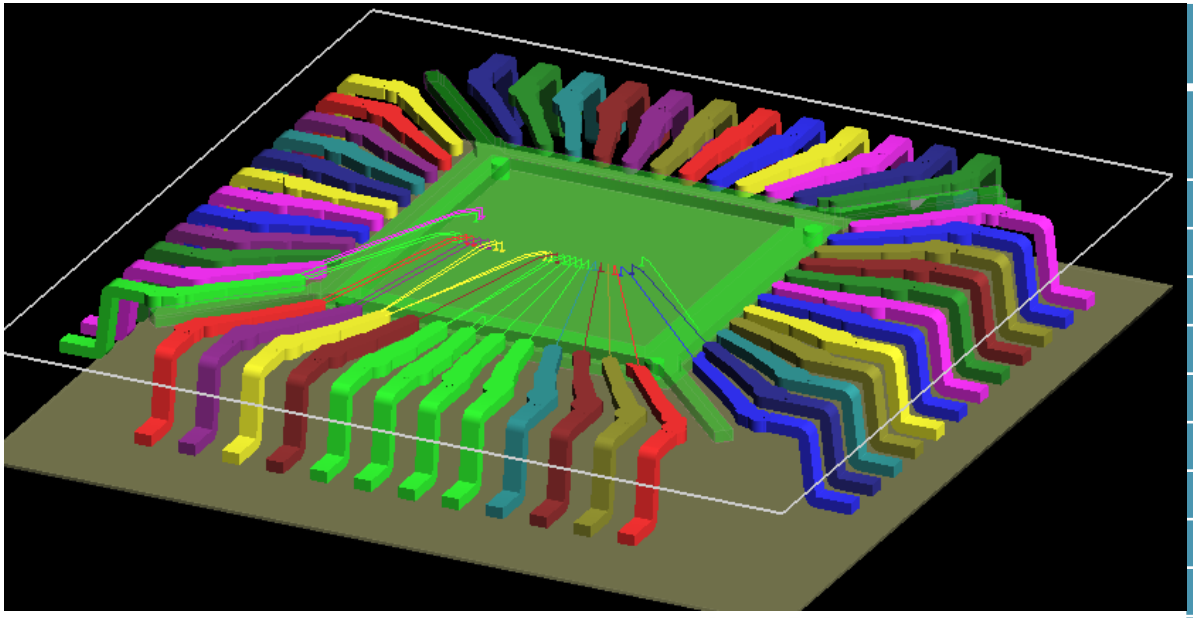
Application9 - Leadframe Model



	Other Tool		XtractIM	
	R (mohm)	AC L (nH)	R (mOhm)	L (nH)
Lead11	135.4	3.51	114.9	3.475
Lead12	98	3.19	80.4	3.124
Lead13	133.3	3.49	111.0	3.578
Lead14	129.1	3.29	105.8	3.301
Lead15	76.2	2.88	61.1	2.859
Lead16	241.9	3.63	198.8	3.745
Lead17	124.8	3.05	102.2	3.177
Lead19	209.5	3.27	169.9	3.441
Lead20	196.1	3.26	165.2	3.469
Lead21	208.3	3.30	166.7	3.516
Lead22	214.9	3.41	173.0	3.644
Lead23	227.5	3.61	182.4	3.802
Lead24	242.5	3.85	196.4	4.068
Lead25	236	3.83	191.4	3.994
Lead26	211.4	3.51	172.1	3.679

5mins model build

1mins model simulation

1. Wirebond pattern study
2. Special lead pattern study

EPA functions

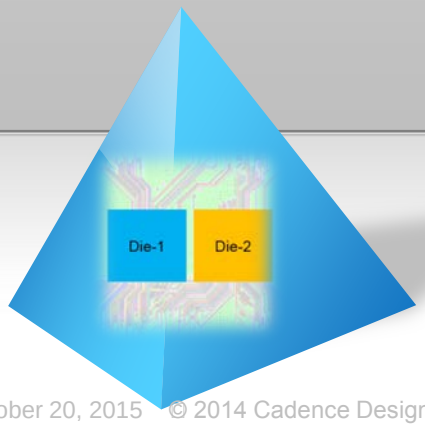
P/G Checking

Net based

1. Find worse loop L & unbalance inductance
2. Find which ground net with the minimum loop inductance

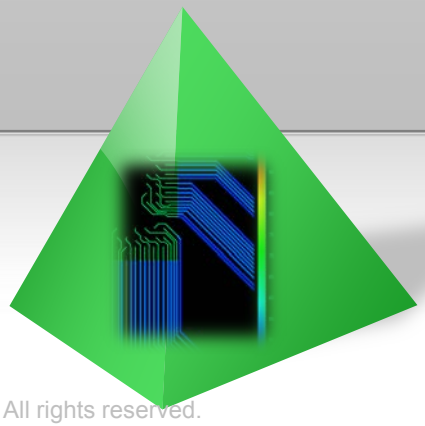
Pin based

1. Easy to find per pin inductance
2. Find the power pin with the lowest coupling



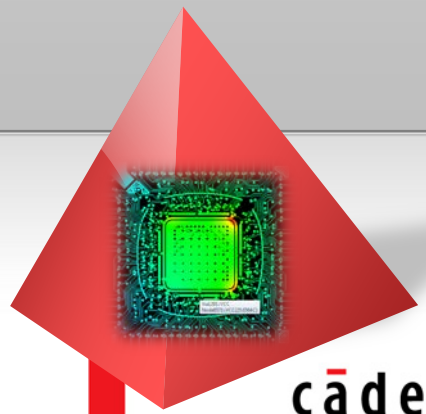
Signal Checking

1. Fast find out the impedance discontinuity location
2. Fast find out the timing difference between max. and min. trace
3. Coplanar net checking
4. Fast find out which net had big coupling



DC Current Checking

1. Identify IR drop bottleneck area included vias, shapes,..
2. Identify high current density area that exceeds limit (PDC)
3. Avoid regional over-heat caused by high current density (PDC)



How to use these applications

Case1 - The numbers of wirebond effect

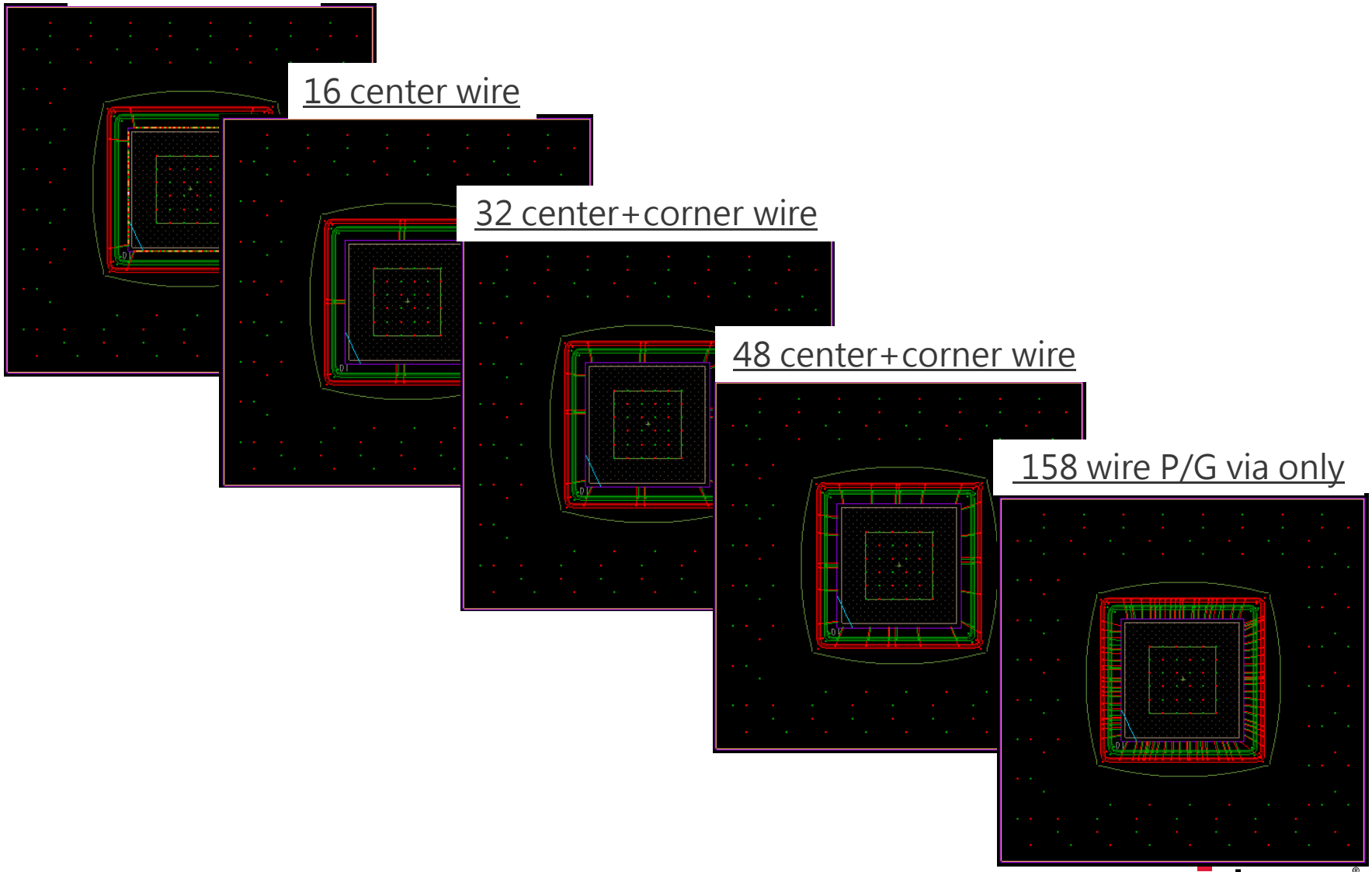
16 corner wire

16 center wire

32 center+corner wire

48 center+corner wire

158 wire P/G via only



Case1 - The numbers of wirebond effect

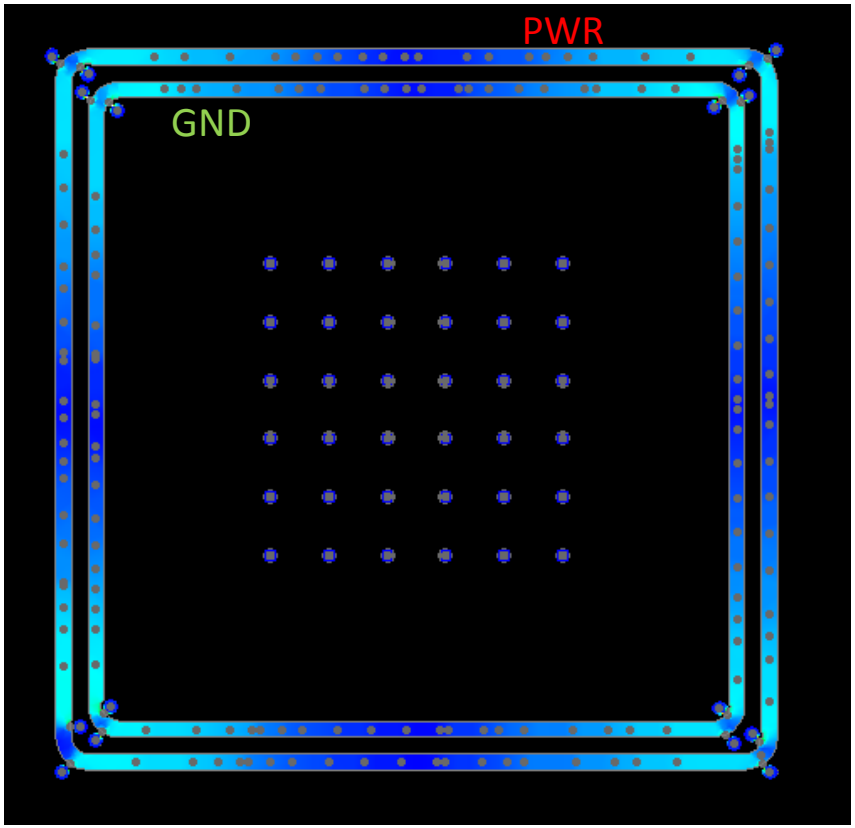
Case	PWR DC-R	GND DC-R	Difference Of PWR
Customer spec.	3.7	3.2	
16 corner wire	15.7	11.0	+324.3%
16 center wire	16.8	12.6	+354.1%
32 center+corner wire	9.0	6.9	+143.2%
48 center+corner wire	6.8	5.3	+83.8%
158 wire P/G via only	3.7	3.2	Target

1. More wirebonds can get lower DC-R.
2. It seems that the DC-R will be converged if added enough wire

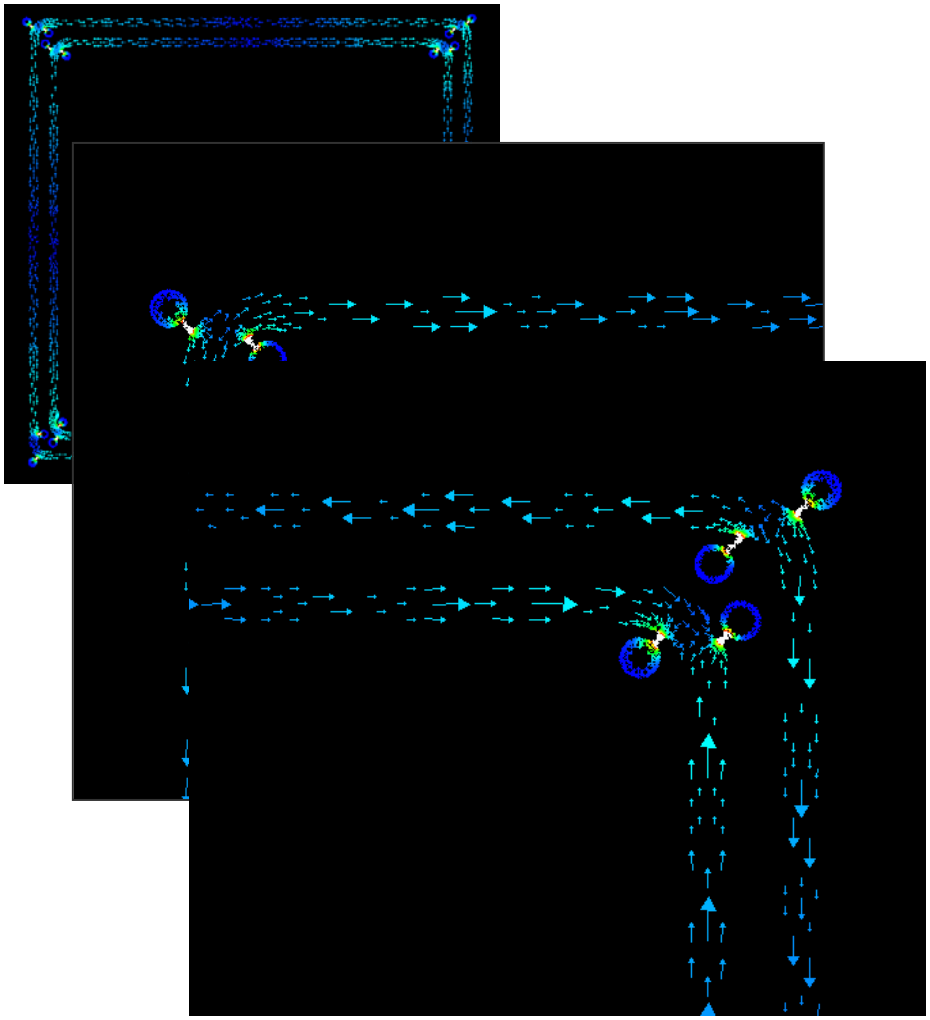
How do we efficiently add wirebonds if limited wirebonds?

Case1 - The numbers of wirebond effect

P/G current density

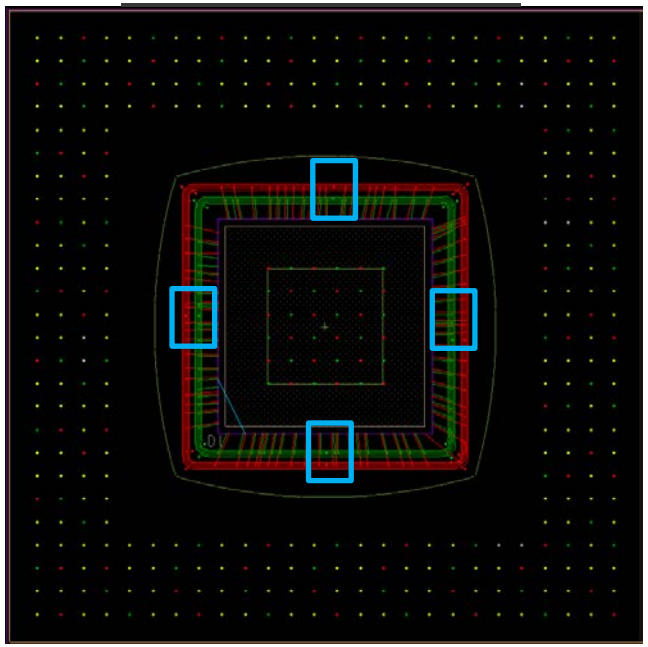


P/G current density with cursor

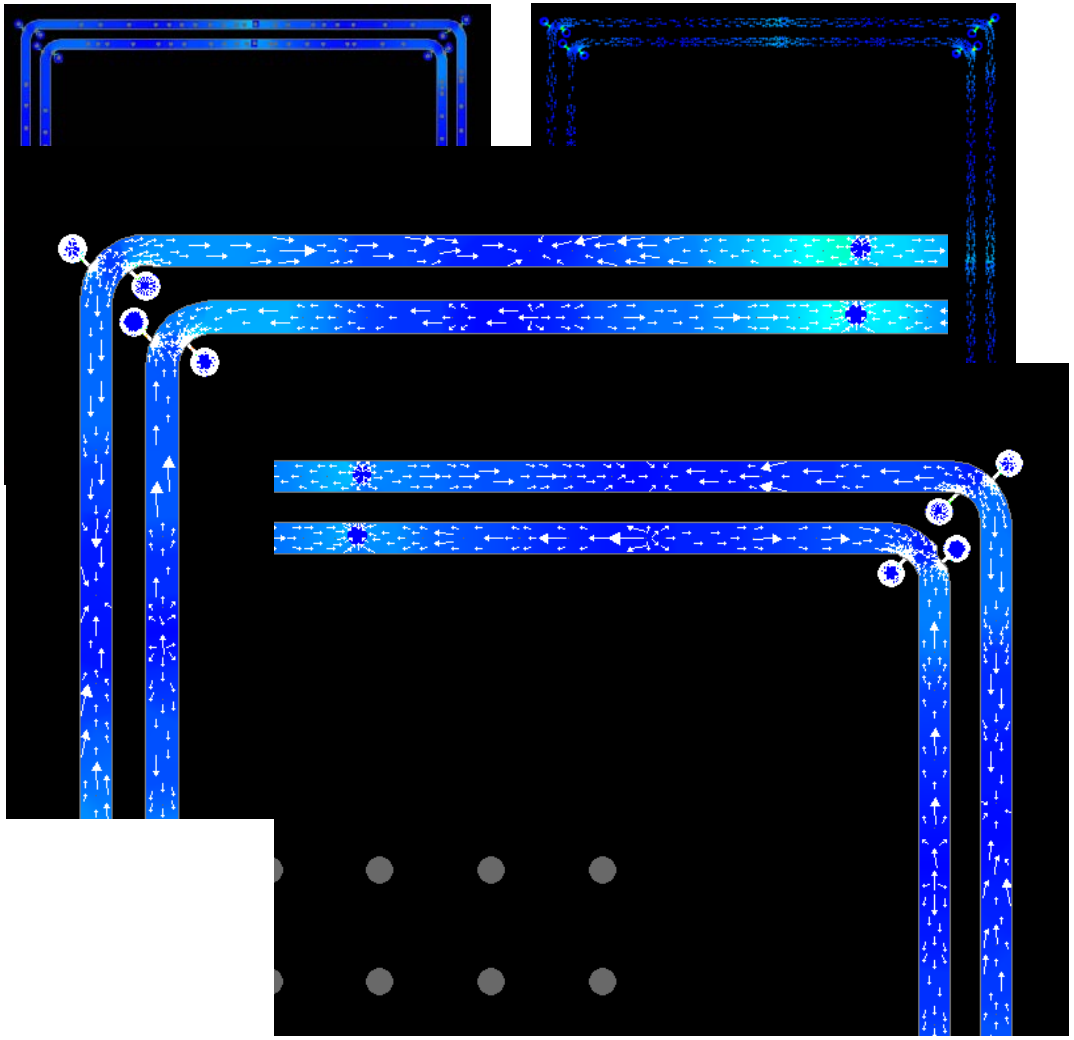


Case1 - The numbers of wirebond effect

158 wire P/G/S
via+manual added



P/G current density with cursor



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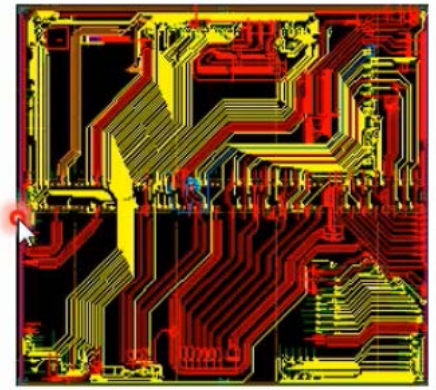
48 center+corner wire	6.8	5.3	+83.8%
158 wire P/G via only	3.7	3.2	Target
158 wire P/G/S via+manual added	2.1	1.6	-43.2%

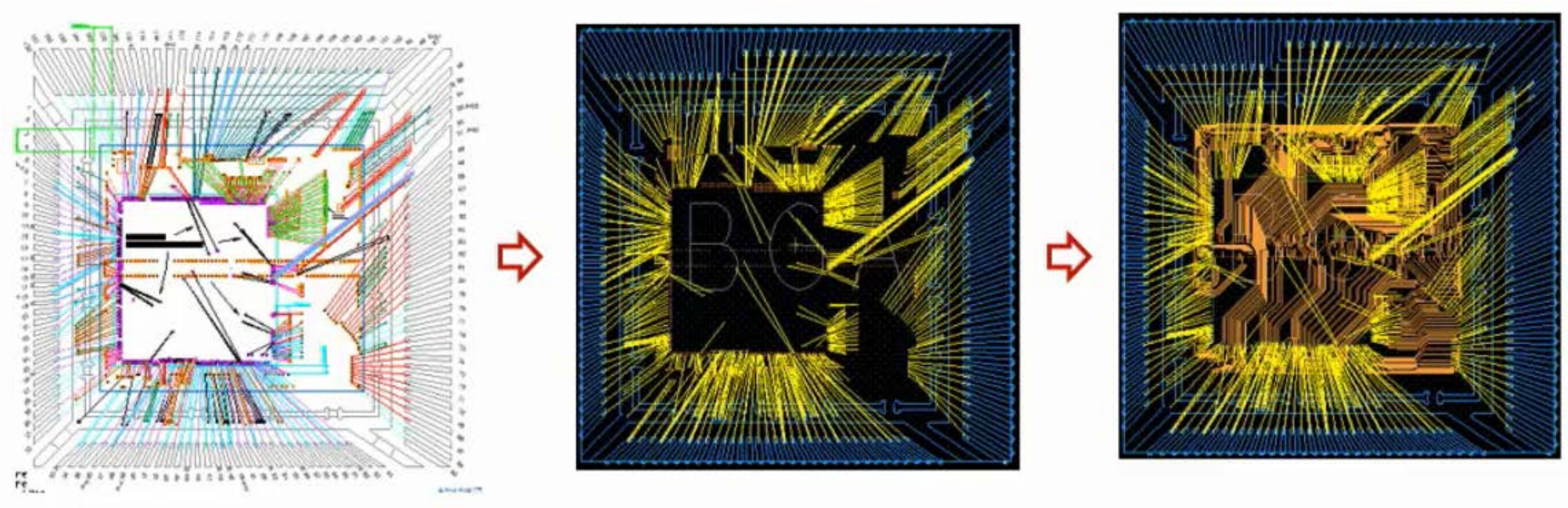
Reduce current density can reduce DC-R effectively.

Case2 – Leadframe PKG with RLC application

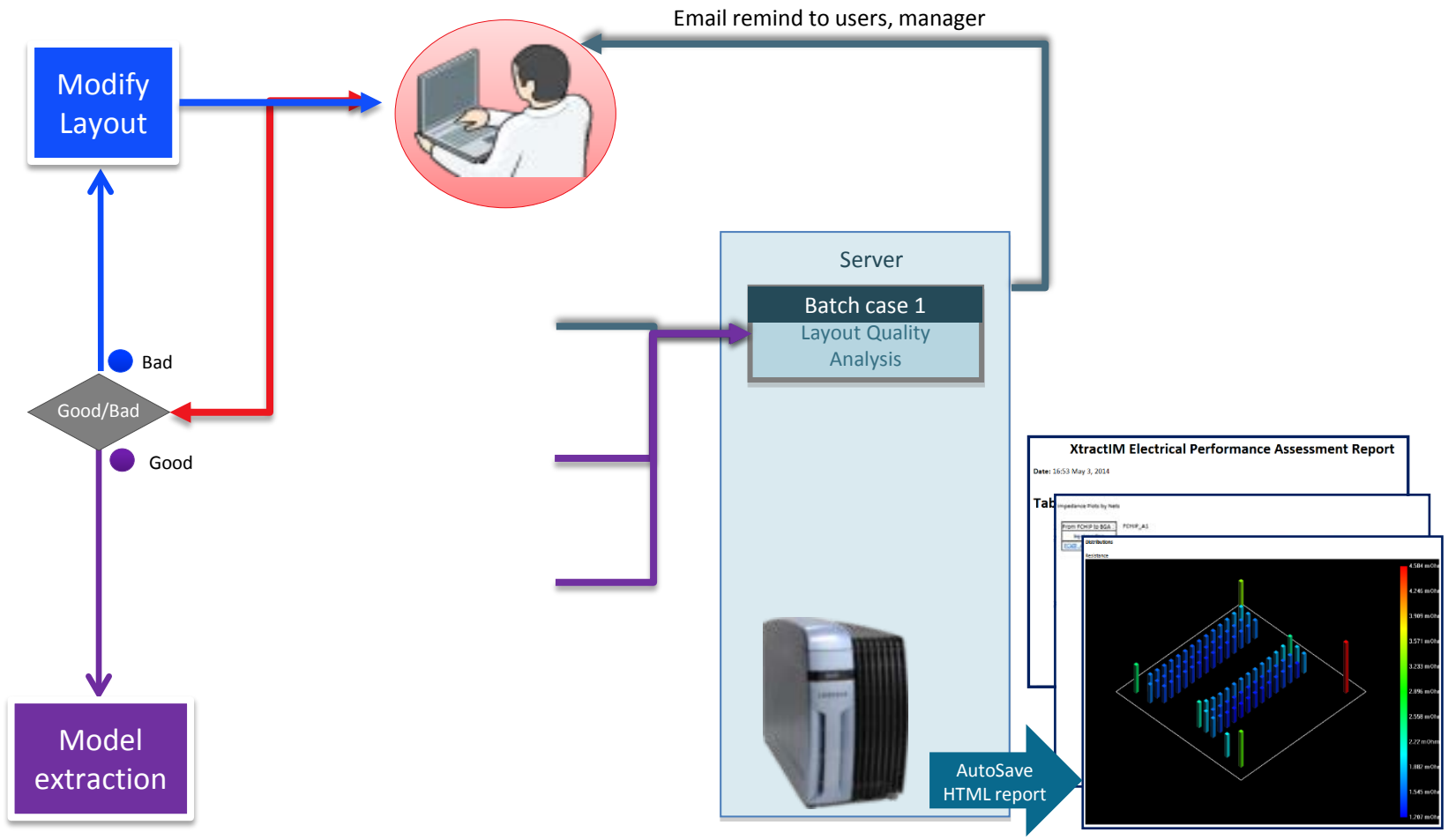
Three major issue for the electrical tools

1. DXF to APD/SiP with netlist in
2. RDL to APD/SiP with netlist in
3. Run time





Case3 - Automation check by TCL commands

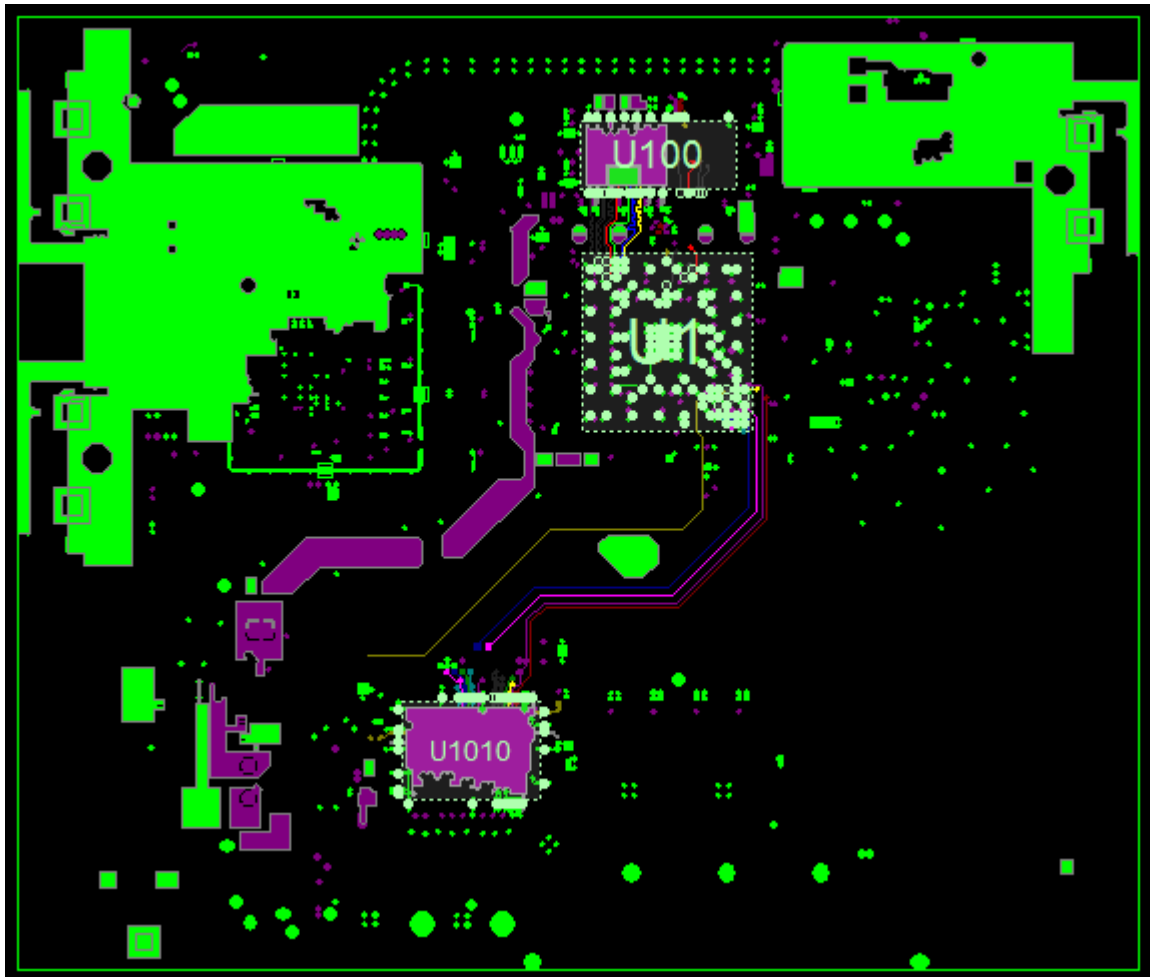


Summary

- Allegro + Sigrity enables seamless physical and electrical design flow
  - Easy for use
  - Well layout version control for simulation
  - Fast for simulation
  - Support automation

- Fast to find and optimize potential risk
  - Impedance/ Trace Timing
  - Power/Ground Inductance
  - Power/Ground Current Density
  - …

Is it possible to check PCB layout ?



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