Smart Die/Package/PCB Planning and Optimization - 跨晶片/封裝/電路板的評估與優化

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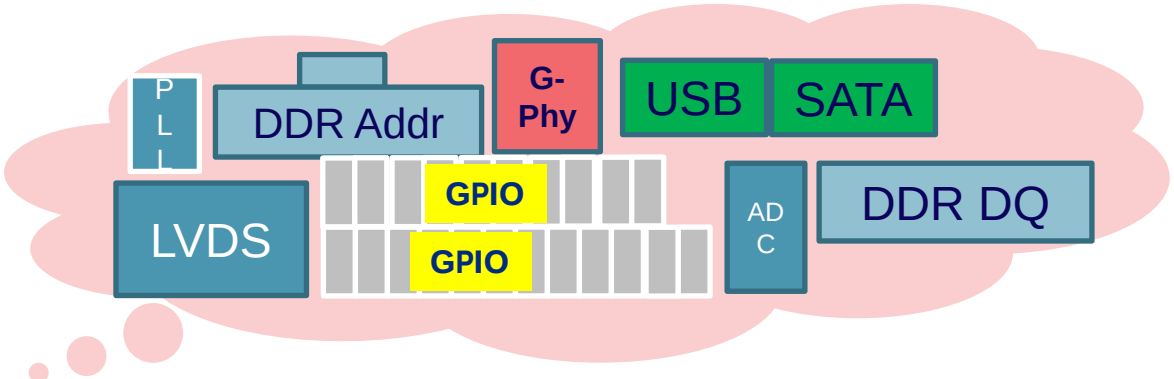
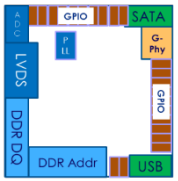
Agenda

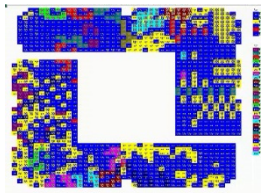
- Design Optimization Challenges
  - Cost vs. Performance vs. Time
- IC-PKG-Board Co-Design Solutions
- More Design Scenarios
- Summary

Chip-Package Evaluation Problem

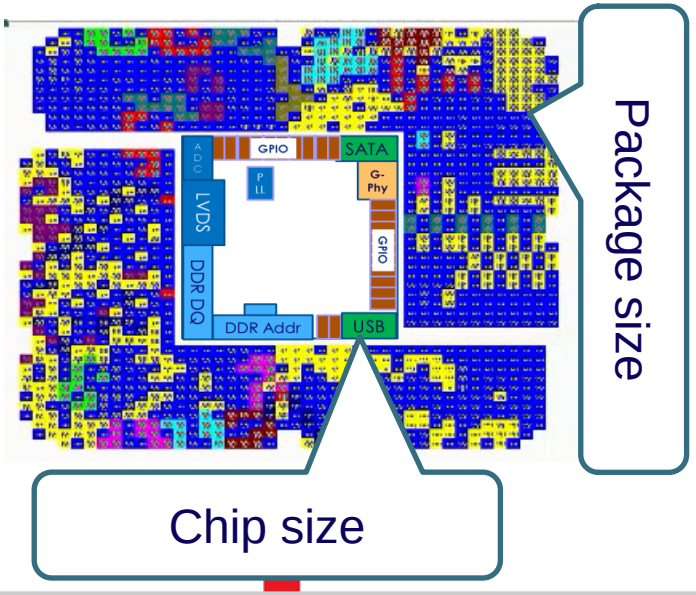
Faraday
CDNLive 2015







- Accuracy
- Data exchange
- Netlist Management



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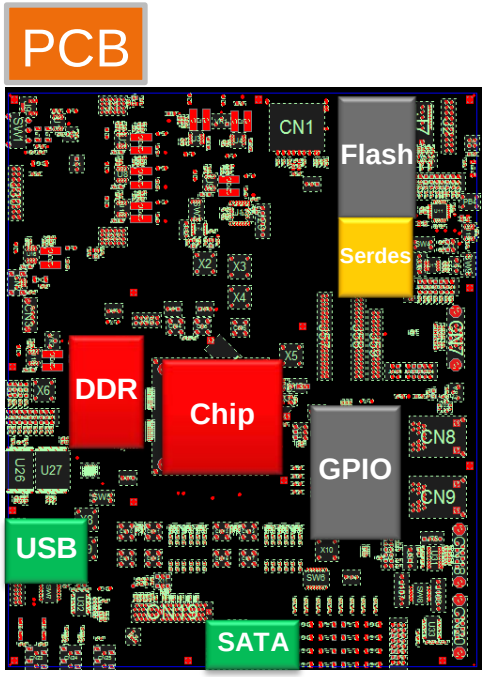
Co-Design Scenario and Barriers

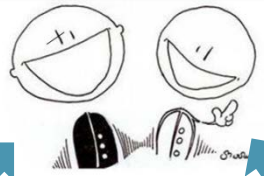
Pains for:

1. Lack global view to assign connectivity.
2. Long iteration time to converge Ball/Bump assignment.
3. ECO issue and Netlst maintenance.
4. Suffering the ASIC schedule.



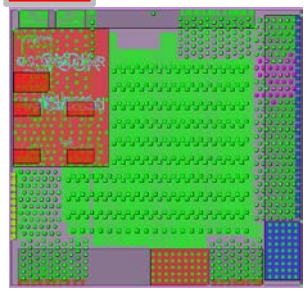
1 PCB

Project Leader works with **PCB** Engineer P&R to converge BGA



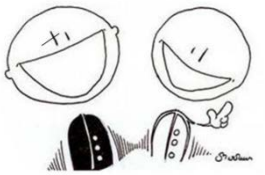
2 weeks

IC



2 IC

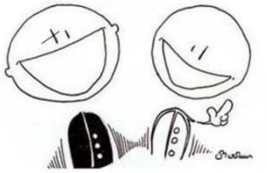
Project Leader works with IC P&R Engineer IO Placement



2 weeks

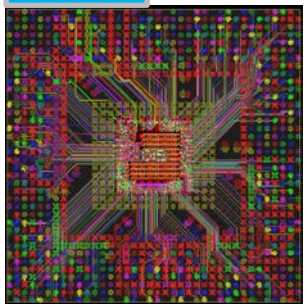
3 PKG

Project Leader works with PKG Engineer Bump Pin Generation



2 weeks

PKG



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Proposed Co-Design Solution

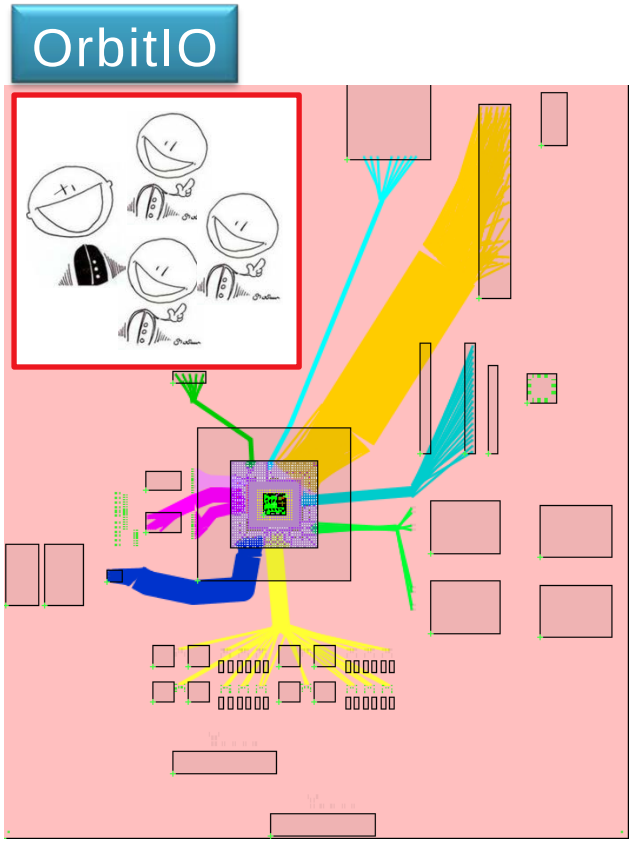
Resolved Pains:

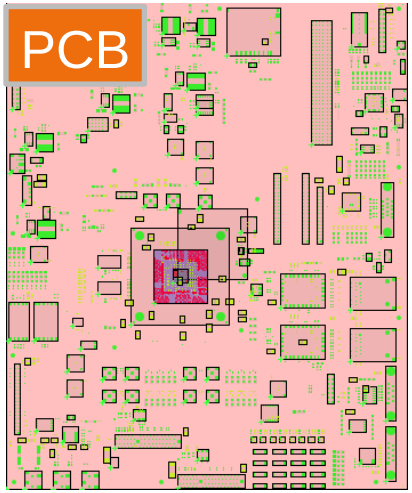
1. Co-design platform to include PCB-PKG-IC.
2. Global view to discuss Pin-Net assignment.
3. Net Manager to maintain Hierarchical Netlst.
4. Improve ASIC design cycle time.

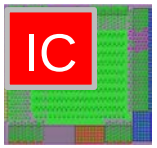
PCB
- Critical part placement
- BGA matrix & nets
- Escape routing

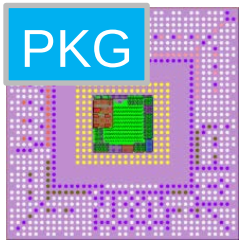
IC
- GPIO & Macro placement
- Bump matrix & net list
- RDL tech and patterns
- Signal – PG ratio

PKG
- Bump pattern & nets
- Ball matrix & net list
- PG supply strategy
- Substrate/RDL routing









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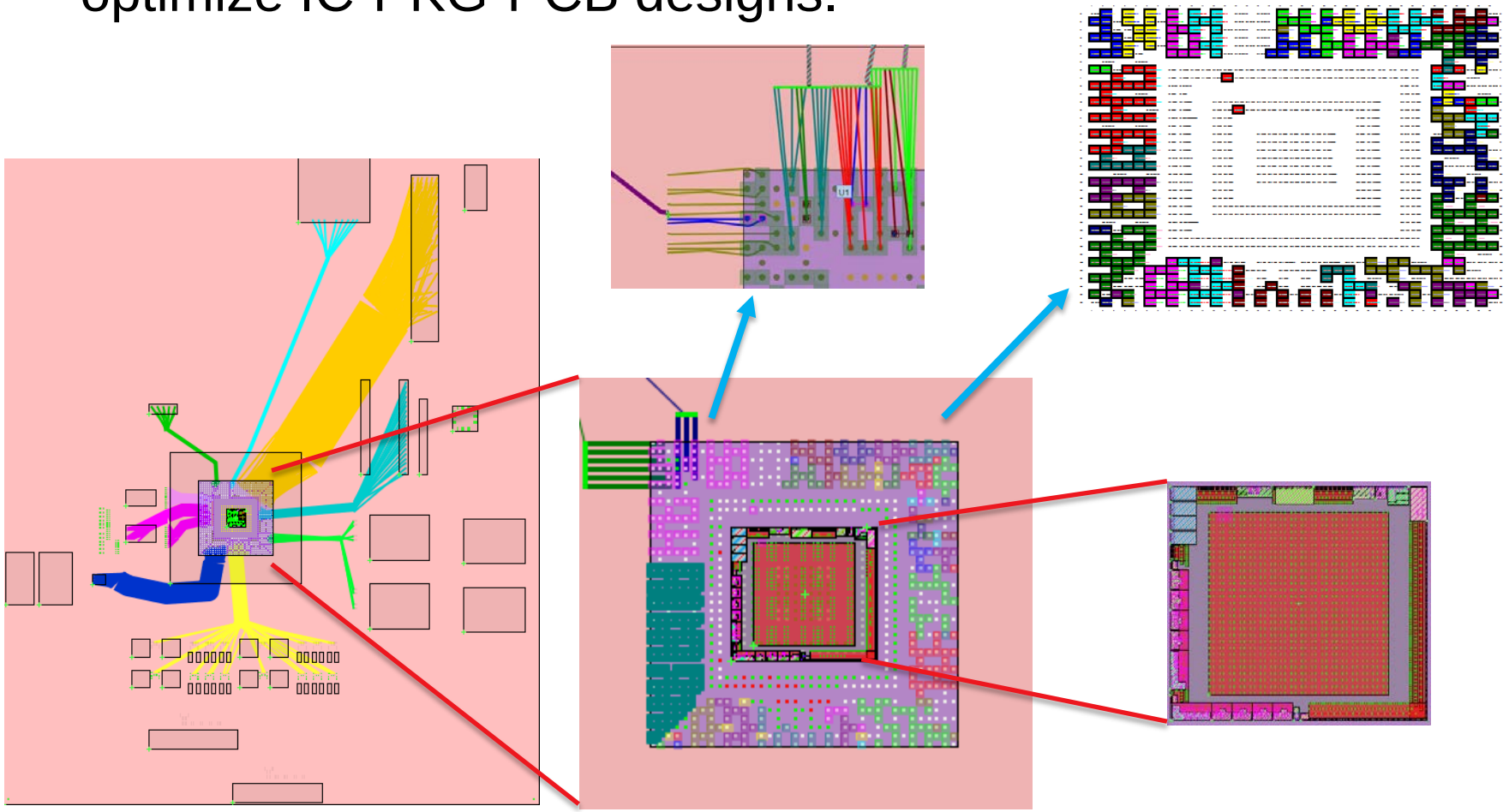
Multi-Dimensional Co-Design

- System view with multi-Dimensional data and tools to optimize IC-PKG-PCB designs.



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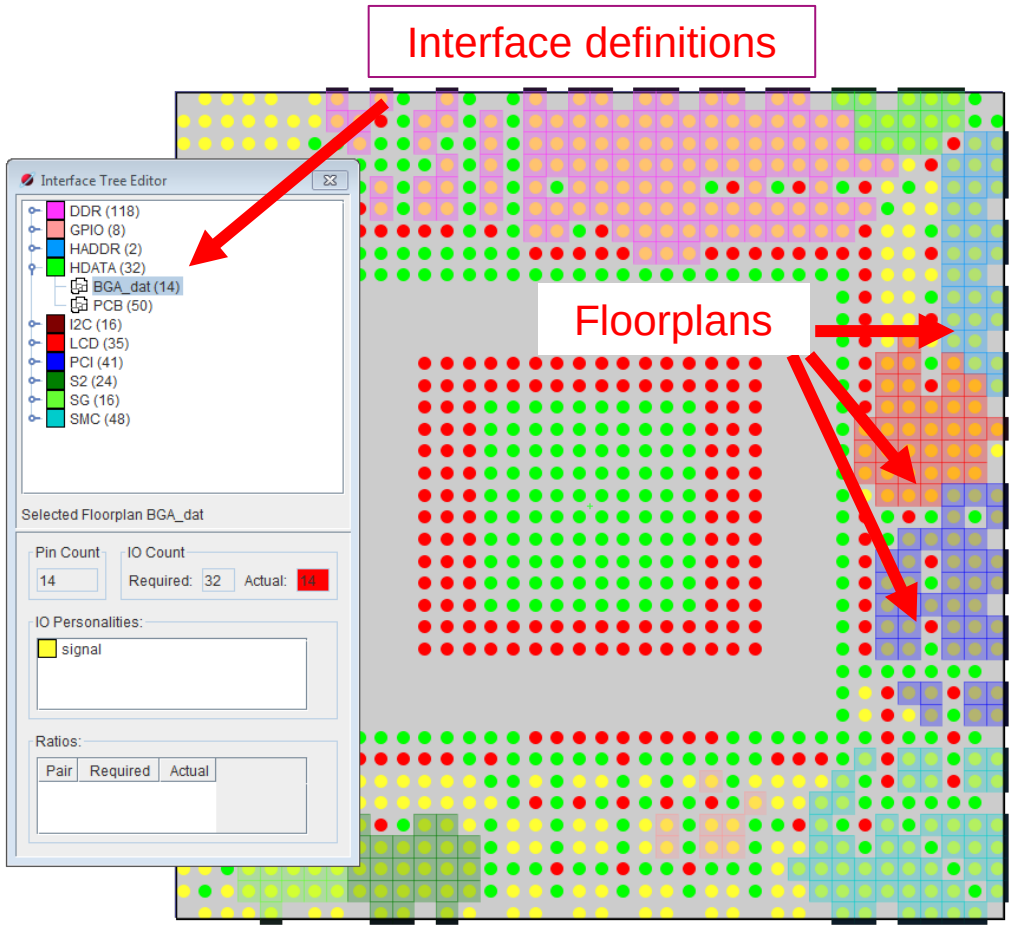
Interface Driven Floorplan capability

- Interface
  - A system level logical grouping of signals grouped hierarchically by function - DDR4, PCIe Gen 3, SATA, etc…
  - May contain any levels of hierarchical sub-interfaces (bank0, bank1, etc.)
- Floorplan
  - The physical application of an interface to a specific device
  - Elements of a floorplan:
    - Pins, bit count, personalities, signal-power-ground ratios
  - May be moved and swapped



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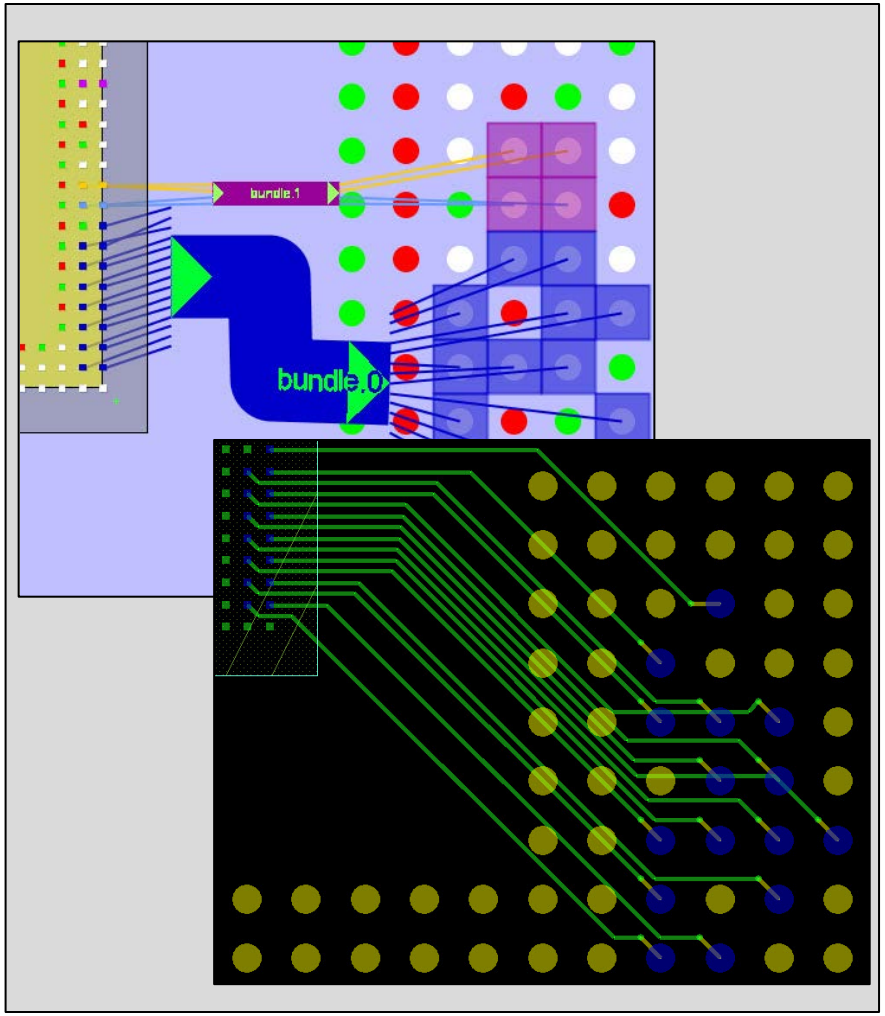
Bundle Driven Pin-Net Assignment

- Route planning and connection optimization
  - Define route plans to guide implementation
- Route feasibility
  - Validate route plan quality and configuration
  - Minimizes iterations between design teams
- Integration with SiP Layout
  - Single file exchange to communicate design intent
  - Design tool compatibility with OSATs
- Detailed routing using imported route plan
  - Auto-Interactive Breakout Technology (AiBT)
  - Advanced Package Router (APR)



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Auto-Interactive Route Environment

Iterative Planning and Route Approach

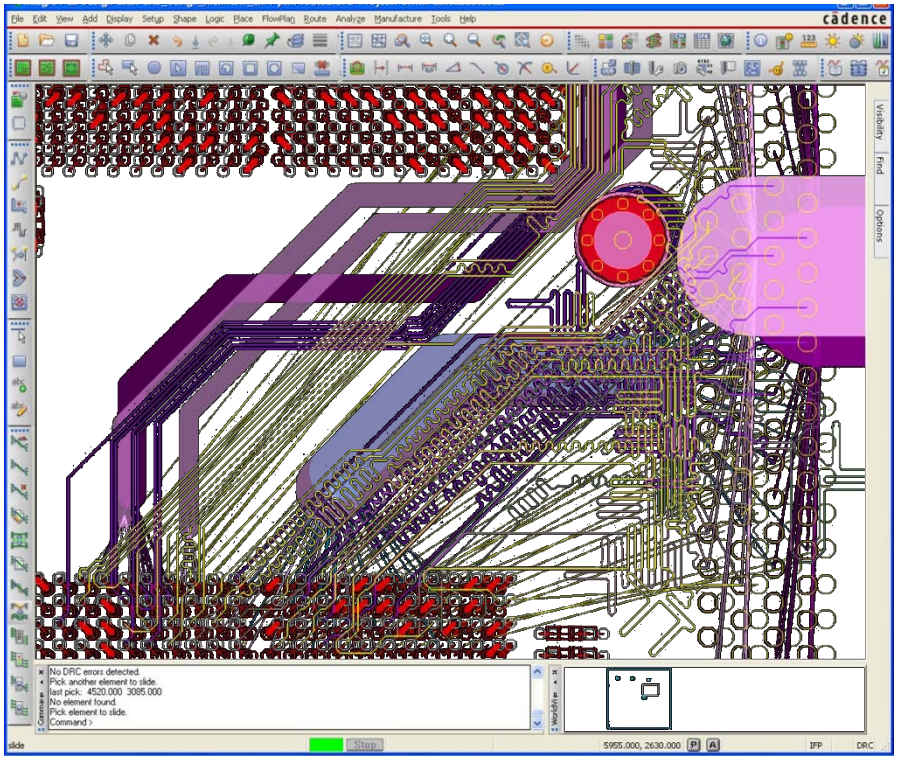
- Iterative stages of route planning

  drive's improved convergence

- Rats-nets grouped in bundle bus

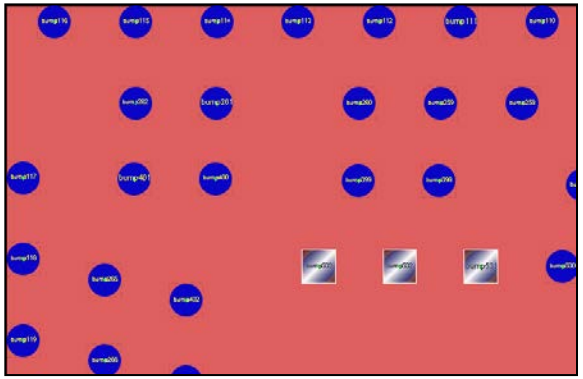
- Bundle flow guided routing path

- Auto-Interactive routing in manufacturing quality data.
  - Break out
  - Truck route
  - Delay tune
  - Phase tune

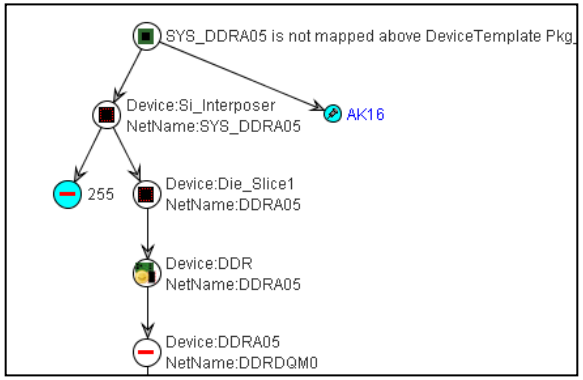


Capabilities …

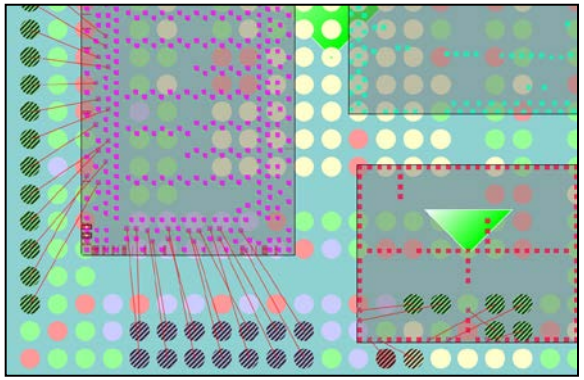
IO Pad Ring Construction



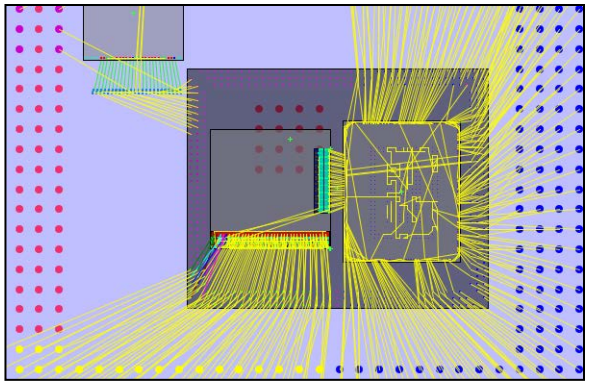
Bump Pattern Development



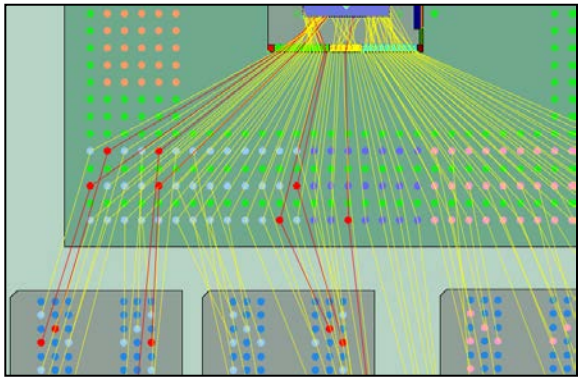
Net Management



Multi-Die Support



2.5D & 3D Planning



System Connection Planning

Single Canvas Optimization of Chip-Interposer-Package-Board

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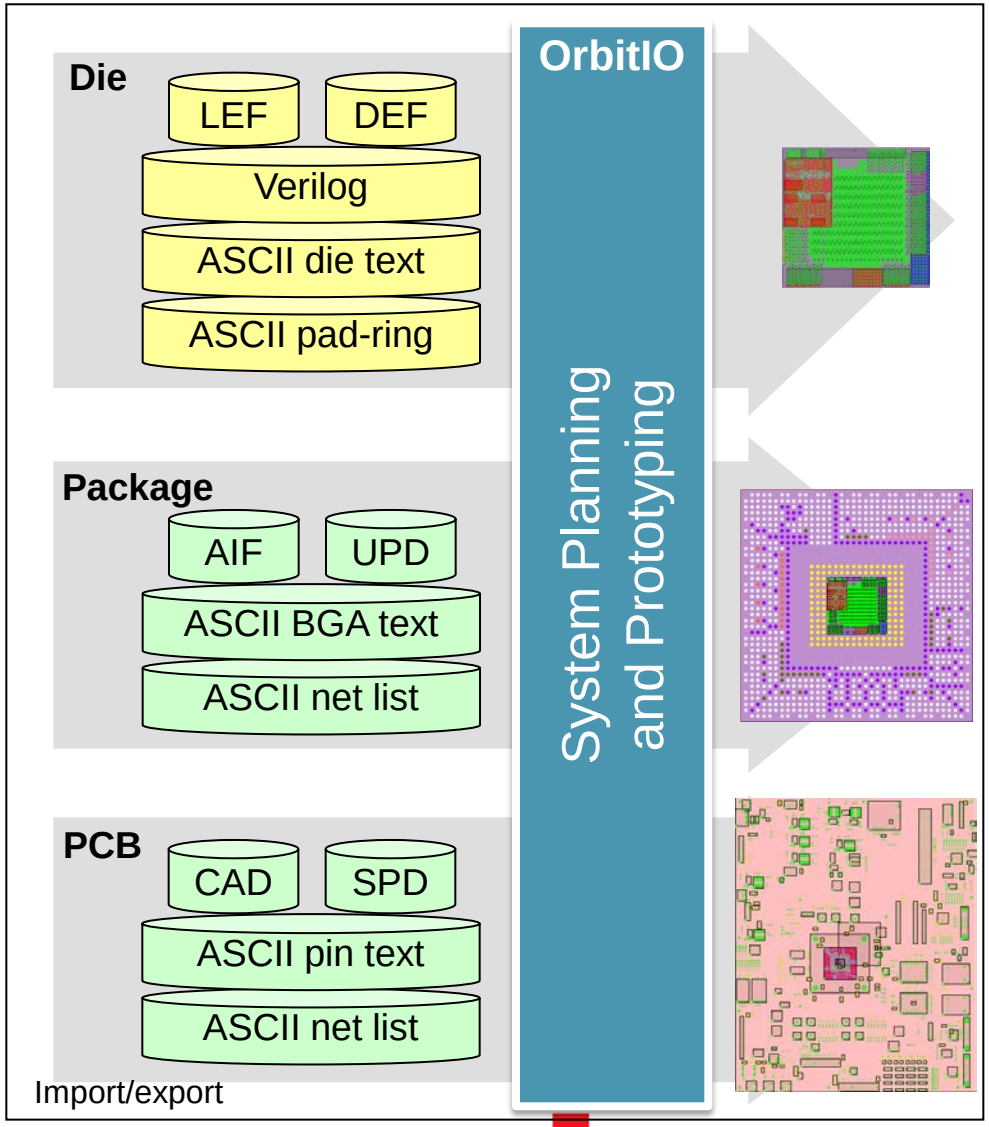
Integrate With Existing Flows and Methodologies

Silicon, package, and PCB support using standard and generic formats

- Partial or complete data
- Merge & compare DEF

Highly flexible scripting with a robust API

- Multiple scripting options with open API
- Platform for third-party or custom applications



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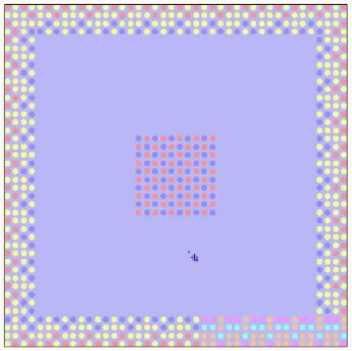
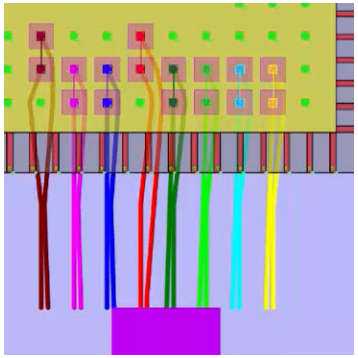
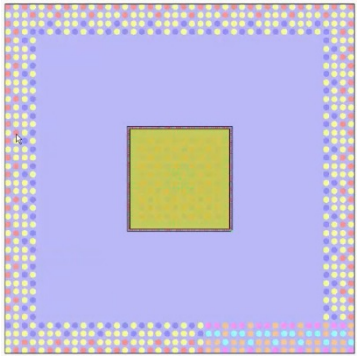
IC-driven Ball Map Creation Flow



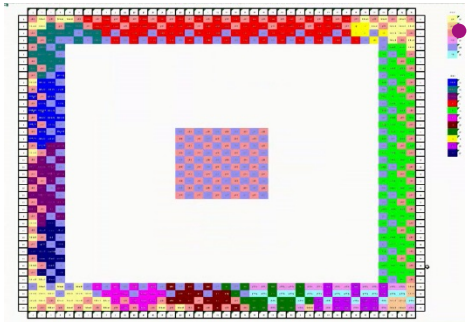
- Import BGA



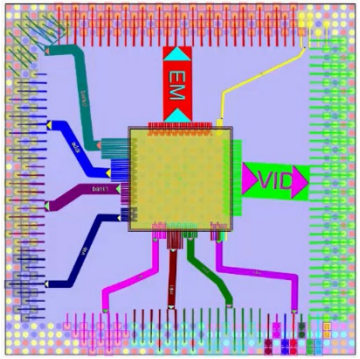
- Die breakout feasibility routes
- Optimize BGA pins



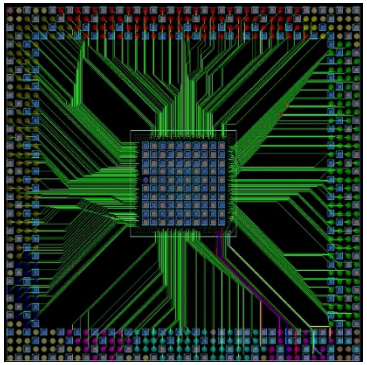
- Load die abstract
- Identify diff pairs



- Export BGA ball map



- Create interfaces
- Bundle from die to BGA
- Creates initial BGA pin-out



- Import design to SiP Layout
- Die breakout routing
- Auto package routing

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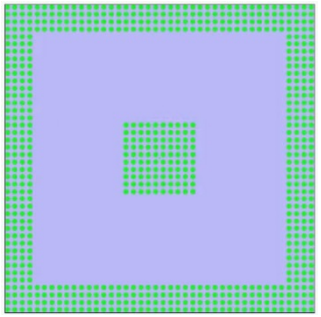
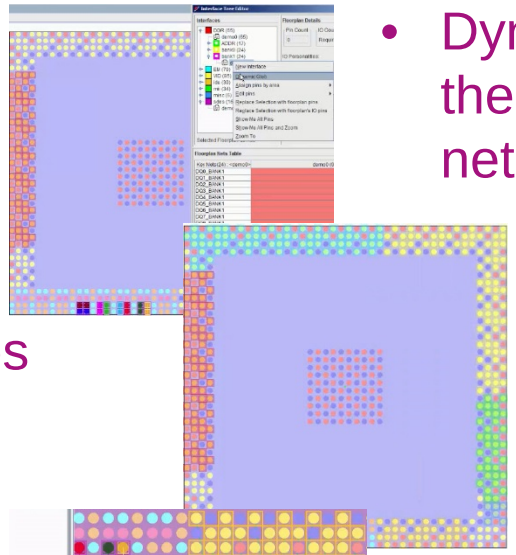
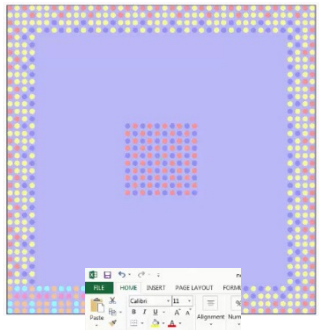
Standalone BGA Ball Map Creation Flow



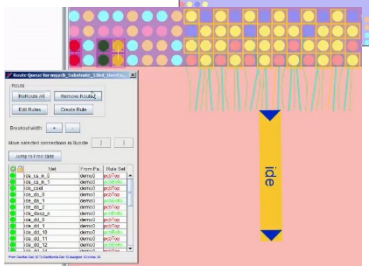
- Import BGA



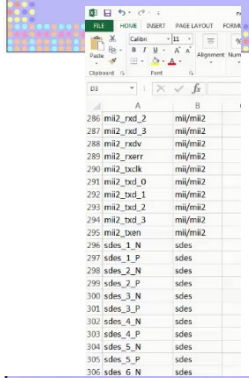
- Dynamically map the interfaces and nets to the BGA



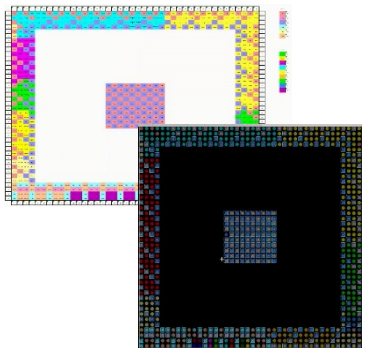
- Define personalities
- Create pattern of personalities



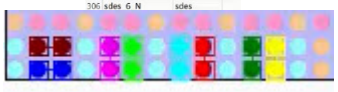
- Breakout die to temp PCB substrate



- Import nets and interfaces



- Create Excel ball map



- Identify and assign diff pairs

- Import to SiP Layout

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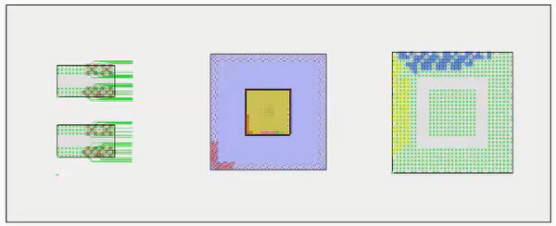
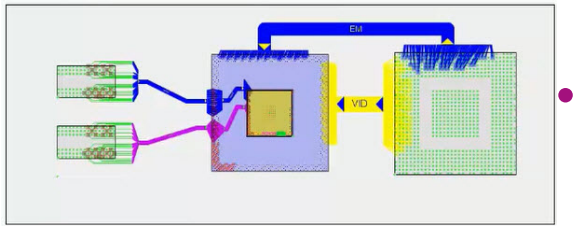
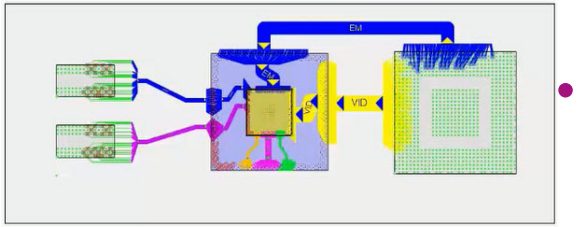
Multi-substrate BGA ball map optimization Flow



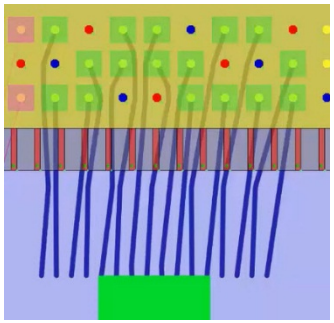
- Import .PCB file
- Create BGA
- Import die abstract
- Create interfaces



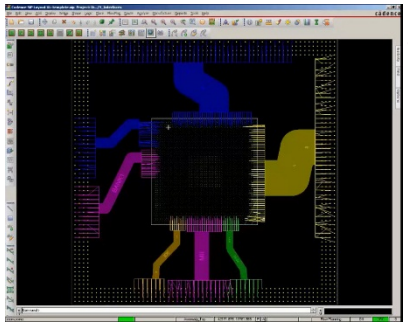
- Create bundles from PCB to die



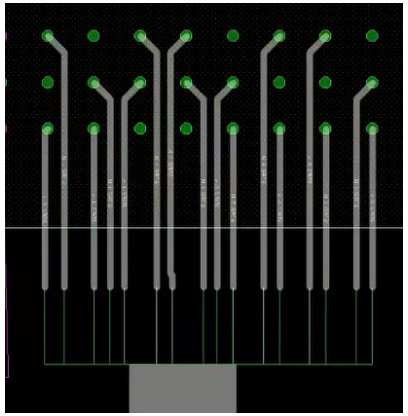
- Create bundles from die to BGA



- Do die and package breakout feasibility routing
- Do BGA pin optimization



- Import OrbitIO file into SiP Layout



- Do die breakout feasibility

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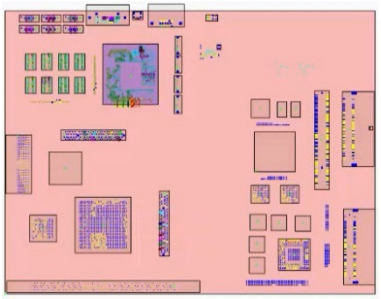
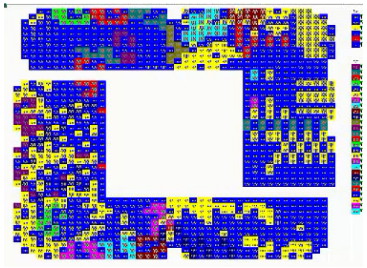
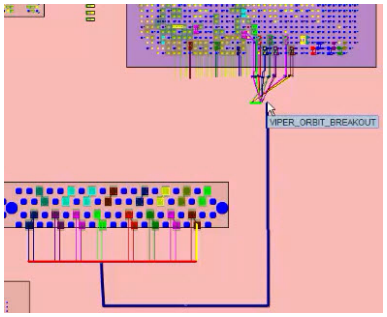
PCB-driven Ball Map Optimization Flow



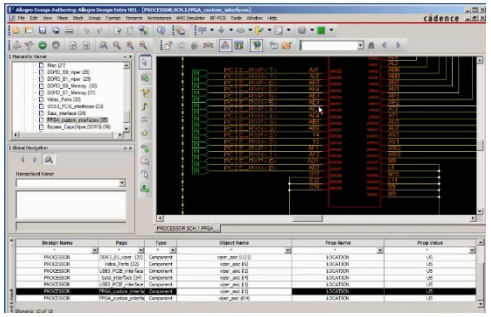
- Import Allegro PCB file
- Export nets and add interface definitions



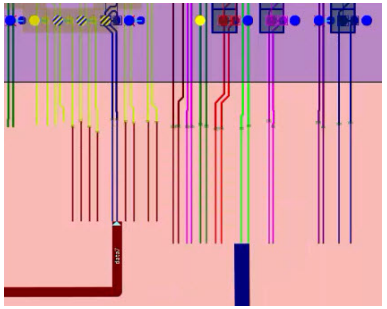
- Generate Excel ball map



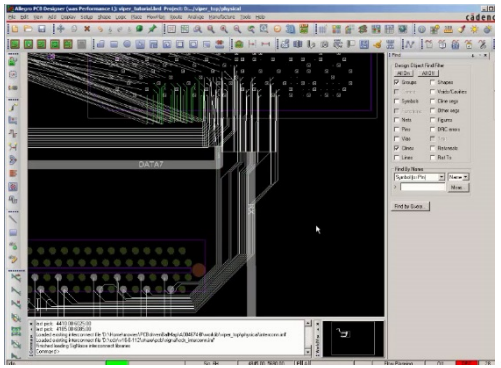
- Create bundles from PCB to BGA



- Export BGA changes to DE-HDL (schematic)



- Optimize pin assign-ments to existing breakouts from the BGA



- Update PCB with logical and physical changes
- Route optimized design

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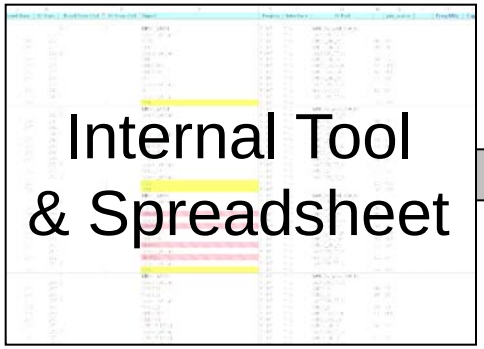
Case Study: Current Pad Ring Design Process

2 Months With Approximately 50 Iterations to Design the Pad Ring

Manual Entry of Logic & Physical Data

Product Engineer

- Pad types / Pin names
- JTAG/DFT information
- Pad control signal assignments
- Padring P/G types
- Utility cells
- IO pad locations
- Bond Pad / Bump locations
- Package nets



Consultation & Verification

Library Engineer

Layout Engineer

Substrate Engineer

- 400K+ cells to manually manage!
- Changes are error-prone and time-consuming
  - Not a simple insert – has ripple effect
- No rule checking
  - Errors undetected until LVS or simulation
- Relies on high-value IC tools for visualization
- Setting pad modes require intimate knowledge of specifications

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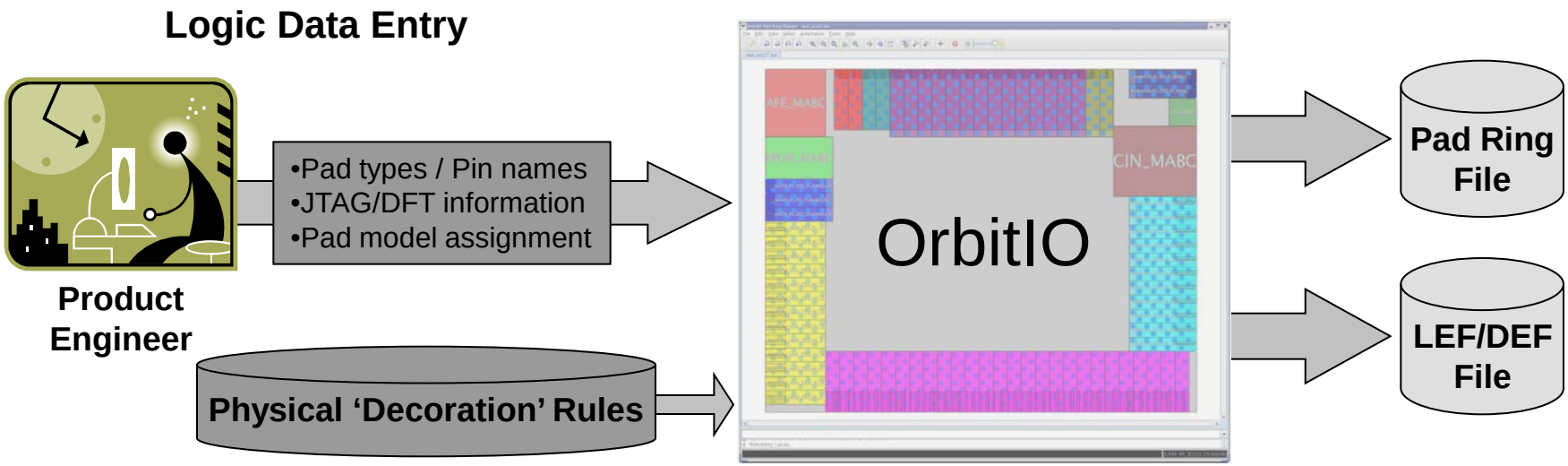
Case Study: OrbitIO Pad Ring Design Process

Significant Cycle-Time Reduction



- Product Engineer focuses on logic
- Minimizes involvement of specialty engineers on per design basis
- Direction captured as design rules

- Changes in seconds, not hours/days
- Eliminate errors - rules driven design
- Immediate visualization
- Automatic management of pad modes

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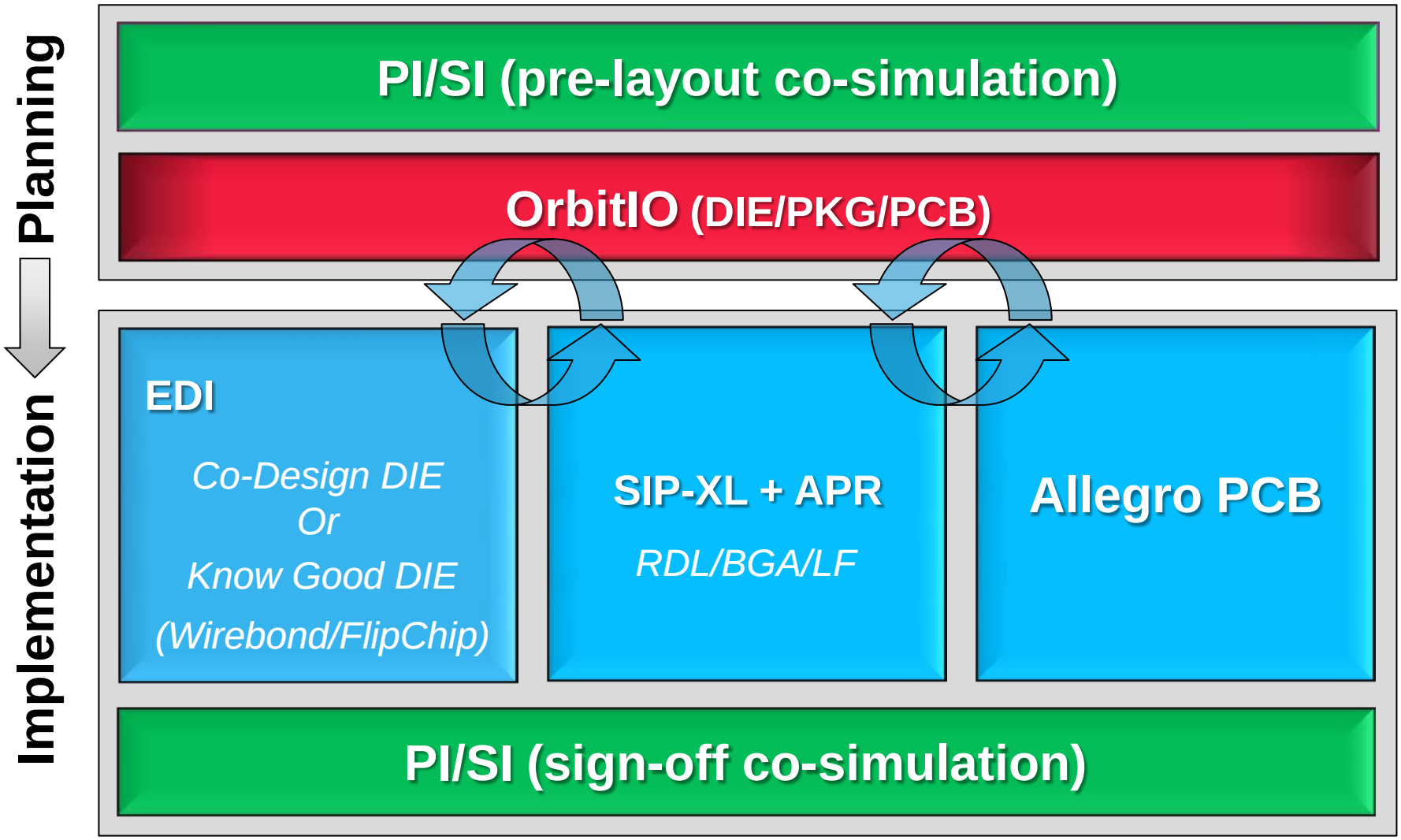
Chip-PKG-PCB Co-Design Platform



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Summary

- Cross-platforms and Multi-fabrics Co-Design solution
- Global view for cost and performance optimization
- Data exchange with standard format
- Central netlist management
- Reduce design iteration and cycle time


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