Taipei 10.16 2015 User Conference Graser

Cadence Transistor-Level EMIR Solution

Voltus-Fi Custom Power Integrity Solution

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Agenda

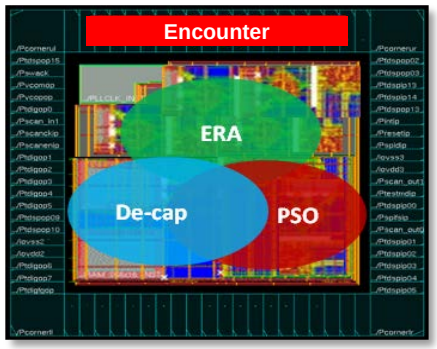
- Introduction -- Cadence Power Signoff Solution
- Transistor-Level EMIR Challenges and Cadence Advantages
- Visualization, Analysis & Debug
- Summary

Introduction –
Cadence Power Signoff Solution

Voltus – Fast Design Closure

Complete Design Flow from Chip to System

- Tight Integration with IC Physical Implementation
  - Early rail analysis & ECO: during power planning stages
  - De-cap & ECO: IR-drop and leakage reduction
  - Power gate switching & ECO: rush current, turn-on time



Tempus
APS
Virtuoso
Palladium

Signoff Ecosystem

- Chip-package-PCB Co-Simulation and Analysis
  - Accurate power grid networks for chip and board
  - Electrical-Thermal analysis
  - 3DIC support, including CoWoS (2.5D)

Voltus IC Power Integrity Solution

- Breakthrough massively parallel execution technology in SoC power signoff
- Up to 10X faster performance gain over existing solutions
- Capacity up to 1 billion instances with hierarchical analysis capability
- Integrated with key Cadence® technology for fast design signoff and closure
- Certified for TSMC 10nm FinFET+ process

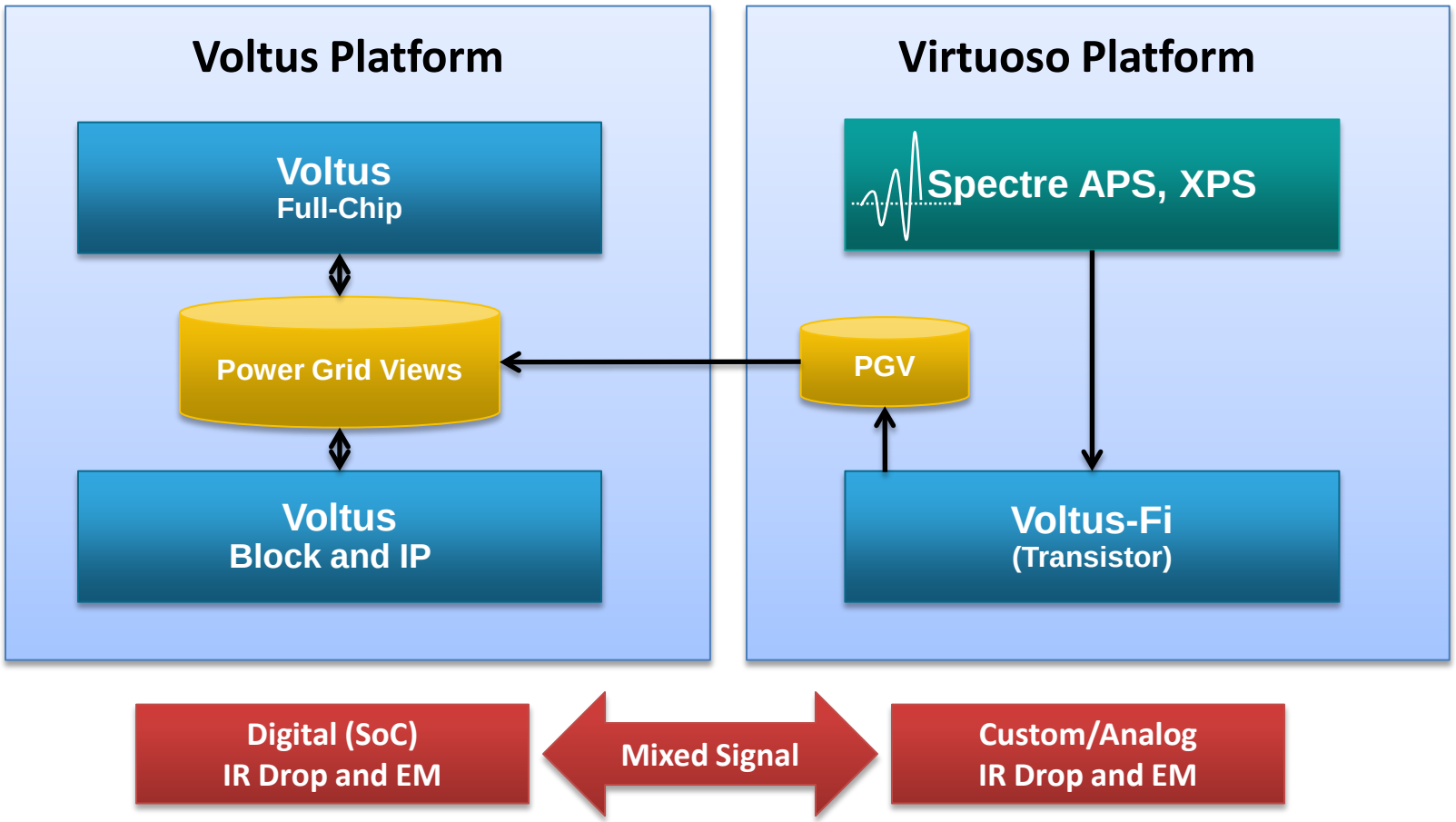
Performance, accuracy, and design closure

Voltus-Fi Custom Power Integrity Solution

- Complete Cadence® IC power signoff platform in “Voltus™ + Voltus-Fi”
- TSMC 10nmFF+ certified, SPICE-accurate transistor-level power signoff
- Industry’s only fully integrated solution in Virtuoso® platform for superior ease-of-use
- Seamless flow in Voltus-Fi to Voltus for accurate full-chip level SoC power signoff
- Tight integration with Cadence’s tools for accuracy, performance, and fast design closure

Fastest path to accurate analog/mixed-signal power signoff

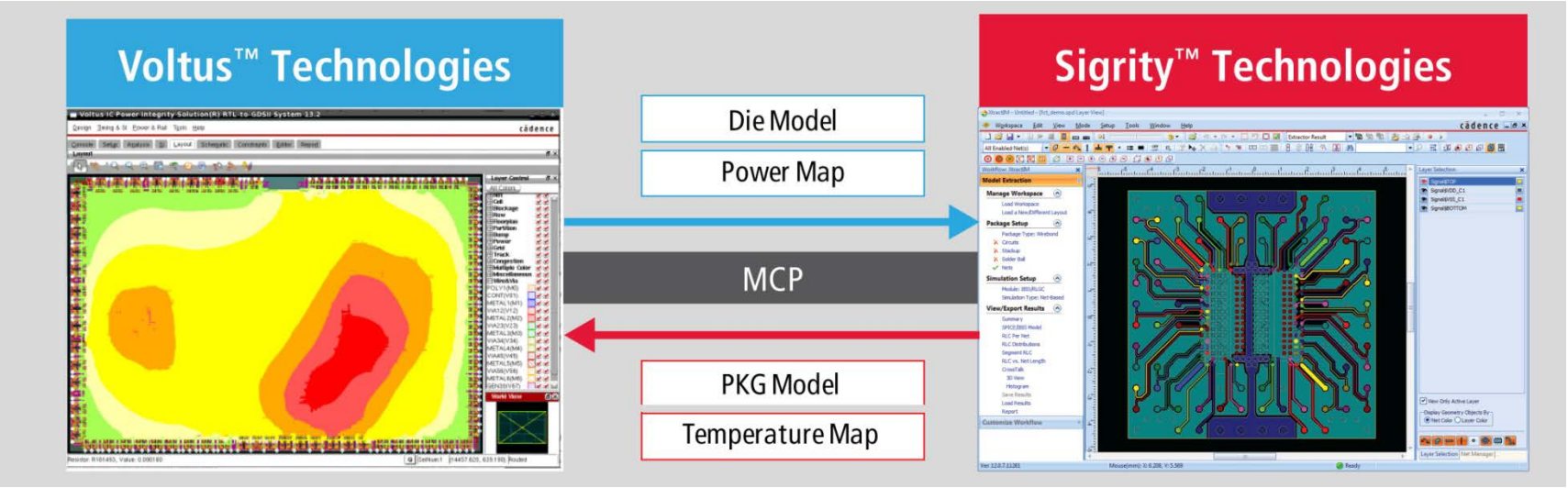
Voltus-Fi Custom Power Integrity Solution



Accurate Transistor EMIR Analysis, High-quality Analog IP Grid Modeling

Voltus and Sigrity Chip-PKG-PCB Co-Analysis

- Accurate Power Signoff for Highly Coupled Power Delivery Network

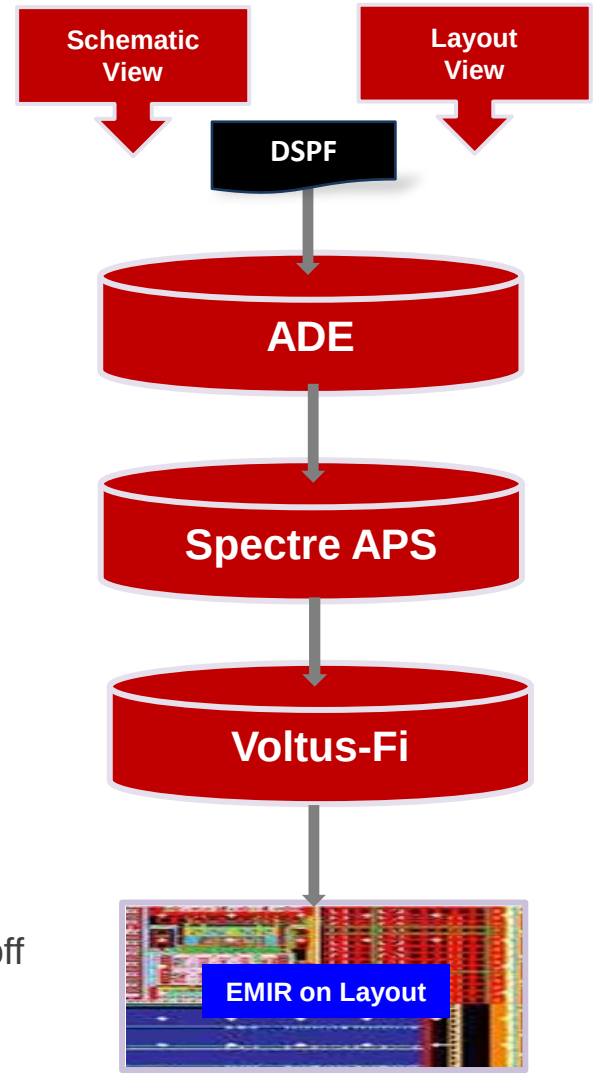


  - Die-model and PKG / PCB-model in broadband SPICE format for “Voltus™ + Sigrity™” co-analysis
  - Power map / temperature map for electro-thermal co-analysis
  - Comprehensive power and signal integrity analysis including IO-SSO

Competitive Advantages

- Cadence Offers a Complete Solution
  - Layout and parasitic Extraction
  - Transistor level EMIR Simulation
  - EMIR Visualization, analysis, debug and fix
  - An Integrated flow for high QoR
- Proprietary Technology in MMSIM Spectre APS|XPS EMIR Algorithm
  - Patented voltage-based “iterated” method in power network RC solving
- Comprehensive EMIR Result Analysis Capability in Voltus-Fi Flow
  - Foundry certification
    - Quantus QRC: extraction accuracy
    - APS: simulation accuracy
    - Voltus-Fi: EM rules and IR-drop accuracy
  - Integration with Virtuoso from ADE to VLS for greater design productivity
  - PGV generation for full-chip level SoC Voltus power signoff

Cadence Voltus-Fi EMIR Flow

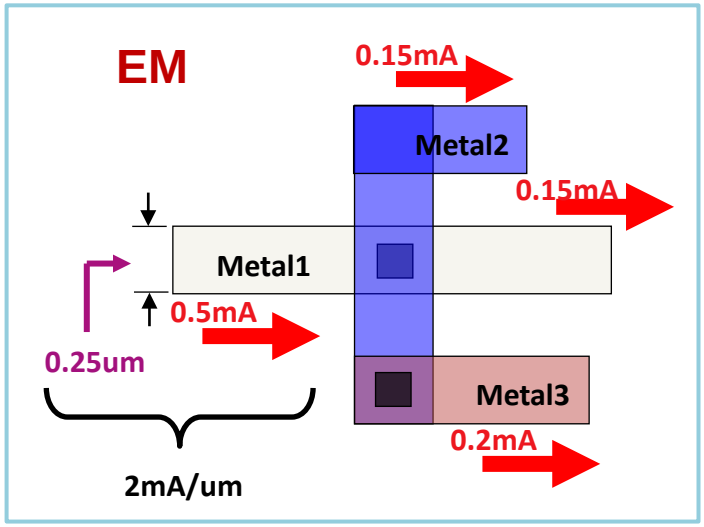


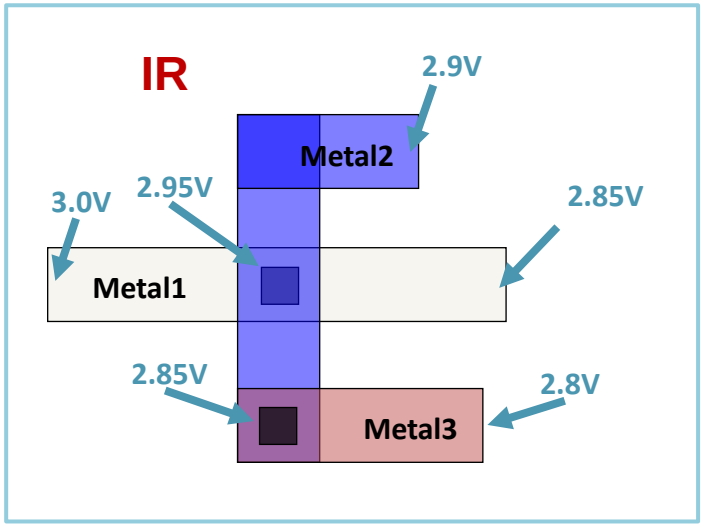
Transistor-level Electro-Migration & IR-Drop

Challenges and Cadence Advantages

Transistor-Level EMIR Analysis

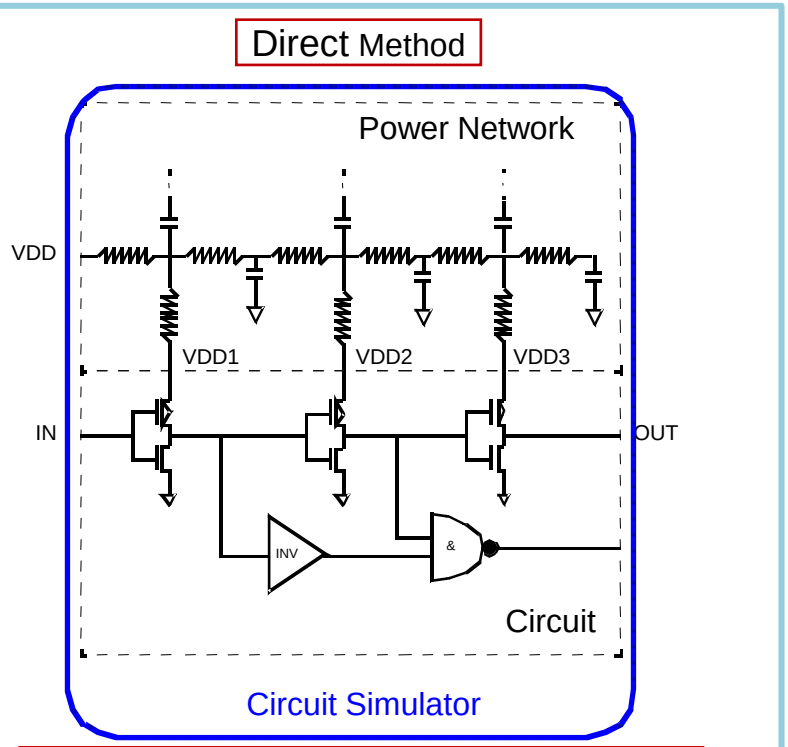
- EM Analysis
  - High density current in a narrow metal wire may destroy the wire by electron migration
  - An EM analysis solution calculates current and compares to EM rules on each wire
  - Advanced nodes, especially on FinFET, have very complex EM rules such as wire length, width, current direction dependency
- IR Analysis
  - Voltage drop along the metal wire may cause signal integrity issue or even functional failure
  - An IR analysis solution calculates voltage and ensures its sufficiency to meet specification
- Unique Challenges in Tx-level EMIR
  - Simulation on large RC network from post-layout for “current” is very expensive
  - Ease-of-Use for quick analysis, debug and fix on a familiar design GUI platform
  - Unified power signoff: “cell + trx” for full-chip SoC



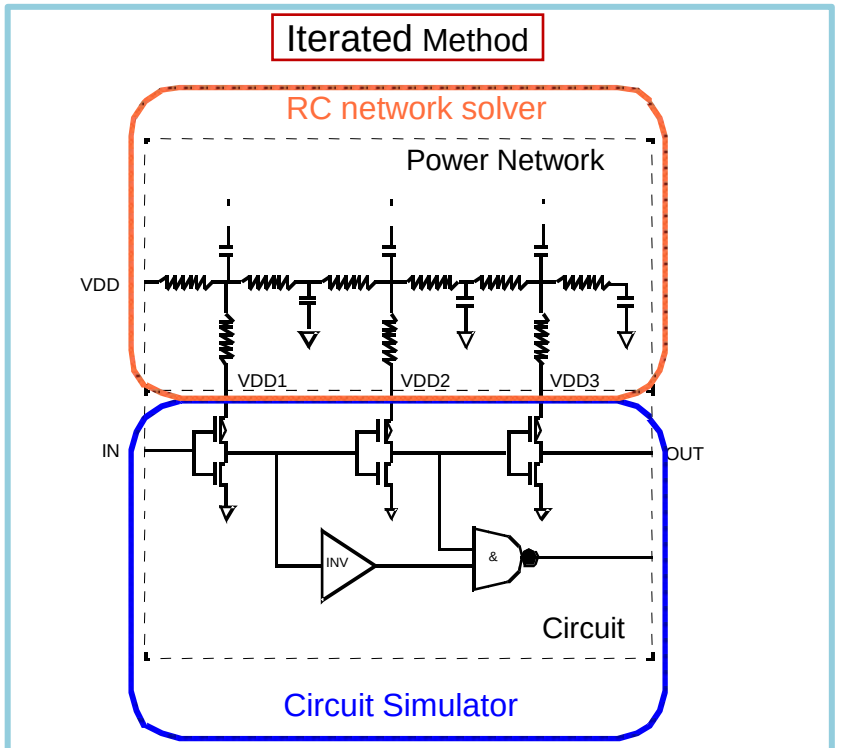


Solving Power Network RC Matrix

- Direct and Iterated Method



- Power RC network and circuit devices in one single simulation
- SPICE-level accuracy with limited capacity and performance
- Best for analog IPs



- 2-staged solution on power RC network and circuit devices
- High capacity and performance with sufficient accuracy
- Best for custom macros, memories

Benchmark Examples

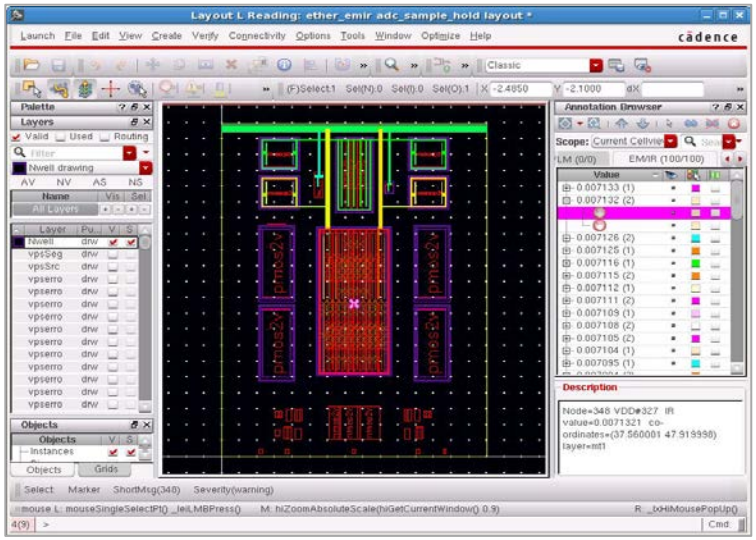
- Power Net EMIR and Signal EM Analysis

Statics		16Kx32-byte-data (90nm)	32K-SRAM (20nm)
Circuit Inventory	MOS	3,226K	~2,000K
	Diode	297	210
	R	25,240K	120M
	C	16,427K	85M
	Nodes	1,072K	605K
Transient Time		5ns	16ns
Simulator		APS	APS
Total Runtime		**4h10m**	**7h36m**
Peak Memory		**97GB**	**120G**

Visualization, Analysis & Debug

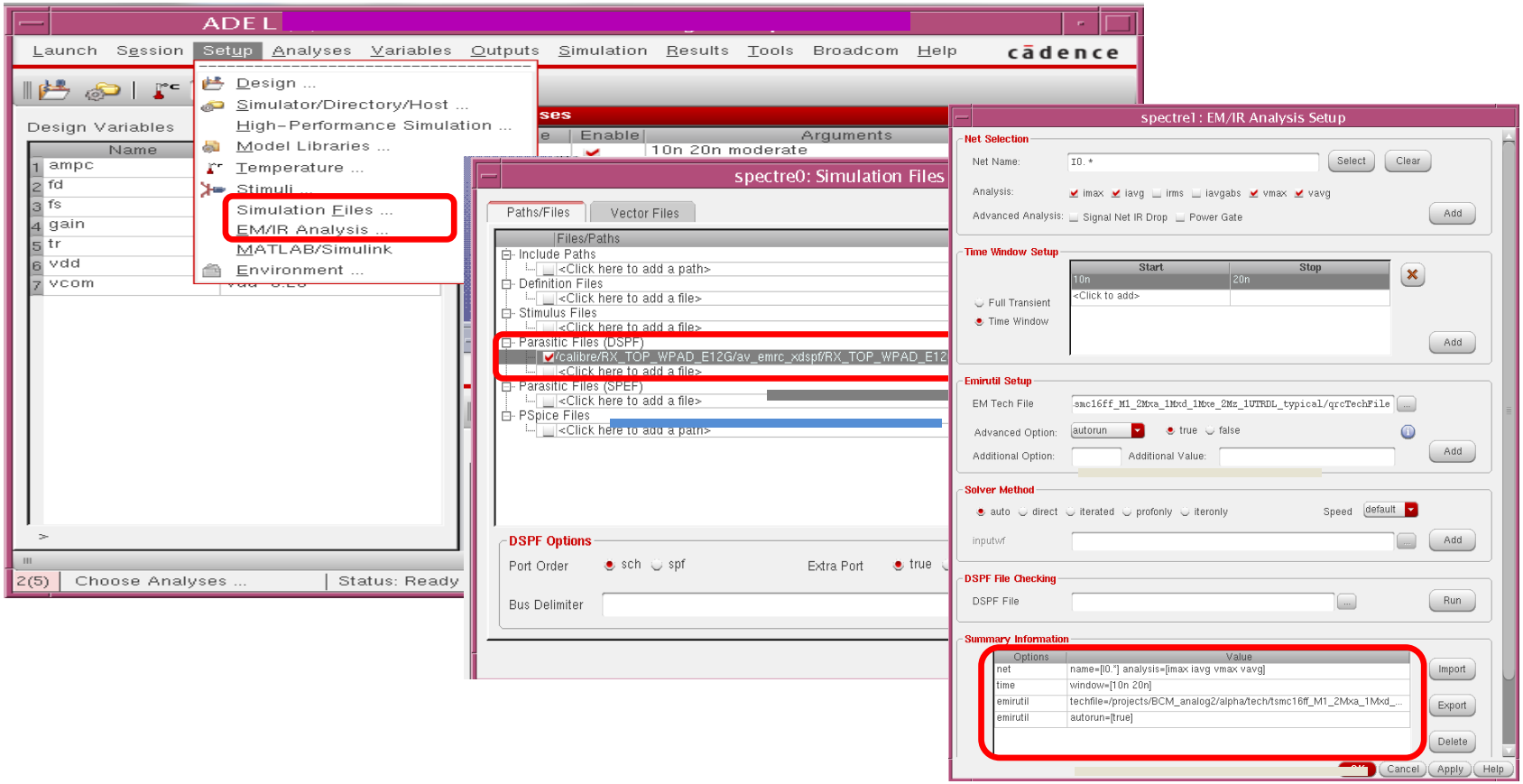
Design Input Data Requirements

- Design Data
  - xDSPF of the design
    - Decoupled RC extracted for all nets, including PG nets
    - With physical information for layers
  - Testbench schematic or netlist
  - DFII schematic for Virtuoso® Analog Design Environment based simulation
  - DFII layout for results visualization and structural checks or GDSII of the design with layer map to pipe it in Virtuoso platform
- Technology Data
  - SPICE models and corners
  - DFII technology library
  - ICT file or qrcTechFile with EM models



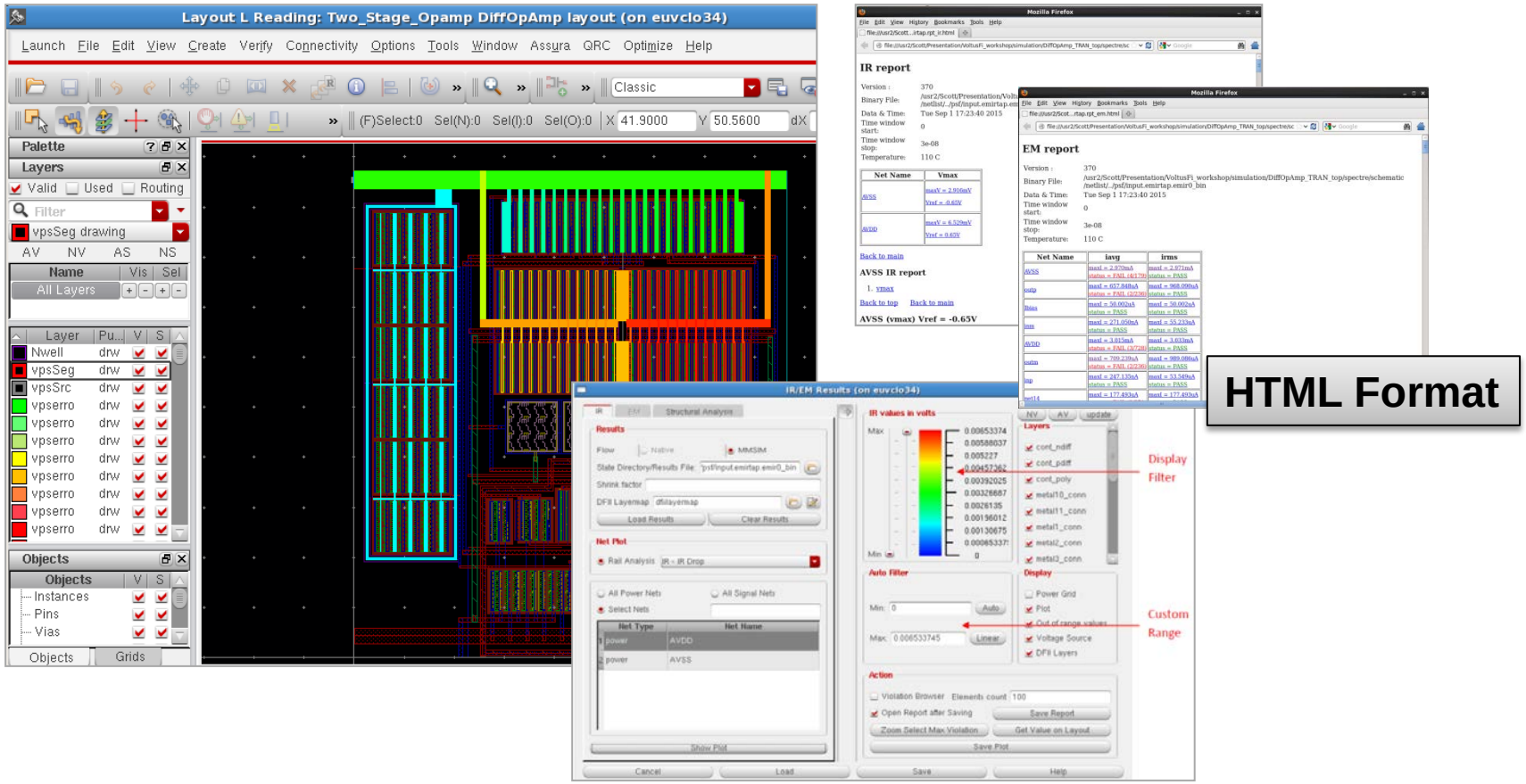
Setting Up Virtuoso-ADE for EMIR

- Loading DSPF Netlist
- Specifying EMIR Analysis Options



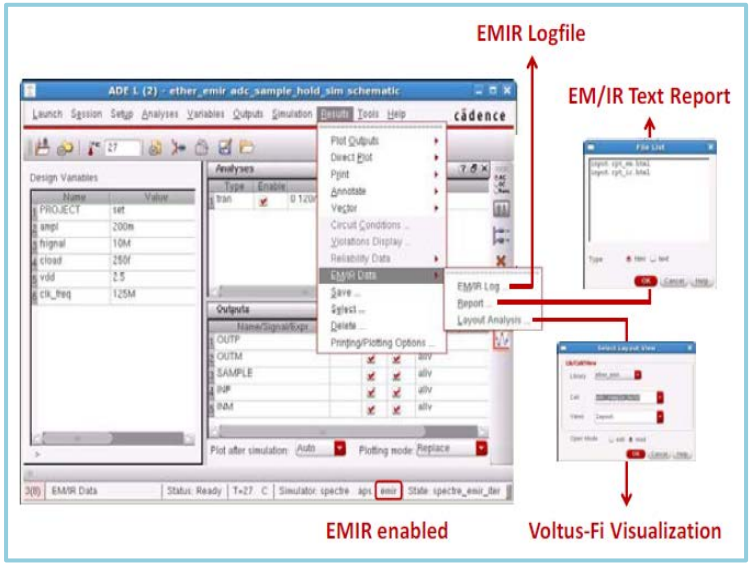
EMIR Result Analysis in Voltus-Fi

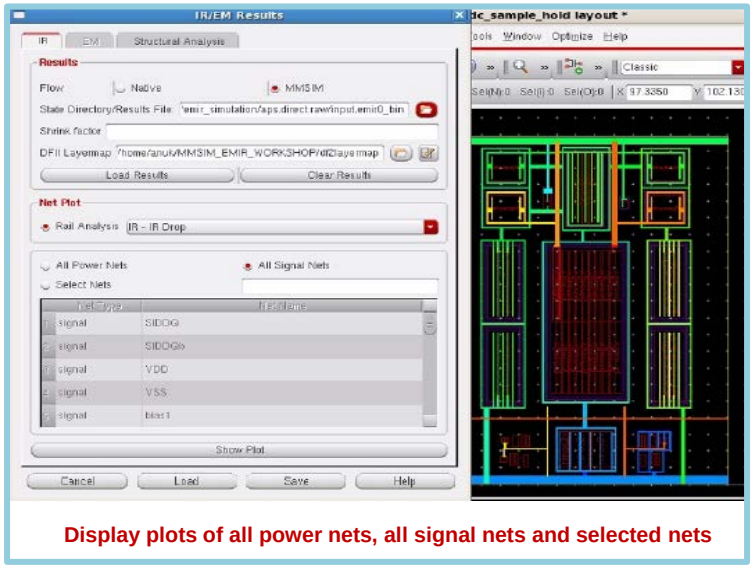
- Launching Voltus-Fi from Virtuoso Layout View
- Enabling Violations Browser for IR Violations and EM Violation
- Cross-probing between Graphic Display and Simulation Text Report



Voltus-Fi Visualization

- Usability and Integration
  - Fully integrated with ADE simulation environment and Virtuoso Layout Editor
  - Plots are overlaid real time over the layout
  - Continuous 100 color filter to improve usability
  - Leverages existing Annotation Browser as Violation Browser
  - Querying the worst violation and worst violation in an area
- Varied EMIR Plots & Detailed EMIR Reports
  - Signal net IR-drop plot
  - Power gating switch analysis plots
- Structural Analysis
  - Early detection of certain EMIR root cause
- Transistor-level Block's PGV Generation
  - For Voltus top-level power signoff analysis

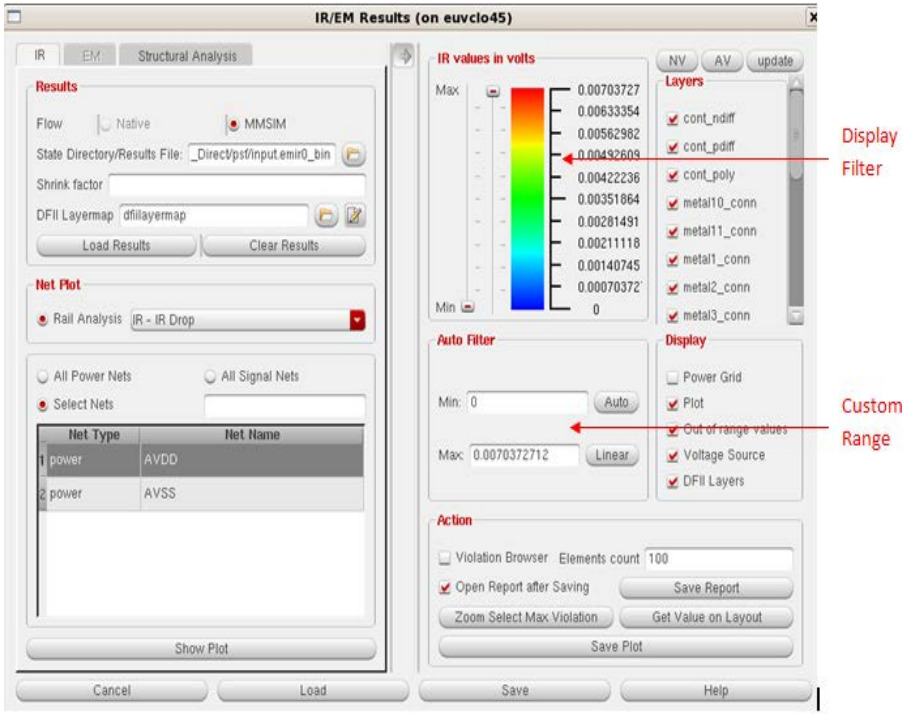




Display plots of all power nets, all signal nets and selected nets

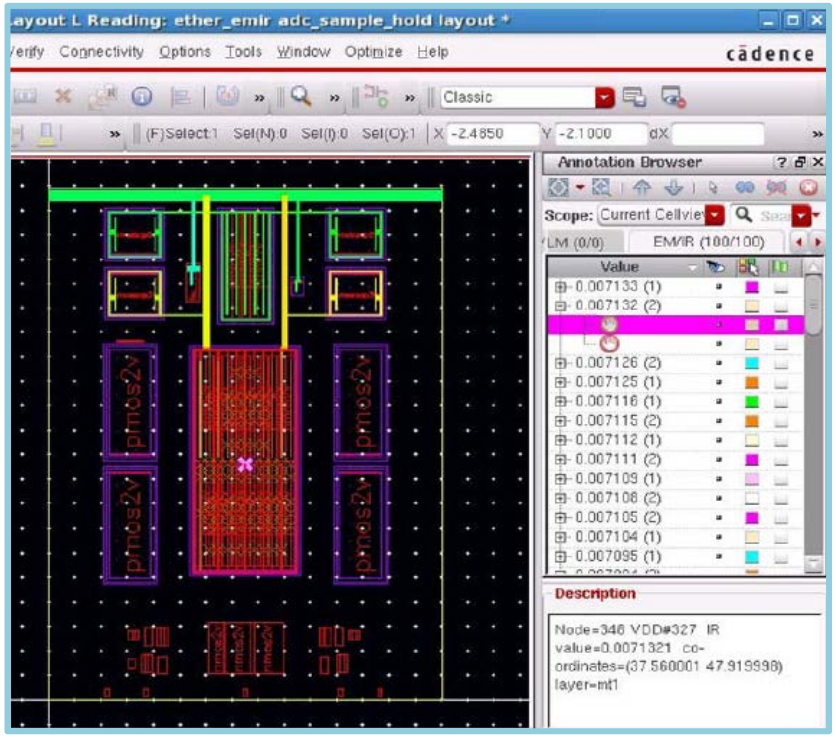
Ease-of-Setup and Rich Features

- The Continuous Filter has Sliders to change the Ranges
- Filters can be set from Fields as well
- The Display of the following can be easily toggled
  - DFII layers
  - Plots
  - Voltage sources
  - Out of range values
- User can also select the worst value in an area
- Layer Specific Results can also be displayed



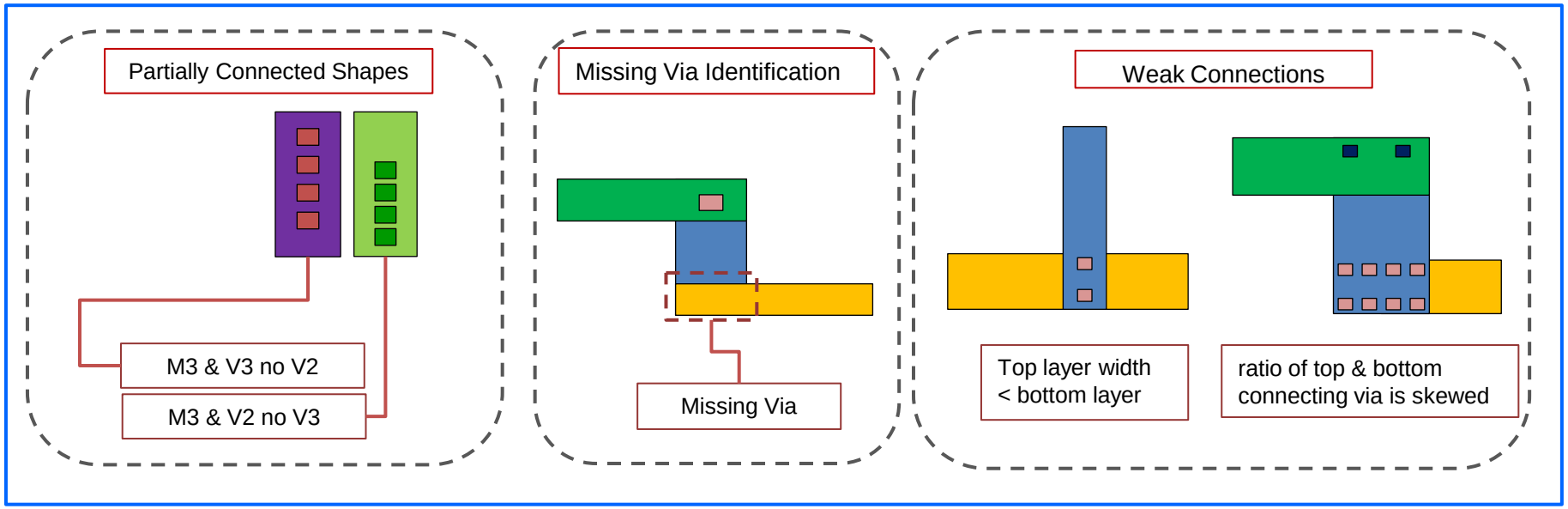
Violation Browser

- Violation Browser, by default, lists Top 100 Violations
- User can use Browser to zoom into the selected Violation
- It is, by default, docked inside the Virtuoso Main Window but can be undocked as well
- It has all the features in Annotation Browser



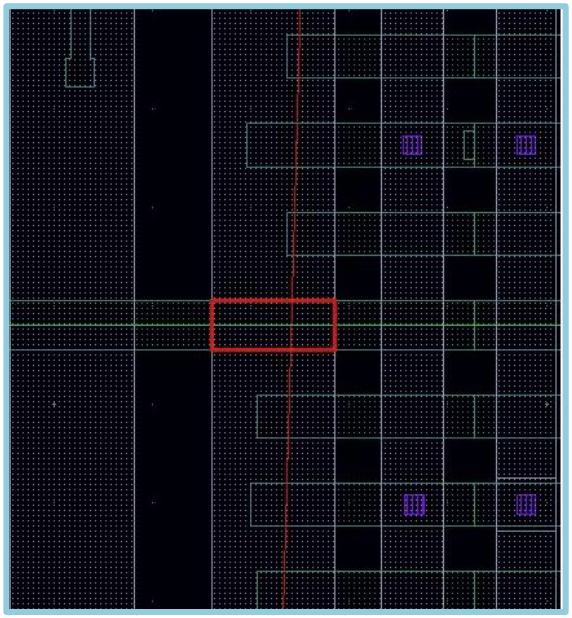
Shape-Based Geometrical Analysis

- To Quickly Identify Power Grid Weakness Through Voltus-Fi Visualization
- Structural Checks on Power Grid Nets
  - Partially connected or unconnected shapes in layout patterns
    - Top VIA missing, Bottom VIA missing
  - Overlapping layers
    - Missing VIA connections, VIA coverage ratio
  - Weakly connected shapes
    - Skewed VIA ratio

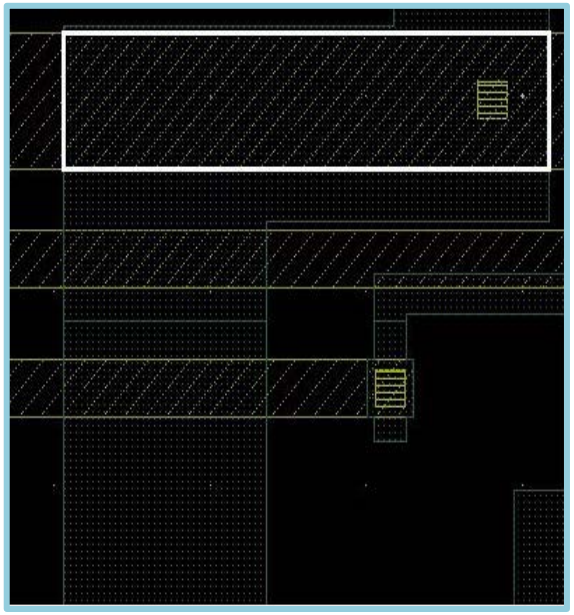


Structural Analysis

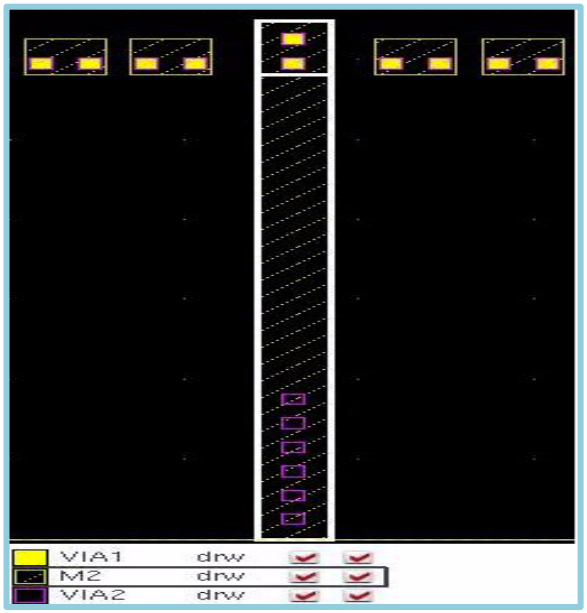
- Example



Missing VIA

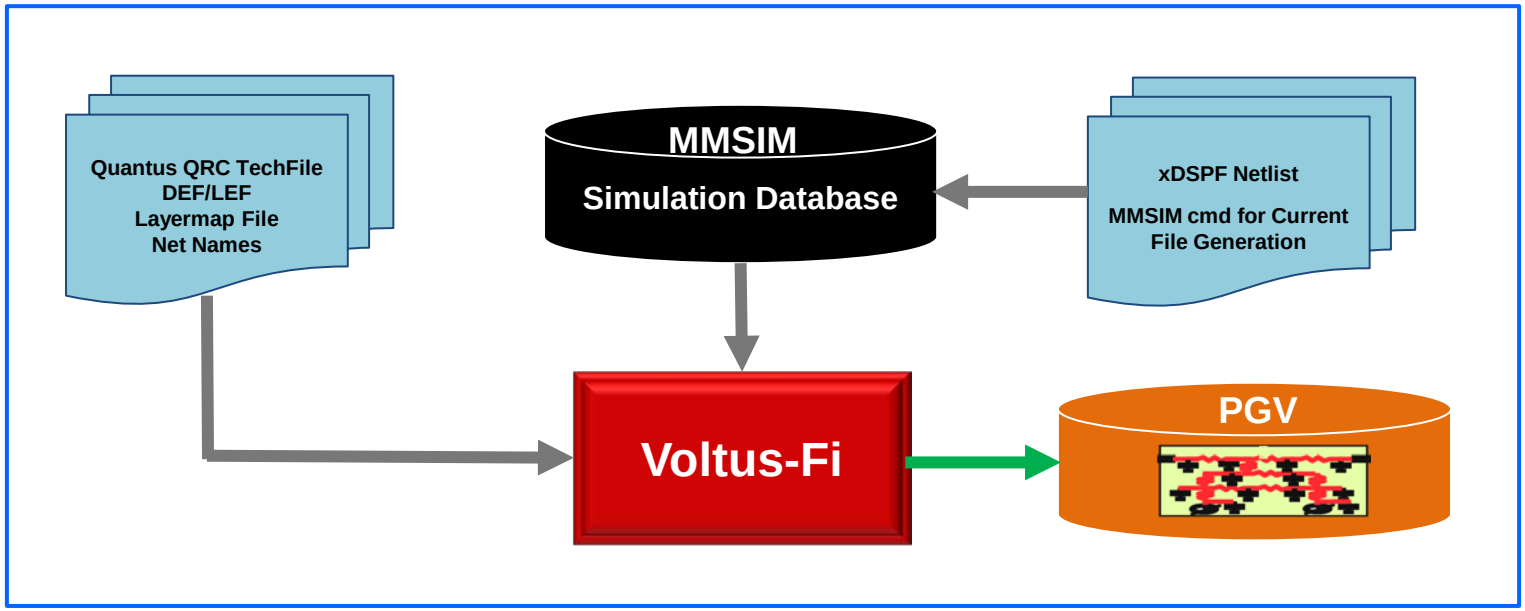


Via Coverage Ratio



Skewed VIA Ratio

Voltus-Fi on PGV Generation



- A Power-Grid-View (PGV) is a Binary Model for an IP's Grid Characteristic
  - Geometric views, port information
  - MMSIM setup for the current characterization of Power & Ground nets
  - Multi-mode feature in capturing various operational modes of an IP block
- An IP's PGV Should be Generated if a Significant Large P|G Nets are Shared Between Transistor-block and Cell-digital (Voltus)
  - Voltus top-level, full-chip power signoff

Summary

Summary

- Voltus is a complete solution in power integrity analysis and signoff
  - Voltus-Fi Custom Power Integrity Solution: Transistor-level power signoff
  - Voltus IC Power Integrity Solution: Cell-level SoC power signoff

- Voltus-Fi solution provides the most accurate transistor-level solution that is fully integrated in the Virtuoso platform
  - Performance and accuracy by Spectre APS/XPS
  - Visualization, debugging, and fixing in Virtuoso platform

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Thanks