Taipei 10.16 2015 User Conference Graser

# 2.5 / 3D Design Solution

*Scott / Graser*

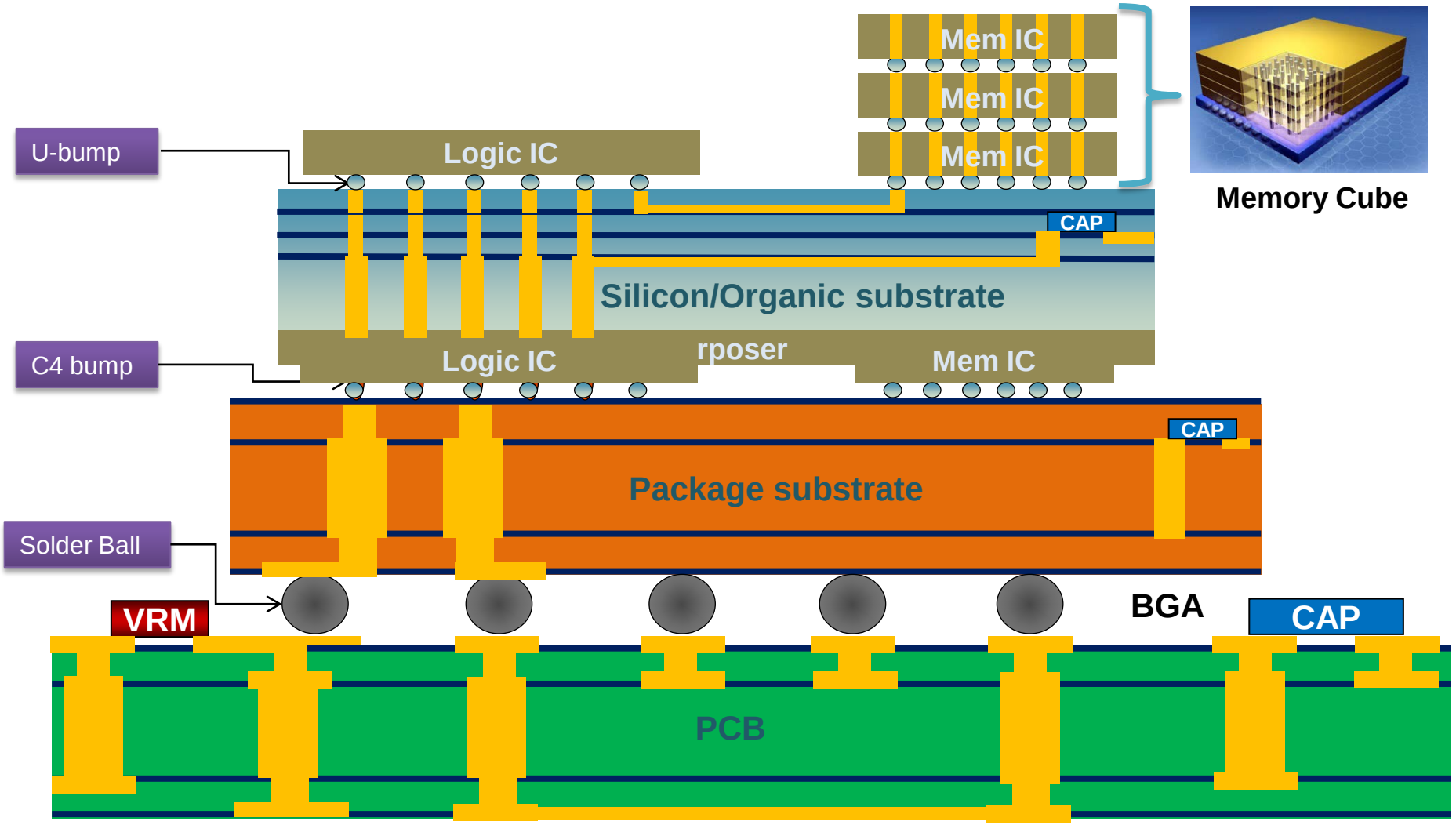
*16 / Oct / 2015*

# Agenda

- Introduction - 2.5 / 3D Design Overview
- Cadence Virtuoso Custom 3D - IC Design Solution
- Summary

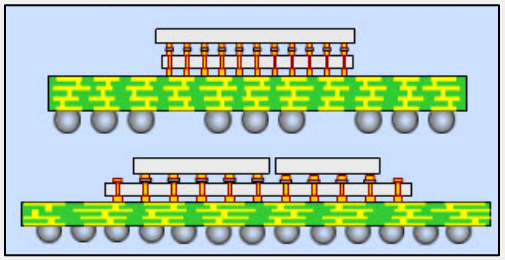
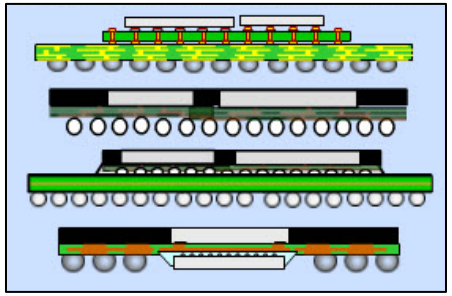
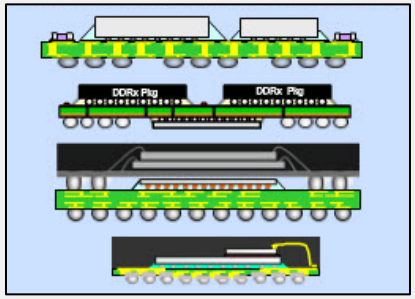
# Introduction –
# 2.5 / 3D Design Overview

# 2.5 / 3D Design Overview

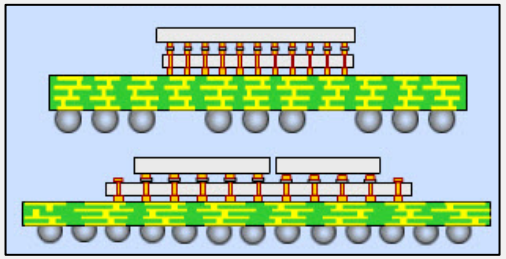
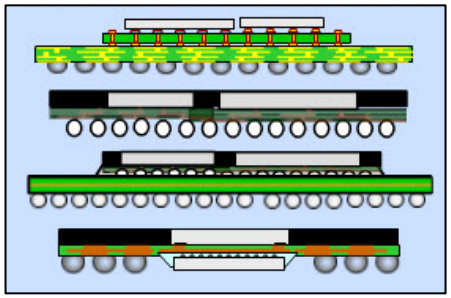
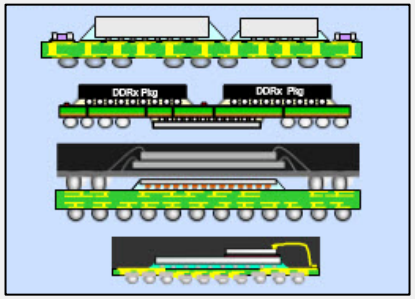



Courtesy of TSMC

# Multiple Pathways to 2.5 / 3D Integration

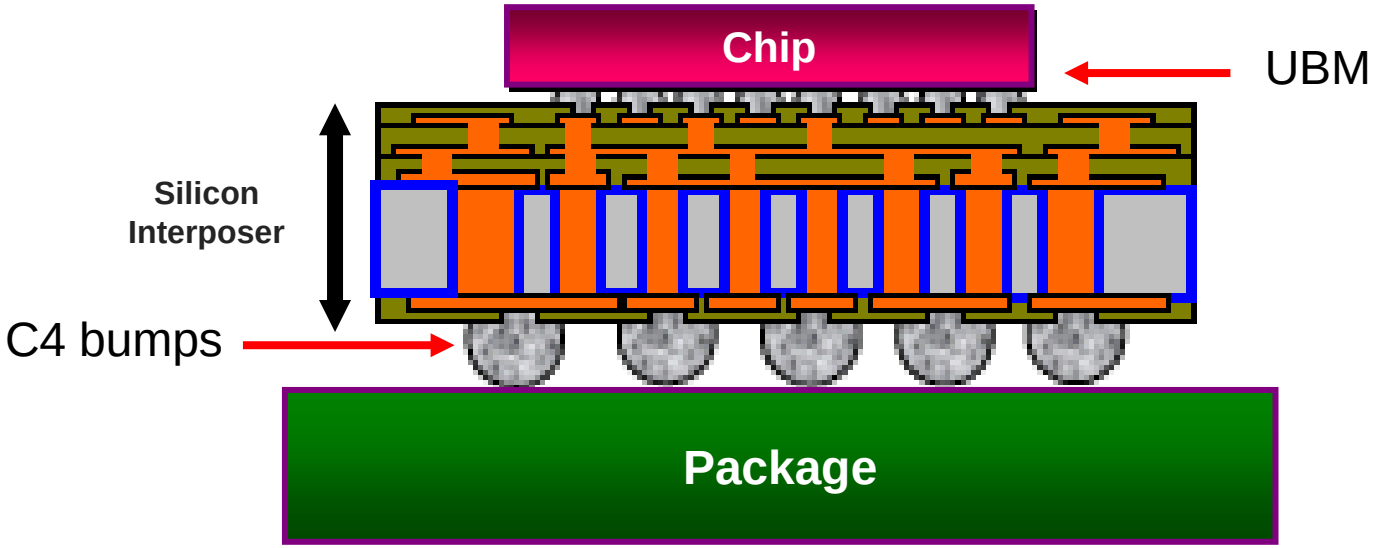
| Packaging Platform | Examples | Drivers / Applications |
|---|---|---|
| Silicon based interposers<br>Die stacking with TSV |  | Silicon partitioning<br>CPU / GPU – memory I / F<br>High-end computing<br>High-end networking<br>Memory, FPGAs |
| Fan out wafer level<br>Organic interposers |  | Silicon partitioning<br>Logic / memory integration<br>Mobile convergence<br>AP, BB, modem, PMIC,<br>RF Smart phones & tables |
| Conventional laminate build-up technologies |  | Multi-die integration<br>Logic / memory integration<br>Baseband, analog,<br>RF, passive |

# Advanced Technology Planning & Implementation

| Packaging Platform | Examples | Cadence Solutions | |
|---|---|---|---|
| Silicon based interposers<br>Die stacking with TSV |  | Encounter / Virtuoso / | SIP Layout-XL |
| Fan out wafer level<br>Organic interposers |  | SIP/APD<br>OrbitIO<br>APR | |
| Conventional laminate build-up technologies |  | | |

# Components of 2.5 / 3D – Silicon Interposer

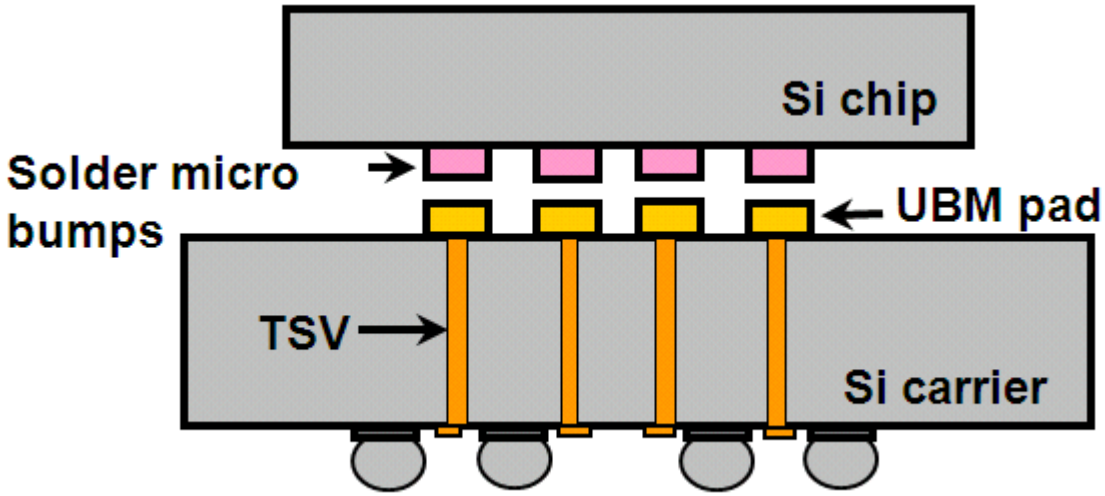
- Silicon interposer: A die made of silicon with vias that connect both sides of die together for signal / power transmission.
- Micro bumps connects multiple die face-down on silicon interposers. The interposer has multi-layer wiring and TSV.
- It provides a higher level of integration together with system performance improvements.

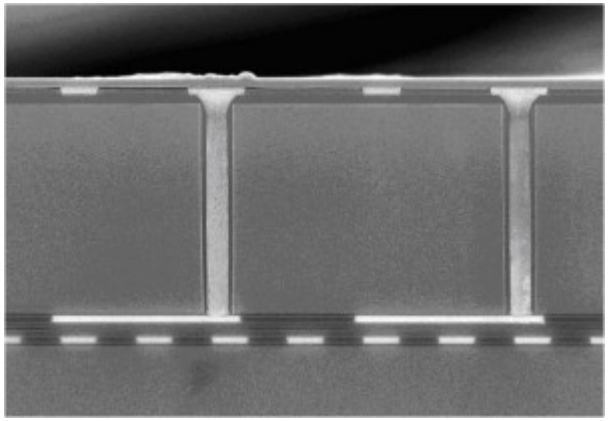



Source: http://semiengineering.com

# Components of 2.5 / 3D – TSV

- TSV can be used with 3D Packages (with Si Interposer) or with 3D ICs (where stacked Si wafer/dies) are connected.
- TSV is etched completely through the silicon substrate, after which it is filled with a conductive material such as copper. After the dielectric and metal patterns have been formed, substrates are thinned to some fraction of their original thickness, then the substrates are bonded together to form one electrical entity.



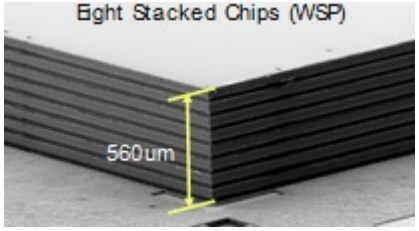



Source: P. Leduc, LETI, D43D, 2010

# Advantages of 2.5 / 3D

## Higher Integration Density

- Integration in horizontal and vertical directions
- Smaller footprint

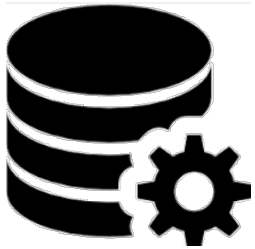



## Shorter Interconnects

- Direct Vertical Communication
  - Shorter Global / Chip-to-Chip interconnects
  - Reduced number of global interconnects
- Less Resistance and Capacitance
  - Less power consumption
  - Higher performance

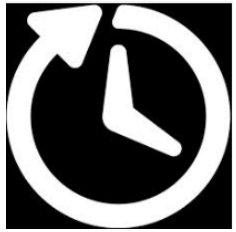
## Heterogeneous Integration

- Exploits the best process technologies for fabrication of different functional blocks
  - No yield compromise
  - Greater functionality



## Short Time to Market

- Can use optimized standard already available products from different vendors

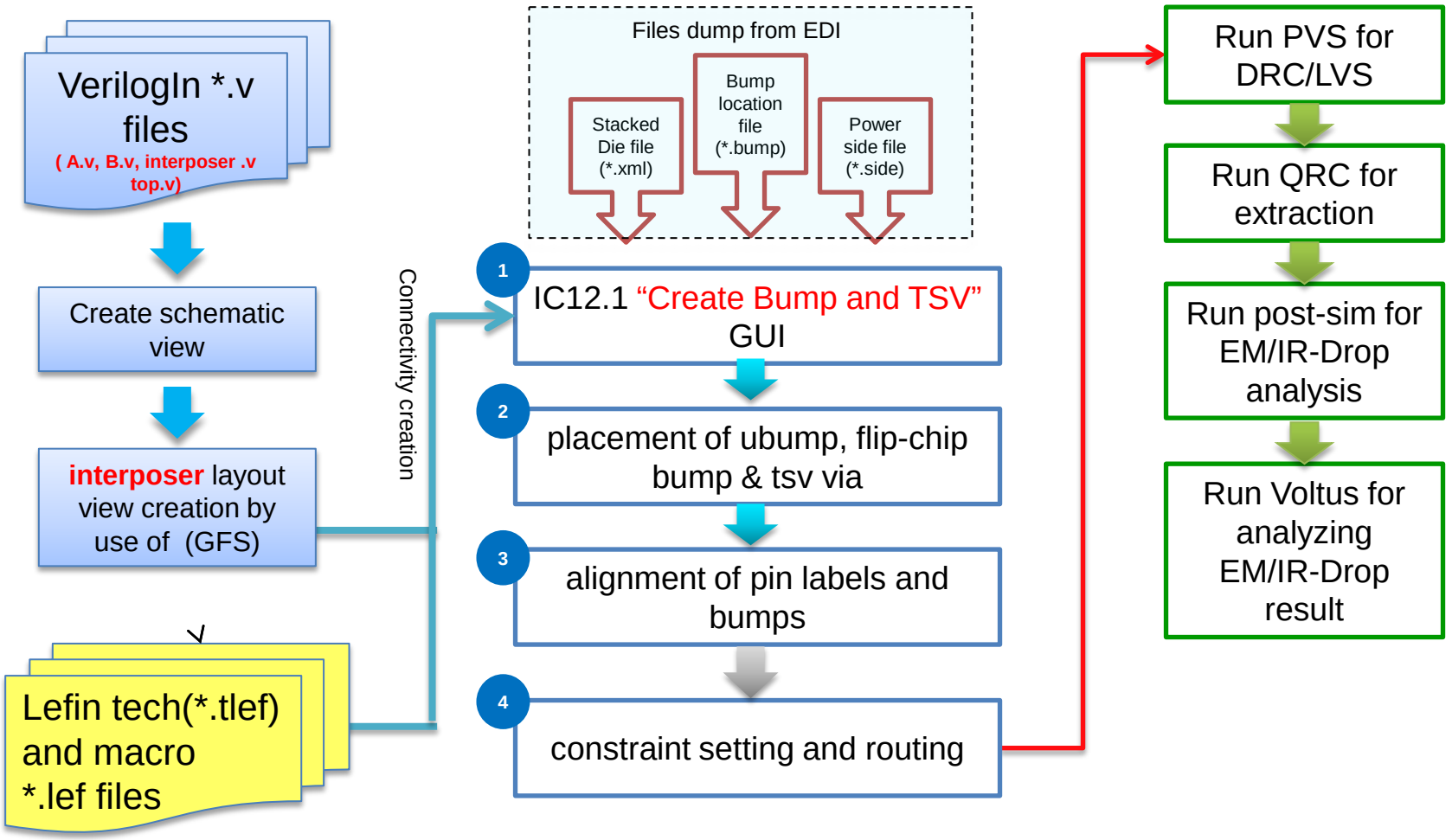


Source: Roshan Weerasekera, KTH

Taipei 10.16 2015 User Conference Graser

# Cadence Virtuoso Custom 3D-IC Design Solution

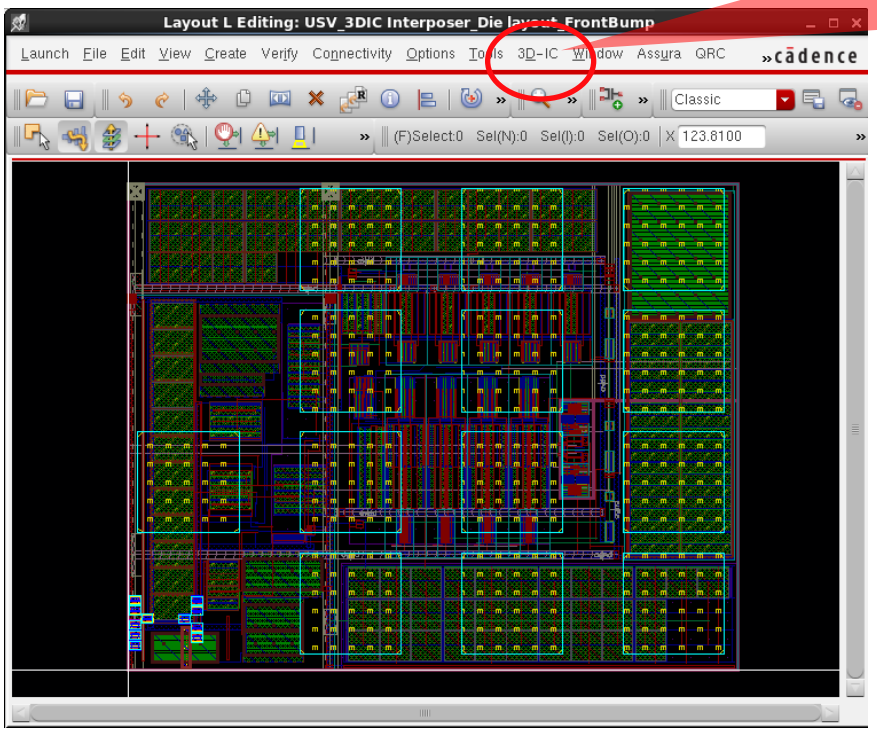
# Virtuoso Custom 3D-IC Design Flow

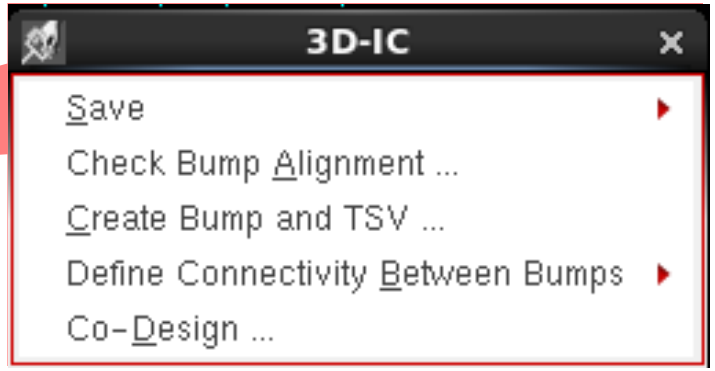



**Note: 1+2+3: IC12.1 3DIC features**

# What's Available in Virtuoso Specifics

- Virtuoso 6.1.6 / ICADV12.1

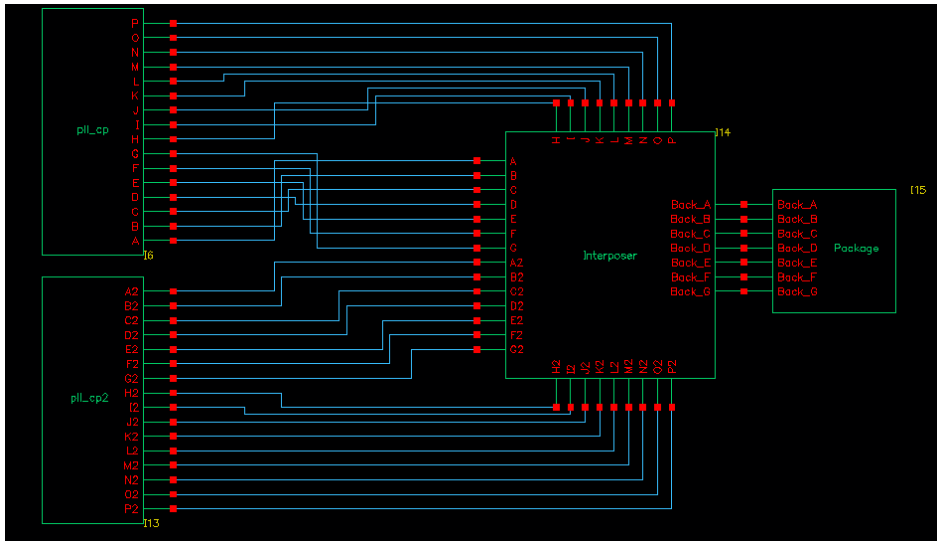


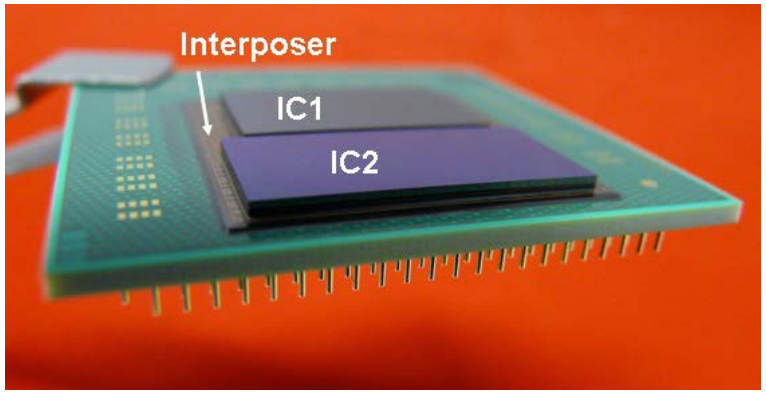



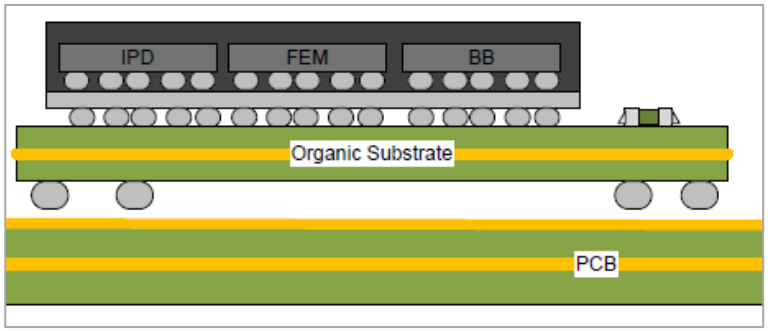

- Bump / TSV creation from adjacent die
- Auto-assign the Terminal to Bump
- Utilities to help resolve bump miss-alignment
- Export the Pad Locations / Bump Mapping File for performing the IR drop analysis

# Wrapper Schematic

- Creating Wrapper in Virtuoso Schematic Editor(VSE)
  - Top schematic storing connectivity from die to die / interposer.

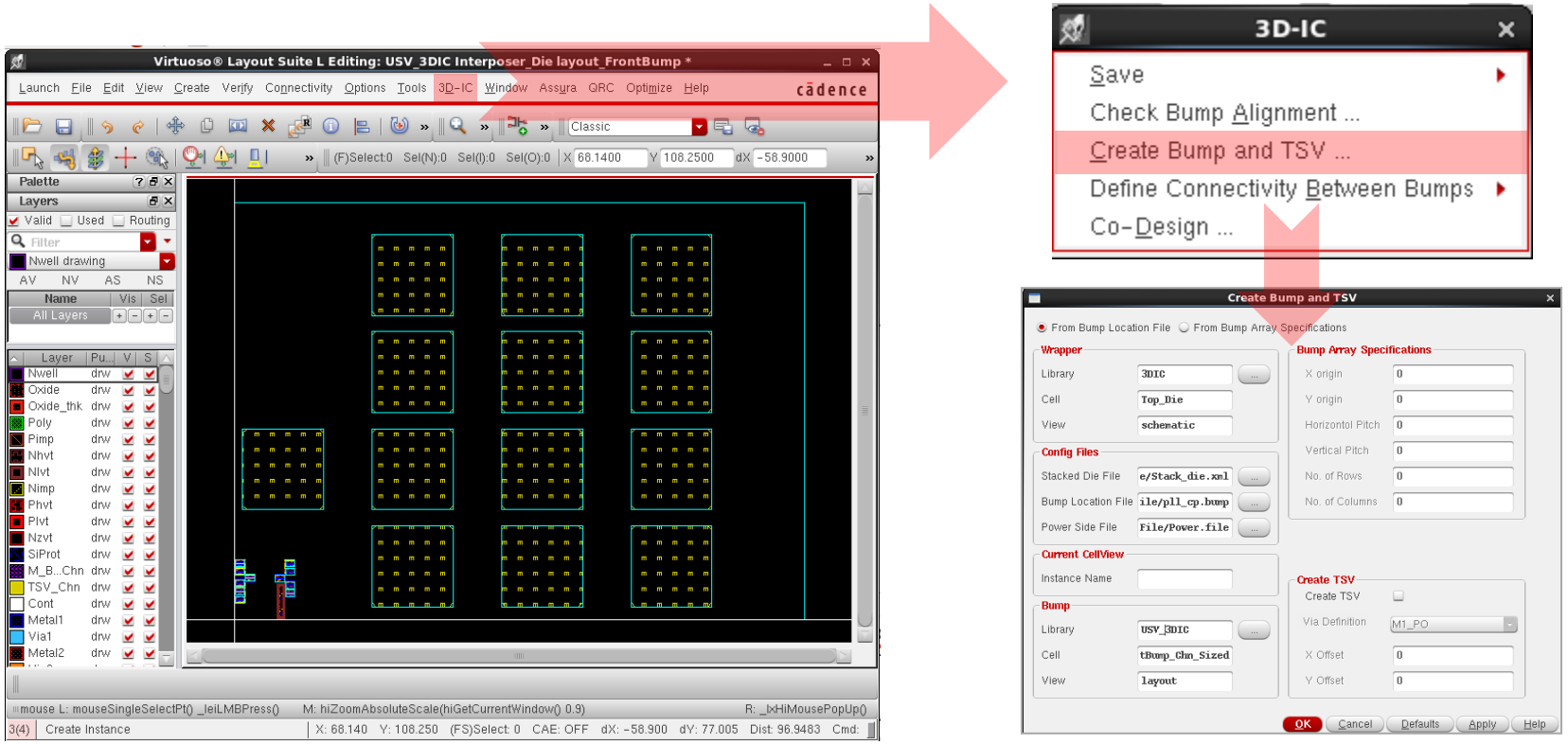


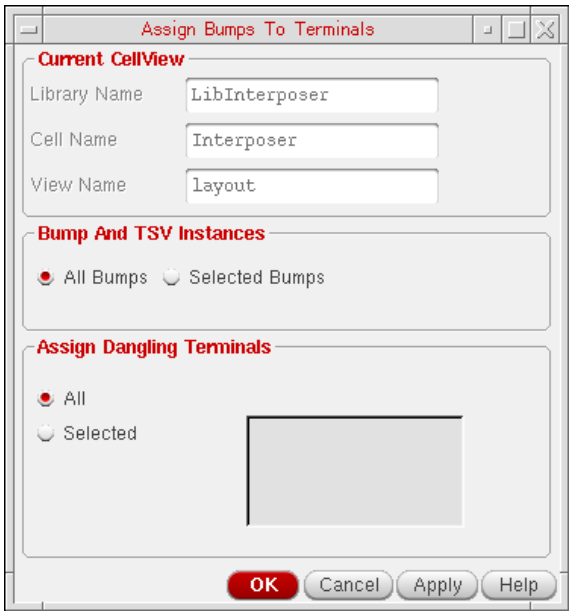
# Creating Bump and TSV from VLS

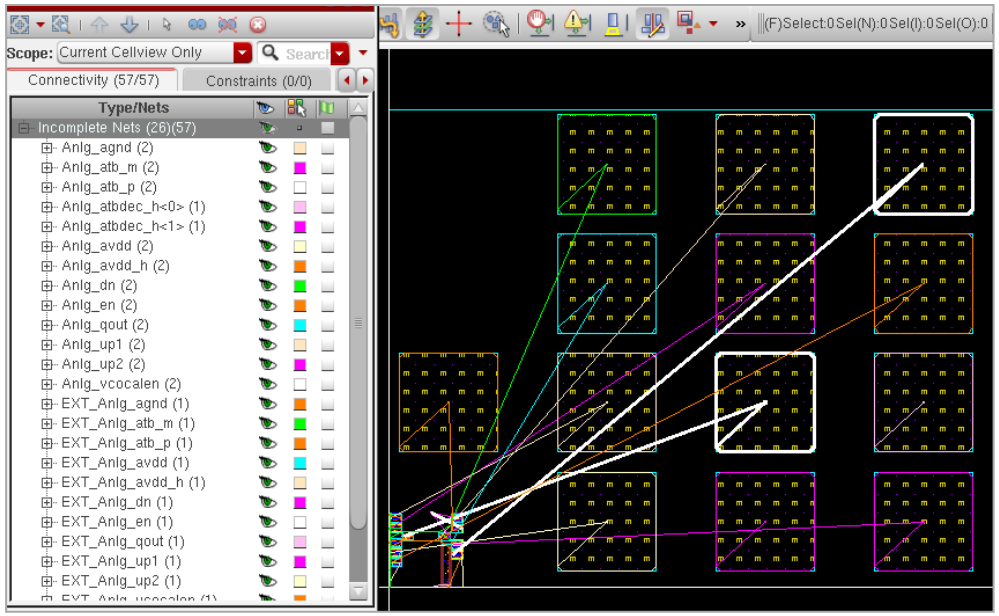
- Create bumps by using a bump location file to transfer bump information from one die to the adjacent die.
- Create bump arrays on dies such as silicon interposers. You need to assign these bump instances to their respective terminals.



# Establishing Connectivity Between Bumps

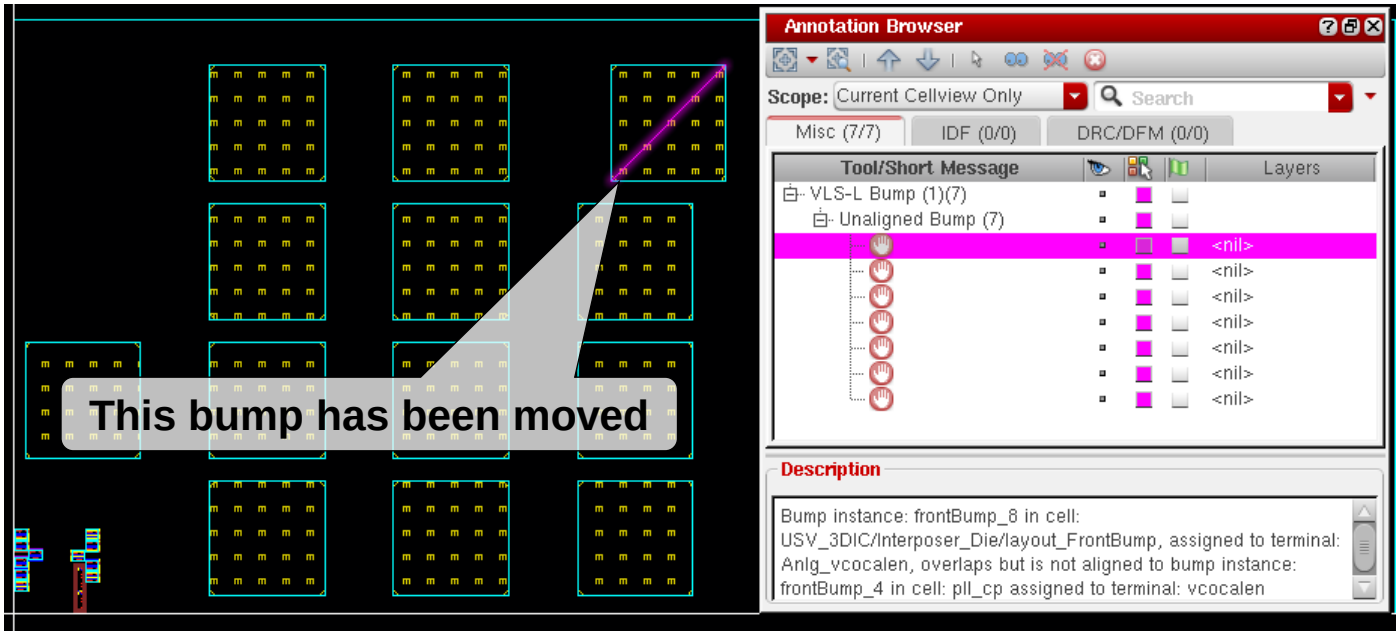
- After creating bumps and TSVs, you establish connectivity between bumps
  - Assigning Bump Instances to Terminals
  - Moving PinFig Objects to Bumps
  - Creating Bump Labels



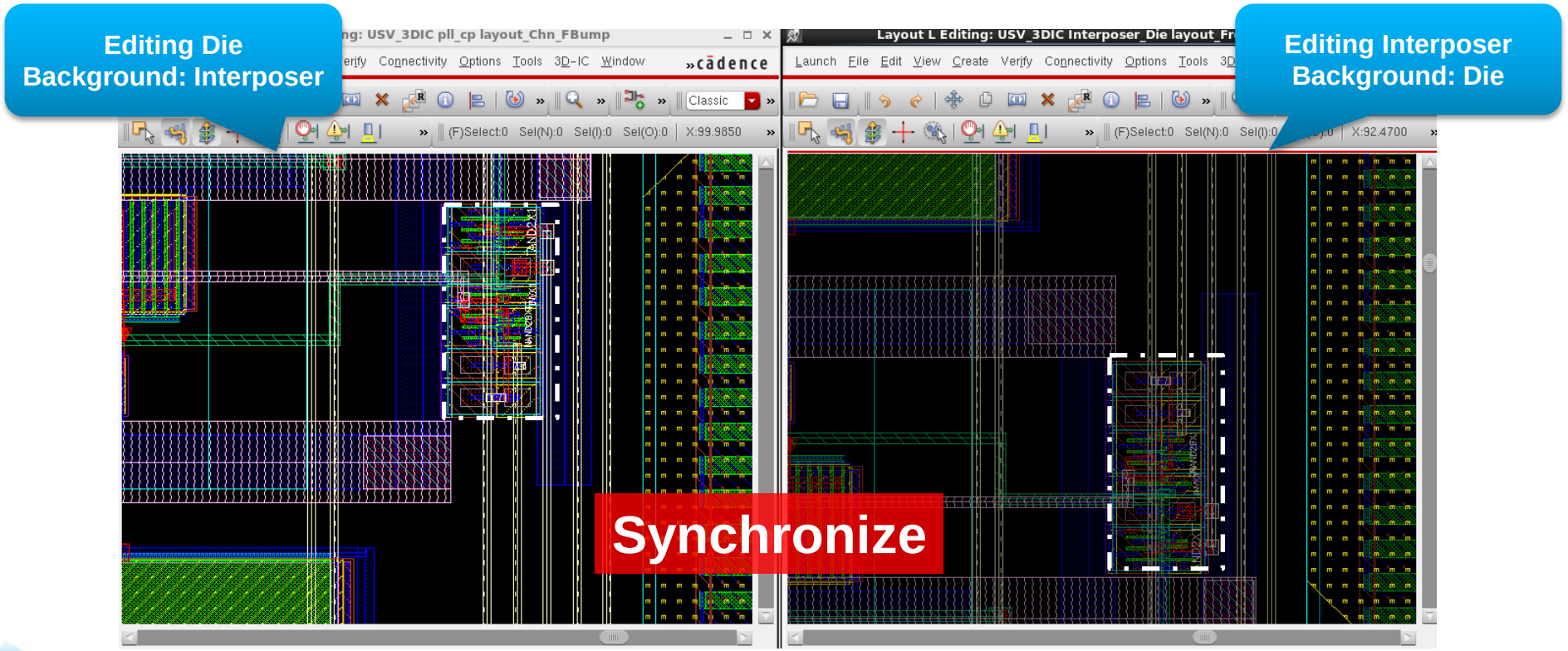
# Bump Alignment Checker

- When making manual adjustments to the design, you may accidently move or delete a bump.
- This is integrated with Annotation Browser. So, you can see the list of misaligned bumps there with all relevant info.
- Using the “Check Bump alignment” to prevent this error condition from occurring.



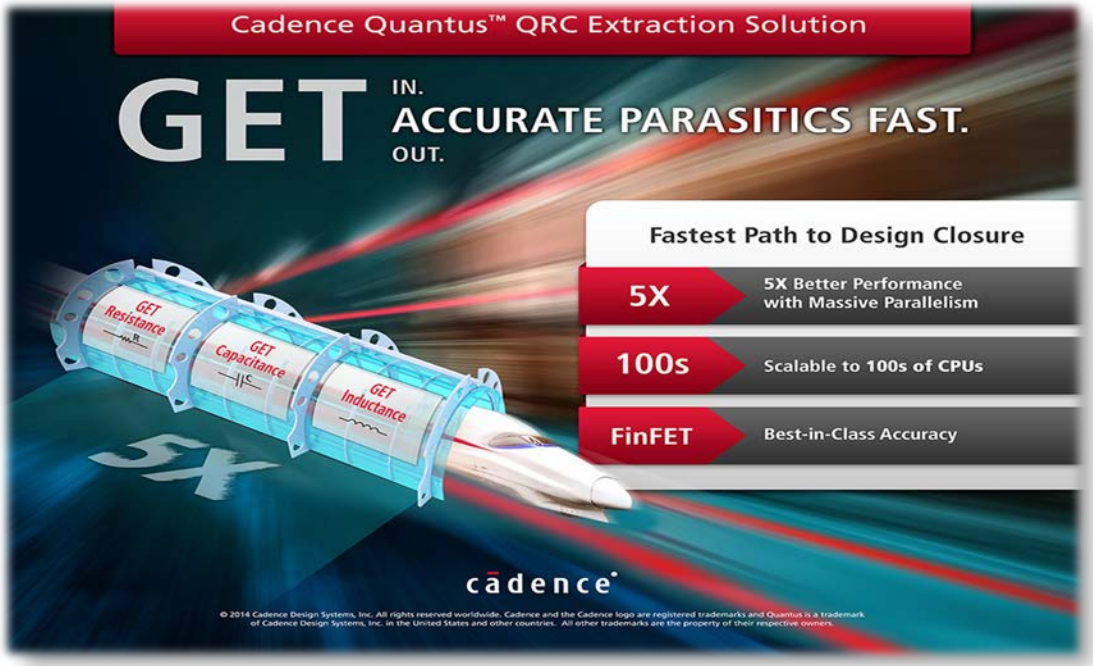
# Using Co-Design

- This allows designer to see one die over another at the same time. For example, you can work on the Interposer actively in one window, with the die visible dimly in the background. And in the second window, it is reverse, i.e. the die is active with Interposer in the background.



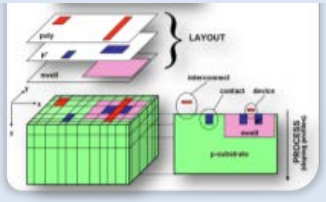
# Parasitic Extraction Solution

- Next-generation Cadence® Quantus™ QRC Extraction Solution
  - Up to 5X faster performance for single and multi-corner extraction runs
  - Scalable to 100s of CPUs / machines
  - Best-in-its-class down to FinFET accuracy / performance
- New random-walk based field solver, Quantus FS
- Fully certified at TSMC for 16nm FinFET

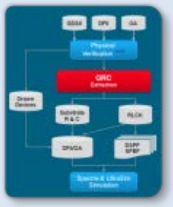


# Supports all Design Types with Industry-Leading Functionality

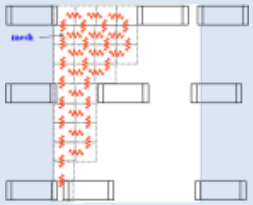
- Custom / Analog and RF Designs
- SerDes
- IP / SRAM / Bitcell Characterization
- Memory, PowerMos, Image Sensors, etc.



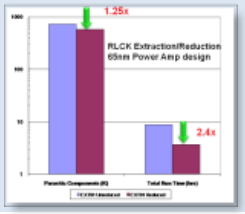

**Substrate Noise Analysis (SNA)**
- Full 3D substrate model
- Full chip and block level
- Tightly integrated in Virtuoso



**Inductance Extraction**
- Support PEEC method
- Sweep from DC→100GHz
- Supports mutual and Self inductance



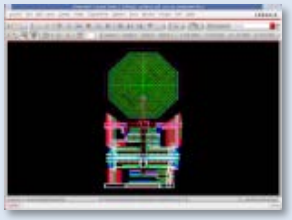
**MeshR**
- Used for PowerMos / LCD
- Better accuracy for all irregular or wide metal shapes

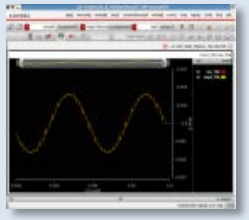



**RLCK Reduction**
- Supports RC and RCLK redux
- 20x simulation time reduction, with 5% accuracy
- 2.4x total TAT— good accuracy

# QRC Extracted View—Integration in Virtuoso Platform

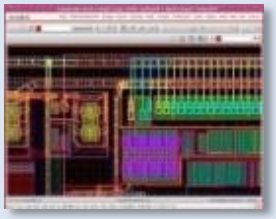
**Extracted View**
- Integrated with Virtuoso®
- LVS View Supports PVS, Assura, Calibre
- MeshR and substrate extraction for powerMos





**Simulation Analysis**
- Integrated with Virtuoso ADE
- Easy simulation debug
- DC simulation for Rdson result

**Design Debug Environment**
- Back Annotation
- Schematic-Layout Cross-probing



**EMIR Analysis**
- Accurate IR Drop Analysis
- Accurate EMIR Analysis & Visualization
- Gen models for cell based analysis
- Supports Voltus / Voltus-Fi

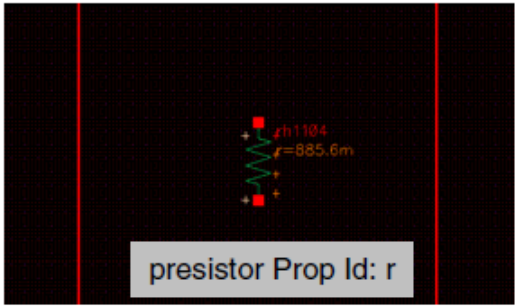
**Integrated with Virtuoso®**

Faster design closure for custom blocks and top level

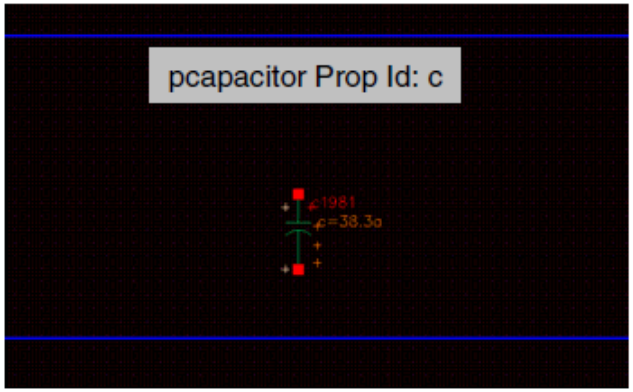
# Output Format Setup: Extracted View

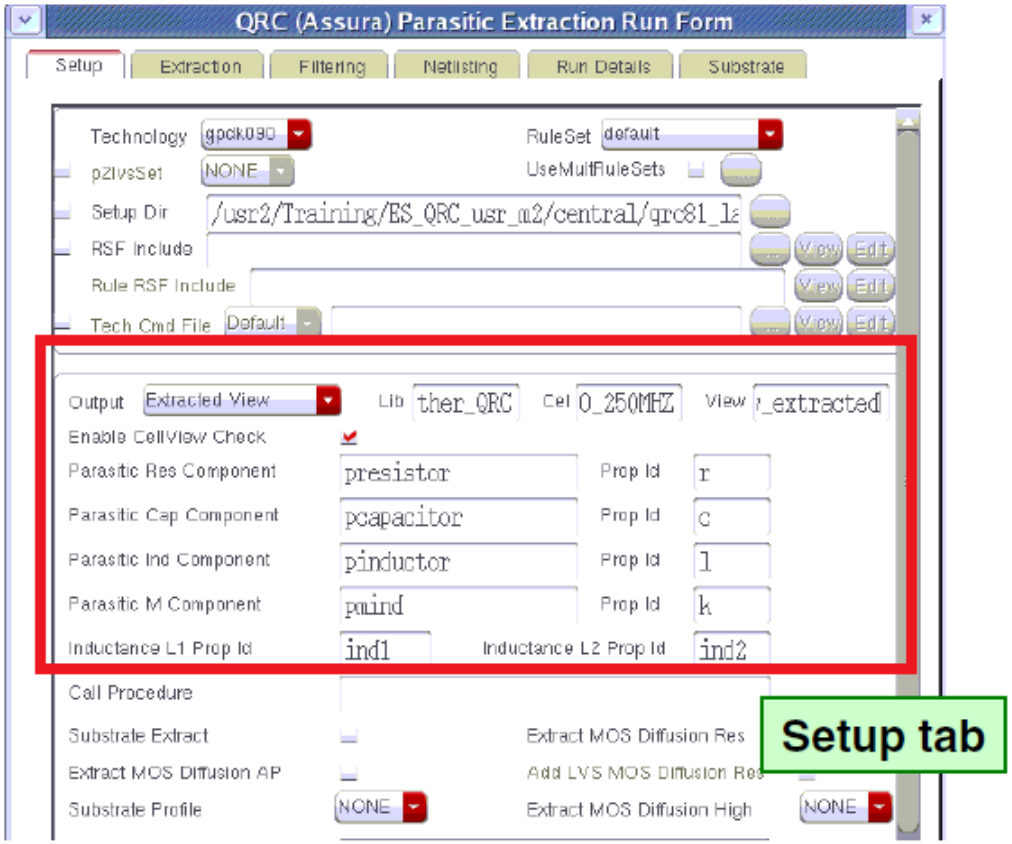
- In extracted view, graphical symbols of parasitic elements are overlaid onto layout shapes seen by QRC

Parasitic resistor in extracted view



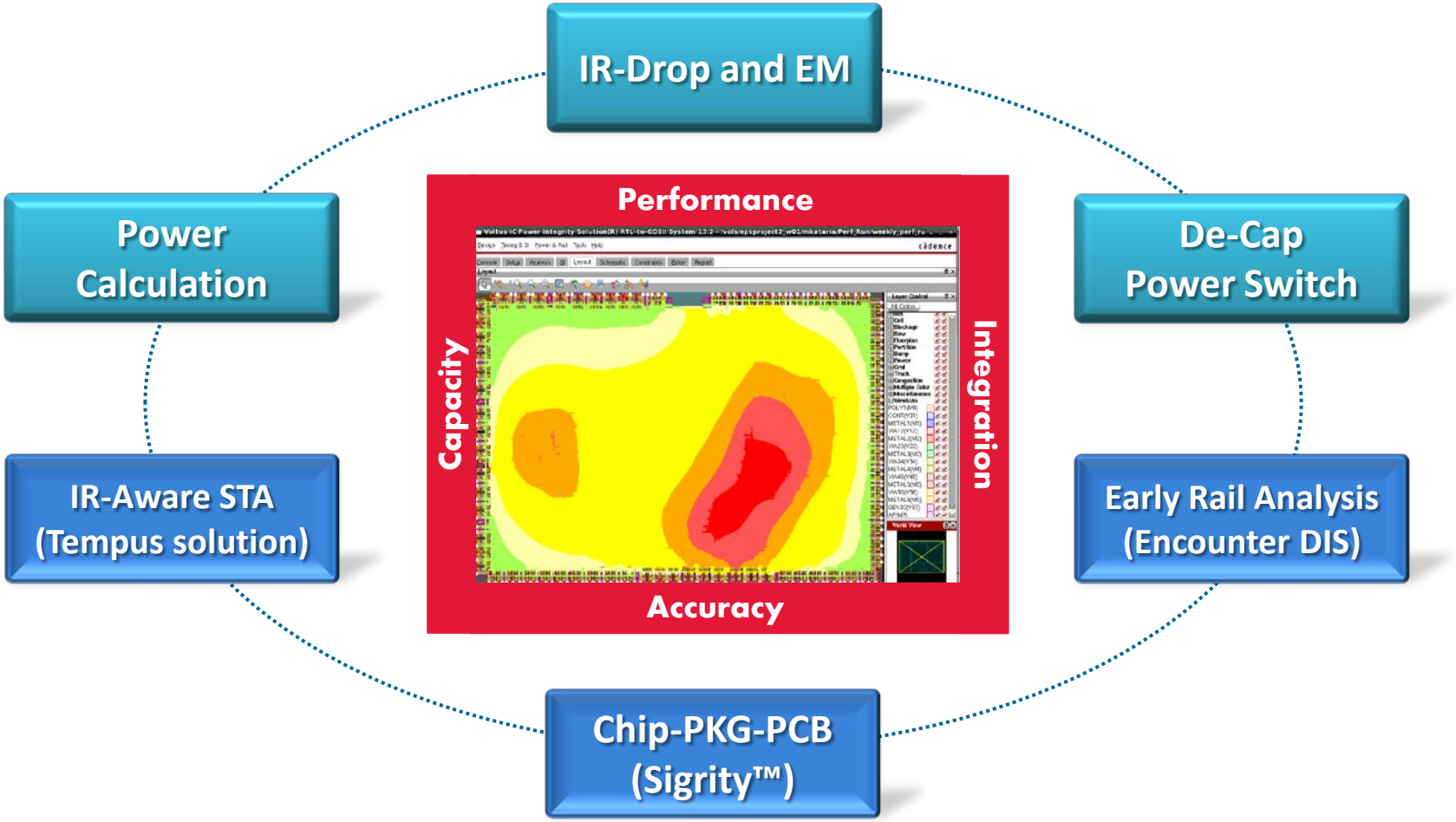

Parasitic capacitor in extracted view



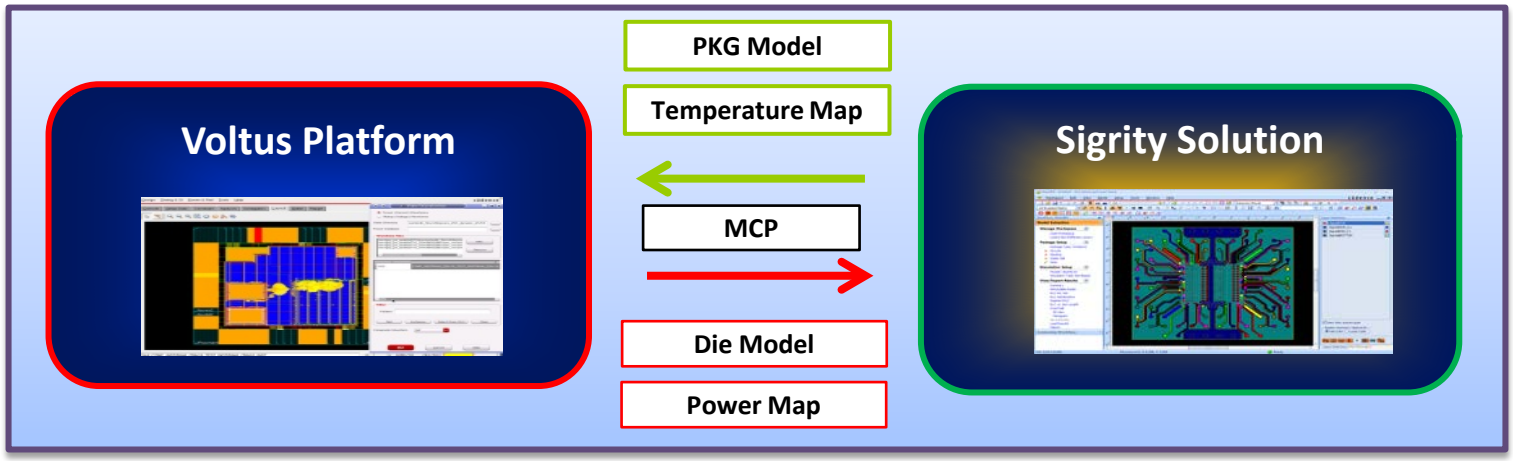
# Voltus IC Power Integrity Solution

- The next-generation SoC power signoff platform



# Voltus and Sigrity Chip-PKG-PCB Co-Simulation

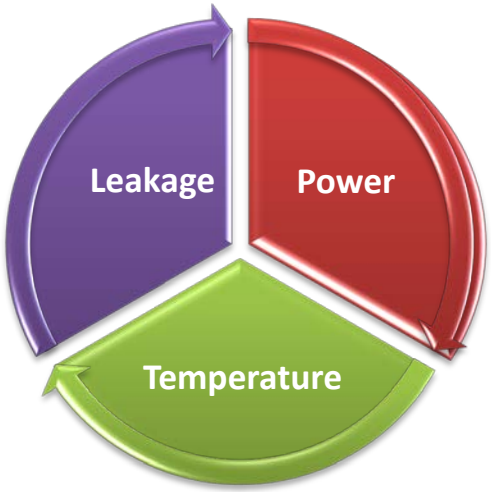
- Accurate power signoff for highly coupled power delivery network

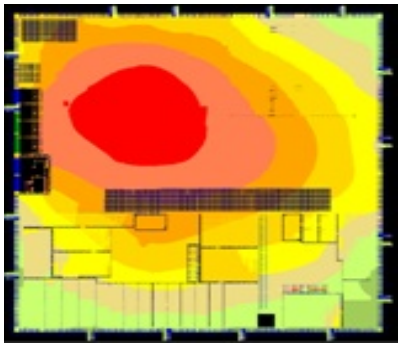



  - Die-model and PKG/PCB-model in broadband SPICE format for “Voltus + Sigrity” co-simulation
  - Power map/temperature map for electro-thermal co-analysis
  - Comprehensive power and signal integrity analysis

# Chip-Centric Thermal Analysis

- Electrical / thermal co-simulation



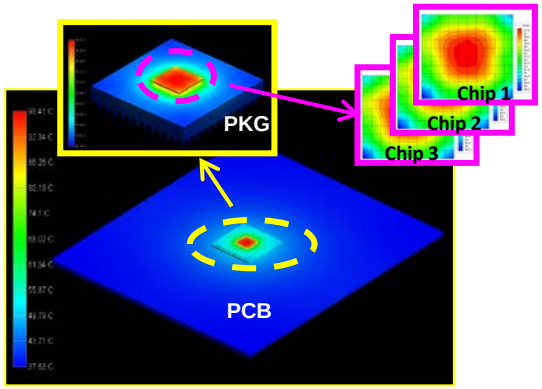



Temperature Map

Chip-PKG-PCB Temperature

Power Map

**Voltus**

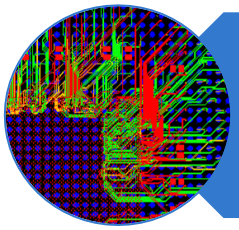



**Sigrity**

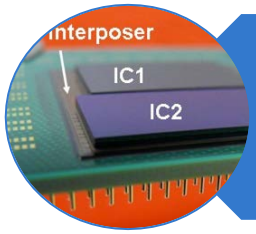
- Thermal runaway
  - Positive feedback among chip's temperature, leakage, and power dissipation
  - Temperature dependent IR-drop and EM
- Chip-centric thermal co-simulation with "Voltus + Sigrity"
  - Voltus output: temperature and location dependent "Power Map" file
  - Sigrity computes detailed temperature distribution for chip-PKG-PCB (T vs. time)
  - Voltus tool reads back "Temperature Map" file for EMIR convergence
  - Thermal view available in 2D/3D

# Summary

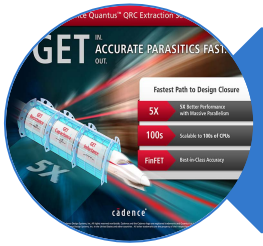
# Summary



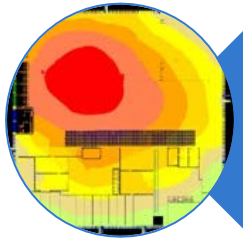
Cadence focuses on making you success




Innovative features to address advanced technologies like interposers, FO-WLP, 2.5 / 3D




Up to 5X faster performance for single and multi-corner extraction runs



Delivers comprehensive EMIR solution with Voltus / Sigrity

Taipei 10.16 2015 User Conference Graser

# Thanks