Potential Power Delivery Network Issue In The Simple Structure Design

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ADLINK TECHNOLOGY INC.

Abstract

- Power integrity concept
- Why is DC analysis important?
- Rule of thumb in DC analysis
- Simple structure design case study
- Summary

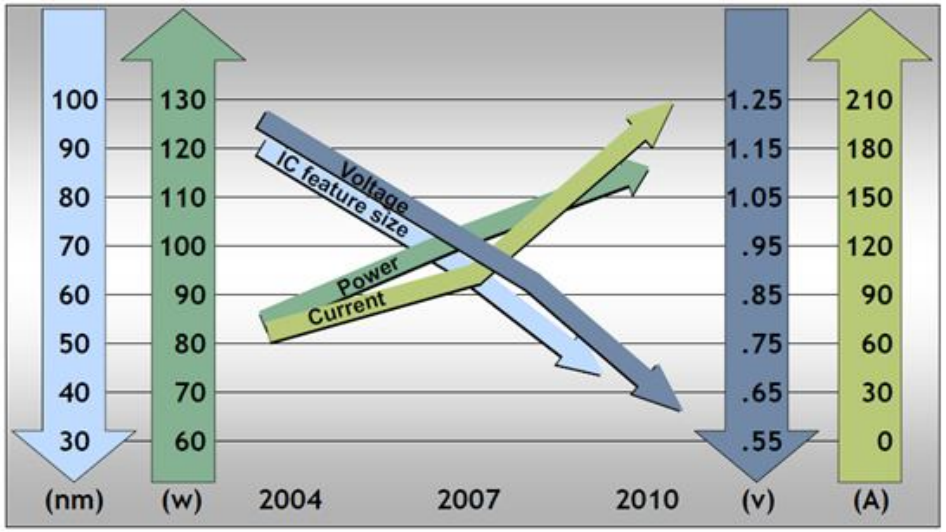
Power Integrity Concept

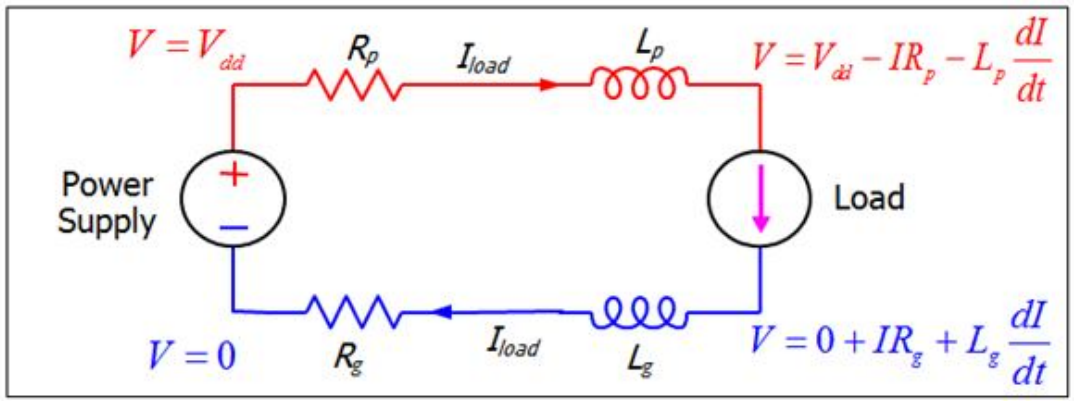
*What is best **DC** power plane performance?*

- *Devices see voltage closet to nominal voltage*
  - ✓ *Low IR drop*
  - ✓ *Well balanced DC voltages among devices on the same rail*
- *Low Temperature Rise on Metal*
  - ✓ *Low Current Density*
- *Power Efficiency*
  - ✓ *Low Power Loss*

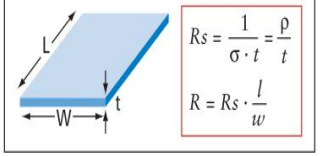
What is best **AC** power plane performance?

- Low noise
  - ✓ Low loop inductance
  - ✓ Low and Flat impedance





The resistance Rs of a plane conductor for a unit length and unit width is called the **surface resistivity** (ohms per square).



Obstacles: Power lines are not ideal and have finite resistance and inductance

- ♦ Resistive noise $V_R = IR$
  - – Caused by high transient currents drawn by the load
- ♦ Inductive noise $V_L = L\ di/dt$
  - – Caused by high current slew rates *di/dt* produced by the load

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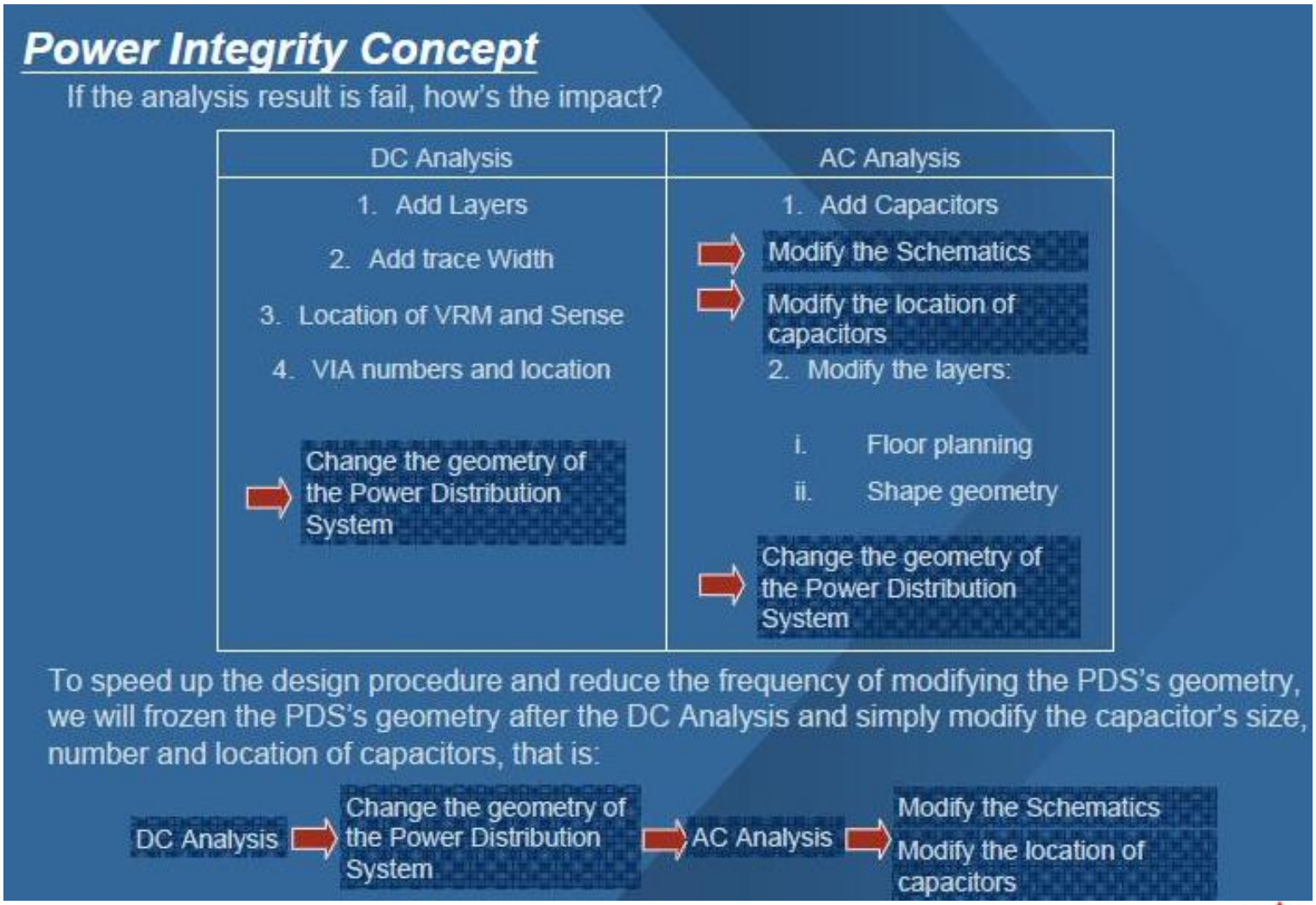
Power Integrity Concept



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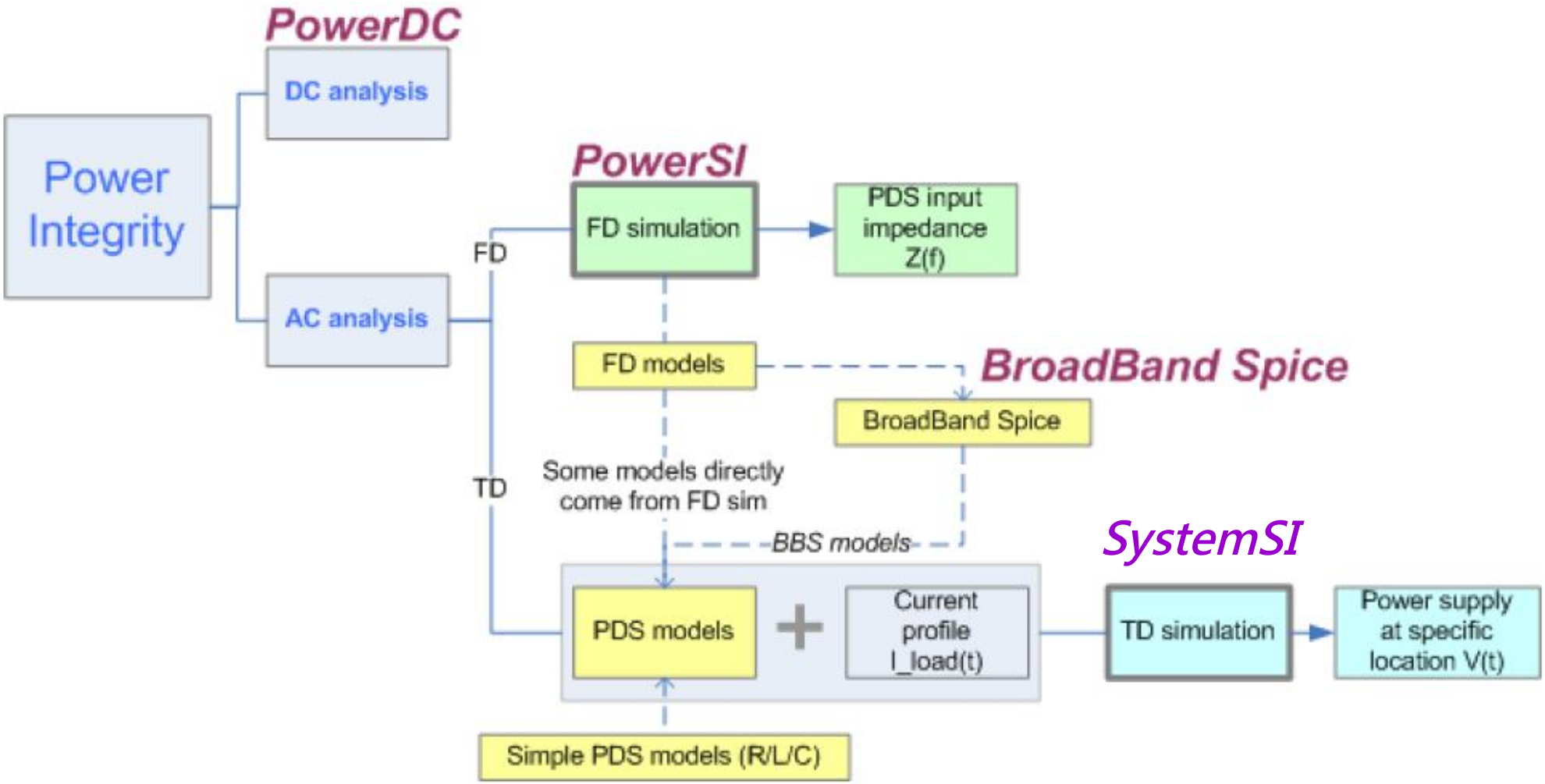

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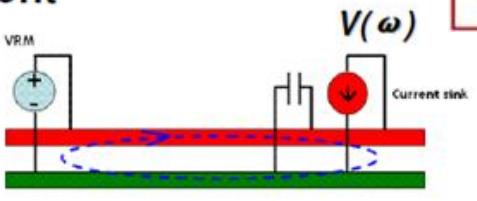
Why Is DC Analysis Important?

Voltage droop while chip sinks current

$$\Delta V(\omega) = Z_{input}(\omega) I(\omega) + IR(\omega = 0)$$

AC term DC term

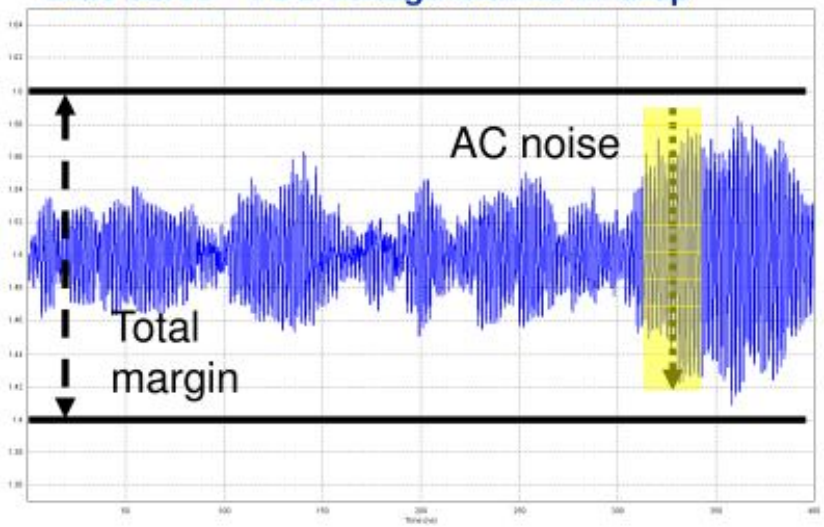


IRdrop	:	AC noise	
20	:	80	(typical)
10	:	90	(aggressive on DC)

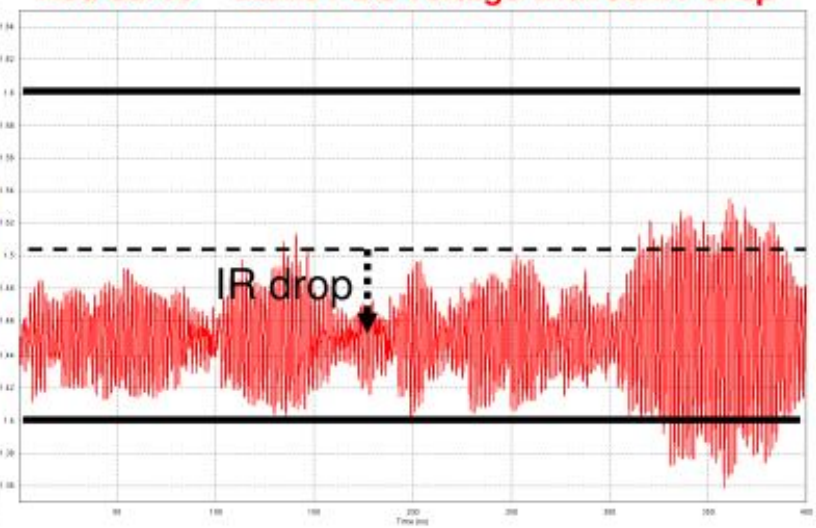
VDD = +1.5V +/- 5%

IRdrop : AC noise	=	20:80
IRdrop	=	+1.5V +/-1%
AC noise	=	+1.5V +/-4%

Blue curve – PDS voltage with no IR drop

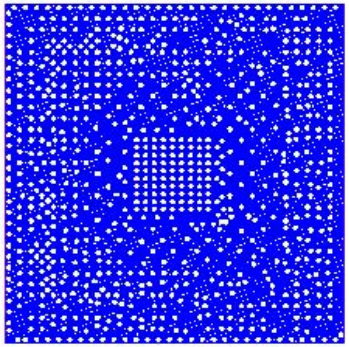


Red curve – Same PDS voltage with 50mV drop



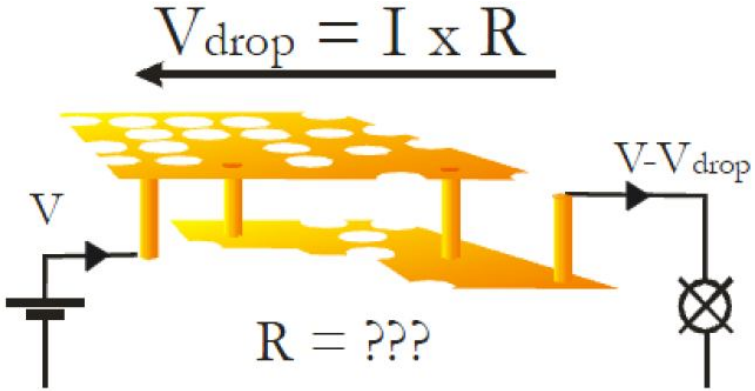
Why Is DC Analysis Important?

Neck-down

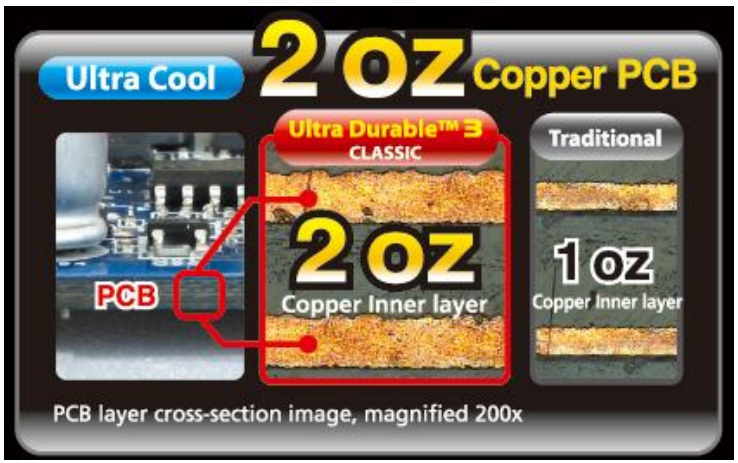


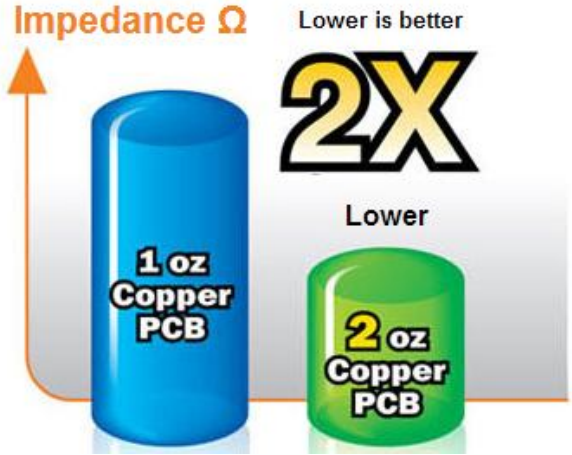
Swiss Cheese on solid plane

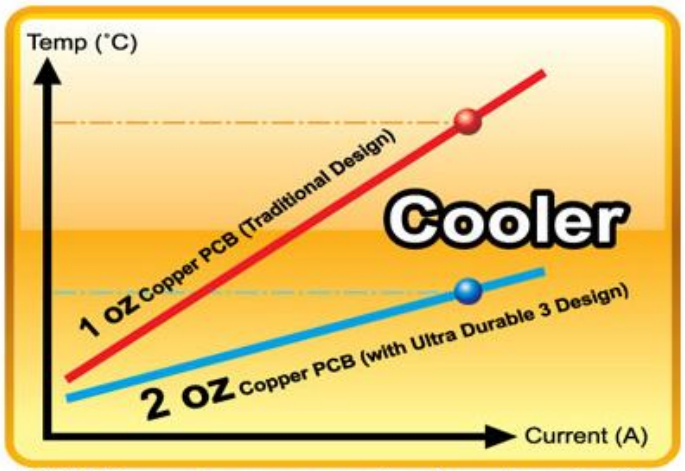
Dynamic trace routing can cut off the PDS



- IR Drop is a system level problem - analysis of the entire power distribution system (PDS) is necessary to optimize the end-to-end voltage margins for every device on the distribution



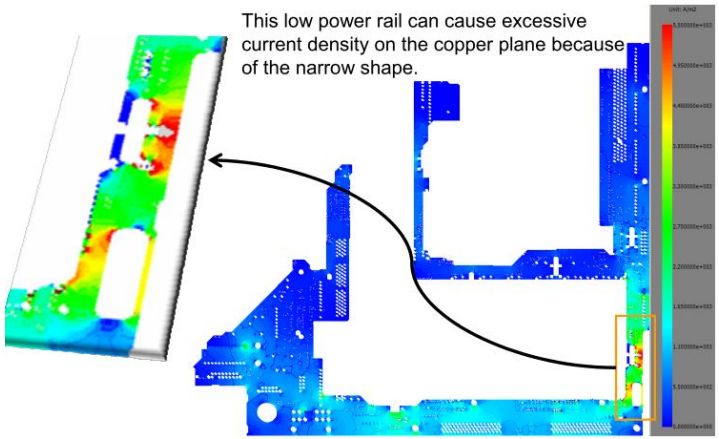




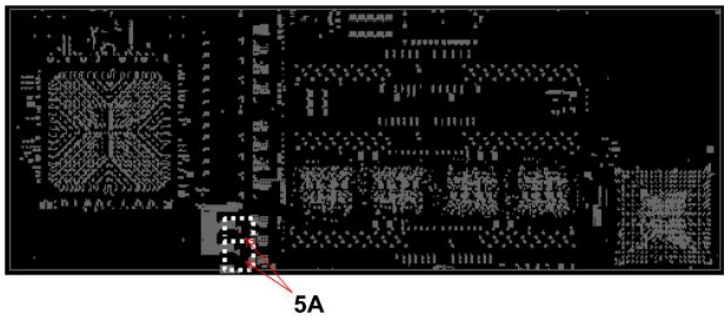
CPU VRM Temperature measurements under system setup with water-cooler block and CPU running at 100% loading

Why Is DC Analysis Important?

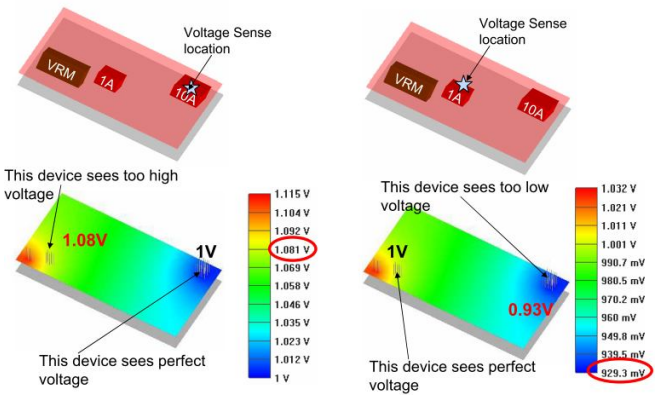
Localize Heat in low power net



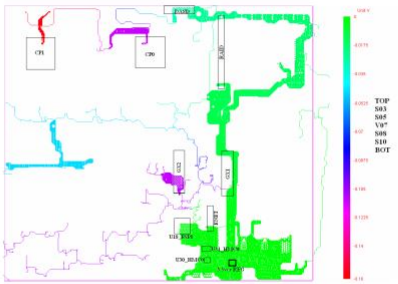
Identify vias that have high current flow.
Via Current plot can be used to pinpoint vias with high current flow.



Where to place the Sense Line when there are more than one device on the power rail?



Excessive IR drop due to narrow and long traces



Functional problem can be caused by too much IRdrop even in the low power .

IR drop target is 66mV

Voltage	refdes	criteria: Breif description	Max current (A)	66mV (2%): IR drop (mV)
+3.3VCS	U3_CP1	P6	0.250	-160
	U2_CP0	P6	0.250	-115
	J23_GX1	GX CARD	0.218	-113
	J24_GX2	GX CARD	0.218	-111
	J54_DASD	DASD backplane	0.006	-29
	J49_RAID	RAID card	0.006	-13
	U18_FSP1	FSP1 chip	0.51	-2.0
	J25_ENET0	ENET card	0.006	-1.4
	U31_HMC0	HMC chip	0.012	-1.2
	U30_HMC0	HMC chip	0.012	-1.0

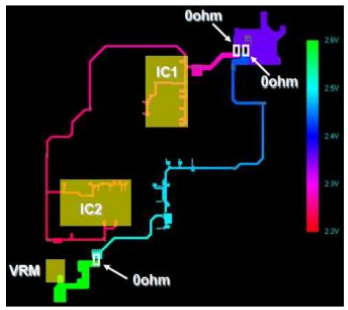
←159% over the target

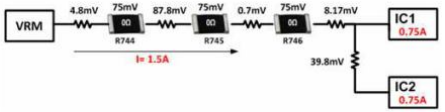
Excessive IR drop due to DC resistance on passive components

Show Results -> Voltage, Current & Resistance Tables (2 of 8 Failed)

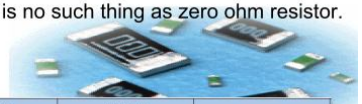
VRM Voltage | **Sink Voltage** | Interconnect Current | Resistance Measurements | Probe Measurements | Global Via Current | Global Via Current

Sink Name	Model	Nominal Voltage (V)	Input Tolerance (%)	Actual Voltage (V)	Margin (V)
IC2	Equal Current	2.600000e+000	2.000000e+000	2.230338e+000 ✗	-3.176616e-001
IC1	Equal Current	2.600000e+000	2.000000e+000	2.270782e+000 ✗	-2.772185e-001



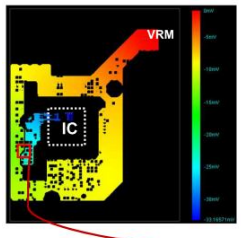


There is no such thing as zero ohm resistor.

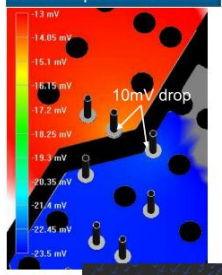


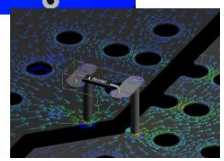
Maximum Continuous Current @ 70°C	Maximum Surge Current @ 70°C	Maximum Resistance
0.5 Amps	1.0 Amp Max. for < 1 second	
0.5 Amps	1.0 Amp Max. for < 1 second	
1.0 Amps	2 Amp Max. for < 1 second	
2.0 Amps	5 Amp Max. for < 1 second	50mΩ
2.0 Amps	10 Amp Max. for < 1 second	

Excessive IR drop on vias



5mV drop on each via





2.4A flows into each via

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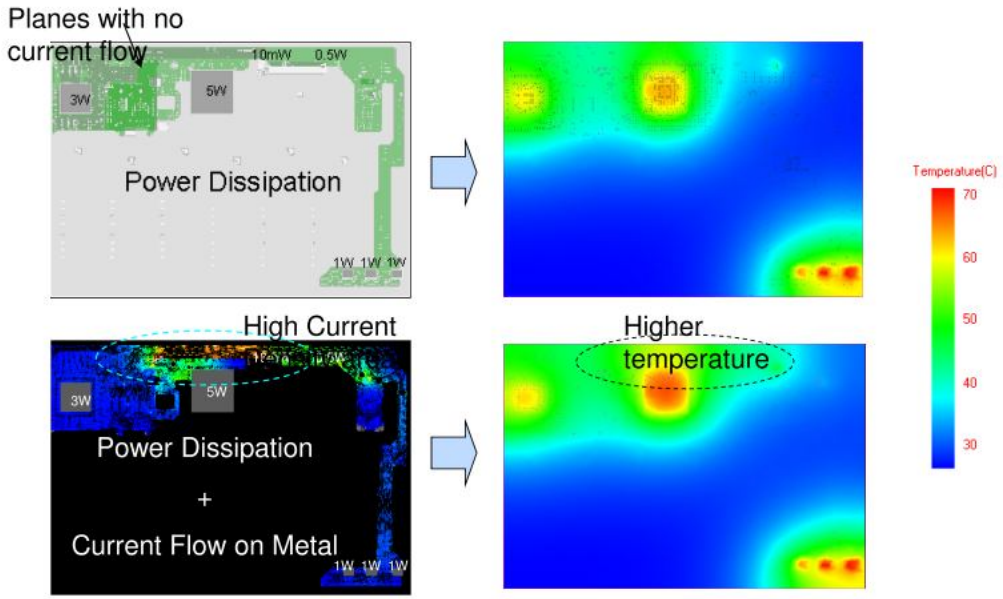
Why Is DC Analysis Important?

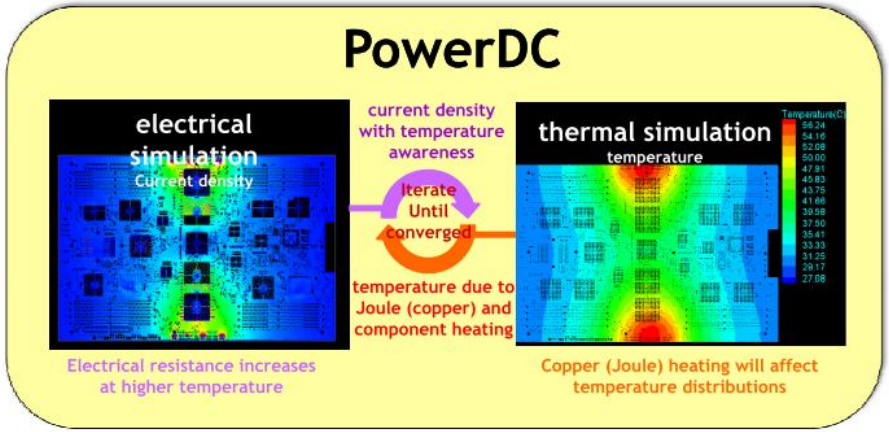
Electrical affects Thermal



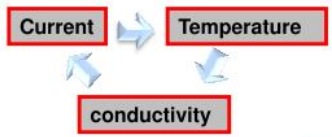
-Temperature increases due to joule heating from current flowing through a conductor

-Without electrical effect, thermal result is under-estimated

Electrical/Thermal Co-Simulation in One Integrated Tool



Integrated electrical/thermal co-simulation provides engineers with efficient design margins and lower manufacturing costs.



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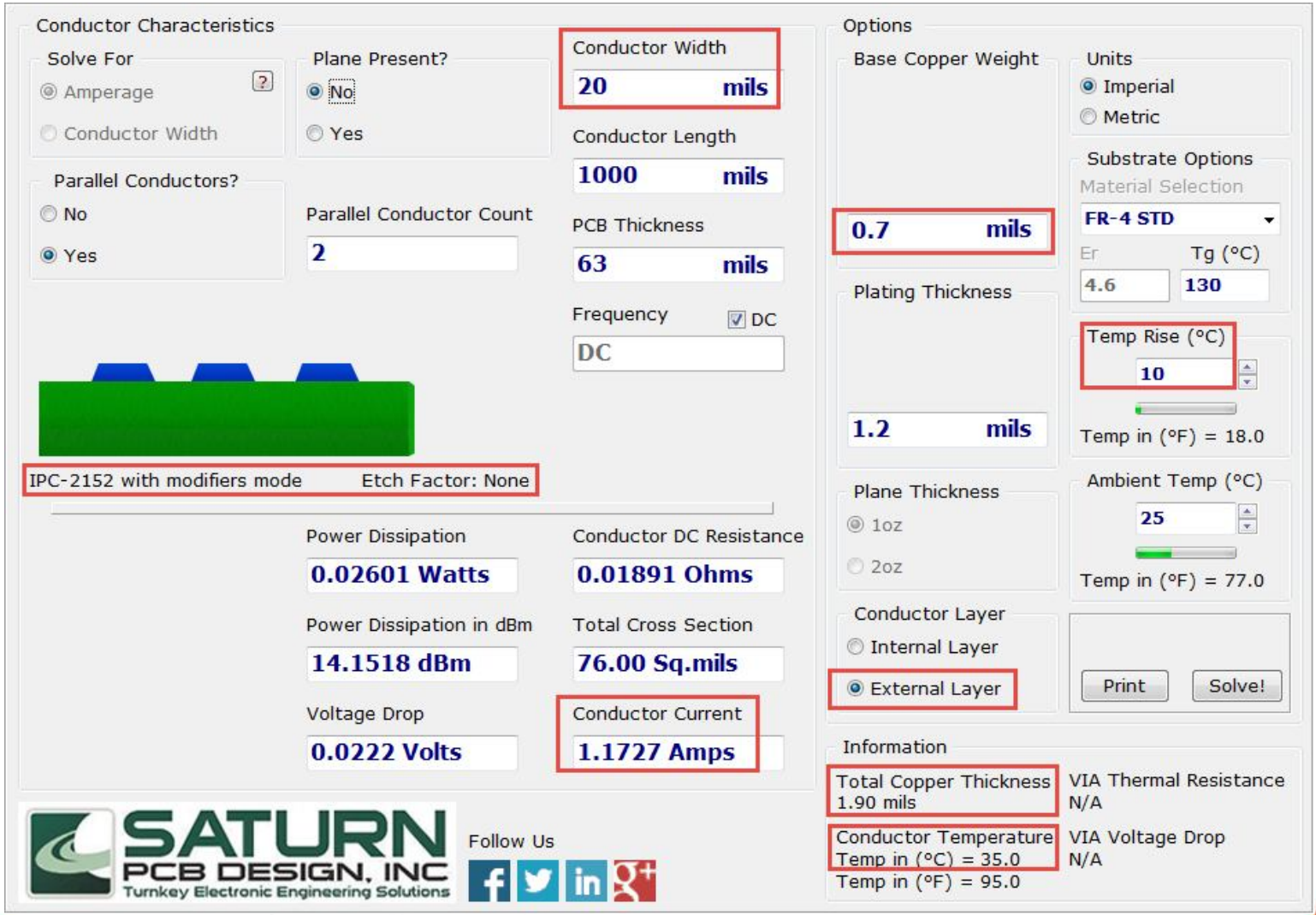
Rule Of Thumb In DC Analysis



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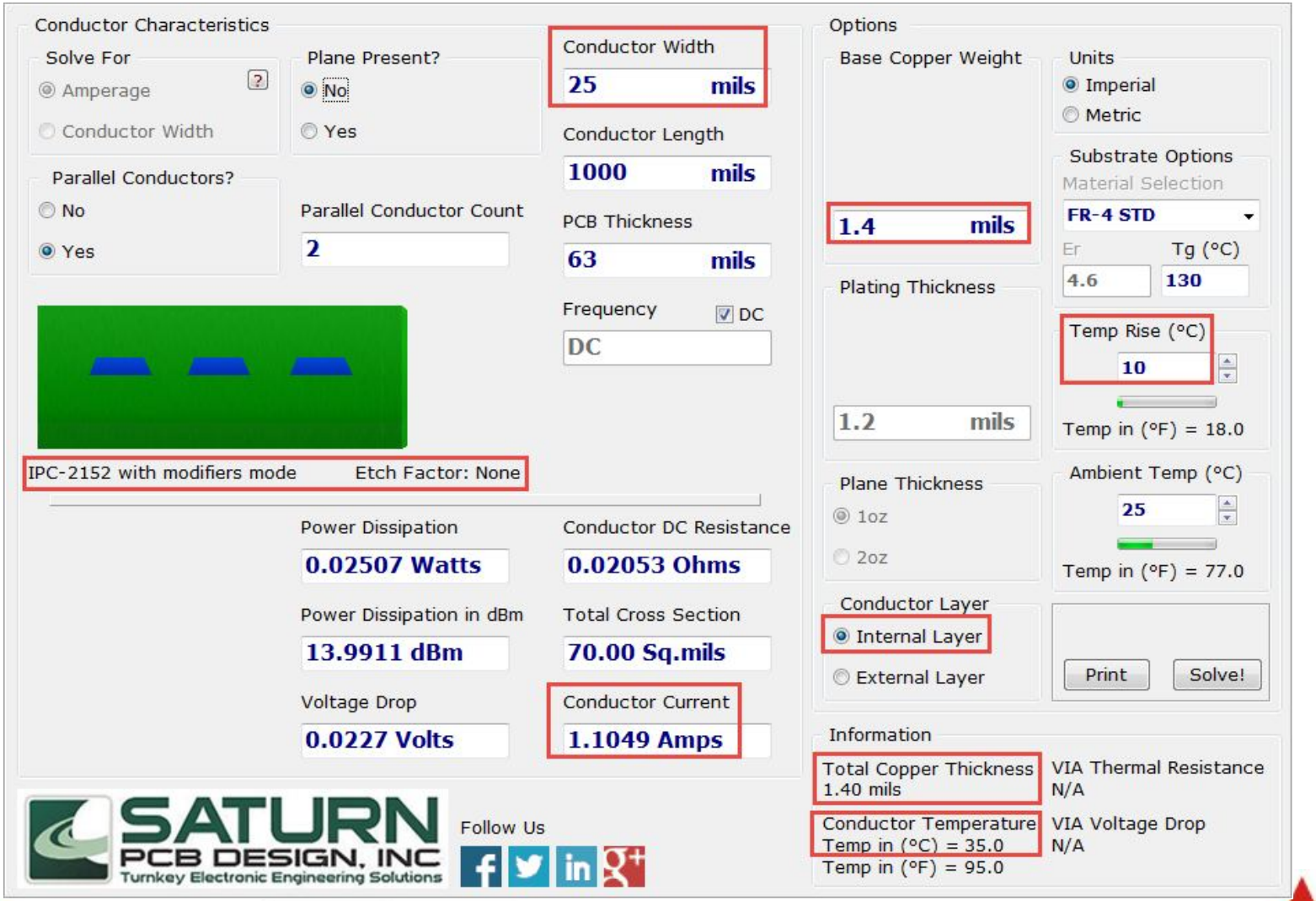

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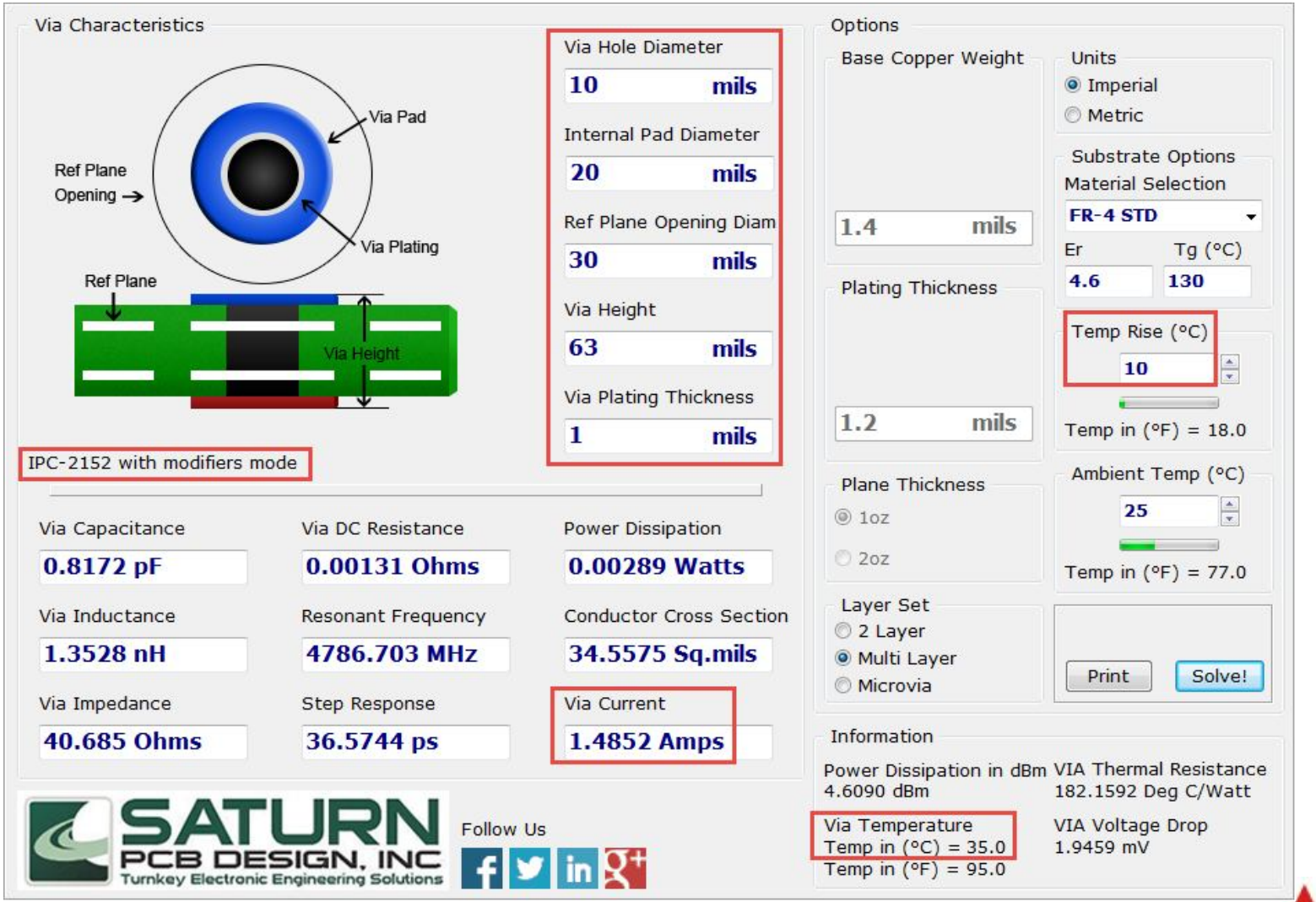
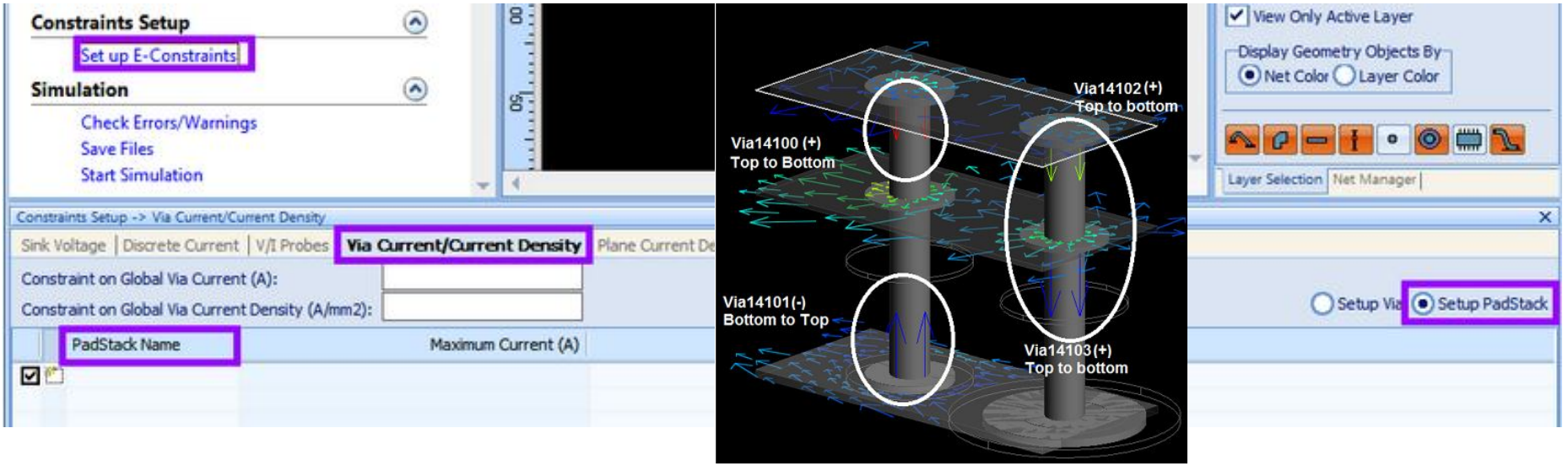


Rule Of Thumb In DC Analysis

The numbers were extracted from IPC-2152, for 1mil plating thickness and no copper planes. If copper planes are present, then the temperature rise will be lower.

Via size (mil)	Current for *10℃* temp rise (A)	Current for *30℃* temp rise (A)	Current for *45℃* temp rise (A)
8	1.2	2	2.3
10	1.4	2.3	2.8
12	1.6	2.6	3.2
16	1.8	3.1	3.8
20	2.1	3.6	4.3
30	2.7	4.6	5.7
40	3	5.5	6.8

Rule Of Thumb In DC Analysis



Your constraint and actual current will be displayed in the ***Global Via Current*** tab of the Results table:

Results and Report -> Global Via Current (7 of 7 Failed)

Other Component Voltage | Power Loss | Probes Measurements | **Global Via Current** | Global Via Current Density | Specific Via Current | Global Plane Current Density | Specific Plane Current Density | Trace Current Density | Wire

Via Name	Net	PosX (mm)	PosY (mm)	StartLayer	Upper Node	EndLayer	Lower Node	PadStack	Maximum Current (A)	Actual Current (A)
Via14095::+...	+1.5V	274.32	213.36	Signal$TOP	Node96515::+...	Signal$L1	Node96516::+...	VIA-22-10HOLE	0.5	1.2532
Via14097::+...	+1.5V	274.32	212.09	Signal$TOP	Node96517::+...	Signal$L1	Node96518::+...	VIA-22-10HOLE	0.5	0.715189
Via14100::+...	+1.5V	273.05	213.36	Signal$TOP	Node96520::+...	Signal$L1	Node96521::+...	VIA-22-10HOLE	0.5	1.96813
Via14102::+...	+1.5V	273.05	212.09	Signal$TOP	Node96522::+...	Signal$L1	Node96523::+...	VIA-22-10HOLE	0.5	1.26348
Via38873::GND	GND	272.415	215.773	Signal$TOP	Node5037::GND	Signal$BOTT...	Node90269::GND	VIA-22-10HOLE0	0.5	-0.832212
Via38877::GND	GND	273.685	214.757	Signal$TOP	Node5036::GND	Signal$BOTT...	Node90285::GND	VIA-22-10HOLE0	0.5	-0.825979
Via38878::GND	GND	272.415	214.757	Signal$TOP	Node5035::GND	Signal$BOTT...	Node90289::GND	VIA-22-10HOLE0	0.5	-2.56298

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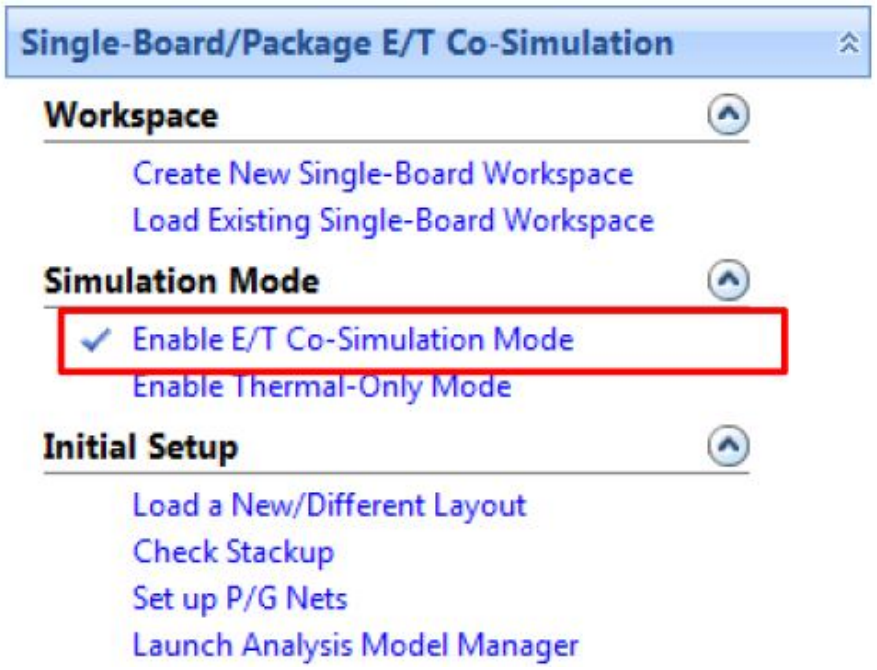
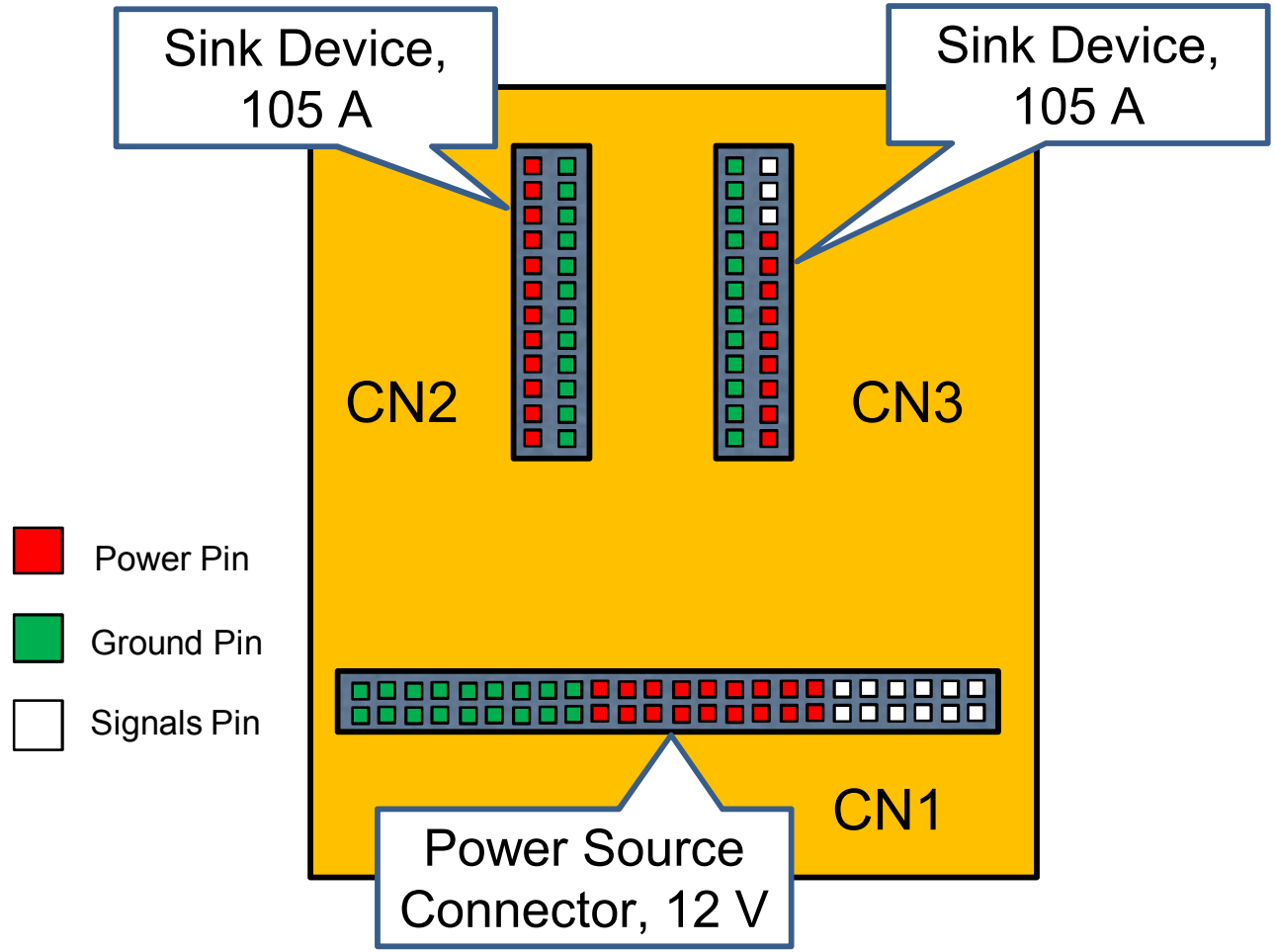
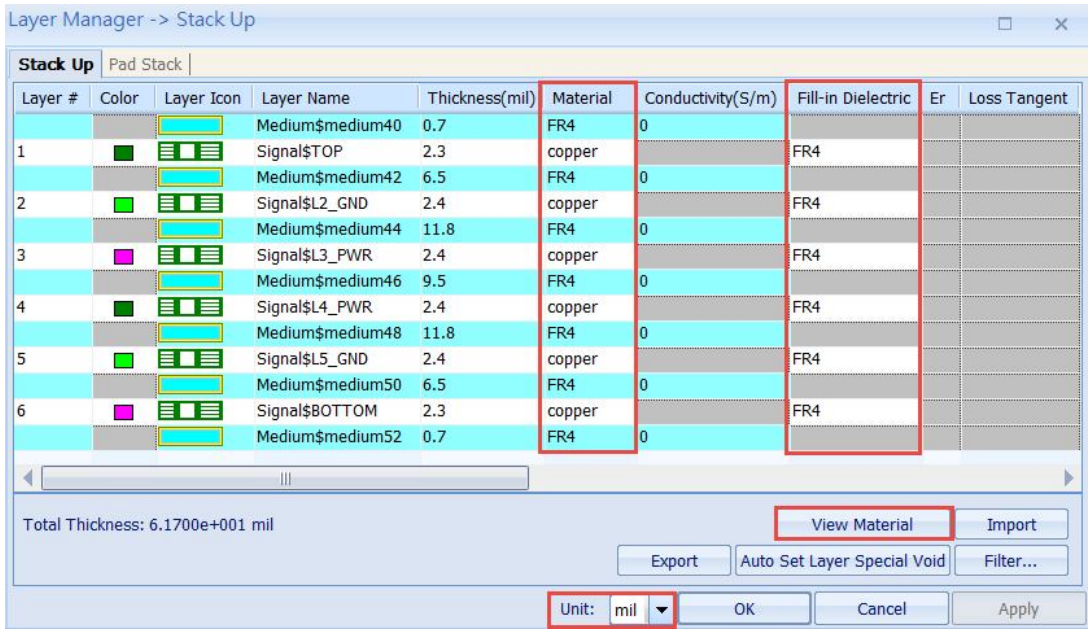
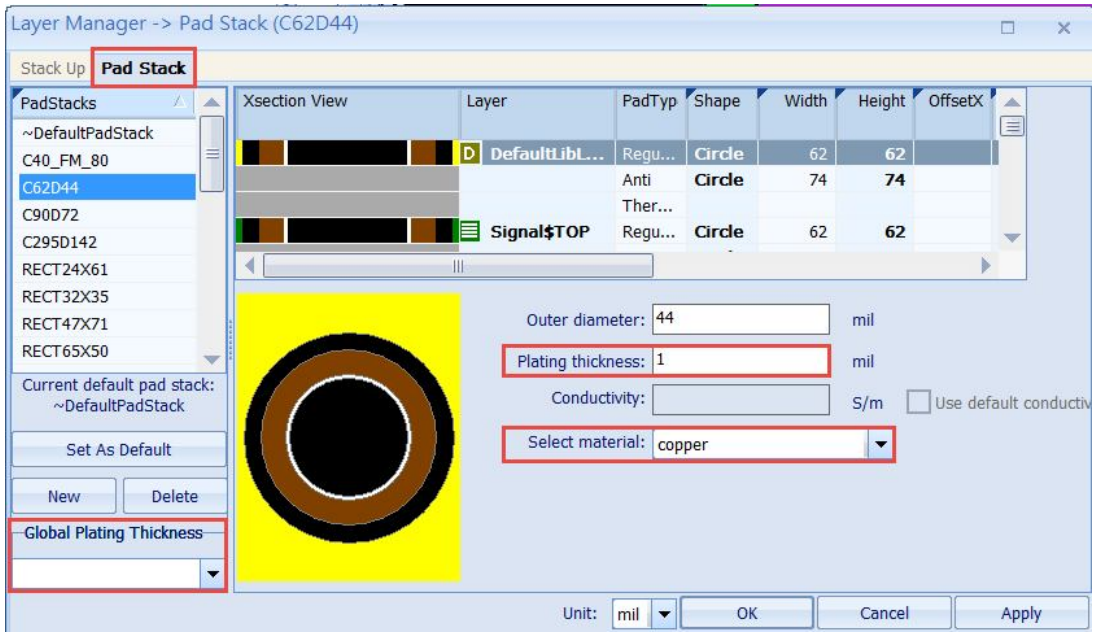
Simple structure design case study





Simple structure design case study

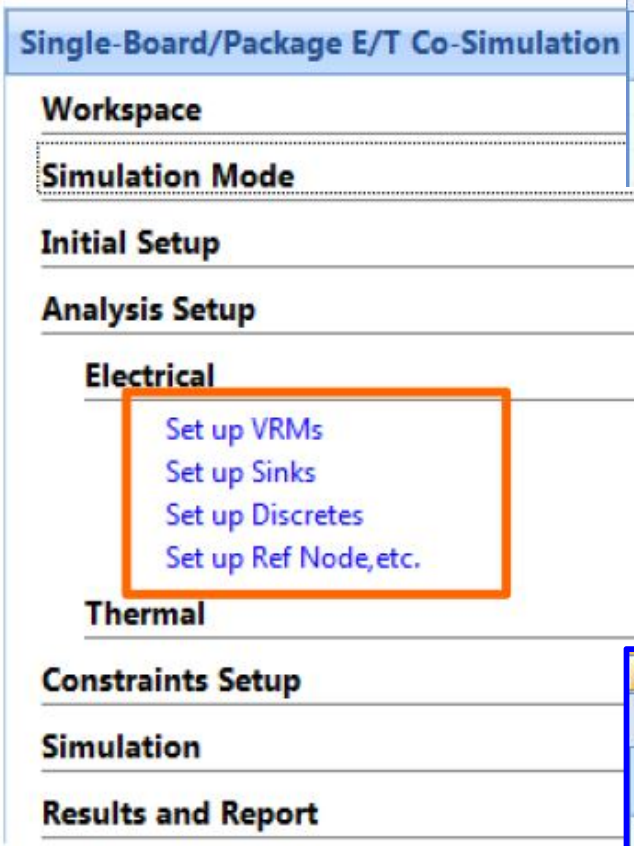




Set the plating thickness is important for IR drop analysis.

Set the material is important for thermal analysis.

Simple structure design case study



Voltage Drop Analysis Setup -> Set up Sinks

Assign | Tolerance | %

	Sink Name	Model	Nominal Voltage (V)	Power/Ground Net	Upper Tolerance(+%)	Lower Tolerance(-%)	P/F Mode	Current (A)
☑	SINK_CN3_P12V_GND	**Equal Current**	12	**P12V_GND**	1	**1**	Worst	**105**
☑	SINK_CN2_P12V_GND	**Equal Current**	12	**P12V_GND**	1	**1**	Worst	**105**

Equal Current

If the model is selected, equal currents will flow through all the layout nodes connected with the same pin of a SINK.

Actual Voltage

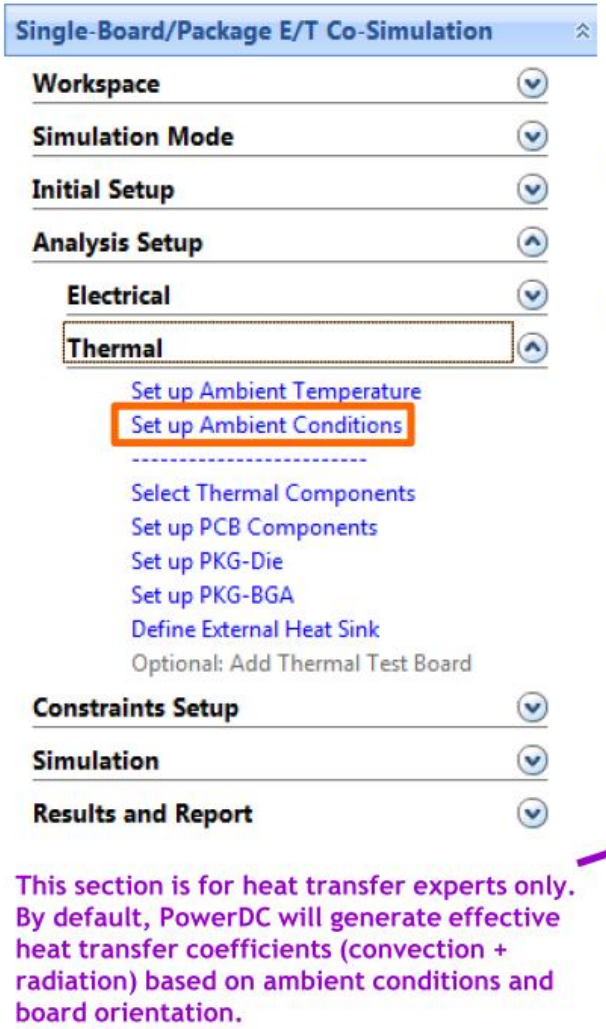
For Equal and Unequal Current model, a voltage value is computed for each layout node. Layout nodes connected with the same pin may have different voltages. The Actual Voltage of the SINK is calculated based on Pass/Fail(P/F) mode.

Voltage Drop Analysis Setup -> Set up Sinks

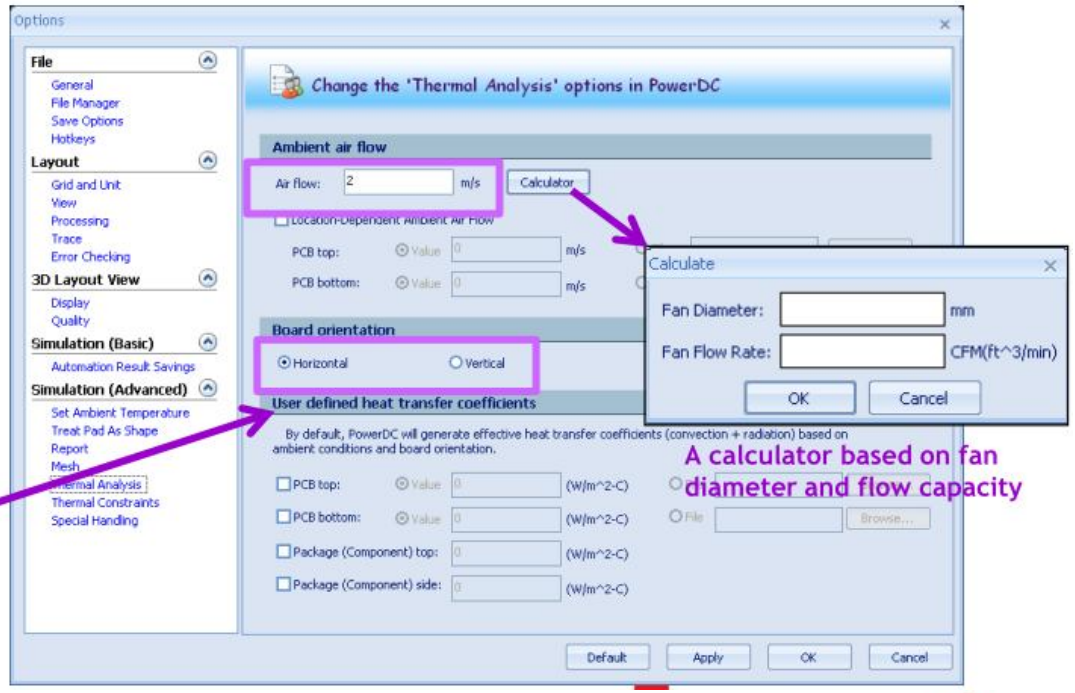
Assign | Tolerance | %

	Sink Name	Model	Nominal Voltage (V)	Power/Ground Net	Upper Tolerance(+%)	Lower Tolerance(-%)	P/F Mode	Current (A)
☑	SINK_CN3_P12V_GND	**Equal Voltage**	12	**P12V_GND**	1	**1**	Not In Use	**105**
☑	SINK_CN2_P12V_GND	**Equal Voltage**	12	**P12V_GND**	1	**1**	Not In Use	**105**

Simple structure design case study



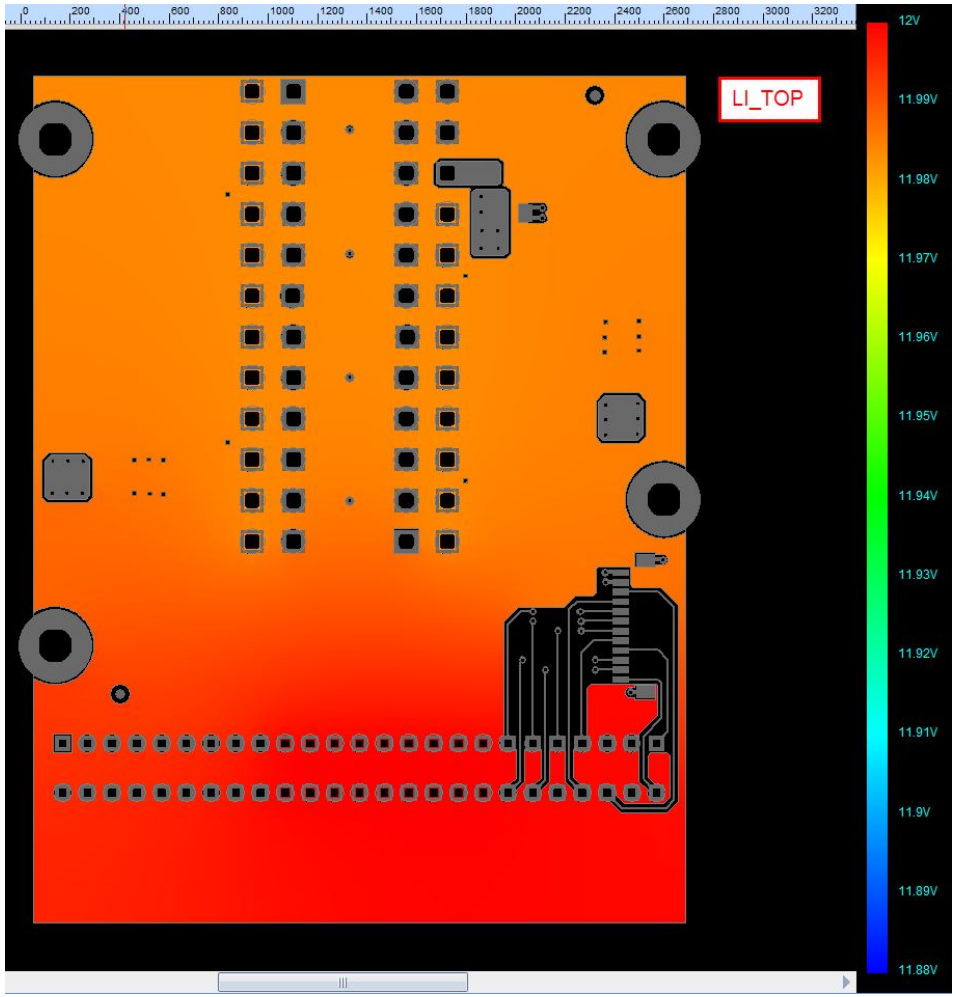
- Objective: Setup ambient air flow and board orientation.
- Explanation: Ambient air flows and board orientation will affect heat transfer.
- Procedure: Fill the menu (see blow).

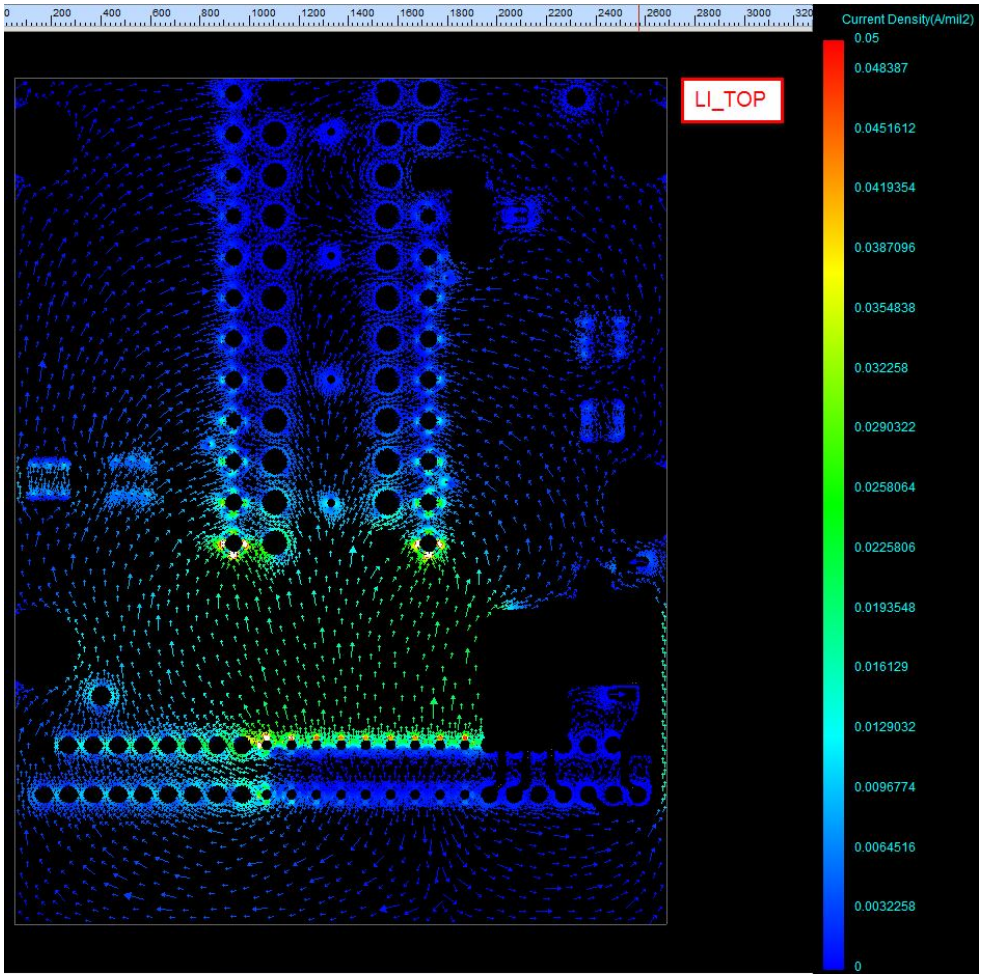


This section is for heat transfer experts only. By default, PowerDC will generate effective heat transfer coefficients (convection + radiation) based on ambient conditions and board orientation.

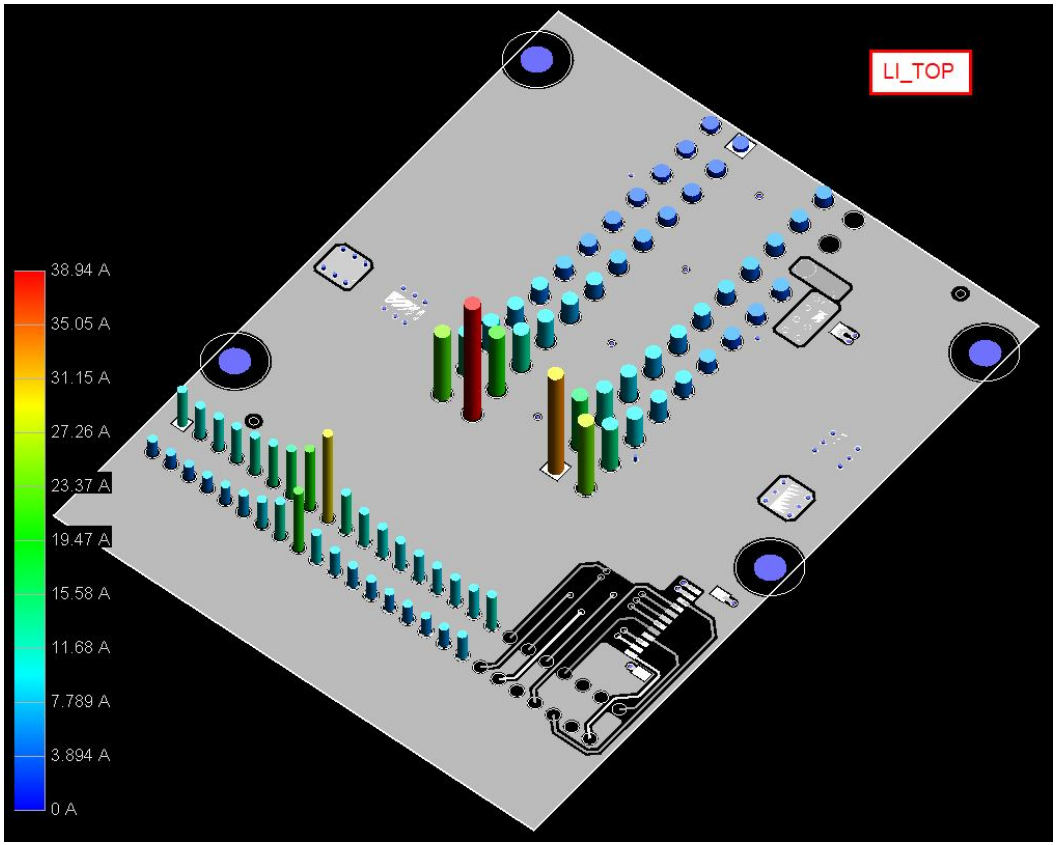
A calculator based on fan diameter and flow capacity

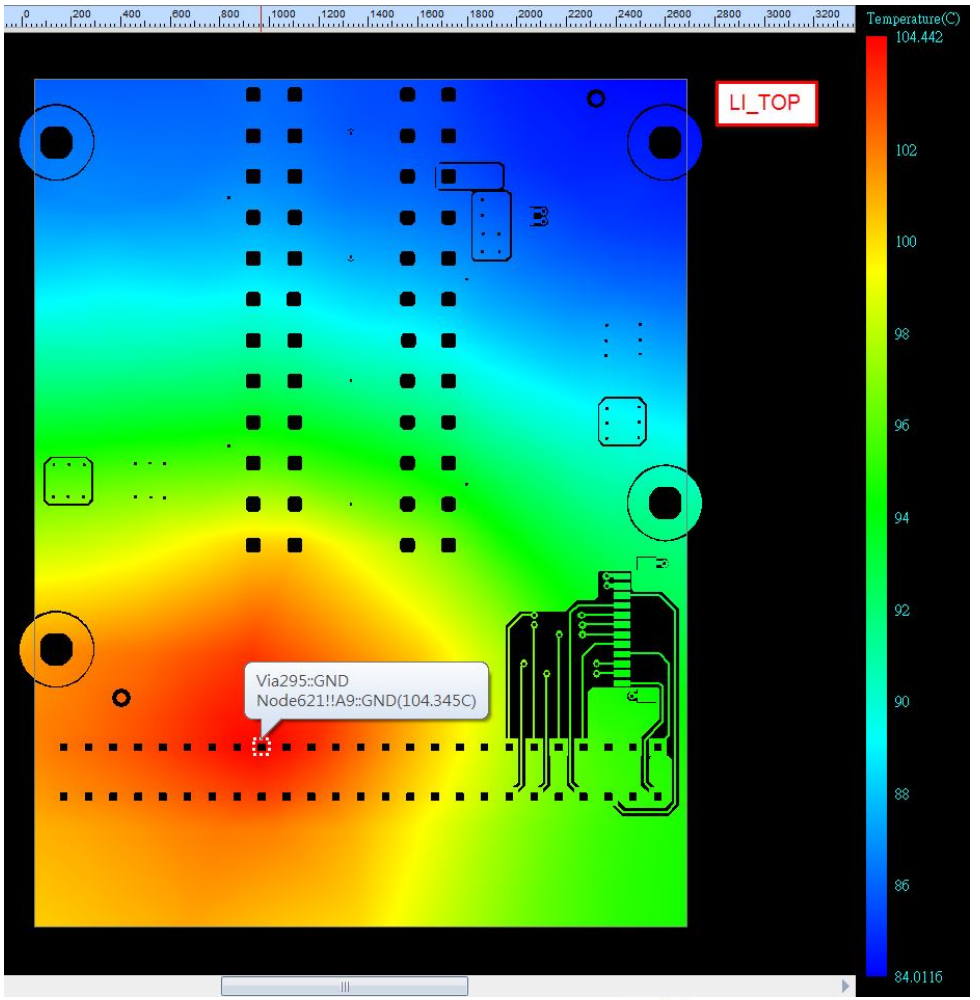
Simple structure design case study



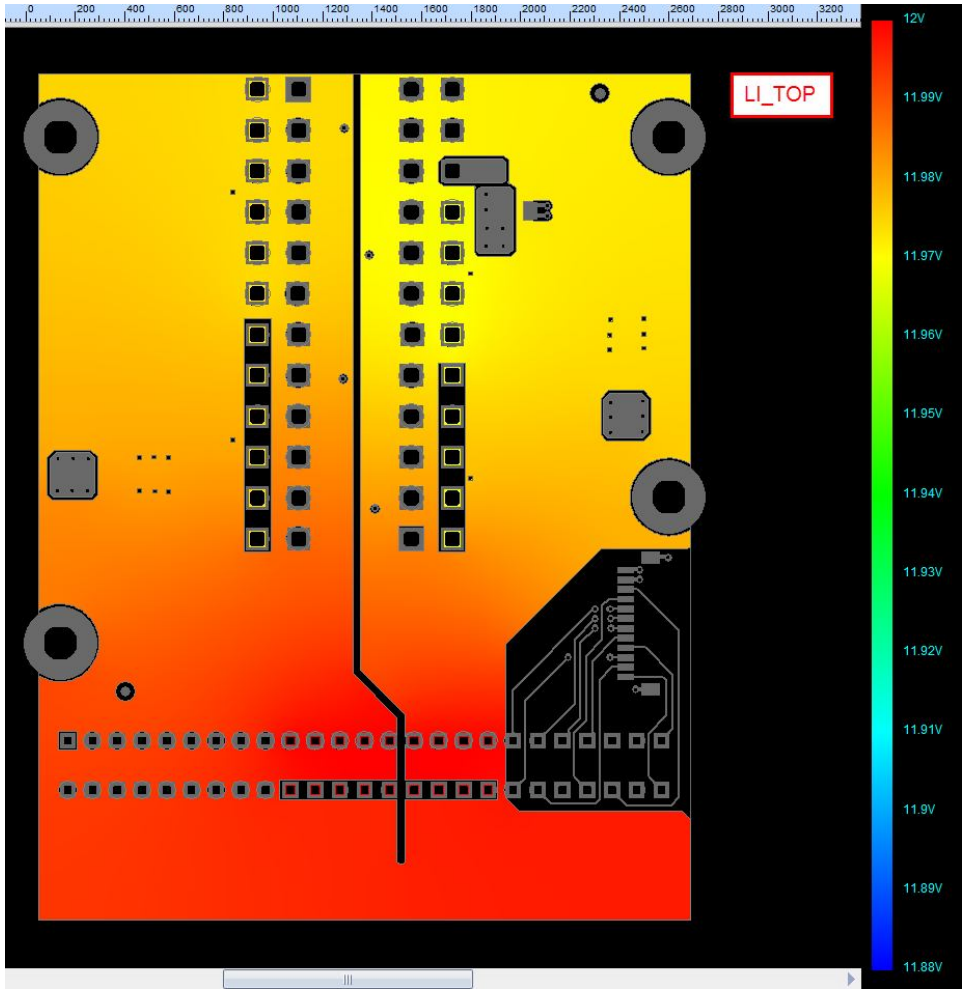


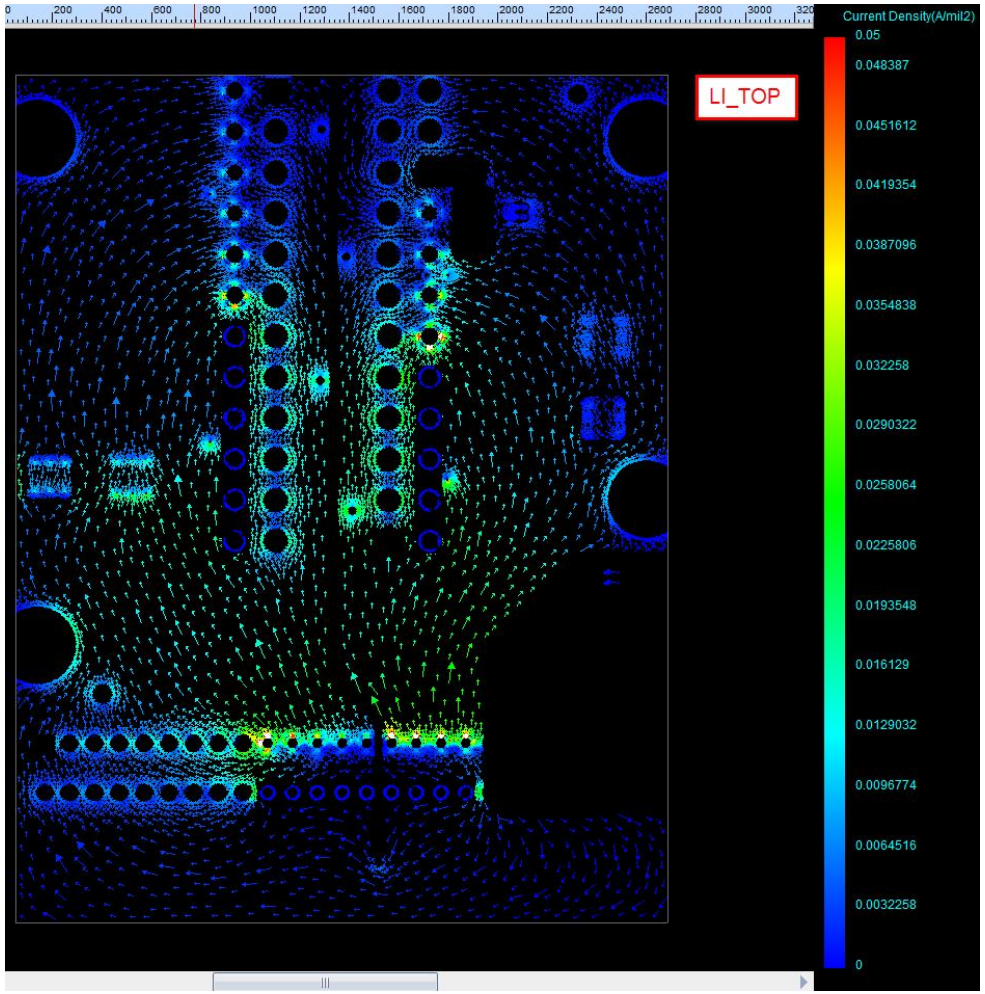
Simple structure design case study



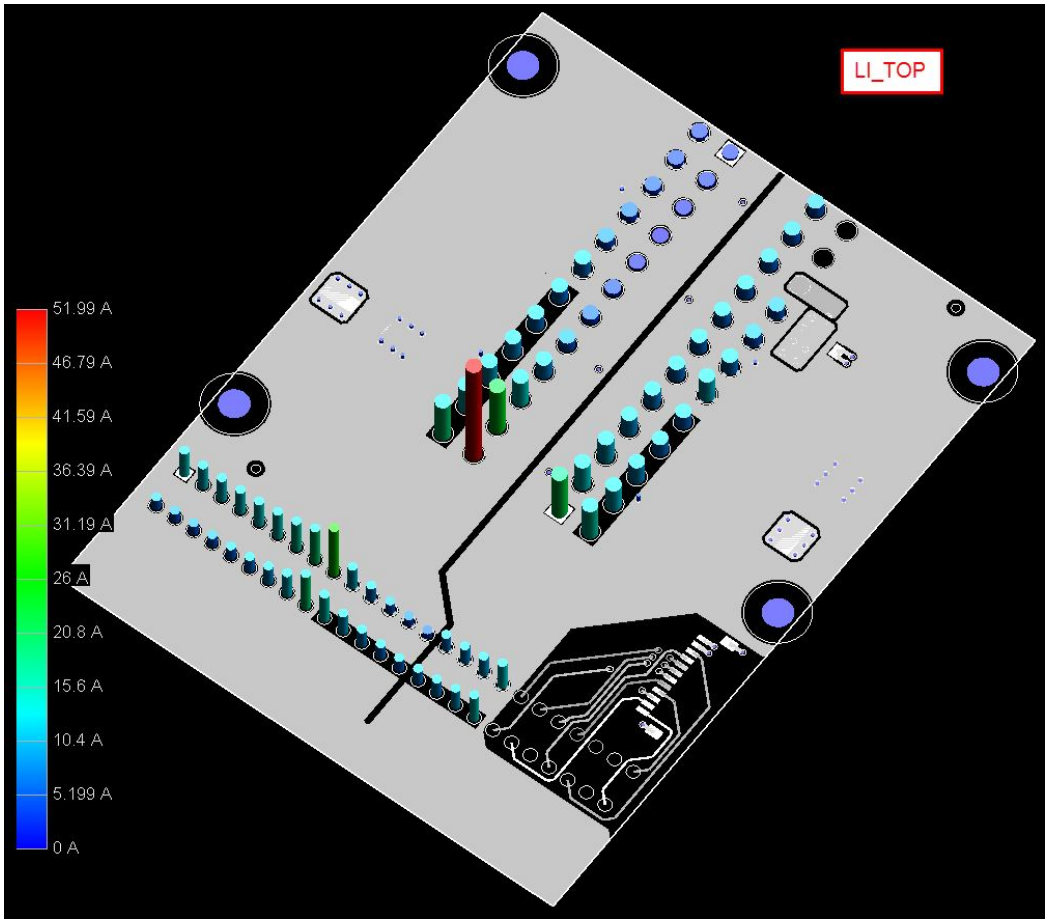


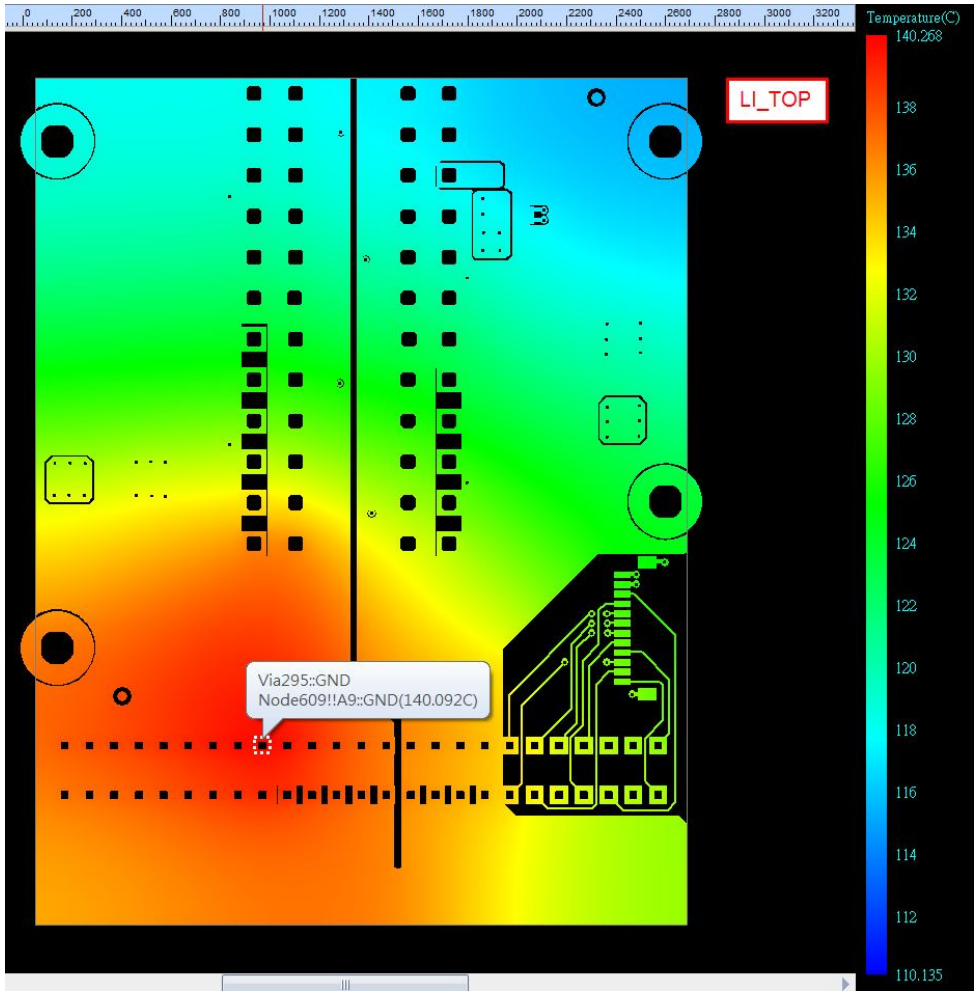
Simple structure design case study



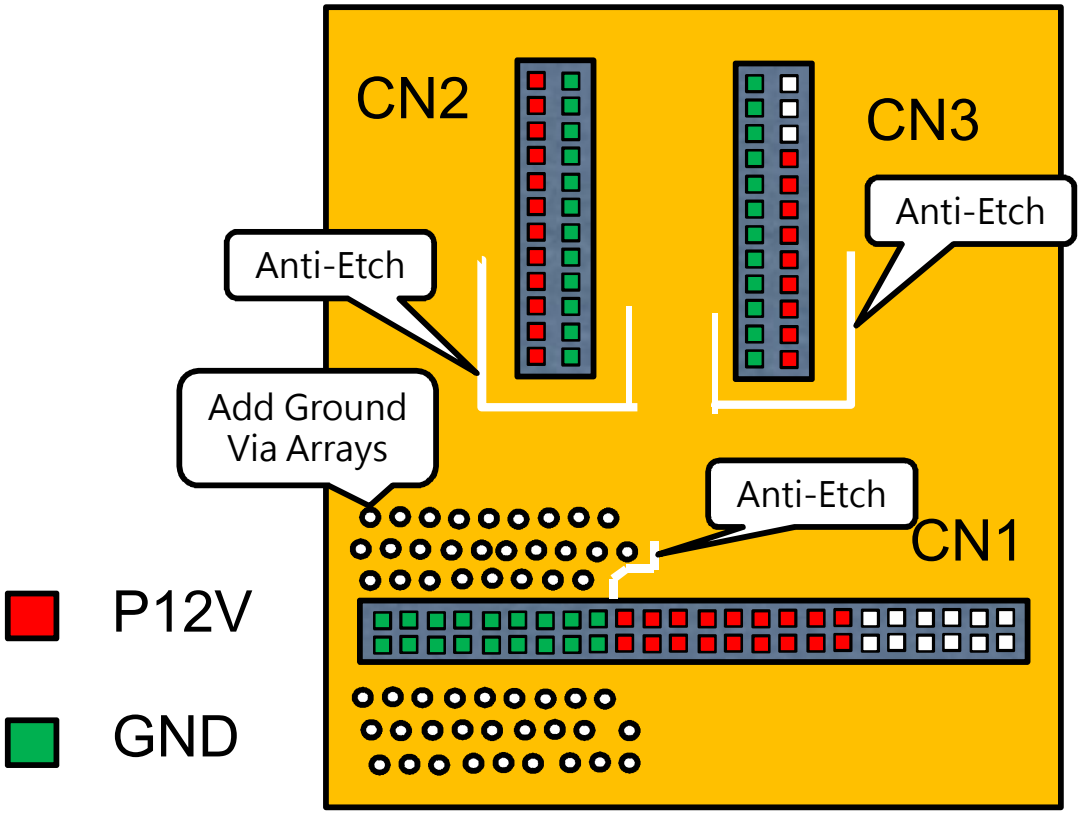


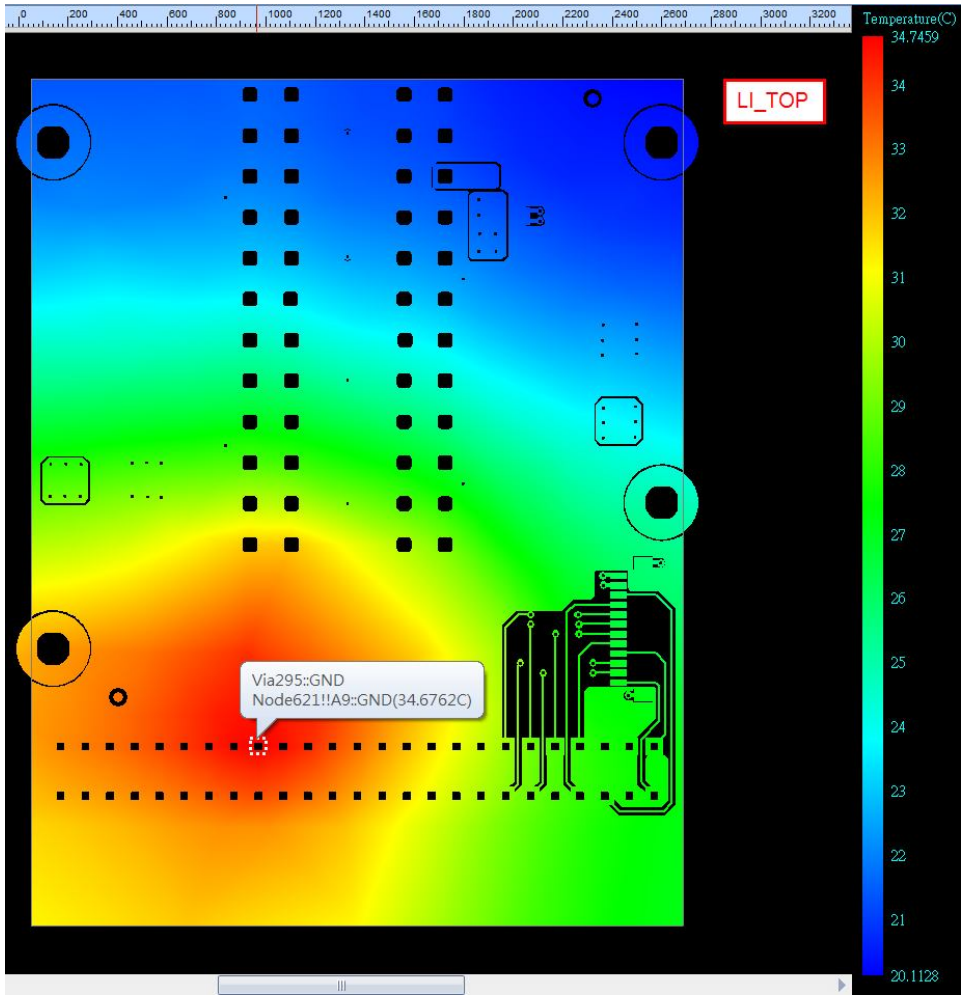
Simple structure design case study





Simple structure design case study





Abstract

- Power integrity concept
- Why is DC analysis important?
- Rule of thumb in DC analysis
- Simple structure design case study
- Summary

Summary

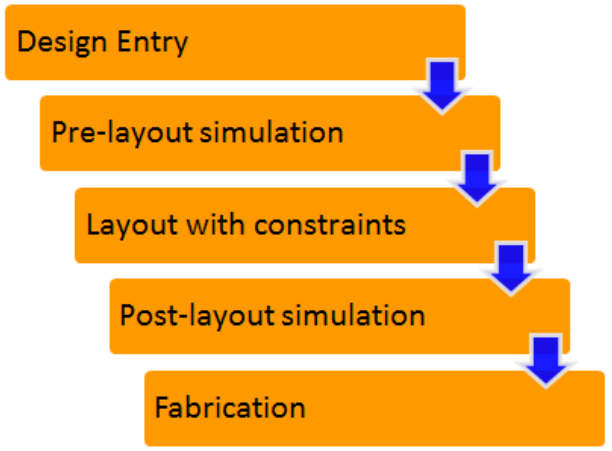
1. The following DC analyses are described as necessary verification items. Missing one or more analyses may degrade the system performance and lead to the product failure.

(a) Actual DC voltages at devices with thermal effect
(b) Current density and temperature on metal
(c) Current carrying capability of interconnect
(d) Power and ground pin effectiveness

2. The HTML report can be used as the design checking and reference.

Traditional design process

Simultaneous design process



Thanks for your attention~