



Potential Power Delivery Network Issue In The Simple Structure Design

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2015/10/08



ADLINK
TECHNOLOGY INC.

Abstract

- Power integrity concept
- Why is DC analysis important?
- Rule of thumb in DC analysis
- Simple structure design case study
- Summary

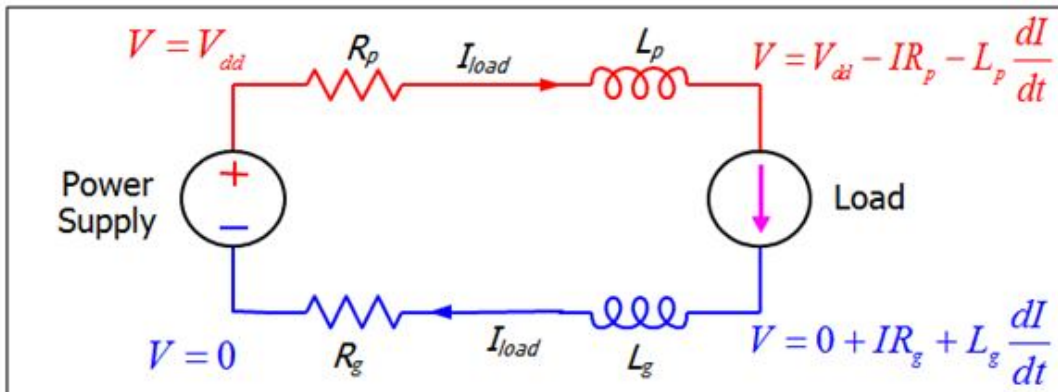
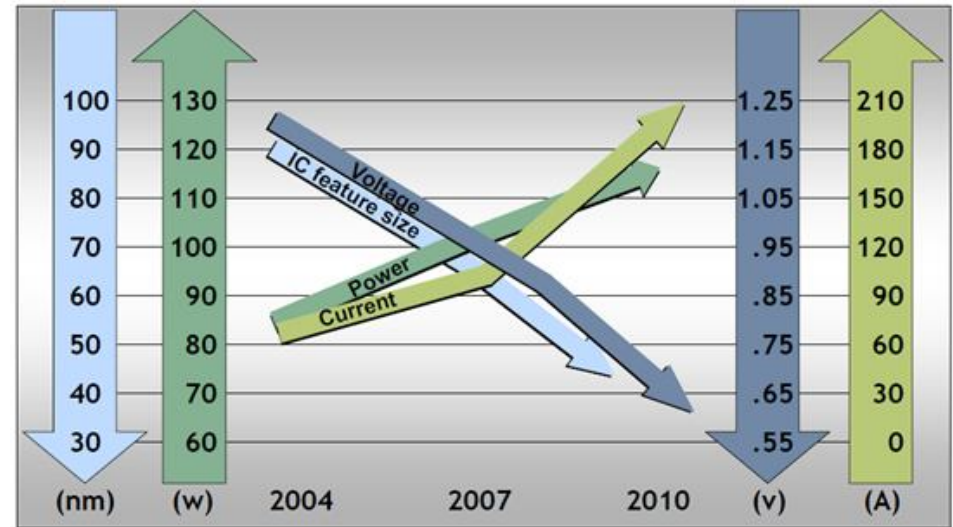
Power Integrity Concept

What is best **DC** power plane performance?

- Devices see voltage closet to nominal voltage
 - ✓ Low IR drop
 - ✓ Well balanced DC voltages among devices on the same rail
- Low Temperature Rise on Metal
 - ✓ Low Current Density
- Power Efficiency
 - ✓ Low Power Loss

What is best **AC** power plane performance?

- Low noise
 - ✓ Low loop inductance
 - ✓ Low and Flat impedance



The resistance R_s of a plane conductor for a unit length and unit width is called the **surface resistivity** (ohms per square).

$$R_s = \frac{1}{\sigma \cdot t} = \frac{\rho}{t}$$

$$R = R_s \cdot \frac{l}{w}$$

Obstacles: Power lines are not ideal and have finite resistance and inductance

◆ Resistive noise $V_R = IR$

- Caused by high transient currents drawn by the load

◆ Inductive noise $V_L = L di/dt$

- Caused by high current slew rates di/dt produced by the load

Power Integrity Concept

Power Integrity Concept

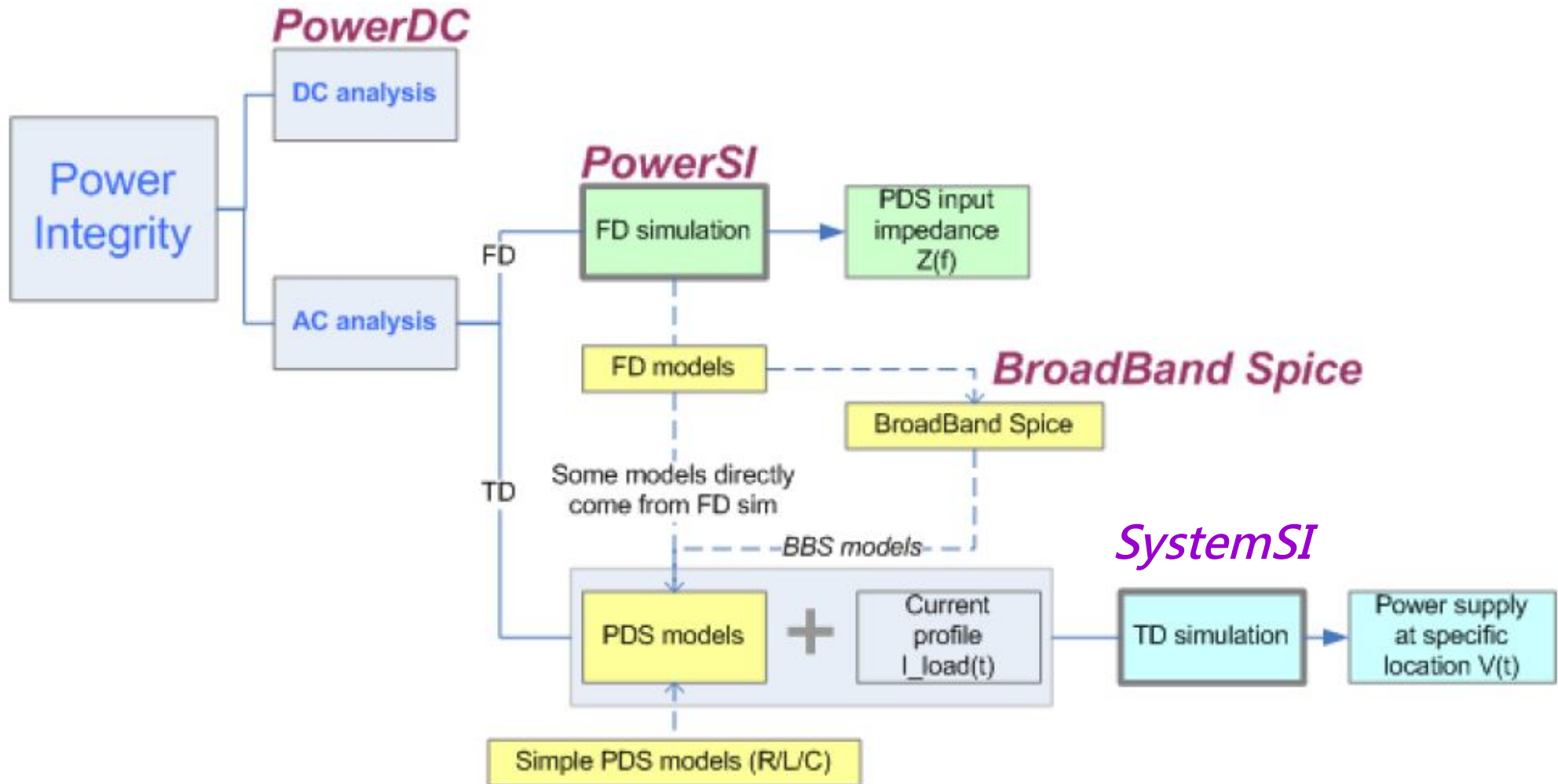
If the analysis result is fail, how's the impact?

DC Analysis	AC Analysis
<ol style="list-style-type: none">1. Add Layers2. Add trace Width3. Location of VRM and Sense4. VIA numbers and location <p>→ Change the geometry of the Power Distribution System</p>	<ol style="list-style-type: none">1. Add Capacitors<ul style="list-style-type: none">→ Modify the Schematics→ Modify the location of capacitors2. Modify the layers:<ol style="list-style-type: none">i. Floor planningii. Shape geometry <p>→ Change the geometry of the Power Distribution System</p>

To speed up the design procedure and reduce the frequency of modifying the PDS's geometry, we will frozen the PDS's geometry after the DC Analysis and simply modify the capacitor's size, number and location of capacitors, that is:



Power Integrity Concept



Abstract

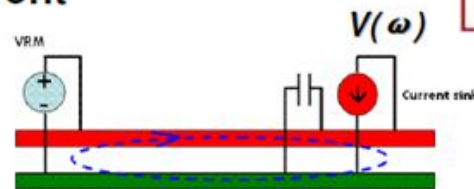
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Why Is DC Analysis Important?

Voltage droop while chip sinks current

$$\Delta V(\omega) = Z_{input}(\omega)I(\omega) + IR(\omega=0)$$

AC term DC term

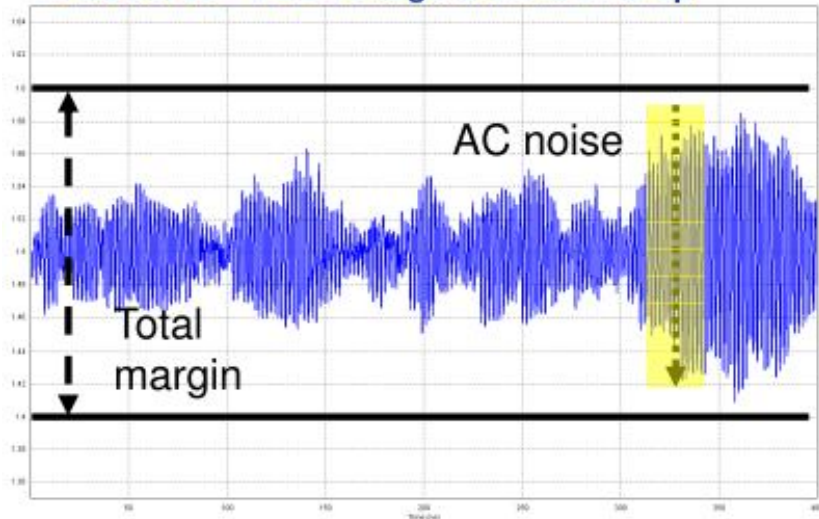


IRdrop	:	AC noise
20	:	80 (typical)
10	:	90 (aggressive on DC)

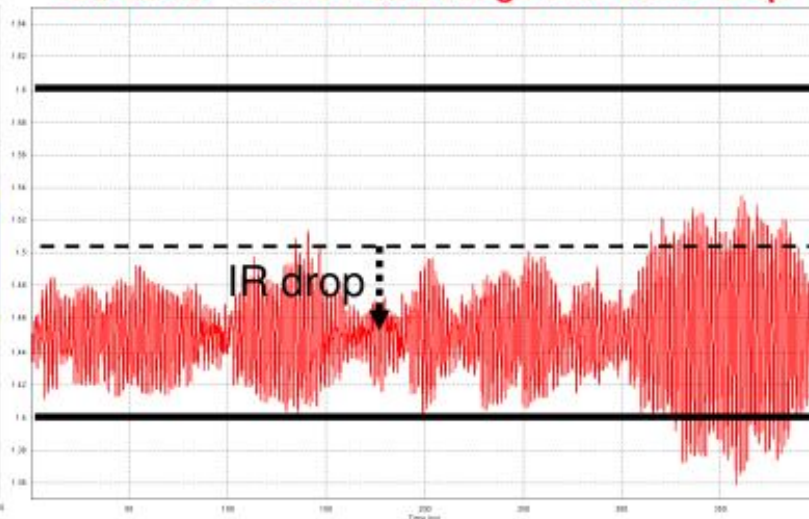
VDD = +1.5V +/- 5%

IRdrop : AC noise	=	20:80
IRdrop	=	+1.5V +/-1%
AC noise	=	+1.5V +/-4%

Blue curve – PDS voltage with no IR drop



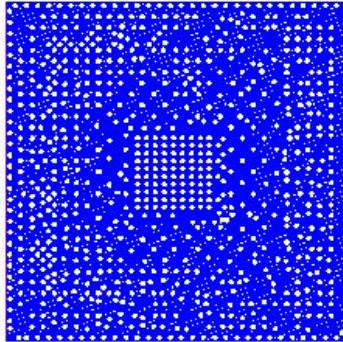
Red curve – Same PDS voltage with 50mV drop



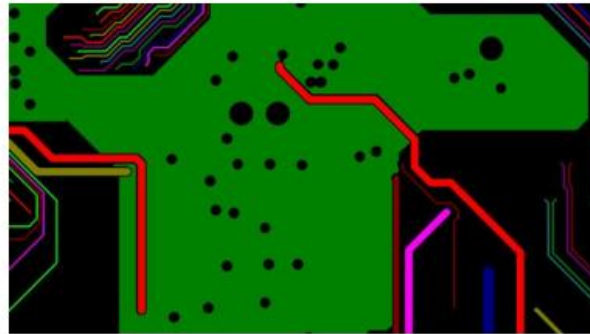
Why Is DC Analysis Important?



Neck-down

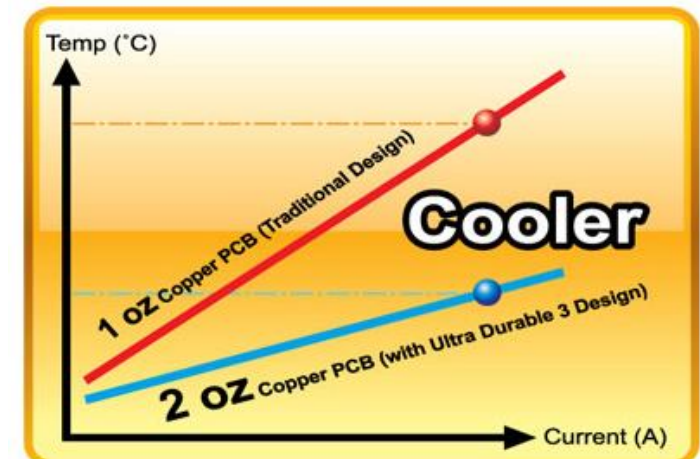
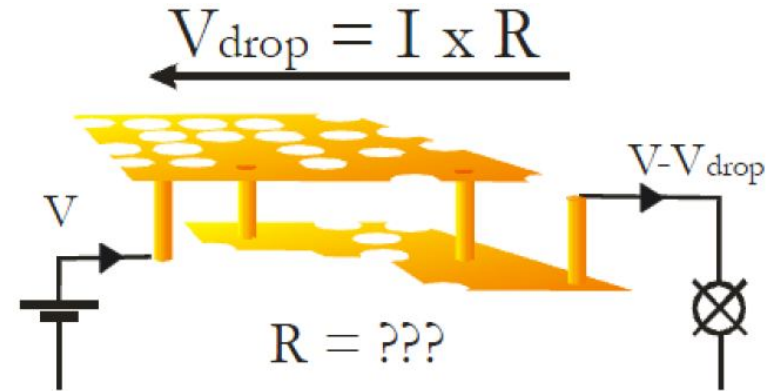


Swiss Cheese on solid plane



Dynamic trace routing can cut off the PDS

- IR Drop is a system level problem - analysis of the entire power distribution system (PDS) is necessary to optimize the end-to-end voltage margins for every device on the distribution

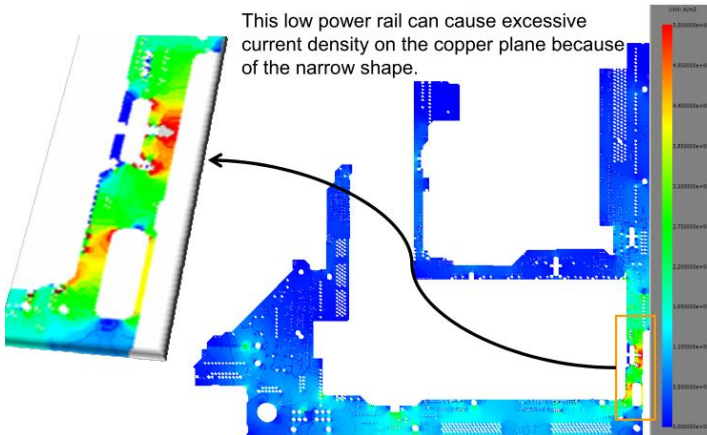


CPU VRM Temperature measurements under system setup with water-cooler block and CPU running at 100% loading

Why Is DC Analysis Important?

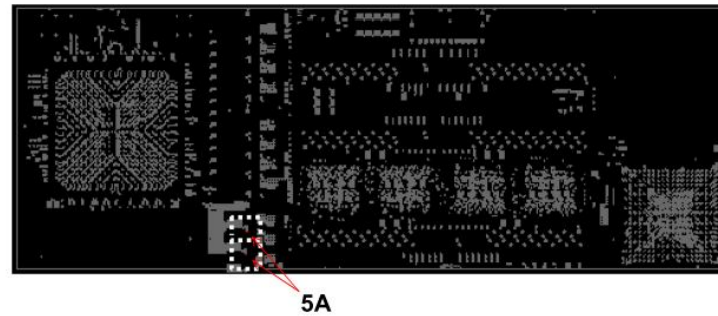
Localize Heat in low power net

This low power rail can cause excessive current density on the copper plane because of the narrow shape.



Excessive IR drop due to narrow and long traces

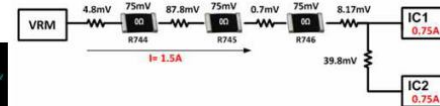
Identify vias that have high current flow. Via Current plot can be used to pinpoint vias with high current flow.



Excessive IR drop due to DC resistance on passive components

Show Results -> Voltage, Current & Resistance Tables (2 of 8 Failed)

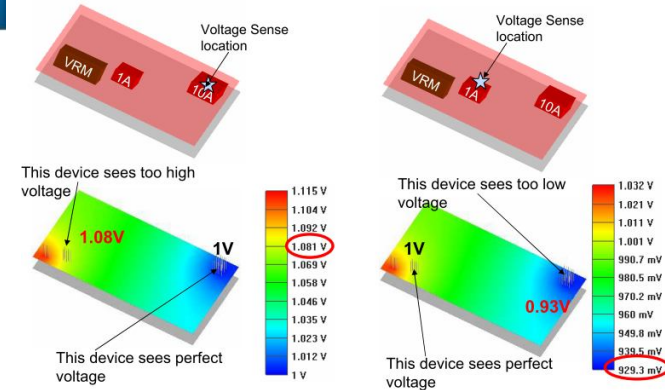
Sink Name	Model	Nominal Voltage (V)	Input Tolerance (%)	Actual Voltage (V)	Margin (V)
IC2	Equal Current	2.600000e+000	2.000000e+000	2.230338e+000	-3.176616e-001
IC1	Equal Current	2.600000e+000	2.000000e+000	2.270782e+000	-2.772185e-001



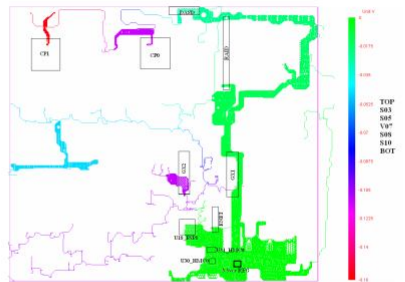
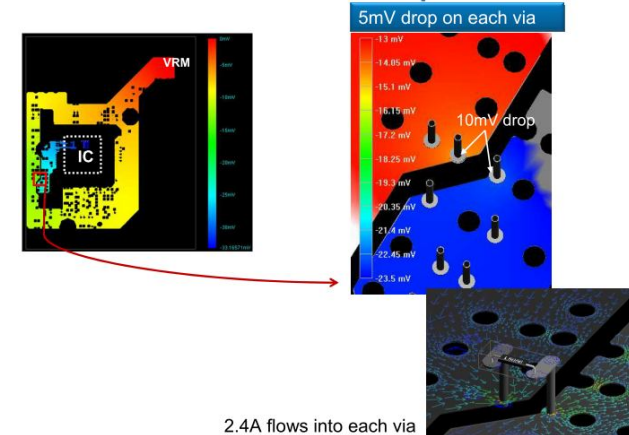
There is no such thing as zero ohm resistor.

Maximum Continuous Current @ 70 °C	Maximum Surge Current @ 70 °C	Maximum Resistance
0.5 Amps	1.0 Amp Max. for < 1 second	50mΩ
0.5 Amps	1.0 Amp Max. for < 1 second	
1.0 Amps	2 Amp Max. for < 1 second	50mΩ
2.0 Amps	5 Amp Max. for < 1 second	
2.0 Amps	10 Amp Max. for < 1 second	

Where to place the Sense Line when there are more than one device on the power rail?



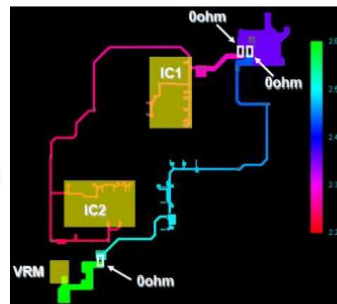
Excessive IR drop on vias



Functional problem can be caused by too much IR drop even in the low power.

IR drop target is 66mV

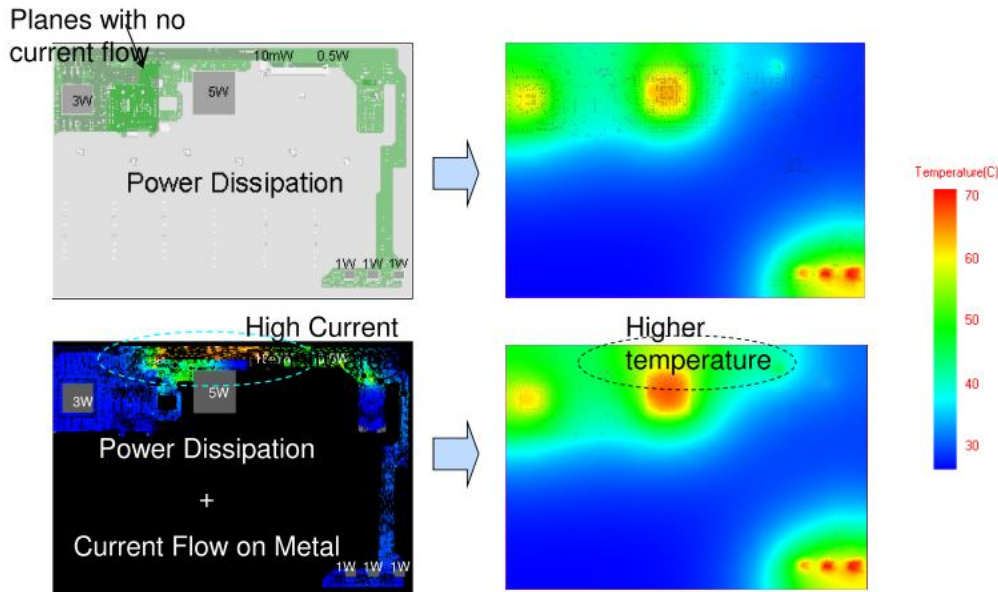
← 159% over the target



criteria	refdes	Brief description	Max current (A)	IR drop (mV)
03.3VCS	U3_CPI1	PE	0.250	-169
	U2_CPI0	PE	0.250	-115
	J24_DASD	DASD CARD	0.218	-113
	J24_DASD	DASD backplane	0.218	-111
	U19_RAM0	RAM0 card	0.008	-13
	U19_ESP1	FSP1 chip	0.51	-2.0
	J25_ENET0	ENET card	0.008	-1.4
	U31_HMC0	HMC chip	0.012	-1.2
	U30_HMC0	HMC chip	0.012	-1.0

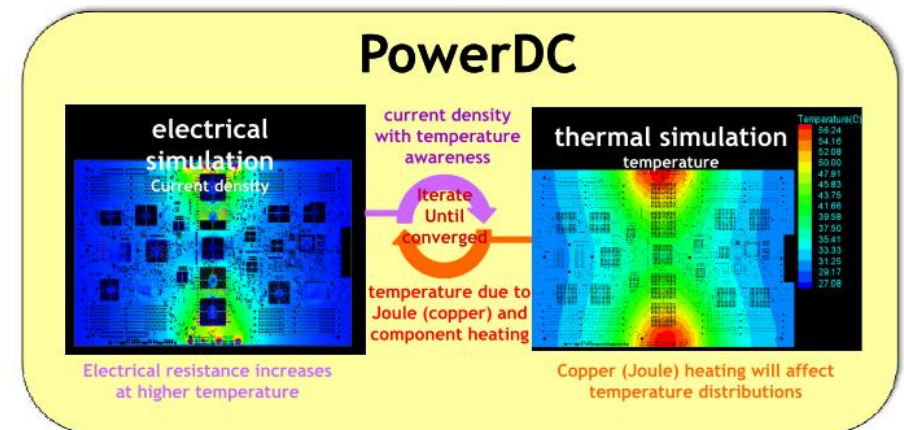
Why Is DC Analysis Important?

Electrical affects Thermal

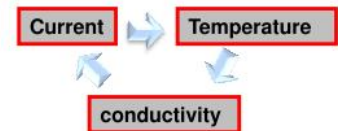


- Temperature increases due to joule heating from current flowing through a conductor
- Without electrical effect, thermal result is under-estimated

Electrical/Thermal Co-Simulation in One Integrated Tool



Integrated **electrical/thermal** co-simulation provides engineers with efficient design margins and lower manufacturing costs.



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Rule Of Thumb In DC Analysis

The screenshot displays the Saturn PCB Design software interface for a DC analysis. The interface is divided into several sections:

- Conductor Characteristics:**
 - Solve For: Amperage, Conductor Width
 - Plane Present?: No, Yes
 - Parallel Conductors?: No, Yes
 - Conductor Width: 20 mils
 - Conductor Length: 1000 mils
 - PCB Thickness: 63 mils
 - Frequency: DC (checked)
 - Parallel Conductor Count: 2
- Options:**
 - Base Copper Weight: 0.7 mils
 - Plating Thickness: 1.2 mils
 - Plane Thickness: 1oz, 2oz
 - Conductor Layer: External Layer, Internal Layer
 - Units: Imperial, Metric
 - Substrate Options: Material Selection: FR-4 STD
 - Er: 4.6, Tg (°C): 130
 - Temp Rise (°C): 10
 - Ambient Temp (°C): 25
- Results:**
 - IPC-2152 with modifiers mode, Etch Factor: None
 - Power Dissipation: 0.02601 Watts
 - Power Dissipation in dBm: 14.1518 dBm
 - Voltage Drop: 0.0222 Volts
 - Conductor DC Resistance: 0.01891 Ohms
 - Total Cross Section: 76.00 Sq.mils
 - Conductor Current: 1.1727 Amps
 - Conductor Temperature: Temp in (°C) = 35.0, Temp in (°F) = 95.0
 - Information: Total Copper Thickness: 1.90 mils, VIA Thermal Resistance: N/A, VIA Voltage Drop: N/A

The Saturn PCB Design, Inc. logo and social media icons are visible at the bottom left of the interface.

Rule Of Thumb In DC Analysis

Conductor Characteristics

Solve For
 Amperage Conductor Width

Plane Present?
 No Yes

Parallel Conductors?
 No Yes

Parallel Conductor Count: 2

Conductor Width: 25 mils

Conductor Length: 1000 mils

PCB Thickness: 63 mils

Frequency: DC

Options

Base Copper Weight: 1.4 mils

Units: Imperial Metric

Substrate Options
Material Selection: FR-4 STD
Er: 4.6 Tg (°C): 130

Plating Thickness: 1.2 mils

Temp Rise (°C): 10
Temp in (°F) = 18.0

Ambient Temp (°C): 25
Temp in (°F) = 77.0

Plane Thickness: 1oz 2oz

Conductor Layer: Internal Layer External Layer

Information

Total Copper Thickness: 1.40 mils
Conductor Temperature: Temp in (°C) = 35.0
Temp in (°F) = 95.0

VIA Thermal Resistance: N/A
VIA Voltage Drop: N/A

Power Dissipation: 0.02507 Watts
Power Dissipation in dBm: 13.9911 dBm
Voltage Drop: 0.0227 Volts

Conductor DC Resistance: 0.02053 Ohms
Total Cross Section: 70.00 Sq.mils
Conductor Current: 1.1049 Amps

IPC-2152 with modifiers mode Etch Factor: None

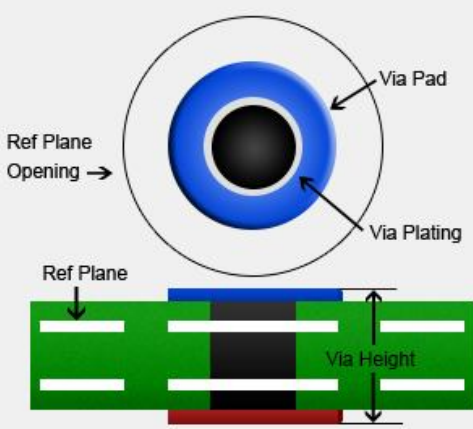


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Rule Of Thumb In DC Analysis

Via Characteristics



Options

Base Copper Weight: 1.4 mils

Units: Imperial, Metric

Substrate Options: Material Selection: FR-4 STD

Er: 4.6, Tg (°C): 130

Plating Thickness: 1.2 mils

Plane Thickness: 1oz, 2oz

Layer Set: 2 Layer, Multi Layer, Microvia

Temp Rise (°C): 10

Temp in (°F) = 18.0

Ambient Temp (°C): 25

Temp in (°F) = 77.0

Print Solve!

Information

Power Dissipation in dBm: 4.6090 dBm

VIA Thermal Resistance: 182.1592 Deg C/Watt

Via Temperature: Temp in (°C) = 35.0, Temp in (°F) = 95.0

VIA Voltage Drop: 1.9459 mV

IPC-2152 with modifiers mode

Via Capacitance	Via DC Resistance	Power Dissipation
0.8172 pF	0.00131 Ohms	0.00289 Watts
Via Inductance	Resonant Frequency	Conductor Cross Section
1.3528 nH	4786.703 MHz	34.5575 Sq.mils
Via Impedance	Step Response	Via Current
40.685 Ohms	36.5744 ps	1.4852 Amps

SATURN PCB DESIGN, INC. Turnkey Electronic Engineering Solutions

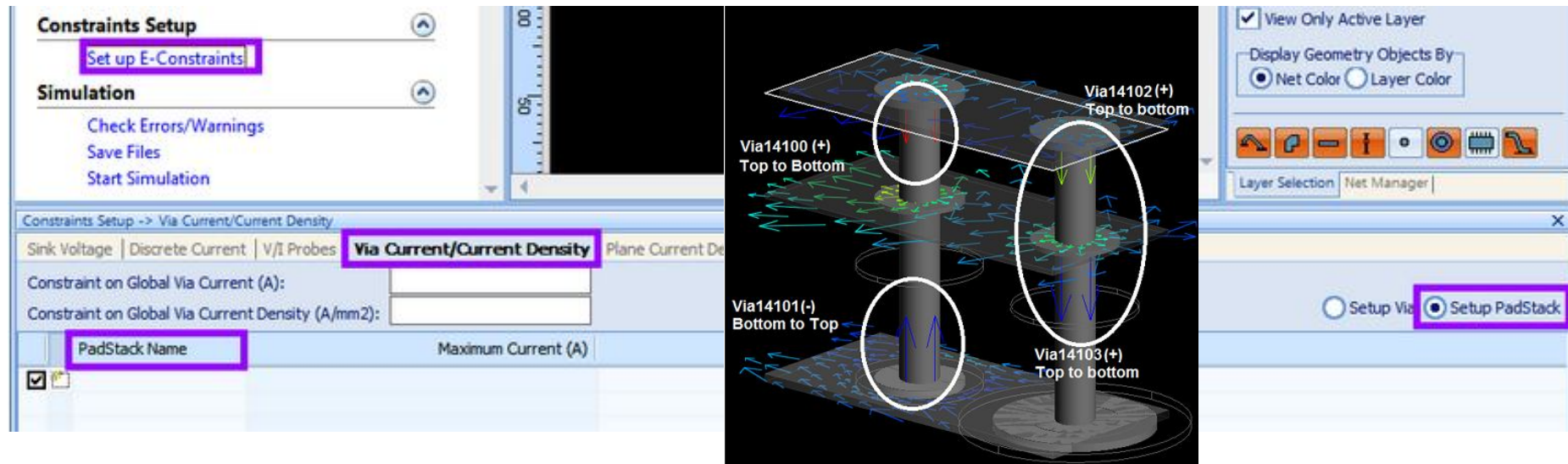
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Rule Of Thumb In DC Analysis

The numbers were extracted from [IPC-2152](#), for **1mil** plating thickness and no copper planes. If copper planes are present, then the temperature rise will be lower.

Via size (mil)	Current for 10°C temp rise (A)	Current for 30°C temp rise (A)	Current for 45°C temp rise (A)
8	1.2	2	2.3
10	1.4	2.3	2.8
12	1.6	2.6	3.2
16	1.8	3.1	3.8
20	2.1	3.6	4.3
30	2.7	4.6	5.7
40	3	5.5	6.8

Rule Of Thumb In DC Analysis



Your constraint and actual current will be displayed in the *Global Via Current* tab of the Results table:

Results and Report -> Global Via Current (7 of 7 Failed)																			
Other Component Voltage		Power Loss		Probes Measurements		Global Via Current		Global Via Current Density		Specific Via Current		Global Plane Current Density		Specific Plane Current Density		Trace Current Density		Wire	
Via Name	Net	PosX (mm)	PosY (mm)	StartLayer	Upper Node	EndLayer	Lower Node	PadStack	Maximum Current (A)	Actual Current (A)									
Via14095::+...	+1.5V	274.32	213.36	Signal\$TOP	Node96515::+...	Signal\$L1	Node96516::+...	VIA-22-10HOLE	0.5	1.2532									
Via14097::+...	+1.5V	274.32	212.09	Signal\$TOP	Node96517::+...	Signal\$L1	Node96518::+...	VIA-22-10HOLE	0.5	0.715189									
Via14100::+...	+1.5V	273.05	213.36	Signal\$TOP	Node96520::+...	Signal\$L1	Node96521::+...	VIA-22-10HOLE	0.5	1.96813									
Via14102::+...	+1.5V	273.05	212.09	Signal\$TOP	Node96522::+...	Signal\$L1	Node96523::+...	VIA-22-10HOLE	0.5	1.26348									
Via38873::GND	GND	272.415	215.773	Signal\$TOP	Node5037::GND	Signal\$BOTT...	Node90269::GND	VIA-22-10HOLE0	0.5	-0.832212									
Via38877::GND	GND	273.685	214.757	Signal\$TOP	Node5036::GND	Signal\$BOTT...	Node90285::GND	VIA-22-10HOLE0	0.5	-0.825979									
Via38878::GND	GND	272.415	214.757	Signal\$TOP	Node5035::GND	Signal\$BOTT...	Node90289::GND	VIA-22-10HOLE0	0.5	-2.56298									

Abstract

- Power integrity concept
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Simple structure design case study

Single-Board/Package E/T Co-Simulation

Workspace




- Create New Single-Board Workspace
- Load Existing Single-Board Workspace

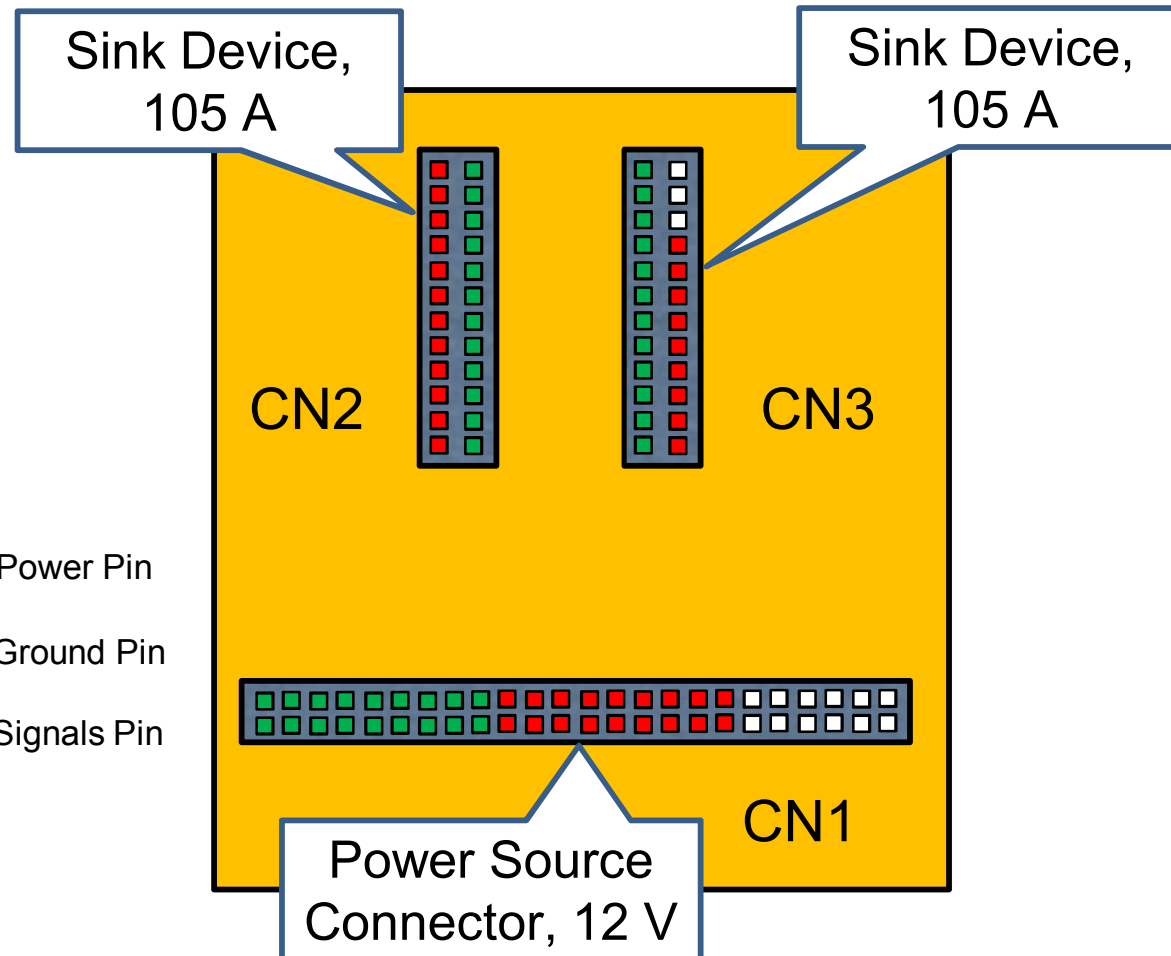
Simulation Mode

- Enable E/T Co-Simulation Mode
- Enable Thermal-Only Mode

Initial Setup

- Load a New/Different Layout
- Check Stackup
- Set up P/G Nets
- Launch Analysis Model Manager

-  Power Pin
-  Ground Pin
-  Signals Pin



Simple structure design case study

Layer Manager -> Stack Up

Layer #	Color	Layer Icon	Layer Name	Thickness(mil)	Material	Conductivity(S/m)	Fill-in Dielectric	Er	Loss Tangent
1			Signal\$TOP	2.3	copper		FR4		
2			Medium\$medium42	6.5	FR4	0			
3			Signal\$L2_GND	2.4	copper		FR4		
4			Medium\$medium44	11.8	FR4	0			
5			Signal\$L3_PWR	2.4	copper		FR4		
6			Medium\$medium46	9.5	FR4	0			
7			Signal\$L4_PWR	2.4	copper		FR4		
8			Medium\$medium48	11.8	FR4	0			
9			Signal\$L5_GND	2.4	copper		FR4		
10			Medium\$medium50	6.5	FR4	0			
11			Signal\$BOTTOM	2.3	copper		FR4		
12			Medium\$medium52	0.7	FR4	0			

Total Thickness: 6.1700e+001 mil

Unit: mil

Layer Manager -> Pad Stack (C62D44)

PadStacks	Xsection View	Layer	PadTyp	Shape	Width	Height	OffsetX
~DefaultPadStack							
C40_FM_80		DefaultLibL...	Regu...	Circle	62	62	
C62D44			Anti	Circle	74	74	
C90D72			Ther...				
C295D142							
RECT24X61							
RECT32X35							
RECT47X71							
RECT65X50							
Signal\$TOP			Regu...	Circle	62	62	

Outer diameter: 44 mil

Plating thickness: 1 mil

Conductivity: S/m Use default conductivity

Select material: copper

Global Plating Thickness:

Unit: mil

Set the plating thickness is important for IR drop analysis.

Set the material is important for thermal analysis.

Simple structure design case study

Single-Board/Package E/T Co-Simulation

Workspace

Simulation Mode

Initial Setup

Analysis Setup

Electrical

Set up VRMs

Set up Sinks

Set up Discretés

Set up Ref Node, etc.

Thermal

Constraints Setup

Simulation

Results and Report

Voltage Drop Analysis Setup -> Set up Sinks

Assign	Tolerance	%	Sink Name	Model	Nominal Voltage (V)	Power/Ground Net	Upper Tolerance(+%)	Lower Tolerance(-%)	P/F Mode	Current (A)
<input checked="" type="checkbox"/>			SINK_CN3_P12V_GND	Equal Current	12	P12V_GND	1	1	Worst	105
<input checked="" type="checkbox"/>			SINK_CN2_P12V_GND	Equal Current	12	P12V_GND	1	1	Worst	105

Equal Current

If the model is selected, equal currents will flow through all the layout nodes connected with the same pin of a SINK.

Actual Voltage

For Equal and Unequal Current model, a voltage value is computed for each layout node. Layout nodes connected with the same pin may have different voltages. The Actual Voltage of the SINK is calculated based on Pass/Fail(P/F) mode.

Assign	Tolerance	%	Sink Name	Model	Nominal Voltage (V)	Power/Ground Net	Upper Tolerance(+%)	Lower Tolerance(-%)	P/F Mode	Current (A)
<input checked="" type="checkbox"/>			SINK_CN3_P12V_GND	Equal Voltage	12	P12V_GND	1	1	Not In Use	105
<input checked="" type="checkbox"/>			SINK_CN2_P12V_GND	Equal Voltage	12	P12V_GND	1	1	Not In Use	105

Simple structure design case study

Single-Board/Package E/T Co-Simulation

Workspace

Simulation Mode

Initial Setup

Analysis Setup

Electrical

Thermal

Set up Ambient Temperature

Set up Ambient Conditions

Select Thermal Components

Set up PCB Components

Set up PKG-Die

Set up PKG-BGA

Define External Heat Sink

Optional: Add Thermal Test Board

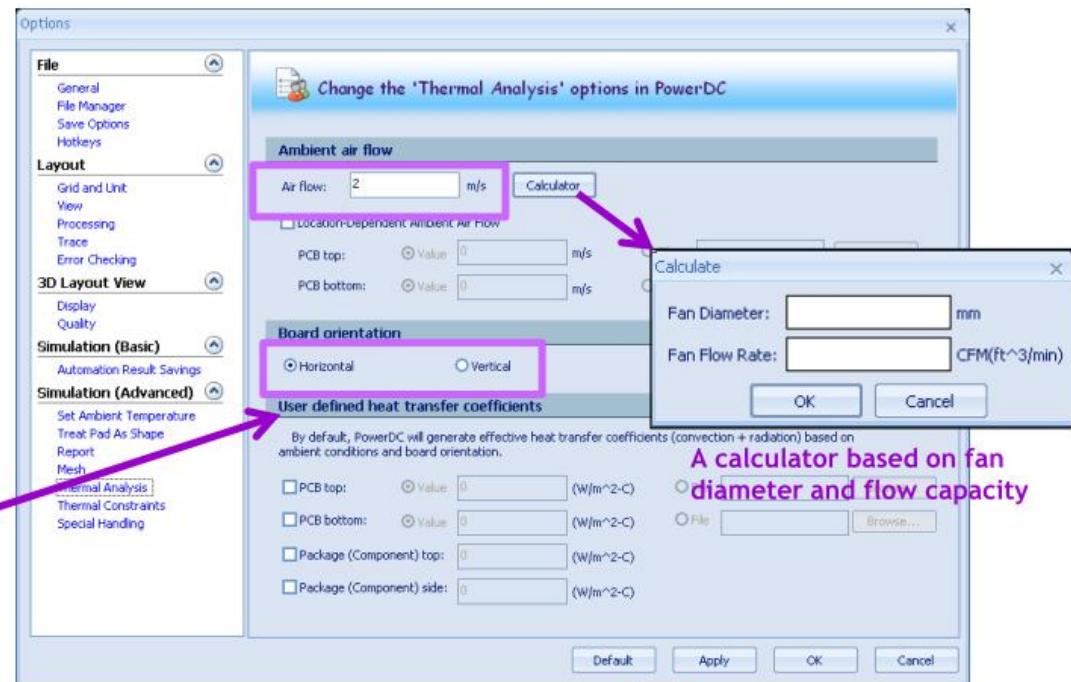
Constraints Setup

Simulation

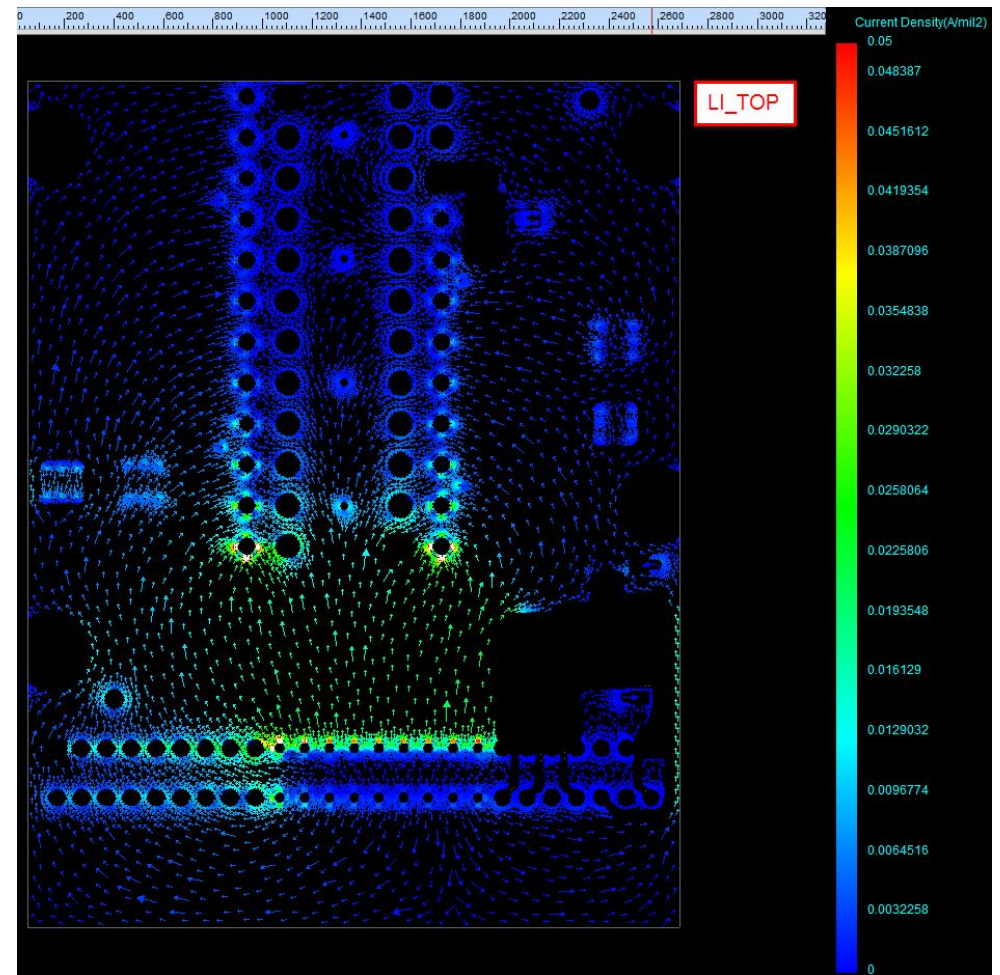
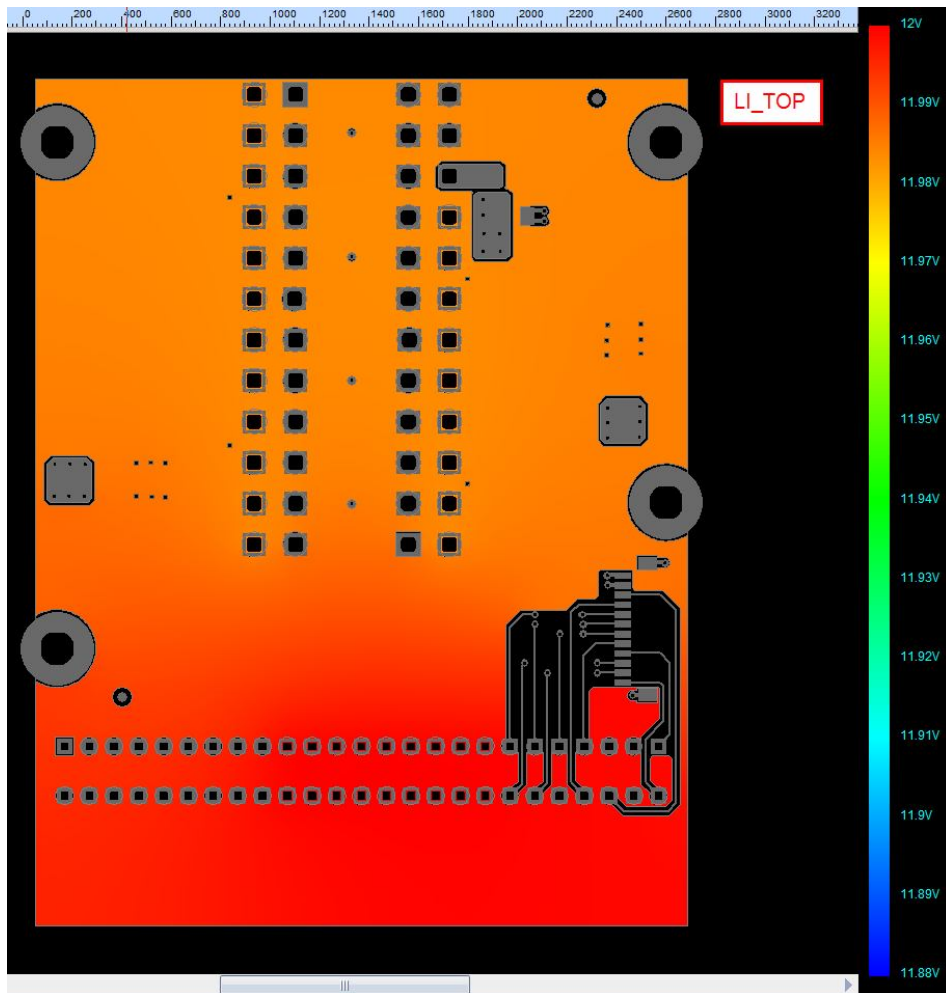
Results and Report

This section is for heat transfer experts only. By default, PowerDC will generate effective heat transfer coefficients (convection + radiation) based on ambient conditions and board orientation.

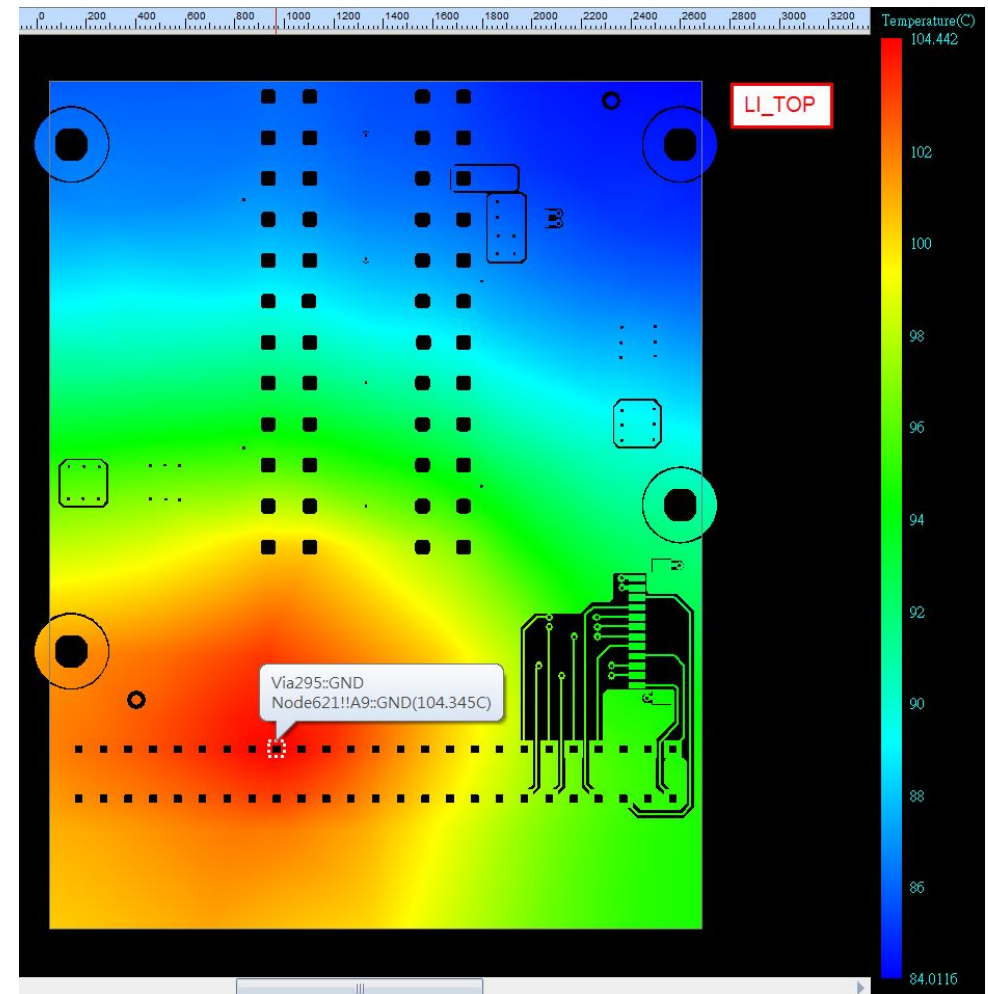
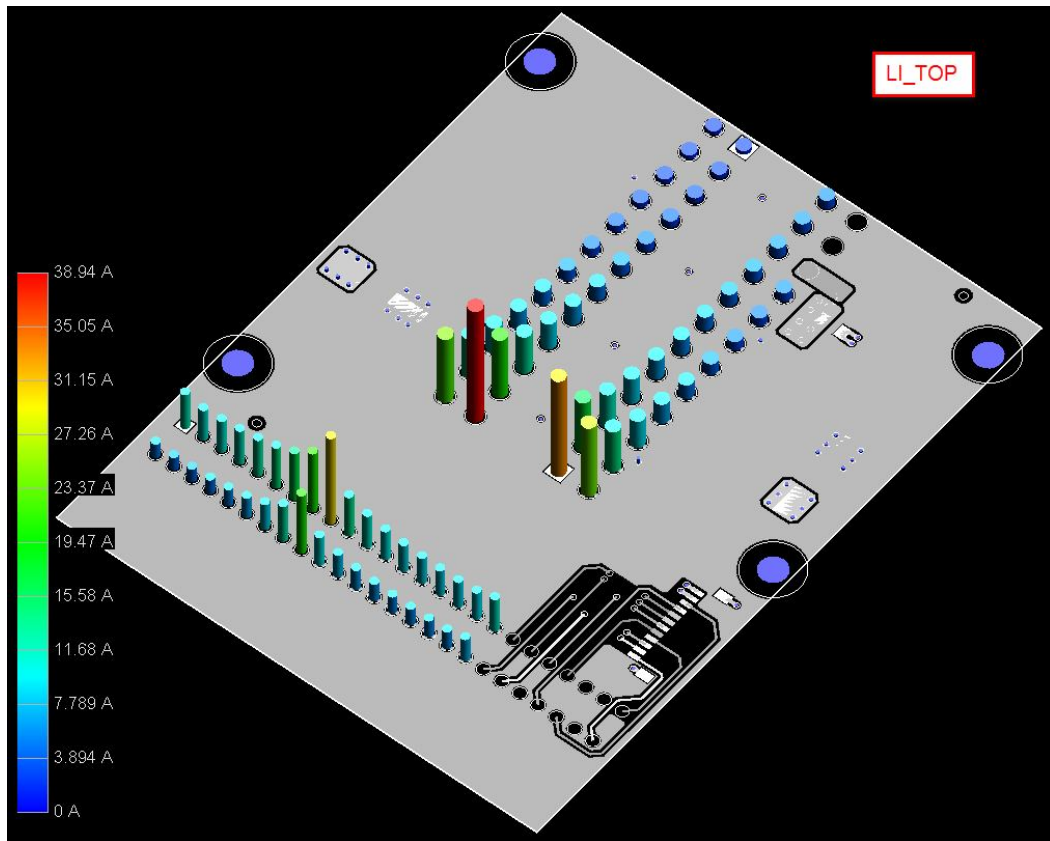
- **Objective:** Setup ambient air flow and board orientation.
- **Explanation:** Ambient air flows and board orientation will affect heat transfer.
- **Procedure:** Fill the menu (see blow).



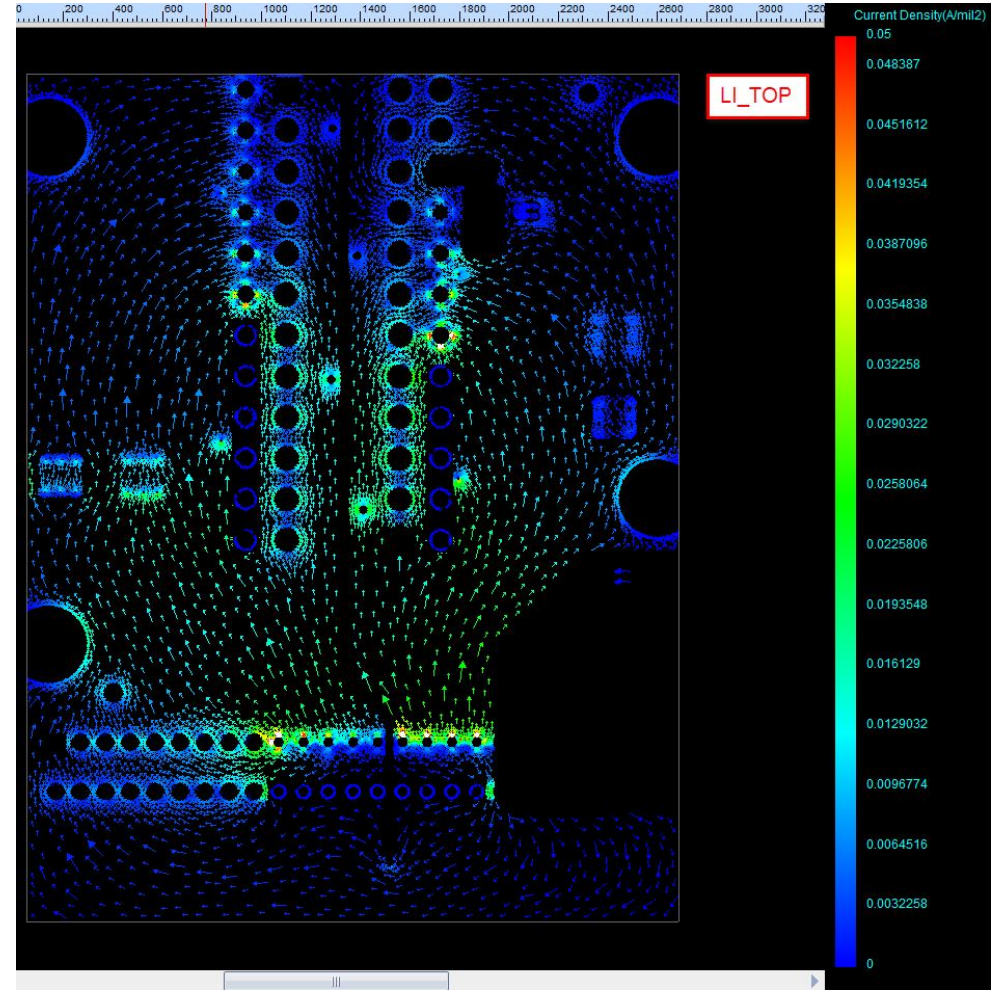
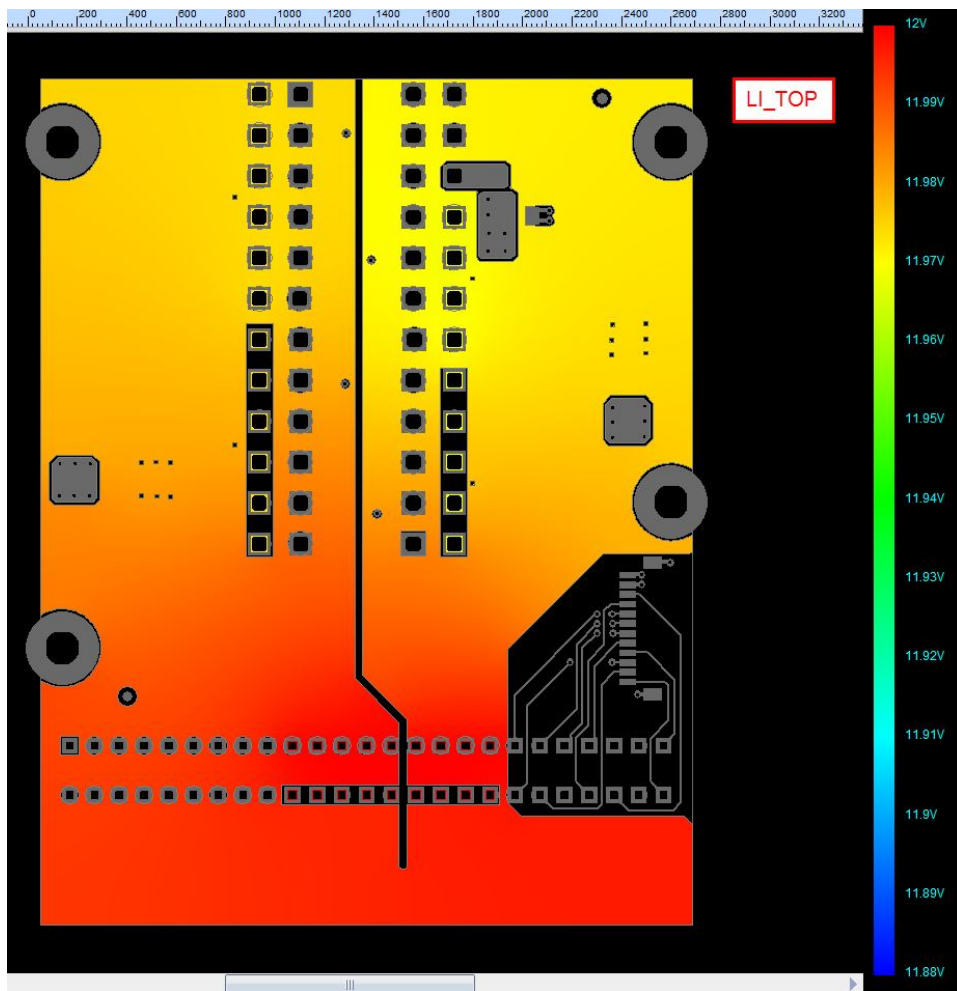
Simple structure design case study



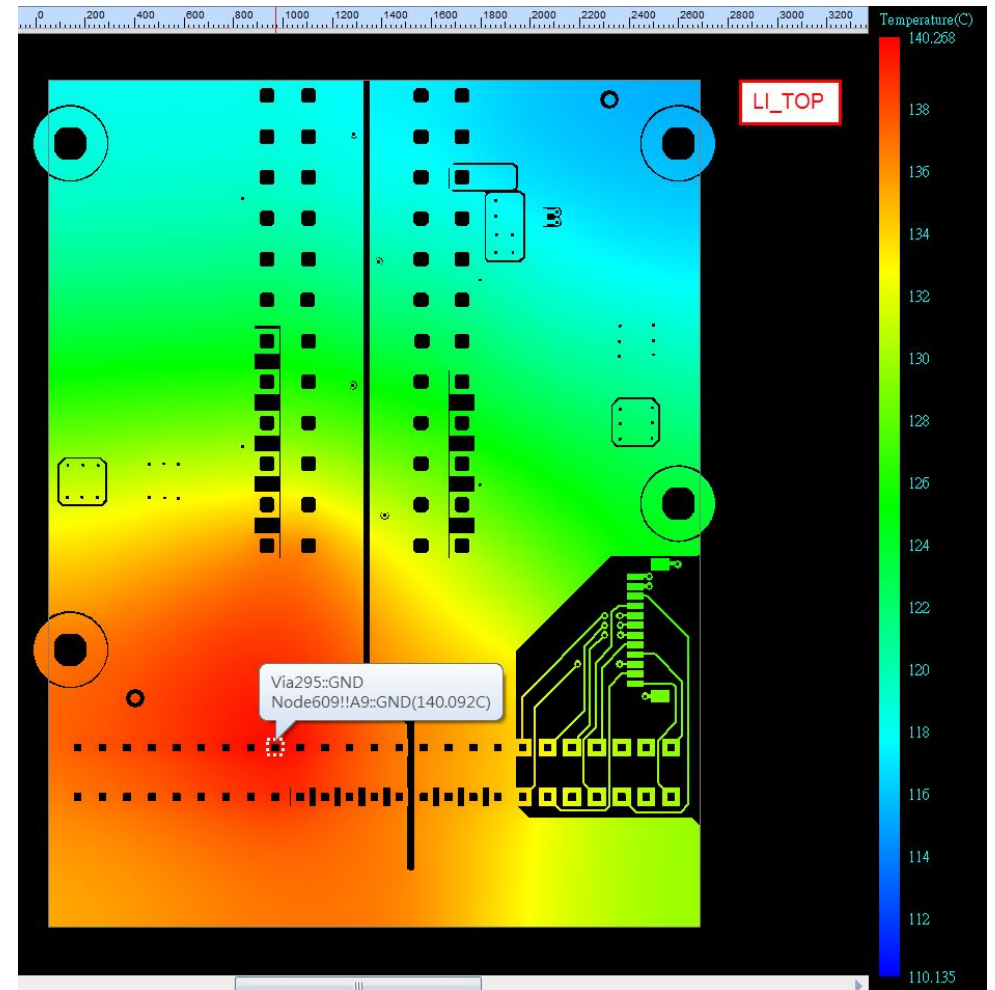
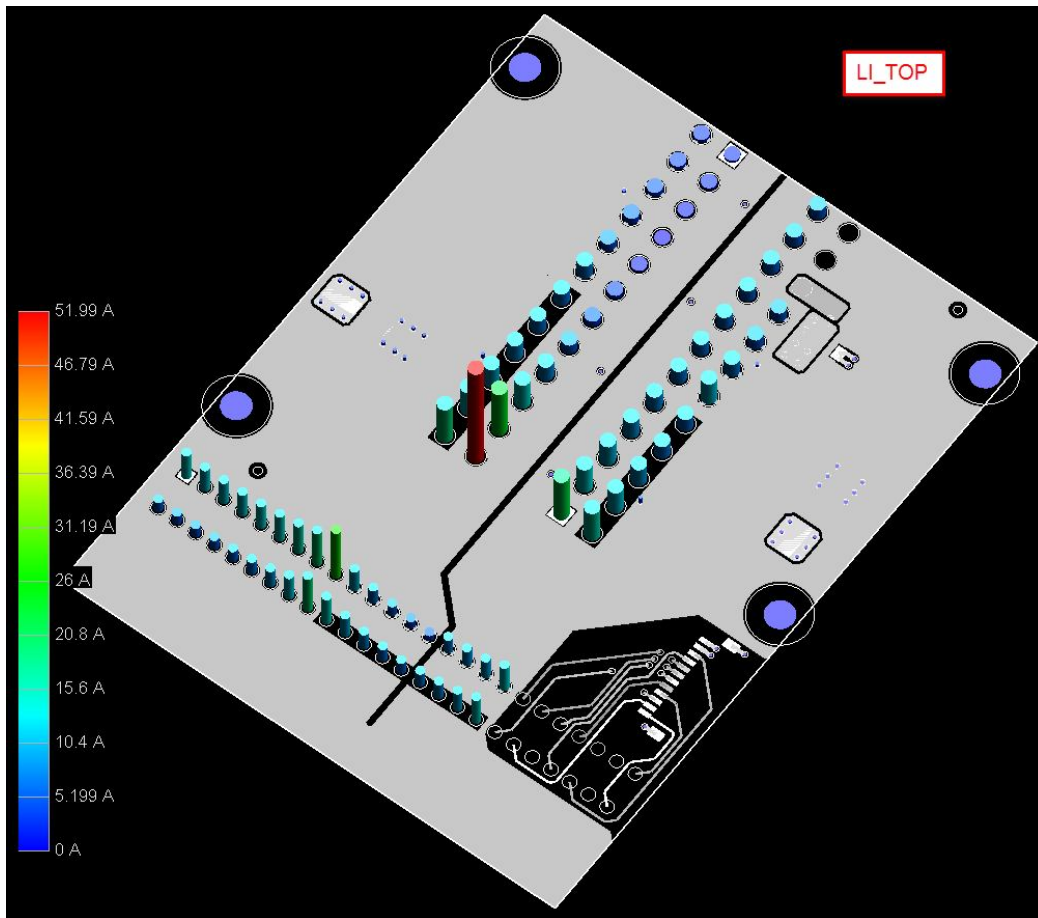
Simple structure design case study



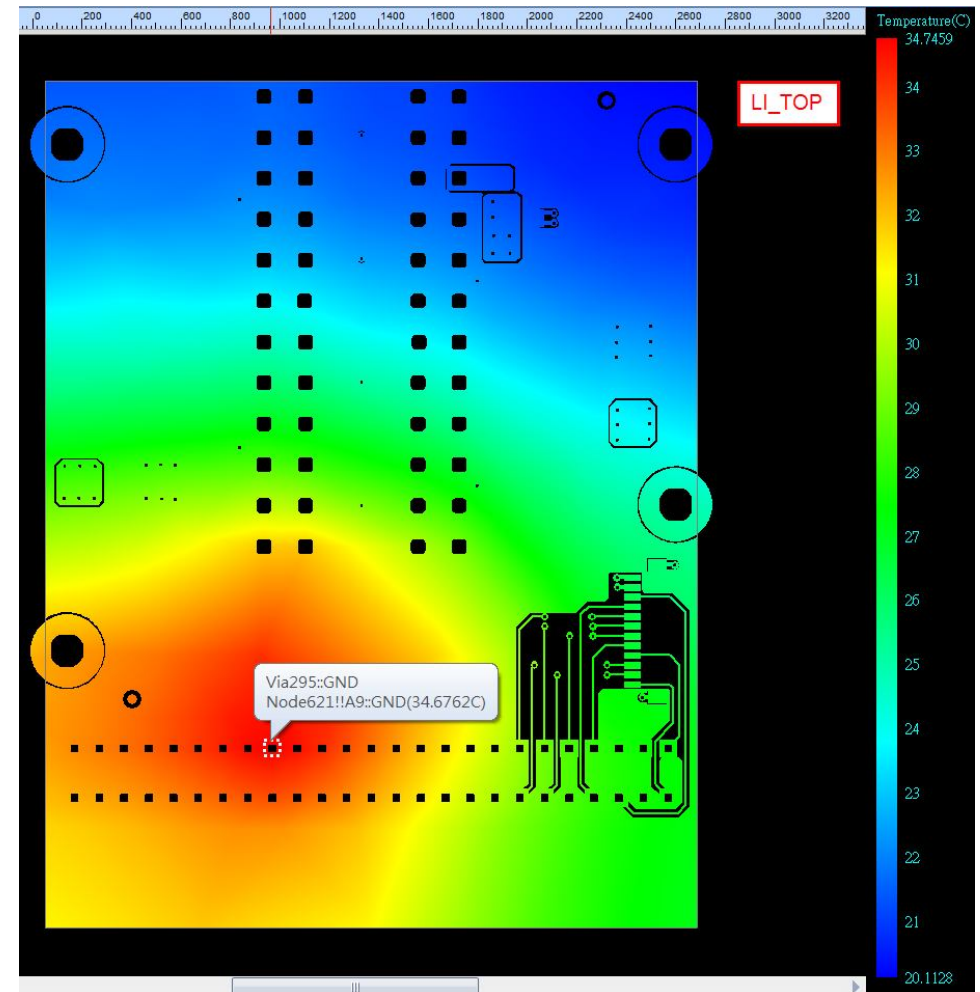
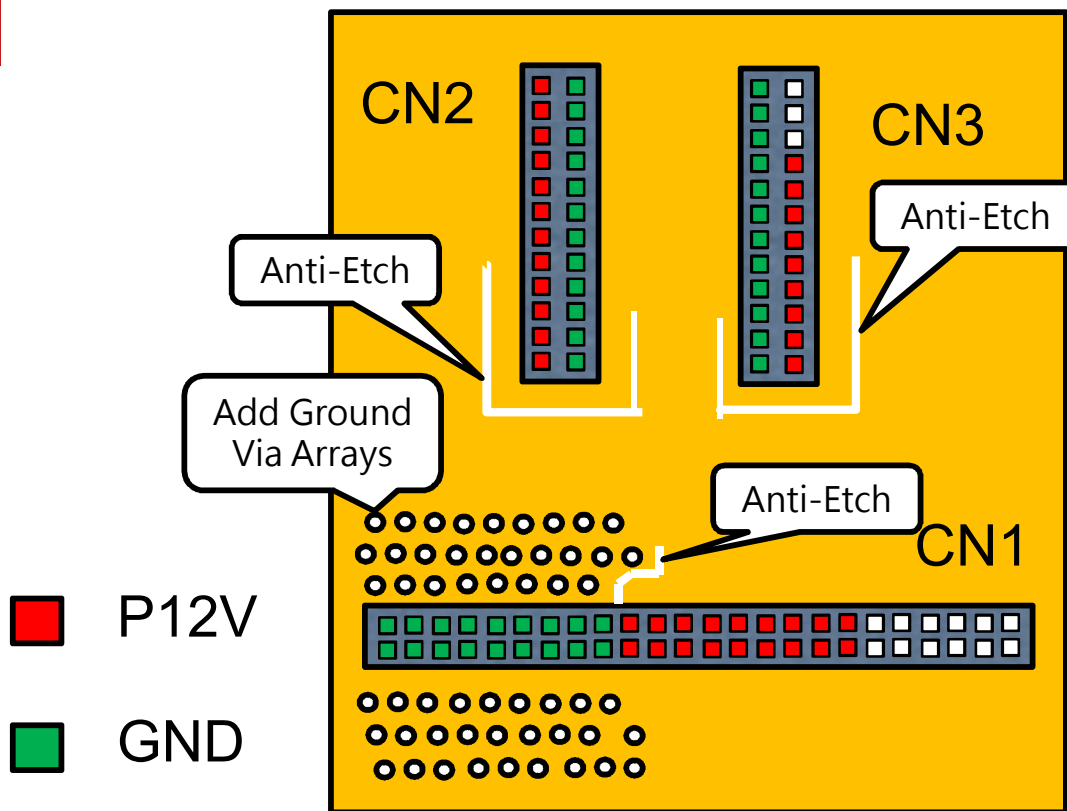
Simple structure design case study



Simple structure design case study



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Summary

1. The following DC analyses are described as necessary verification items. Missing one or more analyses may degrade the system performance and lead to the product failure.

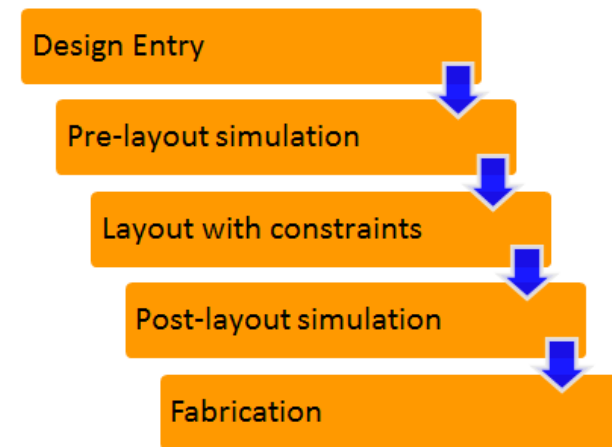
- (a) Actual DC voltages at devices with thermal effect
- (b) Current density and temperature on metal
- (c) Current carrying capability of interconnect
- (d) Power and ground pin effectiveness

2. The HTML report can be used as the design checking and reference.

Simultaneous design process



Traditional design process



Thanks for your attention~

