

Comprehensive DDR4 Design Analysis Experience Sharing

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AIC



Outline

1. Company Facts
2. Target Vertical Markets and Trend



> COMPANY FACTS



Established Date : May 3rd, 1996

Company Founder/ CEO : Michael Liang

HQ Address : No. 152, Section 4th, Linghang N. Road ,
Dayuan District, Taoyuan city 337, Taiwan



> COMPLETE PRODUCT LINES FOR VARIOUS MARKETS

Target Vertical Markets



Cloud Data Center



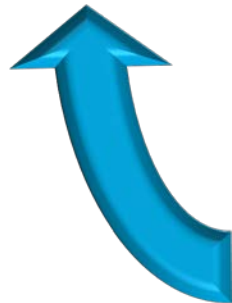
Networking Security



Broadcasting



Industrial PC



Storage Solution



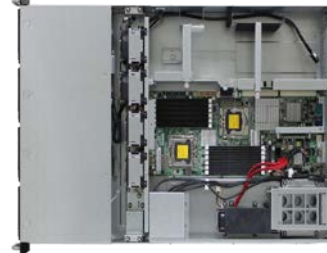
Storage Controller Design

Rackmount Enclosure



Server Board Design

Server Barebone



Agenda

- Introductions
- DDR4 Design Challenges
- Experience Sharing
- Summary



Introductions



DDR3(3L) vs DDR4

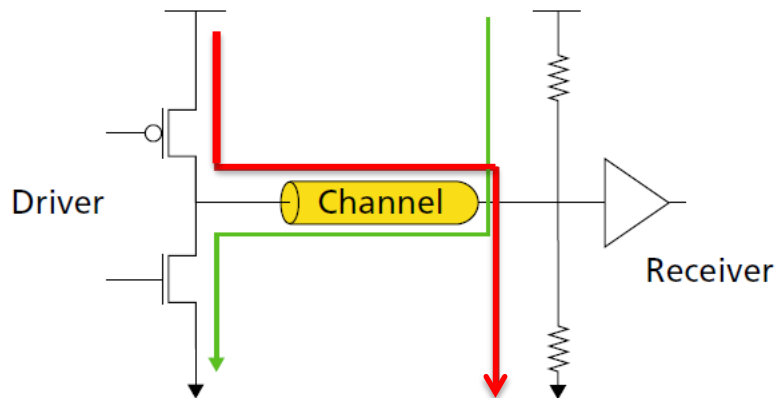
Enhancement	Features/Options	DDR3(3L)	DDR4
Performance & Scalability	Data Rate (Mb/s)	800/1066/1333/1600 plus 1866, 2133	1600/1866/2133 /2400/ 2667/3200
	Vref Inputs	2 – DQs and CMD/ADDR	1 –CMD/ADDR
	Bank Group	0	4
	Data Rate (Mb/s)	800/1066/1333/1600 plus 1866, 2133	1600/1866/2133 /2400/ 2667/3200
Power Efficiency	Voltage (core,VDD,VDDQ)	1.5V (1.35v)	1.2V
	DQ Bus	SSTL15	POD12
	Data Bus Inversion (DBI)	none	supported
	VPP Supply	none	2.5V , wordline boost
Reliability Accessibility & Serviceability	Data Bus Write CRC	none	supported
	Connectivity Test Mode	none	supported
	Register Parity Check	none	supported



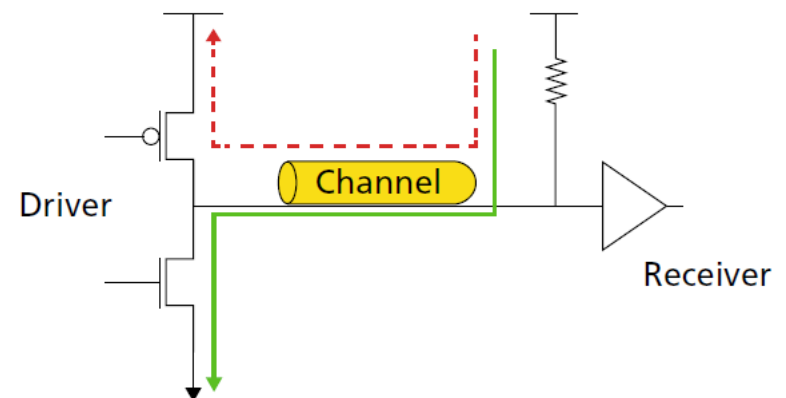
New I/O Interface – Pseudo Open Drain

- DDR4's new memory interface employs pseudo-open-drain (POD) termination
- DDR4 consumes power only when the VDD rail is pulled down to a logical 0 (Low)

DDR3 - push-pull I/O interface

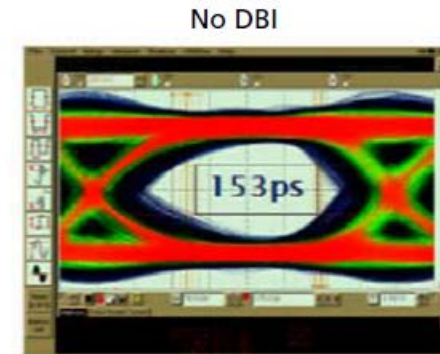


DDR4 - pseudo open drain I/O interface



Data Bus Inversion (DBI)

	Controller				Data Bus				Memory			
DQ0	0	1	0	0	1	1	0	1	0	1	0	0
DQ1	1	1	0	0	0	1	0	1	1	1	0	0
DQ2	0	0	0	0	1	0	0	1	0	0	0	0
DQ3	0	1	1	0	1	1	1	1	0	1	1	0
DQ4	0	1	0	0	1	1	0	1	0	1	0	0
DQ5	1	0	1	0	0	0	1	1	1	0	1	0
DQ6	1	1	1	0	0	1	1	1	1	1	1	0
DQ7	0	0	1	0	1	0	1	1	0	0	1	0
DBI_n					0	1	1	0				
Number of low bits	5	3	4	8	4	3	4	1				



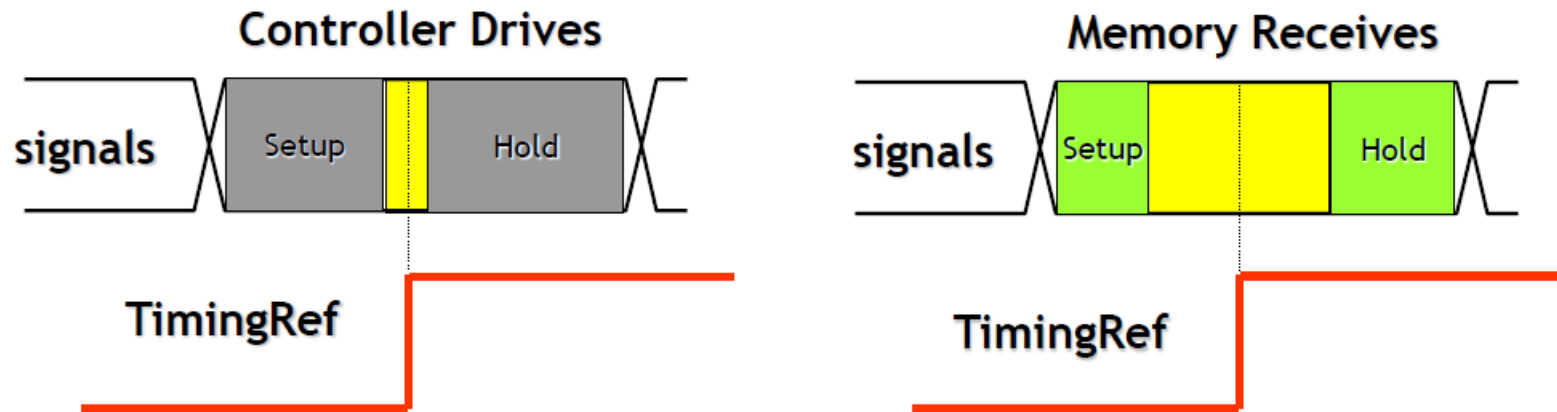
- Drives fewer bits LOW
- Consumes less power
- Enables fewer bits switching

Write	Read
If DBI_n input is LOW(0), write data is inverted – Invert data internally before storage	If more than four bits of a byte lane are LOW(0): – Invert output data – Drive DBI_n pin LOW
If DBI_n input is HIGH(1), write data is not inverted	If four or less bits of a byte lane are LOW(0): – Do not invert output data – Drive DBI_n pin HIGH(1)

DDR4 Design Challenges



Source Synchronous Timing



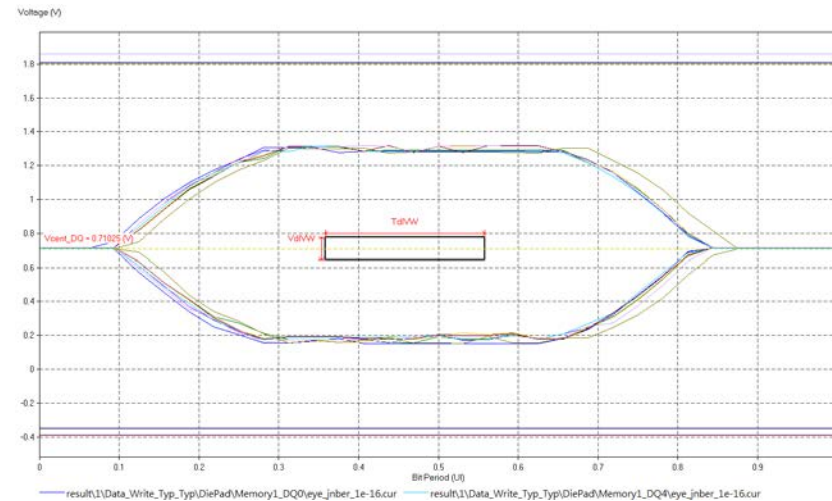
- Signals launched from Controller with known phase relationship, and robust Setup and Hold margin built in (TimingRef roughly middle of eye)
- Need to control skew, such that Setup and Hold requirements at the receiver are met



Bit Error Rate in DDR4

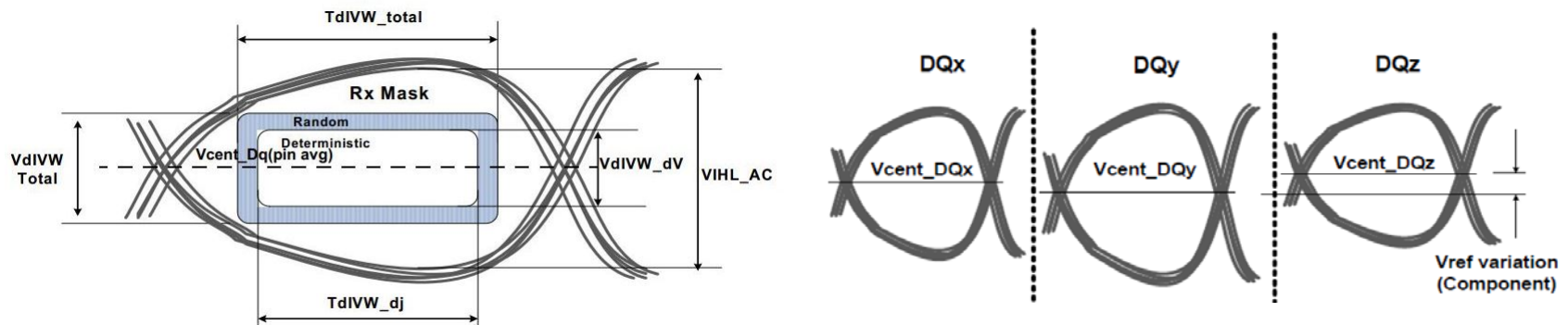
- Faster transfers data rates of 3.2Gb/s or higher.
- Jitter and noise affect the signal integrity and overall reliability.
- JEDEC specification is defines the data-valid window in terms of a **BER < 1E-16**.

Long simulation time to run million bit in TD simulation



DQ Receiver(Rx) Compliance Mask

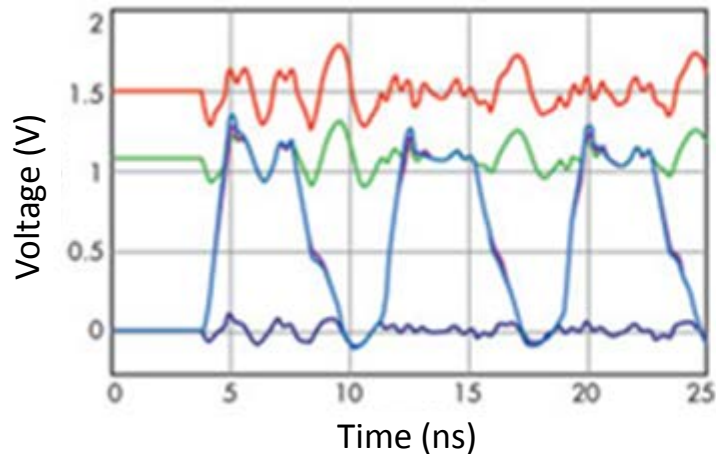
- Write Data signals will be evaluated vs. DQ mask
- Across pin $V_{cent}(V_{ref})$ DQ voltage variation
- Inclusion of jitter requires high-capacity simulation



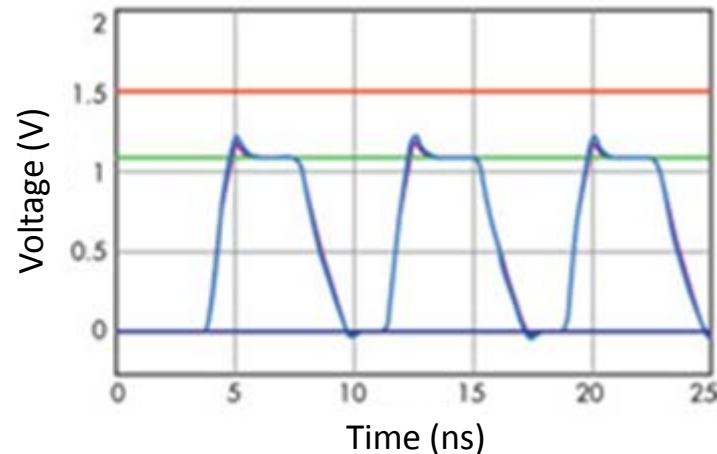
Signal Integrity with Power Aware

- IBISv5.0 improve on power-aware I/O buffer modeling with accuracy correlated in system-level SSO simulation.
- Non-ideal Power Delivery Network (PDN) effect Considering.

Non-ideal power delivery network
(significant Simultaneous Switching Noise effects)



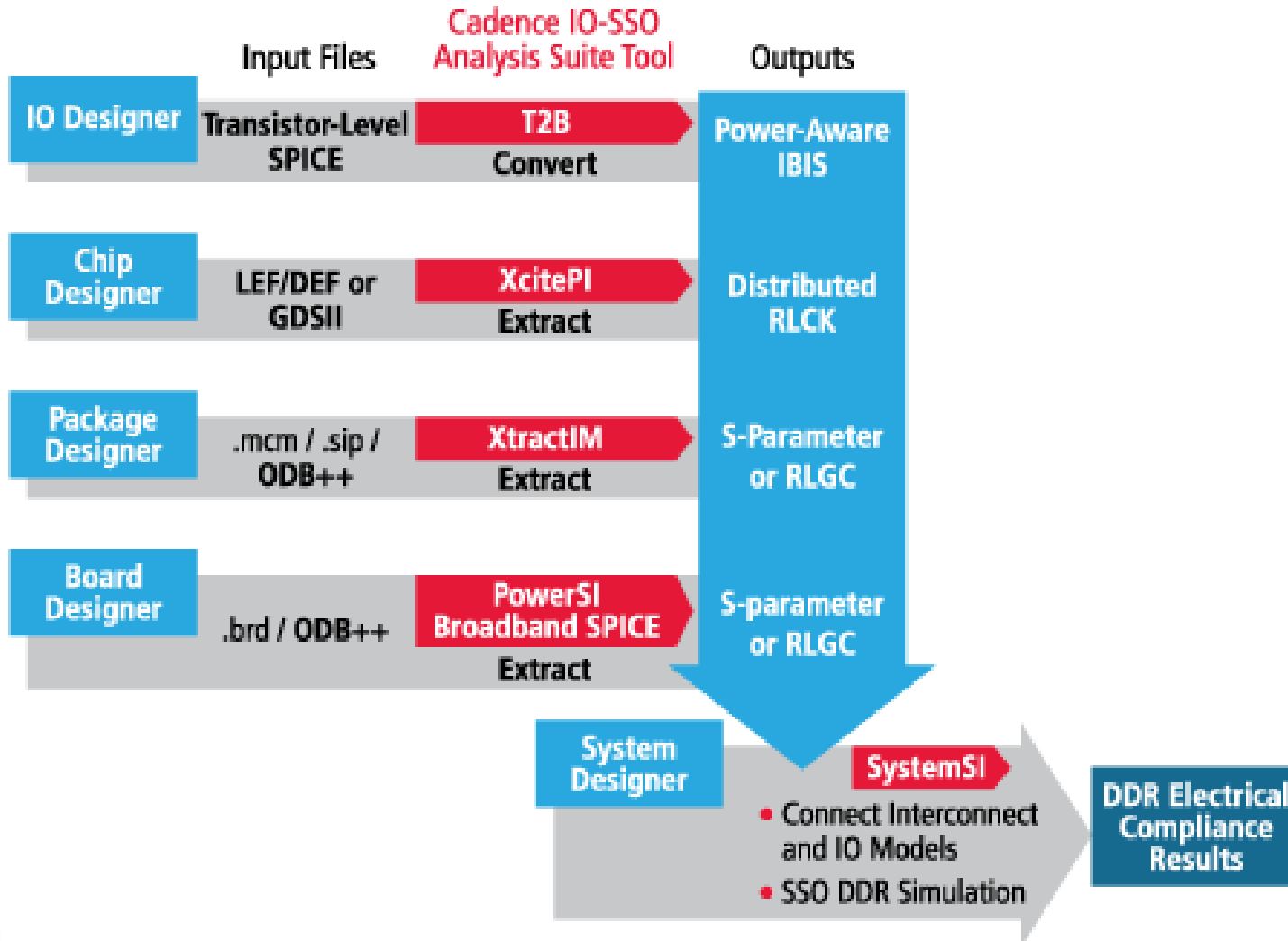
Ideal power delivery network
(minimal Simultaneous Switching Noise predicted)



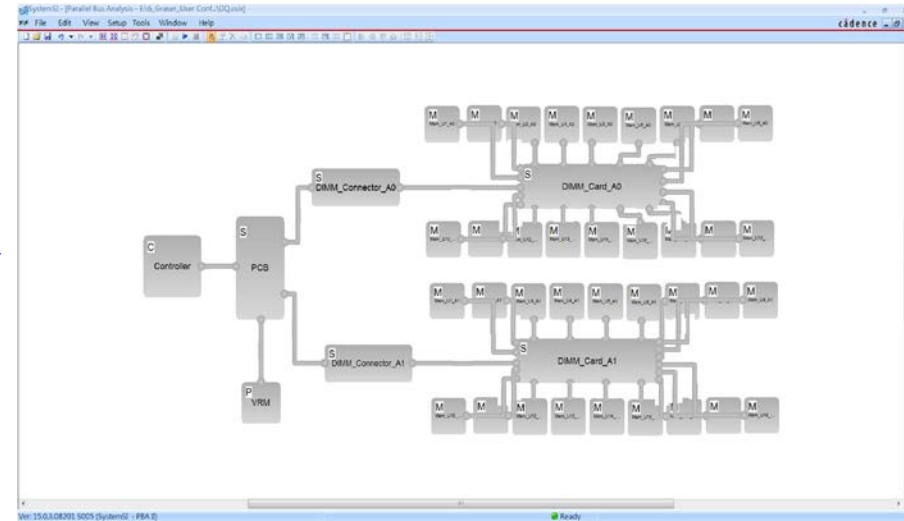
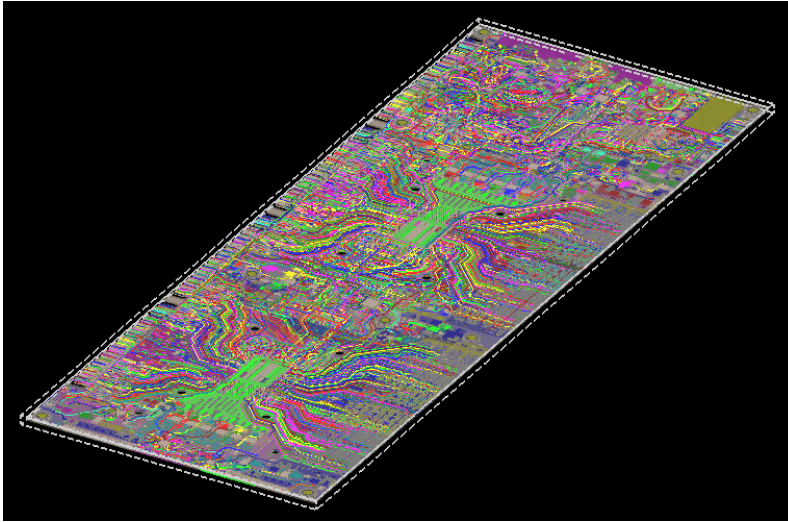
Experience Sharing



IO-SSO Analysis Flow



System Visualization Moves from Physical to Block Level

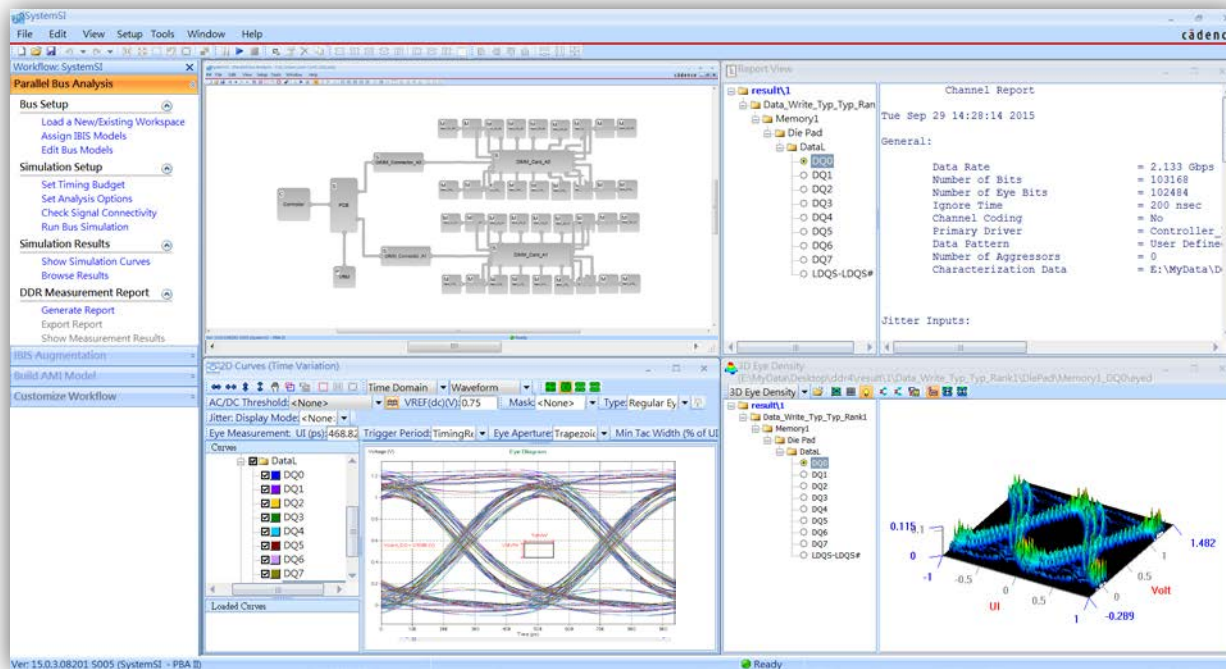


- Die-to-die system modeled at block level
- Signal paths can cross multiple levels of physical hierarchy:
 - Chip
 - Package
 - PCB
 - Connector
 - Cabinet

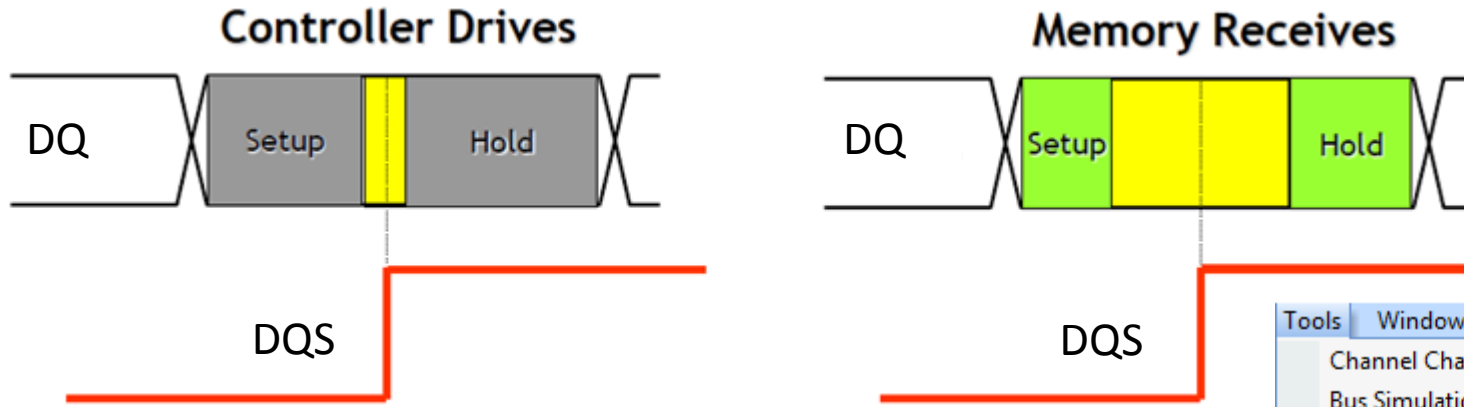


SystemSI-Parallel Bus Analysis

- SSO/SSN Analysis in SystemSI
- Guided of workflow
- Channel simulator for BER consideration $< 1e-16$
- JEDEC specification measurement Report



Timing Budgets – Setup/Hold time specification



The screenshot shows the "Timing Budget" dialog box in a software tool. The dialog is configured for a Data bus type, BothEdges edge type, and a Data Rate of 2.133 Gbps. The Clock Period is 0.937647 ns and the Bit Period is 0.468824 ns. The Controller component is set to "Controller" and the Memory component is set to "Memory". The IBIS File for both is "ssi_pba_ex.ibs".

The "Write" tab is selected, showing the following timing parameters:

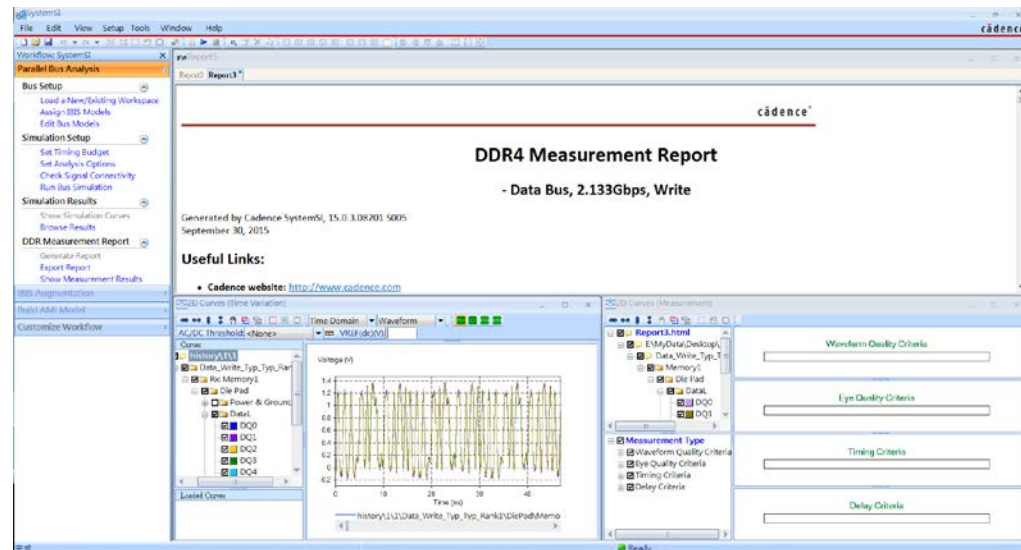
Driving (ns)		Receiving (ns)		Skew Budget (ns)	
Min Transmit	0.5UI	Min Receive	0.3UI	Setup:	0.0937647
Min Transmit	0.5UI	Min Receive Hold:	0.4UI	Hold:	0.0468823

The dialog also includes a "Tools" menu with options like "Channel Characterization", "Bus Simulation", "Timing Budget...", "Write Leveling...", "Frequency Response...", "S Parameter Extraction...", "S Parameter Viewer...", "Sweep Manager...", and "Layout Association...". The "Timing Budget..." option is highlighted. The dialog has "OK", "Cancel", and "Apply" buttons at the bottom right, and a "Ready" status indicator at the bottom center.



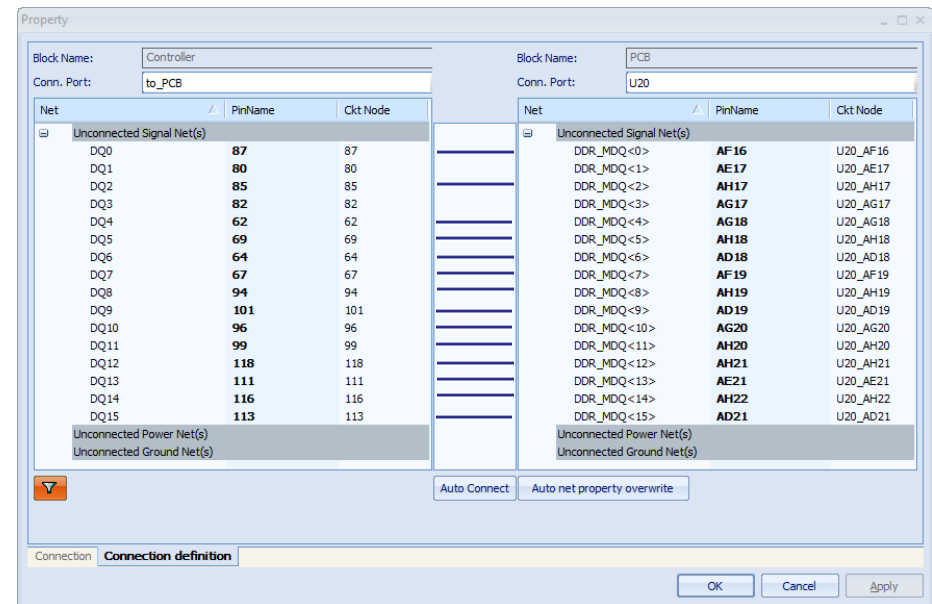
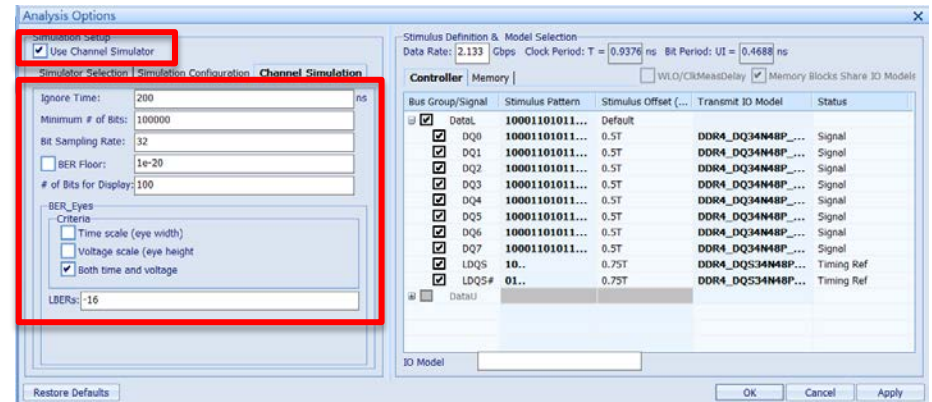
JEDEC Compliance specification Measurement Report

- Automatic waveform measurements post-processing to generate reports
- Use the browser for quick observation waveform
- The report contains a table of contents format :
 - Waveform Quality
 - Overshoot
 - DQ Mask (DDR4)
 - Timing Margin (setup/hold)
 - Delays & skews
 - Corresponding JEDEC specification parameters explanation



Analysis Options

- Channel simulation techniques employed.
- Simulate with IBIS or non-IBIS device models.
- User can Modify Minimum number of bits and BER Eyes elastically setting .
- MCP Header simple operation be fast connection relationship (Net,Pin,Ckt) between each block.



JEDEC Specification Generator Report Support

- DDR4/LPDDR4/DDR3 threshold support
- DQ mask Spec parameters
- Measure VREF(Vcent) on-the-fly

SystemSI-2D Curves (Time Variation)

Workflow: SystemSI

Parallel Bus Analysis

Generate Report

Waveform Location: Die Pad

Measurement Range: 0

DC Threshold: 100

DC Threshold: 75

Threshold: DDR4(AC100/DC25)

Single-E

Cas...

Measurement Options

Eye Trigger: TimingRef

Eye Aperture: Trapezoid

HTML Header

Title: DDR4 Measurement Report

Sub-Title: Data Bus, 2.13Gbps, Write

Notes:

Spec	Value	Unit	Usage
DQ Mask			
Vref			
Vref_max	0.77	VDDQ	Vcent_DQ
Vref_min	0.45	VDDQ	Vcent_DQ
Vref_step	0.0080	VDDQ	Vcent_DQ
Vref_set_tol	0.0015	VDDQ	Vcent_DQ
Mask			
VdW	136	mV	DQ Mask
TdW	0.2	UI	DQ Mask
Max IdQs2DQ	0.17	UI	IDQS2DQ
Max IdQ2DQ	0.1	UI	IDQ2DQ
Min Vth_AC	186	mV	Vth_AC
Min TdPW	0.58	UI	TdPW
Min SlewRate_Mask	1	V/ns	Min SlewRate_Mask
Max SlewRate_Mask	9	V/ns	Max SlewRate_Mask
Min SlewRate_AC_Swing	0.2	V/ns	Min SlewRate_AC_Swing
Max SlewRate_AC_Swing	9	V/ns	Max SlewRate_AC_Swing

Strobe Adjustment: 0.02 UI

Ver: 15.0.3.08201.5005 (SystemSI - PBA II)



DQ Rx Mask Support in SystemSI

- Derive Vcent_DQ level on-the-fly from raw waveforms for each DQ signal
- Automatically position and evaluate DQ mask vs. eye

Report

Iteration (Waveform)	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8	DQ9
1	1	1	1	1	1	1	1	1	1	1

4.2 DQ Mask Report

4.2.1 Data Bus Report

4.2.1.1 E:\SiData\Desktop1237-Result1>Data_Write_Typ_Typ_Rank1.DistPd

4.2.1.1 Memory

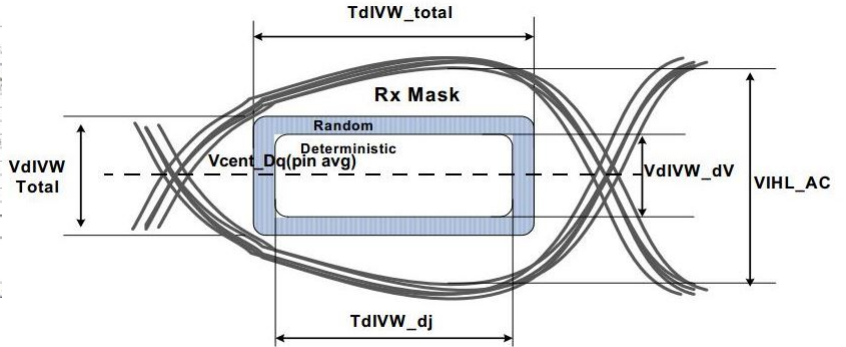
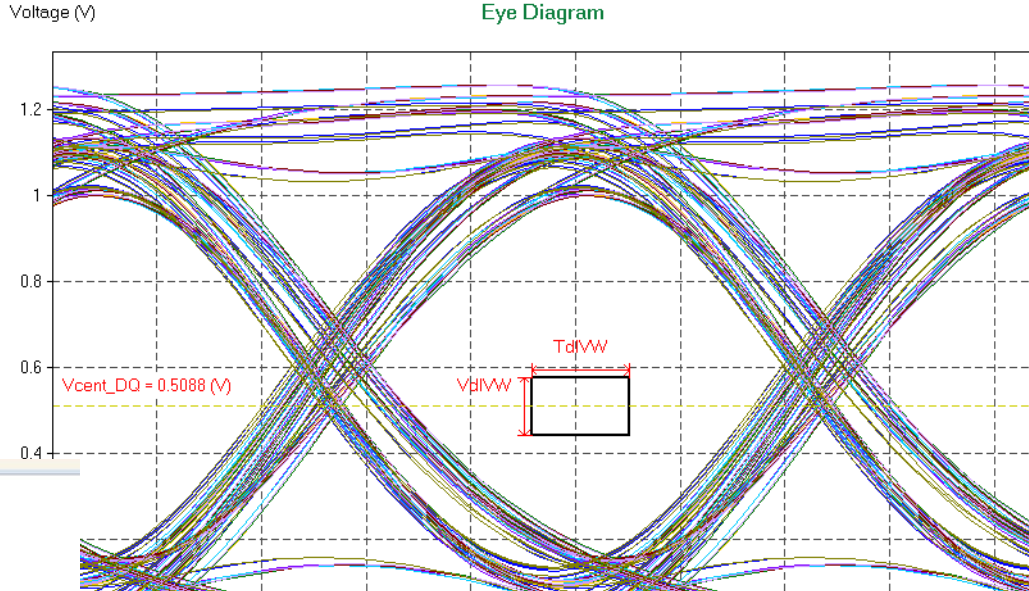
Click on a signal name to see the DQ Mask displayed.

Rx Signal	Pin	Vcent_DQ (V)	DQ Compliance Mask	Min. Rise (ps)	Min. Fall (ps)	V10%_AC (mV)	V90%_AC (mV)	Min. SlewRate (ps)	Max. SlewRate (ps)	Min. SlewRate_Mask (ps)	Max. SlewRate_Mask (ps)	Min. Rise	Max. Rise	Min. Fall	Max. Fall
DQ0	D0	0.500102	Pass	180.418	210.786	1278.19	861.163	16.66486	1.82171	N/A	4.80590	0.27712	4.37375		
DQ1	F1	0.500102	Pass	180.412	214.679	1321.16	861.123	16.27358	1.80721	N/A	4.81087	0.27712	4.39332		
DQ2	F2	0.500104	Pass	181.119	208.421	1328.72	867.867	17.37359	2.06672	N/A	4.80511	0.48476	4.02712		
DQ3	F3	0.500104	Pass	180.809	214.782	1328.72	868.871	17.3969	2.06732	N/A	4.87813	0.02718	4.62156		
DQ4	D3	0.500277	Pass	176.48	214.651	1302.45	865.644	18.8445	2.21772	N/A	4.87485	0.50196	4.76860		
DQ5	D8	0.500571	Pass	179.305	221.971	1480.14	895.902	13.7418	0.48081	N/A	4.80012	0.51028	4.62217		
DQ6	D2	0.500402	Pass	179.141	213.940	1306.58	891.027	18.26113	4.62388	N/A	4.83278	1.97381	4.60986		
DQ7	D7	0.500518	Pass	123.321	214.719	1306.03	882.238	14.2502	4.07066	N/A	1.81975	0.427	4.78347		
AD0[0]	0[0]	Pass	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	4.14732	N/A	N/A		
LDQ0	F1_0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A		

Note: NI = Not Applicable; NMP = No Measurement Possible

4.2.2 Worst Case Summary

Measurement	Vcent_DQ	DQ Compliance	Min. Rise	Min. Fall	Min. SlewRate	Max. SlewRate	Min. Rise	Max. Rise	Min. Fall	Max. Fall
DQ0	0.500102	Pass	180.418	210.786	1278.19	861.163	16.66486	1.82171	N/A	4.80590
DQ1	0.500102	Pass	180.412	214.679	1321.16	861.123	16.27358	1.80721	N/A	4.81087
DQ2	0.500104	Pass	181.119	208.421	1328.72	867.867	17.37359	2.06672	N/A	4.80511
DQ3	0.500104	Pass	180.809	214.782	1328.72	868.871	17.3969	2.06732	N/A	4.87813
DQ4	0.500277	Pass	176.48	214.651	1302.45	865.644	18.8445	2.21772	N/A	4.87485
DQ5	0.500571	Pass	179.305	221.971	1480.14	895.902	13.7418	0.48081	N/A	4.80012
DQ6	0.500402	Pass	179.141	213.940	1306.58	891.027	18.26113	4.62388	N/A	4.83278
DQ7	0.500518	Pass	123.321	214.719	1306.03	882.238	14.2502	4.07066	N/A	1.81975



Summary

- DDR4 new challenges
 - 20% power saving from 1.5 V to 1.2 V
 - Fast transmission speed, grave challenge of timing margin
- New analysis techniques are required to evaluate Rx Mask for Data per JEDEC specifications.
- Employed channel simulator technique for BER < 1E-16 can save calculation time.
- Power aware SSO analysis can not be ignored.
- JEDEC type compliance sign-off report for DDR4.



Thank you !

