Comprehensive DDR4 Design Analysis Experience Sharing

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AIC

Outline

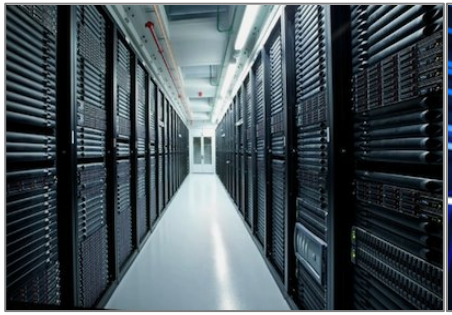
1. Company Facts
2. Target Vertical Markets and Trend

> COMPANY FACTS

Established Date :	May 3rd, 1996
Company Founder/ CEO :	Michael Liang
HQ Address :	No. 152, Section 4th, Linghang N. Road , Dayuan District, Taoyuan city 337, Taiwan

>COMPLETE PRODUCT LINES FOR VARIOUS MARKETS

Target Vertical Markets

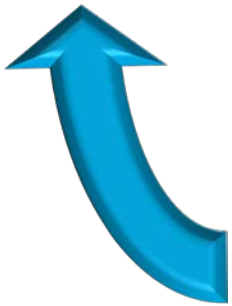


Cloud Data Center

Networking Security

Broadcasting

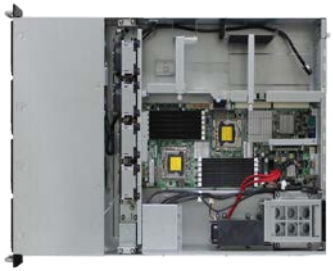
Industrial PC



Storage Solution

Rackmount Enclosure

Server Barebone



Storage Controller Design

Server Board Design

Agenda

- Introductions
- DDR4 Design Challenges
- Experience Sharing
- Summary

Introductions

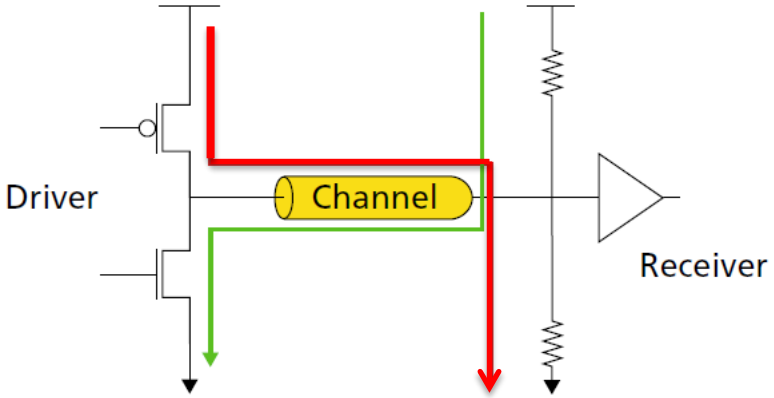
DDR3(3L) vs DDR4

Enhancement	Features/Options	DDR3(3L)	DDR4
Performance & Scalability	Data Rate (Mb/s)	800/1066/1333/1600 plus1866, 2133	1600/1866/2133 /2400/ 2667/3200
	Vref Inputs	2 – DQs and CMD/ADDR	1 –CMD/ADDR
	Bank Group	0	4
	Data Rate (Mb/s)	800/1066/1333/1600 plus1866, 2133	1600/1866/2133 /2400/ 2667/3200
Power Efficiency	Voltage (core,VDD,VDDQ)	1.5V (1.35v)	1.2V
	DQ Bus	SSTL15	POD12
	Data Bus Inversion (DBI)	none	supported
	VPP Supply	none	2.5V , wordline boost
Reliability Accessibility & Serviceability	Data Bus Write CRC	none	supported
	Connectivity Test Mode	none	supported
	Register Parity Check	none	supported

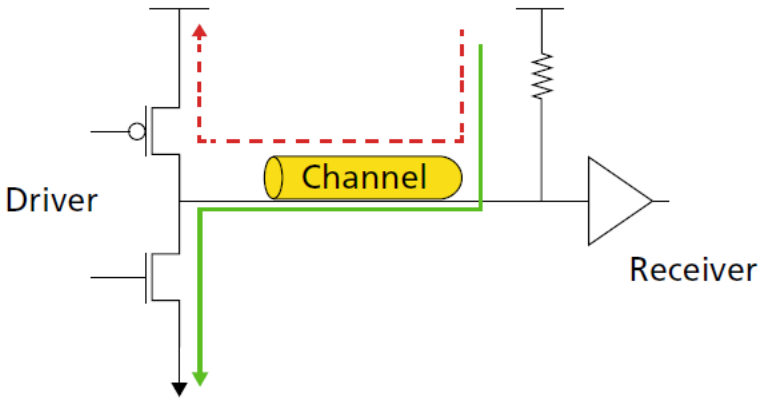
New I/O Interface – Pseudo Open Drain

- DDR4's new memory interface employs pseudo-open-drain (POD) termination
- DDR4 consumes power only when the VDD rail is pulled down to a logical 0 (Low)

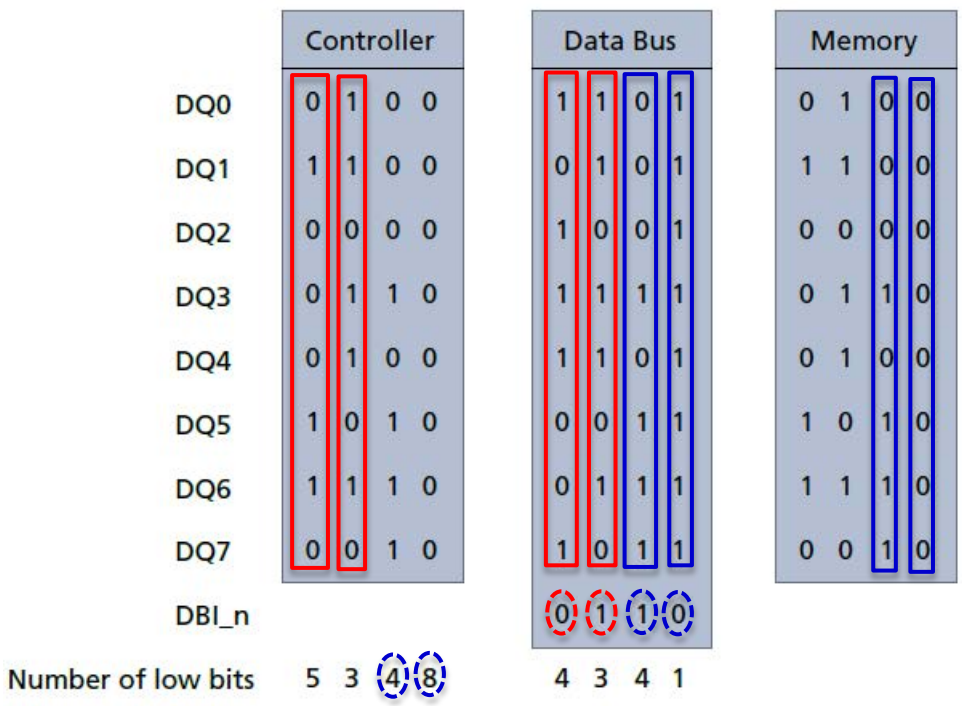
DDR3 - push-pull I/O interface

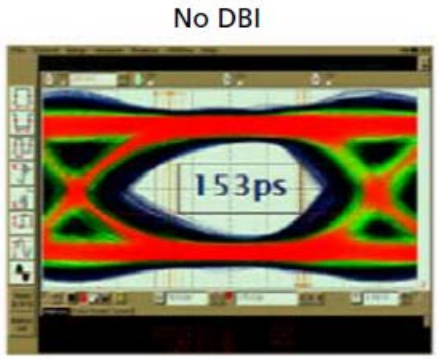


DDR4 - pseudo open drain I/O interface



Data Bus Inversion (DBI)



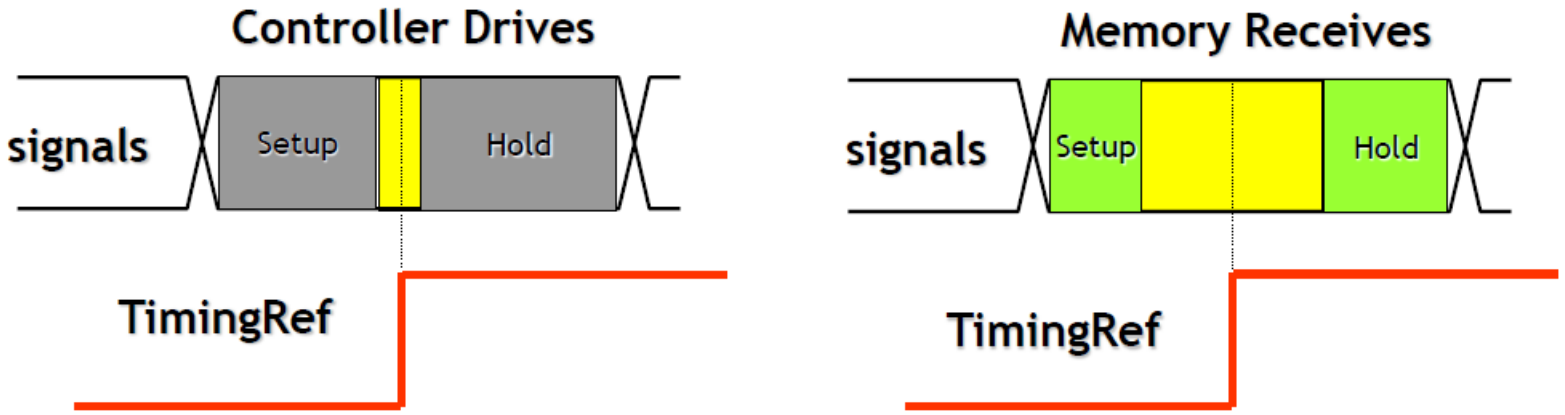


- Drives fewer bits LOW
- Consumes less power
- Enables fewer bits switching

Write	Read
If DBI_n input is LOW(0), write data is inverted – Invert data internally before storage	If more than ***four bits*** of a byte lane are LOW(0): – Invert output data – Drive DBI_n pin LOW
If DBI_n input is HIGH(1), write data is not inverted	If ***four or less bits*** of a byte lane are LOW(0): – Do not invert output data – Drive DBI_n pin HIGH(1)

DDR4 Design Challenges

Source Synchronous Timing

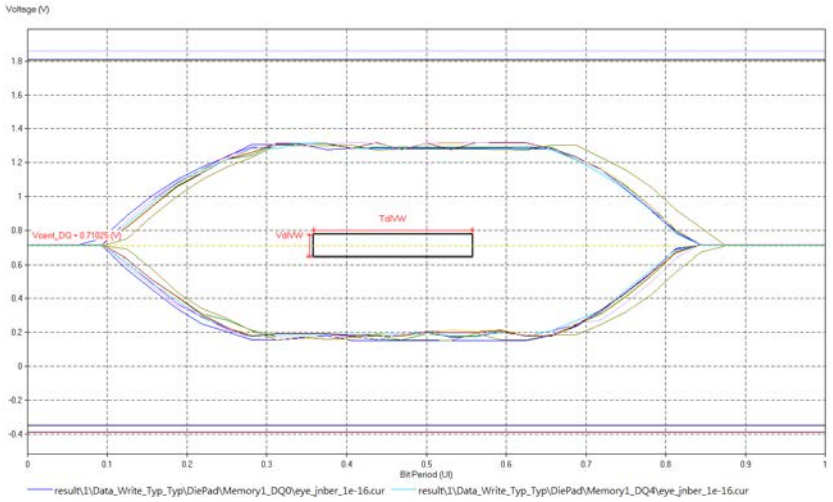


- Signals launched from Controller with known phase relationship, and robust Setup and Hold margin built in (TimingRef roughly middle of eye)
- Need to control skew, such that Setup and Hold requirements at the receiver are met

Bit Error Rate in DDR4

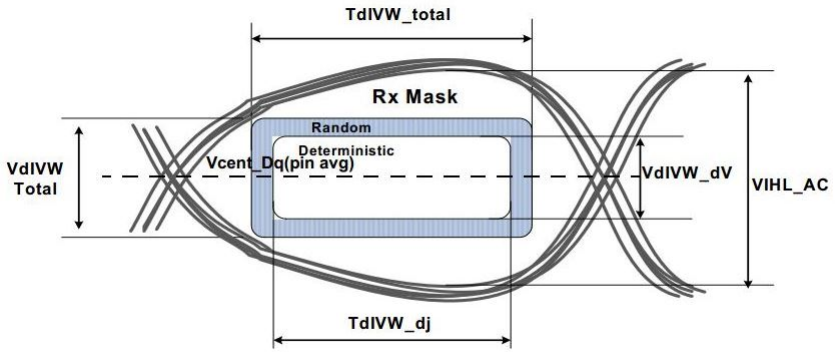
- Faster transfers data rates of 3.2Gb/s or higher.
- Jitter and noise affect the signal integrity and overall reliability.
- JEDEC specification is defines the data-valid window in terms of a BER < 1E-16.

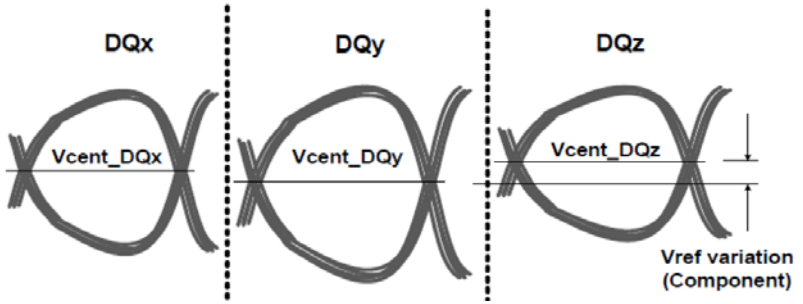
Long simulation time to run million bit in TD simulation



DQ Receiver(Rx) Compliance Mask

- Write Data signals will be evaluated vs. DQ mask
- Across pin Vcent(Vref) DQ voltage variation
- Inclusion of jitter requires high-capacity simulation

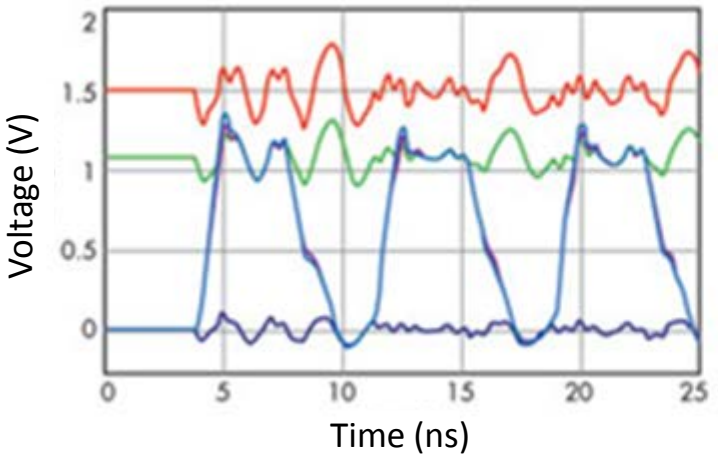




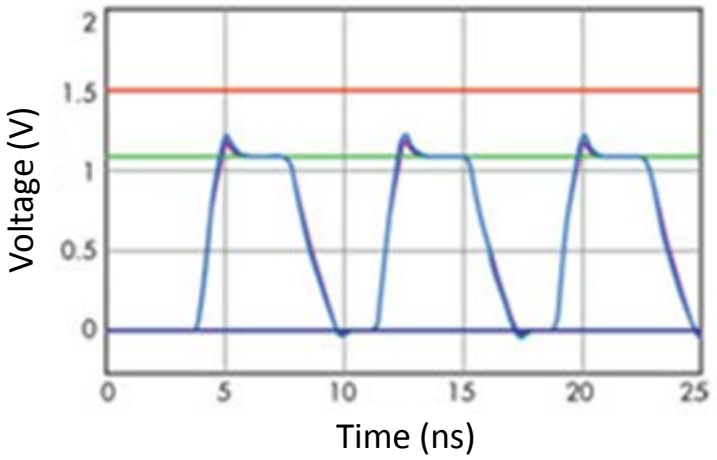
Signal Integrity with Power Aware

- IBISv5.0 improve on power-aware I/O buffer modeling with accuracy correlated in system-level SSO simulation.
- Non-ideal Power Delivery Network (PDN) effect Considering.

Non-ideall power delivery network
(significant Simultaneous Switching Noise effects)

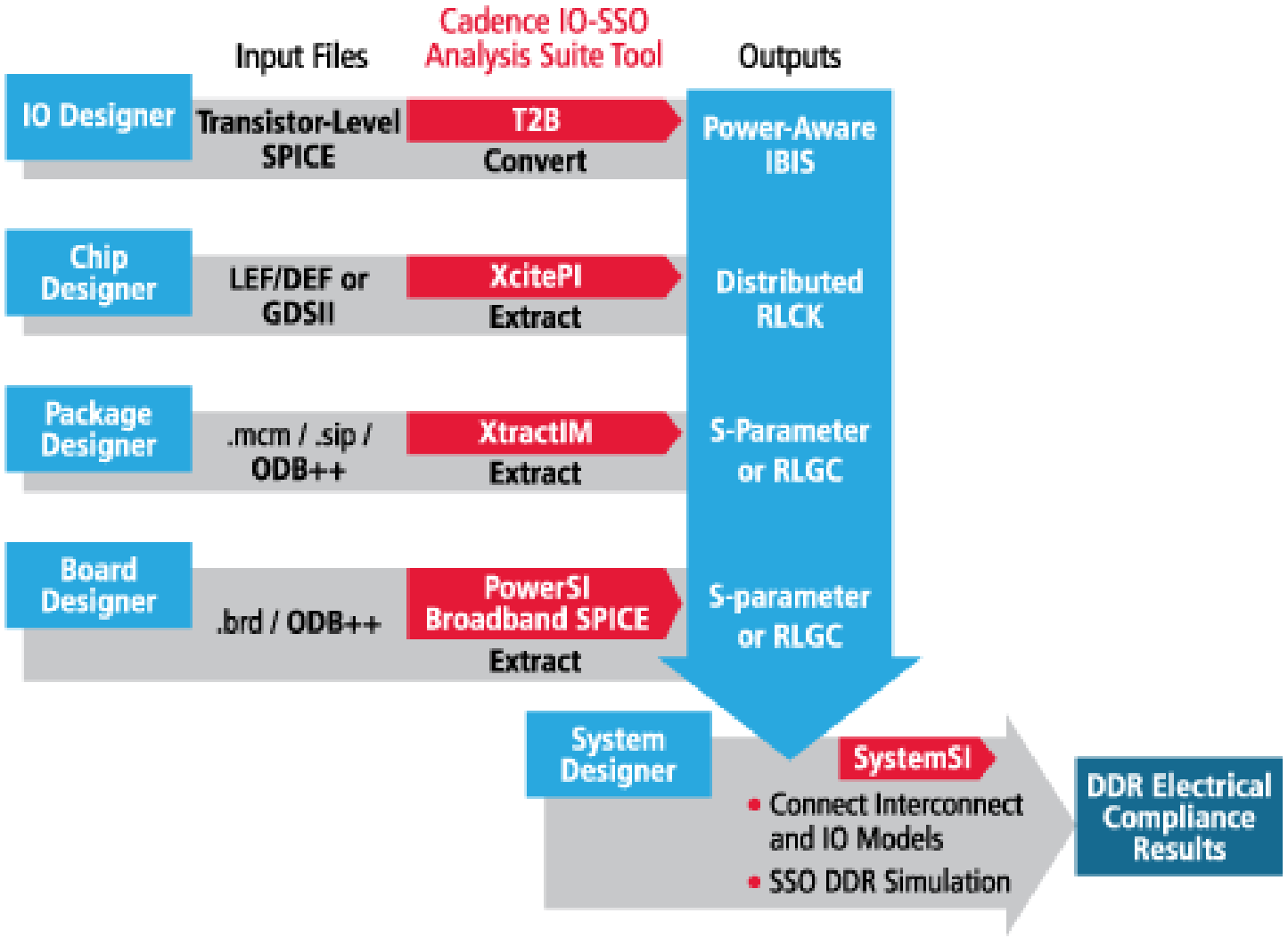


Ideal power delivery network
(minimal Simultaneous Switching Noise predicted)

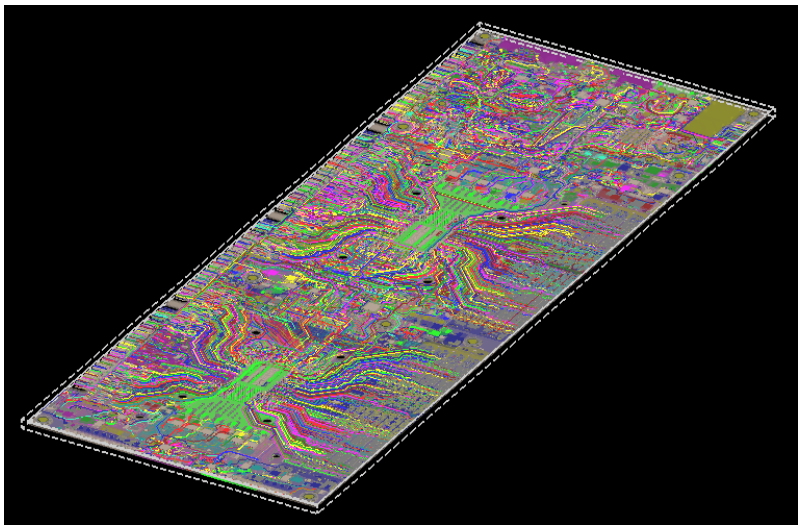


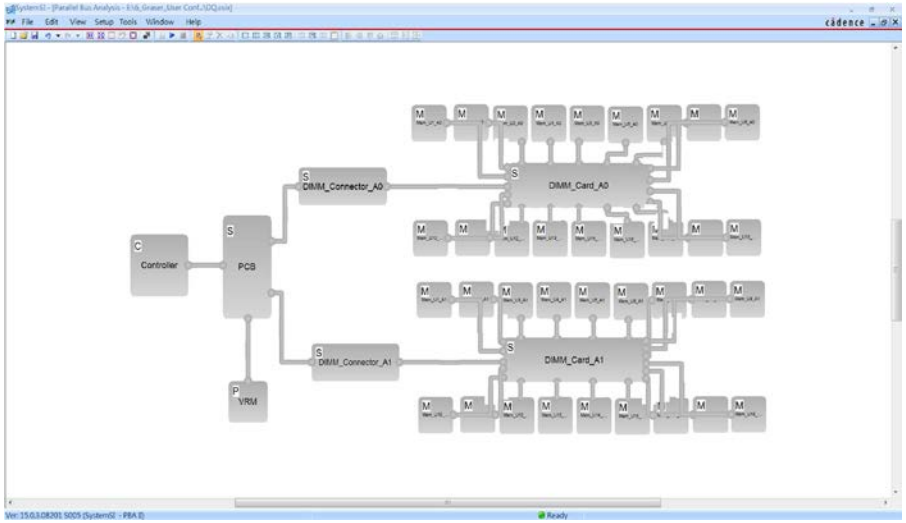
Experience Sharing

IO-SSO Analysis Flow



System Visualization Moves from Physical to Block Level

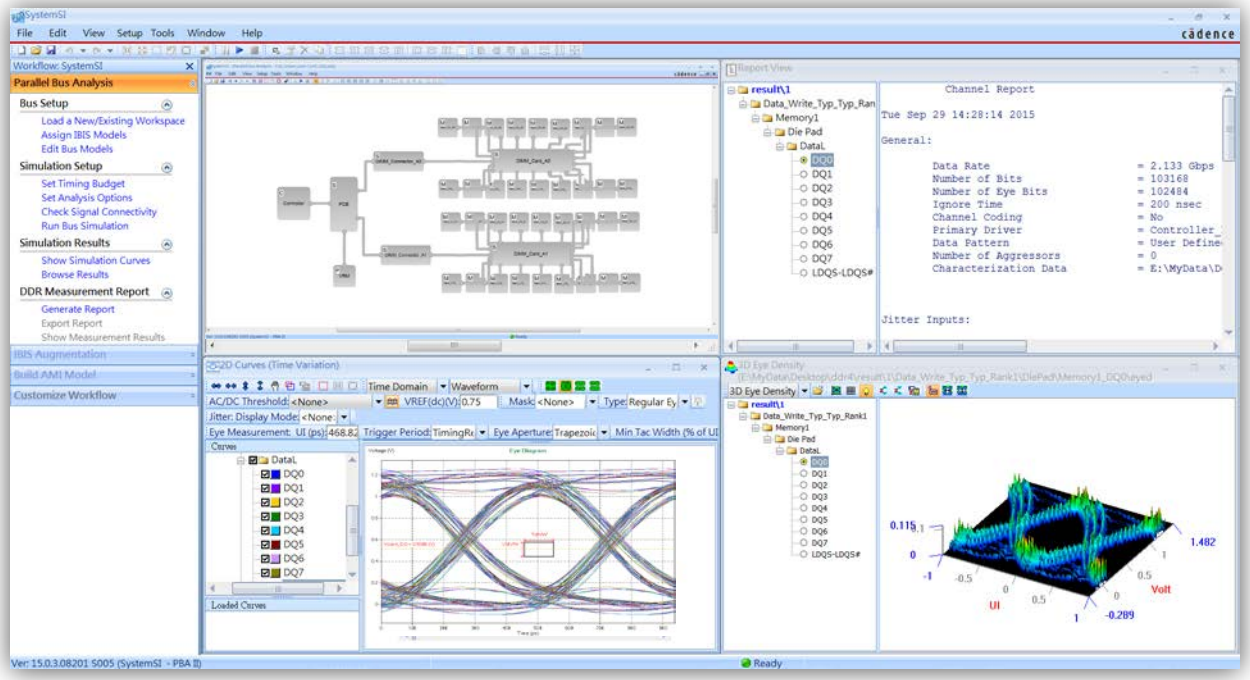




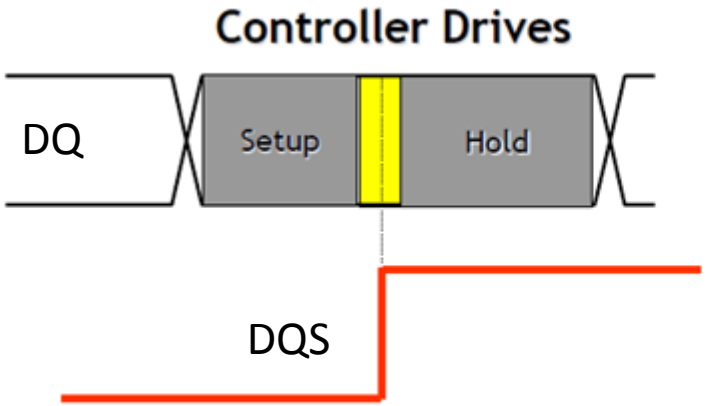
- Die-to-die system modeled at block level
- Signal paths can cross multiple levels of physical hierarchy:
  - Chip
  - Package
  - PCB
  - Connector
  - Cabinet

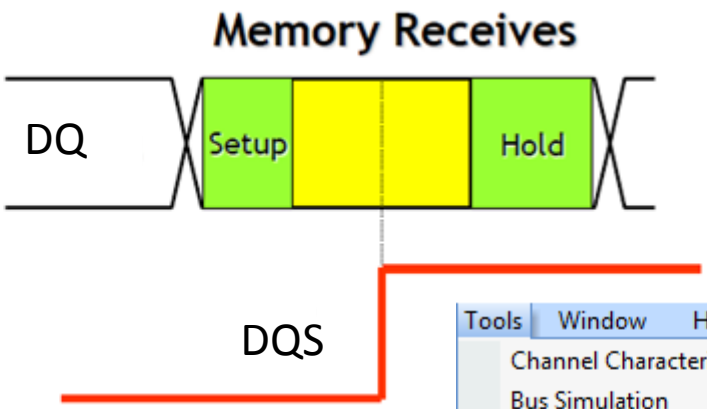
SystemSI-Parallel Bus Analysis

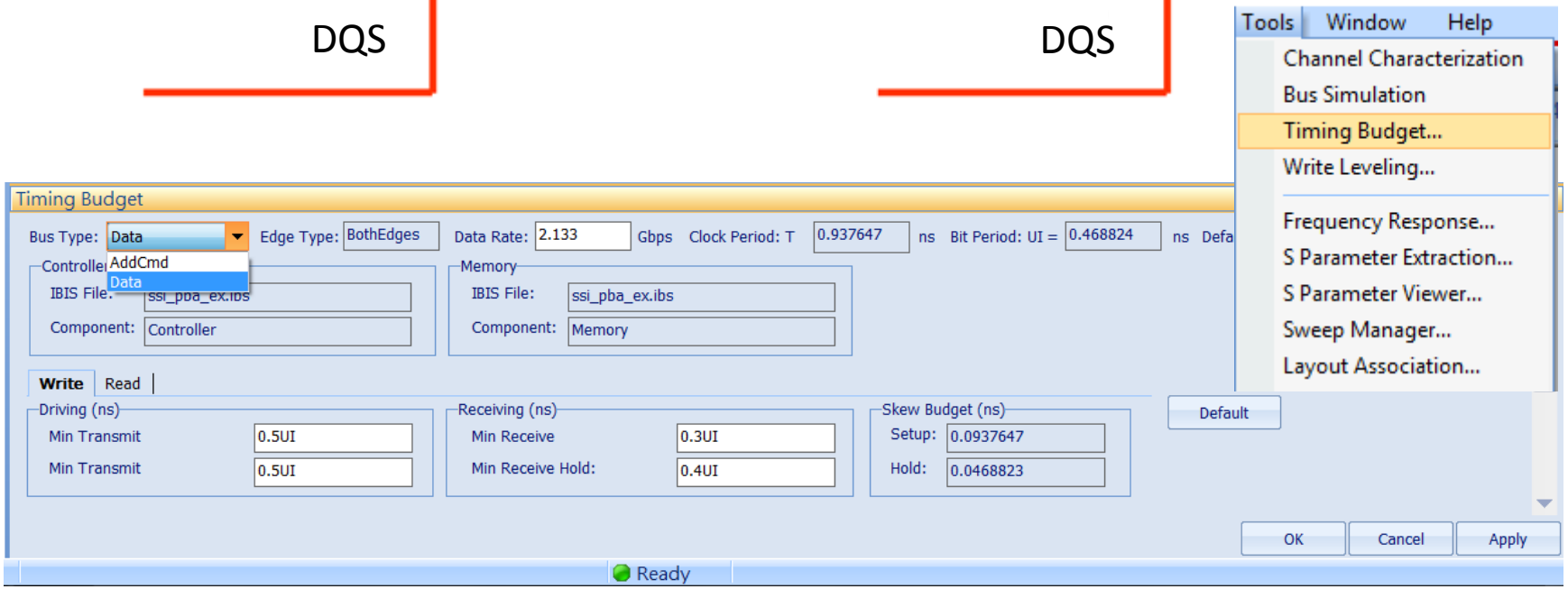
- SSO/SSN Analysis in SystemSI
- Guided of workflow
- Channel simulator for BER consideration < 1e-16
- JEDEC specification measurement Report



Timing Budgets – Setup/Hold time specification

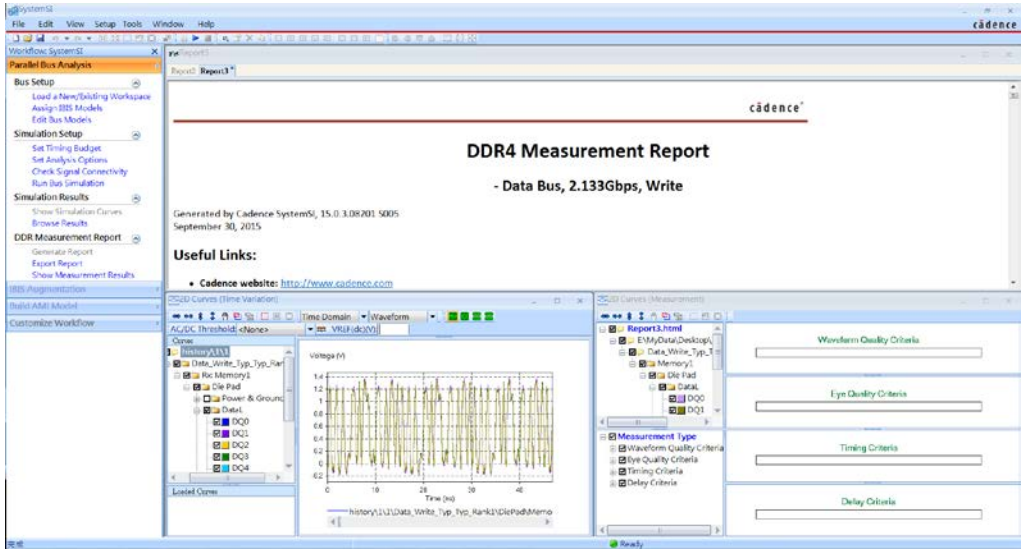






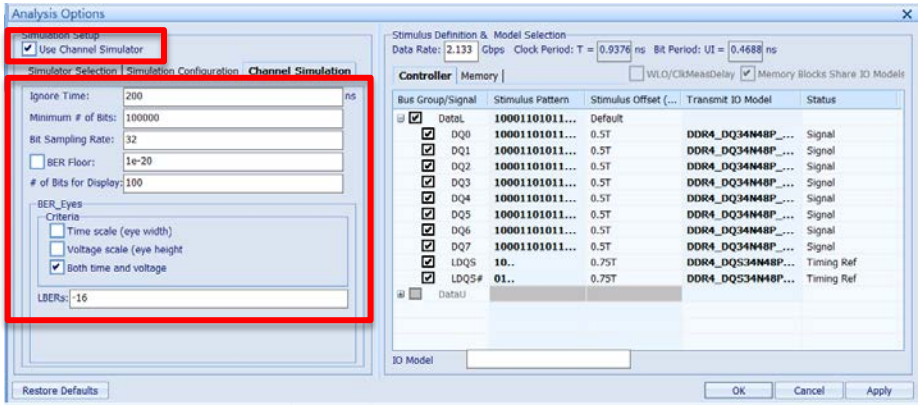
JEDEC Compliance specification Measurement Report

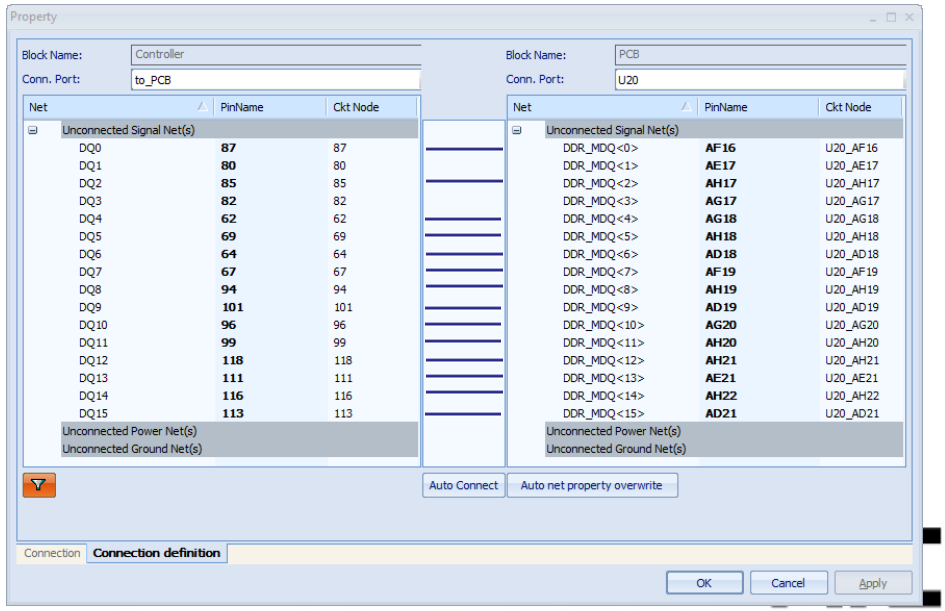
- Automatic waveform measurements post-processing to generate reports
- Use the browser for quick observation waveform
- The report contains a table of contents format :
  - Waveform Quality
  - Overshoot
  - DQ Mask (DDR4)
  - Timing Margin (setup/hold)
  - Delays & skews
  - Corresponding JEDEC specification parameters explanation



Analysis Options

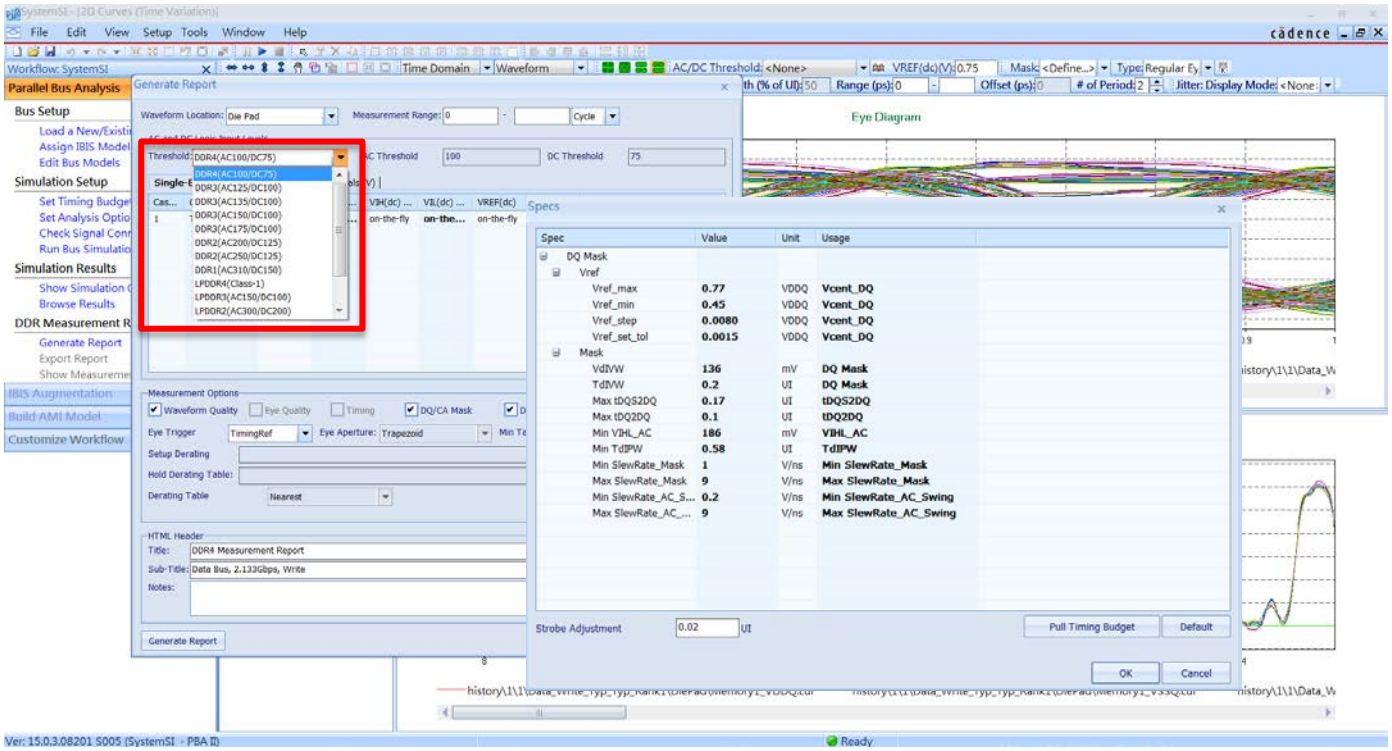
- Channel simulation techniques employeed.
- Simulate with IBIS or non-IBIS device models.
- User can Modify Minimum number of bits and BER Eyes elastically setting .
- MCP Header simple operation be fast connection relationship (Net,Pin,Ckt) between each block.





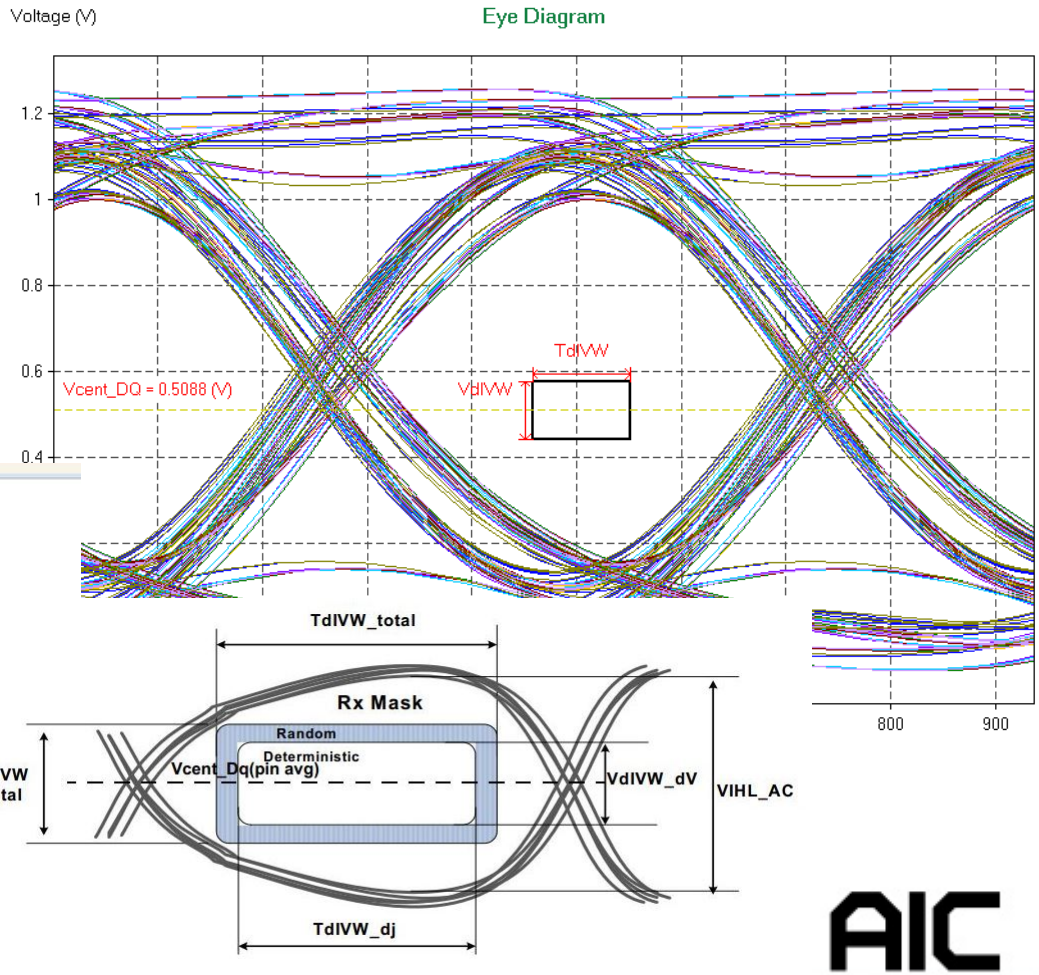
JEDEC Specification Generator Report Support

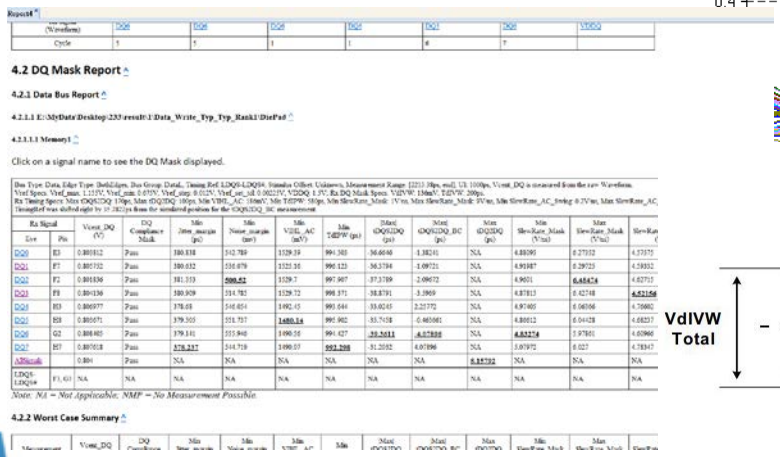
- DDR4/LPDDR4/DDR3 threshold support
- DQ mask Spec parameters
- Measure VREF(Vcent) on-the-fly



DQ Rx Mask Support in SystemSI

- Derive Vcent_DQ level on-the-fly from raw waveforms for each DQ signal
- Automatically position and evaluate DQ mask vs. eye





4.2 DQ Mask Report

4.2.1 Data Bus Report

Click on a signal name to see the DQ Mask displayed.

4.2.2 Worst Case Summary

Summary

- DDR4 new challenges
  - 20% power saving from 1.5 V to 1.2 V
  - Fast transmission speed, grave challenge of timing margin
- New analysis techniques are required to evaluate Rx Mask for Data per JEDEC specifications.
- Employed channel simulator technique for BER < 1E-16 can save calculation time.
- Power aware SSO analysis can not be ignored.
- JEDEC type compliance sign-off report for DDR4.

Thank you !