High Speed Serdes Signal Design Analysis with CTLE

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ADLINK TECHNOLOGY INC.

Abstract

- Source of Signal Loss
- Pre-emphasis and Equalization
- USB 3.0 transmitter compliance test considerations
- USB 3.0 transmitter channel design case study
- Summary

Source of Signal Loss

The important consequence of frequency-dependent loss and rise-time degradation is ISI: The precise waveform of the bit pattern will depend on the previous bits that have passed by. ISI is a significant contributor to jitter.

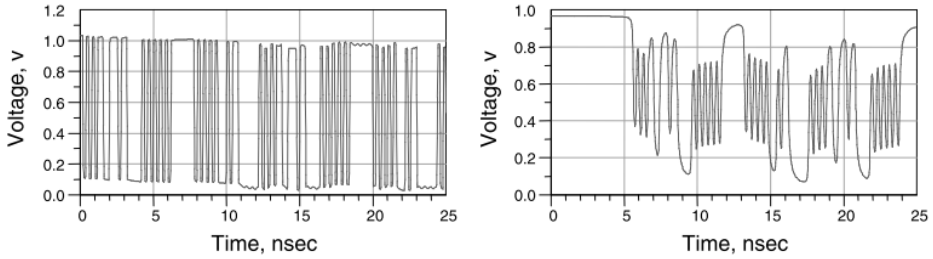


Figure 9-3 5-Gbps pseudorandom bit stream. Left: bit pattern when the rise time is much shorter than the bit period. Right: bit pattern when the rise time is comparable to the bit pattern, causing pattern-dependent voltage levels or intersymbol interference.

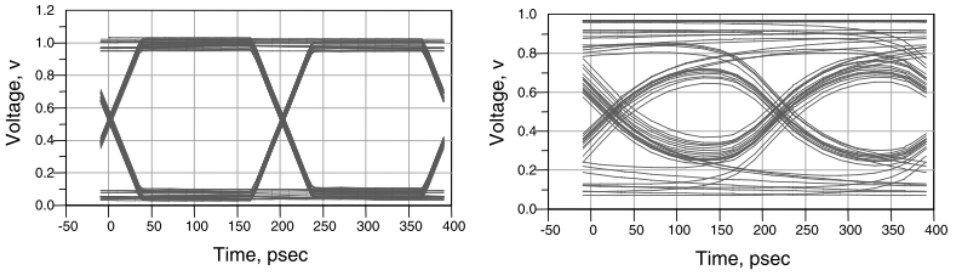


Figure 9-4 Eye diagrams of a 5-Gbps pseudorandom bit stream. Left: little loss. Right: same bit pattern when there is a lot of loss, showing the collapse of the eye diagram, and increased jitter, indicated by the widening of the cross-over regions.

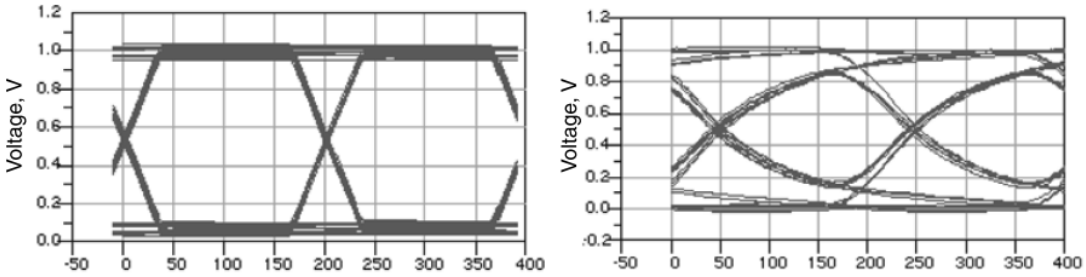


Figure 9-5 Eye diagrams of a 5-Gbps pseudorandom bit stream. Left: little loss. Right: same bit pattern still with no loss, but a 4-pF capacitive discontinuity from four through-hole vias.

1. Radiative loss
2. Coupling to adjacent traces
3. Impedance mismatches ⭐
4. Conductor loss
5. Dielectric loss

Source of Signal Loss

It is important to note that the resistivity of copper, and most conductors, is very constant with frequency. Above about 10 MHz, the resistance per length of the signal path will be frequency dependent. Skin depth is driven by the need for the currents to take the path of the lowest impedance, which is dominated by the loop inductance at higher frequencies.

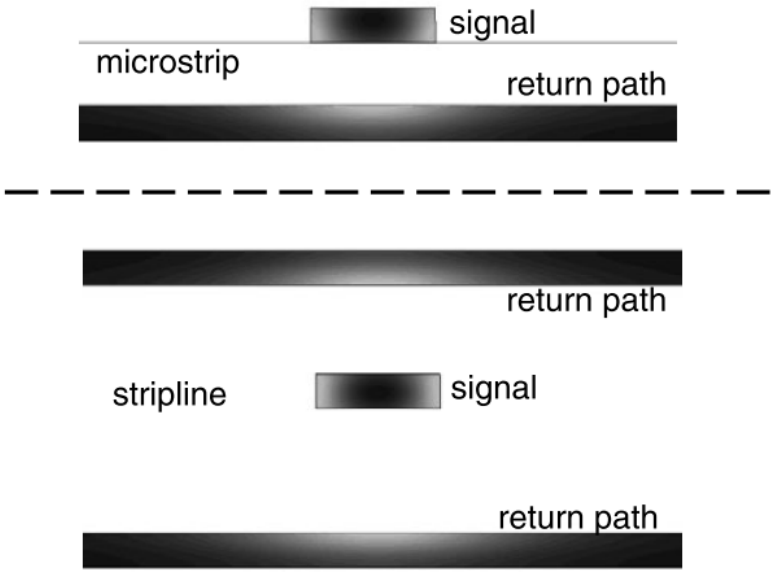


Figure 9-6 Current distribution in 1-ounce copper, for near 50-Ohm lines, at 10 MHz, showing onset of current redistribution due to skin-depth effects. Top: microstrip. Bottom: stripline. The lighter the color, the higher the current density. Simulated with Ansoft's 2D Extractor.

$$R = \rho \frac{Len}{w \times \delta}$$

where:

R = the resistance of the line, in Ohms

ρ = the bulk resistivity of the conductor, in Ohm-inches

Len = the length of the line, in inches

w = the line width, in inches

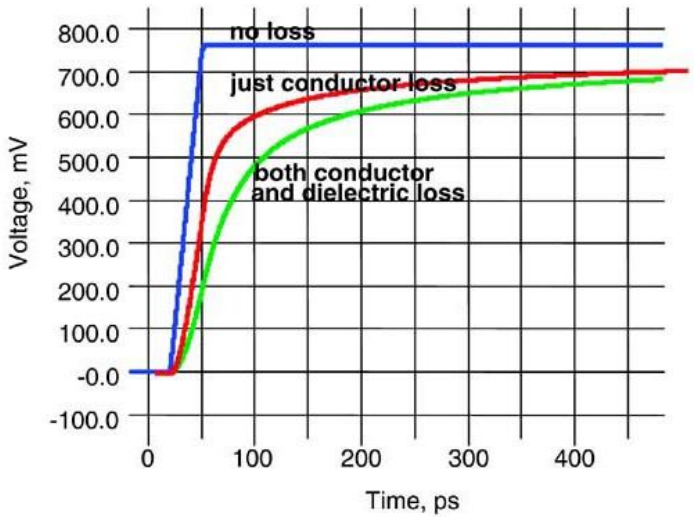
δ = the skin depth of the conductor, in inches

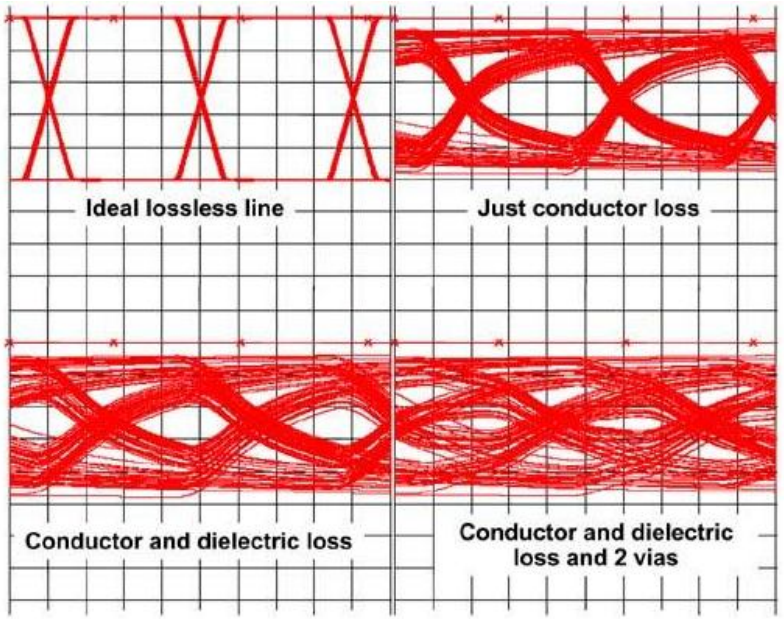
Source of Signal Loss

The dissipation factor, usually written as the tangent of the loss angle, tan(δ), and also abbreviated sometimes as Df, is a measure of the number of dipoles in the material and how far each of them can rotate in the applied field.

The ratio of the powers, in dB, is:

$$r_{dB} = 10 \times \log\left(\frac{P_1}{P_0}\right) = 10 \times \log\left(\frac{V_1^2}{V_0^2}\right) = 10 \times 2\log\left(\frac{V_1}{V_0}\right) = 20\log\left(\frac{V_1}{V_0}\right) \qquad (9\text{-}52)$$





Voltage Ratio	Power Ratio	dB
100	10,000	40
10	100	20
2	4	6
1.4	2	3
1	1	0
0.7	0.5	-3
0.5	0.25	-6
0.1	0.01	-20
0.01	0.0001	-40

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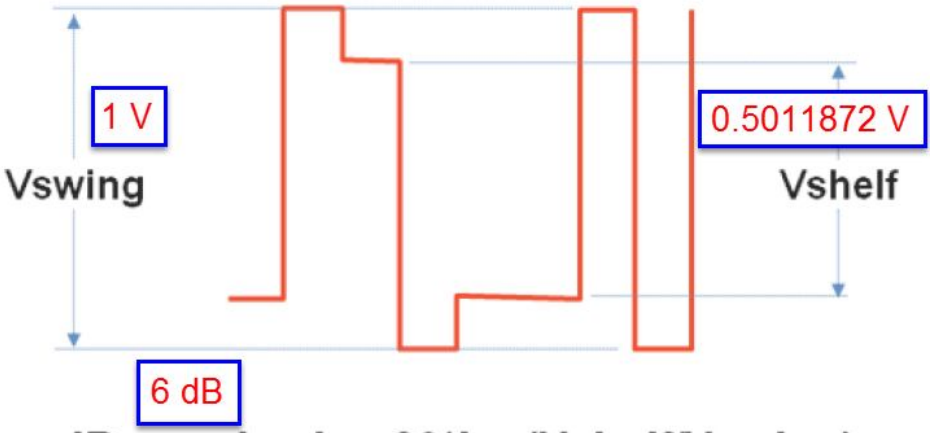
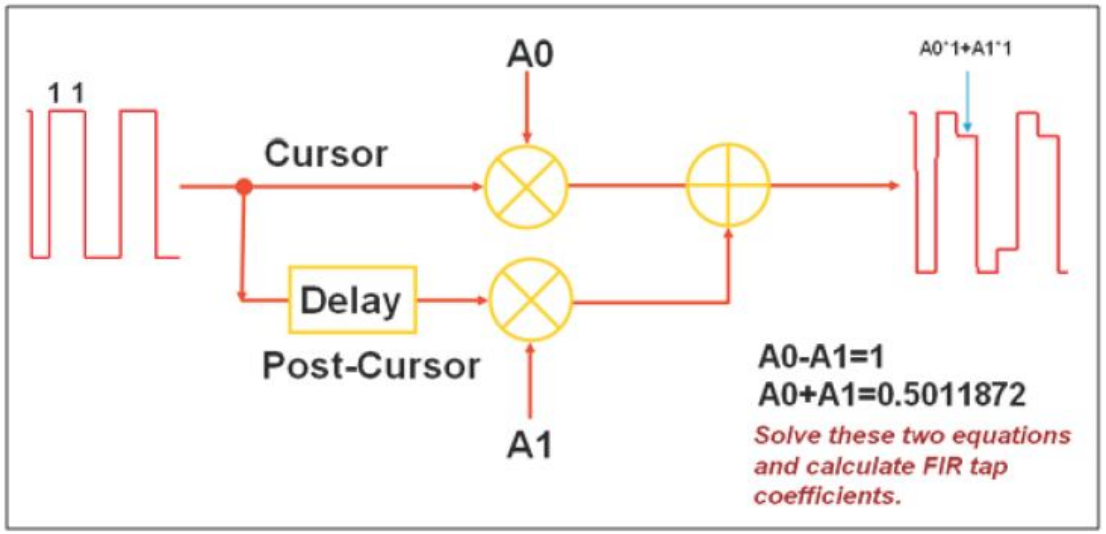
Pre-emphasis and Equalization



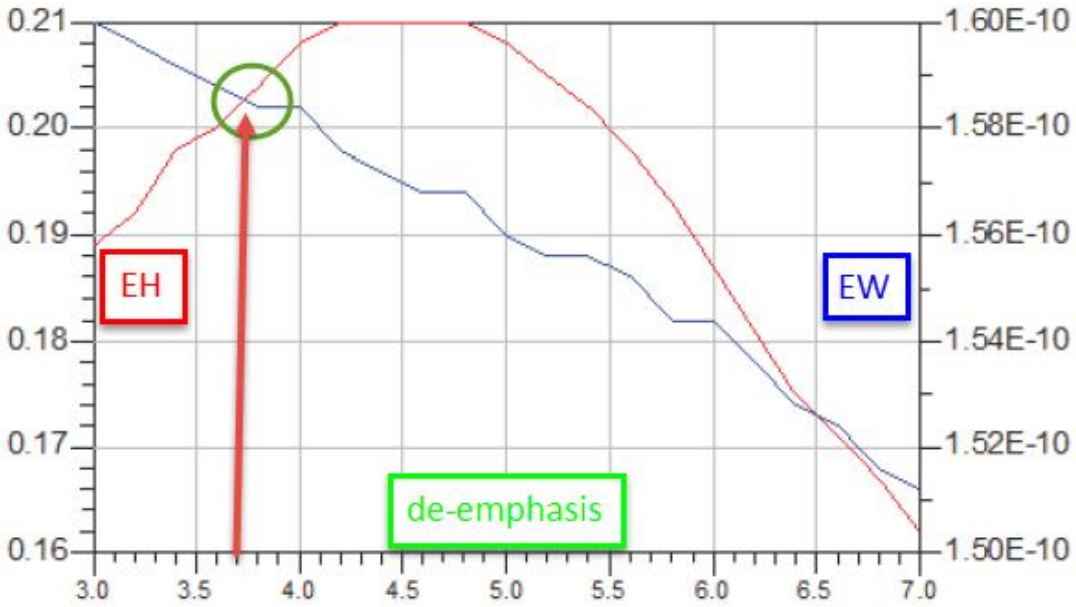


A de-emphasized waveform is defined in terms of the voltage levels called Vshelf and Vswing.

Vshelf is calculated first for a given level of de-emphasis.

Each unique channel has some optimum amount of transmitter de-emphasis that will deliver the best eye performance.

Pre-emphasis and Equalization



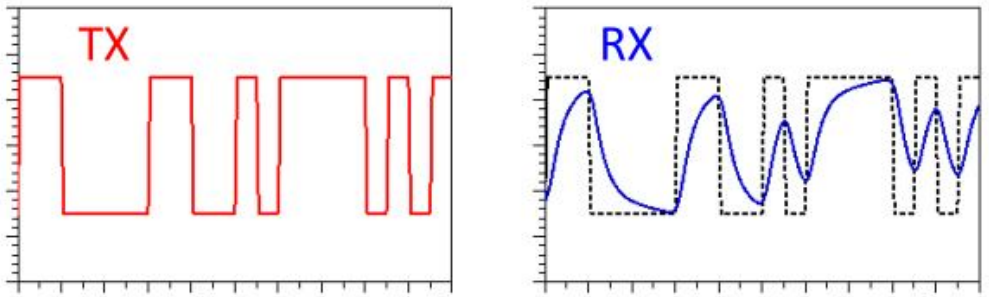


Figure 1. High frequency loss results in signal deterioration at RX

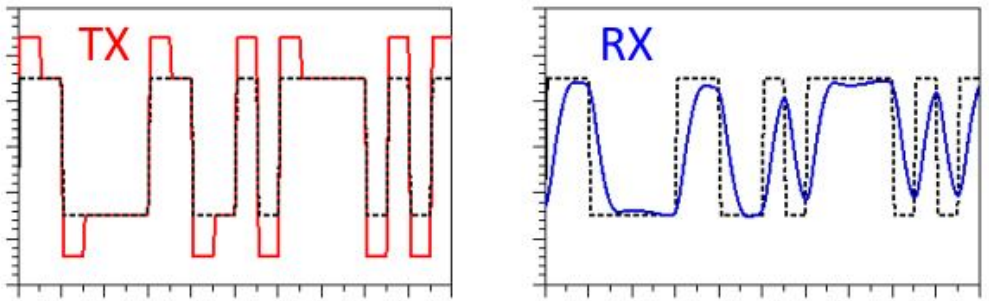
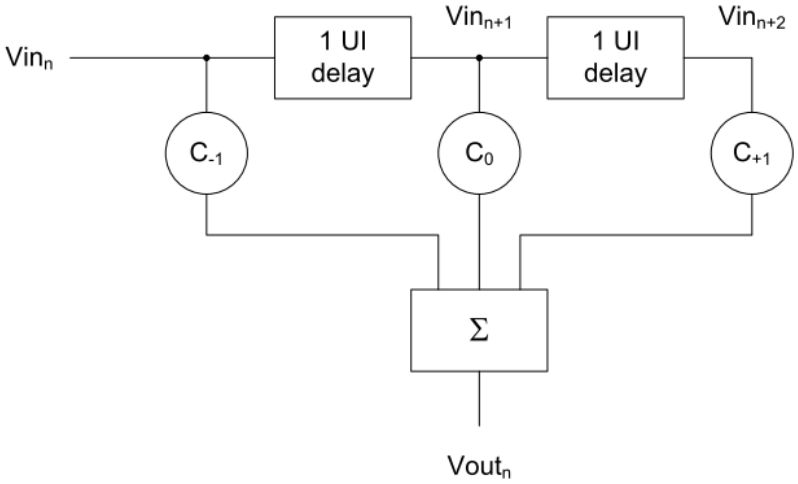


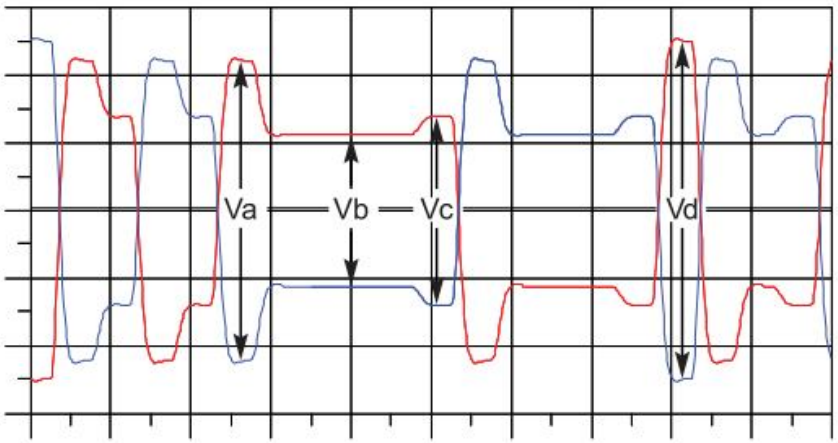
Figure 2. High frequency compensation with pre-emphasis

Cursor tap1 = (1+ Vshelf) / 2

Post cursor tap2 = tap1 - 1

Pre-emphasis and Equalization





De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

PCI EXPRESS BASE SPECIFICATION, REV. 3.0

Pre-emphasis and Equalization

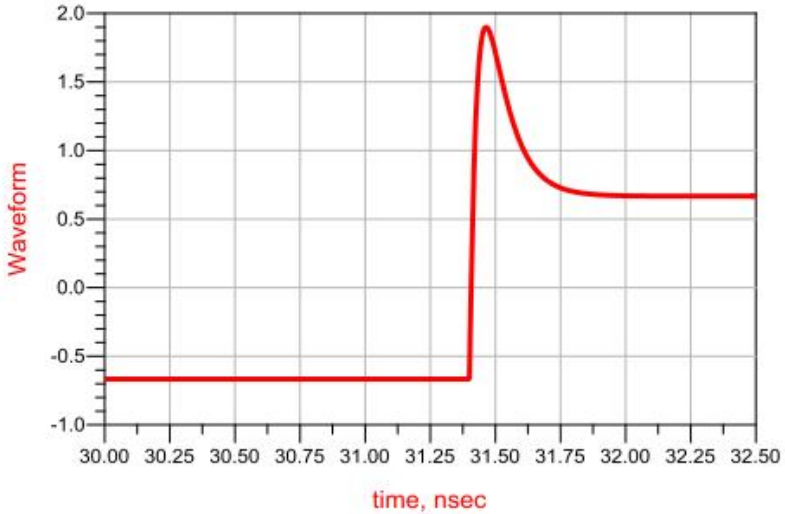
$$(10) \qquad H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

where A_{dc} is the DC gain

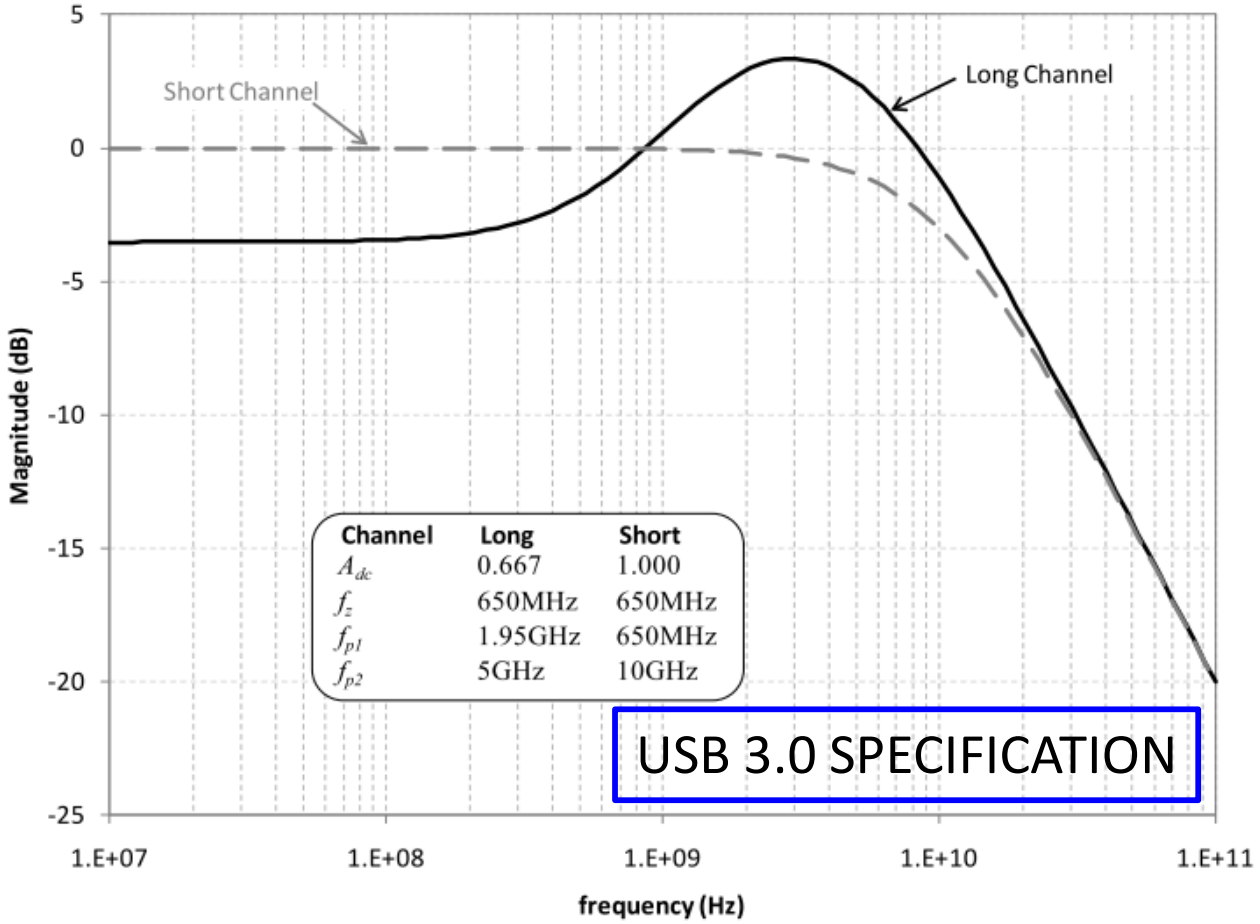
$\omega_z = 2\pi f_z$ is the zero frequency

$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency

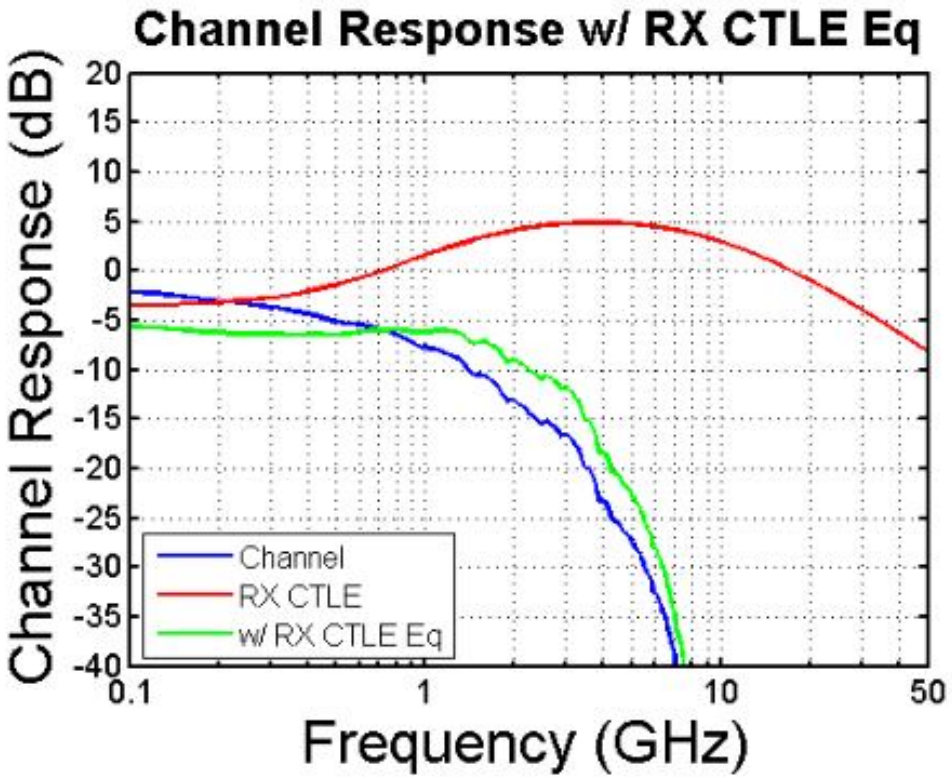
$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency



Step response of the CTLE



Pre-emphasis and Equalization



When a high speed digital signal propagates through a lossy channel, RX CTLE is used to boost high frequency components of the signal to compensate high frequency channel loss.

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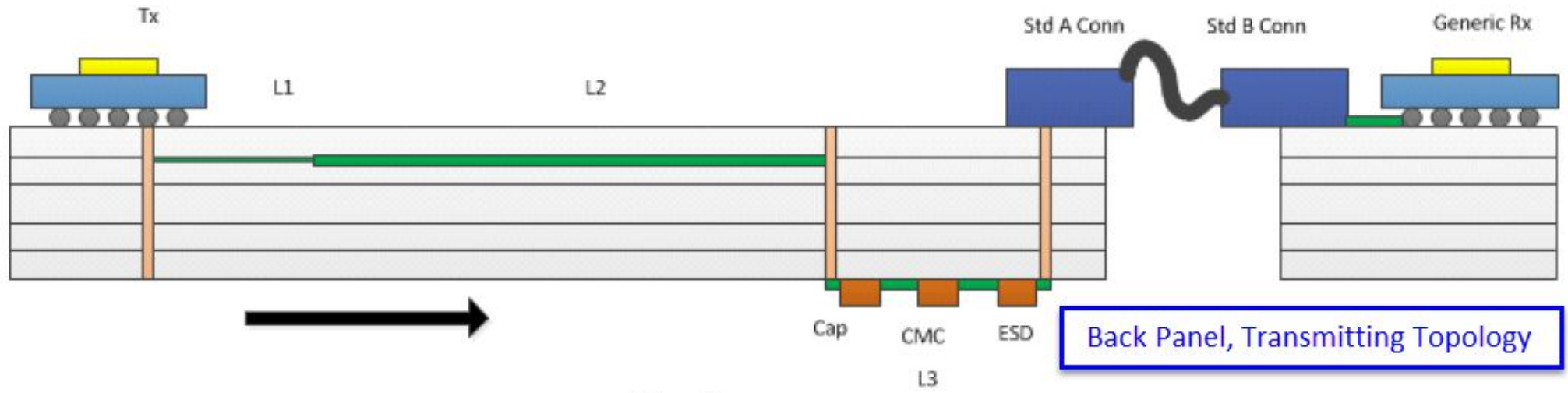
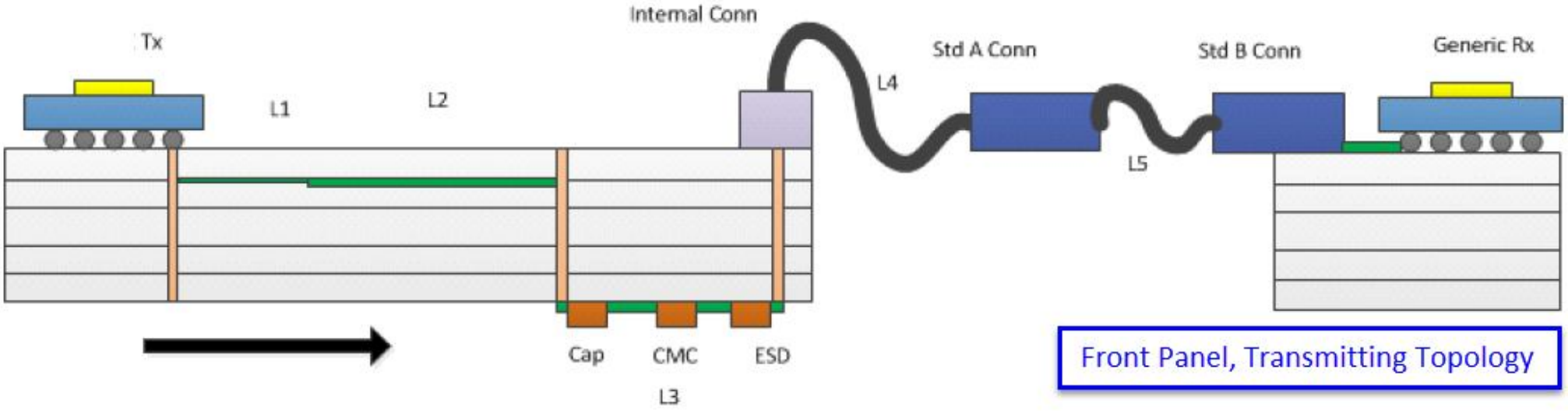
- USB 3.0 transmitter channel design case study
- Summary

USB 3.0 transmitter compliance test considerations



Back Panel, Transmitting Topology



Front Panel, Transmitting Topology

USB 3.0 transmitter compliance test considerations

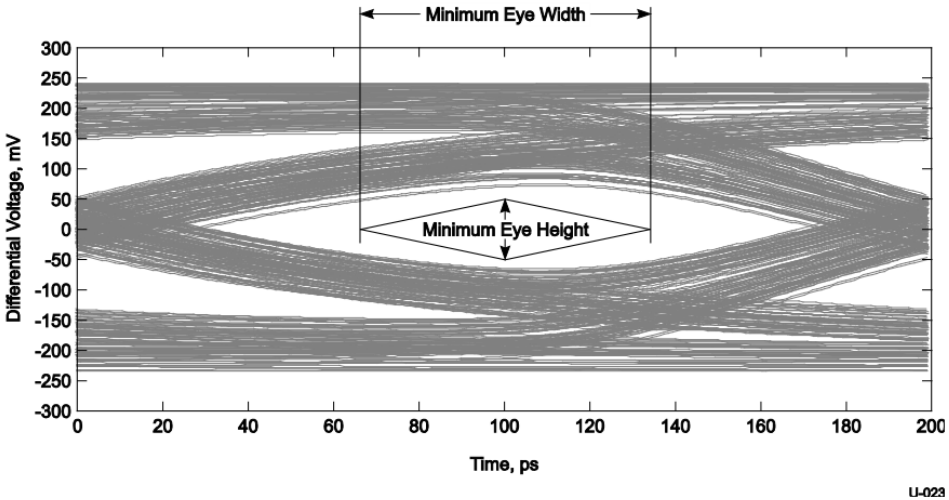
Table 6-19. Normative Transmitter Eye Mask at Test Point TP1

	5GT/s			10GT/s				
Signal Characteristic	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**	**Units**	**Note**
Eye Height	100		1200	70		1200	mV	
Dj			0.43			0.530	UI	
Rj			0.23			0.184	UI	
Tj			0.66			0.714	UI	

Notes:

1. Measured over 10^6 consecutive UI and extrapolated to 10^{-12} BER.
2. Measured after receiver equalization function.
3. Measured at end of reference channel and cables at TP1 in Figure 6-19.
4. The eye height is to be measured at the minimum opening over the range from the center of the eye ± 0
5. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.

The compliance testing setup is shown in Figure 6-19. All measurements are made at the (TP1), and the Tx specifications are applied after processing the measured data with the c reference equalizer transfer function described in the next section.



Gen 1 eye mask

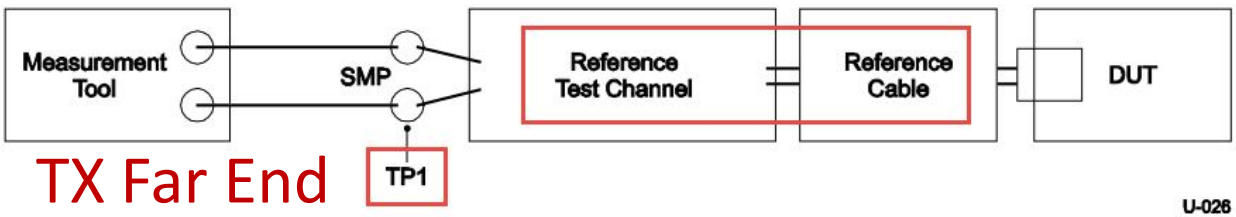


Figure 6-19. Tx Normative Setup with Reference Channel

USB 3.0 transmitter compliance test considerations

Table 3. Summary of transmitter compliance tests

Parameter	Symbol	Specification	Data Pattern	Notes
Differential Swing	$V_{TX-DIFF-PP}$	0.8V – 1.2V	CP8	4, 5
De-emphasis	$V_{TX-DE-RATIO}$	3.0dB – 4.0dB	CP7	4, 5
DC differential impedance	$R_{TX-DIFF-DC}$	72Ω - 120Ω	CP8	4, 5
Deterministic Jitter	Dj	0.465UI (max)	CP0	1, 2, 4
Random Jitter	Rj	0.30UI (max)	CP0, CP1	1, 2, 4
Total Jitter	Tj	0.66UI (max)	CP0	1, 2, 4
Eye Height		100mV (min)	CP0	1, 2, 3, 4

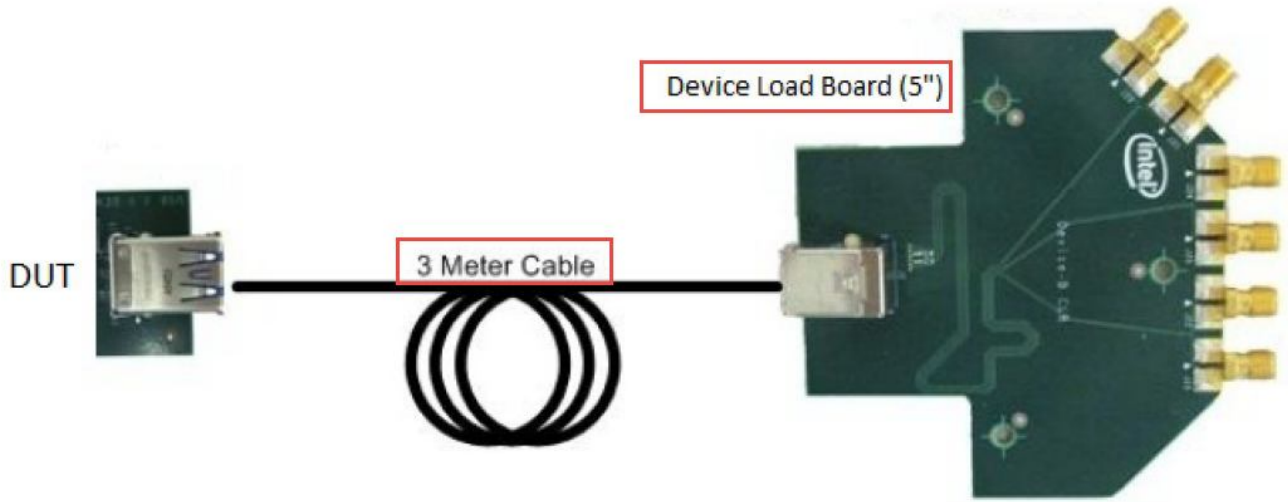
Notes:

1. Measured over 10^6 consecutive UI and extrapolated to 10^{-12} BER. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.
2. Measured after receiver equalization function.
3. The eye height is to be measured at the maximum opening (at the center of the eye width ± 0.05 UI).
4. All specified values in this table were extracted from tables 6-10 and 6-12 of the USB 3.0 Specification. In case of conflict, the values in the USB 3.0 Specification supersede those contained herein.
5. Optional measurement for characterization and troubleshooting purposes.

USB 3.0 transmitter compliance test considerations

The "host compliance test channel" in Figure 6(a) is used to test compliance for host designs. The compliance channel includes a 3m length SuperSpeed cable (the maximum allowed by the spec) connected to a printed circuit board that has 5" of trace providing connection between a standard device connector and SMAs that then connect to a oscilloscope. The five inch trace length represents a maximum loss device design (PCB plus package).

USB 3.0 SuperSpeed Equalizer Design Guidelines



(a) Host compliance test channel

USB 3.0 transmitter compliance test considerations

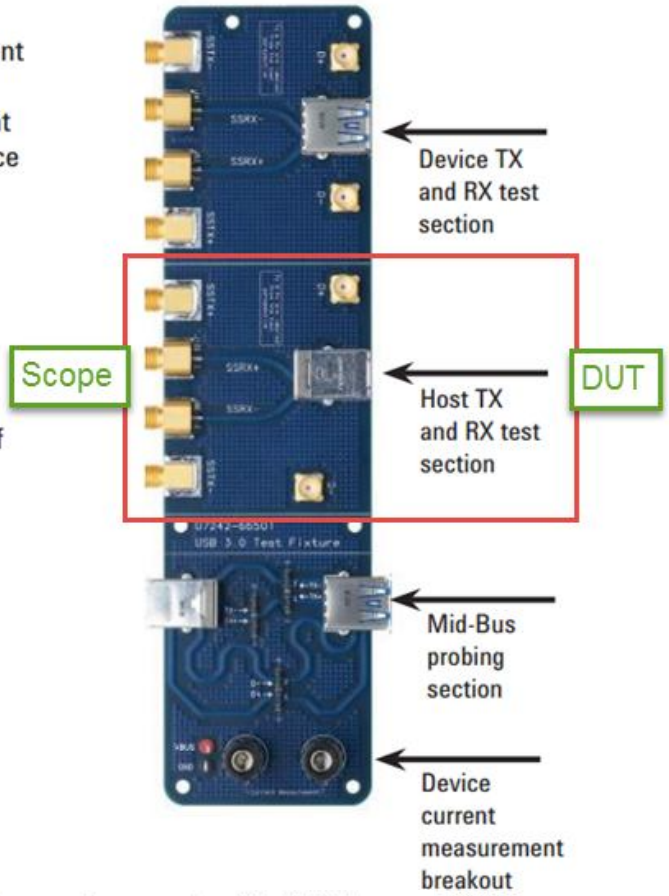
Key specifications:

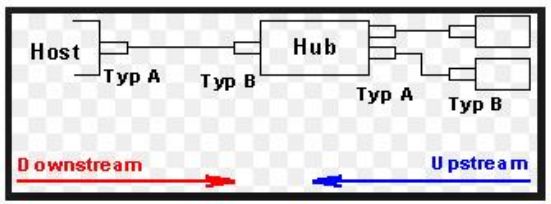
- Provides test point access for transmitter measurements
- Single-ended measurements as required by the USB 3.0 specification for transmitter and receiver validation and compliance testing
- Differential measurements using active probes allow probing of active bus transactions for debug and verification testing
- USB 3.0 power probing features for easy measurement of transient and steady state power states

Description:

The U7242A USB 3.0 test fixture will help simplify the USB 3.0 measurement process by providing access to the transmitter and receiver measurement points required for USB 3.0 compliance testing. It has been designed for direct SMA connections for easy and accurate measurements with direct connections to the oscilloscope and J-Bert SMA connections. It also includes probing connections for InfiniiMax active differential probes for the characterization and testing of active bus signaling of USB 3.0 and USB 2.0 traffic.

The U7242A USB 3.0 superspeed electrical test fixture provides signal accessibility and probing for USB 3.0 devices, host and hub upstream and downstream ports.

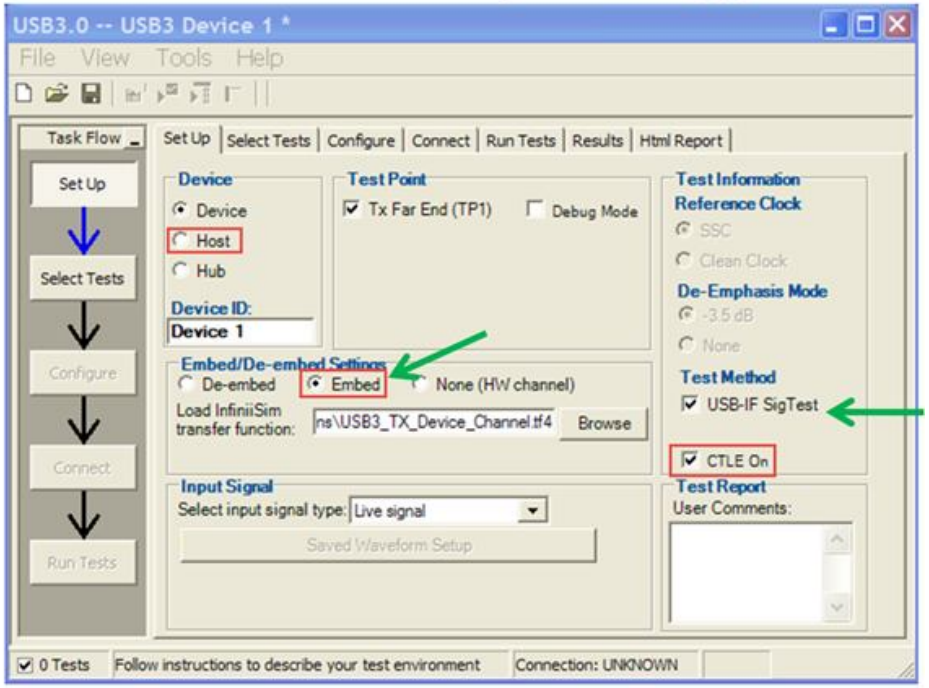




- Accurate fixture de-embed and compliance channel embedding is performed with VNA s-parameter characterization and Agilent InfiniiSim toolset.

USB 3.0 transmitter compliance test considerations

U7243A USB 3.0 TX Compliance Application



Use “KEYSIGHT_ENA_HOST_CHANNEL_3MCABLE.s4p” to express the “host compliance test channel”.

USB3_TX_Host_Channel.tf4

```
4
5
6 ktDef.Transmitter.FileName='C:\Documents and Settings\Administrator\Desktop\USB30\U7242 SHORTCABLE FORHOST.s4p';
7 ansmitter.FileName='C:\Documents and Settings\Administrator\Desktop\USB30\DEVICE_3MCABLE.s4p';SimCktDef.Transmit
```

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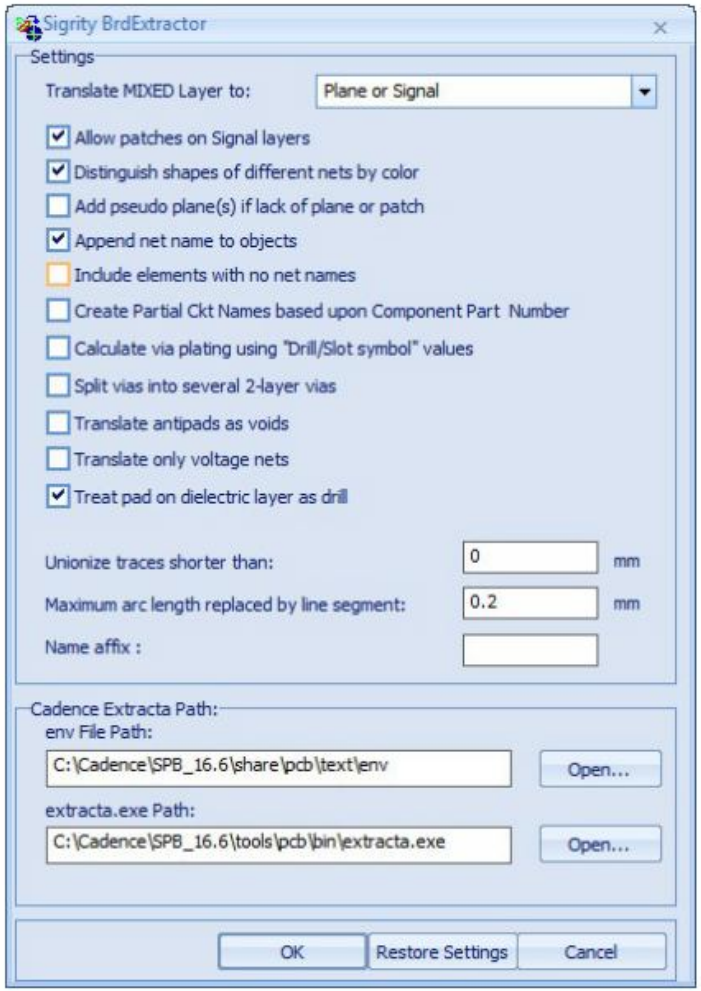
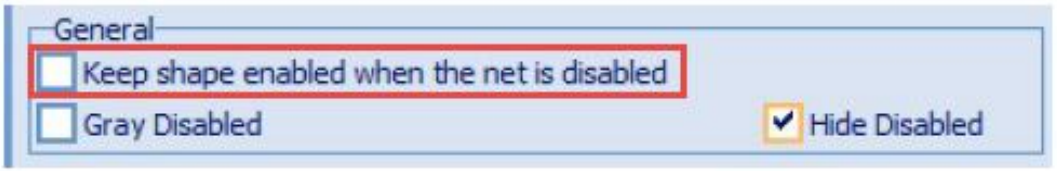
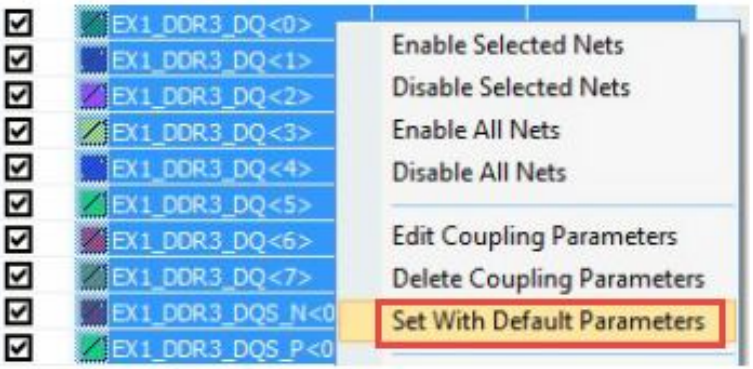


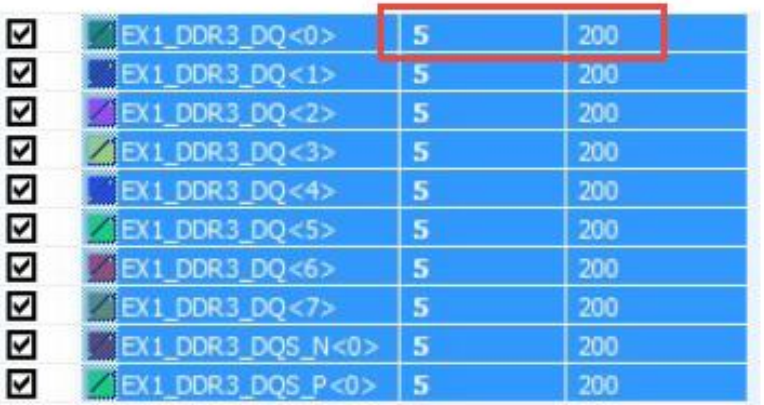
Via plating can also be translated if specified in the Allegro database "Drill / Slot symbol" information.

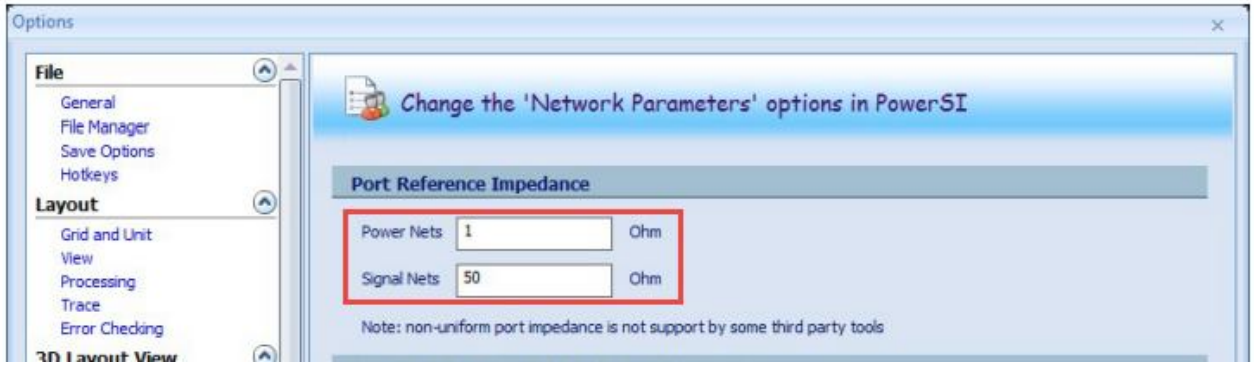
If non-functional pads will not be removed, select option "split vias into several 2-layer vias".

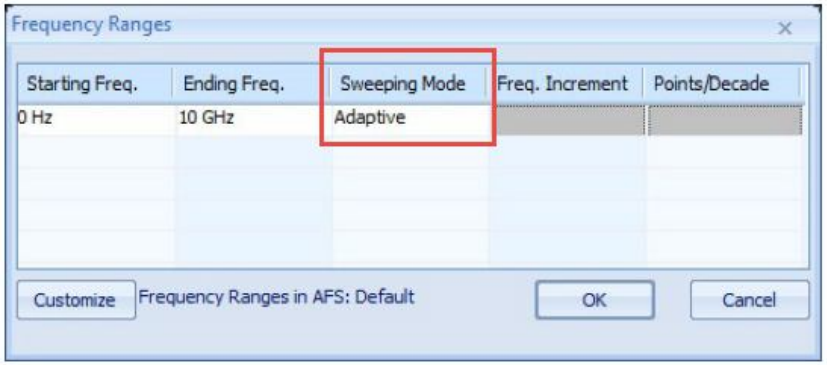


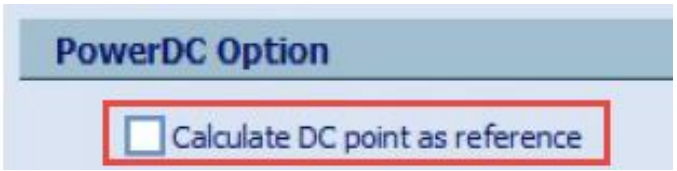
USB 3.0 transmitter channel design case study





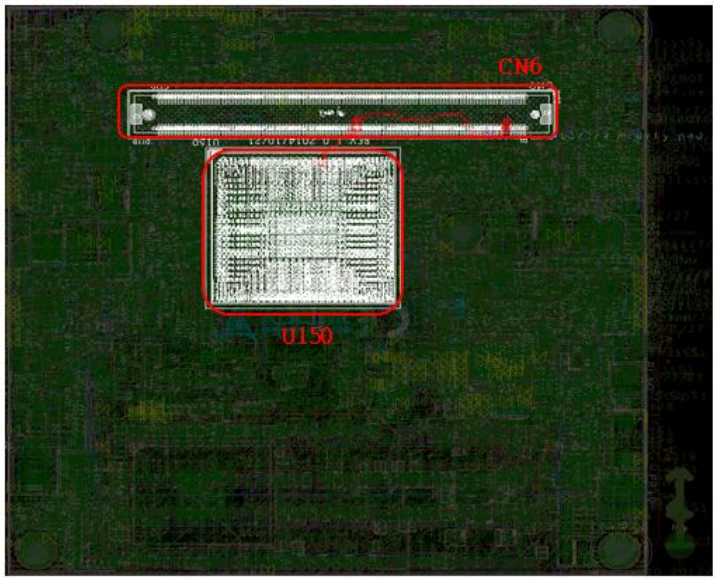




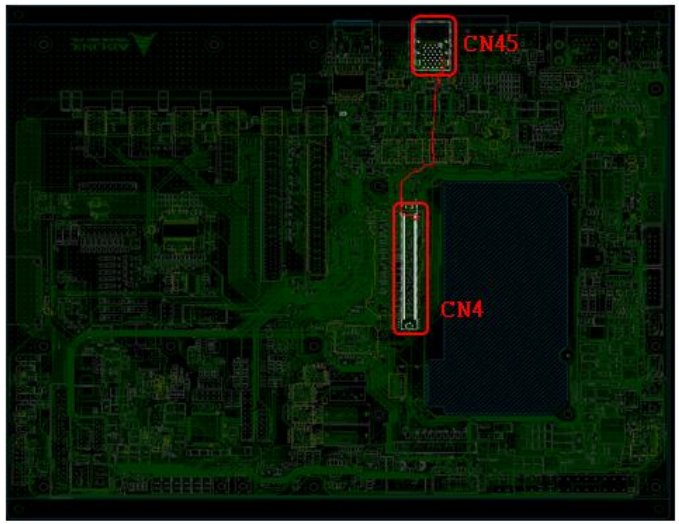


USB 3.0 transmitter channel design case study

Routing (Module Board)

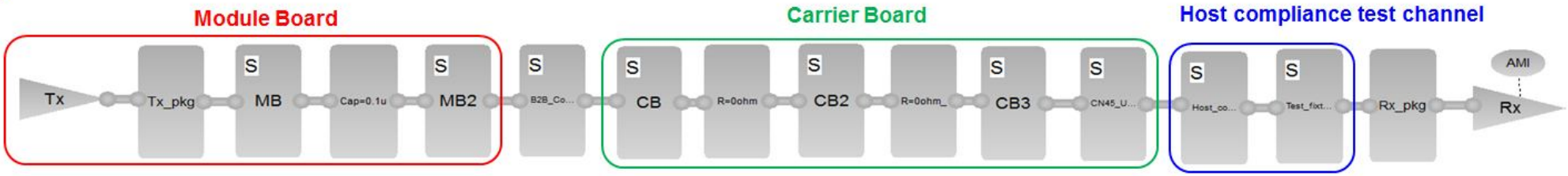


Routing (Carrier Board)



Topology

TX



USB 3.0 transmitter channel design case study

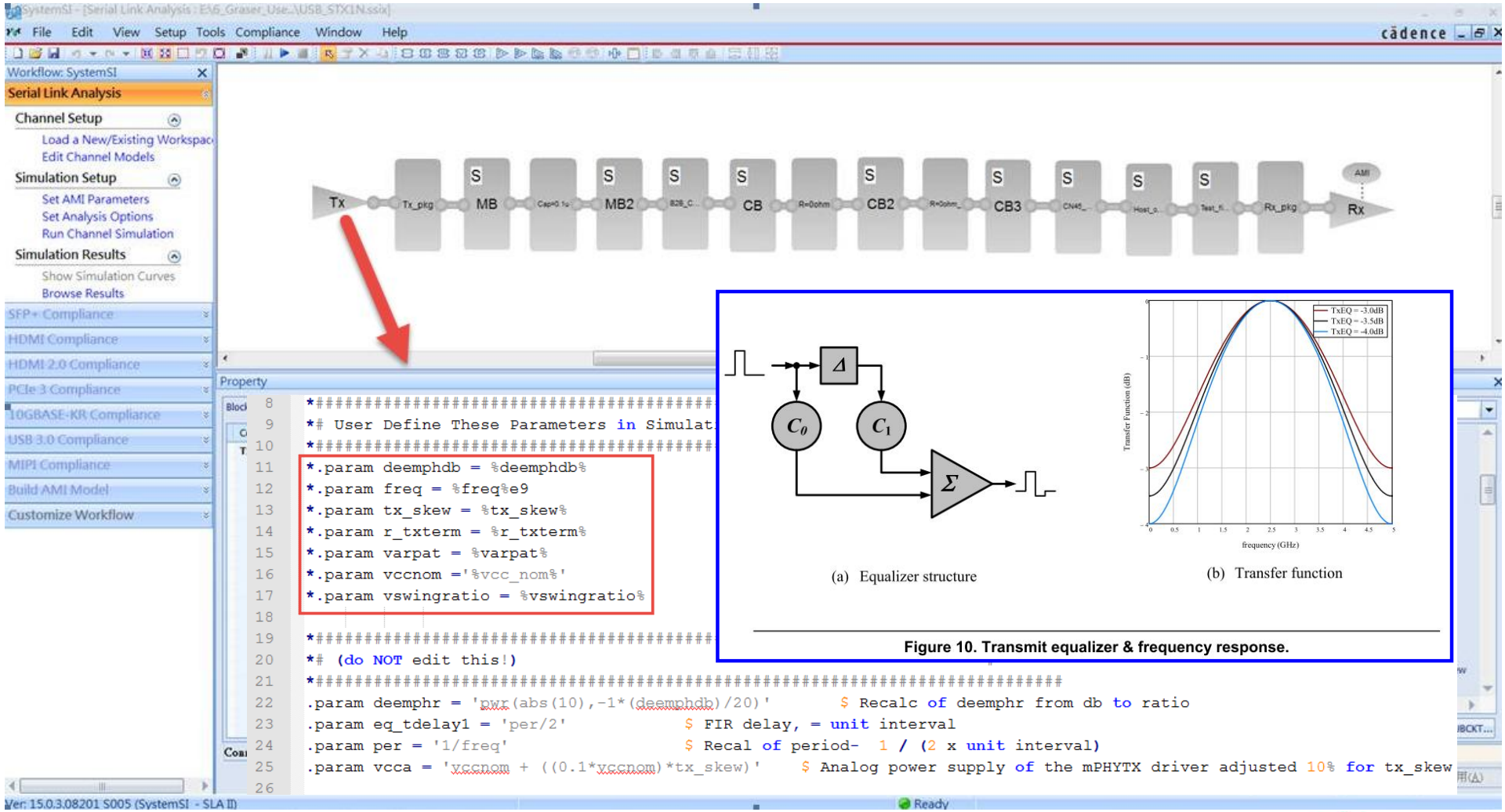
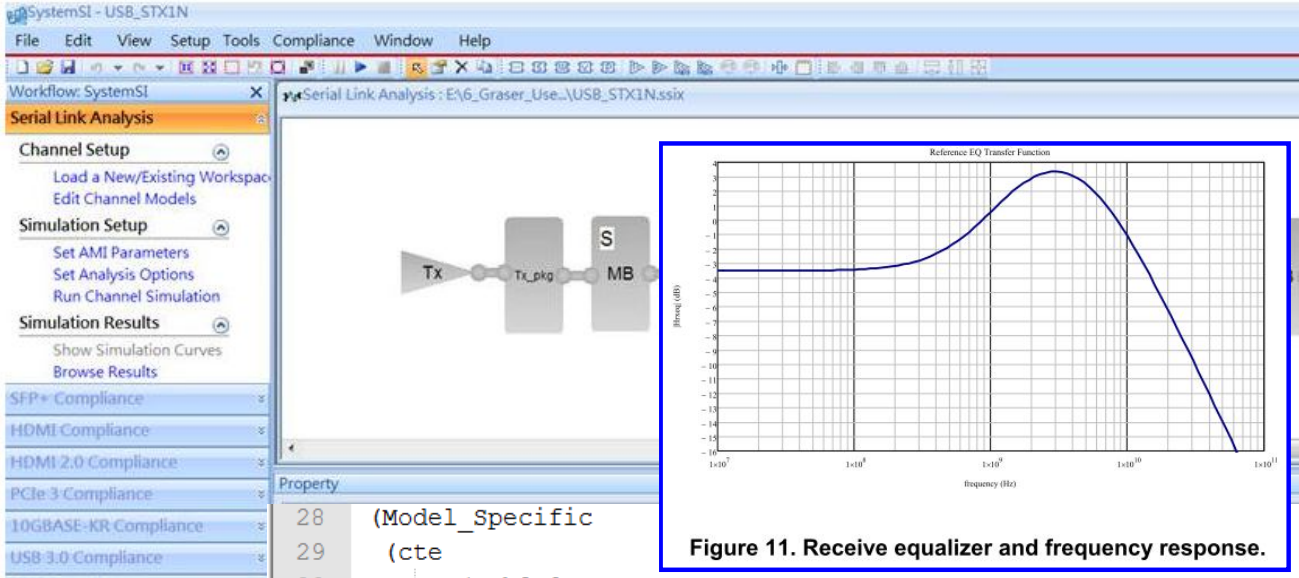


Figure 10. Transmit equalizer & frequency response.

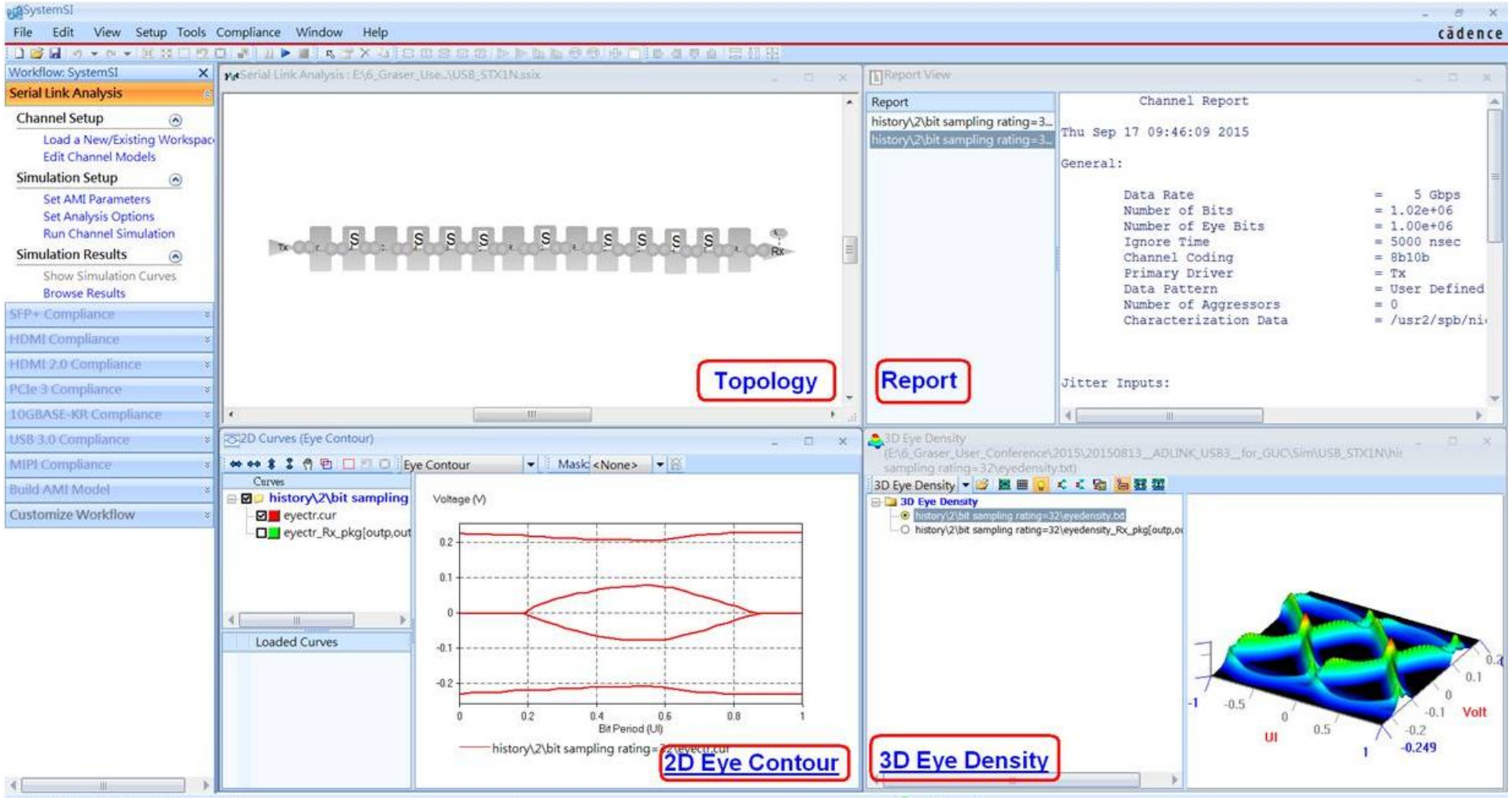
USB 3.0 transmitter channel design case study



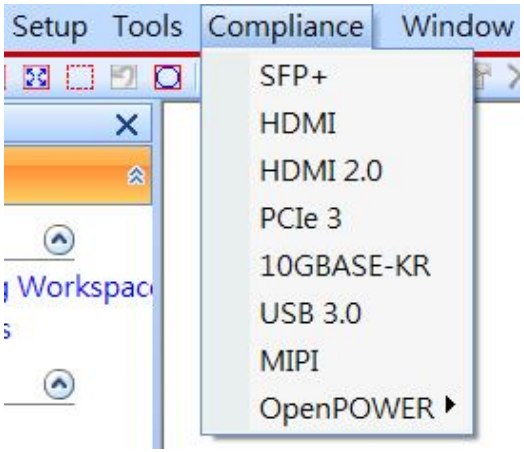

```
28  (Model_Specific
29   (cte
30       (usb3.0
31           (Adc (Usage In)(Type Float) (Range 0.667 0.1 1)(Default 0.667)(Description "DC Gain. 0.667 is
32           (fz (Usage In)(Type Float) (Range 650e6 600e6 700e6)(Default 650e6)(Description "Zero Frequenc
33           (fp1 (Usage In)(Type Float) (Range 1.9e9 650e6 3.0e9)(Default 1.9e9)(Description "First Pole F
34           (fp2 (Usage In)(Type Float) (Range 5.0e9 4.0e9 10.0e9)(Default 5.0e9 )(Description "Second Pol
35       )
36       (module_off (Usage In) (Type Integer) (List 0 1) (Default 0) (Description "Turn CTE module off"))
37   )
38   (cdr
39    (module_off (Usage In) (Type Integer) (List 0 1) (Default 0) (Description "Turn CDR module off"))
```

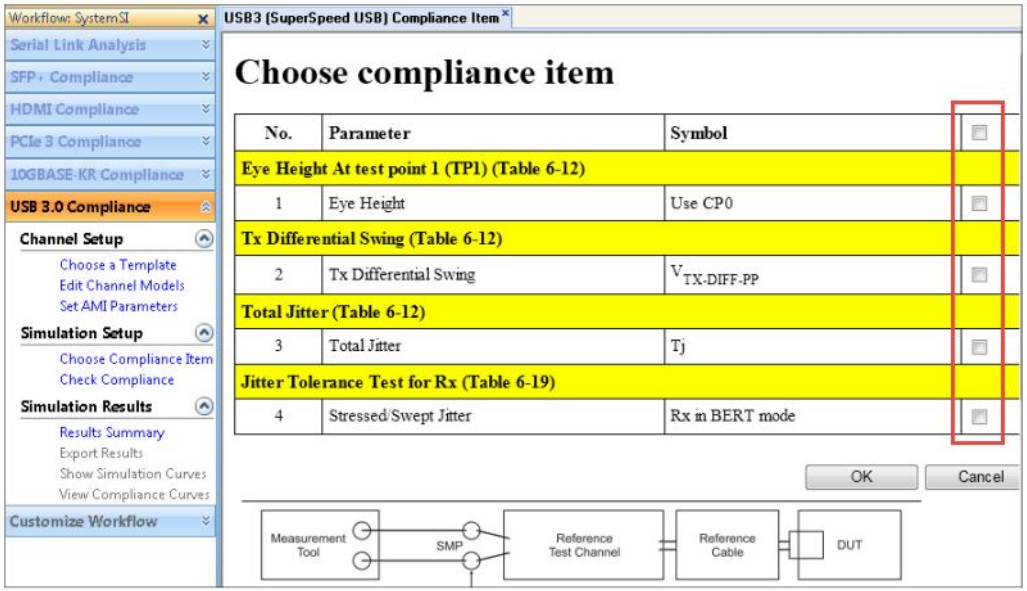
Figure 11. Receive equalizer and frequency response.

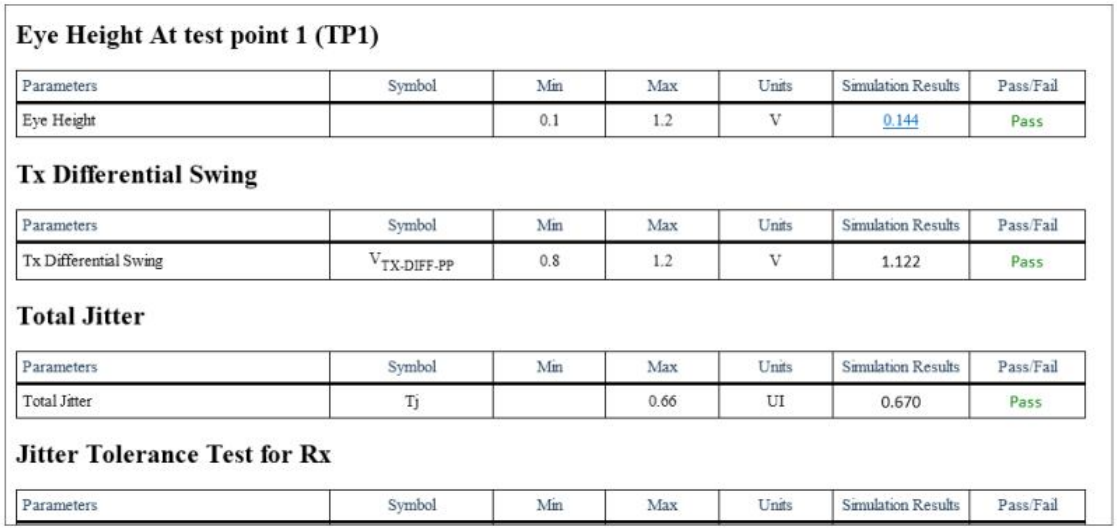
USB 3.0 transmitter channel design case study



USB 3.0 transmitter channel design case study

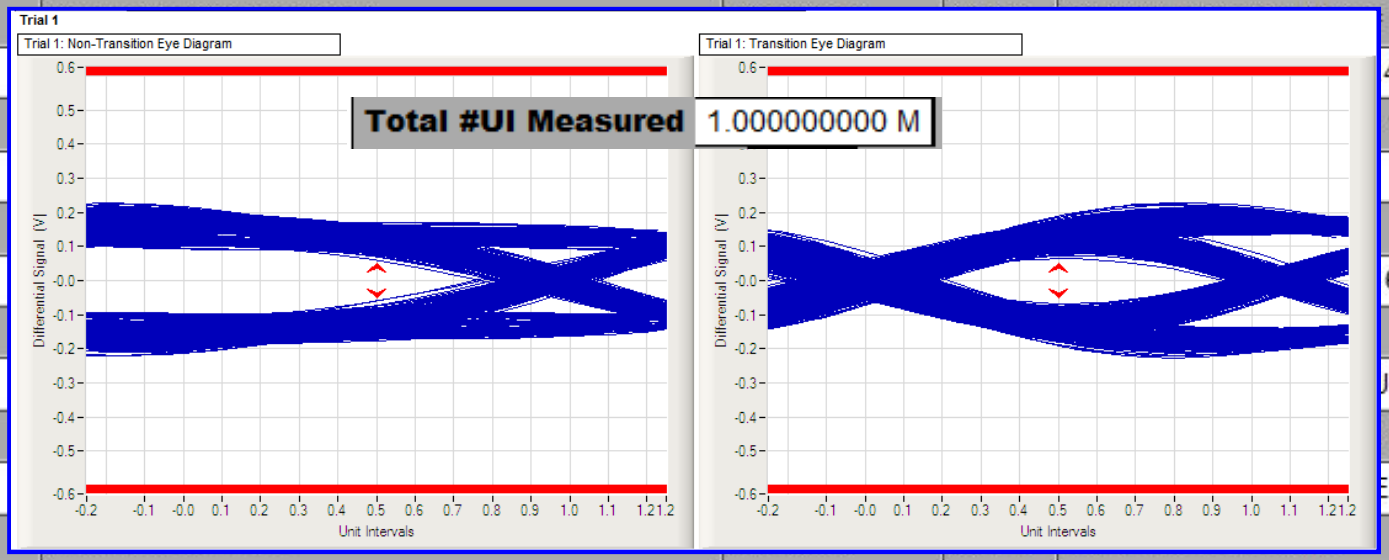






USB 3.0 transmitter channel design case study

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	5G LFPS Peak-Peak Differential Output Voltage	1.1051 V	23.7 %	800.0 mV <= VALUE <= 1.2000 V
✓	0	1				100.0000 ns
✓	0	1				4000 ⵒs
✓	0	1				14.0000 ⵒs
✓	0	1				
✓	0	1				
✓	0	1				60.0000 %
✓	0	1				
✓	0	1				UE <= -3.700000 kppm
✓	0	1				<= TSSCMax ppm
✓	0	1				E <= 33.000000 kHz
✓	0	1				
✓	0	1	5G Far End Random Jitter (CTLE ON)	112 mUI	51.3 %	VALUE <= 230 mUI
✓	0	1	5G Far End Maximum Deterministic Jitter (CTLE ON)	352 mUI	18.1 %	VALUE <= 430 mUI
✓	0	1	5G Far End Total Jitter at BER-12 (CTLE ON)	464 mUI	29.7 %	VALUE <= 660 mUI
✓	0	1	5G Far End Template Test (CTLE ON)	0.000	100.0 %	VALUE = 0.000
✓	0	1	5G Far End Differential Output Voltage (CTLE ON)	116.2 mV	1.5 %	100.0 mV <= VALUE <= 1.2000 V



Abstract

- Source of Signal Loss
- Pre-emphasis and Equalization
- USB 3.0 transmitter compliance test considerations
- USB 3.0 transmitter channel design case study
- Summary

Summary

1. Channel modeling, simulation and measurement can be critical to design success.

2. Using compliance kits in SystemSI automates the testing process.

3. We can use Non-IBIS model as the transmitter and receiver buffer model in SystemSI to conduct the large number of data bits simulation in a short time.

Simulation VS. Measurement		
Characteristic	Simulation	Measurement
When to use	Early on	Near the end
Requirements	Simulation software	Scope / VNA / prototype
Usage	1. Understand system margins 2. Making design tradeoffs 3. Design verification	Prototype verification
Limitations	1. Everything must be modeled 2. Not all effects can be included	1. Affects circuit performance 2. Needs places to probe
Advantages	1. Fix problems before prototype 2. Can probe anywhere 3. No need for physical prototype	1. Includes most effects 2. Close to reality

Thanks for your attention~