Taipei 10.16 2015 User Conference Graser

Allegro New Products - DFM / Rule Checkers

Eric / Graser

16 / Oct / 2015

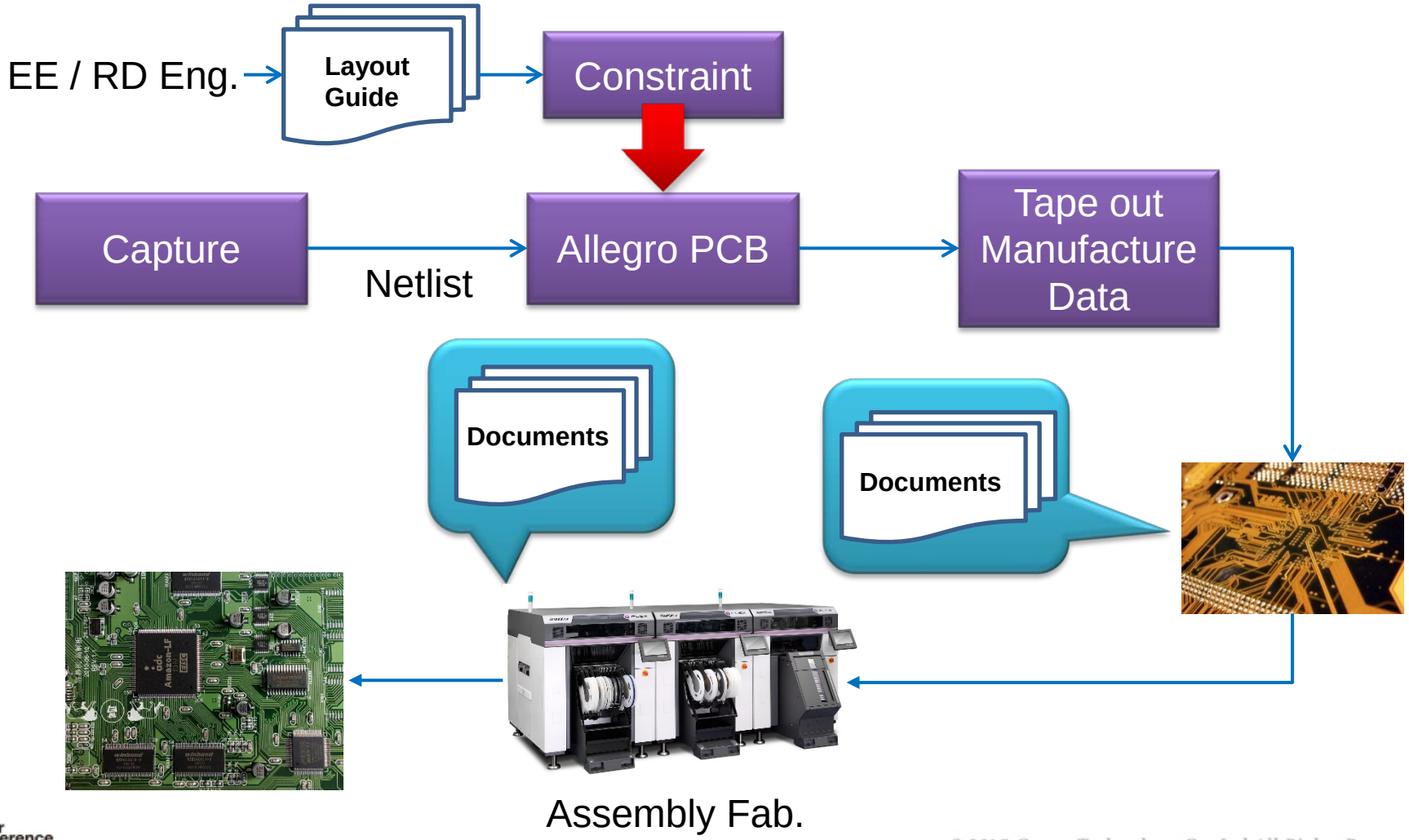
Topic

- Allegro DFM Checker
  in Allegro PCB Manufacturing Option

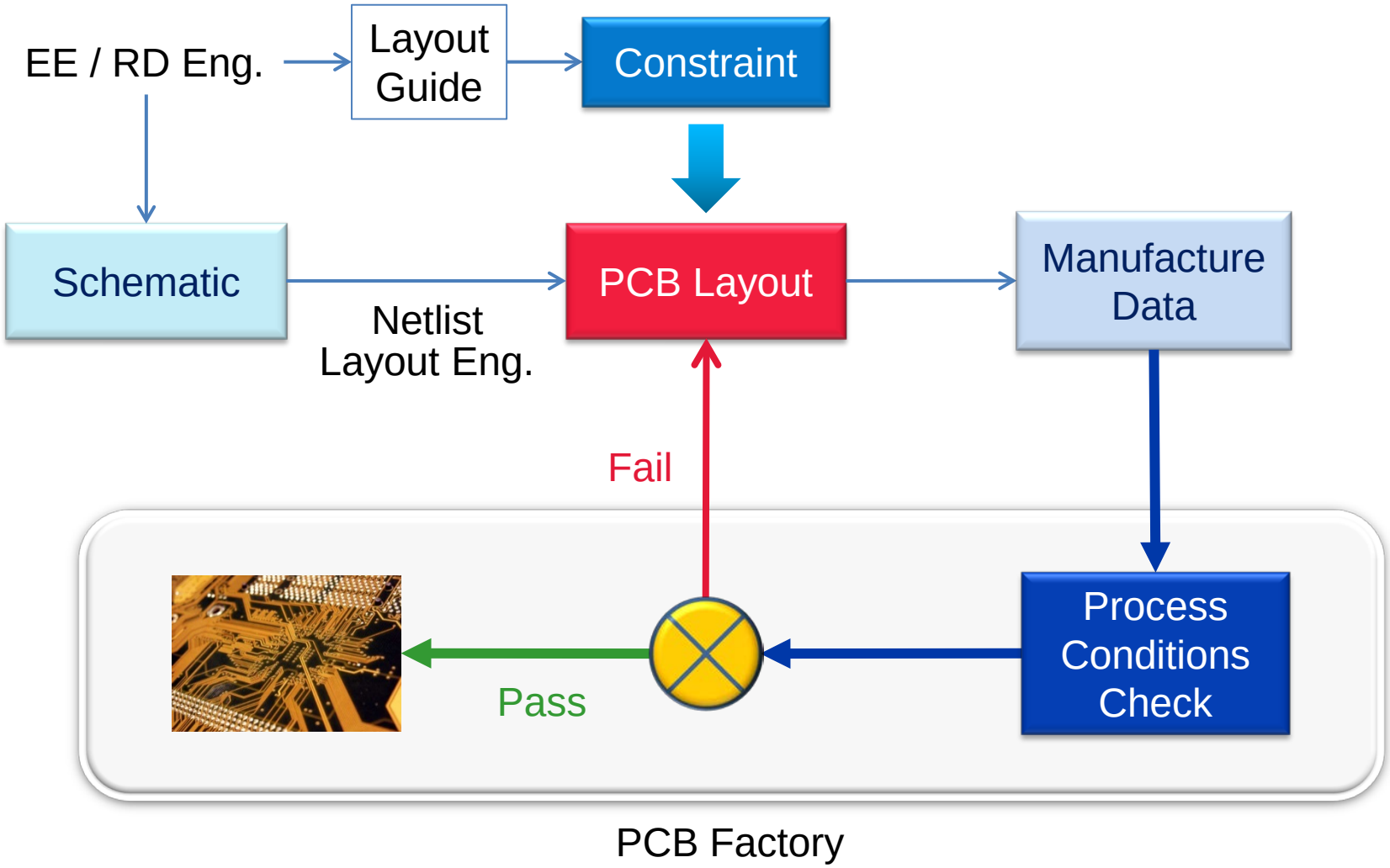
- Allegro PCB Rules Developer / Checker Option

PCB Design & Production Flow

- Documents requirement for production

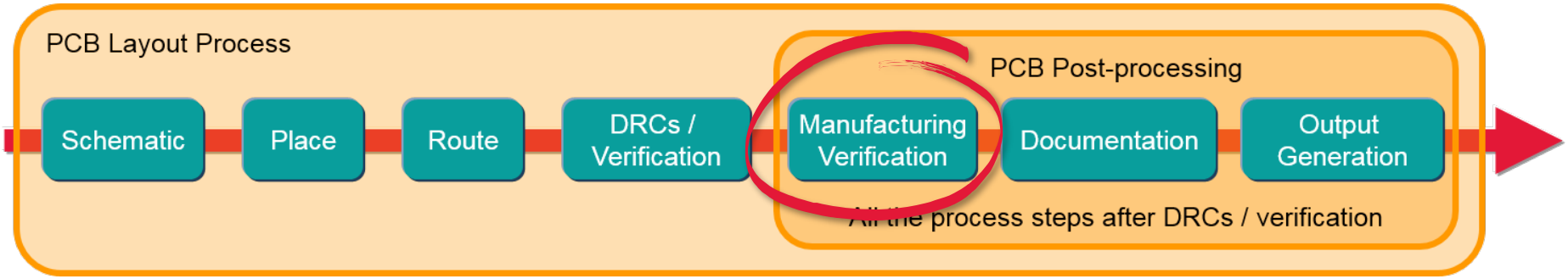


PCB Design Rule Check Workflow



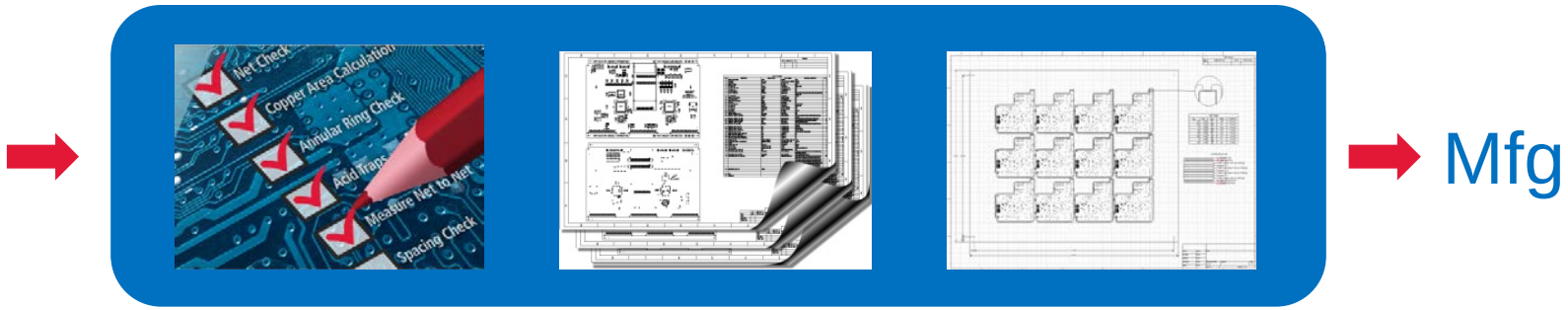
Why to Check Manufacturing Issues?

- Increasing design complexity requires more specialized checking vs. traditional CAD tool DRCs
- Designs that pass standard DRCs may still contain issues that result in low manufacturing yields, or costly scrap
- Correcting fabrication issues can help to reduce the amount of design modification done by the fabricator
- If the fabricator is modifying your design, you have lost database integrity



Allegro PCB Manufacturing Option

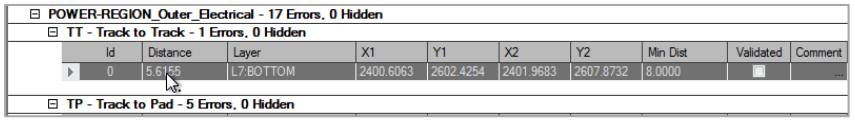
- DFM Checker
  - Easy and fast check manufacture data on Allegro PCB designer environment.
  - Cross probing the point of failure to Allegro PCB designer.
- Documentation Editor
  - Easy and fast generate PCB manufacture documents.
- Panel Editor
  - Easy to make panelization, generate documents and components coordinate for Pick & Place

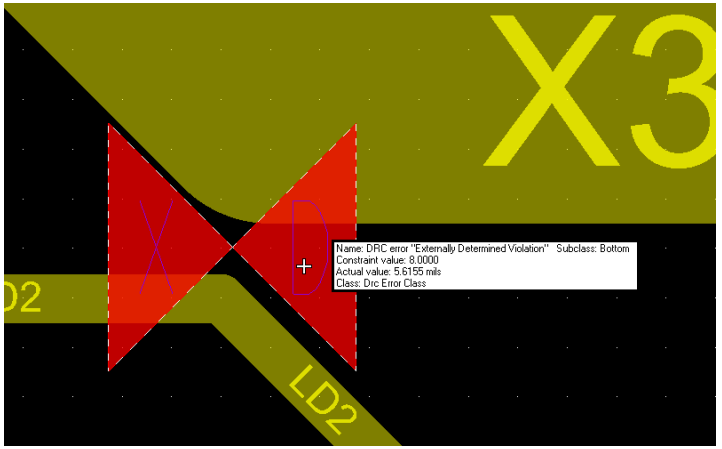


Allegro DFM Checker

What's DFM Checker

- Fabrication Data check
  - IPC-2581
  - Multiple rules check options
    - Rules by group (Streams)





- Imports physical check values
  - Constraint regions
  - Default physical check values
  - Create and store rule set templates
- Check runs in "Background"
  - Allegro editor and document editor can be used while checks are running
- Results review
  - Violations listed by check category
  - Cross probe of violation between violations list and Allegro PCB Editor
- Catches Violations before releasing to Manufacturing

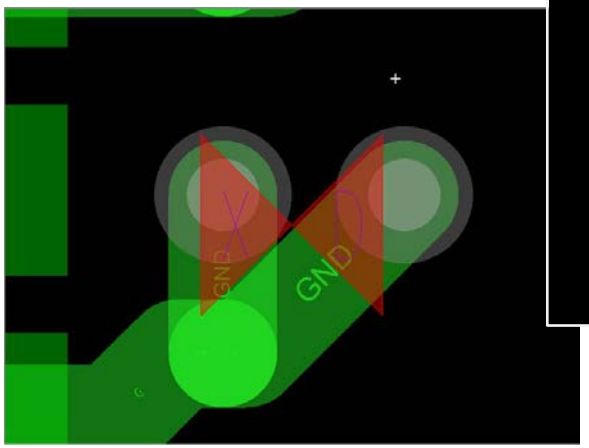
Design For Manufacture (DFM)

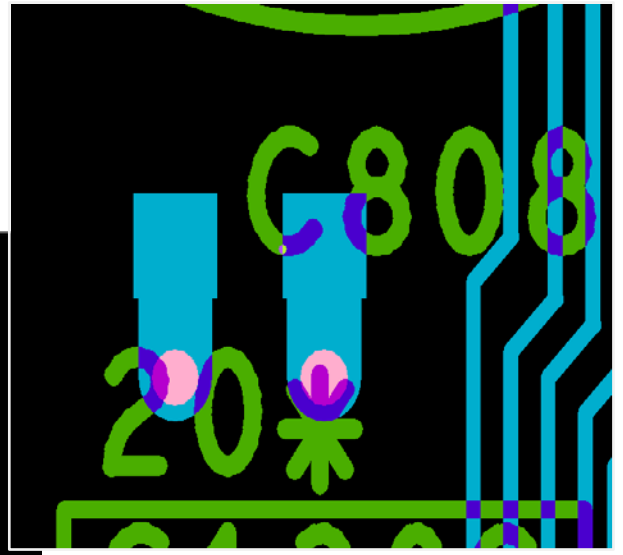
DFM check categories

- Copper checks
  - Trace to trace, trace to pad, pad to pad, shape to pad, ….
  - Redundant pads, superimposed pads
  - Pads without drills
  - Antennas
  - Slivers
  - Acid traps
- Via checks
  - Through hole, laser drill
  - Plated, unplated
  - Backdrills to trace
- Plane checks
  - Positive, Negative
- Solder mask checks
- Paste mask checks
- NC Drill checks
  - Overlapping, coincidental, redundant
  - Drill to drill
  - Imploded Mill path, arcs
- Silkscreen checks
  - To soldermask, board outline
  - Min silkscreen width
- Netlist Compare
- Design Analysis

SECOND SET OF EYES

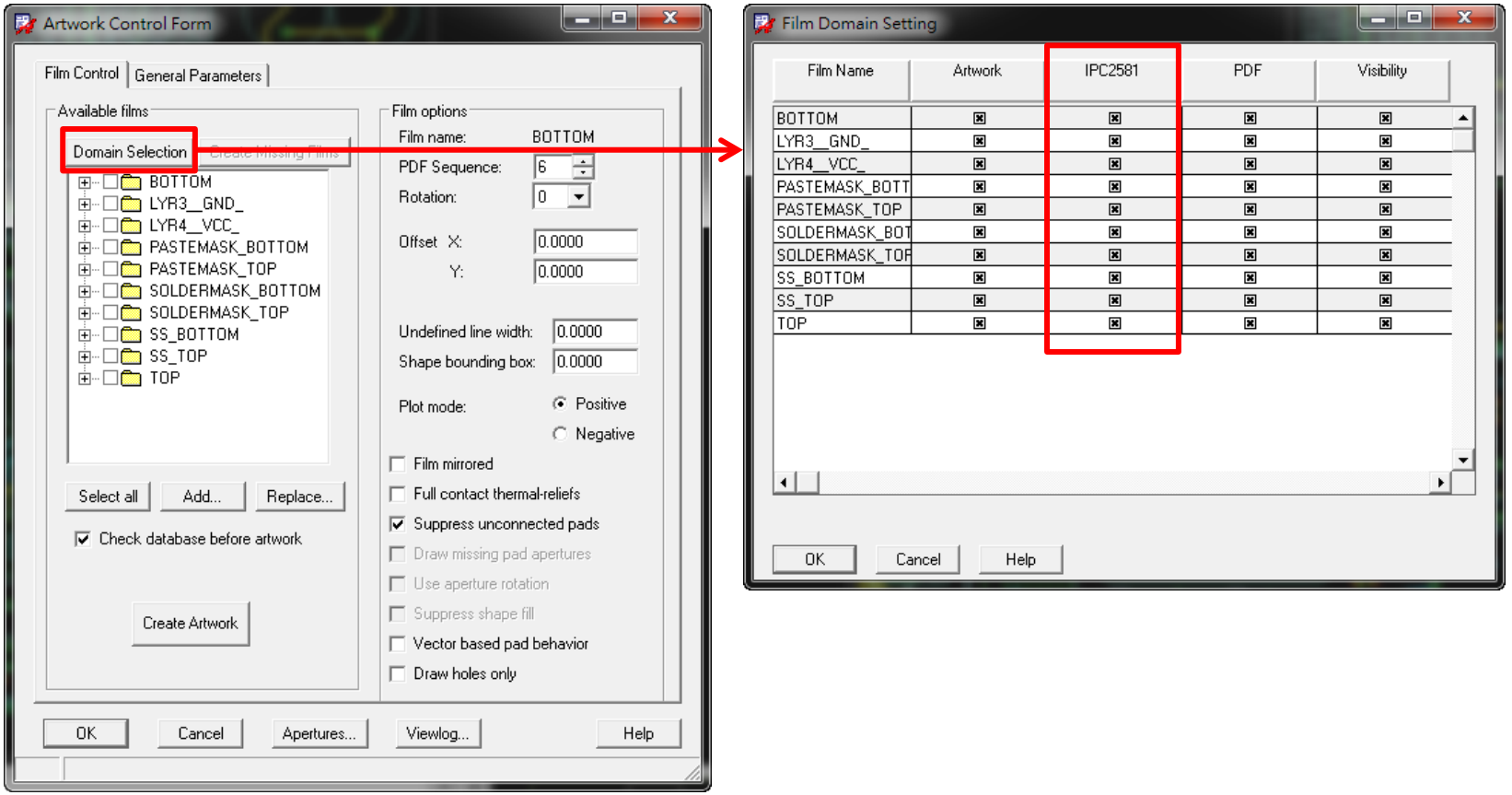
- Quality
- Cost
- Right first time
- Efficiency



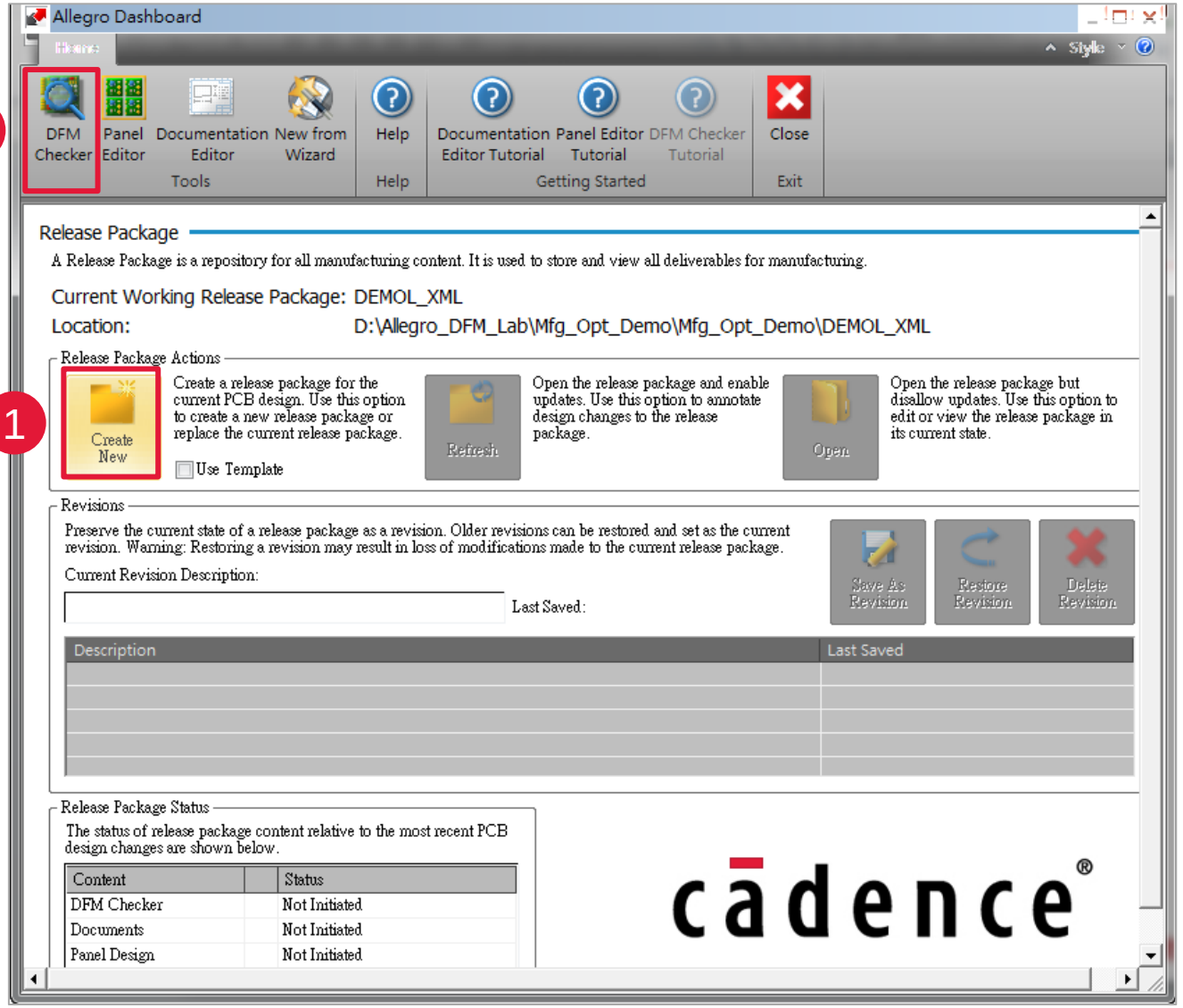


Data Preparation

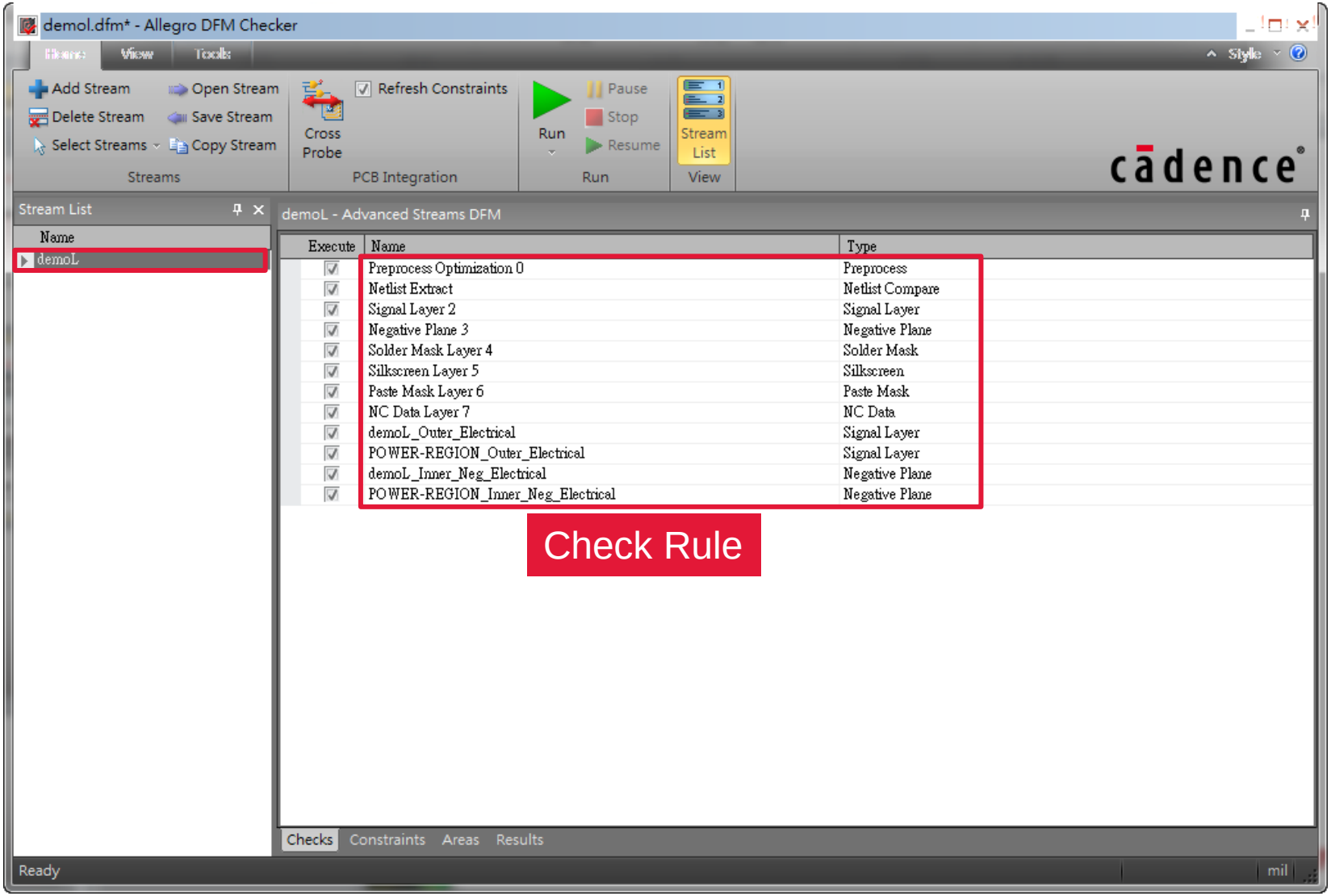
- All artwork film records must be defined
- IPC-2581 Layer mapping must be defined



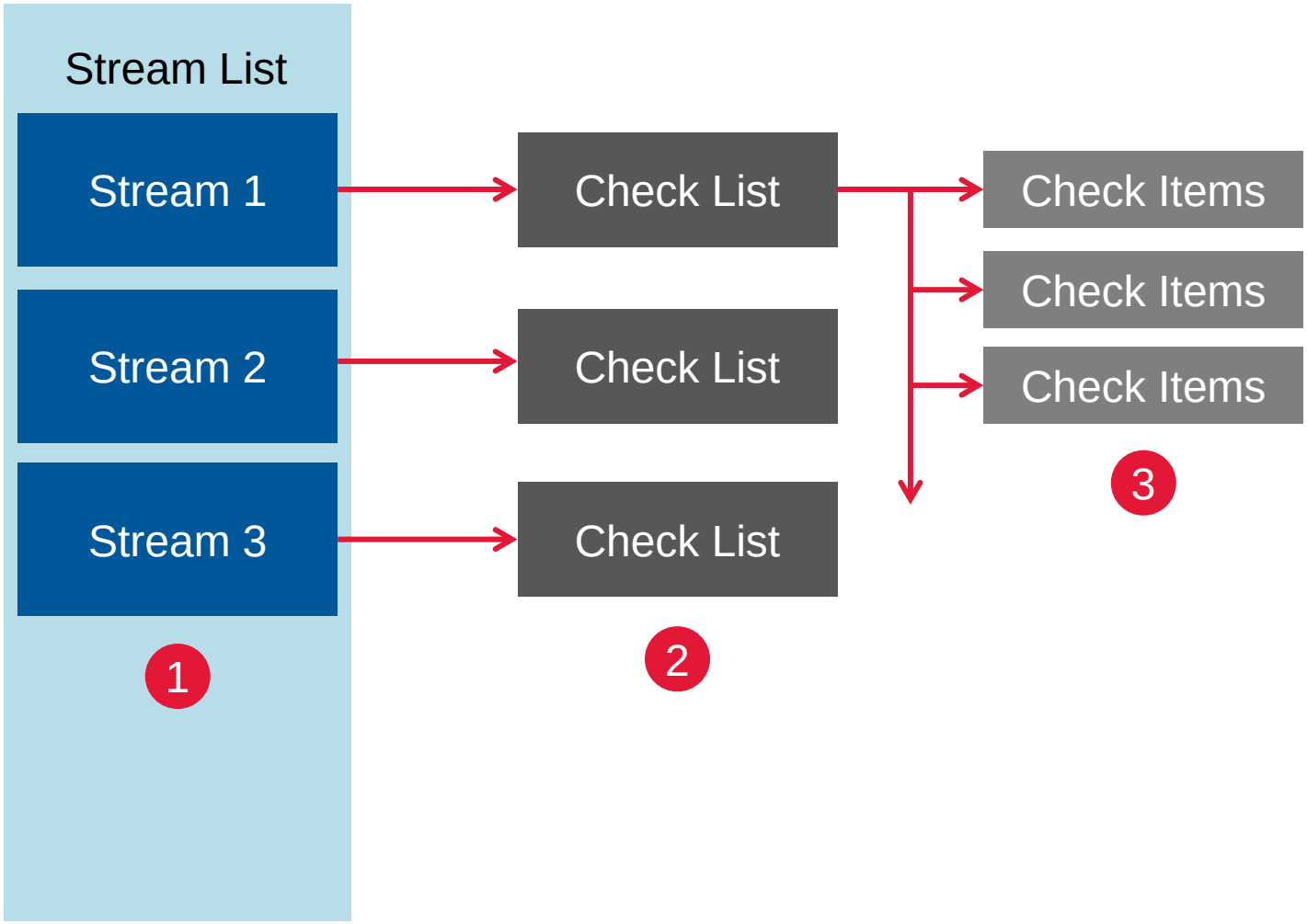
Create DFM Project



Build Stream & Check Rule

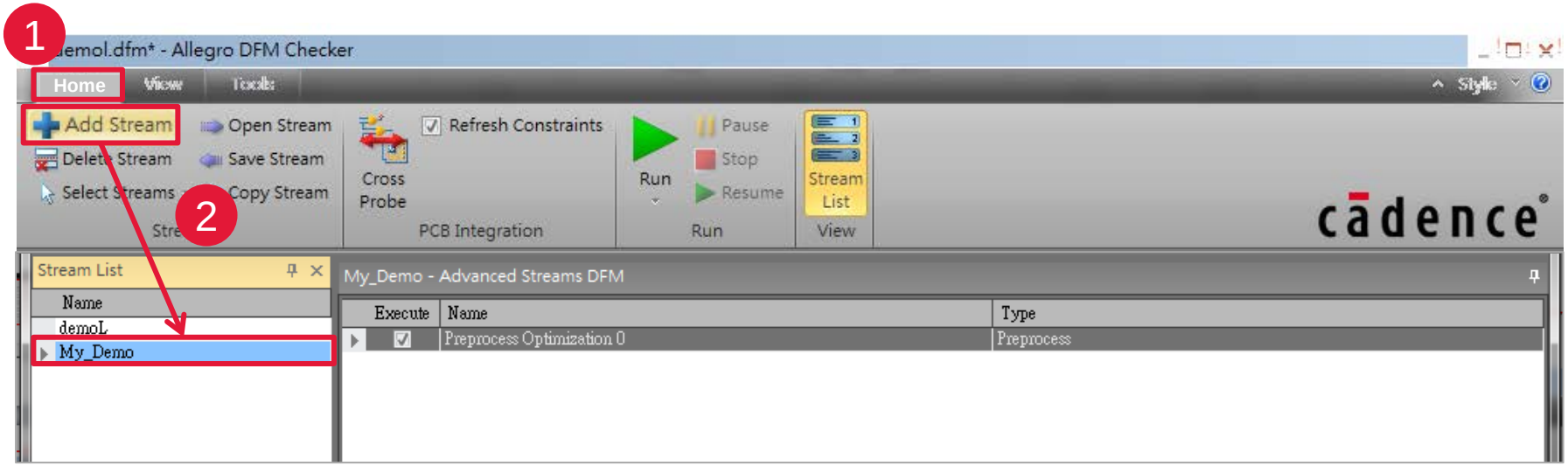


Stream Setting Flow



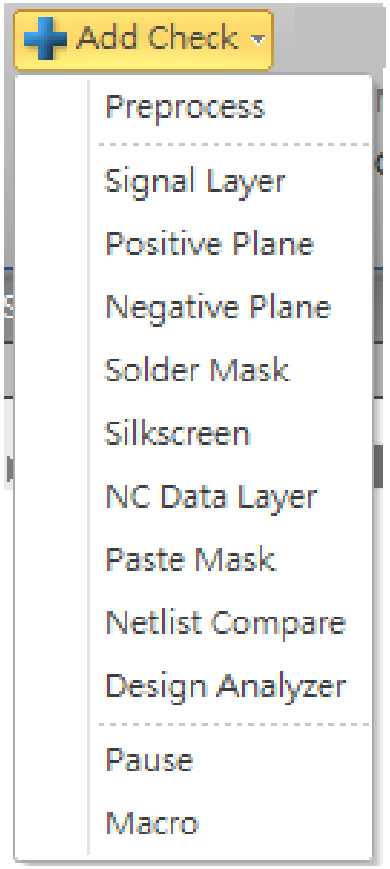
Create Stream

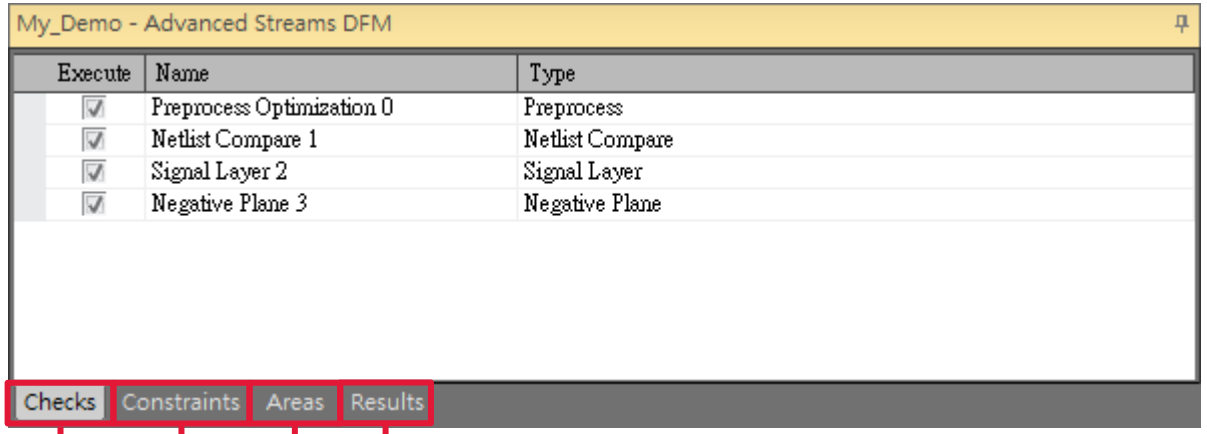
- Create Stream



- Add Checking Rule

Add Check Rule





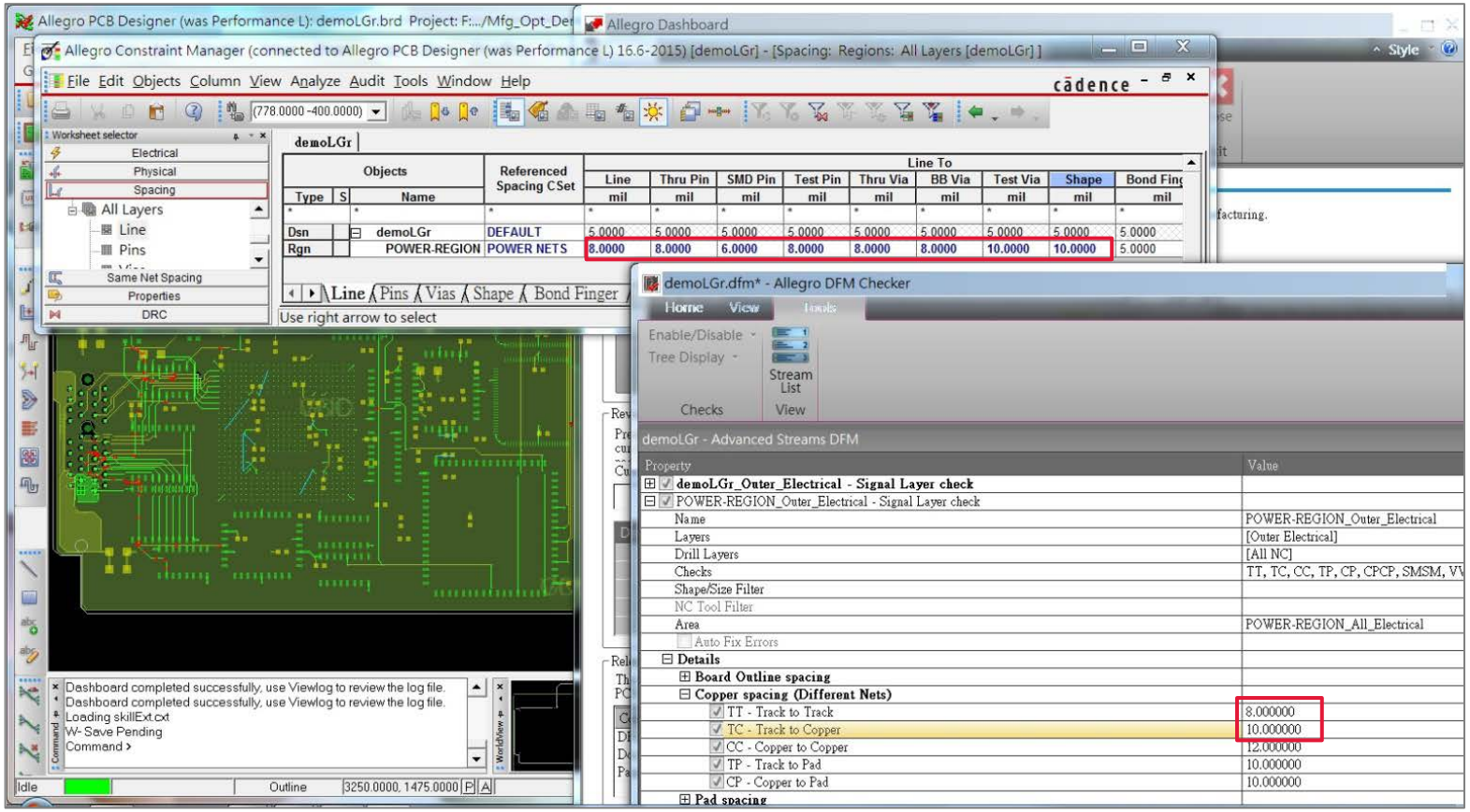
Review check result

Check area and layers definition

Detailed check rule setting

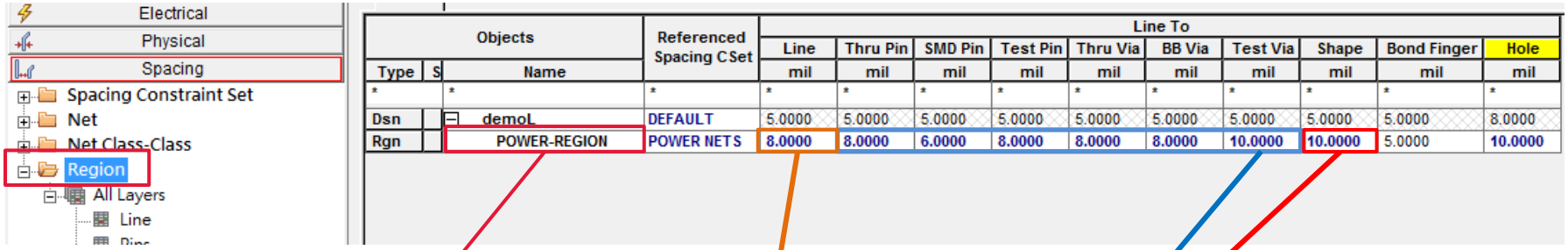
Check rule list

Check Rule Sample



1. 若爲單獨對應條件， 則 constraint 設定值及接引用，如 Line to Line。
2. 若有多對應條件，則會引用最大 constraint 設定值，如 Line to Pad。

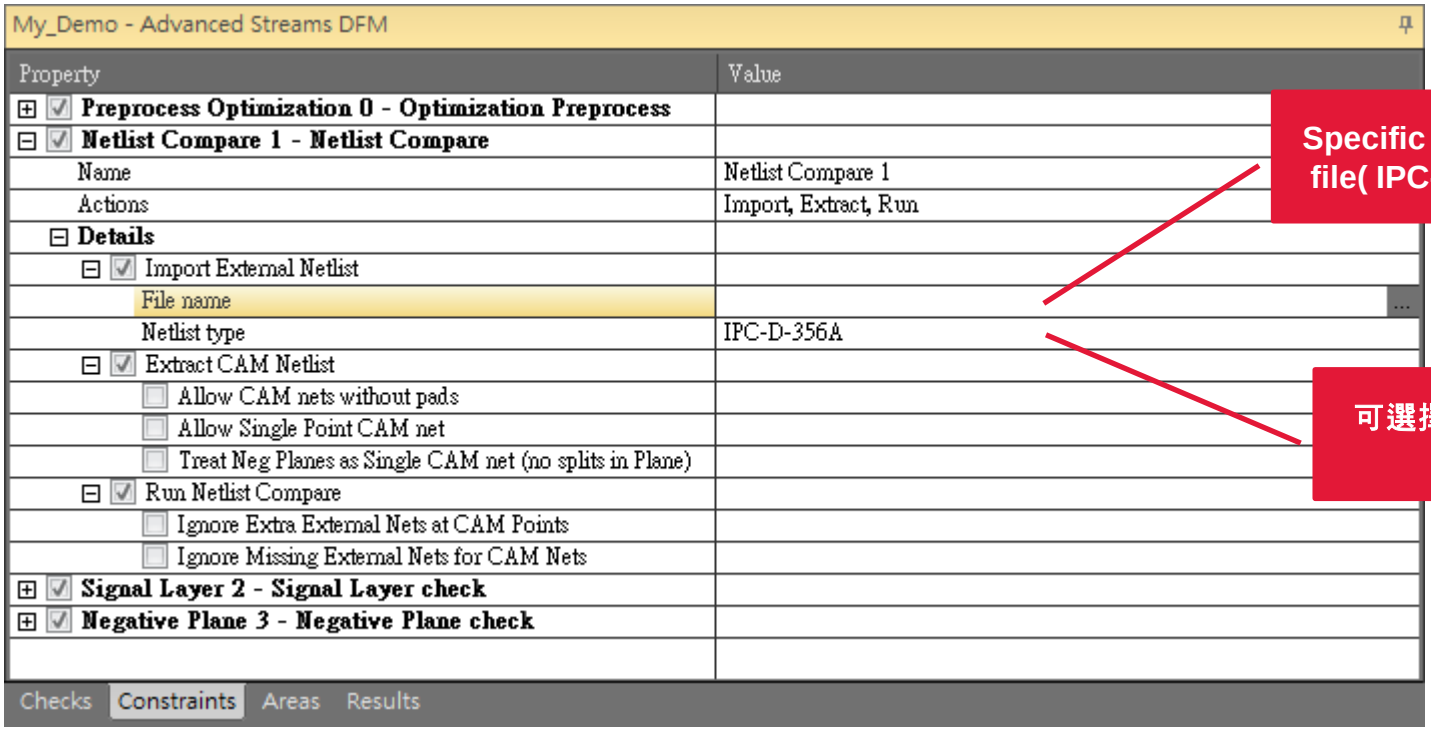
Support Constraint Region



Objects			Referenced Spacing CSet	Line To									
Type	S	Name		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bond Finger	Hole
				mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*		*	*	*	*	*	*	*	*	*	*	*	*
Dsn		demoL	DEFAULT	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	8.0000
Rgn		POWER-REGION	POWER NETS	8.0000	8.0000	6.0000	8.0000	8.0000	8.0000	10.0000	10.0000	5.0000	10.0000

POWER-REGION_Outer_Electrical - Signal Layer check	
Name	POWER-REGION_Outer_Electrical
Layers	[Outer Electrical]
Drill Layers	[All NC]
Checks	TT, TC, CC, TP, CP, CPCP, SMSM, VV, LVLV, THTH, SMV, SMLV, SMTH, VTH, LVTH, DTHC, DT...
Shape/Size Filter	
NC Tool Filter	
Area	POWER-REGION_All_Electrical
Auto Fix Errors	
Details	
Board Outline spacing	
Copper spacing (Different Nets)	
TT - Track to Track	8.000000
TC - Track to Copper	10.000000
CC - Copper to Copper	12.000000
TP - Track to Pad	10.000000
CP - Copper to Pad	10.000000
Pad spacing	
Drill spacing	
Annular Ring	

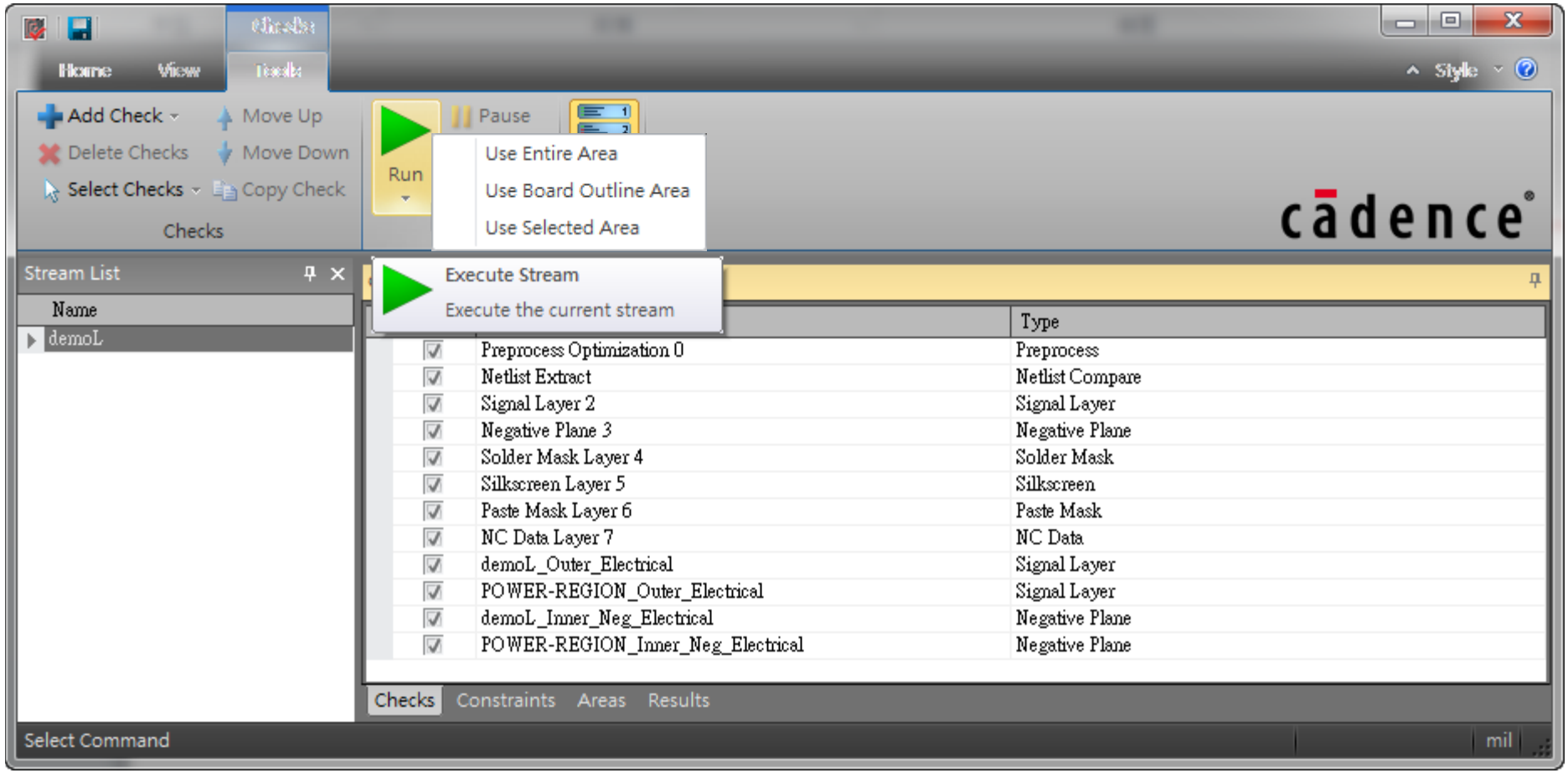
Netlist Compare



Specific external Netlist file(IPC-D-356 format)

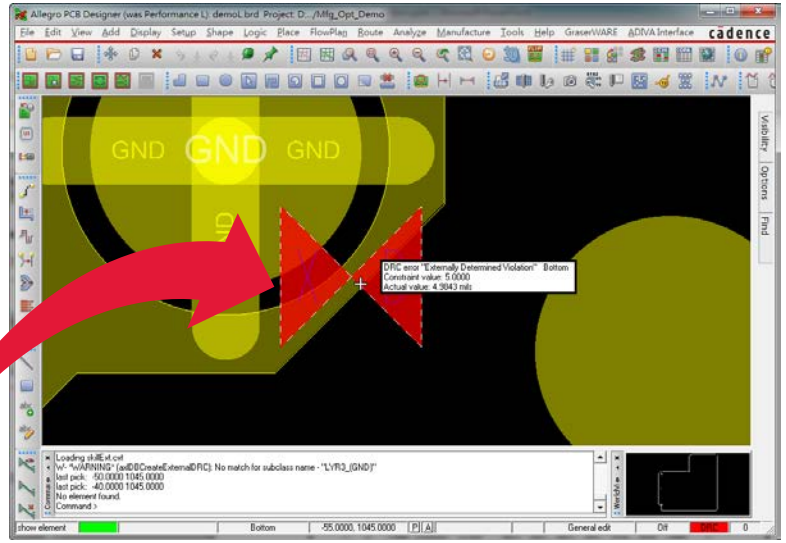
可選擇IPC-D-356或 IPC-D-356A

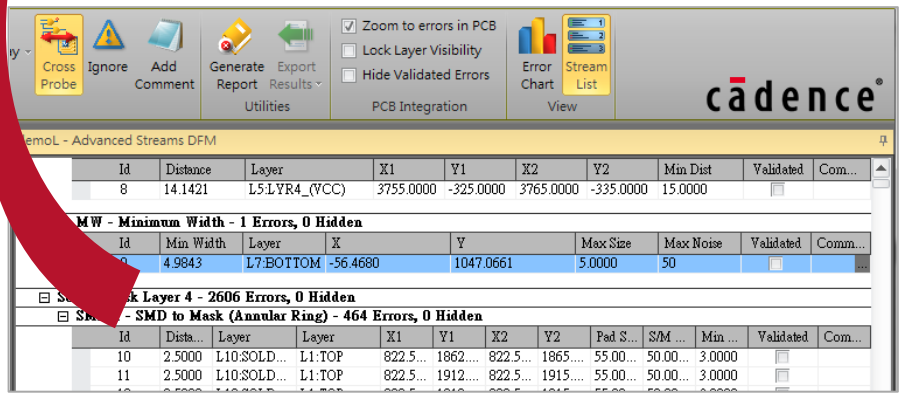
Select Area when run



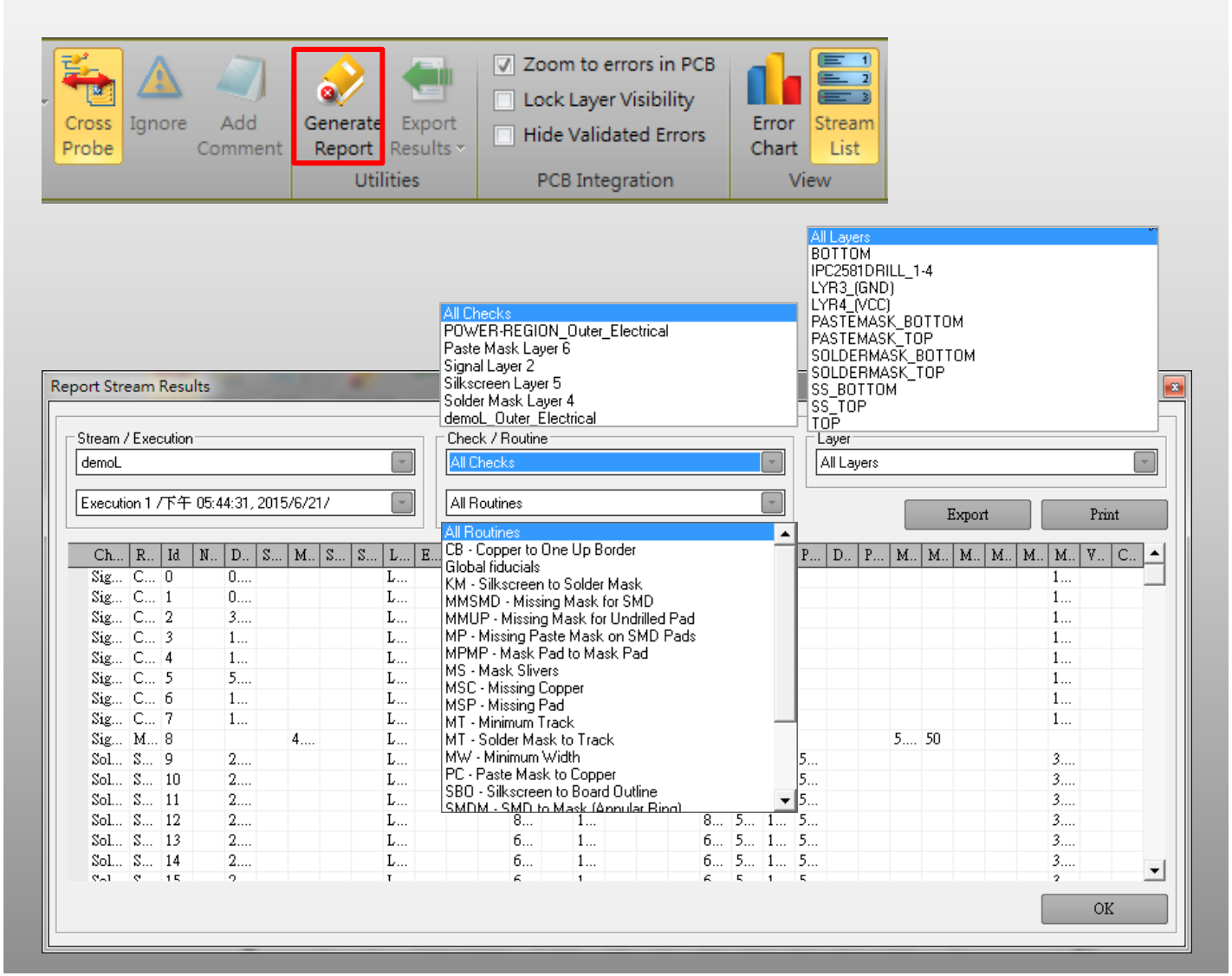
Category Results & Cross Probing

- Constraints and constraint regions are extracted by DFM Checker
- Automatically creates a default verification “stream”
  - From the layer structure, constraints and constraint regions
- DRC markers are added into PCB Editor
  - Selection in the error lists in DFM Checker will zoom to the error location in PCB Editor
  - Details shown through tooltip in PCB Editor

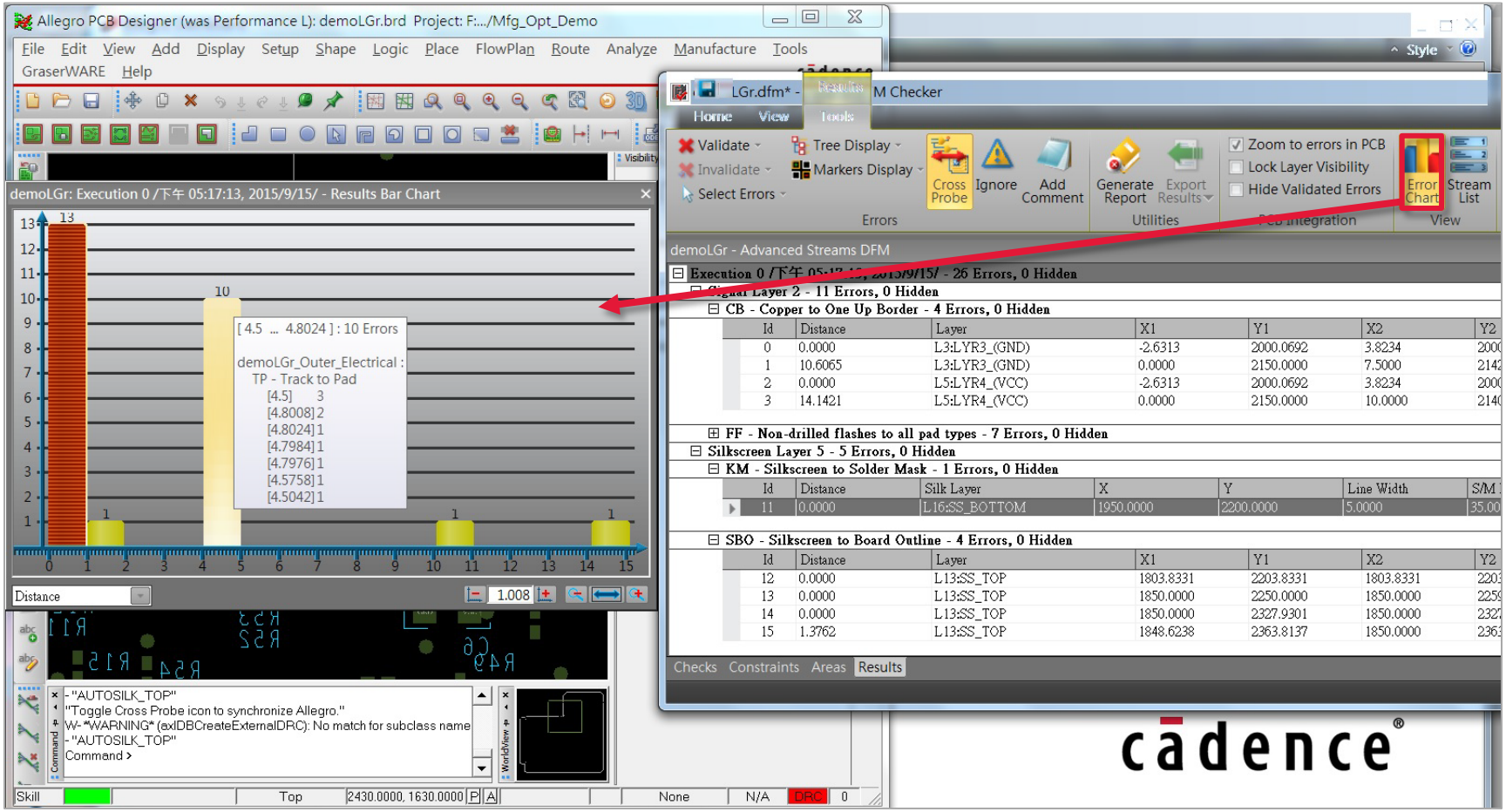




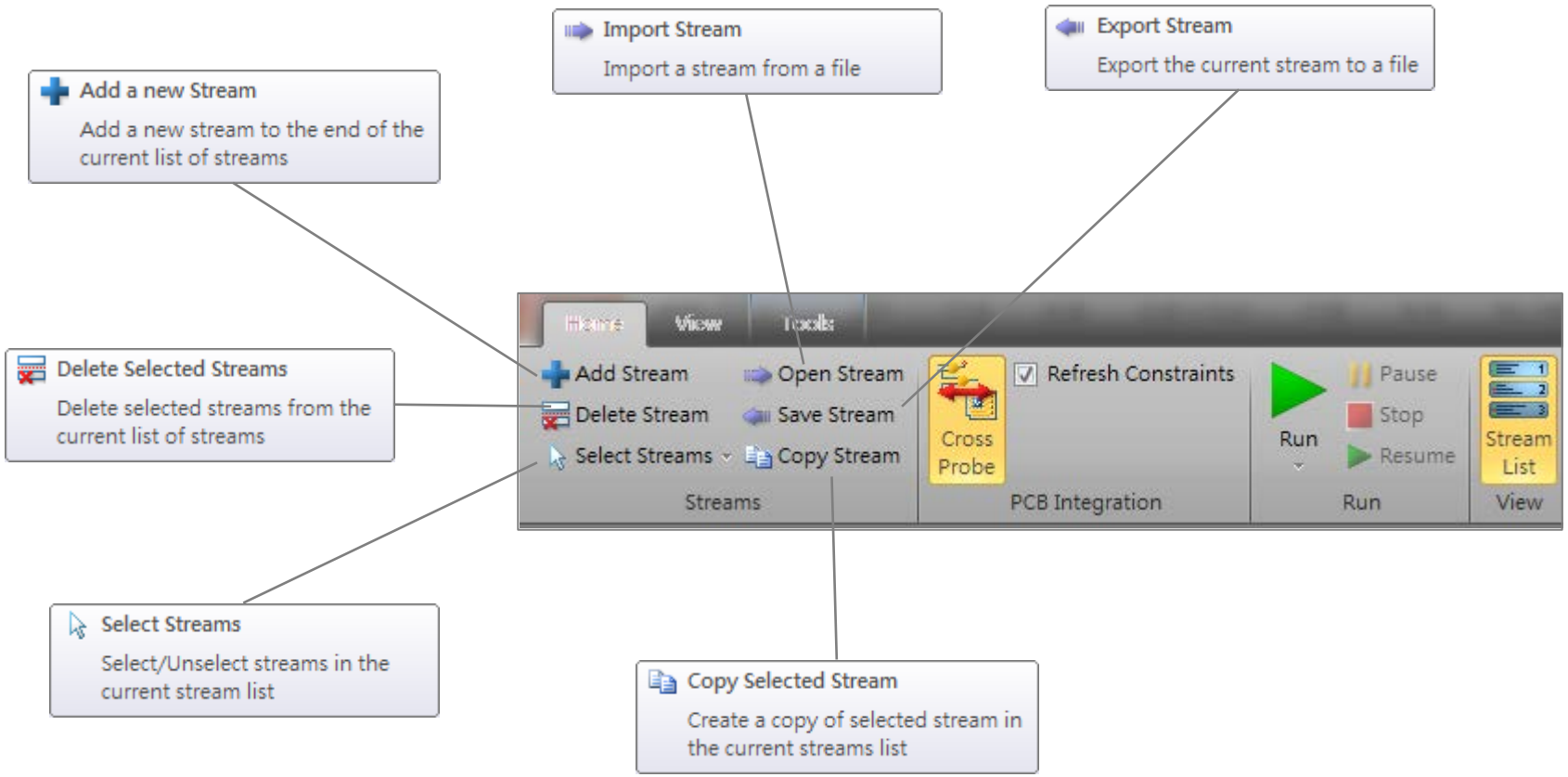
Generate Report



Error Chart



Stream Rule Reuse



Summary of DFM Checker

- Check manufacture data (IPC-2581) with design rules
- Auto generate IPC-2581 to go through DFM check flow
- Direct copy constraint setting value into DFM check rule
- Support constraint region design check
- Netlist Compare for consistency check
- Select Area when run
- Category Results & Cross Probing
- Error Chart for Quality Analysis
- Reuse of Stream

Allegro PCB Rules Developer / Checker Option

Allegro PCB Rules Developer & Checker

Many companies want the ability to extend the rules that Cadence® Allegro® products provide

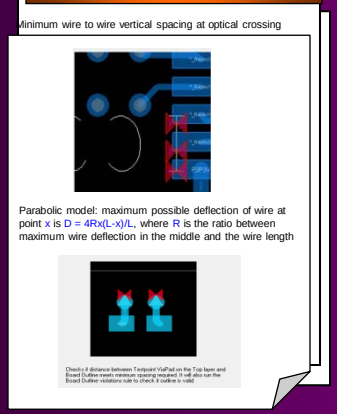
- Customized to their fabrication/assembly needs
- Adopt new emerging fabrication, assembly, test processes before they are supported by the tools

- Allegro Rules Developer
  - Enables customers to create new rules using a relational algebra expression language
    - A programming language that simplifies the creation of rules for DRC checks of all design data types in Allegro platform
    - A platform independent and version agnostic with Allegro platform
  - Allows sharing of custom rules with other user sites, vendors and customers
  - Provides a starter set of rules to help users get started quickly
- Allegro Rules Checker
  - Enables customization of rules for a set of designs
  - Integrated with Allegro PCB Editor
    - Load rules into Allegro Constraint Manager
  - Run the checks
  - Adds DRC violation markers in Allegro PCB Editor

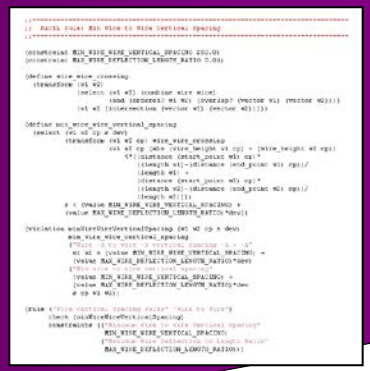
RAVEL DRC System for PCB and SiP

DEVELOPER

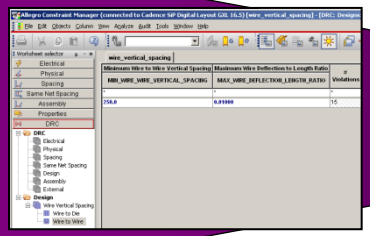
DRC Description in **Design Rule Manual**



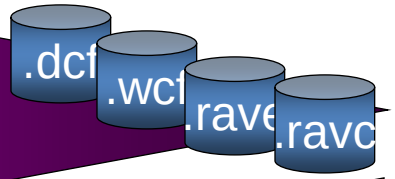
DRC Source Code in **RAVEL Language**



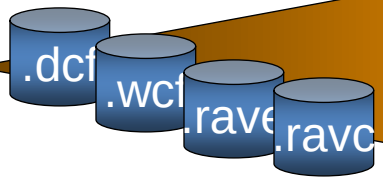
DRC Compilation, Encryption and Integration in **Constraint Manager**

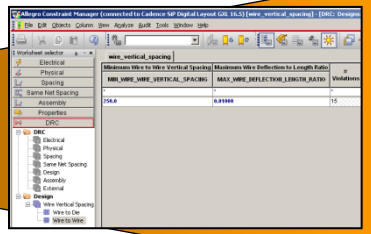


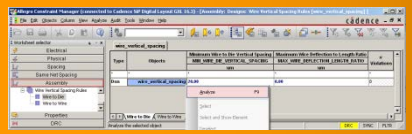
DRC Export to **Constraint Manager Files** and **Batch DRC Files**

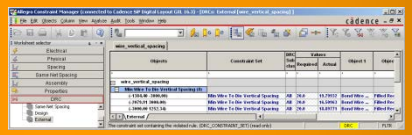


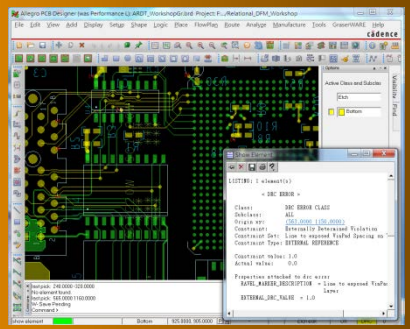
Checker











DRC Import from **Constraint Manager Files or Batch DRC Files**

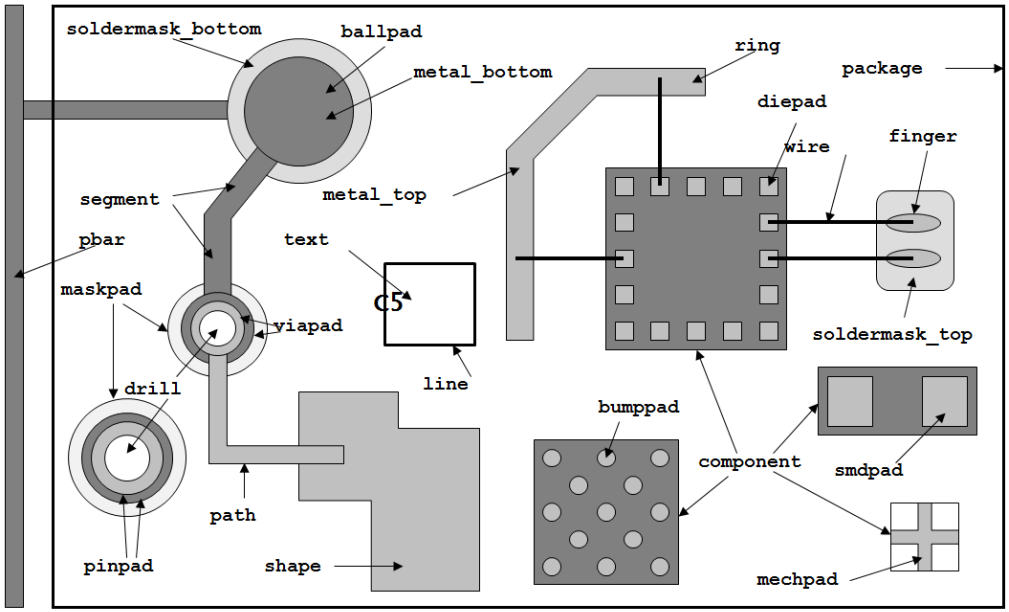
DRC Selection and Constraint Modification in **Constraint Manager** or **Batch Control File**

DRC Execution in **Constraint Manager** or in **Batch**

DRC Cross-Probing in **Allegro PCB** or **SiP Layout**

What is Ravel?

- Relational Algebra Verification Expression Language
- Ravel objects closely correspond to SiP / PCB objects
- Forms relations between objects and queries relational data through combination and filtering
- Can derive new objects through geometric and polygon operations



What is Ravel?

- Fully integrated with SPB tools - directly runs on Allegro SiP / PCB design file
  - Manufacturing data export is not required
- Integrates seamlessly with Constraint Manager
- Geometrical operations are much faster
- Allows sharing of encrypted rules with customers
- Performs checks between different design data types
  - Silkscreen text-Soldermask
- Fewer lines of code to write the rules
- Easy to learn

Example –

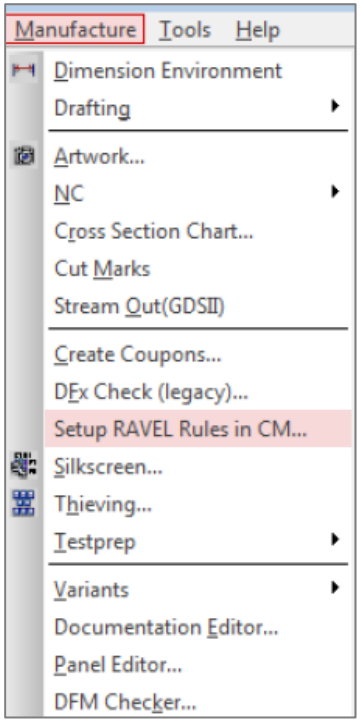
On a 24-layer board, the “trace to board edge spacing” rule checks the distance between 17700+ clines (4400+ nets) and board outline for a constraint value of 100, and reports 2 errors in ……. 10 seconds

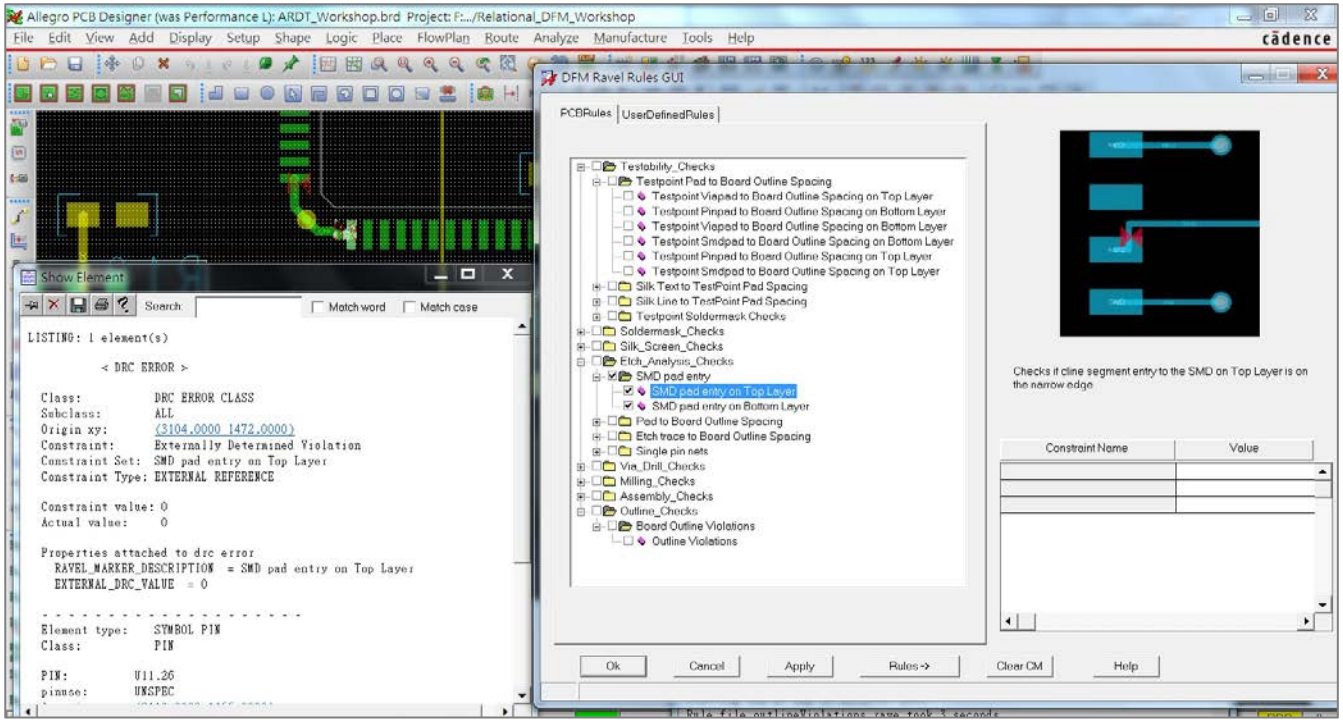
Starter Rules

- Silkscreen rules
  - Min Spacing Silkscreen Line to pad
  - Min Spacing Silkscreen Text to pad
  - Min Spacing Silkscreen Line to exposed pad
  - Min Spacing Silkscreen Text to exposed pad
  - Min Height of Silkscreen
  - Min Length Silkscreen line
- Etch Analysis Checks
  - Min Spacing between Pin pad to board outline
  - Min Spacing between SMD pad to board outline
  - Min Spacing between Etch Trace to board outline
  - Single pin nets check
  - Trace entry into SMD pad
- Testability Checks
  - Min Spacing between Silkscreen text to testpoint pads
  - Min Spacing between Silkscreen line to testpoint pads
  - Mask clearance check for testpoint pad
  - Min Spacing testpoint pads and board outline
- Soldermask Rules
  - Min Spacing Soldermask to Board outline
- Via Drill Rules
  - Max depth of blind microvia
- Assembly checks
  - Min Spacing between pad and component

Rule Checker

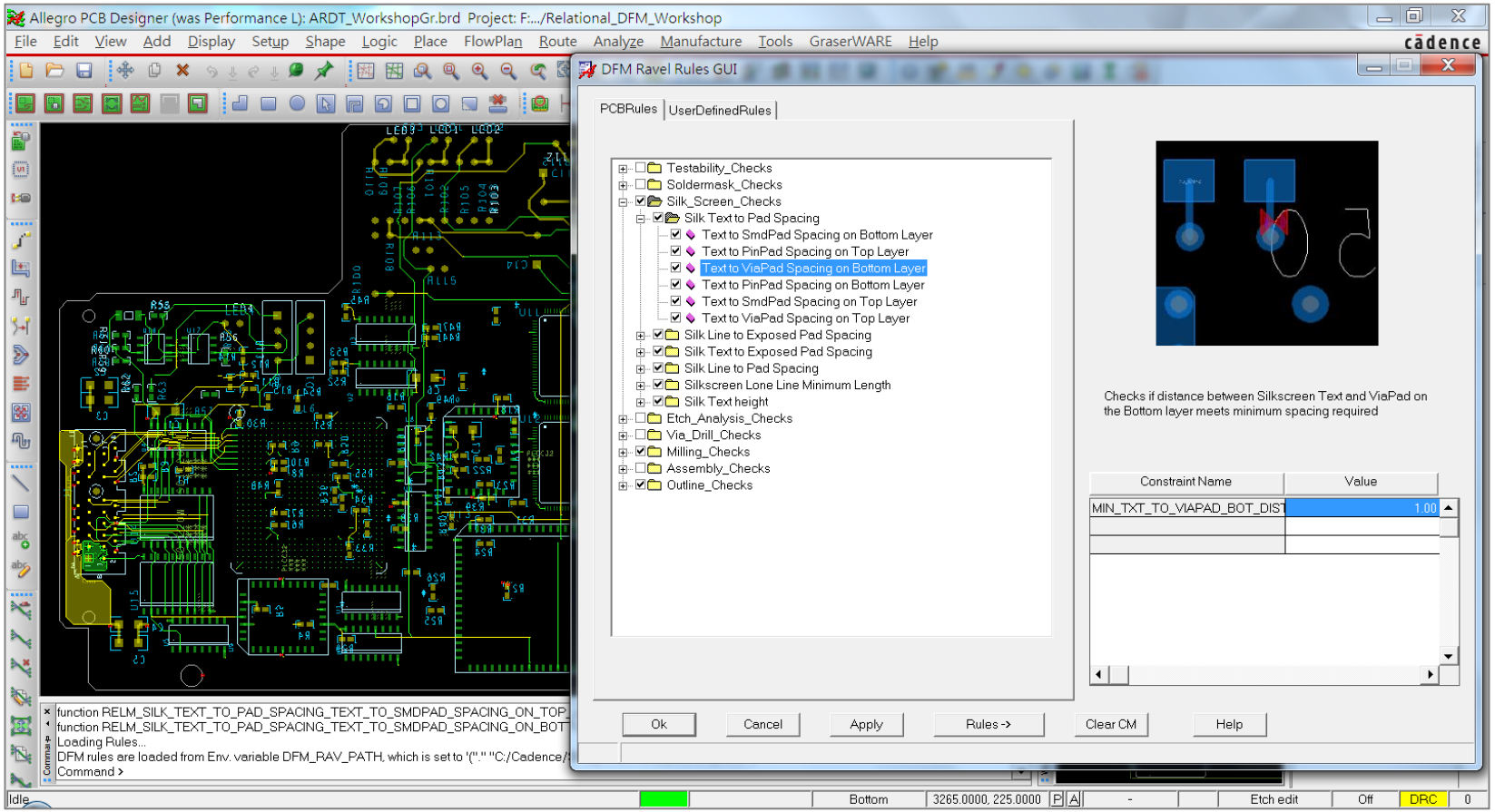
- To start the Allegro Relational Rules Checker Kit, choose ***Manufacture - Setup RAVEL Rules in CM***





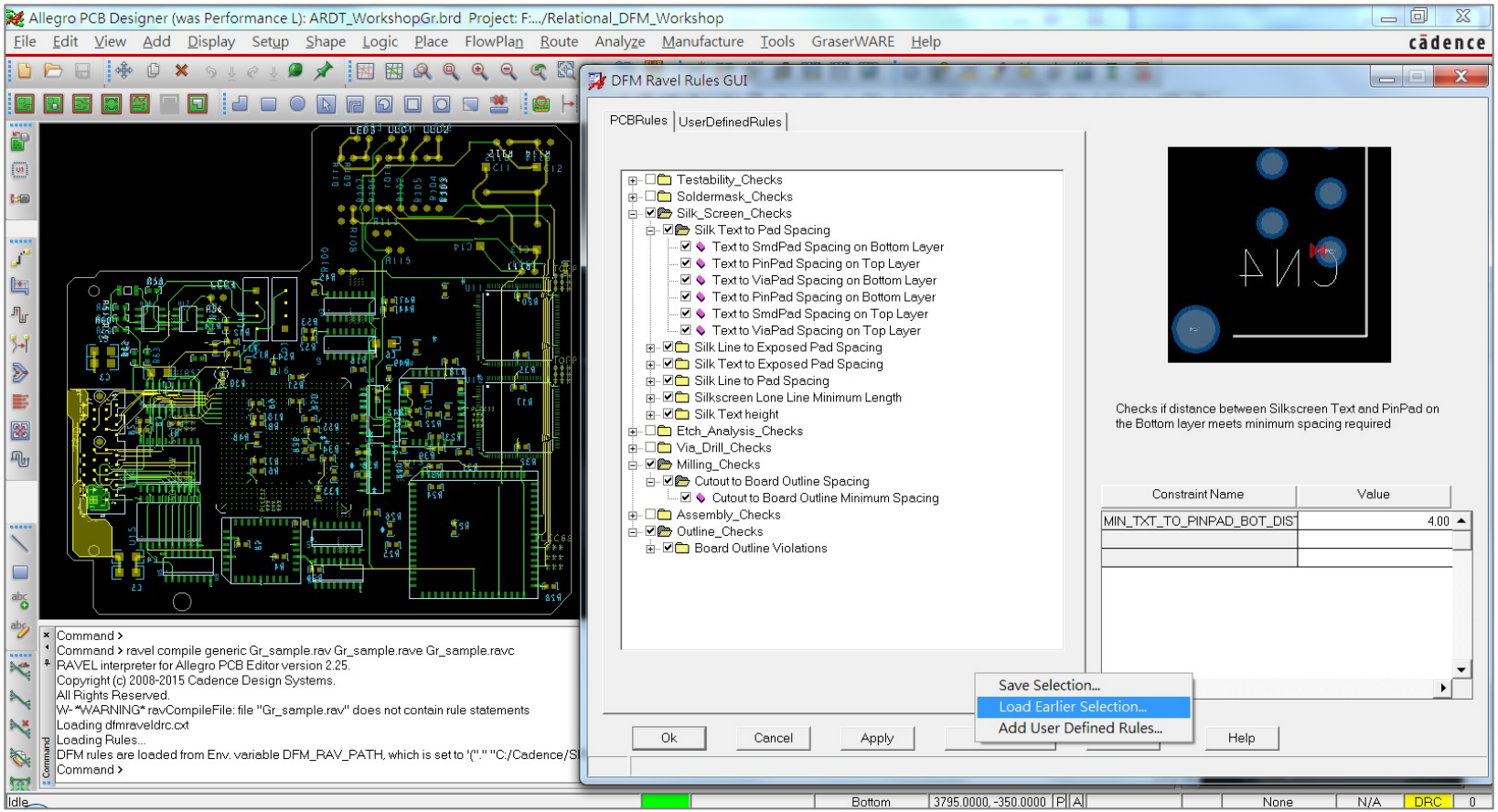
Define Check Values

- Define Ravel check item & value



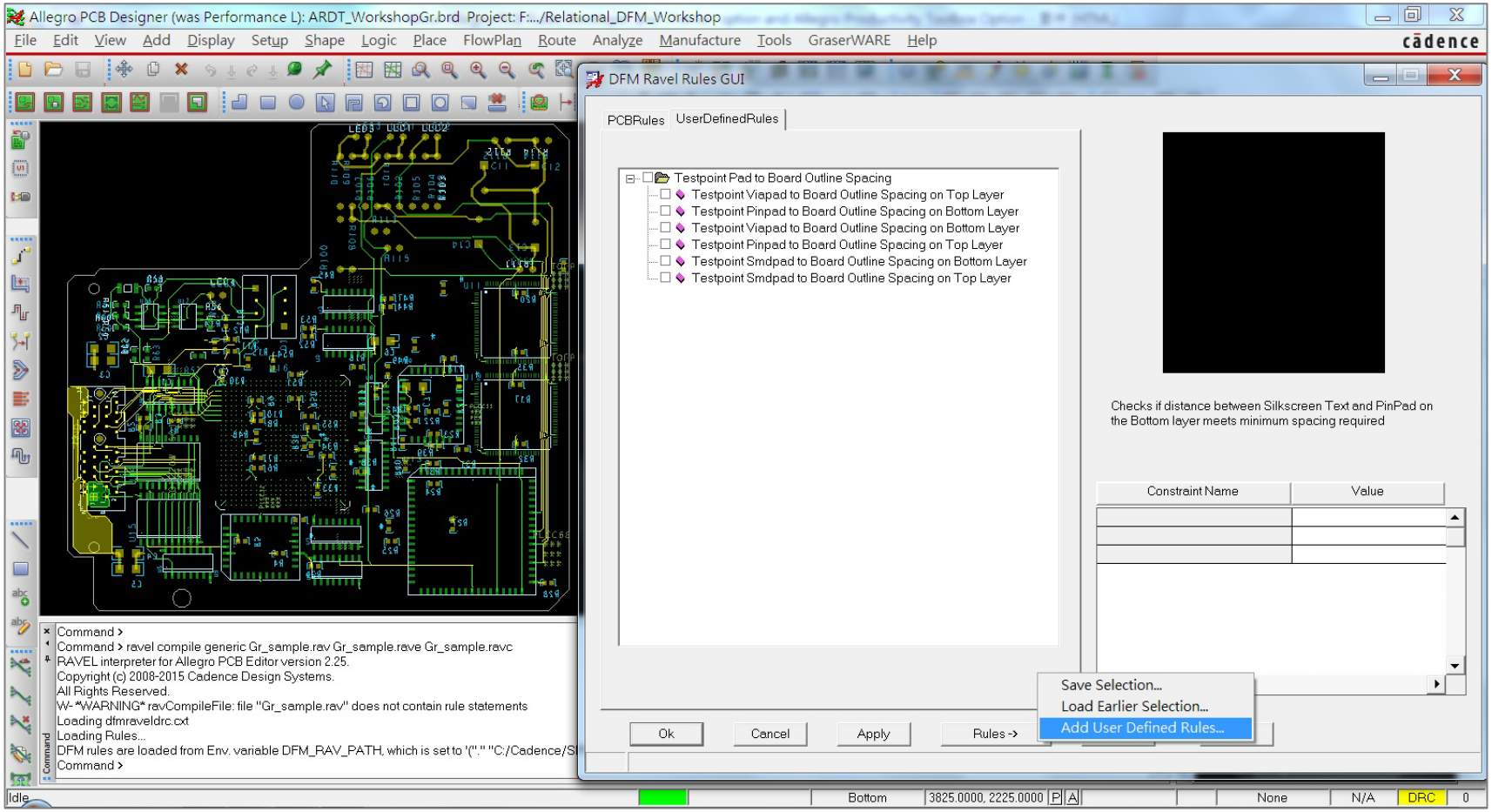
Load Earlier Selection

- Reuse predefined Ravel check items & values



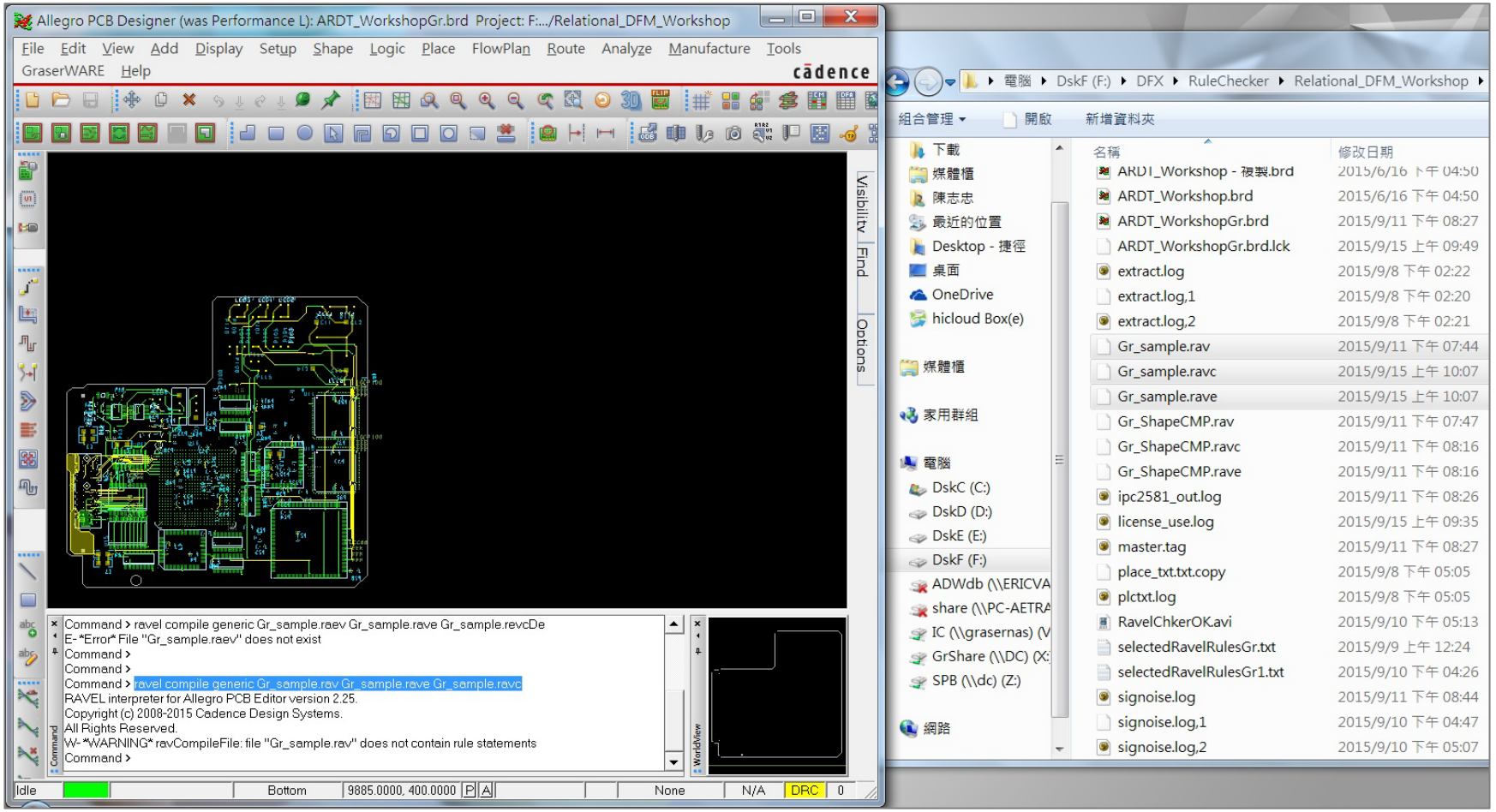
Add User Defined Rules

- Load customized (compiled) ravel rules

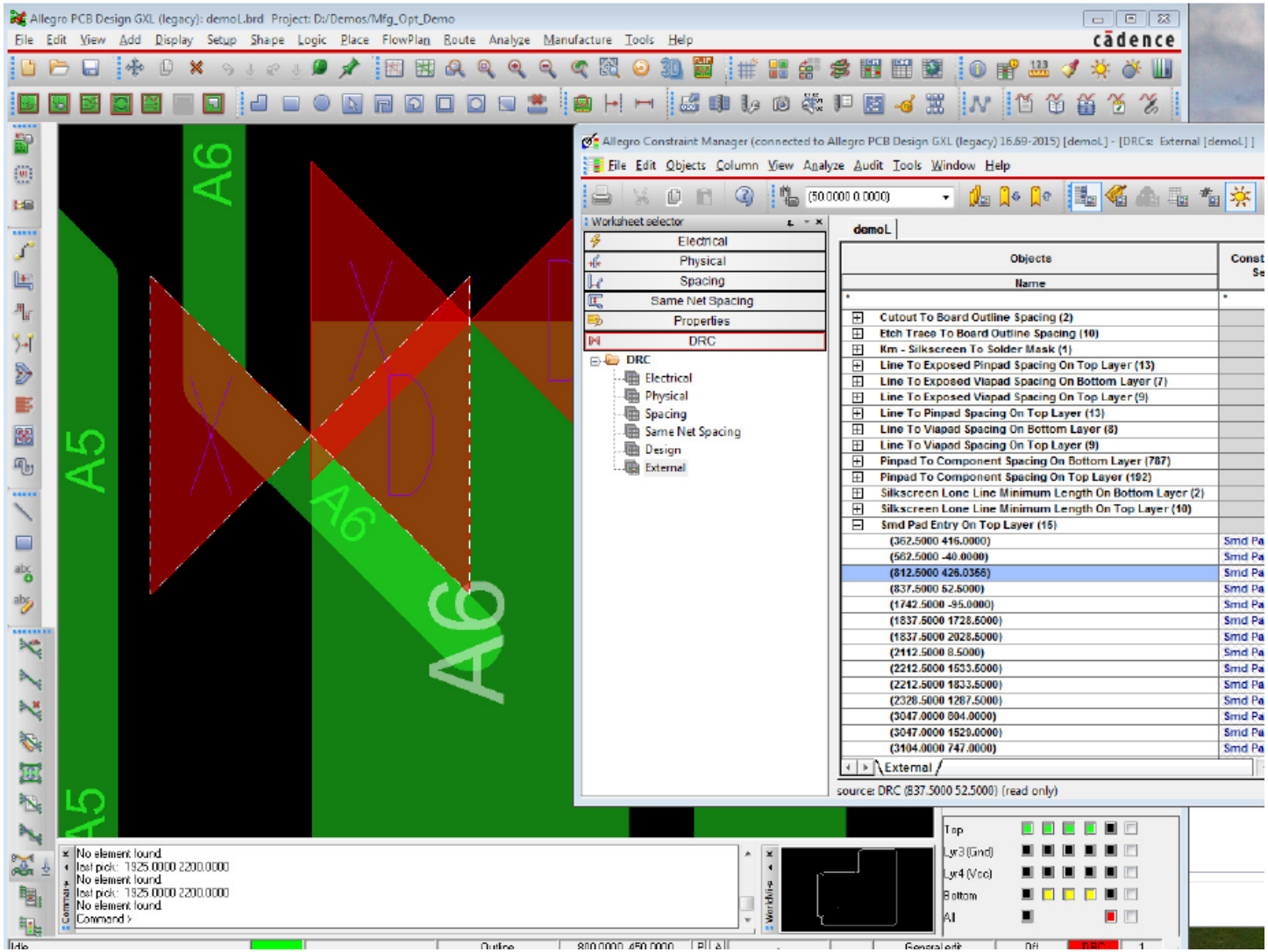


Compile RAVEL

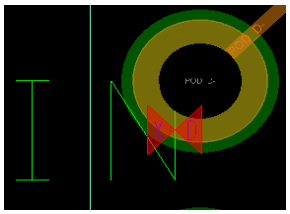
- Compile .rav to .ravc & .rave (by developer)

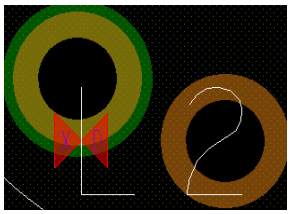


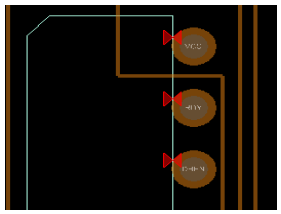
Cross-Highlighted Result in CM

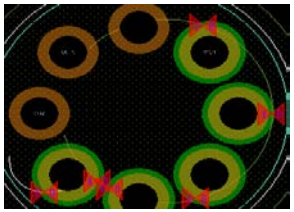


Sample of Starter Rules

1) 

2) 

3) 

4) 

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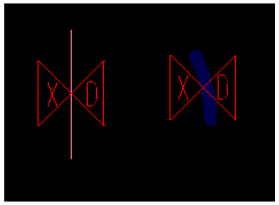
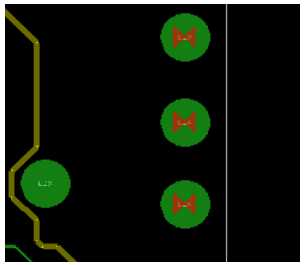
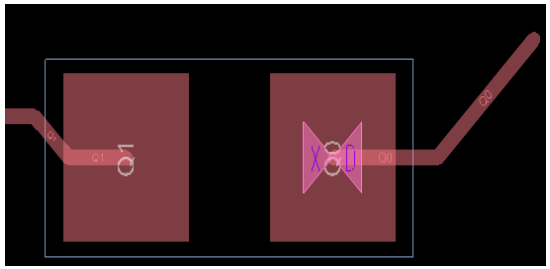
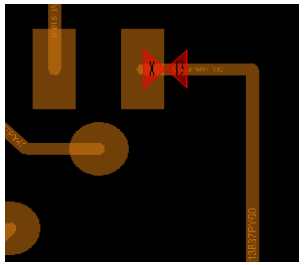
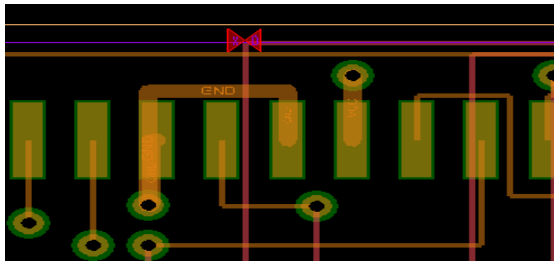
6) 

Silkscreen rules
1) Silk text to pad spacing
2) Silk text to exposed pad spacing
3) Silk line to pad spacing
4) Silk line to exposed pad spacing
5) Silk text height
6) Silkscreen lone line minimum length

1) 

2) 

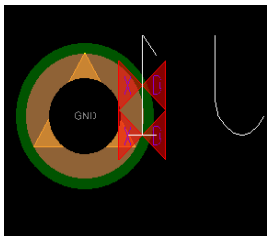
3) 

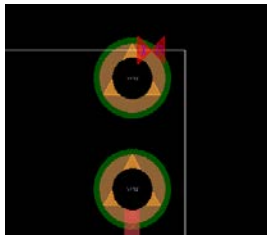
4) 

Etch Analysis Rules
1) Pad to Board Outline Spacing
2) Single pin nets
3) SMD pad entry
4) Etch trace to Board Outline Spacing

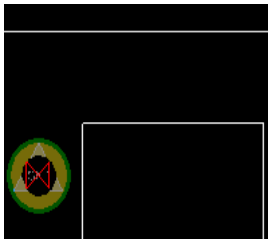
Sample of Starter Rules

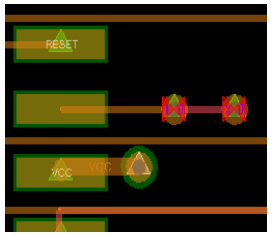
1) 2)



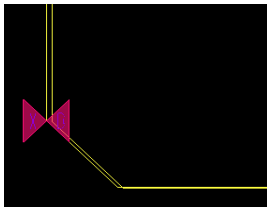


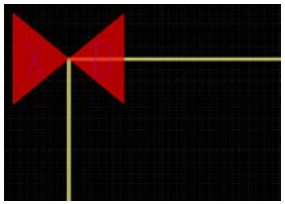
3) 4)





1) 2)





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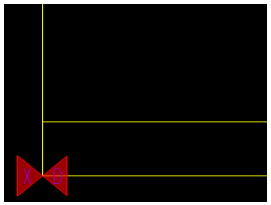

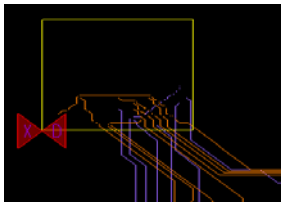

Testability Checks
1) Silk text to testpoint pad spacing
2) Silk line to testpoint pad spacing
3) Testpoint pad to Board Outline spacing
4) Testpoint pad with no soldermask

Outline Checks
1) Duplicate outlines
2) Outline with width > 0
3) Outline made of multiple line segments
4) Shapes on Outline layer with overlapping clines

Summary

- Directly integrated in Allegro
- Starter rules are ready
- User-definable / customizable
- Ravel is Object-oriented , faster than SKILL
- Standard check items & flow

Thanks !!!