

Allegro New Products - DFM / Rule Checkers

Eric / Graser

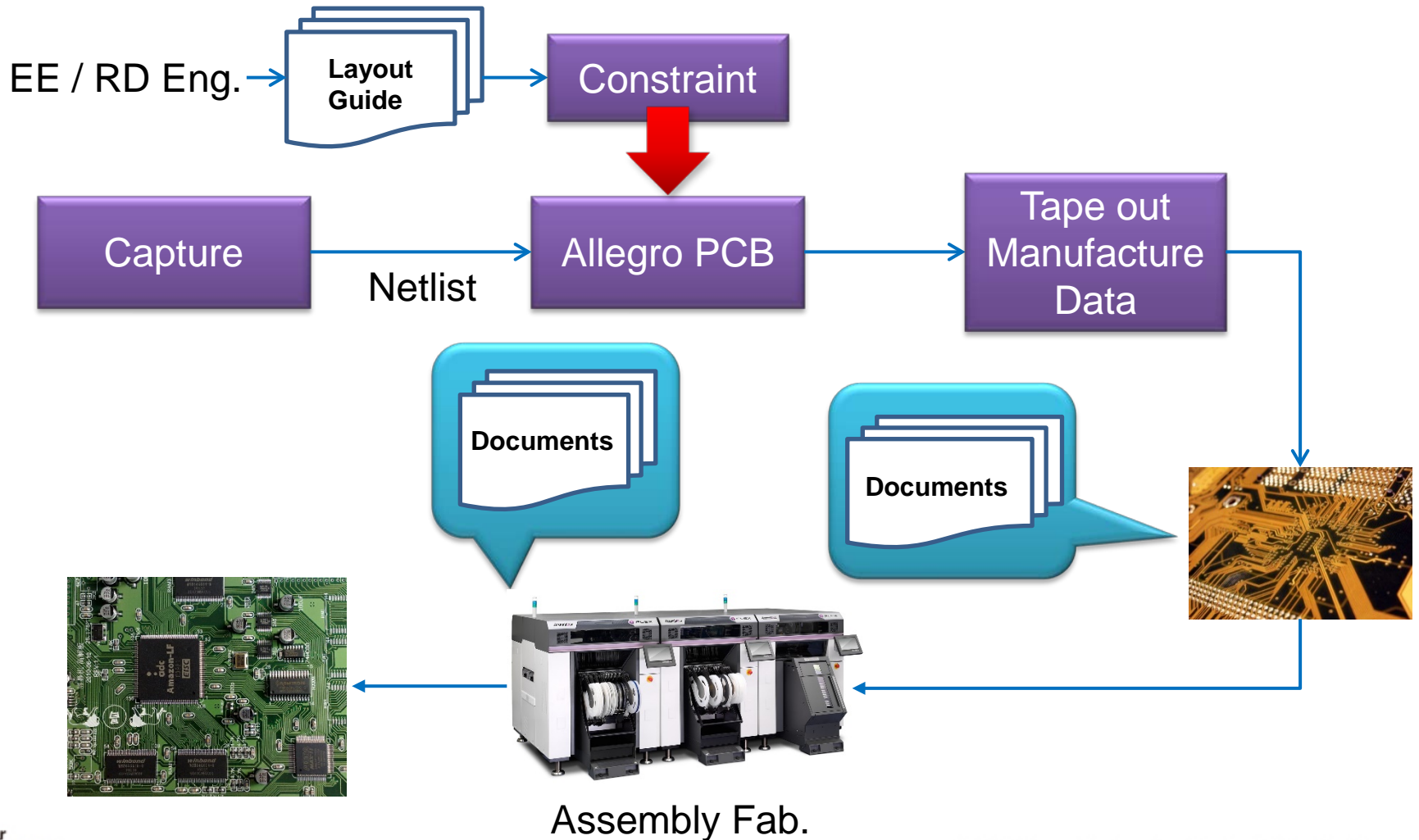
16 / Oct / 2015

Topic

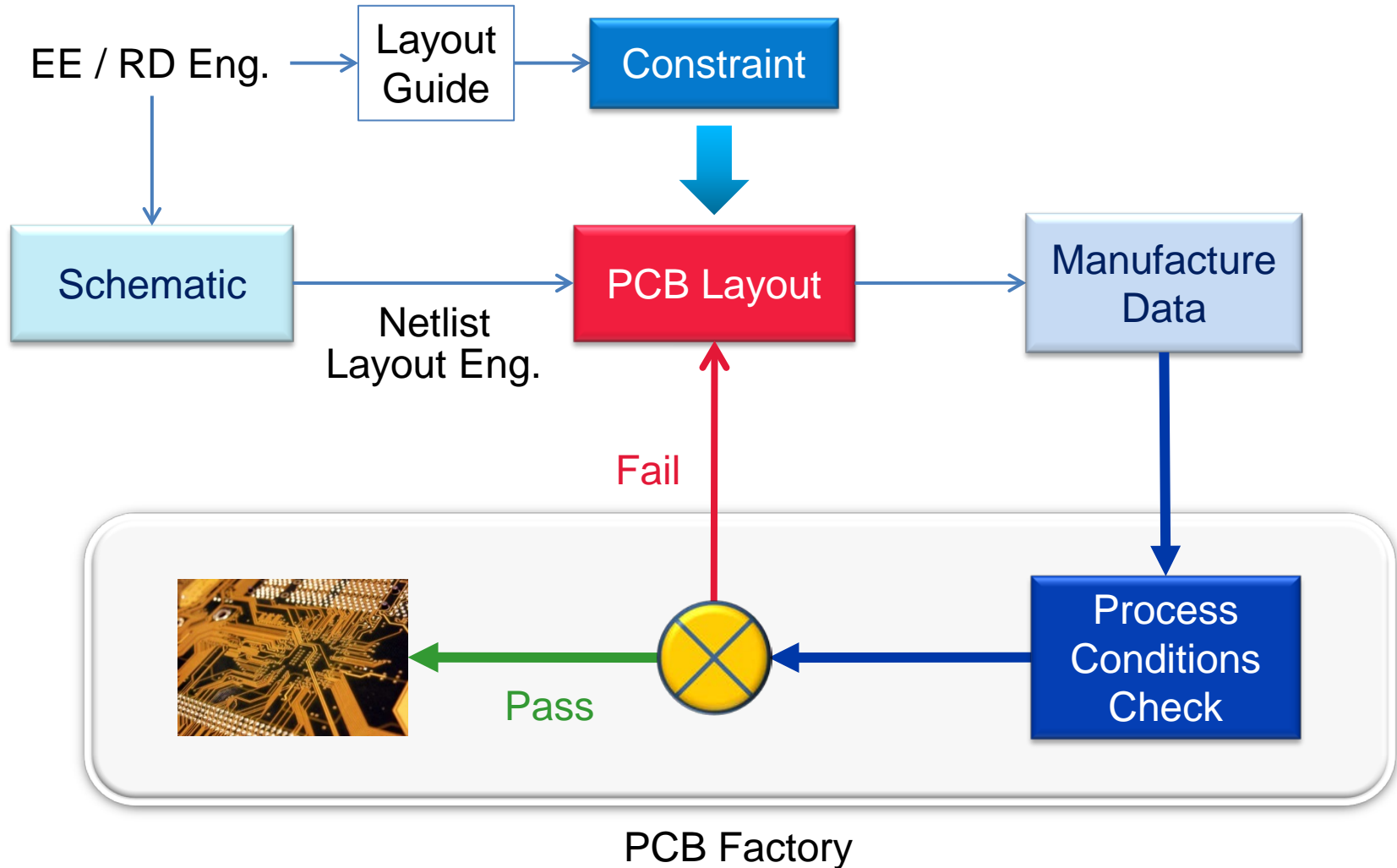
- Allegro DFM Checker
in Allegro PCB Manufacturing Option
- Allegro PCB Rules Developer / Checker Option

PCB Design & Production Flow

- Documents requirement for production

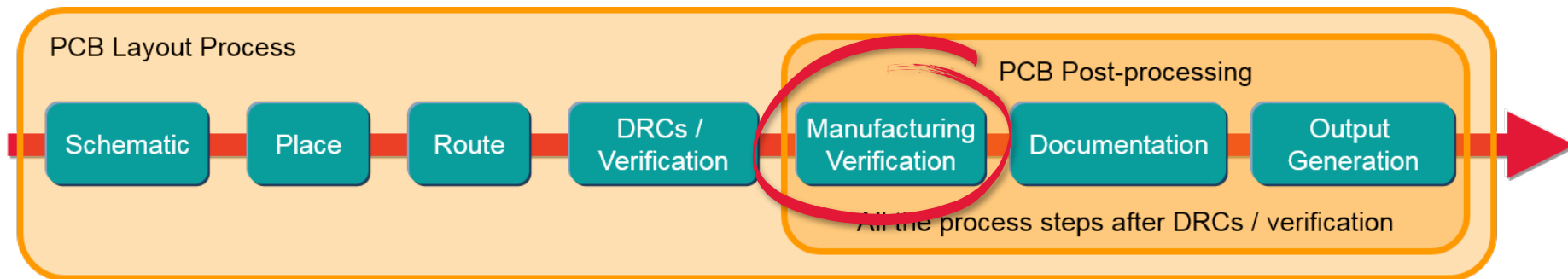


PCB Design Rule Check Workflow



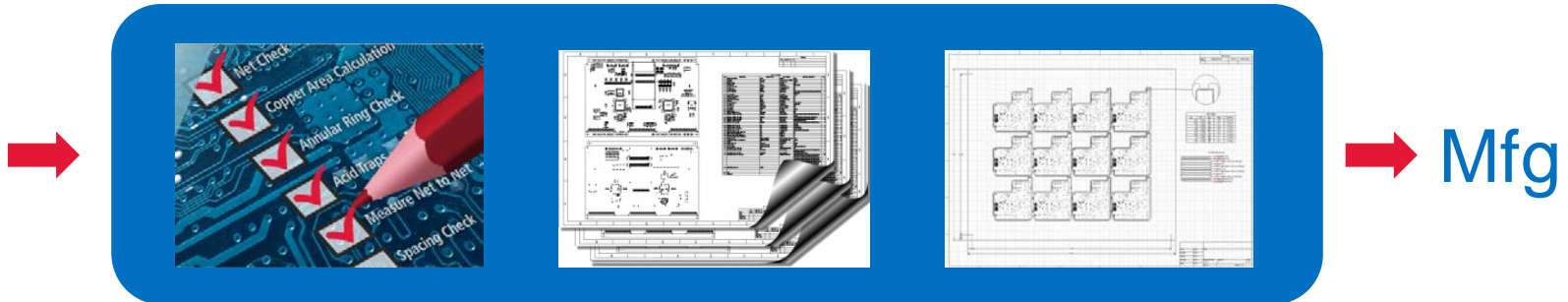
Why to Check Manufacturing Issues?

- Increasing design complexity requires more specialized checking vs. traditional CAD tool DRCs
- Designs that pass standard DRCs may still contain issues that result in low manufacturing yields, or costly scrap
- Correcting fabrication issues can help to reduce the amount of design modification done by the fabricator
- If the fabricator is modifying your design, you have lost database integrity



Allegro PCB Manufacturing Option

- DFM Checker
 - Easy and fast check manufacture data on Allegro PCB designer environment.
 - Cross probing the point of failure to Allegro PCB designer.
- Documentation Editor
 - Easy and fast generate PCB manufacture documents.
- Panel Editor
 - Easy to make panelization, generate documents and components coordinate for Pick & Place

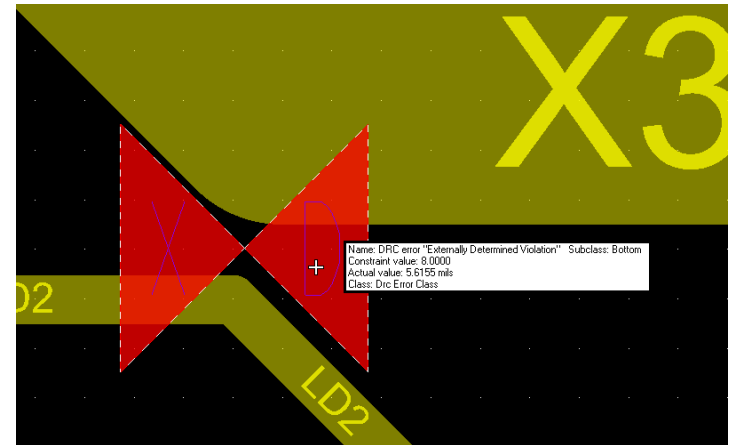


Allegro DFM Checker

What's DFM Checker

- Fabrication Data check
 - IPC-2581
 - Multiple rules check options
 - Rules by group (Streams)
- Imports physical check values
 - Constraint regions
 - Default physical check values
 - Create and store rule set templates
- Check runs in “Background”
 - Allegro editor and document editor can be used while checks are running
- Results review
 - Violations listed by check category
 - Cross probe of violation between violations list and Allegro PCB Editor
- Catches Violations before releasing to Manufacturing

POWER-REGION_Outer_Electrical - 17 Errors, 0 Hidden										
TT - Track to Track - 1 Errors, 0 Hidden										
	Id	Distance	Layer	X1	Y1	X2	Y2	Min Dist	Validated	Comment
	0	5.6155	L7.BOTTOM	2400.6063	2602.4254	2401.9683	2607.8732	8.0000	<input type="checkbox"/>	
TP - Track to Pad - 5 Errors, 0 Hidden										



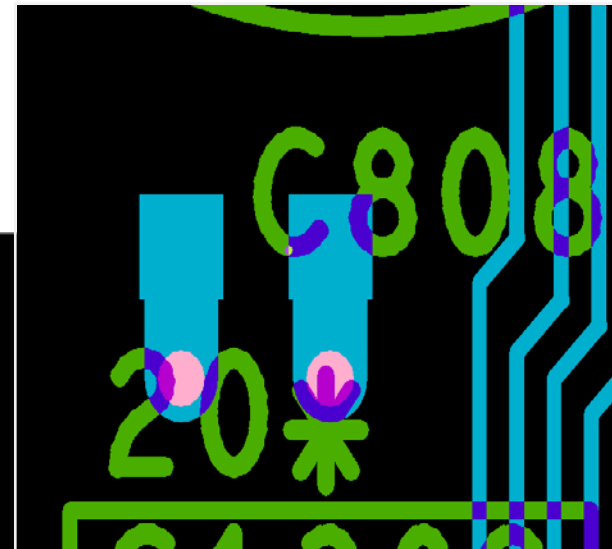
Design For Manufacture (DFM)

DFM check categories

- Copper checks
 - Trace to trace, trace to pad, pad to pad, shape to pad,
 - Redundant pads, superimposed pads
 - Pads without drills
 - Antennas
 - Slivers
 - Acid traps
- Via checks
 - Through hole, laser drill
 - Plated, unplated
 - Backdrills to trace
- Plane checks
 - Positive, Negative
- Solder mask checks
- Paste mask checks
- NC Drill checks
 - Overlapping, coincidental, redundant
 - Drill to drill
 - Imploded Mill path, arcs
- Silkscreen checks
 - To soldermask, board outline
 - Min silkscreen width
- Netlist Compare
- Design Analysis

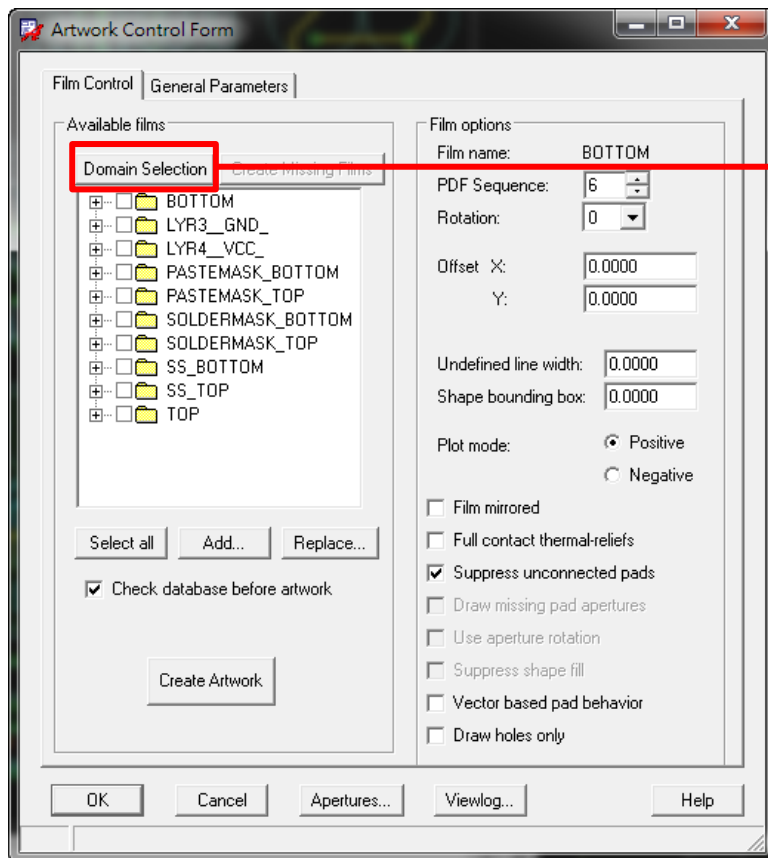
SECOND SET OF EYES

- Quality
- Cost
- Right first time
- Efficiency



Data Preparation

- All artwork film records must be defined
- IPC-2581 Layer mapping must be defined



The 'Film Domain Setting' dialog box is shown with the 'IPC2581' column highlighted by a red box. The table below shows the mapping of film names to their respective settings.

Film Name	Artwork	IPC2581	PDF	Visibility
BOTTOM	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
LYR3_GND_	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
LYR4_VCC_	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PASTEMASK_BOTT	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PASTEMASK_TOP	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SOLDERMASK_BOT	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SOLDERMASK_TOP	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SS_BOTTOM	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SS_TOP	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
TOP	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Create DFM Project

2

DFM Checker Panel Editor Documentation Editor New from Wizard Help Documentation Editor Tutorial Panel Editor Tutorial DFM Checker Tutorial Close

Tools Getting Started Exit

Release Package

A Release Package is a repository for all manufacturing content. It is used to store and view all deliverables for manufacturing.

Current Working Release Package: DEMOL_XML
Location: D:\Allegro_DFM_Lab\Mfg_Opt_Demo\Mfg_Opt_Demo\DEMOL_XML

Release Package Actions

1

Create New Create a release package for the current PCB design. Use this option to create a new release package or replace the current release package. Use Template

Refresh Open the release package and enable updates. Use this option to annotate design changes to the release package.

Open Open the release package but disallow updates. Use this option to edit or view the release package in its current state.

Revisions

Preserve the current state of a release package as a revision. Older revisions can be restored and set as the current revision. Warning: Restoring a revision may result in loss of modifications made to the current release package.

Current Revision Description: Last Saved:

Save As Revision **Restore Revision** **Delete Revision**

Description	Last Saved

Release Package Status

The status of release package content relative to the most recent PCB design changes are shown below.

Content	Status
DFM Checker	Not Initiated
Documents	Not Initiated
Panel Design	Not Initiated

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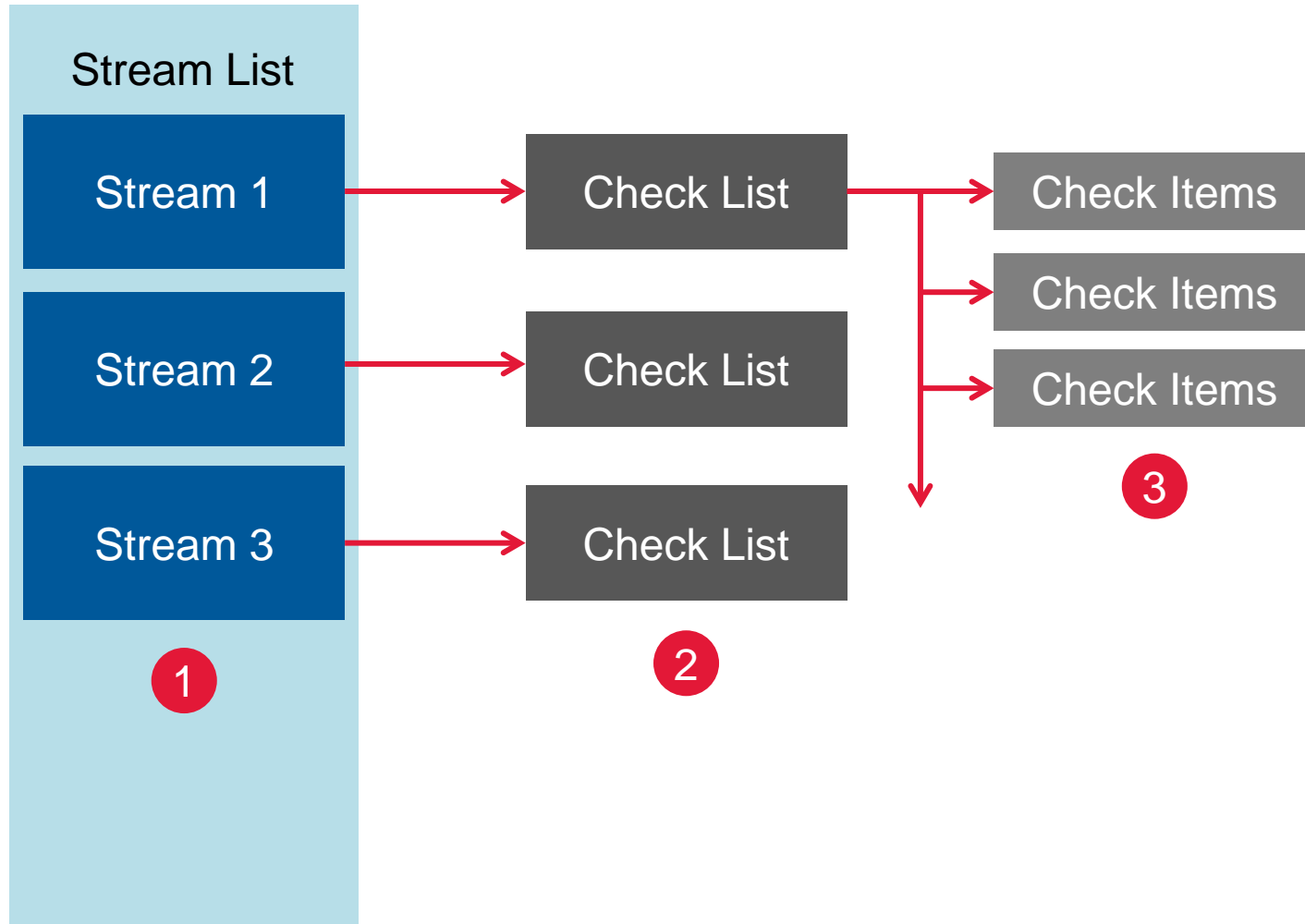
Build Stream & Check Rule

The screenshot displays the Allegro DFM Checker interface. The main window is titled "demoL.dfm* - Allegro DFM Checker". The interface includes a menu bar (File, View, Tools), a toolbar with various icons, and a "Stream List" panel on the left. The "Stream List" panel shows a table of streams, with "demoL" selected. The main area displays a table of stream rules, with a red box highlighting the "Check Rule" button and the table content.

Execute	Name	Type
<input checked="" type="checkbox"/>	Preprocess Optimization 0	Preprocess
<input checked="" type="checkbox"/>	Netlist Extract	Netlist Compare
<input checked="" type="checkbox"/>	Signal Layer 2	Signal Layer
<input checked="" type="checkbox"/>	Negative Plane 3	Negative Plane
<input checked="" type="checkbox"/>	Solder Mask Layer 4	Solder Mask
<input checked="" type="checkbox"/>	Silkscreen Layer 5	Silkscreen
<input checked="" type="checkbox"/>	Paste Mask Layer 6	Paste Mask
<input checked="" type="checkbox"/>	NC Data Layer 7	NC Data
<input checked="" type="checkbox"/>	demoL_Outer_Electrical	Signal Layer
<input checked="" type="checkbox"/>	POWER-REGION_Outer_Electrical	Signal Layer
<input checked="" type="checkbox"/>	demoL_Inner_Neg_Electrical	Negative Plane
<input checked="" type="checkbox"/>	POWER-REGION_Inner_Neg_Electrical	Negative Plane

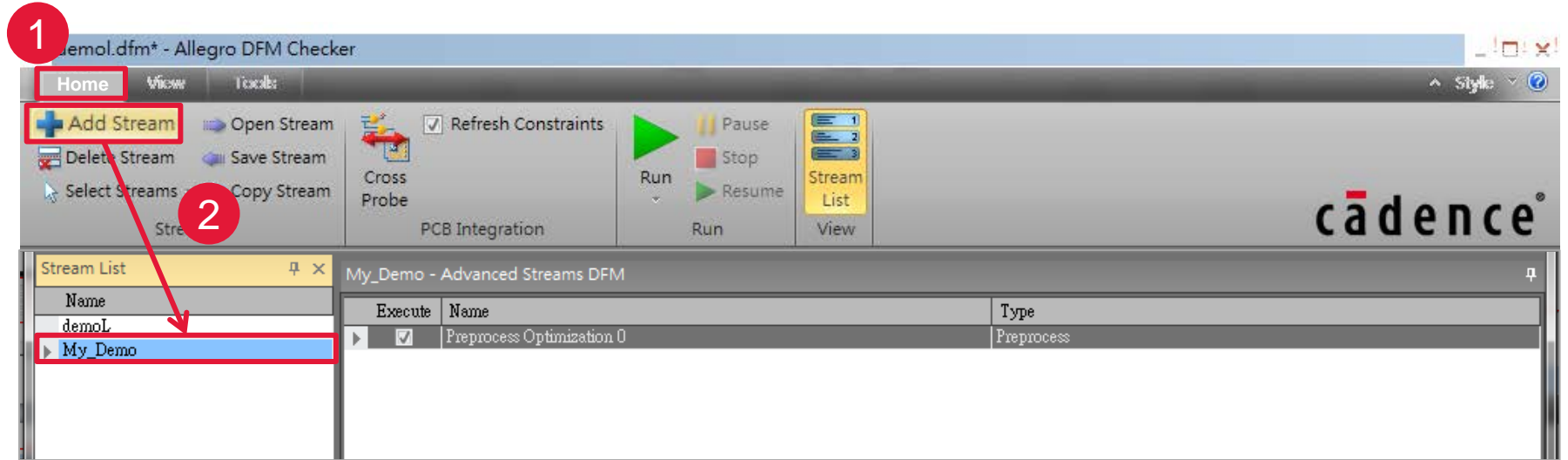
Check Rule

Stream Setting Flow



Create Stream

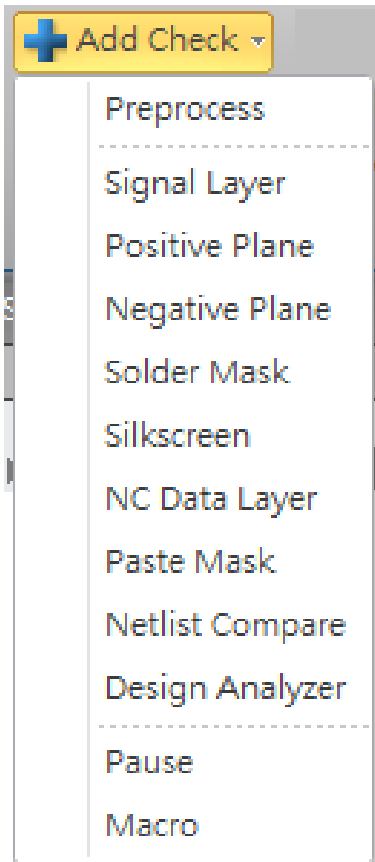
- Create Stream



- Add Checking Rule

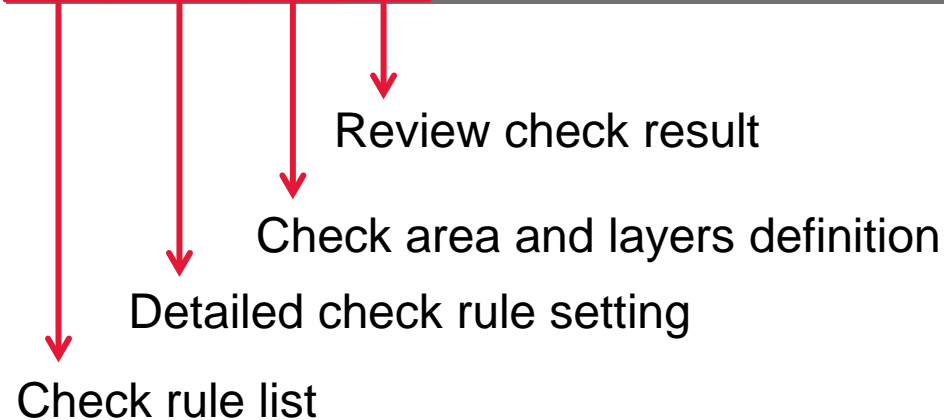


Add Check Rule



Execute	Name	Type
<input checked="" type="checkbox"/>	Preprocess Optimization 0	Preprocess
<input checked="" type="checkbox"/>	Netlist Compare 1	Netlist Compare
<input checked="" type="checkbox"/>	Signal Layer 2	Signal Layer
<input checked="" type="checkbox"/>	Negative Plane 3	Negative Plane

Checks Constraints Areas Results



Check Rule Sample

The screenshot displays the Allegro PCB Designer interface. The 'Objects' table shows constraints for 'demoLGr' and 'POWER-REGION POWER NETS'. The 'Line to' table lists various constraint types and their values. The 'demoLGr.dfm* - Allegro DFM Checker' window shows the 'Advanced Streams DFM' section with a table of properties and values.

Objects	Referenced Spacing CSet	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bond Finger
Type	S	Name	mil	mil	mil	mil	mil	mil	mil	mil
Den		demoLGr	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000
Rgn		POWER-REGION	8.0000	8.0000	6.0000	8.0000	8.0000	10.0000	10.0000	5.0000

Property	Value
<input checked="" type="checkbox"/> demoLGr_Outer_Electrical - Signal Layer check	
<input checked="" type="checkbox"/> POWER-REGION_Outer_Electrical - Signal Layer check	
Name	POWER-REGION_Outer_Electrical
Layers	[Outer Electrical]
Drill Layers	[All NC]
Checks	TT, TC, CC, TP, CP, CPCP, SMSM, VV
Shape/Size Filter	
NC Tool Filter	
Area	POWER-REGION_All_Electrical
<input type="checkbox"/> Auto Fix Errors	
<input checked="" type="checkbox"/> Details	
<input checked="" type="checkbox"/> Board Outline spacing	
<input checked="" type="checkbox"/> Copper spacing (Different Nets)	
<input checked="" type="checkbox"/> TT - Track to Track	8.000000
<input checked="" type="checkbox"/> TC - Track to Copper	10.000000
<input checked="" type="checkbox"/> CC - Copper to Copper	12.000000
<input checked="" type="checkbox"/> TP - Track to Pad	10.000000
<input checked="" type="checkbox"/> CP - Copper to Pad	10.000000
<input checked="" type="checkbox"/> Pad spacing	

1. 若為單獨對應條件，則 constraint 設定值及接引用，如 Line to Line。
2. 若有多對應條件，則會引用最大 constraint 設定值，如 Line to Pad。

Support Constraint Region

Electrical

Physical

Spacing

Spacing Constraint Set

Net

Net Class-Class

Region

All Layers

Line

Plane

Type	S	Name	Referenced Spacing CSet	Line To										
				Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil	Test Via mil	Shape mil	Bond Finger mil	Hole mil	
*	*		*	*	*	*	*	*	*	*	*	*	*	*
Dsn		demol	DEFAULT	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	5.0000	8.0000
Rgn		POWER-REGION	POWER NETS	8.0000	8.0000	6.0000	8.0000	8.0000	8.0000	10.0000	10.0000	10.0000	5.0000	10.0000

POWER-REGION_Outer_Electrical - Signal Layer check

Name: POWER-REGION_Outer_Electrical

Layers: [Outer Electrical]

Drill Layers: [All NC]

Checks: TT, TC, CC, TP, CP, CPCP, SMSM, VV, LV, TV, THTH, SMV, SMLV, SMTH, VTH, LVTH, DTHC, DT...

Shape/Size Filter:

NC Tool Filter:

Area: POWER-REGION_All_Electrical

Auto Fix Errors

Details

Board Outline spacing

Copper spacing (Different Nets)

TT - Track to Track: 8.000000

TC - Track to Copper: 10.000000

CC - Copper to Copper: 12.000000

TP - Track to Pad: 10.000000

CP - Copper to Pad: 10.000000

Pad spacing

Drill spacing

Annular Ring

Name	POWER-REGION_Outer_Electrical
Layers	[Outer Electrical]
Drill Layers	[All NC]
Checks	TT, TC, CC, TP, CP, CPCP, SMSM, VV, LV, TV, THTH, SMV, SMLV, SMTH, VTH, LVTH, DTHC, DT...
Shape/Size Filter	
NC Tool Filter	
Area	POWER-REGION_All_Electrical
<input type="checkbox"/> Auto Fix Errors	
Details	
<input checked="" type="checkbox"/> Board Outline spacing	
<input checked="" type="checkbox"/> Copper spacing (Different Nets)	
<input checked="" type="checkbox"/> TT - Track to Track	8.000000
<input checked="" type="checkbox"/> TC - Track to Copper	10.000000
<input checked="" type="checkbox"/> CC - Copper to Copper	12.000000
<input checked="" type="checkbox"/> TP - Track to Pad	10.000000
<input checked="" type="checkbox"/> CP - Copper to Pad	10.000000
<input checked="" type="checkbox"/> Pad spacing	
<input checked="" type="checkbox"/> Drill spacing	
<input checked="" type="checkbox"/> Annular Ring	

Netlist Compare

My_Demo - Advanced Streams DFM

Property	Value
<input checked="" type="checkbox"/> Preprocess Optimization 0 - Optimization Preprocess	
<input checked="" type="checkbox"/> Netlist Compare 1 - Netlist Compare	
Name	Netlist Compare 1
Actions	Import, Extract, Run
<input type="checkbox"/> Details	
<input checked="" type="checkbox"/> Import External Netlist	
File name	...
Netlist type	IPC-D-356A
<input checked="" type="checkbox"/> Extract CAM Netlist	
<input type="checkbox"/> Allow CAM nets without pads	
<input type="checkbox"/> Allow Single Point CAM net	
<input type="checkbox"/> Treat Neg Planes as Single CAM net (no splits in Plane)	
<input checked="" type="checkbox"/> Run Netlist Compare	
<input type="checkbox"/> Ignore Extra External Nets at CAM Points	
<input type="checkbox"/> Ignore Missing External Nets for CAM Nets	
<input checked="" type="checkbox"/> Signal Layer 2 - Signal Layer check	
<input checked="" type="checkbox"/> Negative Plane 3 - Negative Plane check	

Checks Constraints Areas Results

Specific external Netlist file(IPC-D-356 format)

可選擇IPC-D-356或 IPC-D-356A

Select Area when run

The screenshot shows the Cadence software interface. The 'Run' button is highlighted, and a context menu is open with the following options:

- Use Entire Area
- Use Board Outline Area
- Use Selected Area

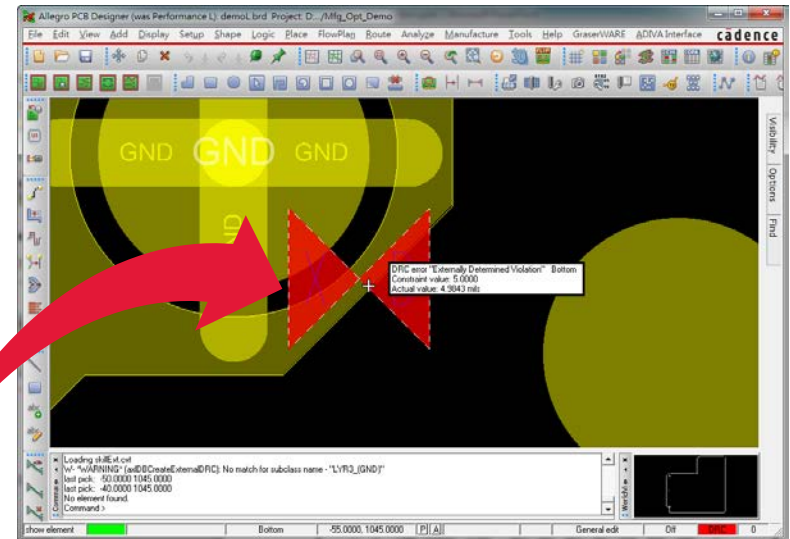
The 'Execute Stream' dialog is also open, showing the following table:

Name	Type
<input checked="" type="checkbox"/> Preprocess Optimization 0	Preprocess
<input checked="" type="checkbox"/> Netlist Extract	Netlist Compare
<input checked="" type="checkbox"/> Signal Layer 2	Signal Layer
<input checked="" type="checkbox"/> Negative Plane 3	Negative Plane
<input checked="" type="checkbox"/> Solder Mask Layer 4	Solder Mask
<input checked="" type="checkbox"/> Silkscreen Layer 5	Silkscreen
<input checked="" type="checkbox"/> Paste Mask Layer 6	Paste Mask
<input checked="" type="checkbox"/> NC Data Layer 7	NC Data
<input checked="" type="checkbox"/> demoL_Outer_Electrical	Signal Layer
<input checked="" type="checkbox"/> POWER-REGION_Outer_Electrical	Signal Layer
<input checked="" type="checkbox"/> demoL_Inner_Neg_Electrical	Negative Plane
<input checked="" type="checkbox"/> POWER-REGION_Inner_Neg_Electrical	Negative Plane

The 'Stream List' on the left shows a single entry: demoL.

Category Results & Cross Probing

- Constraints and constraint regions are extracted by DFM Checker
 - From the layer structure, constraints and constraint regions
- Automatically creates a default verification “stream”
 - Selection in the error lists in DFM Checker will zoom to the error location in PCB Editor
 - Details shown through tooltip in PCB Editor



Id	Distance	Layer	X1	Y1	X2	Y2	Min Dist	Validated	Com...
8	14.1421	L5-LYR4_(VCC)	3755.0000	-325.0000	3765.0000	-335.0000	15.0000		

Id	Min Width	Layer	X	Y	Max Size	Max Noise	Validated	Comm...
9	4.9843	L7-BOTTOM	-56.4680	1047.0661	5.0000	50		

Id	Dista...	Layer	Layer	X1	Y1	X2	Y2	Pad S...	S/M ...	Min ...	Validated	Com...
10	2.5000	L10.SOLD...	L1:TOP	822.5...	1862...	822.5...	1865...	55.00...	50.00...	3.0000		
11	2.5000	L10.SOLD...	L1:TOP	822.5...	1912...	822.5...	1915...	55.00...	50.00...	3.0000		

Generate Report

The screenshot shows the 'Generate Report' button in the software's toolbar, which is highlighted with a red box. Below the toolbar, the 'Report Stream Results' dialog box is open, showing a table of report items. The table has columns for 'Ch...', 'R...', 'Id', 'N...', 'D...', 'S...', 'M...', 'S...', 'S...', 'L...', and 'E...'. The rows list various checks and routines, such as 'CB - Copper to One Up Border', 'Global fiducials', 'KM - Silkscreen to Solder Mask', etc., along with their counts for different layers and checks.

Report Stream Results

Stream / Execution: demoL
 Execution 1 / 下午 05:44:31, 2015/6/21/

Ch...	R...	Id	N...	D...	S...	M...	S...	S...	L...	E...
Sig...	C...	0	0...						L...	
Sig...	C...	1	0...						L...	
Sig...	C...	2	3...						L...	
Sig...	C...	3	1...						L...	
Sig...	C...	4	1...						L...	
Sig...	C...	5	5...						L...	
Sig...	C...	6	1...						L...	
Sig...	C...	7	1...						L...	
Sig...	M...	8			4...				L...	
SoL...	S...	9	2...						L...	
SoL...	S...	10	2...						L...	
SoL...	S...	11	2...						L...	
SoL...	S...	12	2...						L...	
SoL...	S...	13	2...						L...	
SoL...	S...	14	2...						L...	
S...	S...	15	2...						L...	

All Checks

- POWER-REGION_Outer_Electrical
- Paste Mask Layer 6
- Signal Layer 2
- Silkscreen Layer 5
- Solder Mask Layer 4
- demoL_Outer_Electrical

All Routines

- CB - Copper to One Up Border
- Global fiducials
- KM - Silkscreen to Solder Mask
- MMSMD - Missing Mask for SMD
- MMUP - Missing Mask for Undrilled Pad
- MP - Missing Paste Mask on SMD Pads
- MPMP - Mask Pad to Mask Pad
- MS - Mask Silvers
- MSC - Missing Copper
- MSP - Missing Pad
- MT - Minimum Track
- MT - Solder Mask to Track
- MW - Minimum Width
- PC - Paste Mask to Copper
- SBD - Silkscreen to Board Outline
- SMDM - SMD to Mask (Annular Ring)

All Layers

- BOTTOM
- IPC2581DRILL_1-4
- LYR3_(GND)
- LYR4_(VCC)
- PASTEMASK_BOTTOM
- PASTEMASK_TOP
- SOLDERMASK_BOTTOM
- SOLDERMASK_TOP
- SS_BOTTOM
- SS_TOP
- TOP

Buttons: Export, Print, OK

Error Chart

The screenshot shows the Allegro PCB Designer interface. The main window displays a PCB layout. Overlaid on this is the 'Error Chart' window, which shows a bar chart of error counts. The chart has a y-axis from 0 to 13 and an x-axis from 0 to 15. A tooltip is visible over the bar at x=4.5, showing details for 10 errors: 'demoLGr_Outer_Electrical: TP - Track to Pad' with a list of coordinates and counts.

Another window, 'Advanced Streams DFM', is open, showing a tree view of error categories and their counts. A red arrow points from the 'Error Chart' window to the 'CB - Copper to One Up Border' category in the DFM window.

Advanced Streams DFM Error Summary:

- Execution 0 / 下午 05:17:13, 2015/9/15/ - 26 Errors, 0 Hidden
- Signal Layer 2 - 11 Errors, 0 Hidden
- CB - Copper to One Up Border - 4 Errors, 0 Hidden
- FF - Non-drilled flashes to all pad types - 7 Errors, 0 Hidden
- Silkscreen Layer 5 - 5 Errors, 0 Hidden
- KM - Silkscreen to Solder Mask - 1 Errors, 0 Hidden
- SBO - Silkscreen to Board Outline - 4 Errors, 0 Hidden

CB - Copper to One Up Border Error Table:

Id	Distance	Layer	X1	Y1	X2	Y2
0	0.0000	L3:LYR3_(GND)	-2.6313	2000.0692	3.8234	2000.0692
1	10.6065	L3:LYR3_(GND)	0.0000	2150.0000	7.5000	2142.0000
2	0.0000	L5:LYR4_(VCC)	-2.6313	2000.0692	3.8234	2000.0692
3	14.1421	L5:LYR4_(VCC)	0.0000	2150.0000	10.0000	2142.0000

KM - Silkscreen to Solder Mask Error Table:

Id	Distance	Silk Layer	X	Y	Line Width	S/M
11	0.0000	L16:SS_BOTTOM	1950.0000	2200.0000	5.0000	35.0000

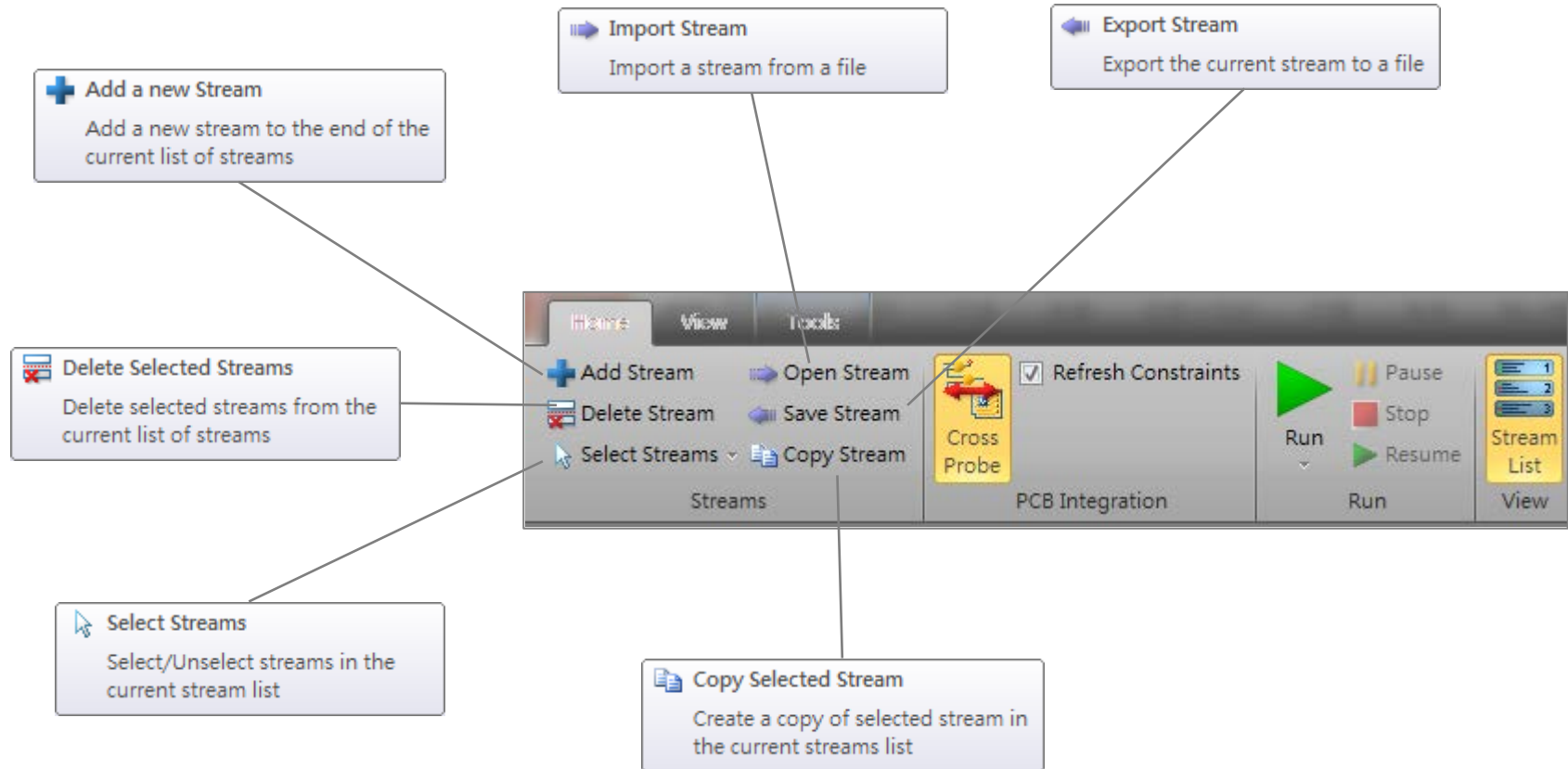
SBO - Silkscreen to Board Outline Error Table:

Id	Distance	Layer	X1	Y1	X2	Y2
12	0.0000	L13:SS_TOP	1803.8331	2203.8331	1803.8331	2203.8331
13	0.0000	L13:SS_TOP	1850.0000	2250.0000	1850.0000	2250.0000
14	0.0000	L13:SS_TOP	1850.0000	2327.9301	1850.0000	2327.9301
15	1.3762	L13:SS_TOP	1848.6238	2363.8137	1850.0000	2363.8137

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Stream Rule Reuse



Summary of DFM Checker

- Check manufacture data (IPC-2581) with design rules
- Auto generate IPC-2581 to go through DFM check flow
- Direct copy constraint setting value into DFM check rule
- Support constraint region design check
- Netlist Compare for consistency check
- Select Area when run
- Category Results & Cross Probing
- Error Chart for Quality Analysis
- Reuse of Stream

Allegro PCB Rules Developer / Checker Option

Allegro PCB Rules Developer & Checker

Many companies want the ability to extend the rules that Cadence® Allegro® products provide

- Customized to their fabrication/assembly needs
- Adopt new emerging fabrication, assembly, test processes before they are supported by the tools

- **Allegro Rules Developer**

- Enables customers to create new rules using a relational algebra expression language
 - A programming language that simplifies the creation of rules for DRC checks of all design data types in Allegro platform
 - A platform independent and version agnostic with Allegro platform
- Allows sharing of custom rules with other user sites, vendors and customers
- Provides a starter set of rules to help users get started quickly

- **Allegro Rules Checker**

- Enables customization of rules for a set of designs
- Integrated with Allegro PCB Editor
 - Load rules into Allegro Constraint Manager
- Run the checks
- Adds DRC violation markers in Allegro PCB Editor

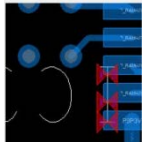


RAVEL DRC System for PCB and SiP

DEVELOPER

DRC Description in Design Rule Manual

Minimum wire to wire vertical spacing at optical crossing



Parabolic model: maximum possible deflection of wire at point x is $D = 4Rx(L-x)/L$, where R is the ratio between maximum wire deflection in the middle and the wire length



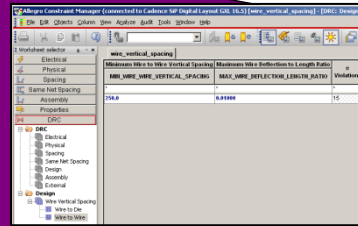
Check if distance between Topmost ViaPill on the Top layer and Board Outline meets minimum clearance. If not, drill via has the Board Outline violation rule to check. Look for a rule.

DRC Source Code in RAVEL Language

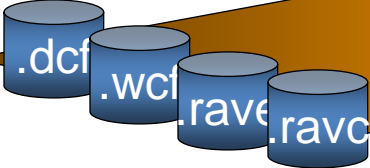
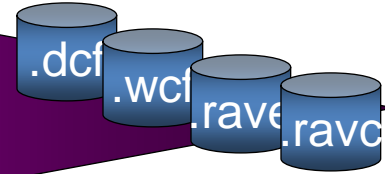
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1) RAVEL DRC: MIN WIRE TO WIRE VERTICAL SPACING
2) RAVEL DRC: MIN WIRE TO WIRE VERTICAL SPACING
3) RAVEL DRC: MIN WIRE TO WIRE VERTICAL SPACING
4) RAVEL DRC: MIN WIRE TO WIRE VERTICAL SPACING
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```

DRC Compilation, Encryption and Integration in Constraint Manager



DRC Export to Constraint Manager Files and Batch DRC Files

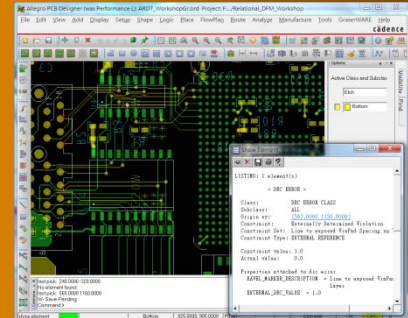
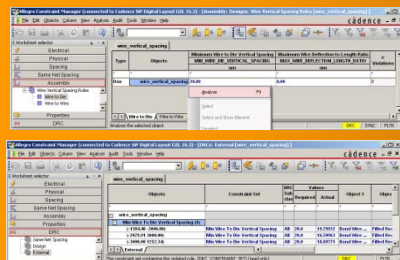
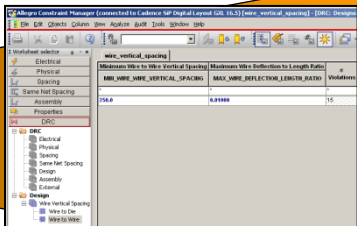


DRC Import from Constraint Manager Files or Batch DRC Files

DRC Selection and Constraint Modification in Constraint Manager or Batch Control File

DRC Execution in Constraint Manager or in Batch

DRC Cross-Probing in Allegro PCB or SiP Layout

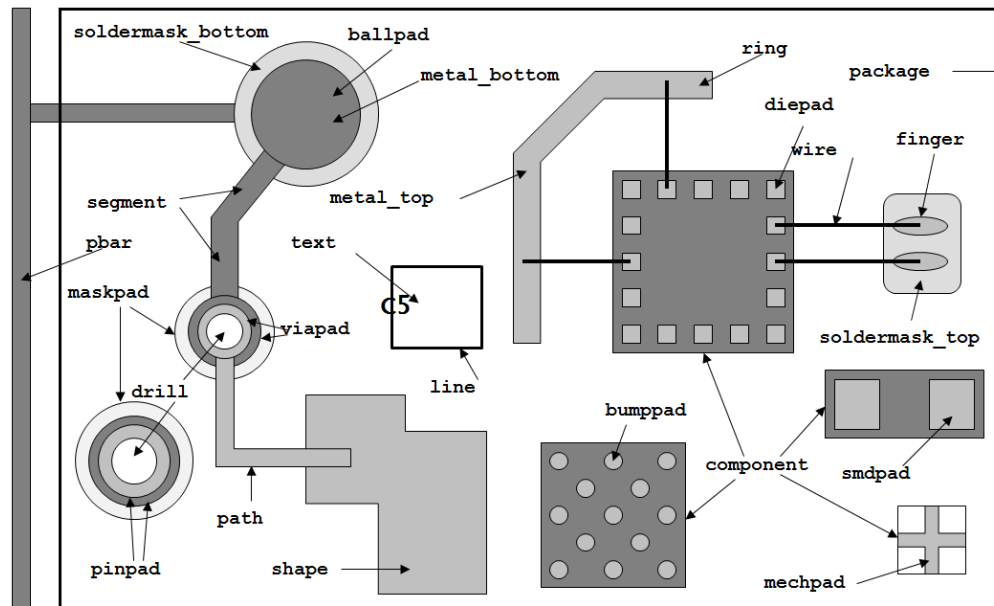


Checker



What is Ravel?

- Relational Algebra Verification Expression Language
- Ravel objects closely correspond to SiP / PCB objects
- Forms relations between objects and queries relational data through combination and filtering
- Can derive new objects through geometric and polygon operations



What is Ravel?

- Fully integrated with SPB tools - directly runs on Allegro SiP / PCB design file
 - Manufacturing data export is not required
- Integrates seamlessly with Constraint Manager
- Geometrical operations are much faster
- Allows sharing of encrypted rules with customers
- Performs checks between different design data types
 - Silkscreen text-Soldermask
- Fewer lines of code to write the rules
- Easy to learn

Example –

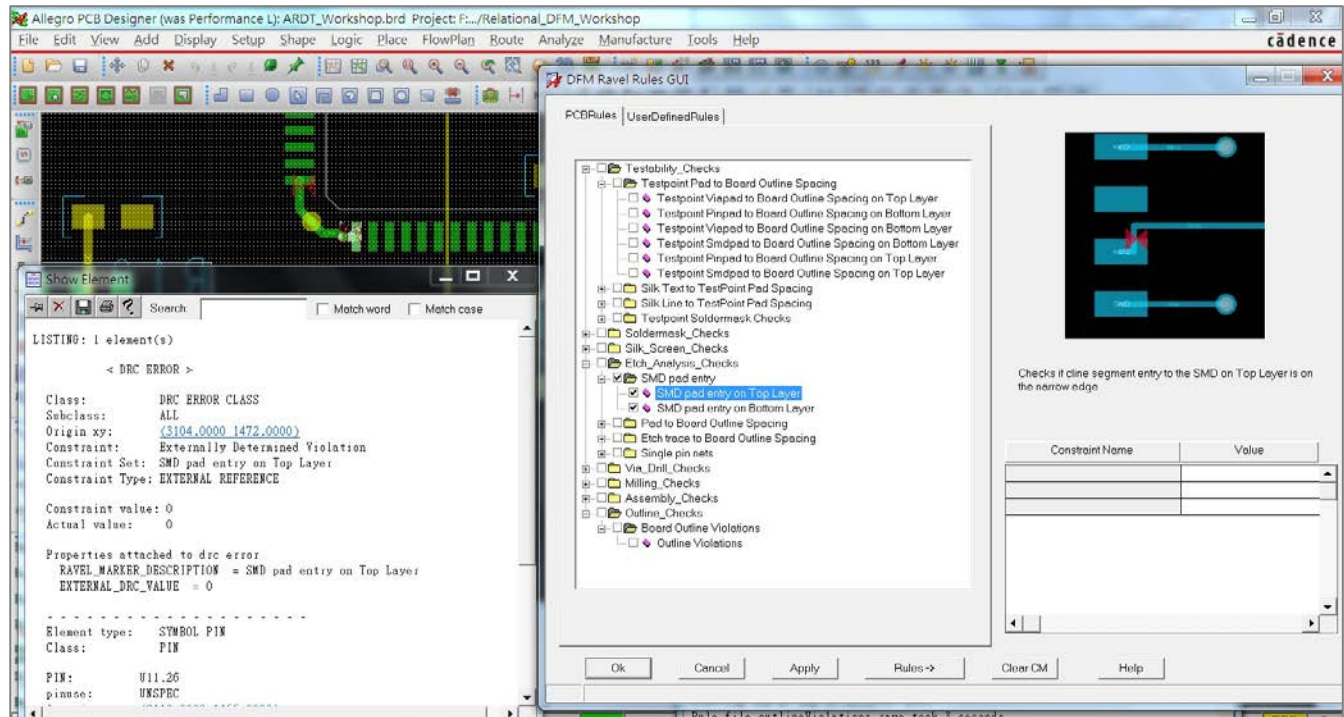
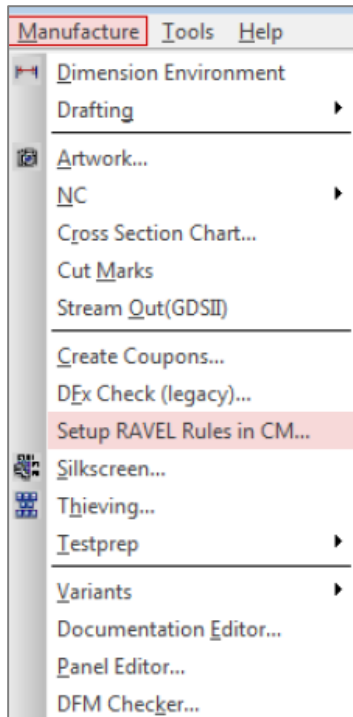
On a 24-layer board, the “trace to board edge spacing” rule checks the distance between 17700+ clines (4400+ nets) and board outline for a constraint value of 100, and reports 2 errors in **10** seconds

Starter Rules

- **Silkscreen rules**
 - Min Spacing Silkscreen Line to pad
 - Min Spacing Silkscreen Text to pad
 - Min Spacing Silkscreen Line to exposed pad
 - Min Spacing Silkscreen Text to exposed pad
 - Min Height of Silkscreen
 - Min Length Silkscreen line
- **Etch Analysis Checks**
 - Min Spacing between Pin pad to board outline
 - Min Spacing between SMD pad to board outline
 - Min Spacing between Etch Trace to board outline
 - Single pin nets check
 - Trace entry into SMD pad
- **Testability Checks**
 - Min Spacing between Silkscreen text to testpoint pads
 - Min Spacing between Silkscreen line to testpoint pads
 - Mask clearance check for testpoint pad
 - Min Spacing testpoint pads and board outline
- **Soldermask Rules**
 - Min Spacing Soldermask to Board outline
- **Via Drill Rules**
 - Max depth of blind microvia
- **Assembly checks**
 - Min Spacing between pad and component

Rule Checker

- To start the Allegro Relational Rules Checker Kit, choose **Manufacture - Setup RAVEL Rules in CM...**



Define Check Values

- Define Ravel check item & value

Allegro PCB Designer (was Performance L): ARDT_WorkshopGr.brd Project: F:\...\Relational_DFM_Workshop

File Edit View Add Display Setup Shape Logic Place FlowPlan Route Analyze Manufacture Tools GraserWARE Help

DFM Ravel Rules GUI

PCBRules | UserDefinedRules |

- Testability_Checks
- Soldermask_Checks
- Silk_Screen_Checks
 - Silk Text to Pad Spacing
 - Text to SmdPad Spacing on Bottom Layer
 - Text to PinPad Spacing on Top Layer
 - Text to ViaPad Spacing on Bottom Layer**
 - Text to PinPad Spacing on Bottom Layer
 - Text to SmdPad Spacing on Top Layer
 - Text to ViaPad Spacing on Top Layer
 - Silk Line to Exposed Pad Spacing
 - Silk Line to Pad Spacing
 - Silkscreen Lone Line Minimum Length
 - Silk Text height
- Etch_Analysis_Checks
- Via_Drill_Checks
- Milling_Checks
- Assembly_Checks
- Outline_Checks

Checks if distance between Silkscreen Text and ViaPad on the Bottom layer meets minimum spacing required

Constraint Name	Value
MIN_TXT_TO_VIAPAD_BOT_DIST	1.00

Ok Cancel Apply Rules-> Clear CM Help

function RELM_SILK_TEXT_TO_PAD_SPACING_TEXT_TO_SMDPAD_SPACING_ON_TOP...
function RELM_SILK_TEXT_TO_PAD_SPACING_TEXT_TO_SMDPAD_SPACING_ON_BOT...
Loading Rules...
DFM rules are loaded from Env. variable DFM_RAV_PATH, which is set to '...' 'C:/Cadence/...'
Command >

Bottom 3265.0000, 225.0000 Etch edit Off DRC 0

Load Earlier Selection

- Reuse predefined Ravel check items & values

The screenshot shows the Allegro PCB Designer interface with the DFM Ravel Rules GUI open. The GUI is divided into two main sections: 'PCBRules' and 'UserDefinedRules'. The 'UserDefinedRules' section contains a tree view of rules, including 'Silk_Screen_Checks' and 'Silk Text to Pad Spacing'. A table on the right side of the GUI shows the constraint name 'MIN_TXT_TO_PINPAD_BOT_DIS' with a value of 4.00. A context menu is open over the 'Load Earlier Selection...' option.

Constraint Name	Value
MIN_TXT_TO_PINPAD_BOT_DIS	4.00

Add User Defined Rules

- Load customized (compiled) ravel rules

The screenshot shows the Allegro PCB Designer interface with the DFM Ravel Rules GUI open. The main window displays a PCB layout. The DFM Ravel Rules GUI has two tabs: 'PCBRules' and 'UserDefinedRules'. The 'UserDefinedRules' tab is active, showing a list of rules:

- Testpoint Pad to Board Outline Spacing
 - Testpoint Viaepad to Board Outline Spacing on Top Layer
 - Testpoint Pinpad to Board Outline Spacing on Bottom Layer
 - Testpoint Viaepad to Board Outline Spacing on Bottom Layer
 - Testpoint Pinpad to Board Outline Spacing on Top Layer
 - Testpoint Smdpad to Board Outline Spacing on Bottom Layer
 - Testpoint Smdpad to Board Outline Spacing on Top Layer

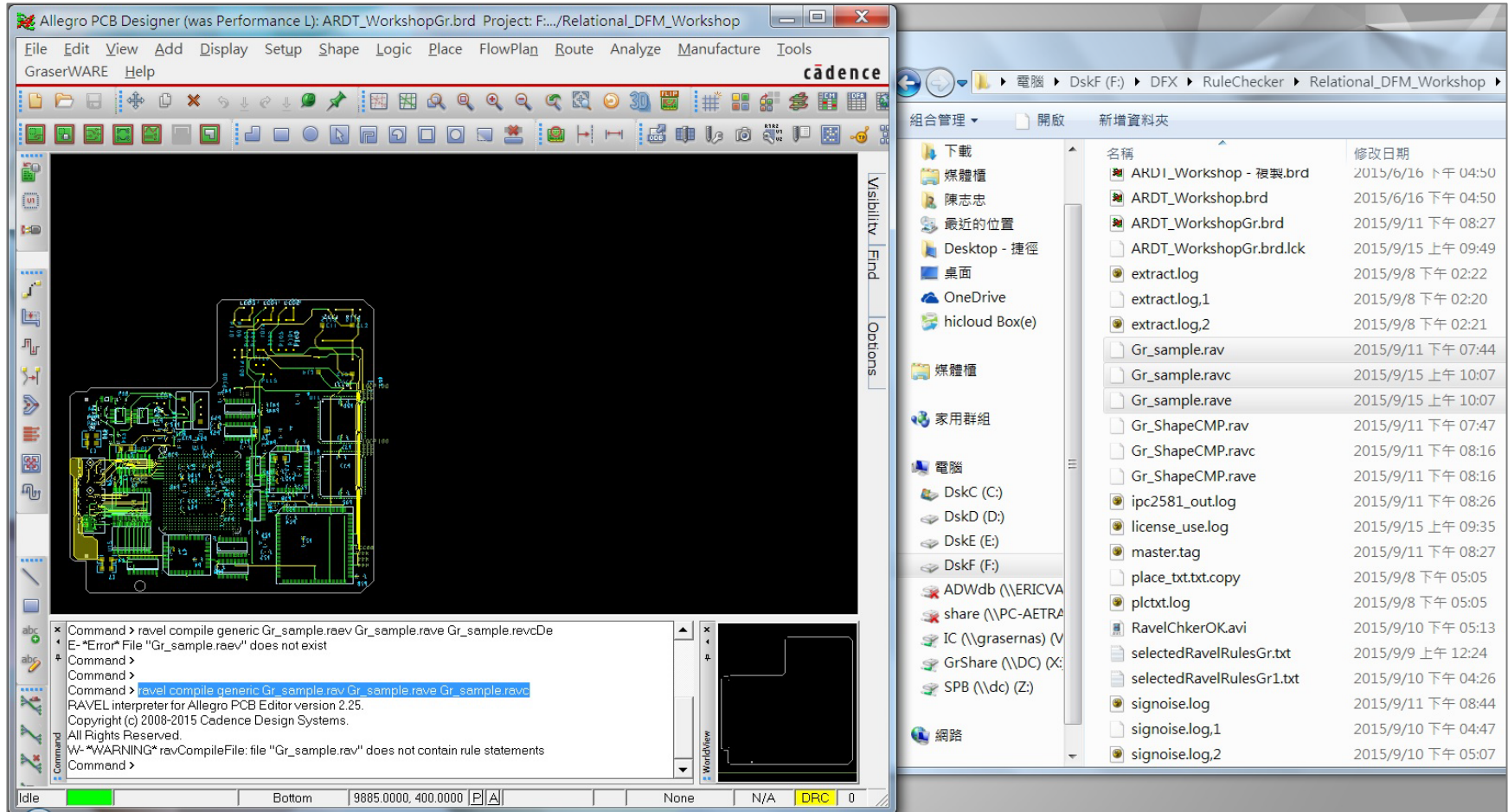
Below the list is a description: "Checks if distance between Silkscreen Text and PirPad on the Bottom layer meets minimum spacing required". A table with columns 'Constraint Name' and 'Value' is present but empty. A context menu is open over the 'Add User Defined Rules...' button, showing options: 'Save Selection...', 'Load Earlier Selection...', and 'Add User Defined Rules...'.

Command >
* Command > ravel compile generic Gr_sample.rav Gr_sample.rave Gr_sample.ravc
RAVEL interpreter for Allegro PCB Editor version 2.25.
Copyright (c) 2008-2015 Cadence Design Systems.
All Rights Reserved.
W- *WARNING* ravCompileFile: file "Gr_sample.rav" does not contain rule statements
Loading dfm_ravel.drc.txt
Loading Rules...
DFM rules are loaded from Env. variable DFM_RAV_PATH, which is set to ("!" "C:/Cadence/S...
Command >

Bottom | 3825.0000, 2225.0000 | P | A | None | N/A | DRC | 0

Compile RAVEL

- Compile .rav to .ravc & .rave (by developer)



The image shows a screenshot of the Allegro PCB Designer software interface. The main window displays a complex PCB layout with various components and traces. The command window at the bottom shows the following text:

```
Command > ravel compile generic Gr_sample.rave Gr_sample.rave Gr_sample.ravecDe
E- "Error" File "Gr_sample.ravev" does not exist
Command >
Command > ravel compile generic Gr_sample.rave Gr_sample.rave Gr_sample.ravec
RAVEL interpreter for Allegro PCB Editor version 2.25.
Copyright (c) 2008-2015 Cadence Design Systems.
All Rights Reserved.
W- *WARNING* ravCompileFile: file "Gr_sample.rav" does not contain rule statements
Command >
```

Below the command window, the status bar shows "Idle", "Bottom", "9885.0000, 400.0000", "None", "N/A", and "DRC 0".

To the right of the Allegro window, a Windows File Explorer window is open, showing the contents of the folder "D:\DFX\RuleChecker\Relational_DFM_Workshop". The file list is as follows:

名稱	修改日期
ARDI_Workshop - 複製.brd	2015/6/16 下午 04:50
ARDT_Workshop.brd	2015/6/16 下午 04:50
ARDT_WorkshopGr.brd	2015/9/11 下午 08:27
ARDT_WorkshopGr.brd.lck	2015/9/15 上午 09:49
extract.log	2015/9/8 下午 02:22
extract.log.1	2015/9/8 下午 02:20
extract.log.2	2015/9/8 下午 02:21
Gr_sample.rav	2015/9/11 下午 07:44
Gr_sample.ravc	2015/9/15 上午 10:07
Gr_sample.rave	2015/9/15 上午 10:07
Gr_ShapeCMP.rav	2015/9/11 下午 07:47
Gr_ShapeCMP.ravc	2015/9/11 下午 08:16
Gr_ShapeCMP.rave	2015/9/11 下午 08:16
ipc2581_out.log	2015/9/11 下午 08:26
license_use.log	2015/9/15 上午 09:35
master.tag	2015/9/11 下午 08:27
place_txt.txt.copy	2015/9/8 下午 05:05
plcxt.log	2015/9/8 下午 05:05
RavelChkerOK.avi	2015/9/10 下午 05:13
selectedRavelRulesGr.txt	2015/9/9 上午 12:24
selectedRavelRulesGr1.txt	2015/9/10 下午 04:26
signoise.log	2015/9/11 下午 08:44
signoise.log.1	2015/9/10 下午 04:47
signoise.log.2	2015/9/10 下午 05:07

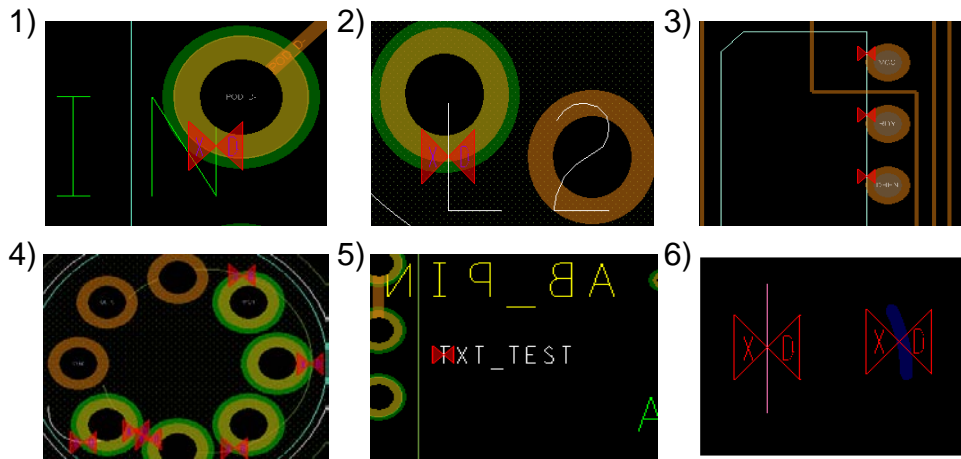
Cross-Highlighted Result in CM

The screenshot shows the Allegro PCB Design GXL (legacy) interface. The main window displays a PCB layout with green and red areas labeled A5 and A6. The Constraint Manager window is open, showing a list of objects with the entry '(837.5000 52.5000)' highlighted in blue. The status bar at the bottom indicates 'source: DRC (837.5000 52.5000) (read only)'.

Objects	Const Se
Name	
Cutout To Board Outline Spacing (2)	
Etch Trace To Board Outline Spacing (10)	
Km - Silkscreen To Solder Mask (4)	
Line To Exposed Pinpad Spacing On Top Layer (13)	
Line To Exposed Viapad Spacing On Bottom Layer (7)	
Line To Exposed Viapad Spacing On Top Layer (9)	
Line To Pinpad Spacing On Top Layer (13)	
Line To Viapad Spacing On Bottom Layer (8)	
Line To Viapad Spacing On Top Layer (9)	
Pinpad To Component Spacing On Bottom Layer (787)	
Pinpad To Component Spacing On Top Layer (182)	
Silkscreen Lone Line Minimum Length On Bottom Layer (2)	
Silkscreen Lone Line Minimum Length On Top Layer (10)	
Smd Pad Entry On Top Layer (15)	
(362.5000 416.0000)	Smd Pa
(562.5000 -40.0000)	Smd Pa
(812.5000 426.0368)	Smd Pa
(837.5000 52.5000)	Smd Pa
(1742.5000 -95.0000)	Smd Pa
(1837.5000 1728.6000)	Smd Pa
(1837.5000 2028.6000)	Smd Pa
(2112.5000 8.5000)	Smd Pa
(2212.5000 1533.6000)	Smd Pa
(2212.5000 1833.6000)	Smd Pa
(2328.5000 1287.5000)	Smd Pa
(3047.0000 894.0000)	Smd Pa
(3047.0000 1529.0000)	Smd Pa
(3104.0000 747.0000)	Smd Pa

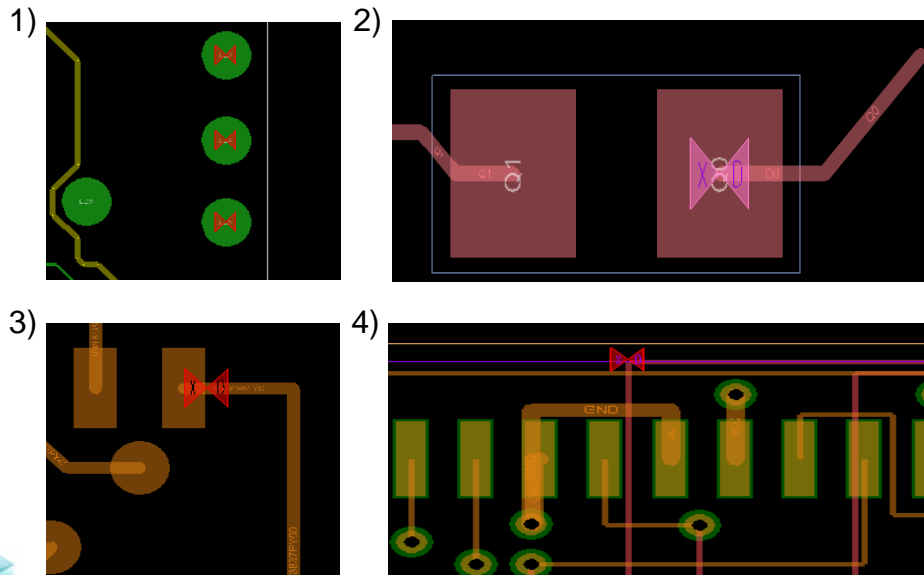
source: DRC (837.5000 52.5000) (read only)

Sample of Starter Rules



Silkscreen rules

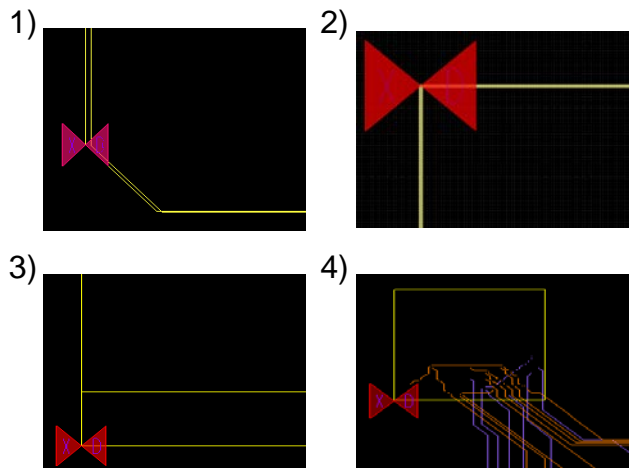
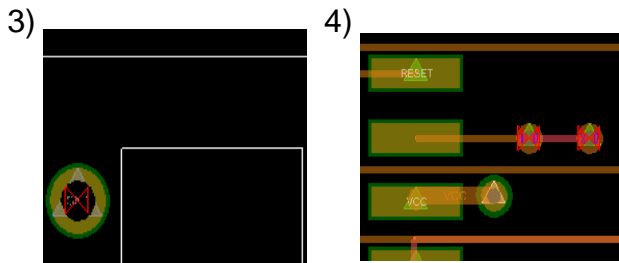
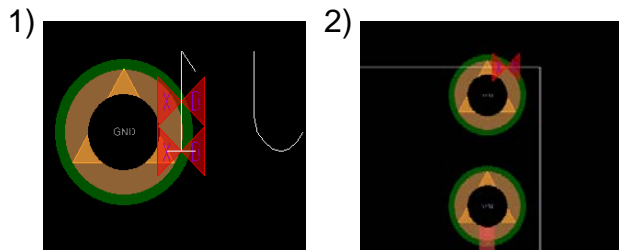
- 1) Silk text to pad spacing
- 2) Silk text to exposed pad spacing
- 3) Silk line to pad spacing
- 4) Silk line to exposed pad spacing
- 5) Silk text height
- 6) Silkscreen lone line minimum length



Etch Analysis Rules

- 1) Pad to Board Outline Spacing
- 2) Single pin nets
- 3) SMD pad entry
- 4) Etch trace to Board Outline Spacing

Sample of Starter Rules



Testability Checks

- 1) Silk text to testpoint pad spacing
- 2) Silk line to testpoint pad spacing
- 3) Testpoint pad to Board Outline spacing
- 4) Testpoint pad with no soldermask

Outline Checks

- 1) Duplicate outlines
- 2) Outline with width > 0
- 3) Outline made of multiple line segments
- 4) Shapes on Outline layer with overlapping clines

Summary

- Directly integrated in Allegro
- Starter rules are ready
- User-definable / customizable
- Ravel is Object-oriented , faster than SKILL
- Standard check items & flow

Thanks !!!