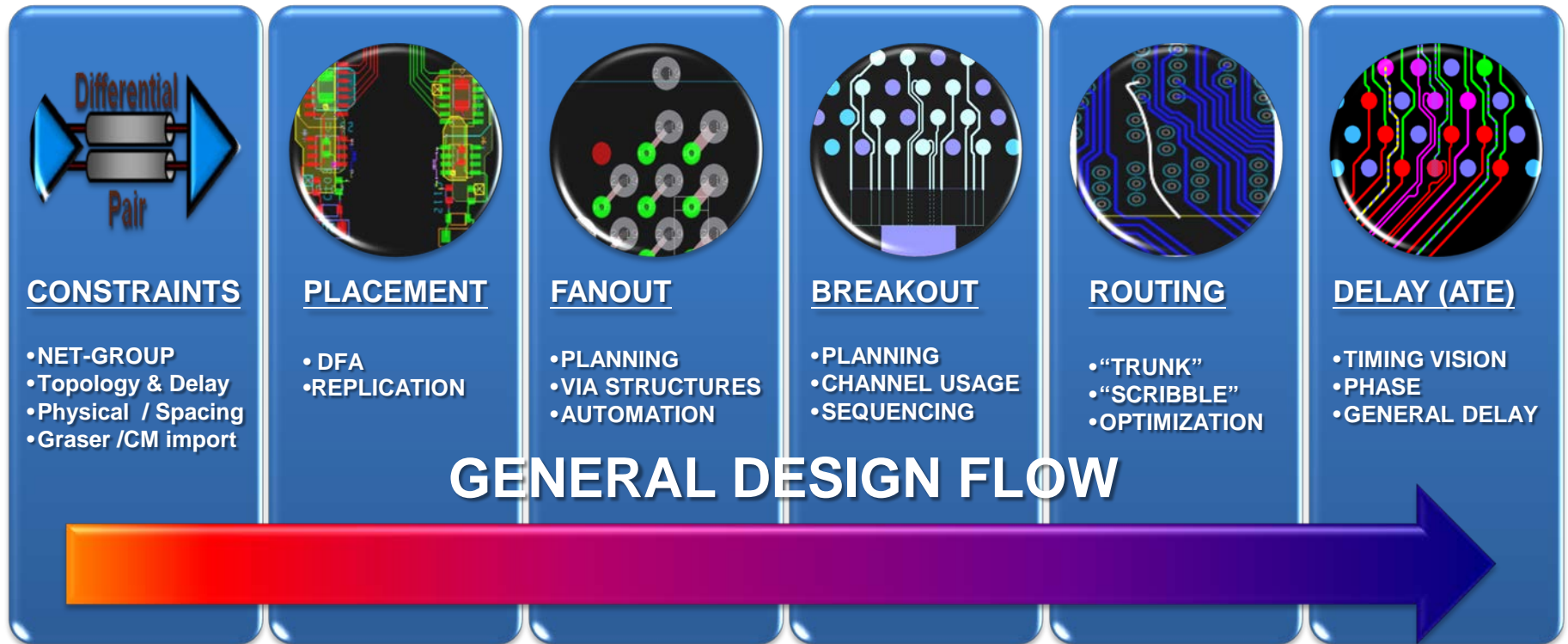


# Increase Productivity and Quality by New Layout Flow

*Jonathan / Graser*

*16 / Oct / 2015*

# Design Process Introduction



# Productivity Enhancements

---

- Constraints
  - Graser / CM import
- Routing
  - Auto Connect
  - Create Flow
  - Compress Route
  - Auto-Routing Enhancements / Flow Routing Adherence
  - Auto-Interactive Adjust Spacing
  - Trim to Breakout
  - Delete Breakout
  - Add Differential Pair Return Path Vias During Add Connect
  - Fiber Weave Off - Angle Routing
  - Integrate Snake Router into Add Connect Now
- Delay
  - Allegro TimingVision Environment

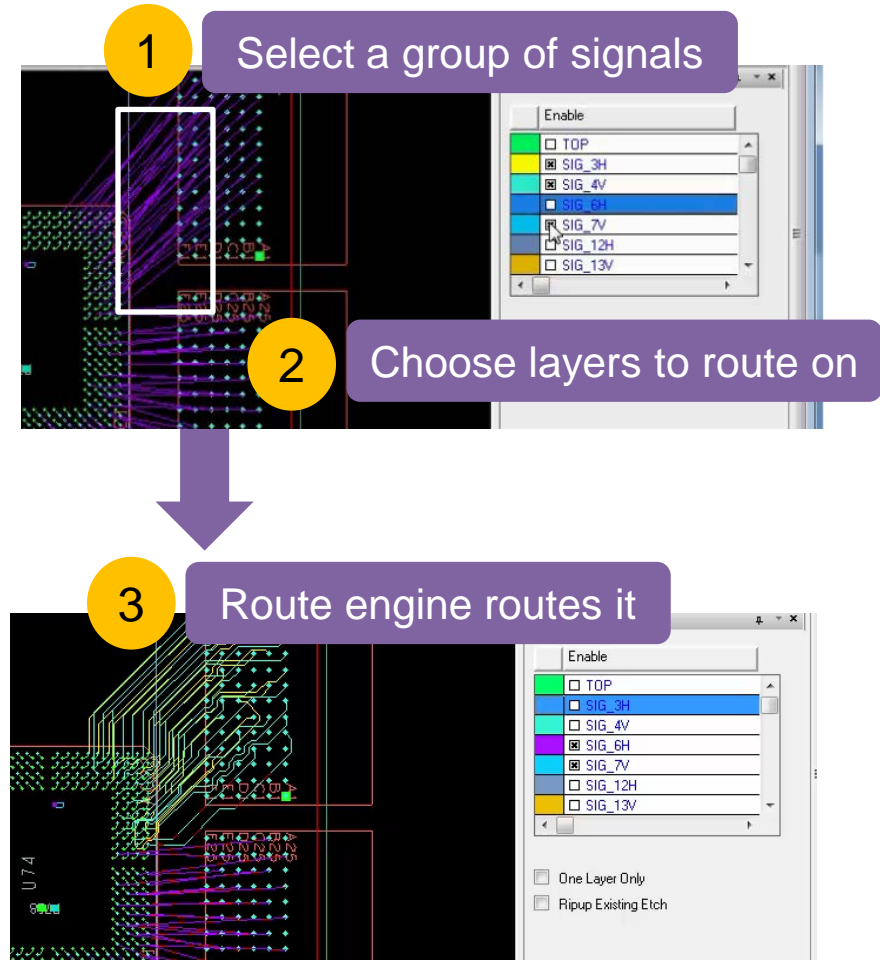




# Auto Connect

## Direct to etch auto-routing

- Fast routing of selected set of signals
  - No planning required
- Out of the box technology leverage underlying route engine
- User selects rats, adjusts layer settings and system routes it
- Results are very similar to “hand routed” efforts but in a fraction of time
- Rip up and retry option

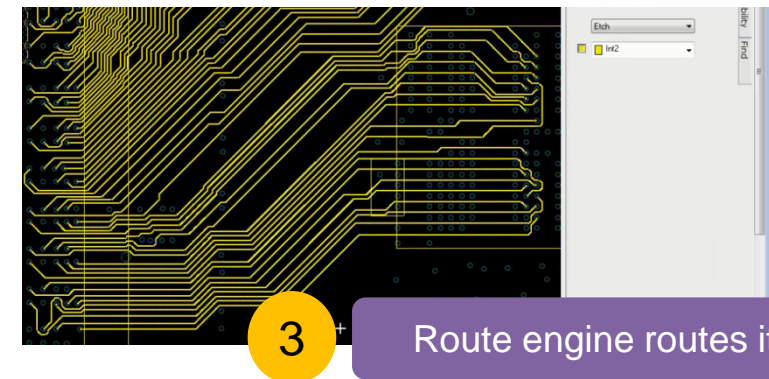
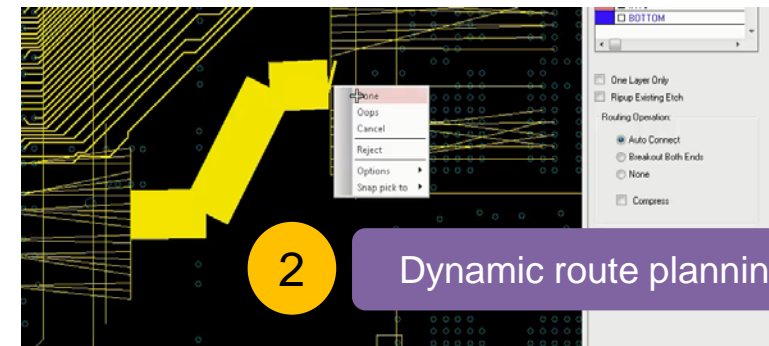


(Design Planning Option)

# Create Flow

## Dynamic flow creation with routing

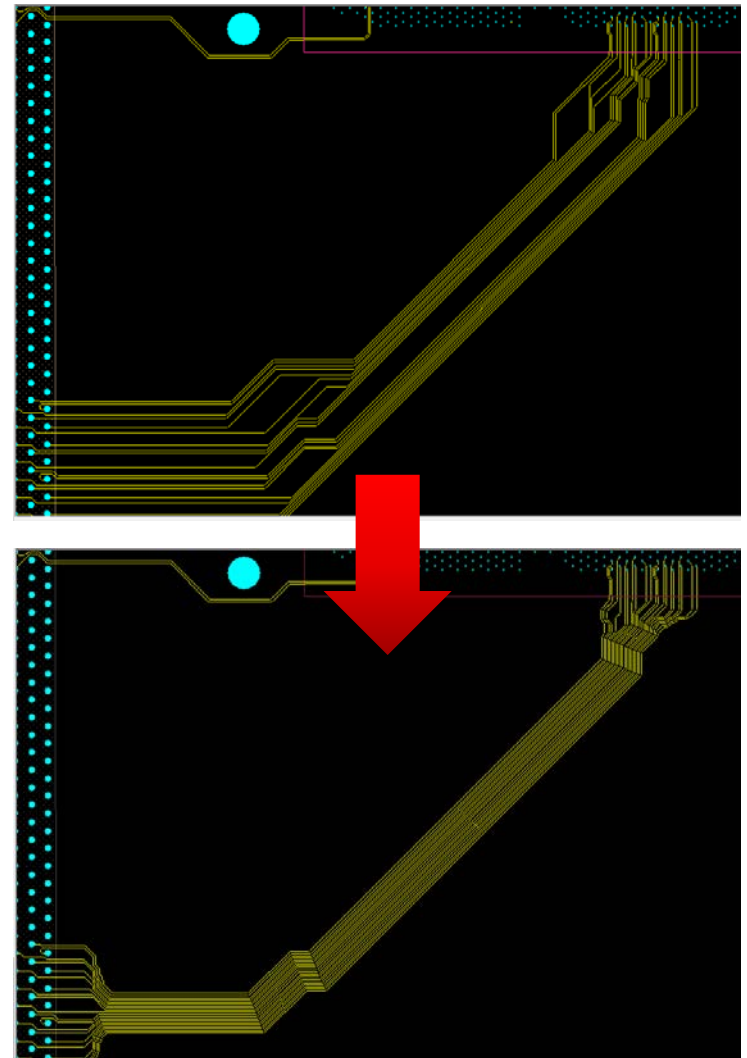
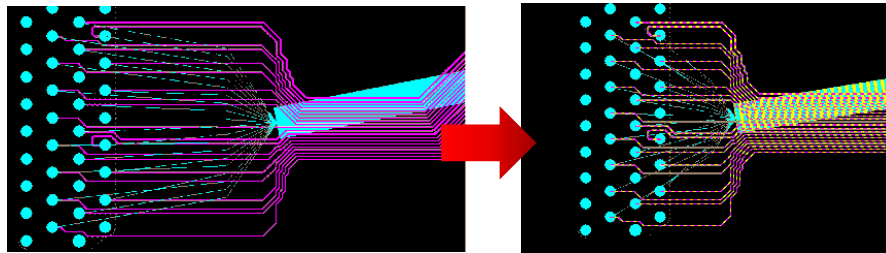
- Fast routing with route intent preserved
  - Rerouting signals is easy with changing layers if necessary
  - Route intent is reused in future revisions
- User selects a group of signals
- System creates the bundle dynamically
- User continues defining route plan / path to guide route engine
- Route engine routes it by using Auto connect
- Option to route in sections
  - Breakout
  - Trunk



# Compress Route

## User controlled compression

- Compress routing to MIN DRC Gap
- Compress routes are attached to a bundle
- User can control compression area
- Location of bundle end point controls the compression around break out
- Faster clean up

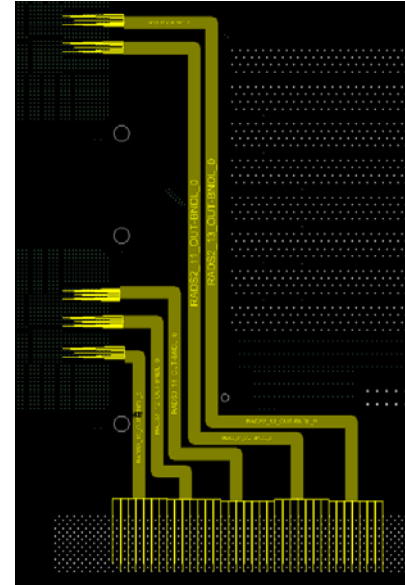


(Design Planning Option)

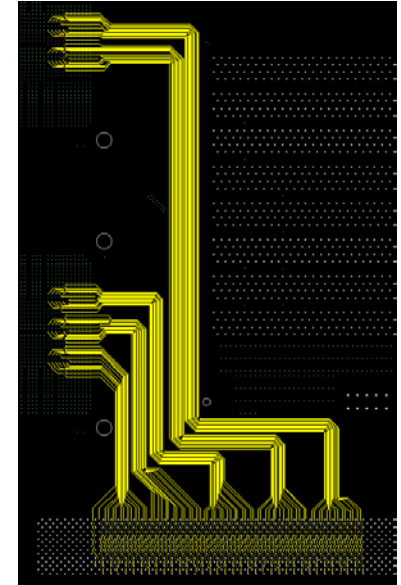
# Auto-Routing Enhancements

## Flow Routing Adherence

- Auto-router will follow bundle path more “strictly”
  - User draws flow path for each net group
  - Auto - Breakout both ends of bundle ( AiBT )
- Generate route results that match hand routing



Flow Bundles

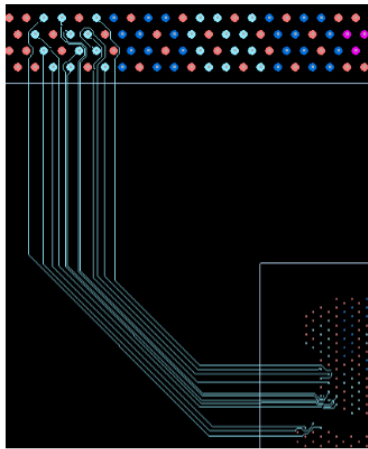


Router Results

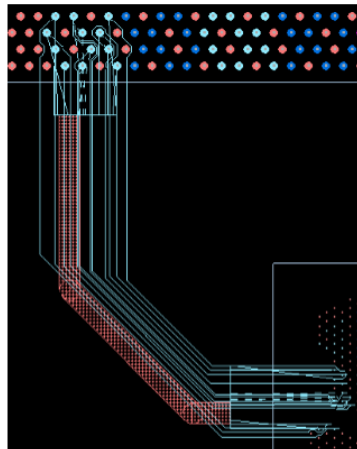
**(Design Planning Option)**

# Auto-Interactive Adjust Spacing

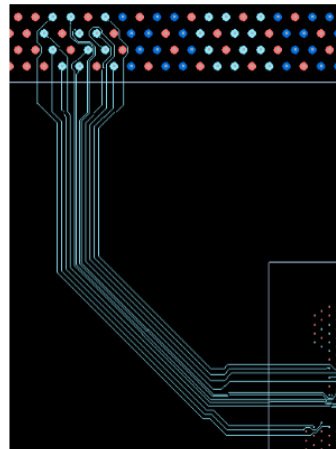
- Allow users to compress / expand line to line spacing within signal group
- Use RMB on bundle → Adjust Spacing
  - Enter spacing ( constraint or user value )
- Adjust spacing for tuning or plan other routes



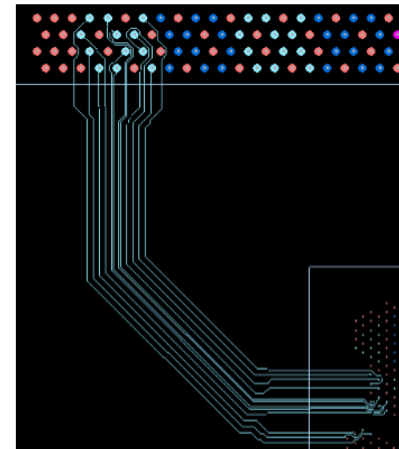
Initial Routes



Display Flow Bundle



Adjust Spacing to  
Min Constraint



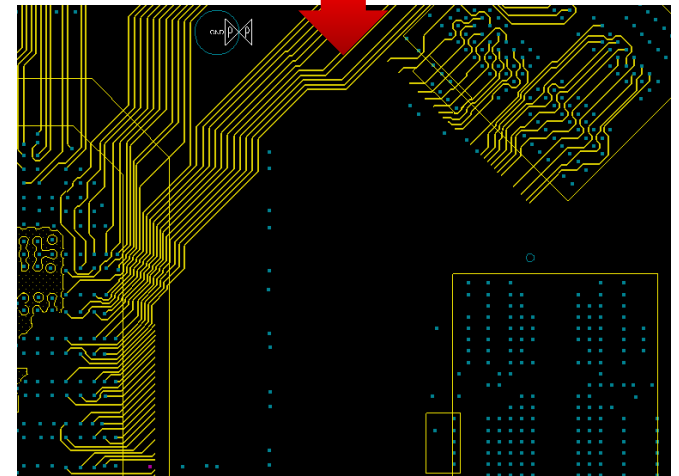
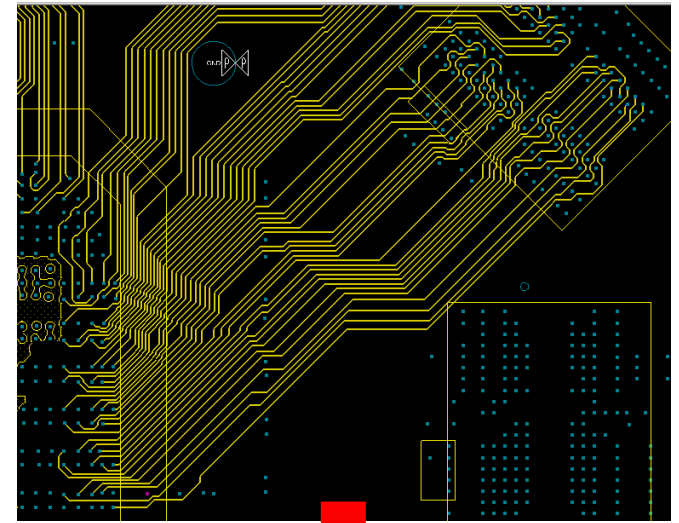
Increased Line  
to Line Spacing

**(Design Planning Option)**

# Trim to Breakout / Delete Breakout

## Multi-stage routing / changes

- Trim to Breakout
  - Removes trunk of routed bus
  - Trims or extends dangling etch
  - Bundle defines cut line
- Delete Breakout
  - Deletes breakout etch on the selected side of bundle
- Work with groups of signals
- Handle breakout / component changes



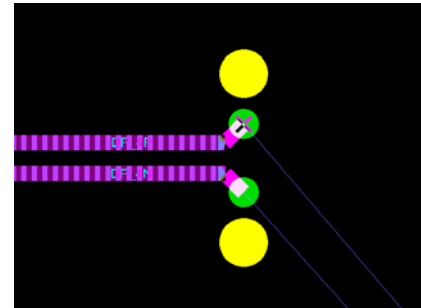
(Design Planning Option)



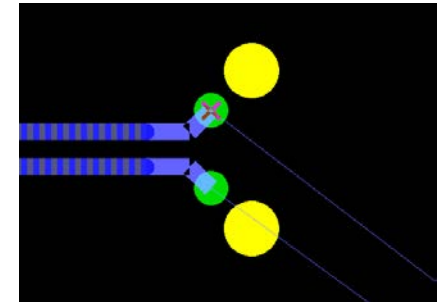
# Add Differential Pair Return Path Vias

## During Add Connect

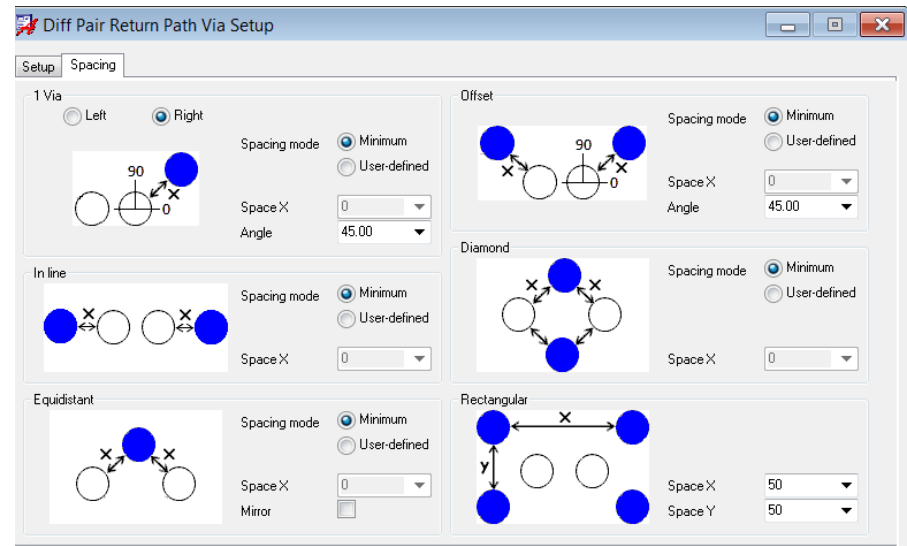
- Choose 1 of 6 pre-defined configurations when routing Diff Pairs
  - Single shared via
  - In line
  - Equidistant
  - Offset
  - Diamond
  - Rectangular
- User selectable
  - Assignment of netname ( GND etc )
  - Padstack or via structure



In Line



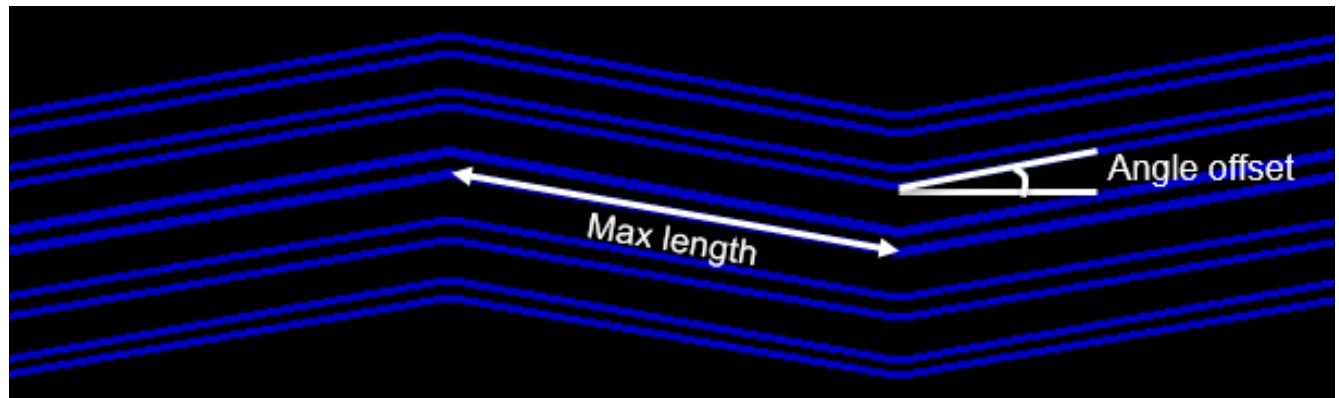
Offset



(High-Speed Option)

# Fiber Weave Off – Angle Routing

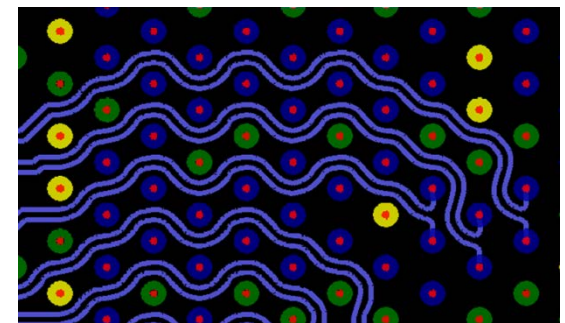
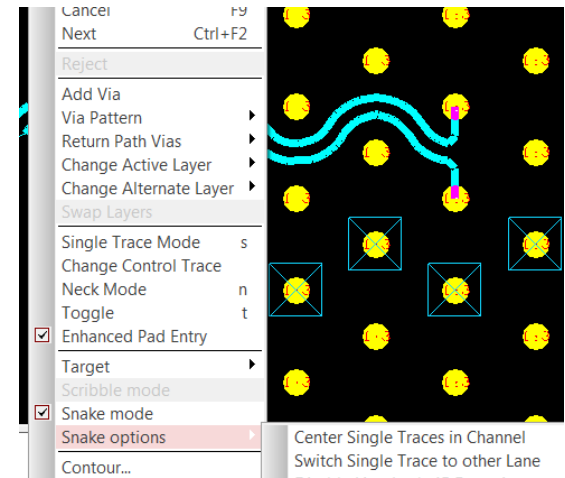
- Change a group of parallel segments to a Zig-Zag pattern
- Support for Diff Pairs and Single Ended Nets
- Convert full segments or user defined start/end points
- Options
  - Angle offset ( defaults to 10 degrees )
  - Max Length of legs ( user entry )



**(High-Speed Option)**

# Integrate Snake Router into Add Connect Now

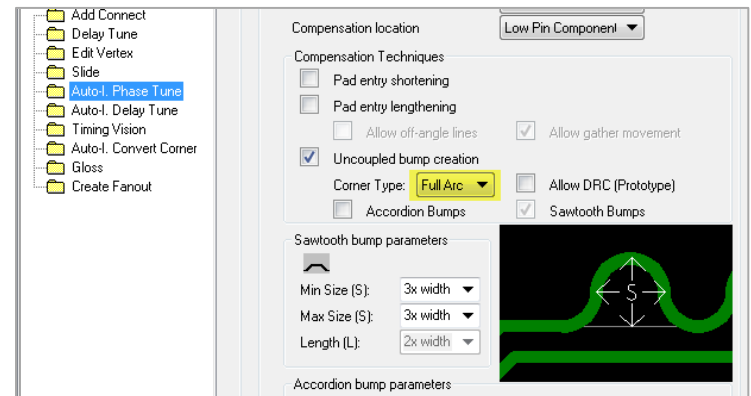
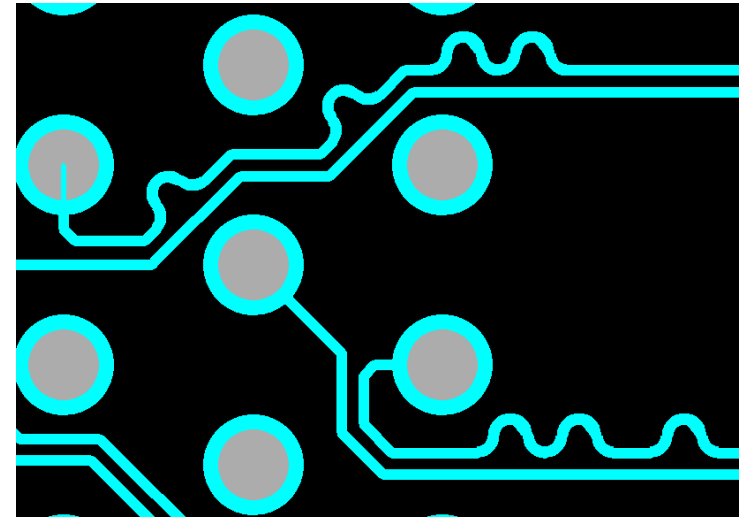
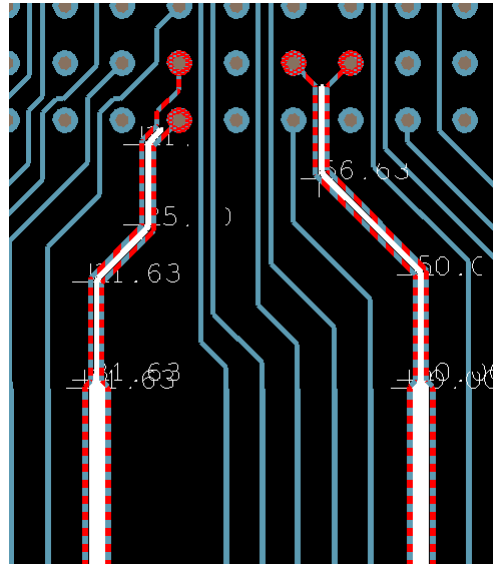
- User doesn't have to enter line width and gap any more
- Resume snake routing from partially routed path
- Natural line angle transition when routing into open space
- Single line centering option



Snake Routing

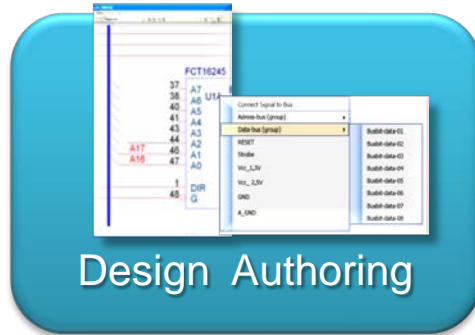
# Allegro TimingVision Environment

- AiPT : Arc phase bumps
- AiDT : Arc delay tuning bumps
- Timing Vision - Diff Pair dynamic phase support



**(High-Speed Option)**

# Design Productivity and Predictability with Interface – aware PCB Design



- Accelerate design intent creating with Interfaces
- Constraint interfaces

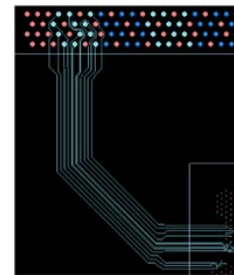
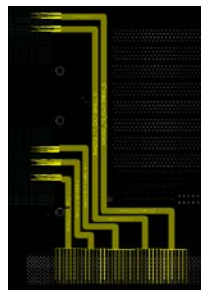
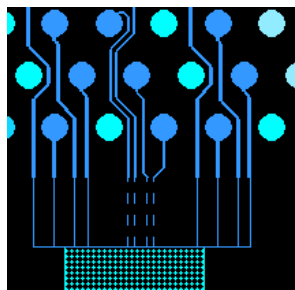
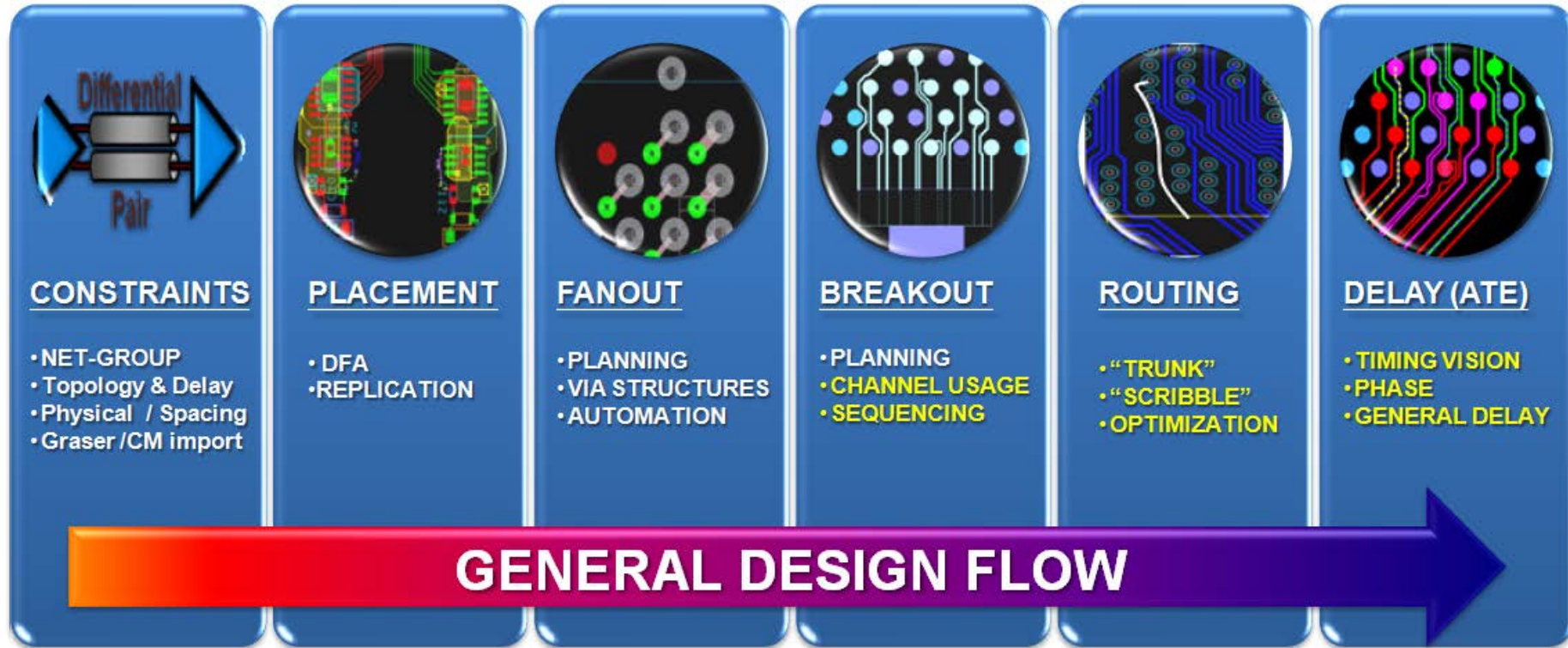


- Finalize critical component placement
- Route planning
- Perform Feasibility analysis



- Refine Route plan
- Auto-interactive Breakout Tuning
- Auto-interactive Trunk Routing
- Auto Connect
- Auto-Interactive Phase Tune
- Auto-Interactive Delay Tune

# Design Process ( Outsourcing )



**Increase  
Productivity and  
Quality!**

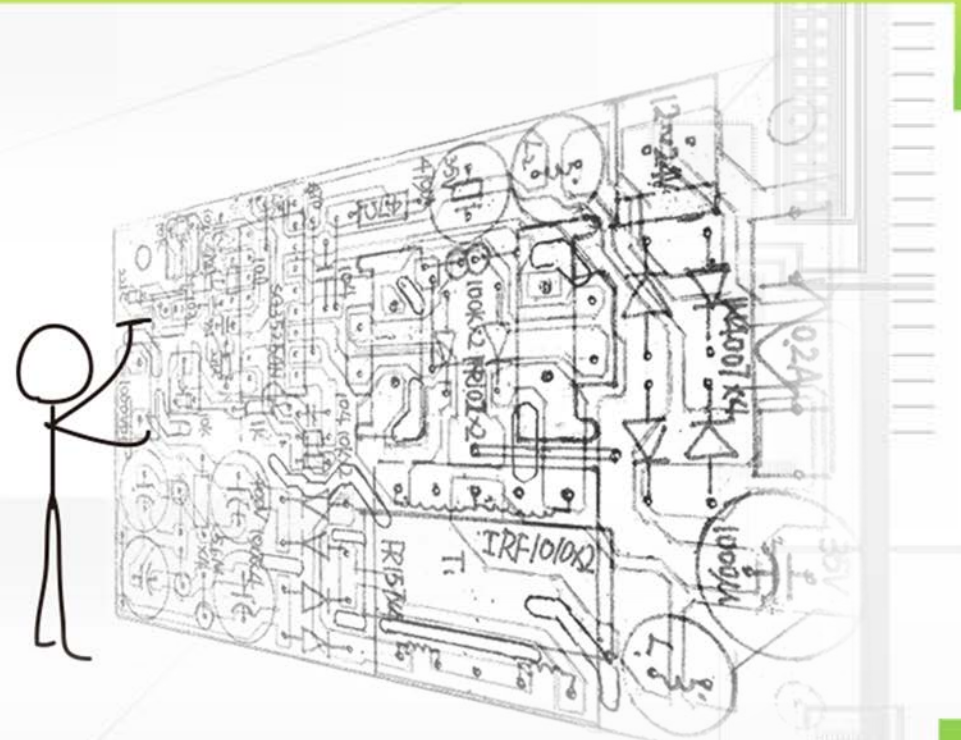


# PAL-PILOT

## Experience Sharing

未來の進行式

INTEGRITY, QUALITY, SPEED



# PCB Design for maximum productivity

Edward Lai & Jason Jiang

16/Oct/2015

# Agenda

- PCB Estimate in Allegro
- Allegro 16.6 Enhancement
- Experience Sharing
- Improve Productivity
- Improve Quality

# PCB Estimate in Allegro

- **主要目標**

減少Layout與EE間的評估時間，加速專案開發。

- **使用功能**

Net Group

Bundle Operation

# Create Net Group

The screenshot illustrates the process of creating a net group in a PCB design tool. It shows the 'Physical' properties panel, the 'Objects' table, and the 'Create NetGroup' dialog box.

**Physical Properties Panel:**

- Physical
- Spacing
- Same Net Spacing
- Properties
- Net
  - Electrical Properties
  - General Properties
  - Ratsnest Bundle Properties
- Component
  - Component Properties
  - Pin Properties

**Objects Table:**

Type	S	Name	Layer Matching	Max Transition Count	Tuning Pattern
MGrp		M_B_CLK (4)			
MGrp		M_B_DQS_CLK (20)			
NGrp		DDR8 (2)			
NGrp		DDR8_ADD-CMD-CTL-CLK (3)			
NGrp		DDR8_ADDCMD (1)			
NGrp		DDR8_CLK (1)			
NGrp		DDR8_CTL (1)			
NGrp		DDR8_DATA (8)			
NGrp		DDR8_DATA0 (1)			
NGrp		DDR8_DATA1 (1)			
NGrp		DDR8_DATA2 (1)			
NGrp		DDR8_DATA3 (1)			
NGrp		DDR8_DATA4 (1)			
NGrp		DDR8_DATA5 (1)			
NGrp		DDR8_DATA6 (1)			
NGrp		DDR8_DATA7 (1)			
Bus		MBD7 (11)			
Bus		AUDIO (15)			
Bus		CARD (15)			
Bus		CCD (2)			
Bus		CPU (28)			
Bus		EDP (20)			
Bus		GPUPOWER (5)			
Bus		HDMI0 (32)			
Bus		HDMI1 (2)			
Bus		HP (21)			
Bus		LAN (16)			
Bus		LPC (18)			
Bus		MAA (20)			
Bus		MAC (10)			
Bus		MAD0 (10)			
Bus		MAD1 (10)			
Bus		MAD2 (10)			
Bus		MAD3 (10)			
Bus		MAD4 (10)			
Bus		MAD5 (10)			
Bus		MAD6 (10)			
Bus		MAD7 (10)			
Bus		MCLKA (4)			
Bus		OTHER (14)			

**Create NetGroup Dialog:**

NetGroup: DDRB\_D7

Selections:

Name	Type	NetGroup
MBD7	Bus	DDR8_D...

**Context Menu:**

- Analyze
- Select
- Select and Show Element
- Deselect
- Find... (Ctrl+F)
- Bookmark...
- Expand (Num +)
- Expand All
- Collapse (Num -)
- Create**
- Add to...
  - Match Group...
  - Ratsnest Bundle...
  - Net Group...**
  - Pin Pair...
  - Differential Pair...
- Bus members...
- Remove
- Rename... (F2)
- Delete
- Compare...

# Create Net Group

階層如下：

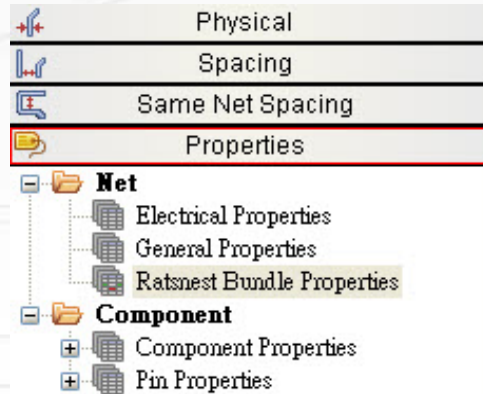
Net Group



Net Group



RBnd



Objects		
Type	S	Name
NGrp	*	<input type="checkbox"/> DDRB (2)
NGrp		<input type="checkbox"/> DDRB_ADD-CMD-CTL-CLK (3)
NGrp		<input type="checkbox"/> DDRB_ADDCMD (1)
NGrp		<input type="checkbox"/> DDRB_CLK (1)
NGrp		<input type="checkbox"/> DDRB_CTL (1)
NGrp		<input type="checkbox"/> DDRB_DATA (8)
NGrp		<input type="checkbox"/> DDRB_DATA0 (1)
NGrp		<input type="checkbox"/> DDRB_DATA1 (1)
NGrp		<input type="checkbox"/> DDRB_DATA2 (1)
NGrp		<input type="checkbox"/> DDRB_DATA3 (1)
NGrp		<input type="checkbox"/> DDRB_DATA4 (1)
NGrp		<input type="checkbox"/> DDRB_DATA5 (1)
NGrp		<input type="checkbox"/> DDRB_DATA6 (1)
NGrp		<input type="checkbox"/> DDRB_DATA7 (11)
RBnd	N	<input checked="" type="checkbox"/> DDRB_DATA7_B (10)
Net		<input type="checkbox"/> M_B_DQSN7
Net		<input type="checkbox"/> M_B_DQSP7
Net		<input type="checkbox"/> M_B_DQ56
Net		<input type="checkbox"/> M_B_DQ57
Net		<input type="checkbox"/> M_B_DQ58
Net		<input type="checkbox"/> M_B_DQ59
Net		<input type="checkbox"/> M_B_DQ60
Net		<input type="checkbox"/> M_B_DQ61
Net		<input type="checkbox"/> M_B_DQ62
Net		<input type="checkbox"/> M_B_DQ63



# Create Ratsnest Bundle

The screenshot shows the 'Objects' table with columns: Type, S, Name, Layer Matching, Max Transition Count, and Tuning Pattern. A context menu is open over the selected 'M\_B\_DQ63' net, with 'Create' and 'Ratsnest Bundle...' highlighted in red. The 'Ratsnest Bundle Properties' dialog is also visible at the bottom.

Type	S	Name	Layer Matching	Max Transition Count	Tuning Pattern
Net		M_B_DQSN7			
Net		M_B_DQSP7			
Net		M_B_DQ56			
Net		M_B_DQ57			
Net		M_B_DQ58			
Net		M_B_DQ59			
Net		M_B_DQ60			
Net		M_B_DQ61			
Net		M_B_DQ62			
Net		M_B_DQ63			
Bus		AUDIO (15)			
Bus		CARD (15)			
Bus		CCD (2)			
Bus		CPU (28)			
Bus		EDP (20)			
Bus		GPUPOWER (5)			
Bus		HDMI0 (32)			
Bus		HDMI1 (2)			
Bus		HP (21)			
Bus		LAN (16)			
Bus		LPC (18)			
Bus		MAA (20)			
Bus		MAC (10)			
Bus		MAD0 (10)			
Bus		MAD1 (10)			
Bus		MAD2 (10)			
Bus		MAD3 (10)			
Bus		MAD4 (10)			
Bus		MAD5 (10)			
Bus		MAD6 (10)			
Bus		MAD7 (10)			
Bus		MCLKA (4)			
Bus		OTHER (14)			
Bus		PCH (27)			
Bus		PCICLK (6)			
Bus		PCIE (36)			
Bus		PCIECLK (11)			
Bus		PEC1 (2)			
Bus		POWER (16)			
Bus		RST (13)			

◎直接選擇Net



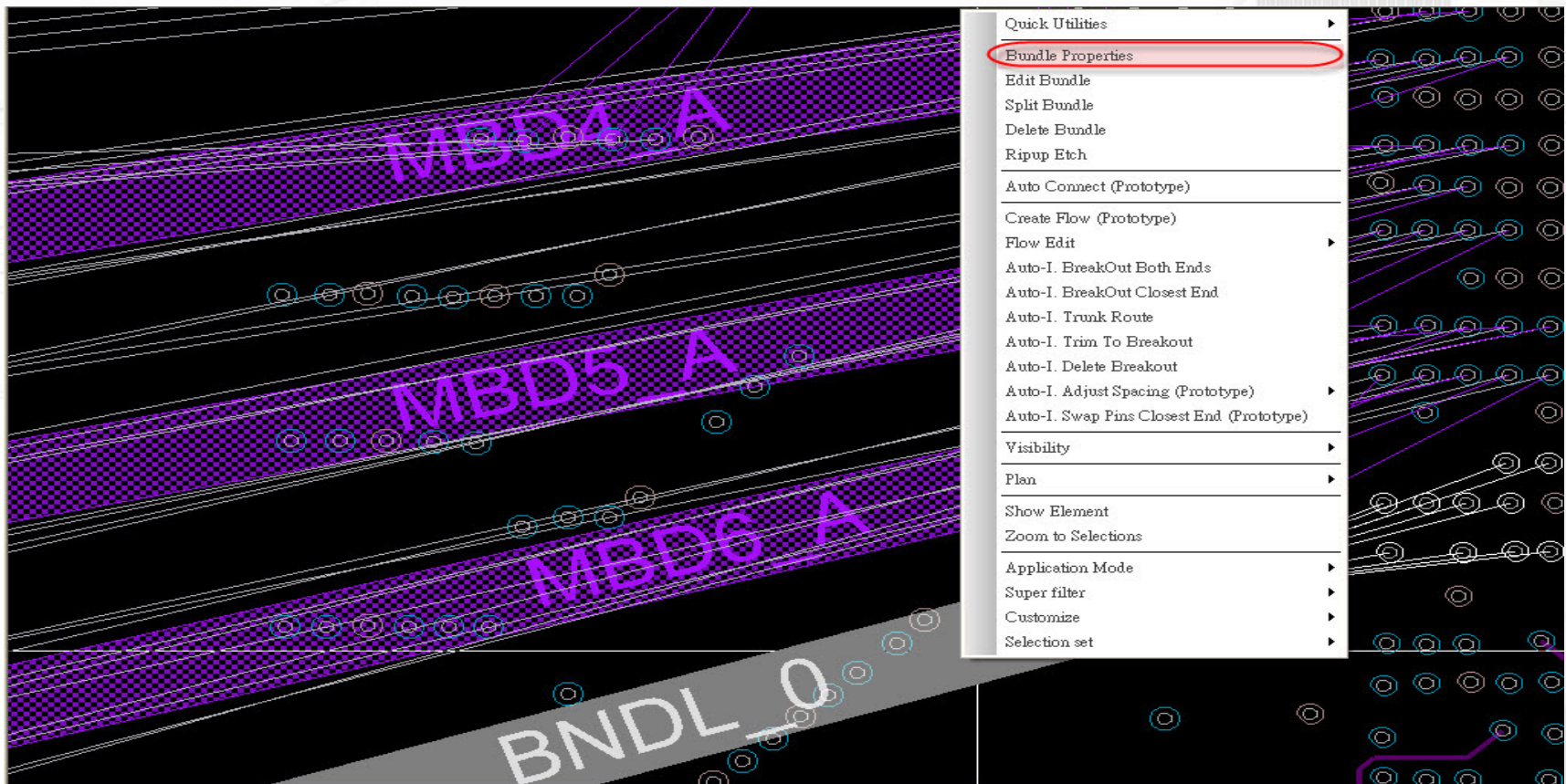
The dialog box 'Create Ratsnest Bundle' has a text field containing 'BNDL\_2'. Below it, a table lists the selected nets for the bundle.

Name	Type	Ratsnes...
JDIM2.237:U20.AP22 [...]	Ratsnest ...	MBD7_A
JDIM2.240:U20.AR22 [...]	Ratsnest ...	MBD7_A
JDIM2.242:U20.AR21 [...]	Ratsnest ...	MBD7_A
JDIM2.246:U20.AN21 [...]	Ratsnest ...	MBD7_A
U20.AN22:JDIM2.236 [...]	Ratsnest ...	MBD7_A
U20.AP21:JDIM2.250 [...]	Ratsnest ...	MBD7_A
U20.AT21:JDIM2.249 [...]	Ratsnest ...	MBD7_A
U20.AT22:JDIM2.233 [...]	Ratsnest ...	MBD7_A
U20.AU21:JDIM2.245 [...]	Ratsnest ...	MBD7_A
U20.AU22:JDIM2.232 [...]	Ratsnest ...	MBD7_A

Buttons: OK, Cancel, Help

# Bundle Properties

◎右鍵選單→Bundle Properties

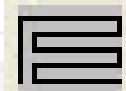


# Routing Controls

⊙ Allow in constraint area  
允許在constraint area處理

⊙ Tuning Pattern

Accordion

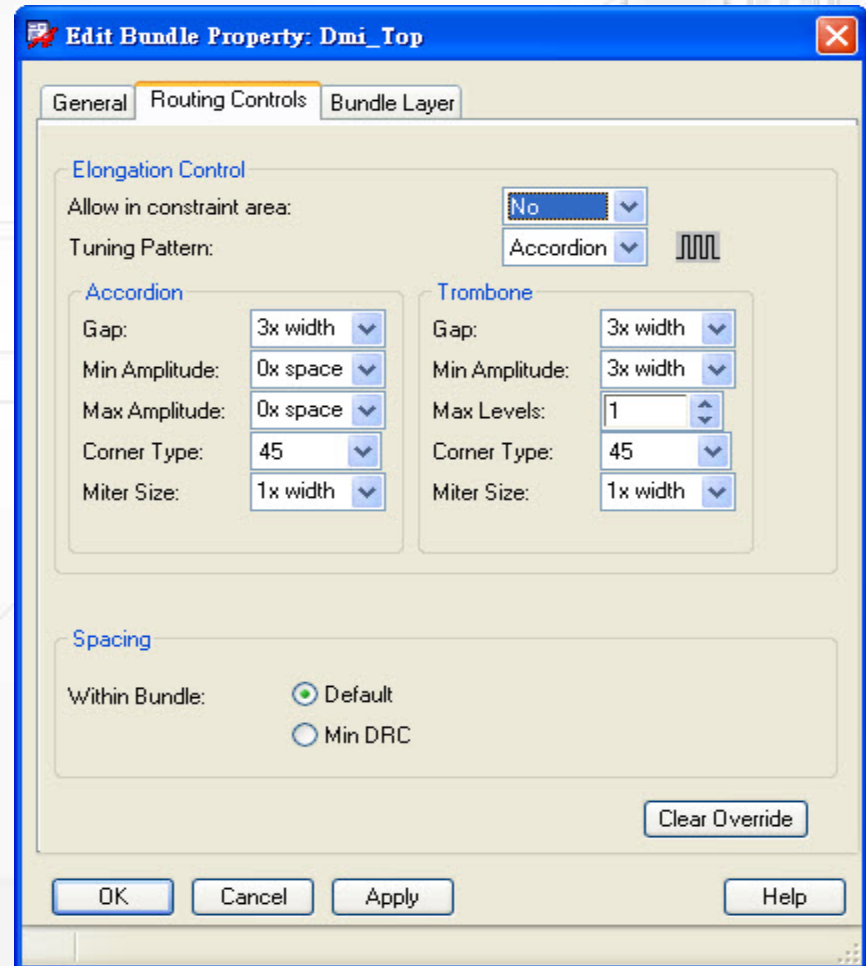


Trombone



⊙ Within Bundle

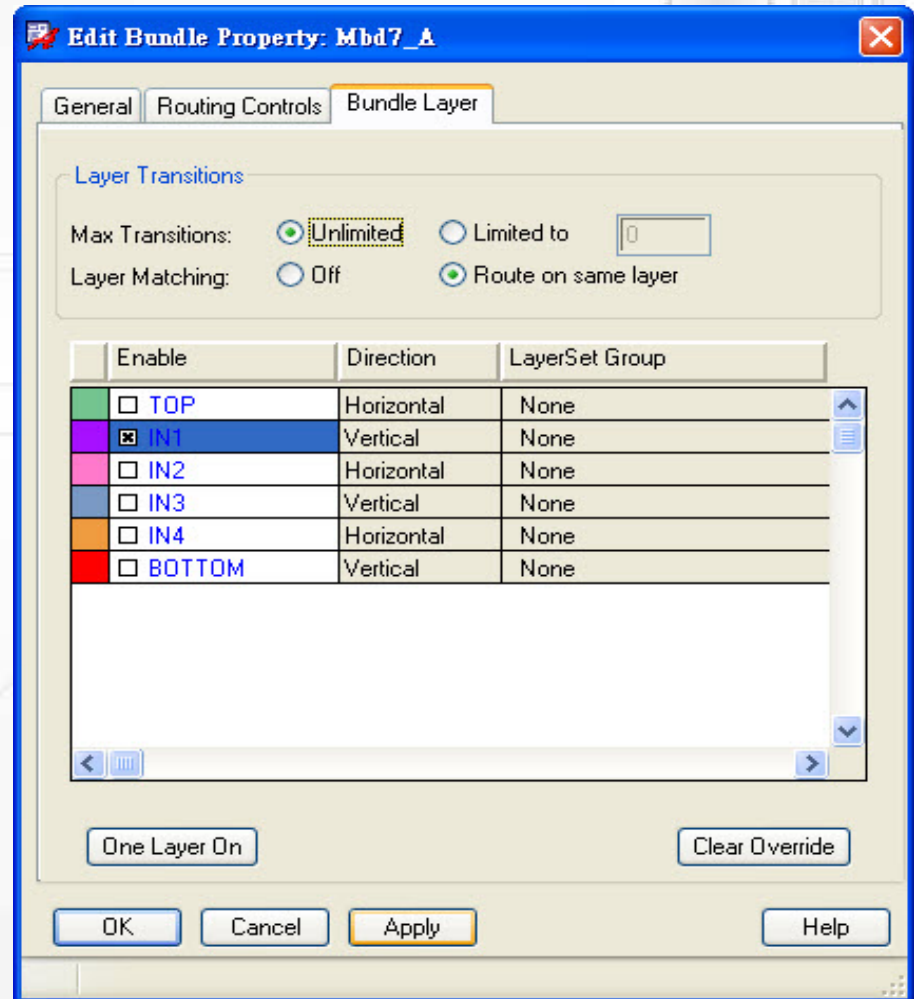
在Bundle內部spacing選項



# Bundle Layer

◎ One Layer On

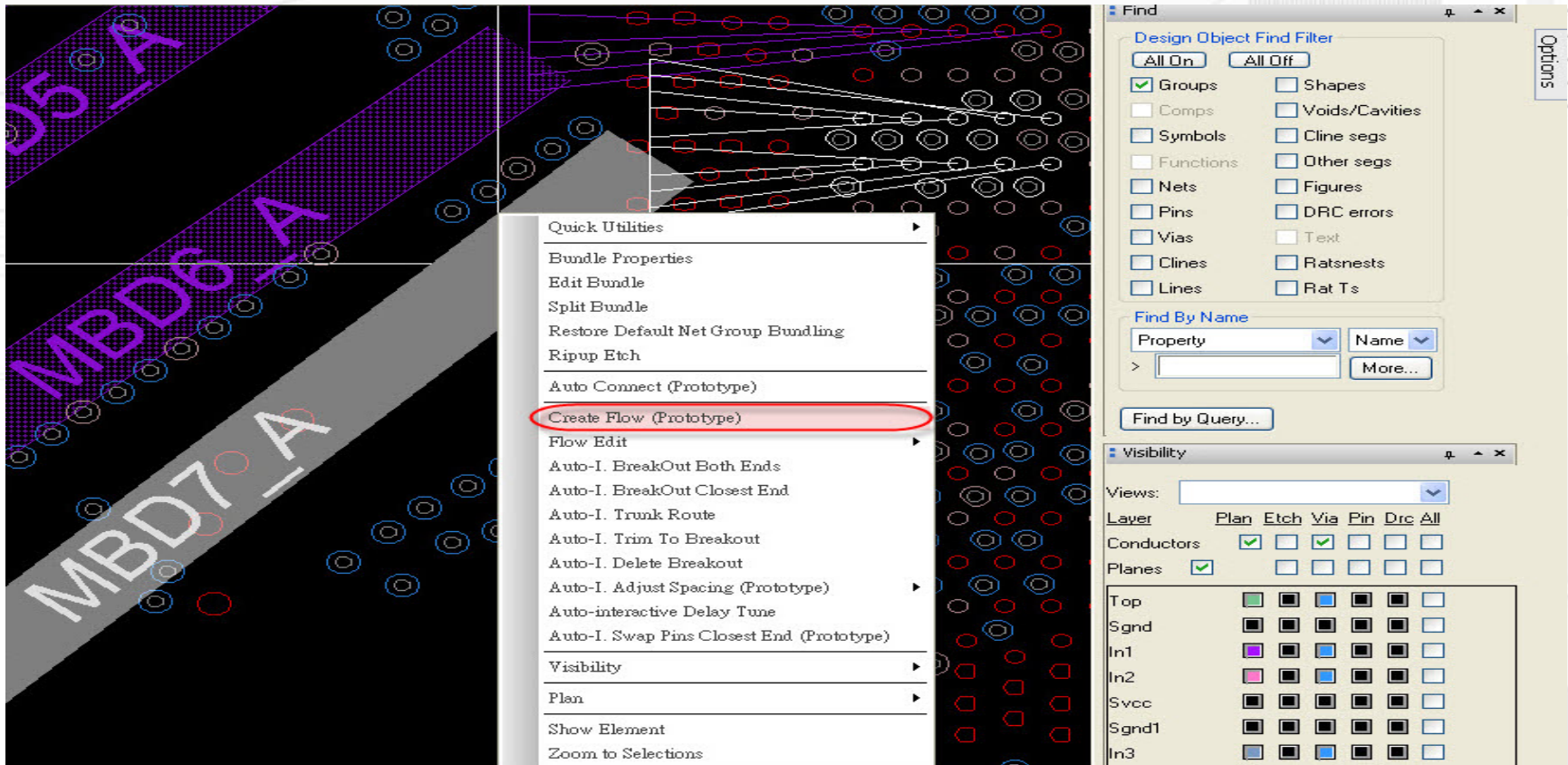
先點選再選擇層面





# Create Flow

◎點選後操作如一般走線



# Vertex Bundle

◎ Flow Planning → Other segs → 滑鼠左鍵長按

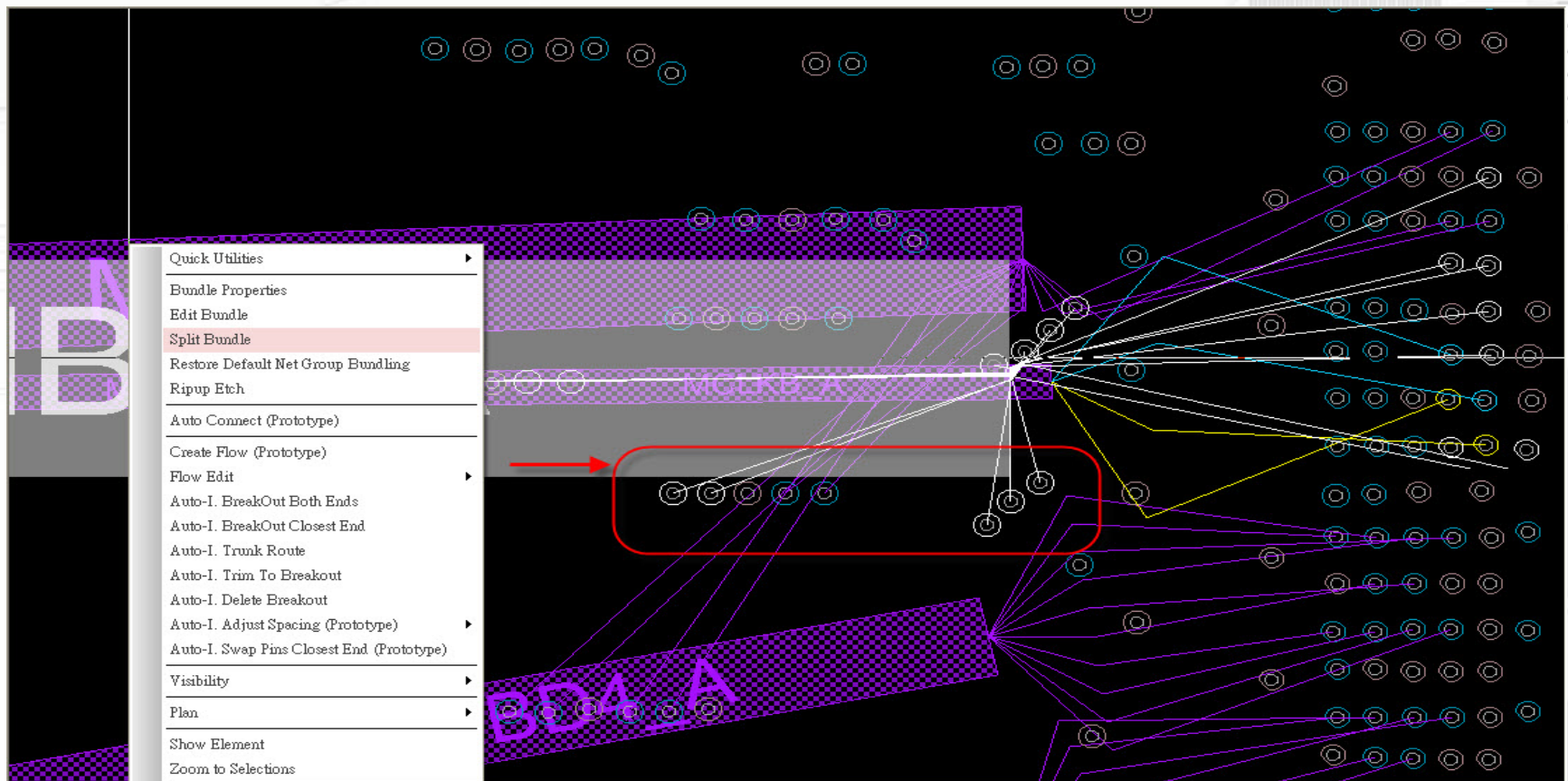
The screenshot displays a complex PCB layout with a vertex bundle. Several segments are highlighted in purple and labeled: MBD0\_A, MBD2\_A, MBA\_A, and MBD3\_A. A tooltip for 'Flow Segment MBD3\_A IN1 Cline' is visible. The 'Find' dialog box on the right has 'Other segs' checked under 'Design Object Find Filter'. The 'Visibility' panel shows various layers and their visibility status.

Layer	Plan	Etch	Via	Pin	Drc	All
Conductors	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Planes	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Top	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Sgnd	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
In1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
In2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Svcc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Sgnd1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
In3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
In4	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Sgnd2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bottom	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
All	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

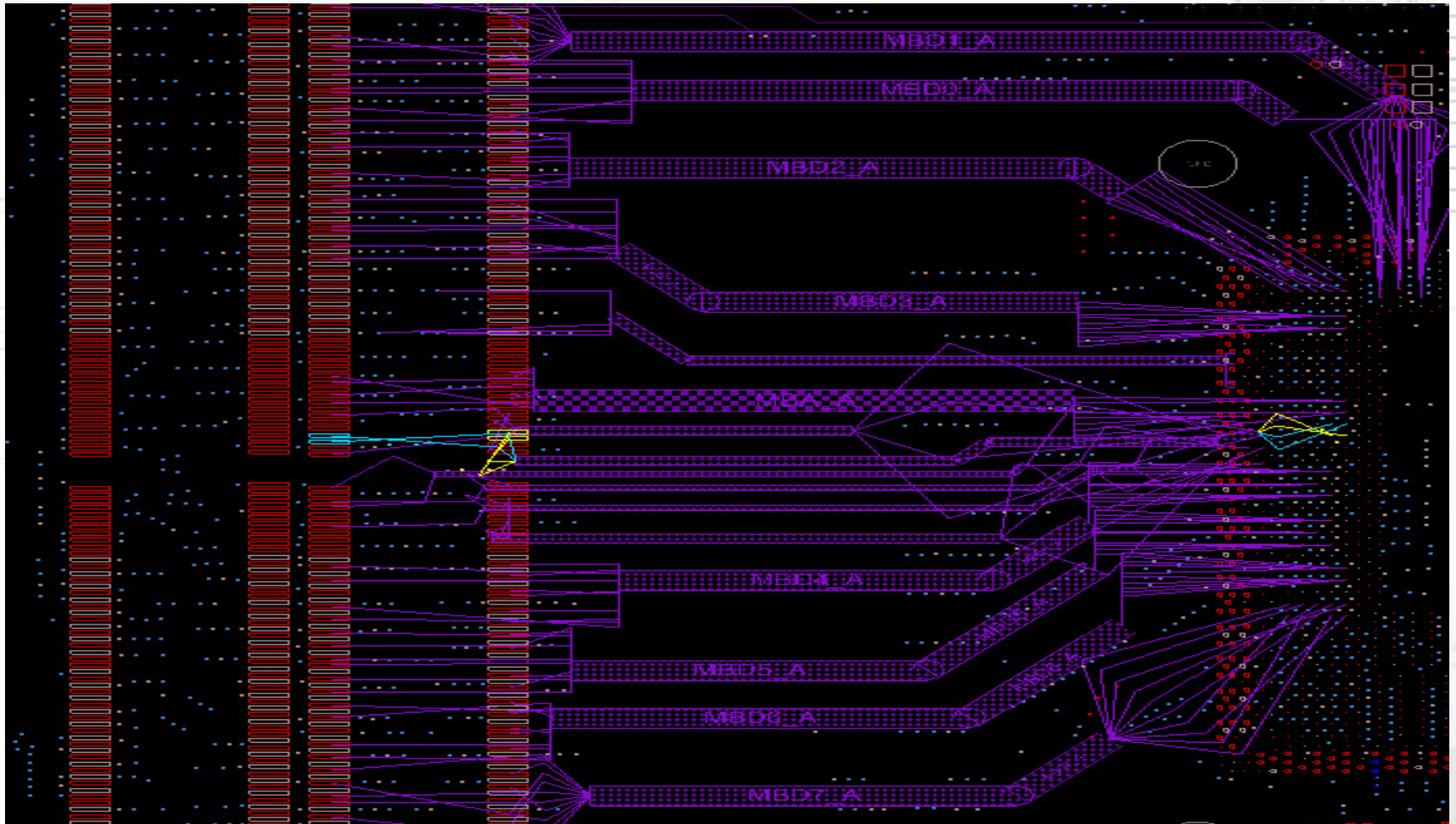


# Split Bundle

◎點選欲分離的信號



# Bundle Finish



# Allegro 16.6 Enhancement

- Auto Connect
- Flow Edit
- Auto-I. BreakOut Both Ends/ Closest End
- Auto-I. Trunk Route
- Auto-I. Adjust Spacing
- Auto-I. Delay Tune
- Auto-I. Phase Tune

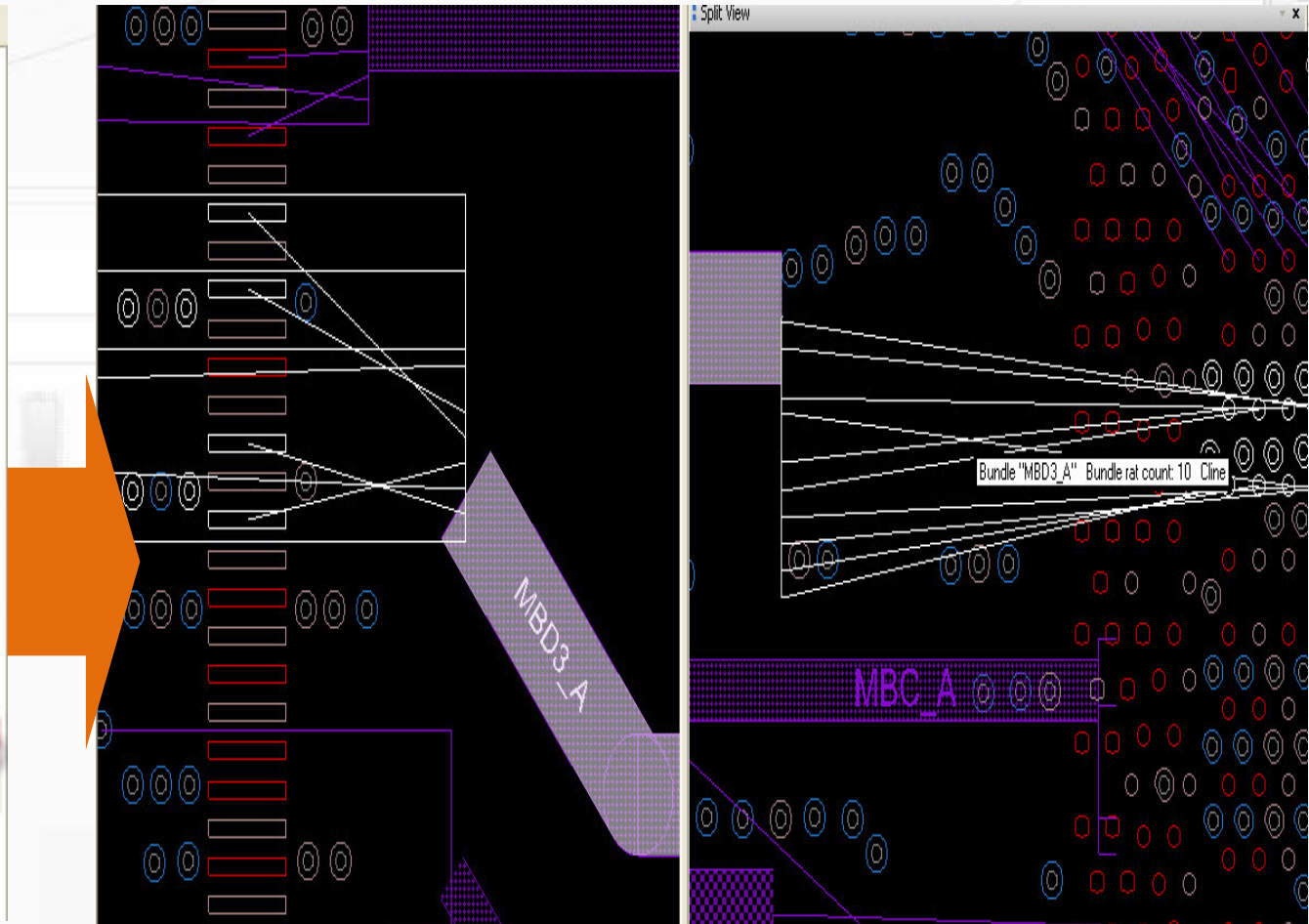
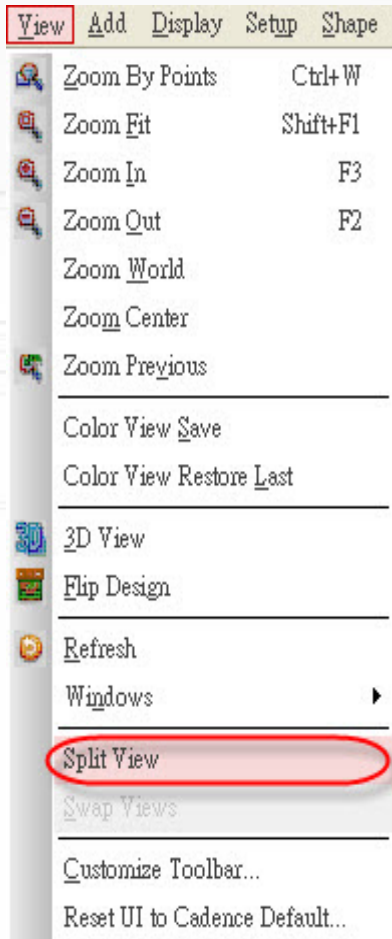


# Auto Connect-DDR

◎ 滑鼠右鍵 → Auto Connect

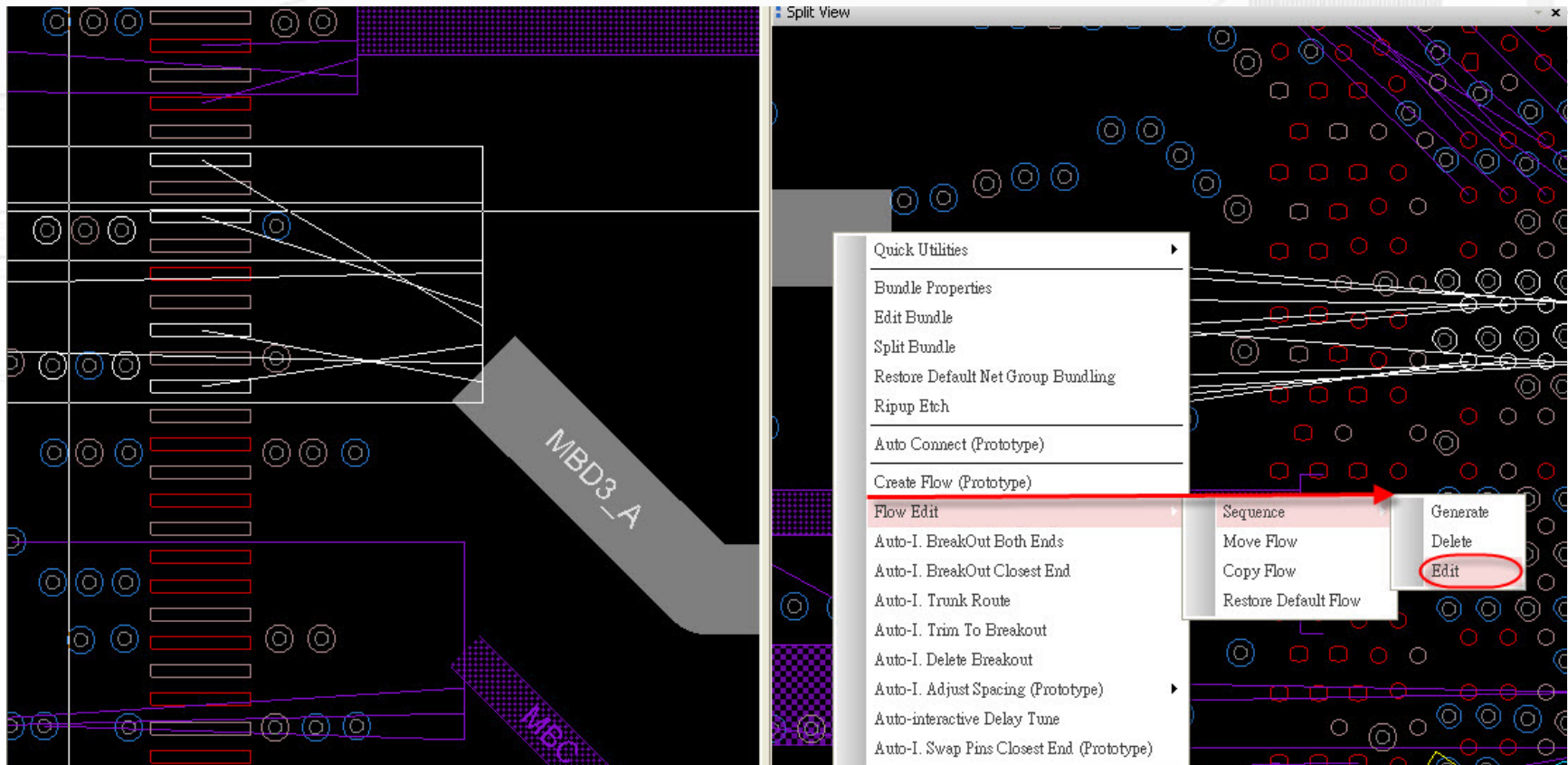


# Split View



# Flow Edit

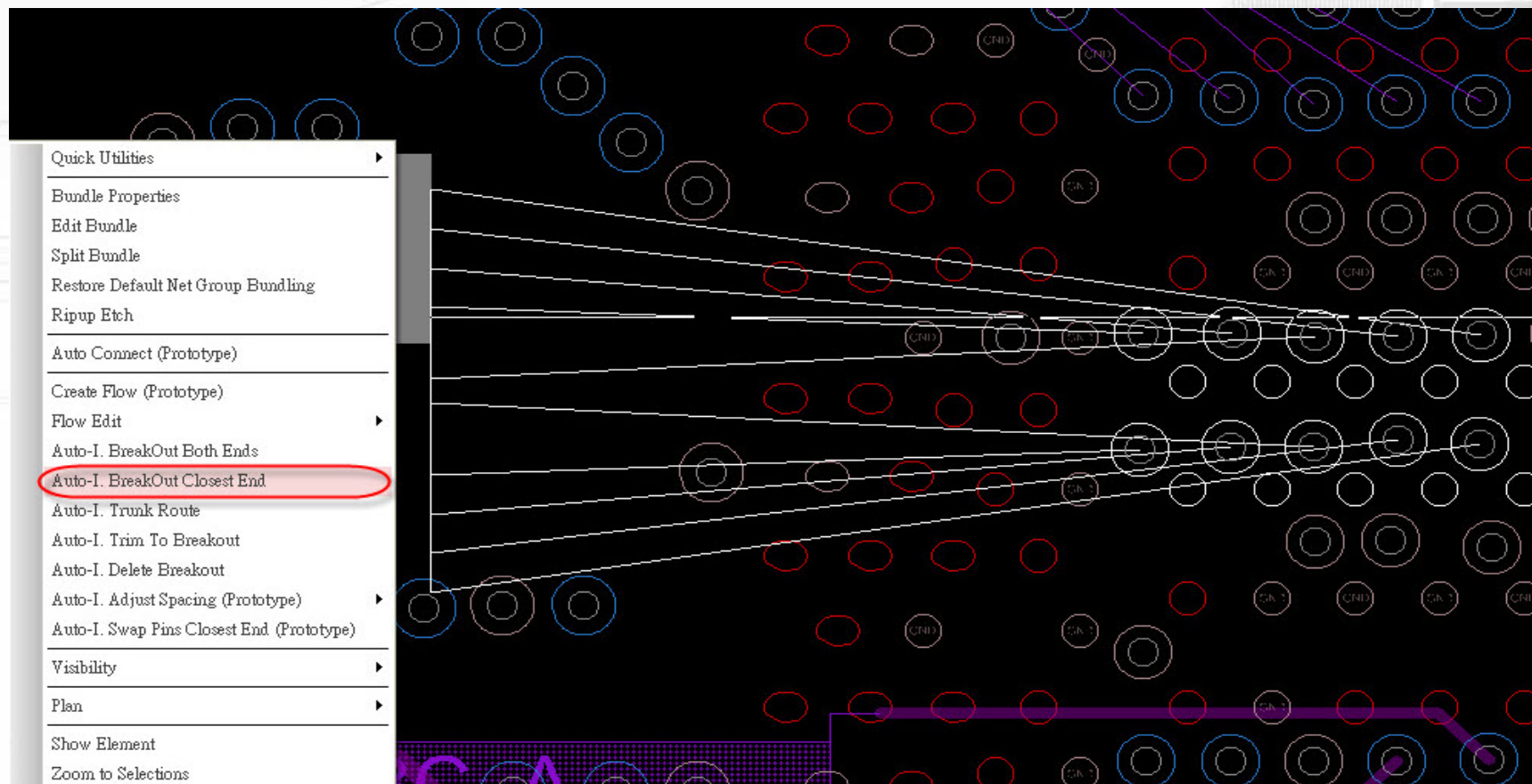
◎ 用於調整走線順序





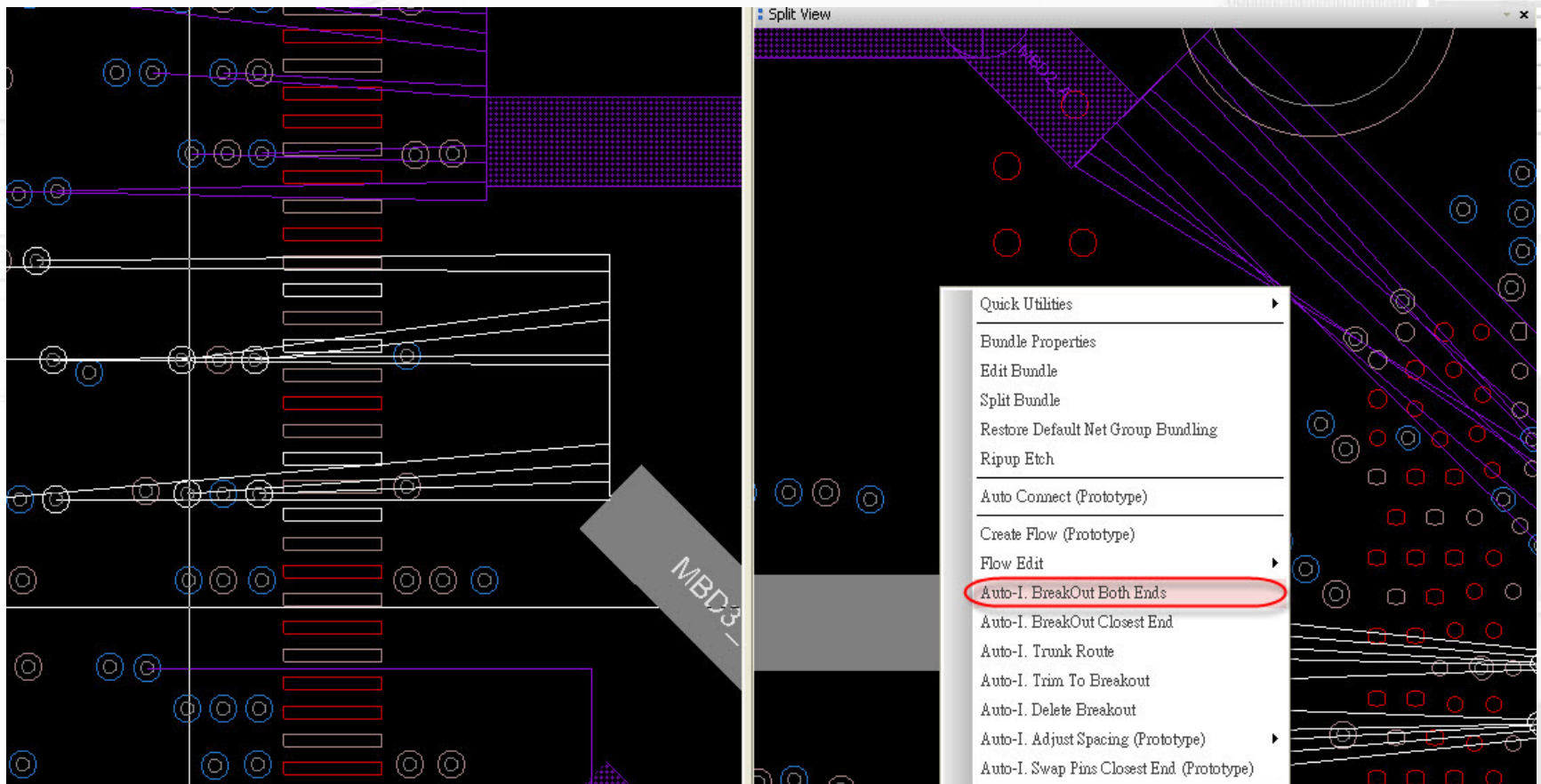
# Auto-I. BreakOut Closest End

◎ BreakOut接近點選處出Pin



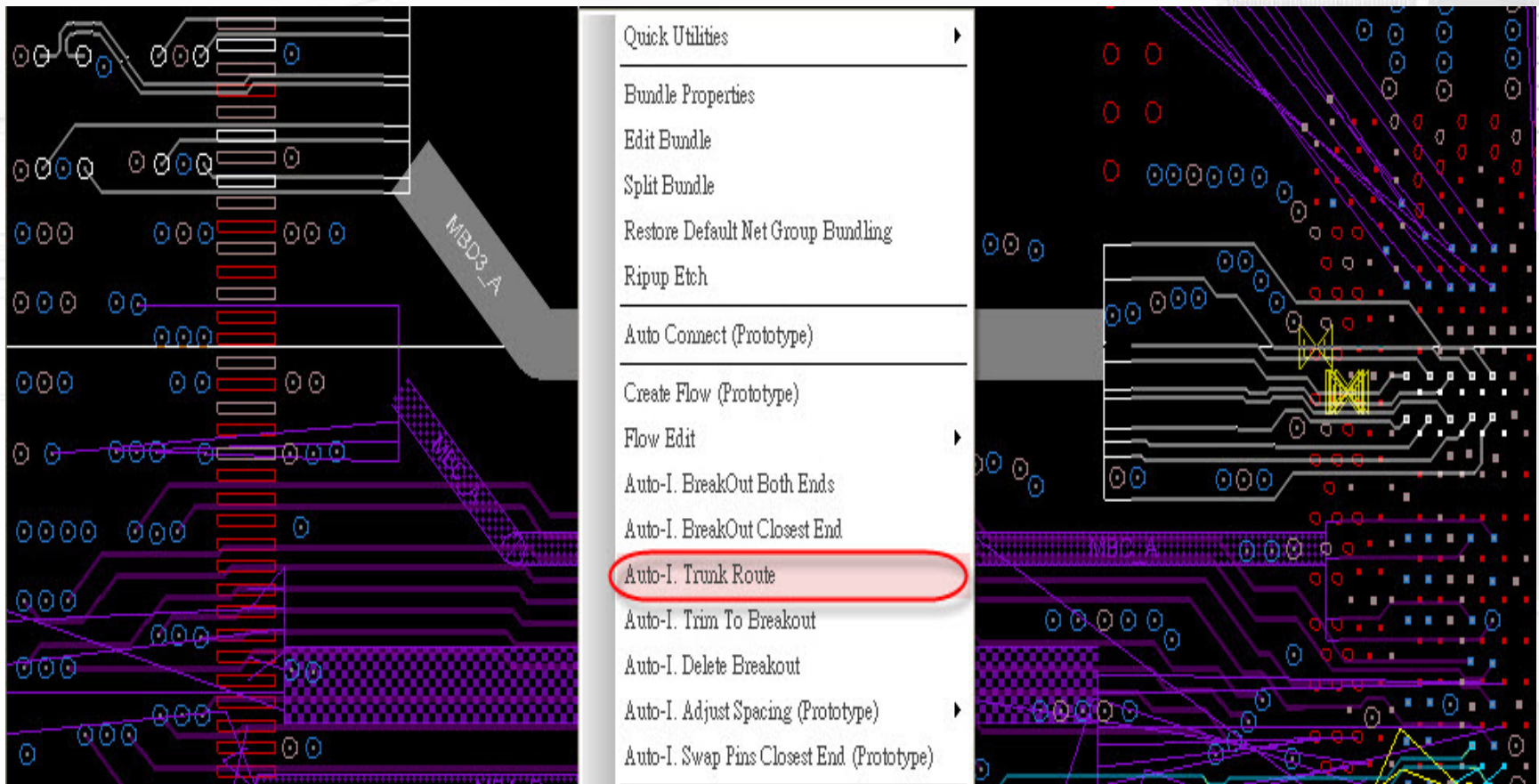
# Auto-I. BreakOut Both Ends

◎ BreakOut兩側同步出Pin



# Auto-I. Trunk Route

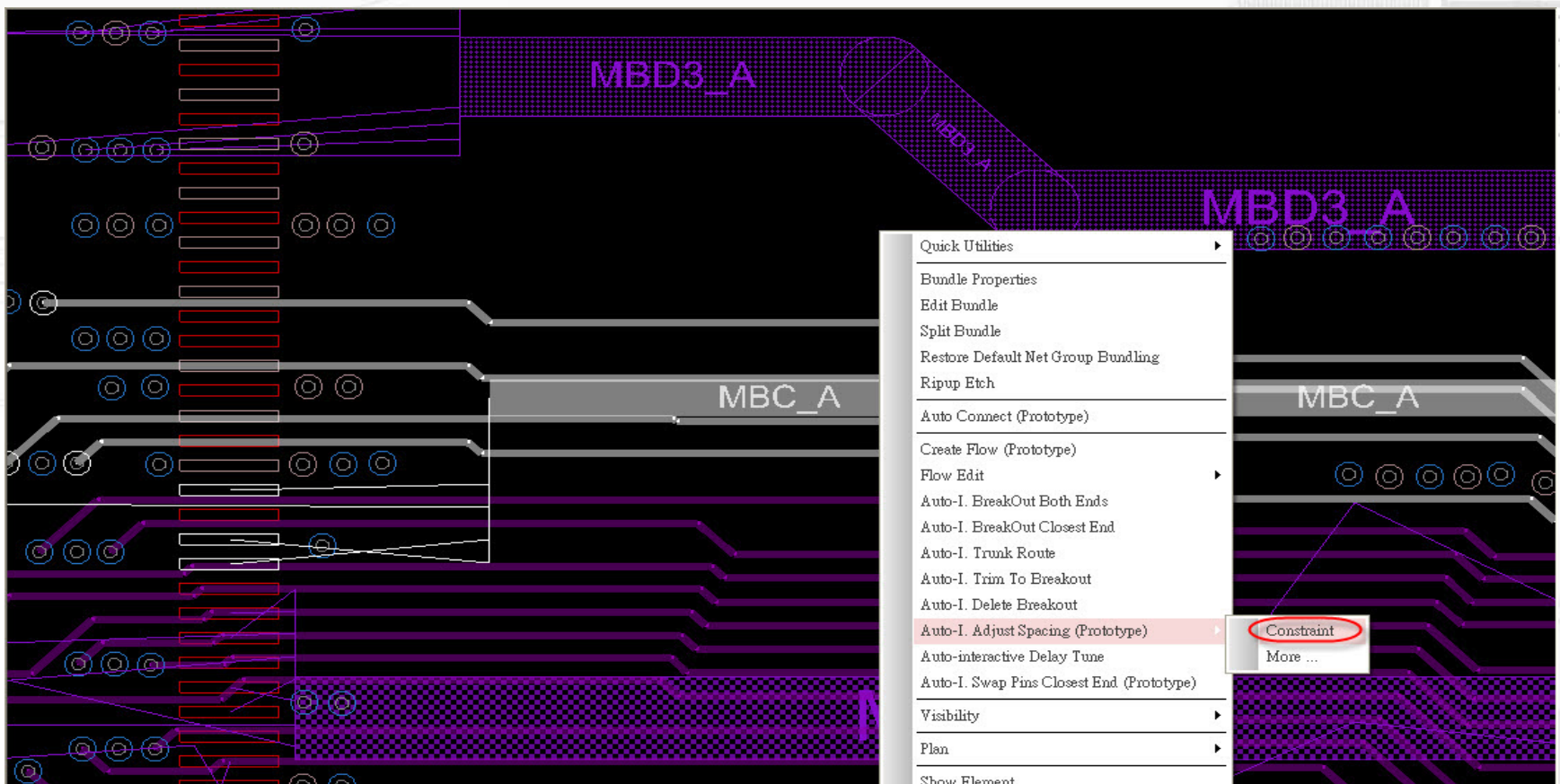
◎ 連接中間未接上部分



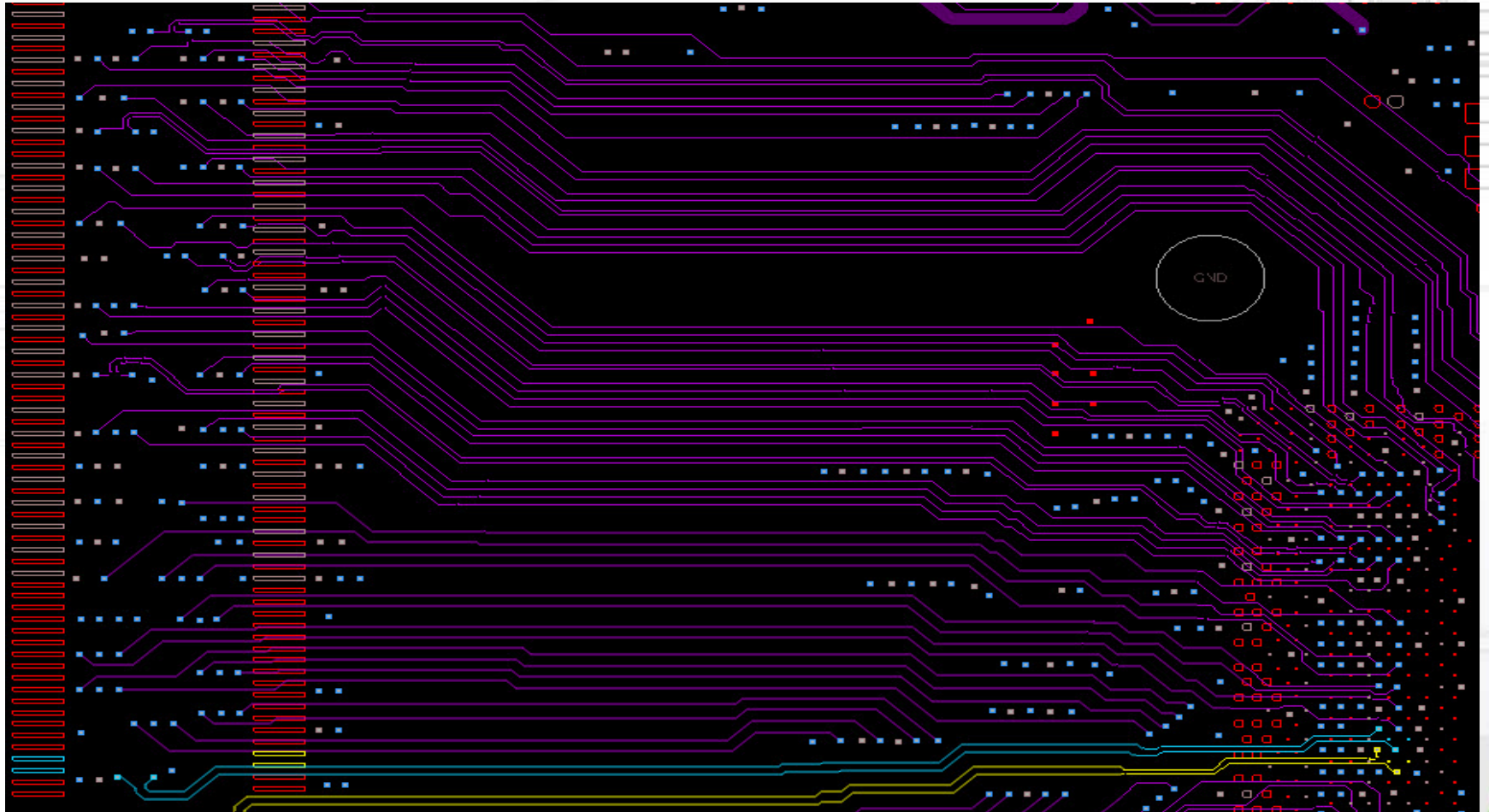


# Auto-I. Adjust Spacing

☉ Default → Constraint



# Route Finish



# Auto-I. Delay Tune

◎ Override bundle params

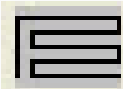
優先於bundle的設定→建議勾選

◎ Tuning Pattern

Accordion



Trombone



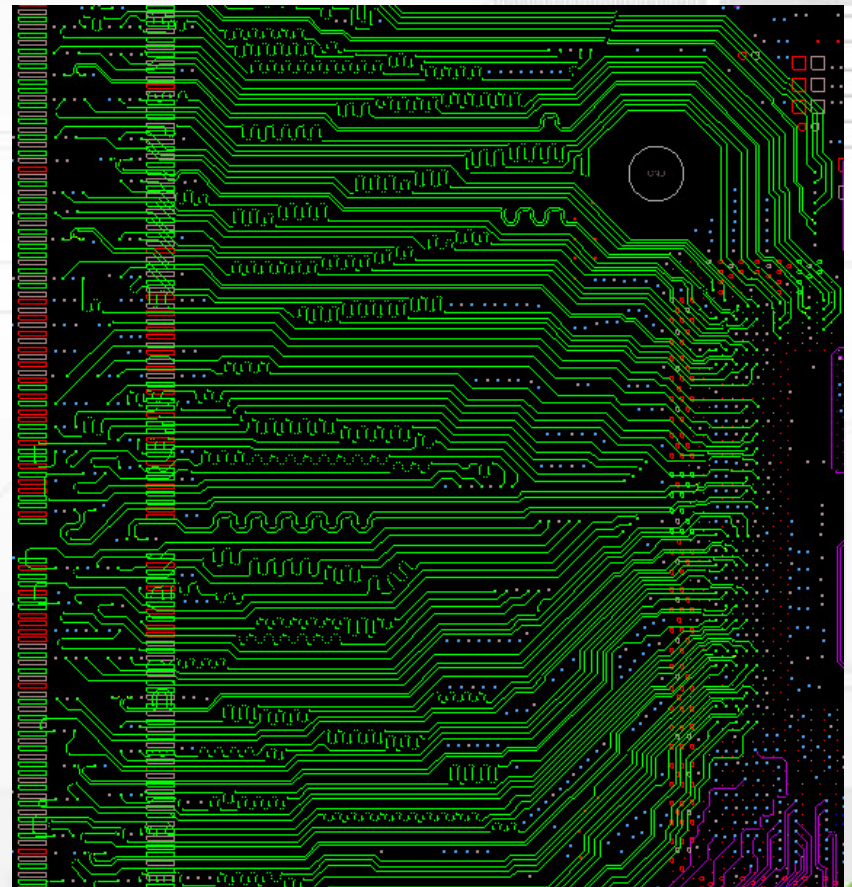
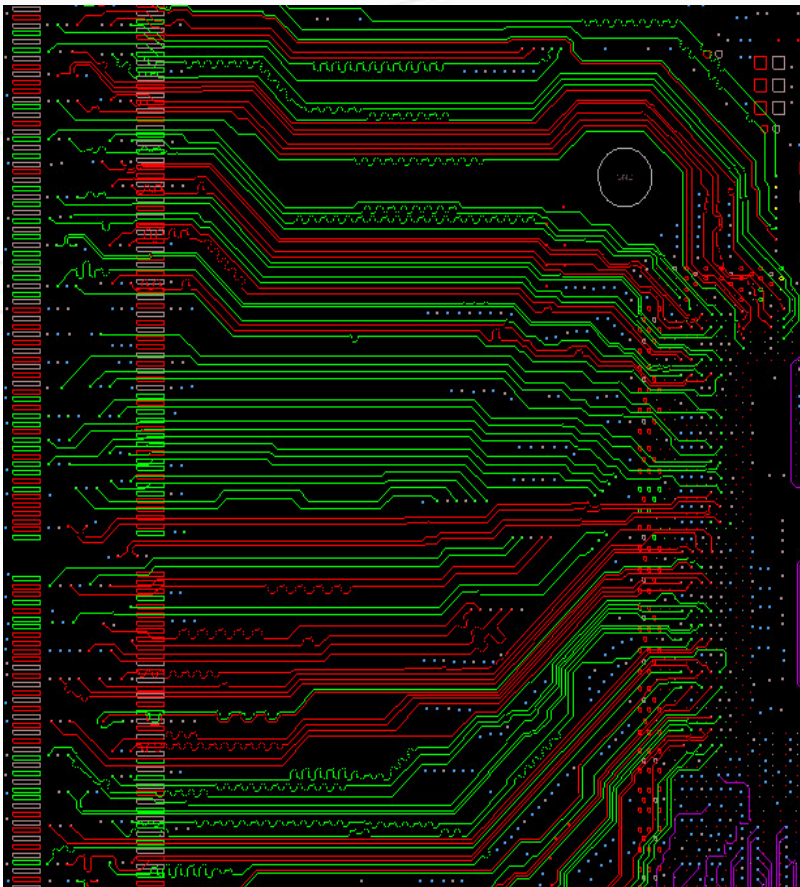
The screenshot shows the 'Route' menu with 'Auto-interactive Delay Tune' highlighted in red. The 'Options' dialog box is open, showing settings for 'Active etch subclass' (In1) and 'Tuning Pattern' (Accordion). The 'Override bundle params' checkbox is checked. The 'Accordion' section shows 'Gap' set to 3x width, 'Min Amplitude' set to 3x width, 'Max Amplitude' set to 40x width, 'Corner Type' set to 45, and 'Miter Size' set to FullArc. The 'Trombone' section shows 'Max Levels' set to 1, 'Gap' set to 3x width, 'Min Amplitude' set to 3x width, 'Corner Type' set to 45, and 'Miter Size' set to 1x width.



# AiDT Finish

AiDT

Manual after AiDT



# Auto-I. Delay Tune

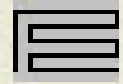
◎ Override bundle params  
優先於bundle的設定

◎ Tuning Pattern

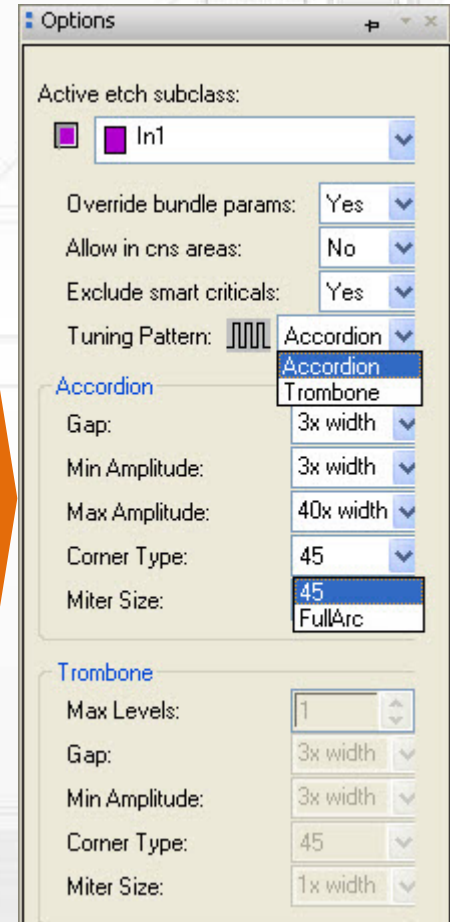
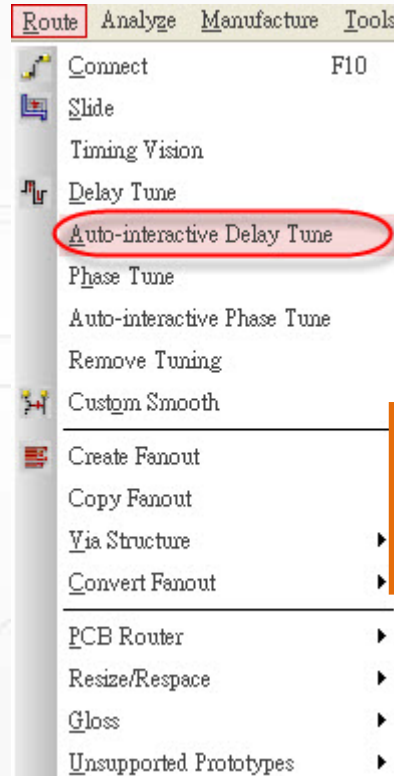
Accordion



Trombone



Corner Type **FullArc**



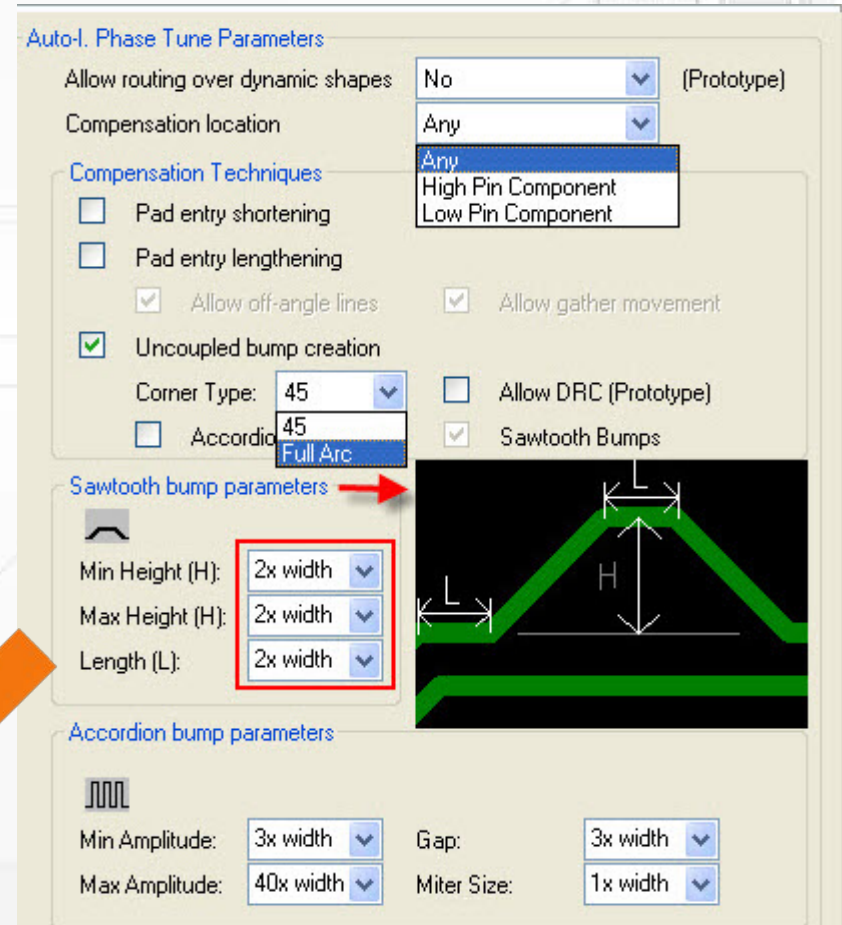
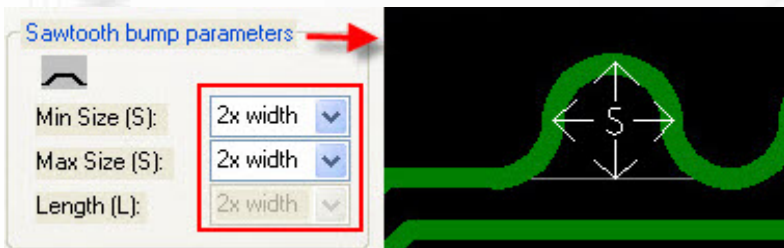
# Auto-I. Phase Tune

## ◎ Compensation Location

走線等長補償位置

## ◎ Corner Type

可選擇45度角及圓弧線



# Experience share

- 如Net Group內有設置Bus,Bundle會鎖定Bus name
- 如果使用新流程,可由Net Group 自動產生Bundle
- 若CM已設置Net Group,則可自動顯示Plan
- Breakout處或瓶頸區不規劃Bundle較能提高出線率
- AiDT: Accordion比Trombone有更高的繞線成功率
- AiDT: 建議先完成target,再對其他走線執行AiDT
- AiPT:建議視狀況勾選Compensation Techniques

# Improve Productivity

## NB/DDR SODIMM

Case	Operation mode	Time
Case1	<ul style="list-style-type: none"> <li>• Manual</li> </ul>	28hr
Case2	<ul style="list-style-type: none"> <li>• Flow Edit</li> <li>• Auto-I. BreakOut Both Ends</li> <li>• Auto-I. Trunk Route</li> <li>• Auto-I. Adjust Spacing</li> <li>• Auto-I. Delay Tune</li> <li>• Auto-I. Phase Tune</li> <li>• <b>Manual edit after AiDT</b></li> </ul>	19hr

**67%**



# Improve Quality

## ERC

- Impedance
- Coupling
- Reference



# Thank you