OrCAD Sigrity ERC

Advanced and Easy to Use PCB Electrical Check Tool

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Topic 1

1. The gap between DRC and SI simulations is filled by Sigrity ERC/SRC
2. Demo
3. More ERC/SRC application examples
4. Conclusion

DRC is the starting point of a good PCB design

- Good PCB SI design starts with adequate DRCs in layout tools
- Today's designs are getting complicated, DRCs are getting complicated too
- General limitations for complicated DRCs
  - Complicated DRCs are normally harder to set up
  - PCB designs are still measured in mil/mm, so the rules tend to be more conservative

The gap between DRC and SI performance

- The gap between layout designers and SI engineers is huge
  - Have different design expertise
  - Using different tools
  - Measured by different units

Gap

Layout/Board designer

Layout tools

Geometry domain (mil/mm)

SI engineer

Simulation tools

Electrical domain (mv, ps)

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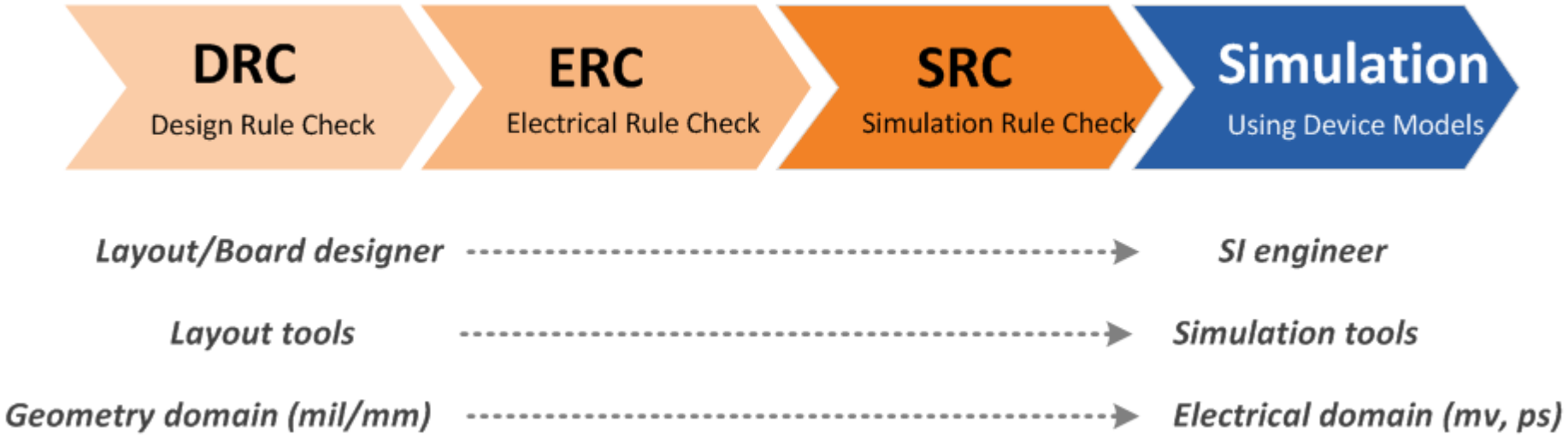
Sigrity ERC/SRC fills the gap

- Sigrity ERC/SRC fills the gap between layout designers and SI engineers
  - Expanded expertise
  - Using same tools
  - Measured by same units



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What is Sigrity ERC?

- Sigrity ERC is individual, segment-level view in geometry domain for PCB's SI performance with
  - Trace reference
  - Trace reference-aware impedance
  - Trace reference-aware coupling
  - Differential pair routing phase
  - # of vias and via locations, ….

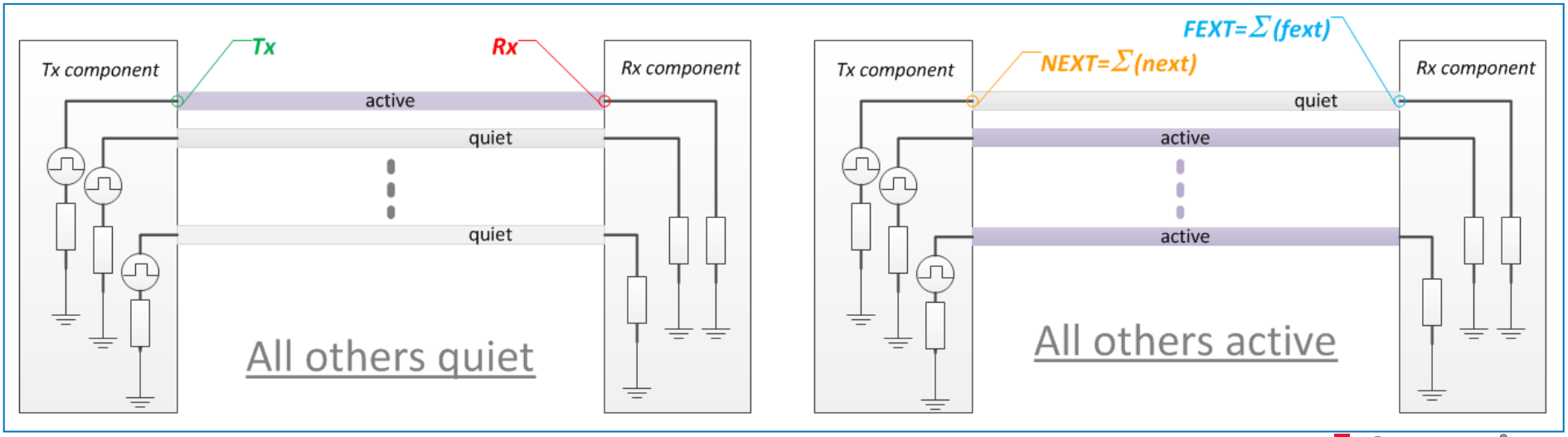
1

  - Organized for easy SI performance interpretation

2

What is Sigrity SRC?

- Sigrity SRC is Macro, combined, net-level view in time-domain of impact due to ERC violations measured in mv&ps (no device model needed)
  - Setup considering termination impedance, data rate (pulse width, rise/fall time), and amplitude
  - Results with Tx/Rx/NEXT/FEXT waveforms, SI performance metrics
  - Organized to easy SI performance interpretation along with ERC

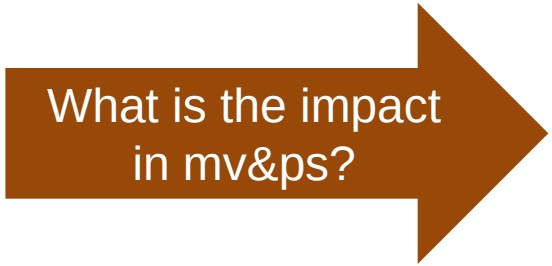


ERC/SRC applications (1)

ERC → SRC
→ SI simulation

- To screen board and to identify worst case for further analysis
- To investigate SI impact of design rule violations and trade-offs

Problems found in layout design



To fix, or not to fix?

If layout problems can be quantified using mv/ps, it is much easier to decide

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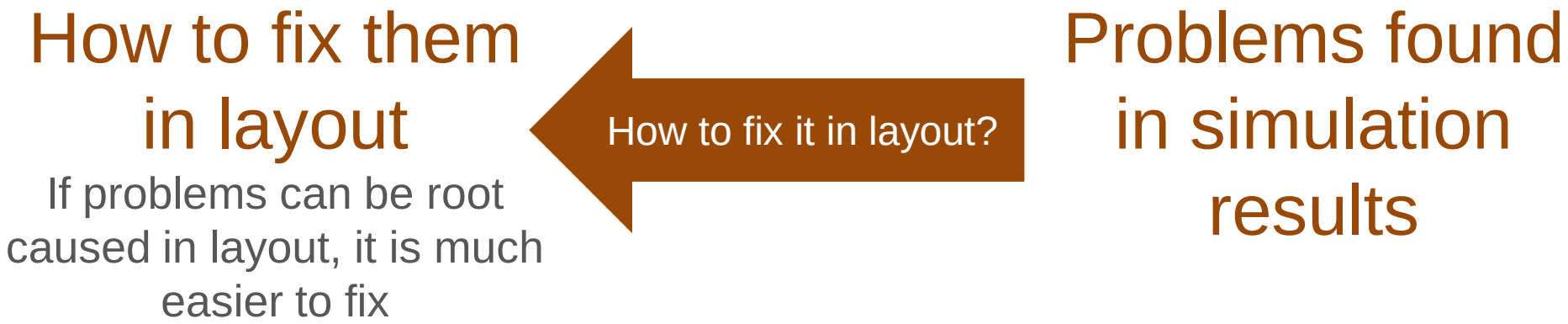
ERC/SRC applications (2)

ERC ← SRC

- To find out how to fix SI problems shown in SRC simulation



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ERC/SRC applications (3)

ERC screening & sign-off
SRC screening & sign-off

- To compare against ERC/SRC results with
  - Known-good design
  - Reference design
  - Part of the design that has been fully analyzed

SI engineer: Define ERC/SRC rules

Layout designer: Check for compliance

Topic 2

1. The gap between DRC and SI simulations is filled by Sigrity ERC/SRC
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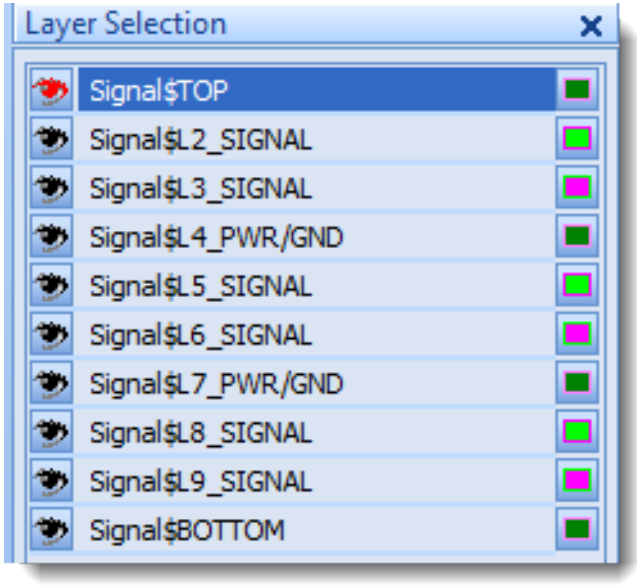
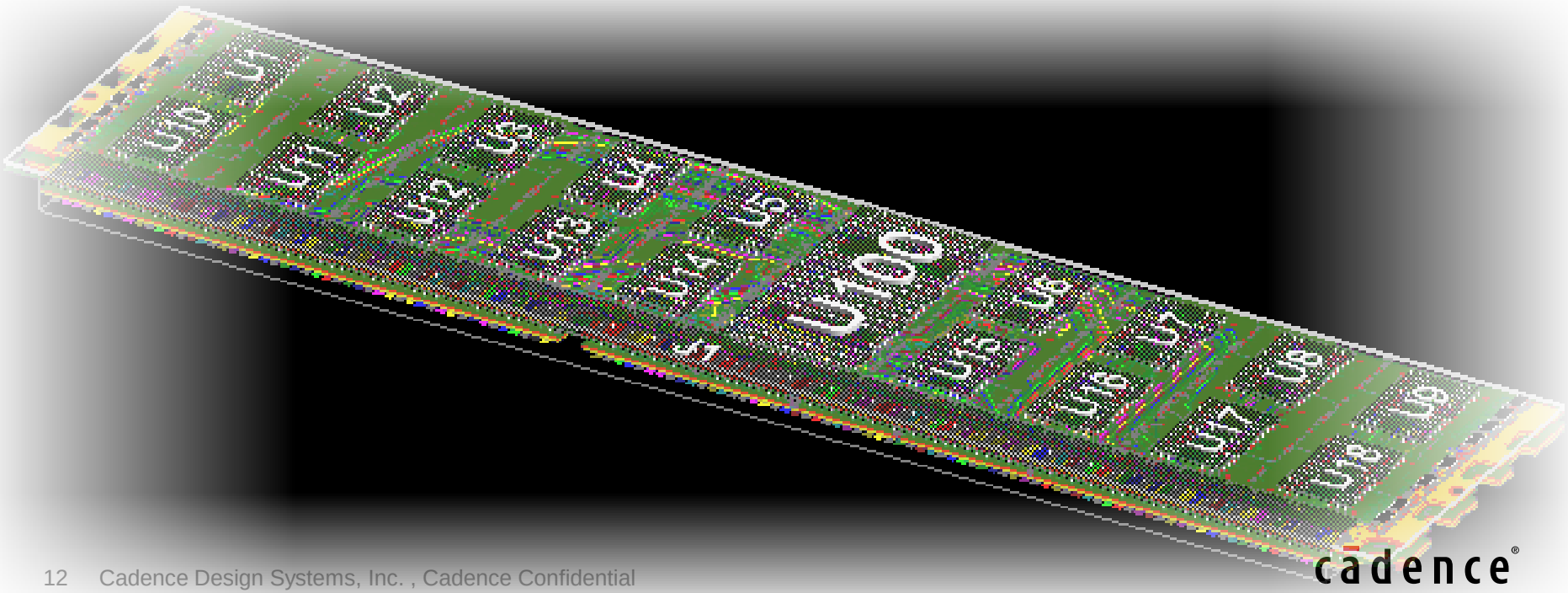
Demo board: DDR3 LRDIMM

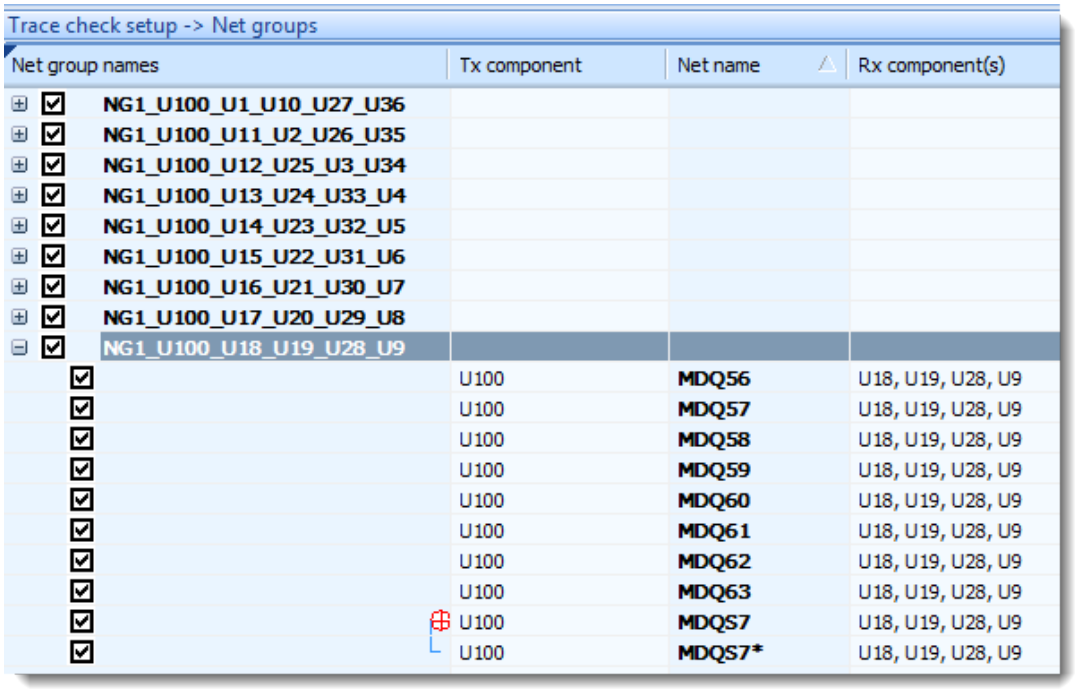


- 1 buffer: U100
- 36 DRAMs: U1 – U36
- 10 layers



Generate net groups

- 9 Data net groups
- These net groups can be used for both ERC and SRC



Net group naming:
InterfaceName_TxCompName_AllRxCompNames

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SRC setup

- Simple and easy

Set up Simulation Option

- Level-1 (Single lines with ideal PDN; delay, loss, reflection effects)
- Level-2 (Coupled lines with ideal PDN; plus trace, via xtalk effects)
- Level-3 (Coupled lines with non-ideal PDN; plus return path and SSO effects)
- Level-4 (3DFEM model based; lack of reference cases)

Transient Time Step (ps): 5

Coupling (%): 2

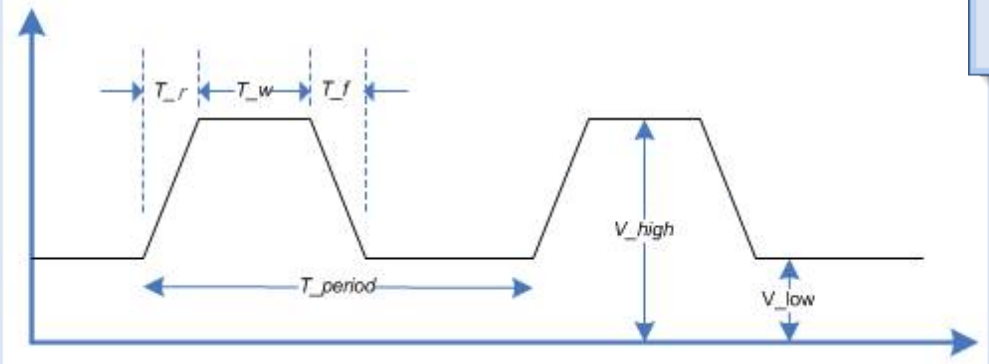
Rise Time (ps): 50

Sim Time: 2 ns

OK Cancel

Set up SI Metrics Check Wizard

Set up Tx/Rx Models



Import Tx/Rx Models Export Tx/Rx Models

Interface and ckt type	Tx_term type	R(ohm)	C(F)	V_low(V)	V_high(V)	Tdelay(s)	T_r(s)	T_f(s)	T_w(s)	T_period(s)	Rx_term type	R(ohm)	C(F)	(S)Rx_term type	(S)R(ohm)	(S)C(F)
NG1:SE	**R**	40	-	0	**1**	0p	**100p**	100p	**525p**	30n	**R**	40	-	R	**5000**	-
NG1:Diff	**R**	40	-	0	**0.5**	0p	**100p**	100p	**525p**	30n	**R**	40	-	R	**5000**	-

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SRC simulation

- 9 data signal net groups selected, with 72 SE nets and 9 diff pairs
- Level-2 simulation with
  - Trace-2-trace couplings
  - Via-2-via couplings
- Simulation time: 18.5min

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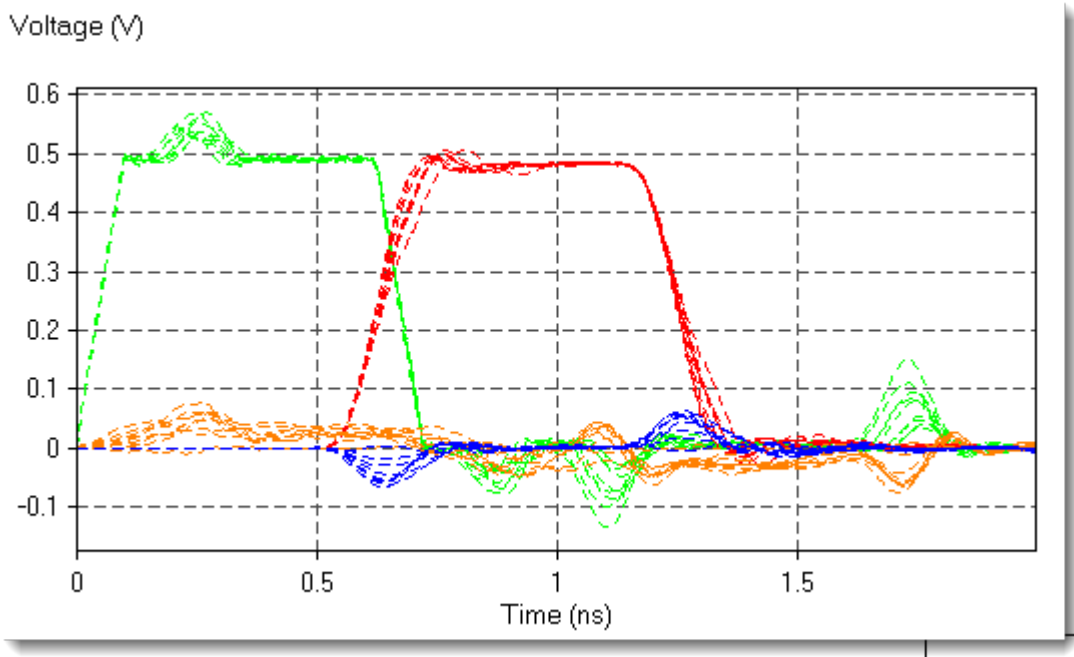
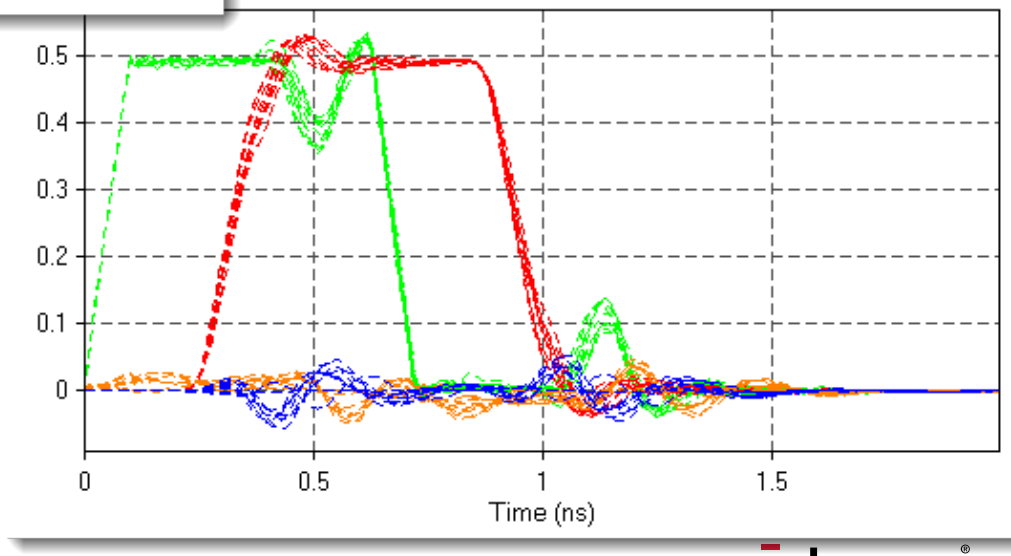
SRC results – Tx/Rx/NEXT/FEXT waveforms



- Tx / Rx / NEXT / FEXT waveforms



Which net group's traces are longer?

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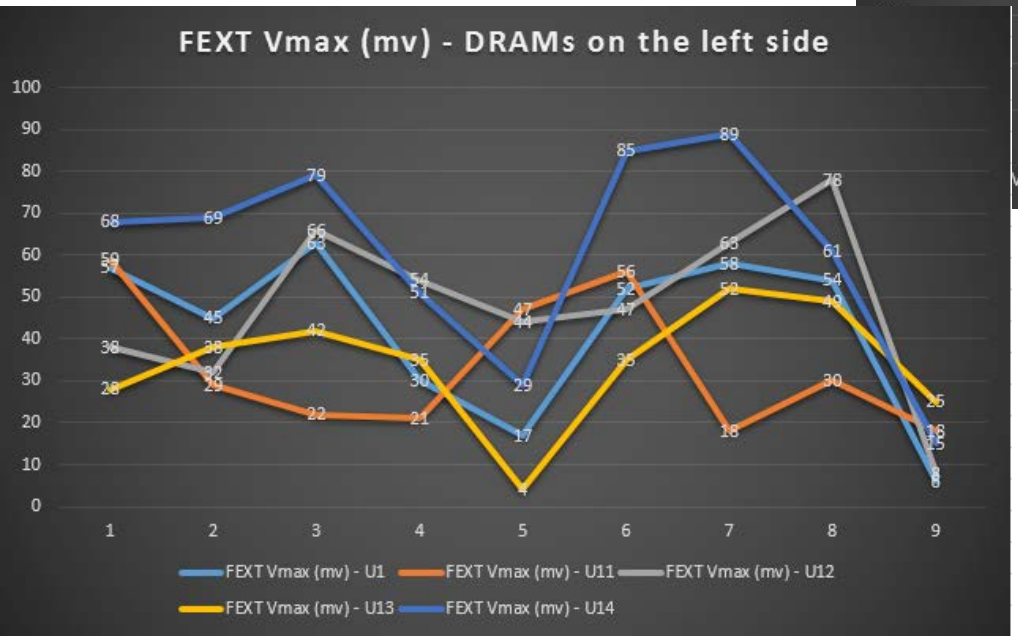
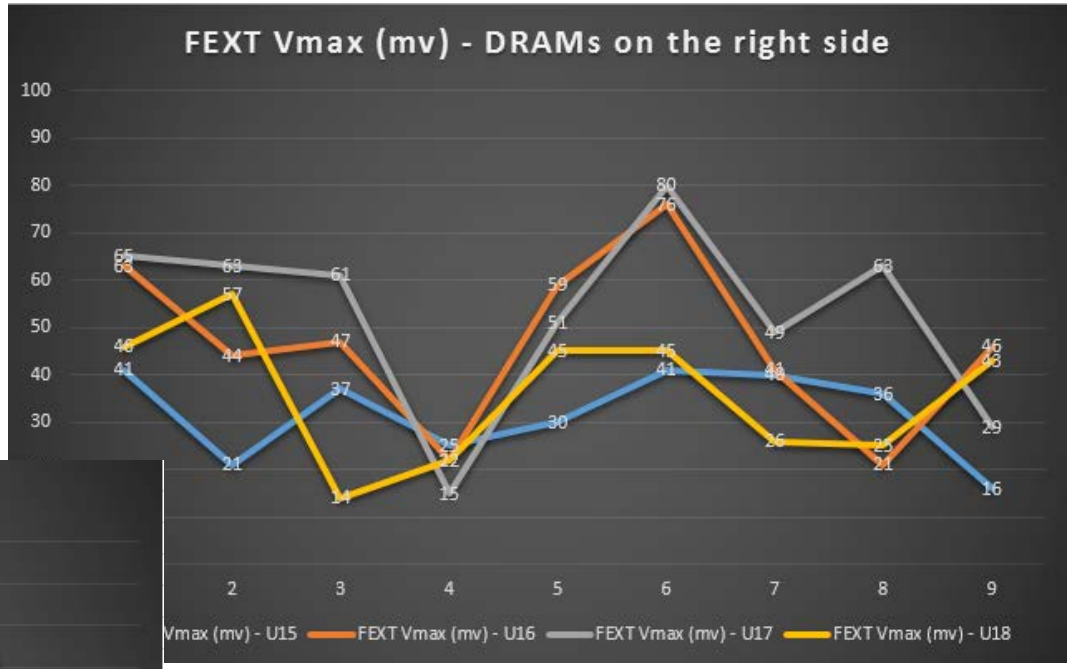
SRC results – FEXT for data signals

- Chart FEXT Vmax for all 9 data net groups





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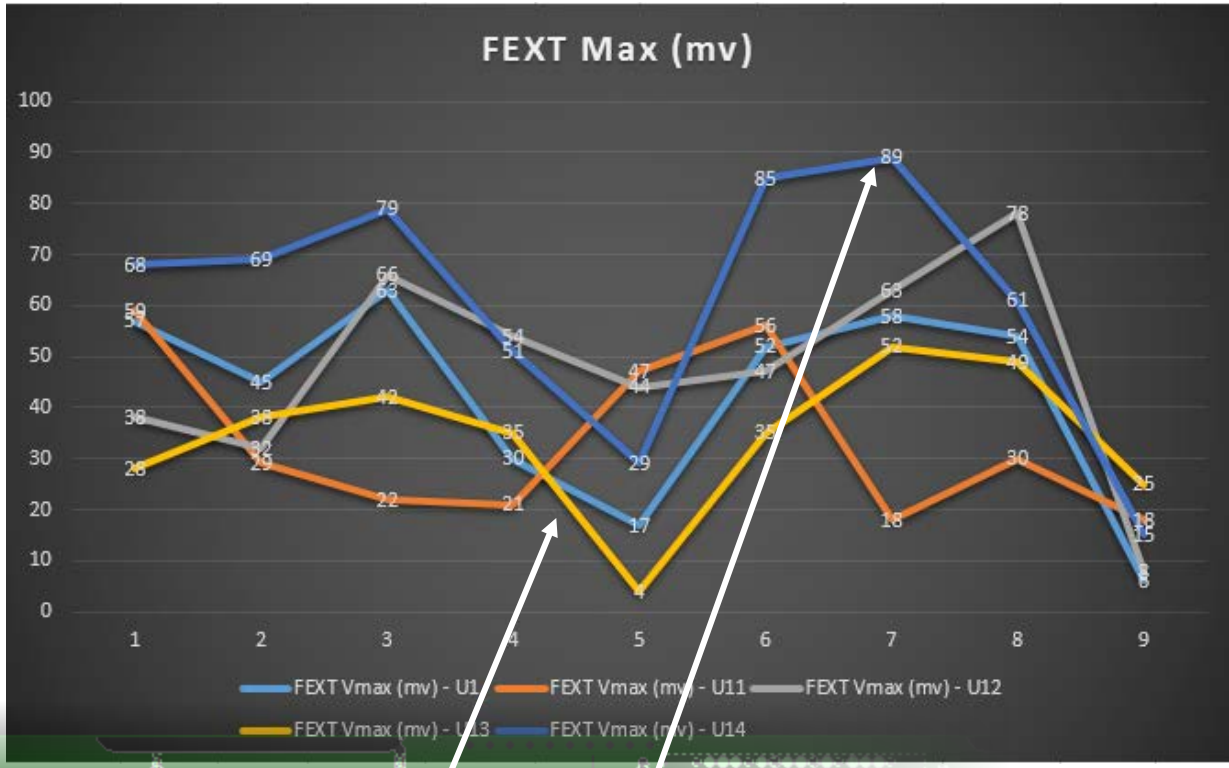
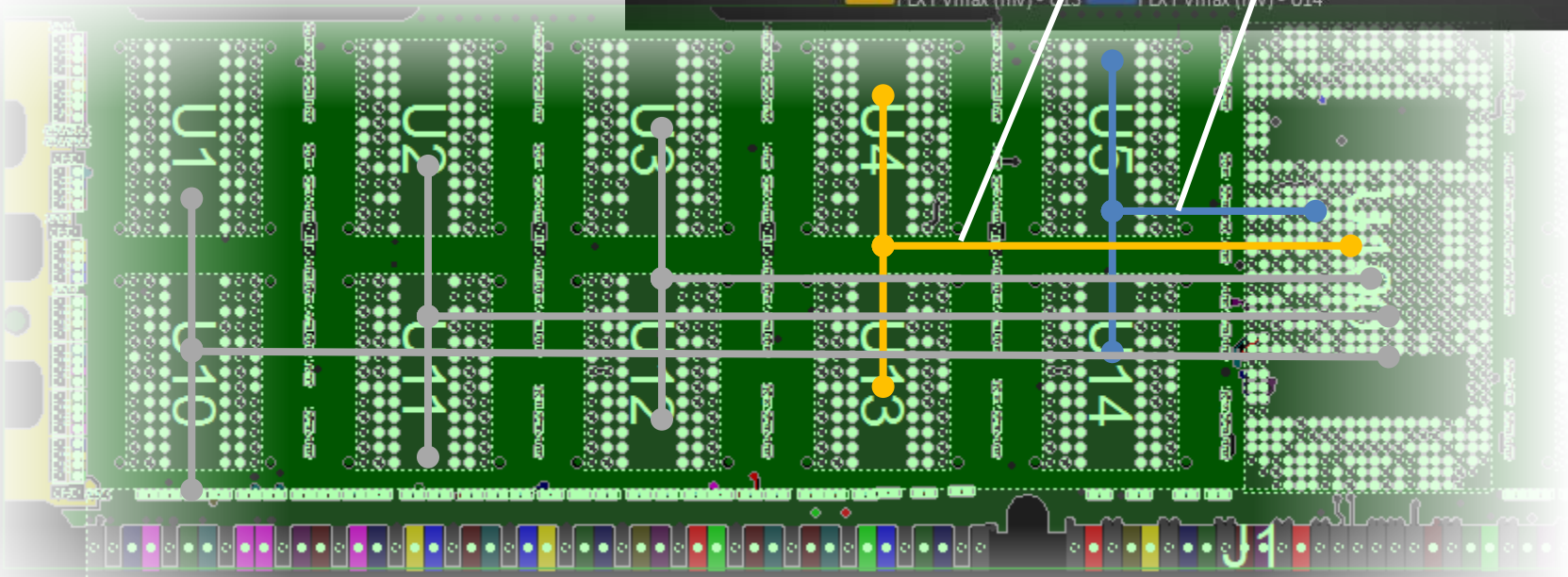
SRC results analysis – FEXT Vmax

- The longer data signals at **U13** have **less** FEXT
- The shorter data signals at **U14** have **more** FEXT





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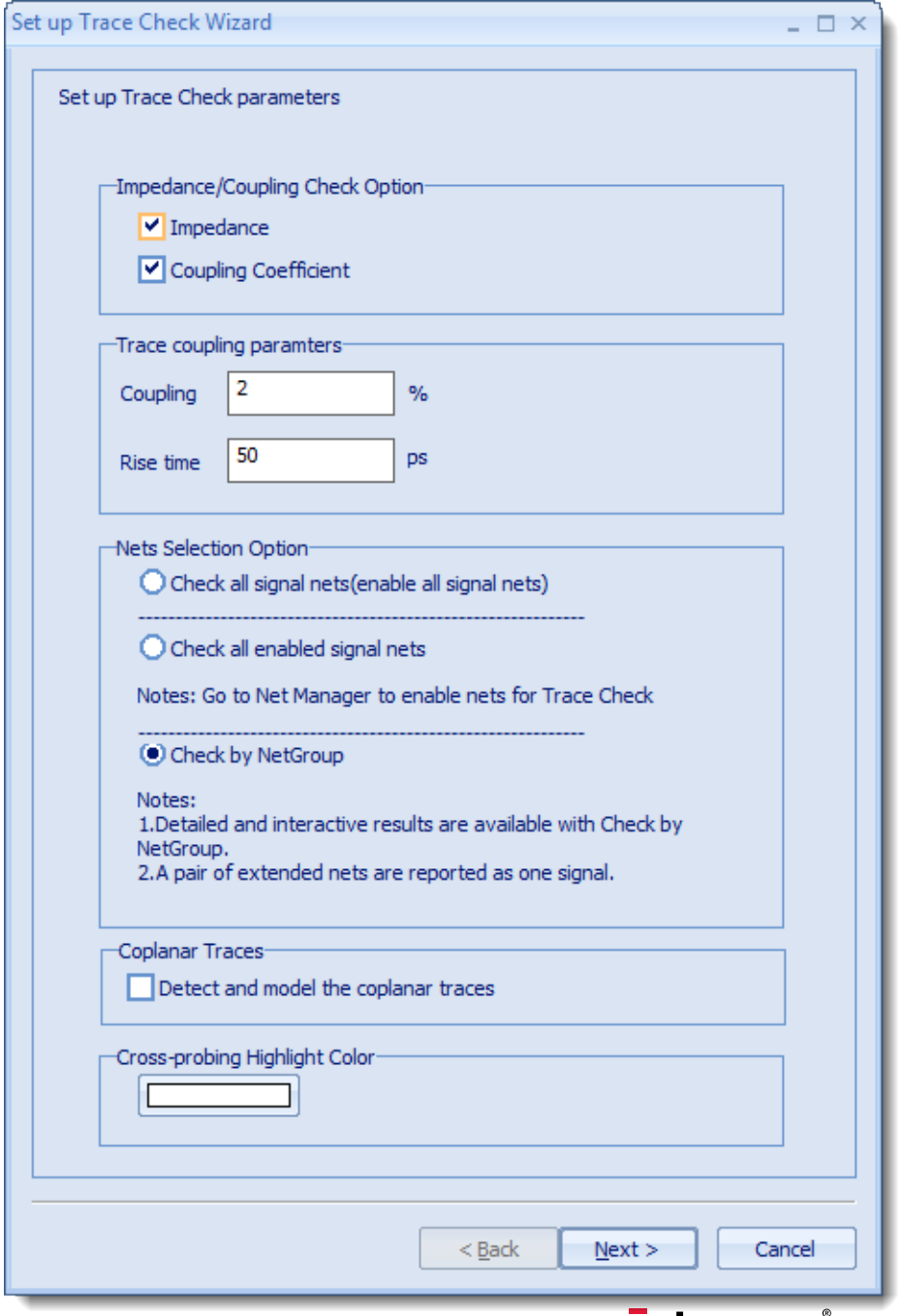
ERC setup

- ERC setup: Also simple and easy
- All 4 net groups are included in running ERC



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ERC Results

Name

- ERC_DDR3_LRDIMM_BoardRoutingInfo_091515_192115.csv
- ERC_DDR3_LRDIMM_CplDetailed_091515_192115.csv
- ERC_DDR3_LRDIMM_CplSum_091515_192115.csv
- ERC_DDR3_LRDIMM_ImpDetailed_091515_192115.csv
- ERC_DDR3_LRDIMM_ImpSum_091515_192115.csv
- ERC_DDR3_LRDIMM_UpperLowerRefSum_091515_192115.csv
- TraceCKResult_ERC_DDR3_LRDIMM_091515_192115_result.xml
- TraceCKResult_ERC_DDR3_LRDIMM_091515_192115_resultBin.bin

Results and Report

Net Based Tables/Plots

- Impedance Summary Table
- Impedance Detailed Table
- Coupling Summary Table
- Coupling Detailed Table
- Upper/Lower Layer Reference Table
- Coplanar Reference Table
- Board Routing Information Table
- Impedance Layout Overlay
- Coupling Layout Overlay

Impedance between 2 Components

- Impedance Plot (collapsed)
- Impedance Plot (expanded)
- Impedance Table
- Impedance Layout Overlay

Coupling between 2 Components

- Coupling Plot (collapsed)
- Coupling Plot (expanded)
- Coupling Table
- Coupling Layout Overlay

Reference between 2 Components

- Reference Plot (expanded)

Violations

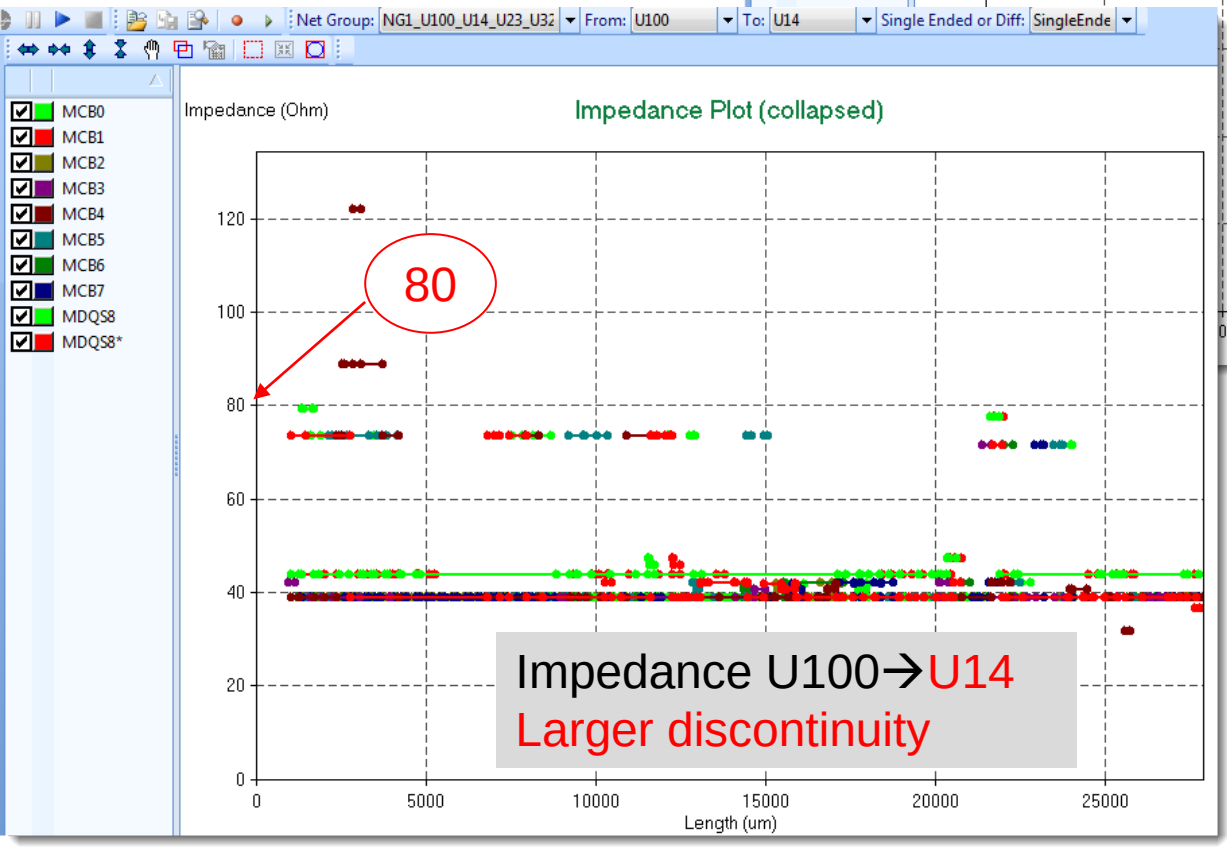
- Impedance Violation Table
- Coupling Violation Table

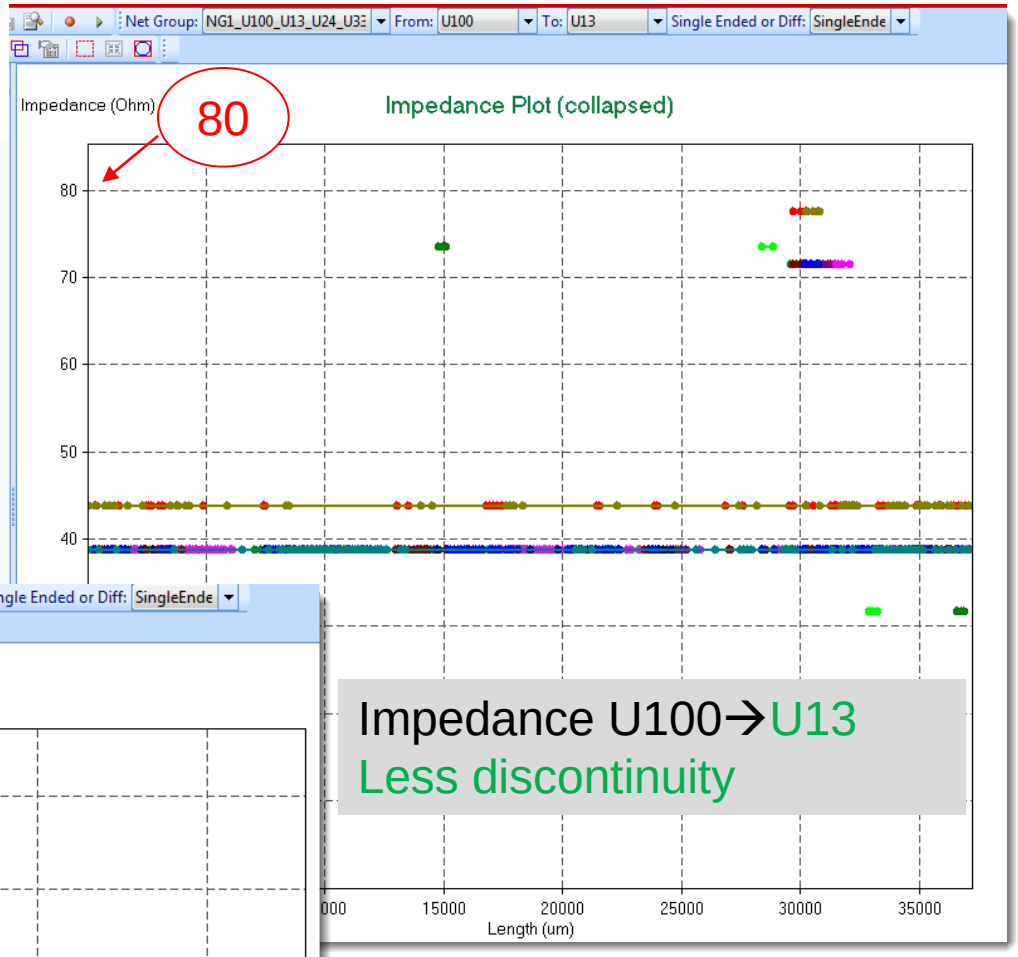
Result File and Report

- Save Results
- Load Results
- Generate HTML Report
- Save HTML Report

U13 vs. U14

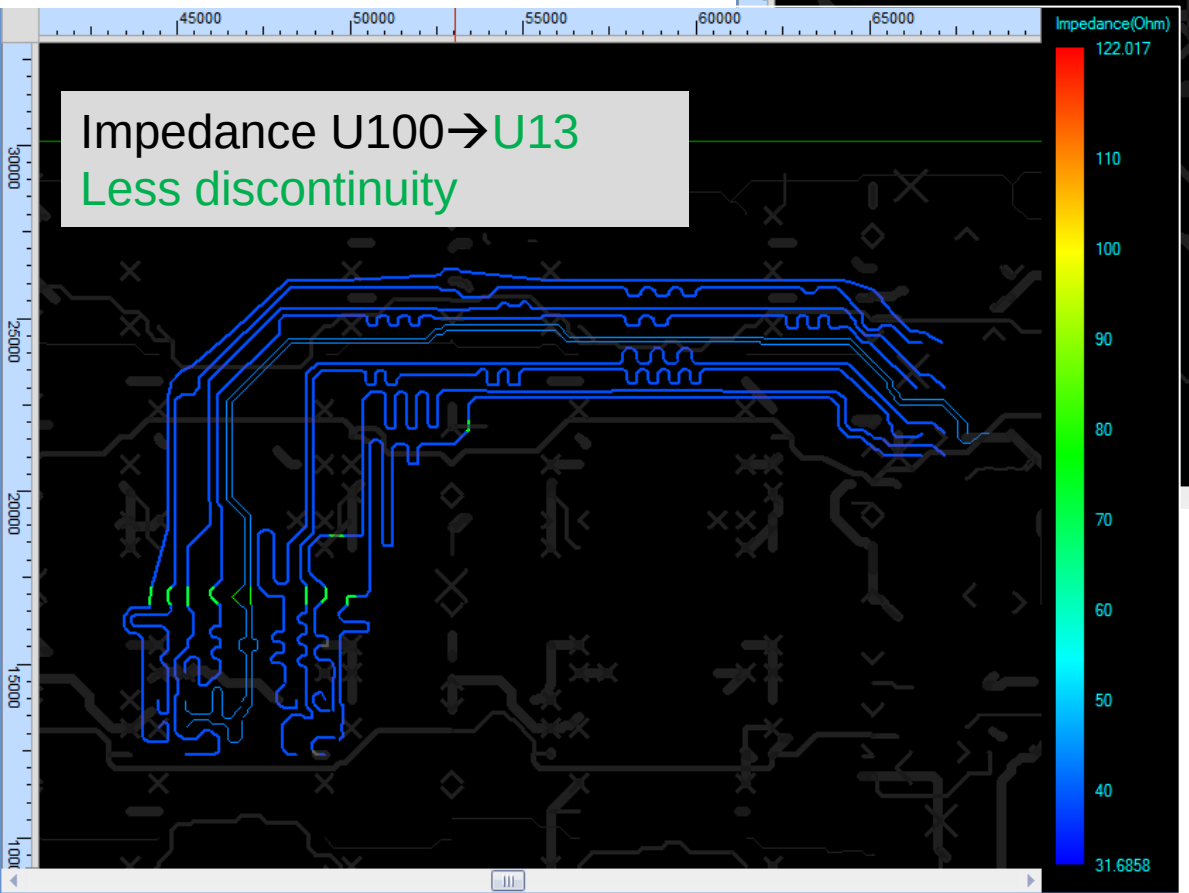
Impedance comparison



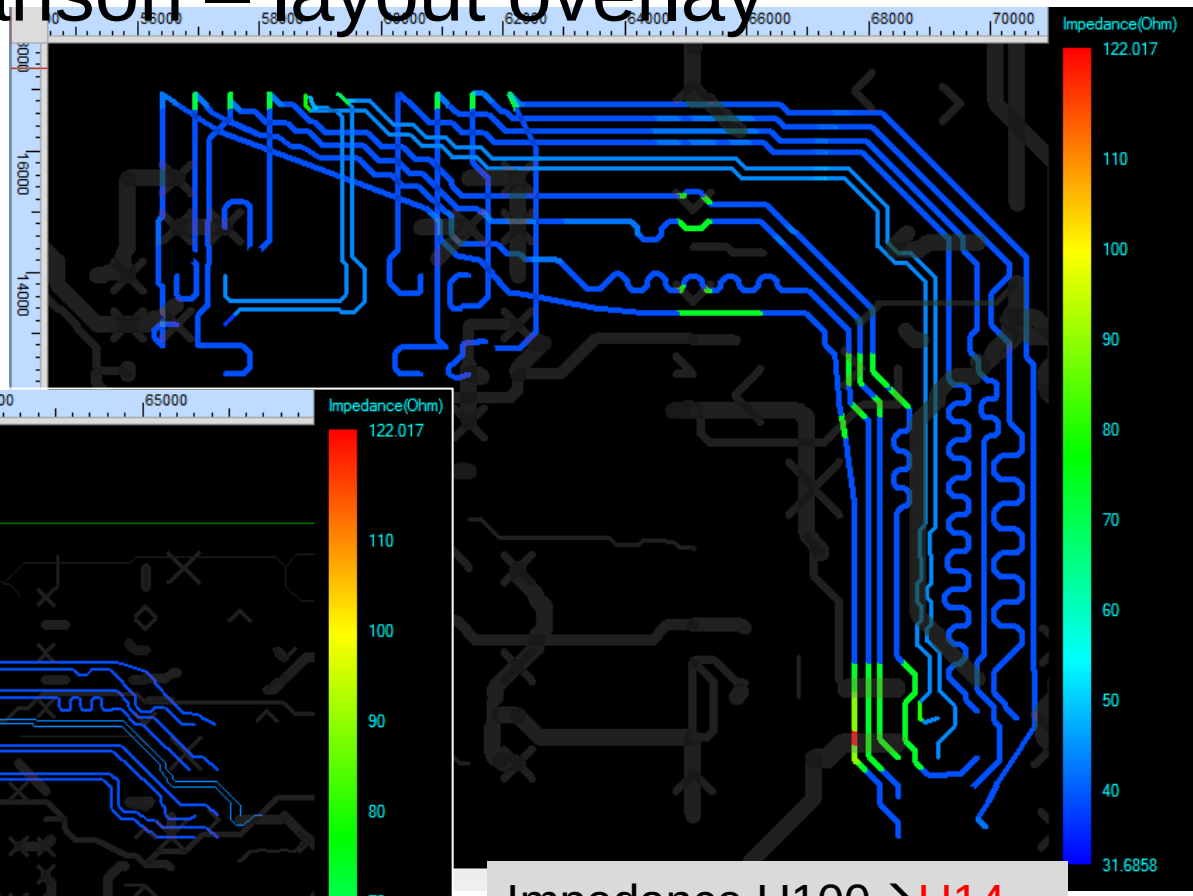


U13 vs. U14

Impedance comparison – layout overlay



Impedance U100→U13
Less discontinuity



Impedance U100→U14
Larger discontinuity

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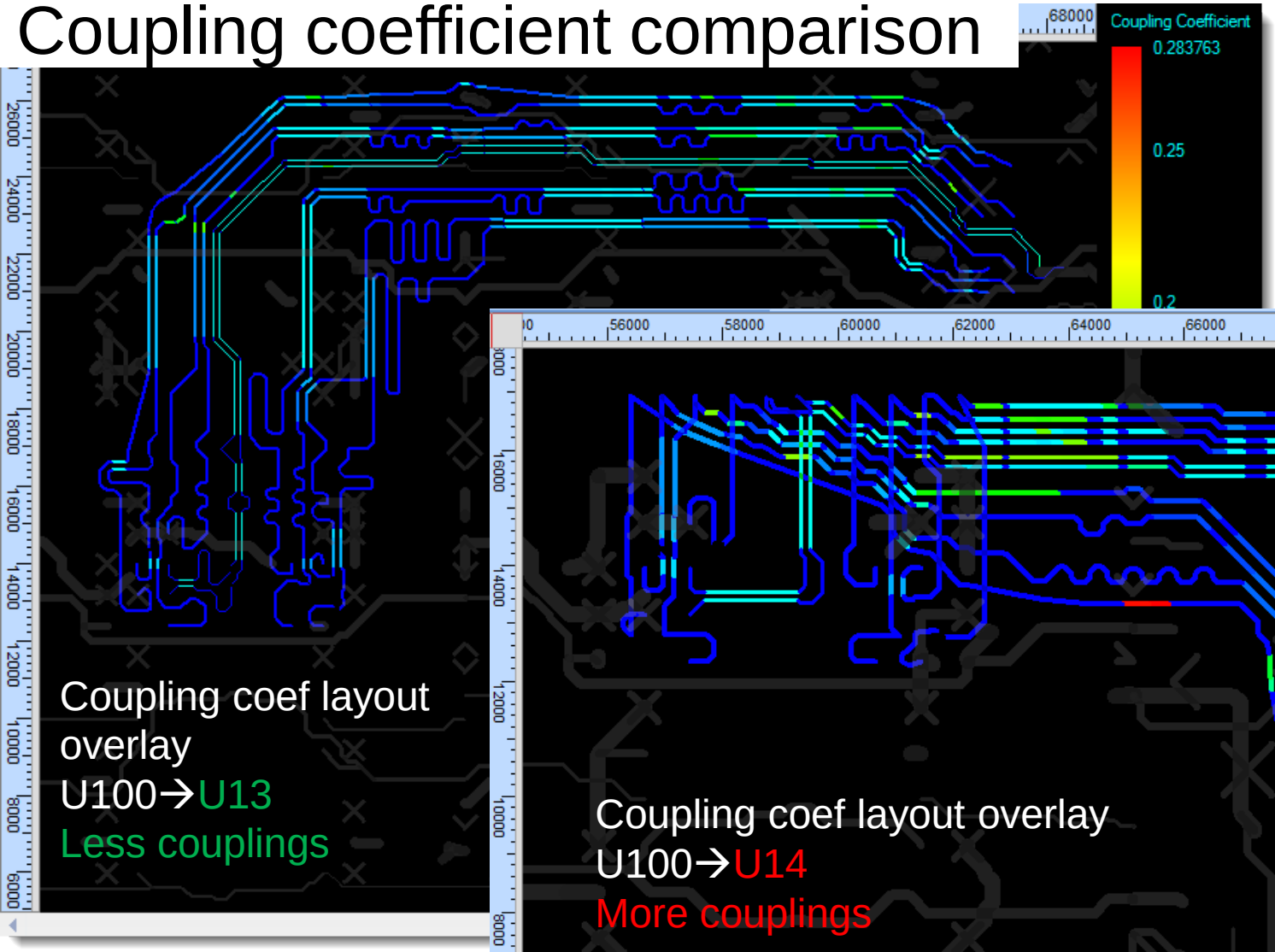
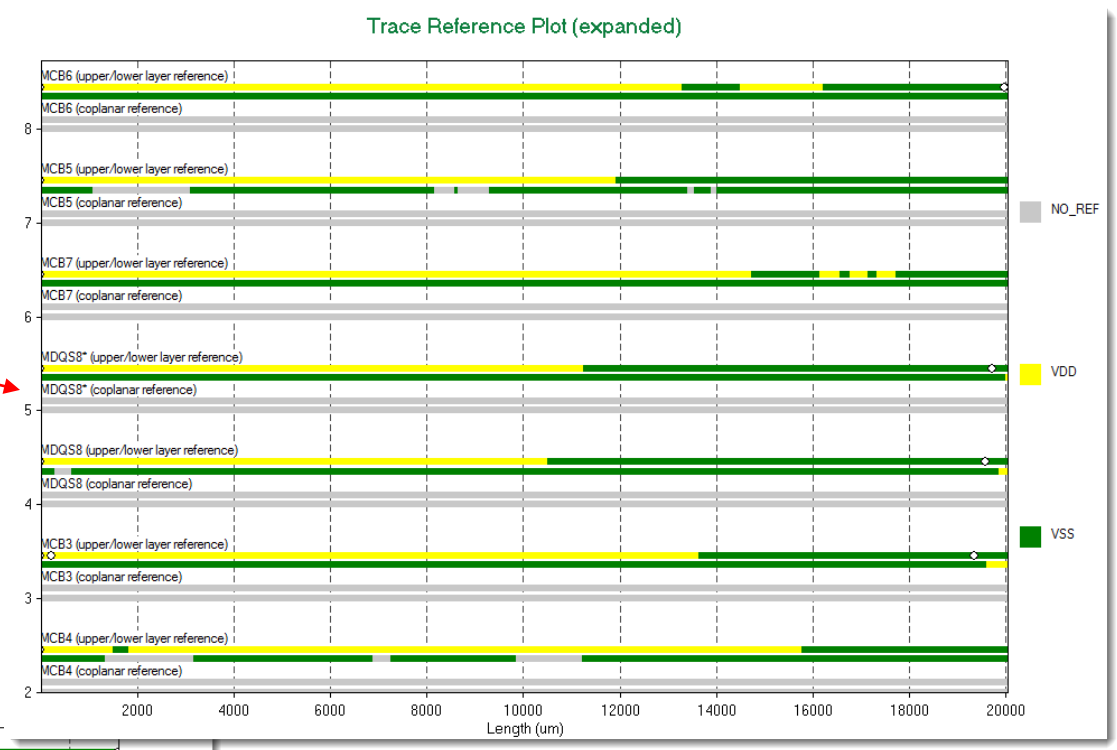
Coupling coefficient comparison



U13 vs. U14

Trace reference

Reference U100→U14
More discontinuity



Reference U100→U13
Less discontinuity

Note:

- The effect of impedance changes caused by trace reference changes are included in level-2 SRC simulation
- Since level-2 simulation assumes ideal pwr/gnd, the return path discontinuities effects are not included

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Topic 3

1. The gap between DRC and SI simulations is filled by Sigrity ERC/SRC
2. Demo
3. More ERC/SRC application examples
4. Conclusion

ERC/SRC example 1

ERC → SRC
→ SI simulation

- To screen board and to identify worst case for further analysis
- To investigate SI impact of design rule violations and trade-offs

ERC ← SRC

- To find out how to fix SI problems shown in SRC simulation

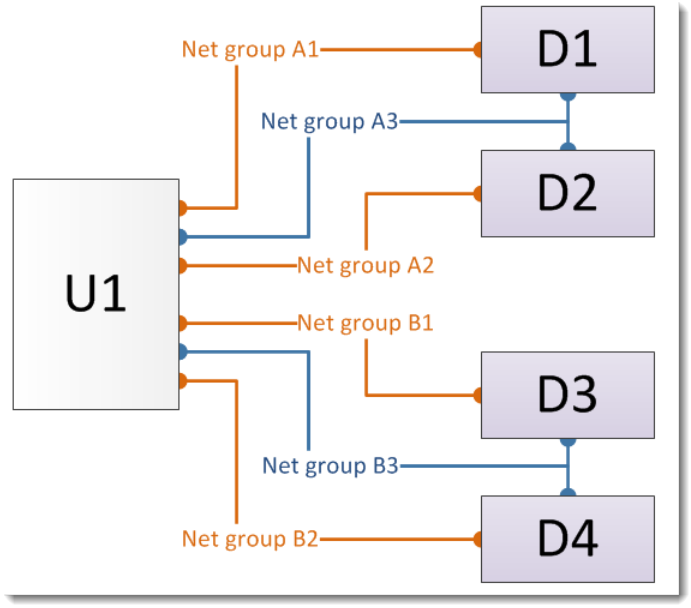
ERC screening & sign-off
SRC screening & sign-off

- To compare against ERC/SRC results with
  - Known-good design
  - Reference design
  - Part of the design that has been fully analyzed

ERC/SRC example 1

DDR

- Memory subsystem for a typical low-end server board
  - 1 controller, 4 DRAMs 2 DDR channels
  - 6 net groups for all DDR nets (178 SE nets; 20 diff pairs)



SI metrics check setup -> Net groups

Net group names	Tx component	Net name	Rx component(active)
NG1_U 1_ D1			
NG1_U 1_ D1_ D2			
NG1_U 1_ D2			
NG1_U 1_ D3_ D4			
NG1_U 1_ D3			
NG1_U 1_ D4			
	UC1	DDR_B_CAB0	D4
	UC1	DDR_B_CAB1	D4
	UC1	DDR_B_CAB2	D4
	UC1	DDR_B_CAB3	D4
	UC1	DDR_B_CAB4	D4
	UC1	DDR_B_CAB5	D4
	UC1	DDR_B_CAB6	D4
	UC1	DDR_B_CAB7	D4
	UC1	DDR_B_CAB8	D4
	UC1	DDR_B_CAB9	D4

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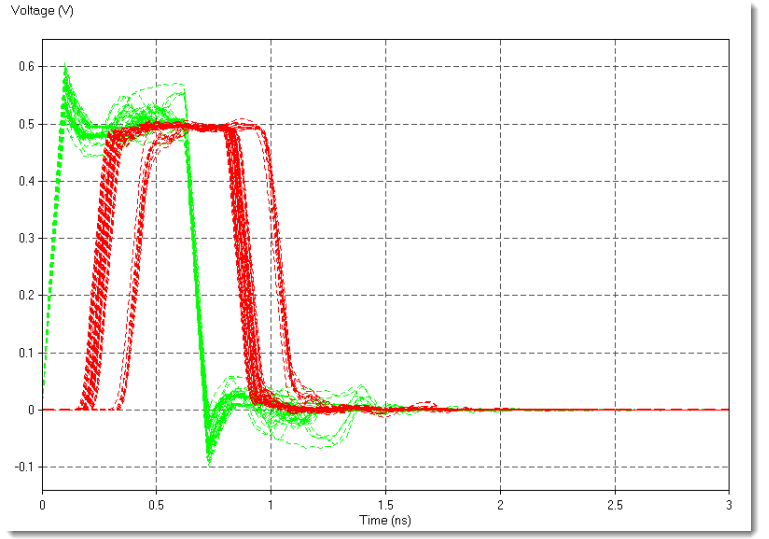
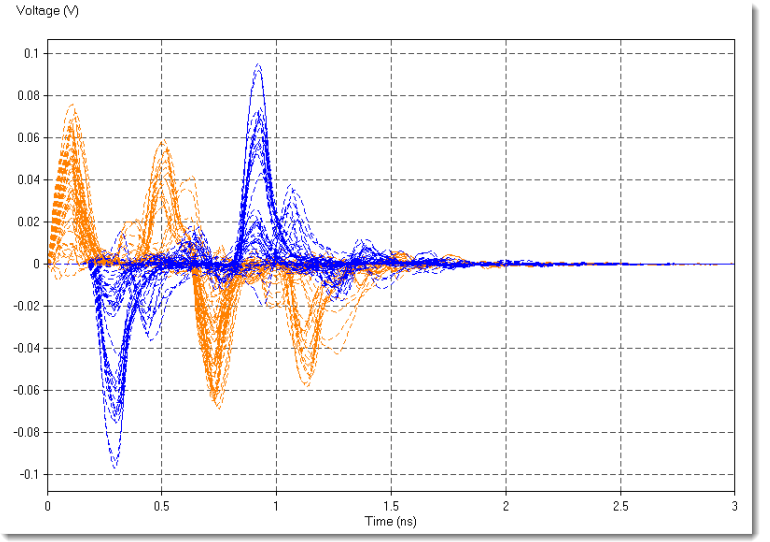
ERC/SRC example 1

SRC setup and waveform results

- SRC setup
  - Pulse width for 1.6GT data with 100ps rise ti
  - 40Ω termination
- Results
  - **Tx** waveforms
  - **Rx** waveforms (simulated delays)
  - **FEXT** waveforms (max, min, pk-2-pk)
  - **NEXT** waveforms (max, min, pk-2-pk)





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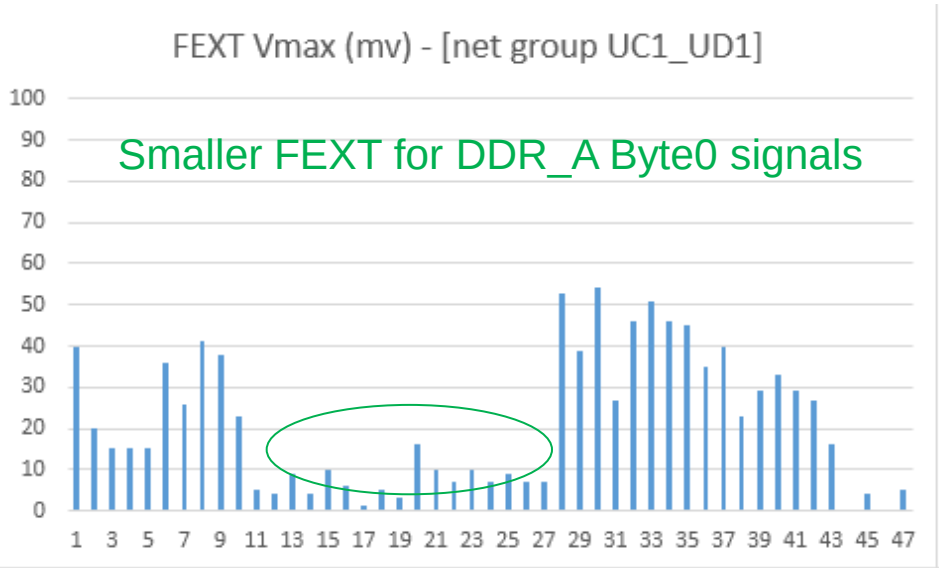
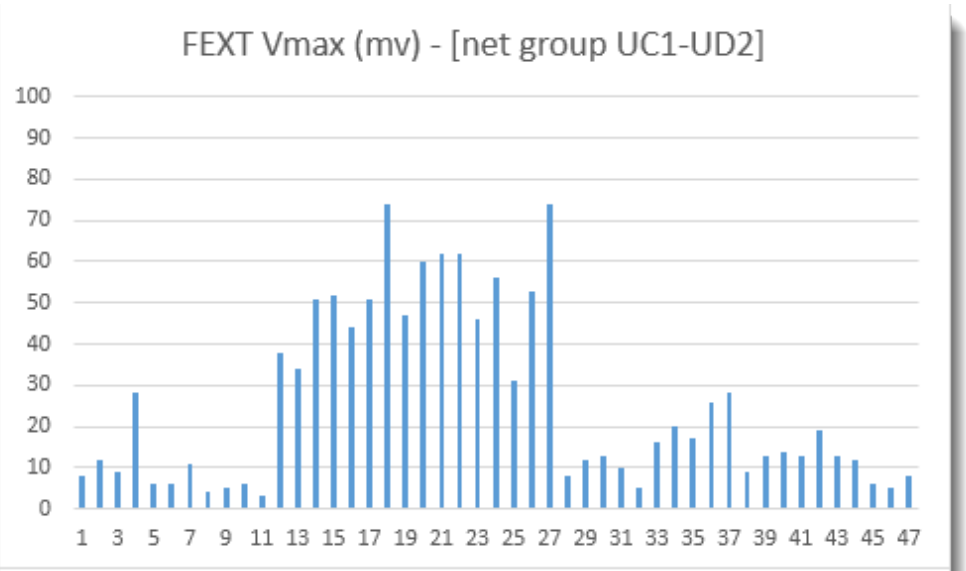
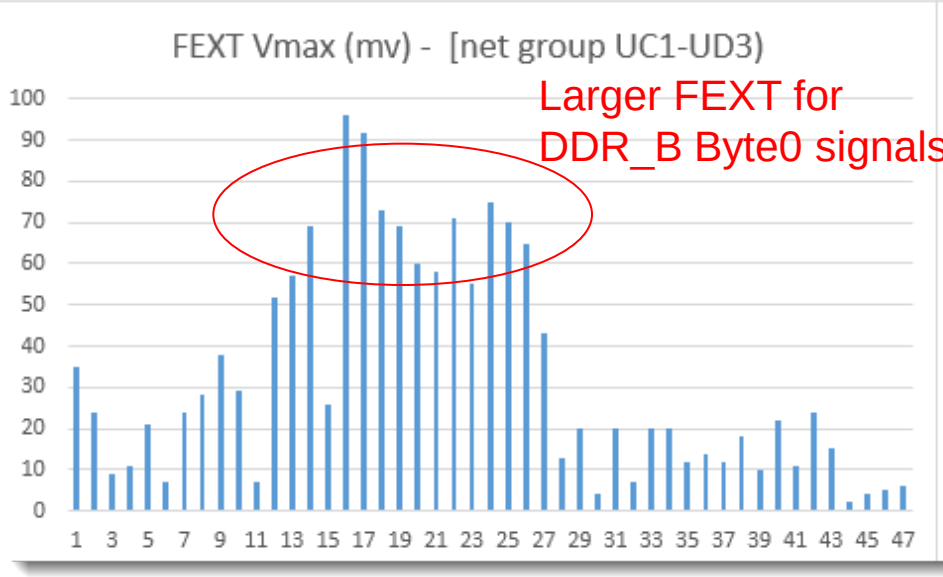
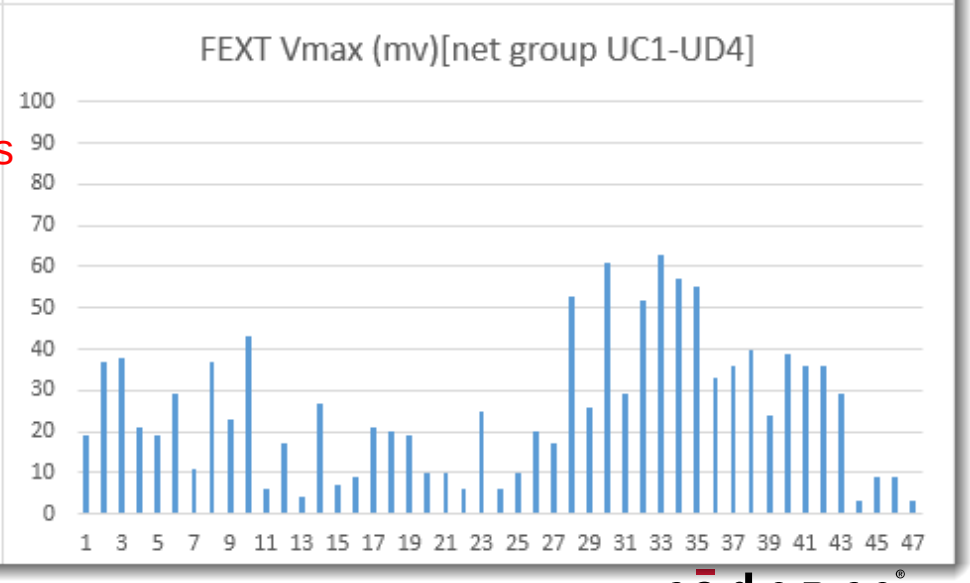
ERC/SRC example 1

SRC – FEXT results









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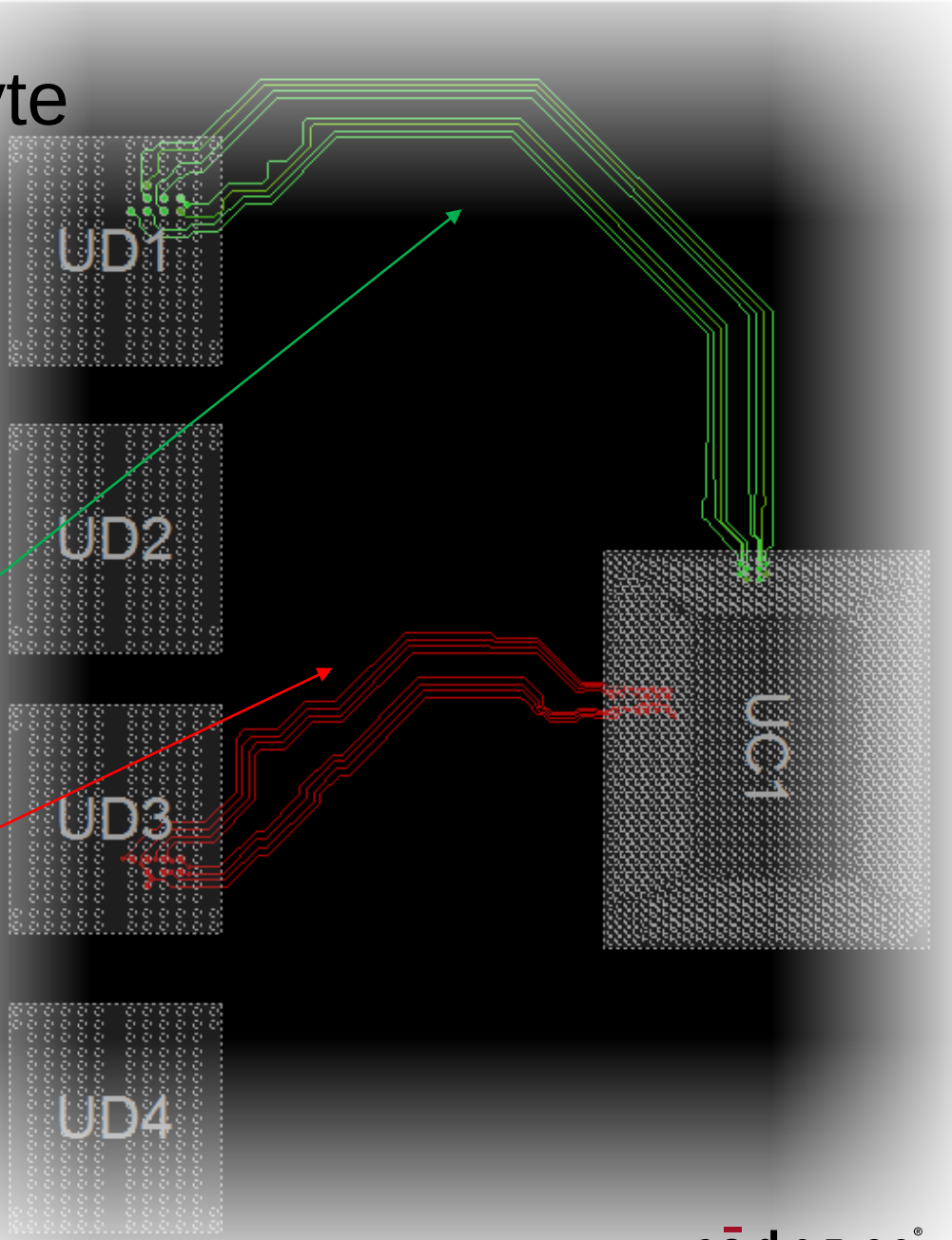
ERC/SRC example 1

SRC – the problem Byte

- One of the problems identified is Byte0 for channel B has large xtalk
- PCB routing
  - Data_A Byte0
    - **Smaller** FEXTs
  - Data_B Byte0
    - **Larger** FEXTs



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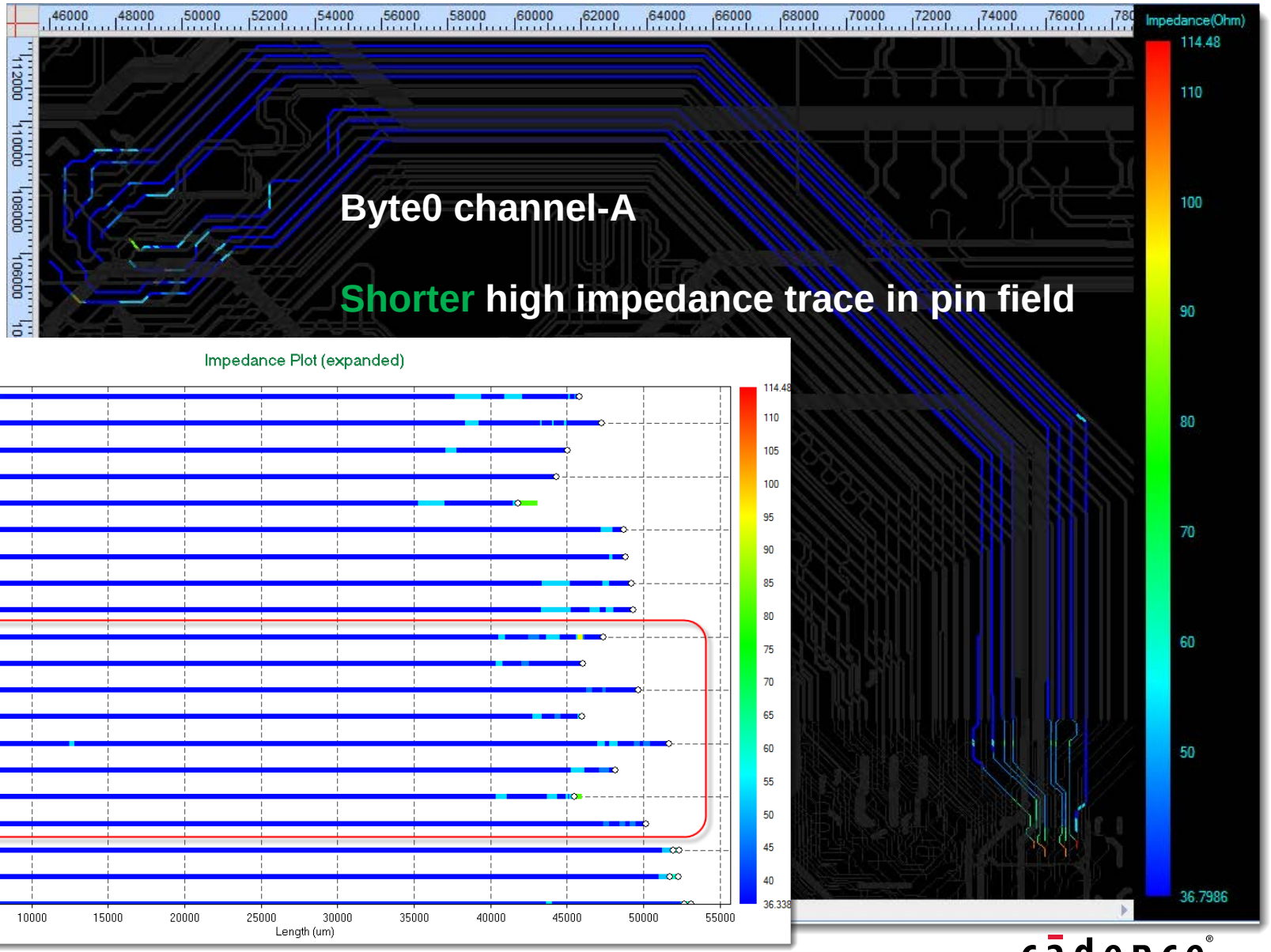
ERC/SRC example 1

ERC – DataA Byte0 impedance



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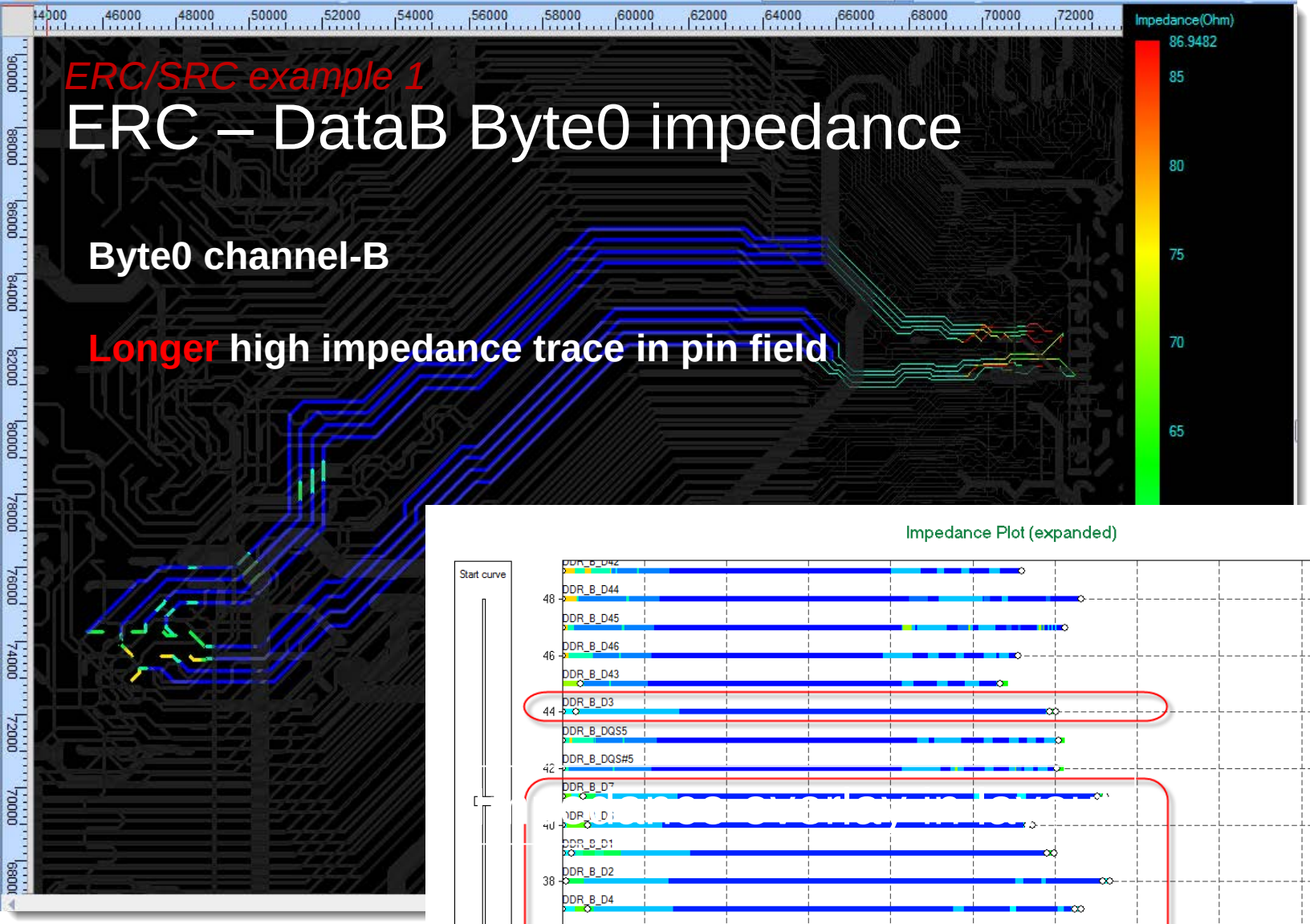
ERC/SRC example 1

ERC – DataB Byte0 impedance

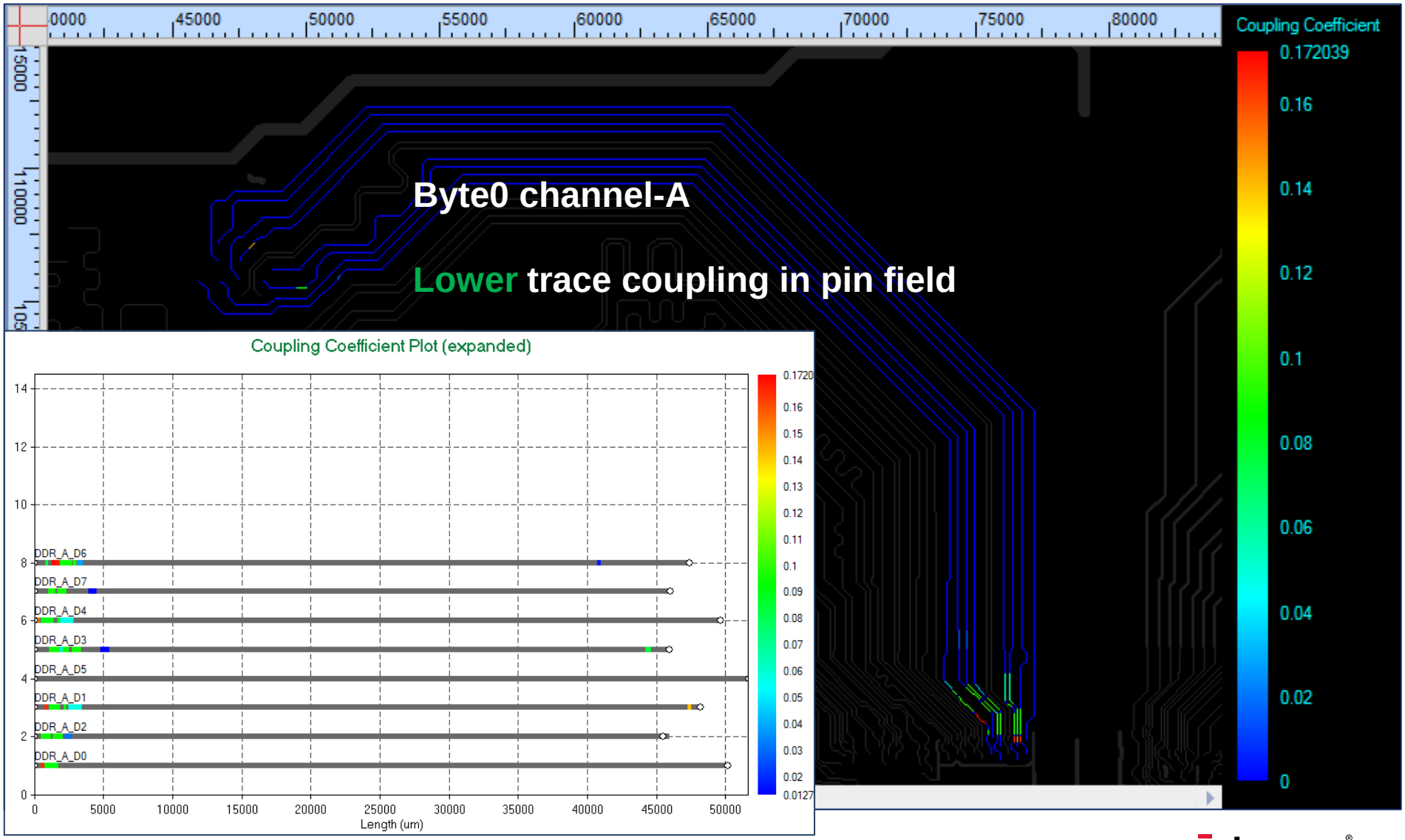
Byte0 channel-B

Longer high impedance trace in pin field



ERC/SRC example 1

ERC – DataA Byte0 coupling



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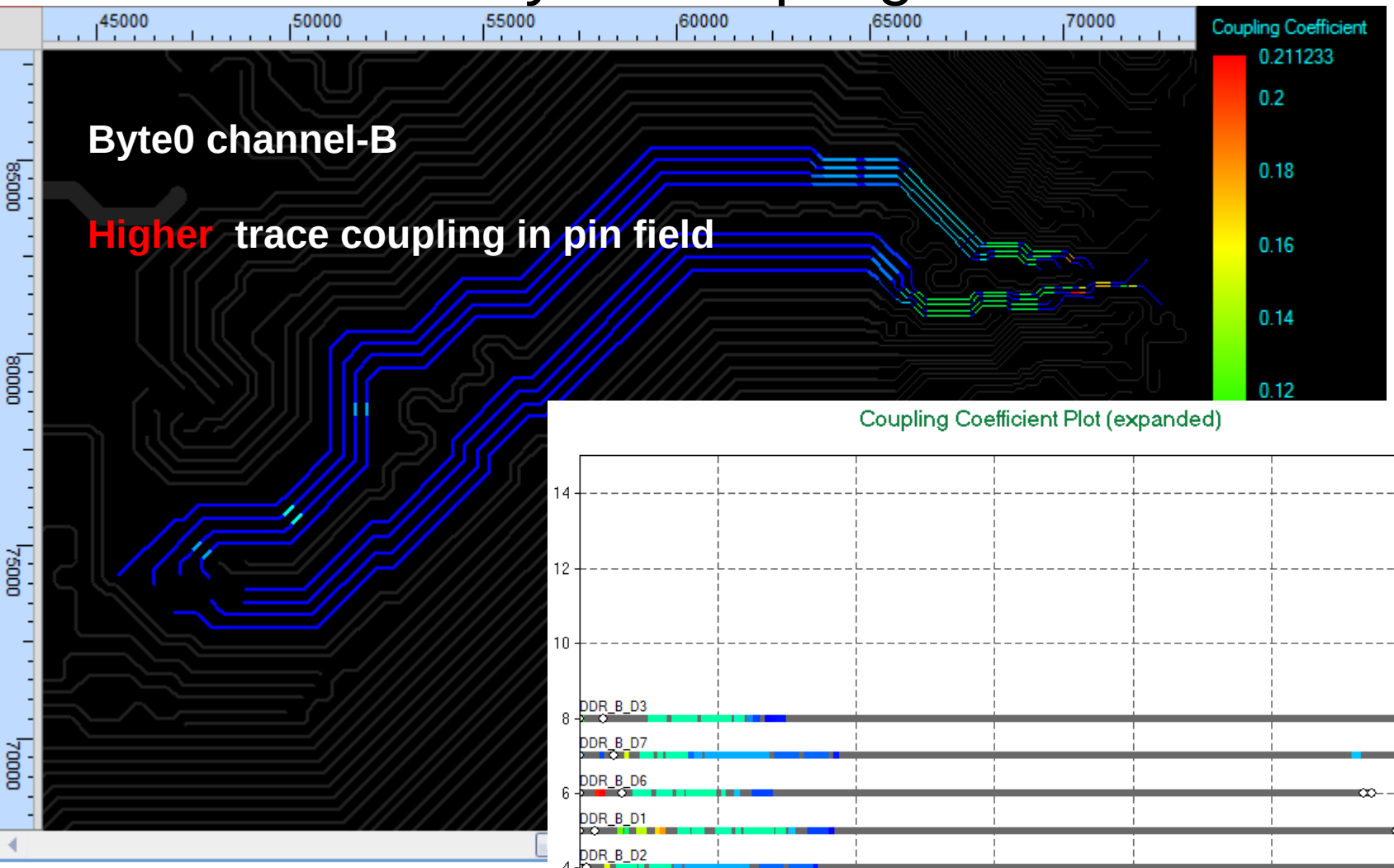
ERC – DataB Byte0 coupling



ERC/SRC example 1

ERC – # of vias

- DataA Byte0: 2 vias
- DataB Byte0: 4 vias

Net name	No. of vias
DDR_A_D0	2
DDR_A_D1	2
DDR_A_D2	2
DDR_A_D3	2
DDR_A_D4	2
DDR_A_D5	2
DDR_A_D6	2
DDR_A_D7	2

Net name	No. of vias
DDR_B_D0	4
DDR_B_D1	4
DDR_B_D2	4
DDR_B_D3	4
DDR_B_D4	4
DDR_B_D5	4
DDR_B_D6	4
DDR_B_D7	4

ERC/SRC example 1

ERC – # of reference discontinuities

- Comparable

Net count	Net name	No. of reference discontinuities	No. of no ref segments
29	**DDR_A_D0**	11	**0**
30	**DDR_A_D1**	8	**0**
31	**DDR_A_D2**	11	**0**
32	**DDR_A_D3**	9	**0**
33	**DDR_A_D4**	7	**0**
34	**DDR_A_D5**	13	**0**
35	**DDR_A_D6**	14	**0**
36	**DDR_A_D7**	7	**0**

Net count	Net name	No. of reference discontinuities	No. of no ref segments
138	**DDR_B_D0**	6	**0**
139	**DDR_B_D1**	9	**0**
140	**DDR_B_D2**	7	**0**
141	**DDR_B_D3**	6	**0**
142	**DDR_B_D4**	10	**0**
143	**DDR_B_D5**	11	**0**
144	**DDR_B_D6**	5	**0**
145	**DDR_B_D7**	10	**0**
146	**DDR_B_D8**	9	**0**

How to fix

To reduce the xtalk level of channel B Byte 0, user can consider one, or combination, of the following improvements

1. Via – reduce via number
2. Impedance – reduce the impedance discontinuities in pin field routing length
3. Coupling – reduce the coupling in pin field routing

ERC/SRC example 2

ERC → SRC
→ SI simulation

- To screen board and to identify worst case for further analysis
- To investigate SI impact of design rule violations and trade-offs

ERC ← SRC

- To find out how to fix SI problems shown in SRC simulation

ERC screening & sign-off
SRC screening & sign-off

- To compare against ERC/SRC results with
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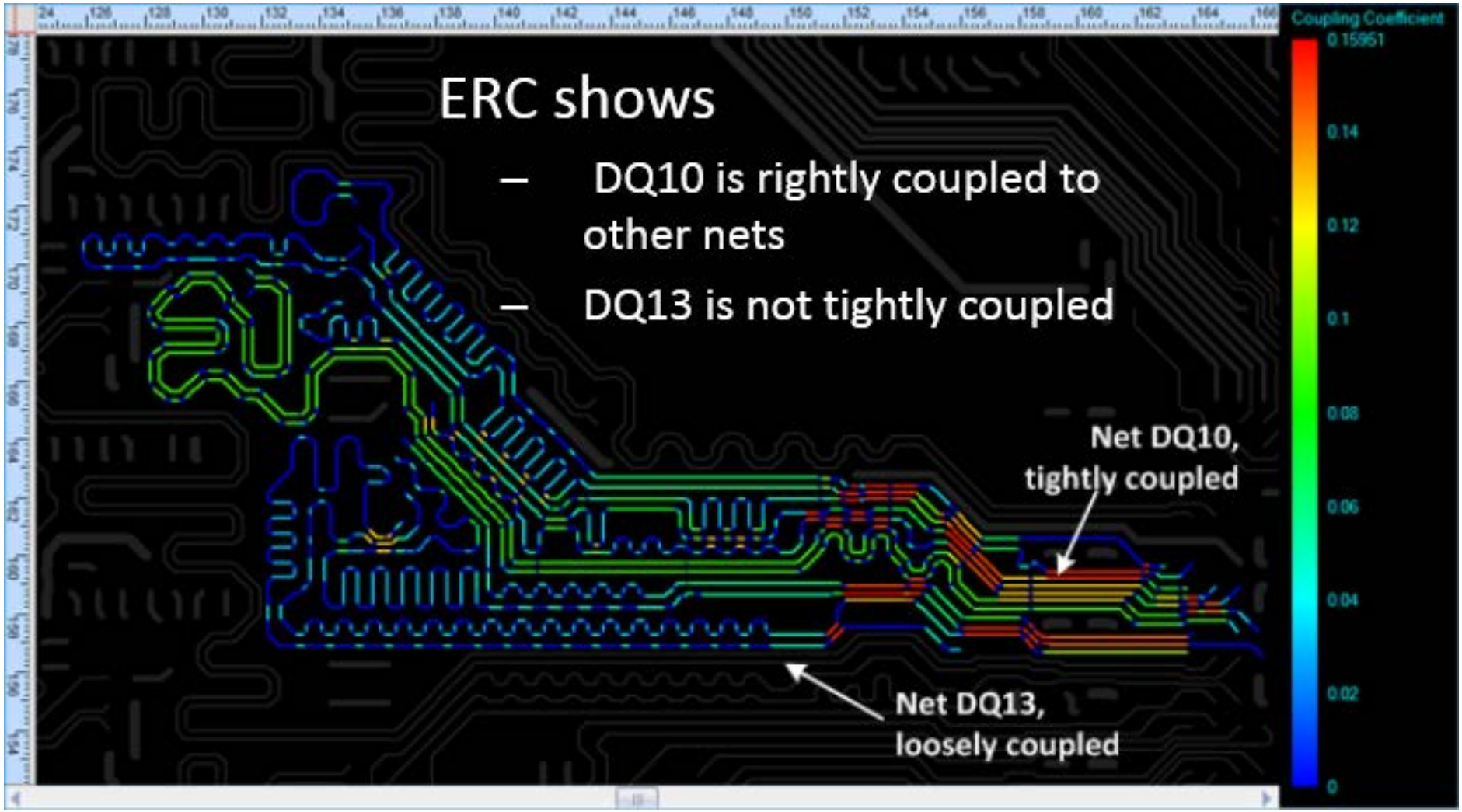
ERC/SRC example 2

ERC coupling results



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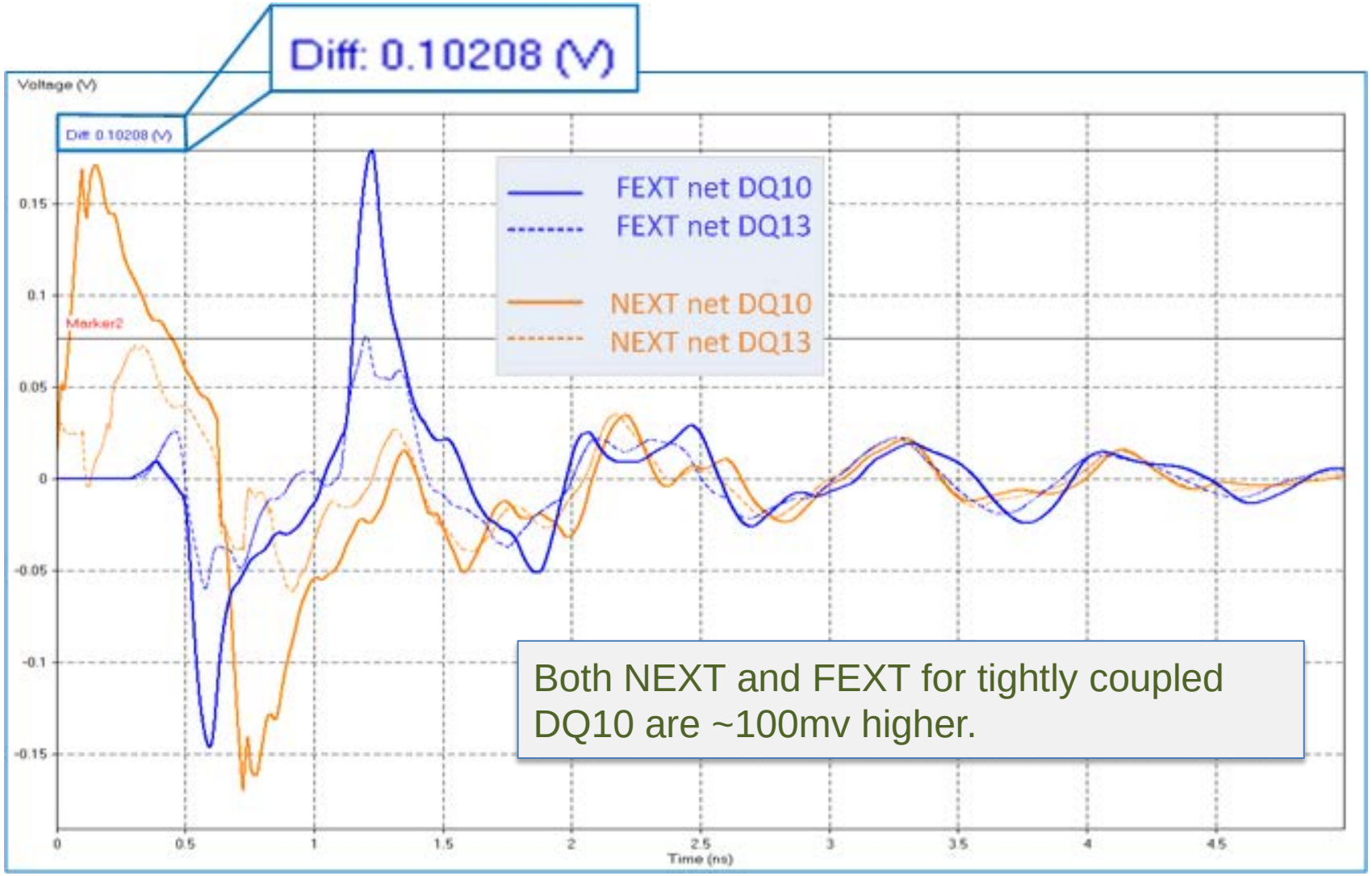
ERC/SRC example 2

SRC NEXT/FEXT waveforms



Both NEXT and FEXT for tightly coupled DQ10 are ~100mv higher.

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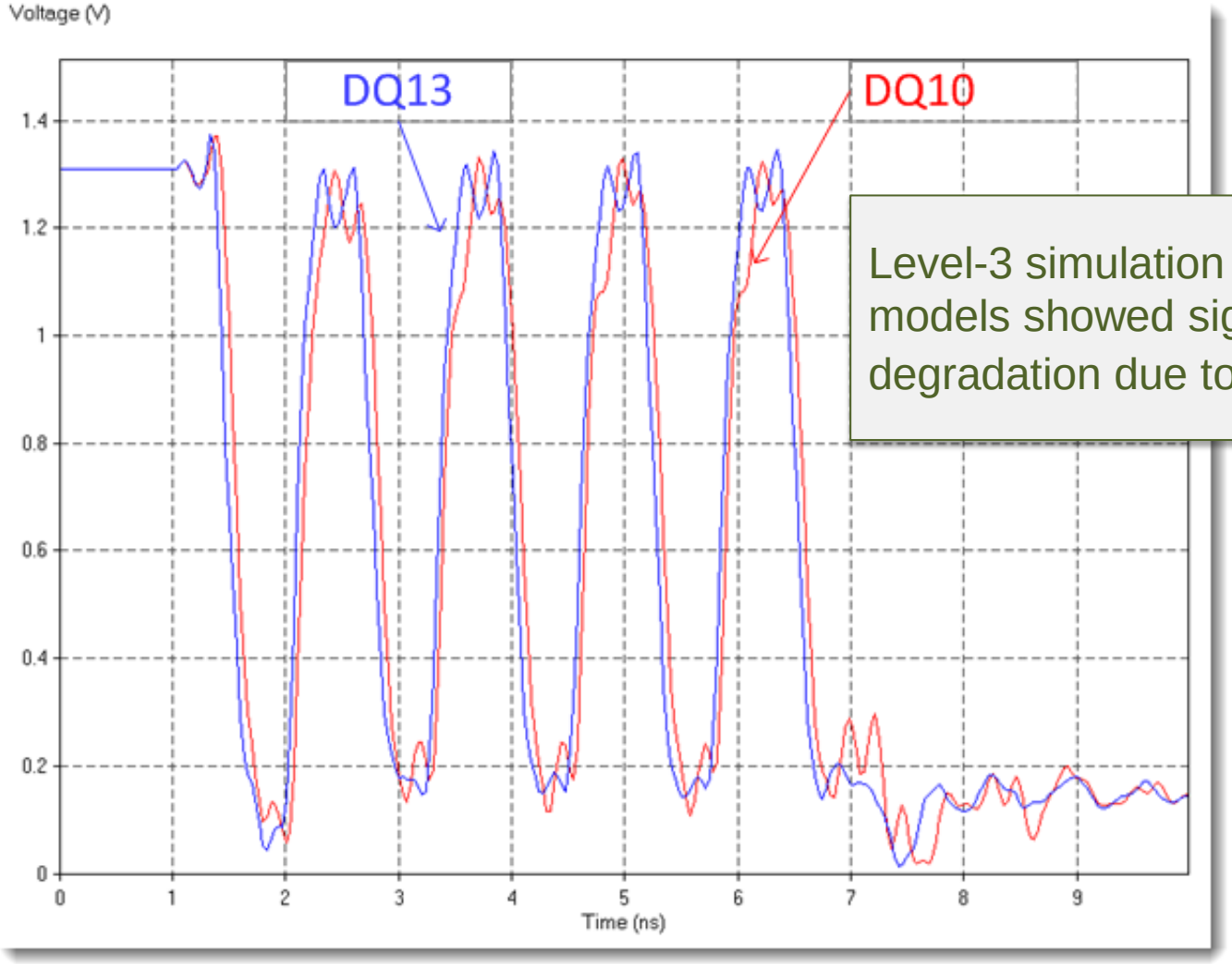
ERC/SRC example 2

Level-3 SI simulation using IBIS models



Level-3 simulation using ibis models showed signal degradation due to xtalk issues

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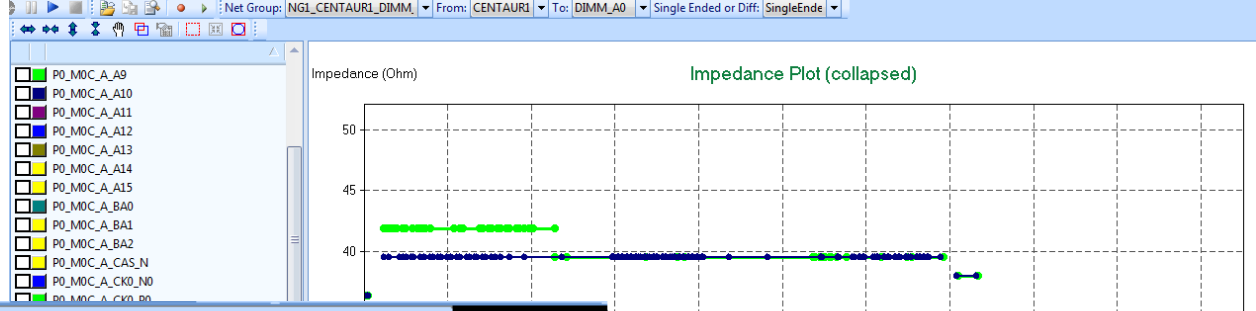
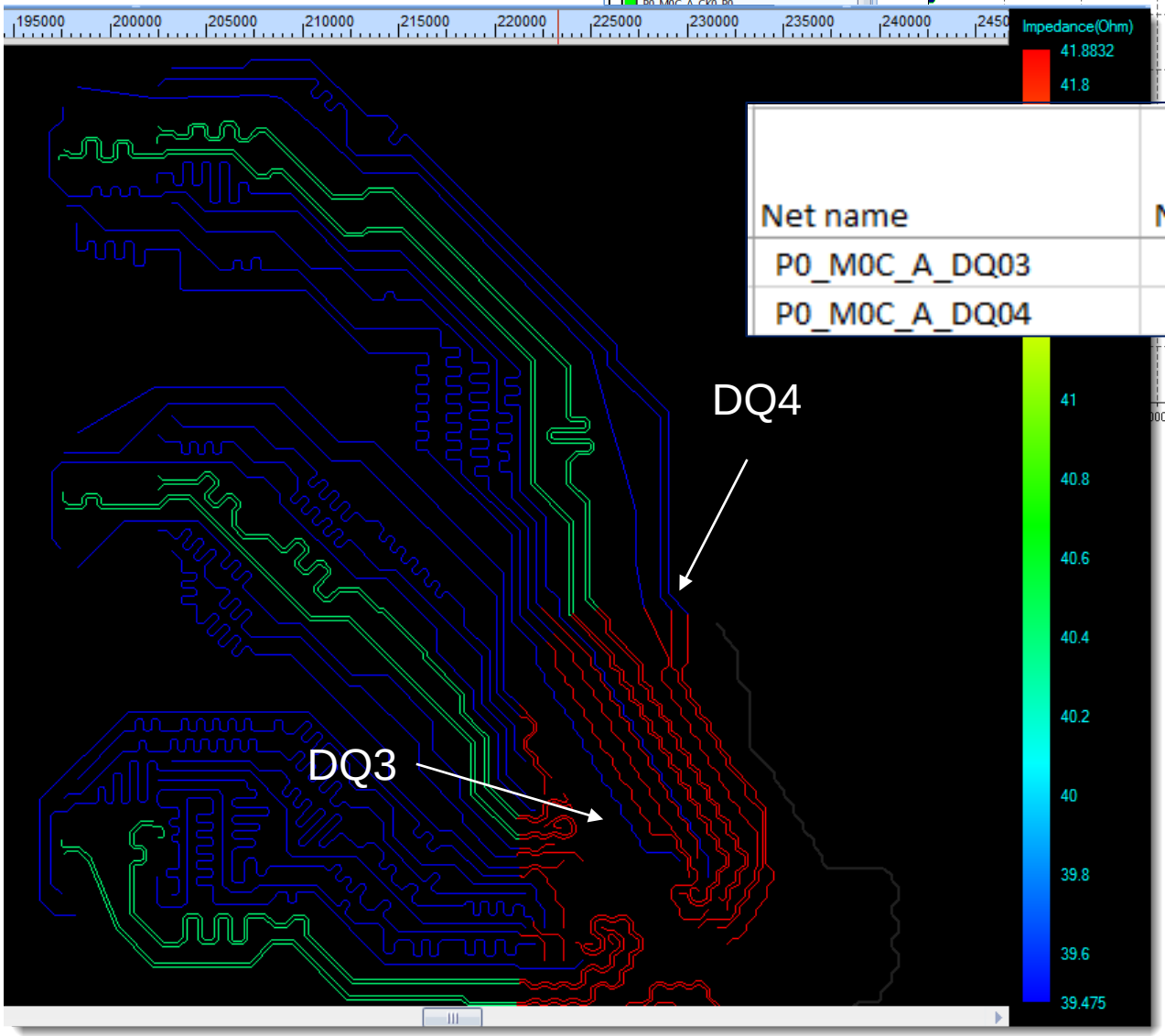
Application example 3

DQ3 vs. DQ4





Net name	NEXT Vmax (mv)	FEXT Vmax (mv) DIMM A
P0_M0C_A_DQ03	0	0
P0_M0C_A_DQ04	26	26

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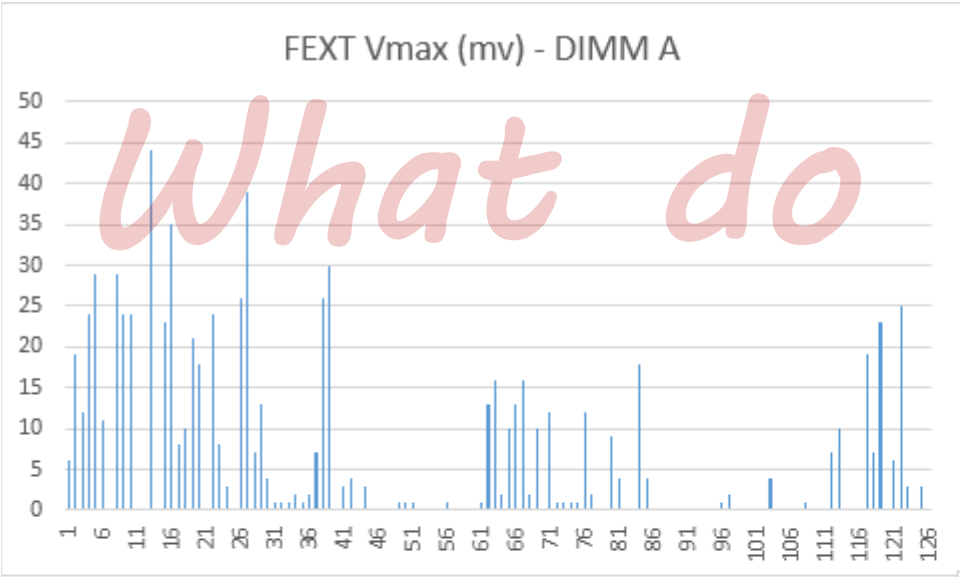
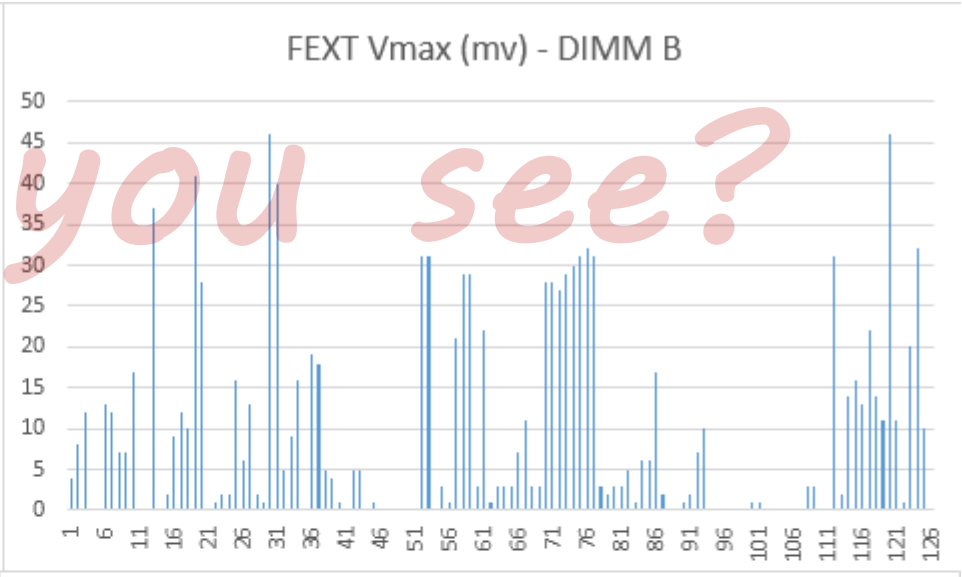
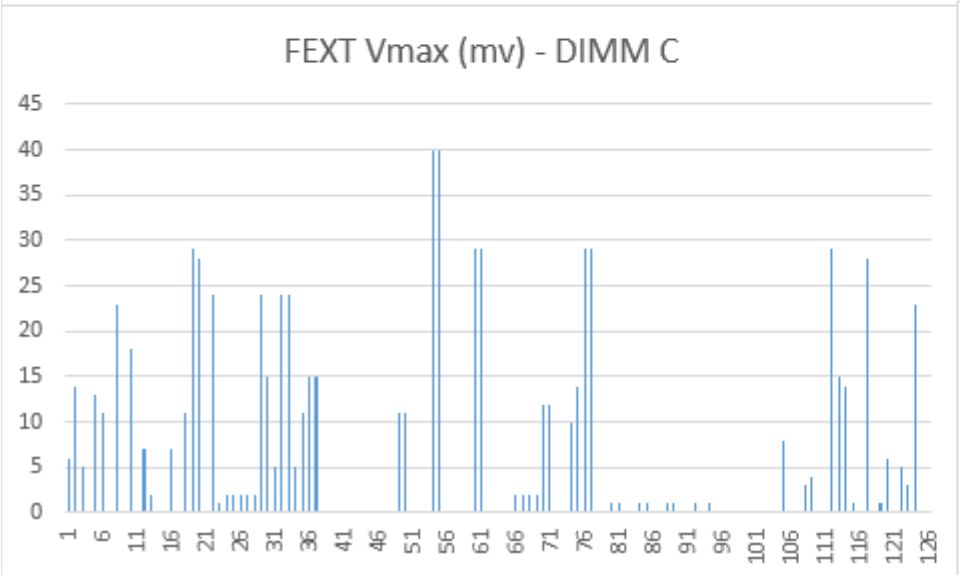
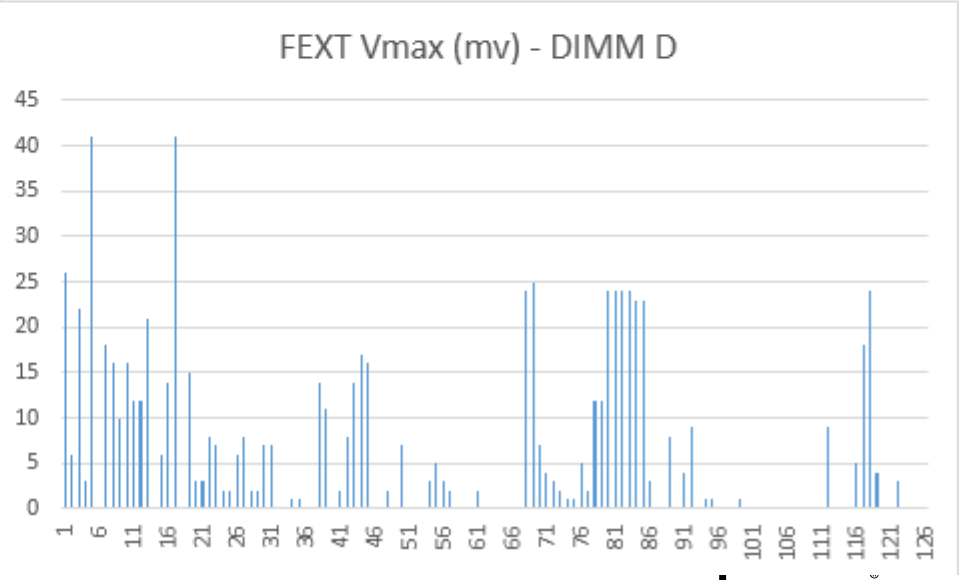
ERC/SRC example 3

FEXT results









What do you see?

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Topic 4

1. The gap between DRC and SI simulations is filled by Sigrity ERC/SRC
2. Demo
3. More ERC/SRC application examples
4. Conclusion

SRC net-level view → ERC's segment-level view

Sigrity SRC

- Layout SI macro view at net level
- All inclusive end results
- Shows what happened and its effect on performance

Sigrity ERC

- Layout SI micro level view at segment level
- Individual segmented results
- Shows why low performance happened and how to fix it


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