# Circuit Design / Simulation Requirement & Solution

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16 / Oct / 2015

OrCAD PCB Design Flow – Overview
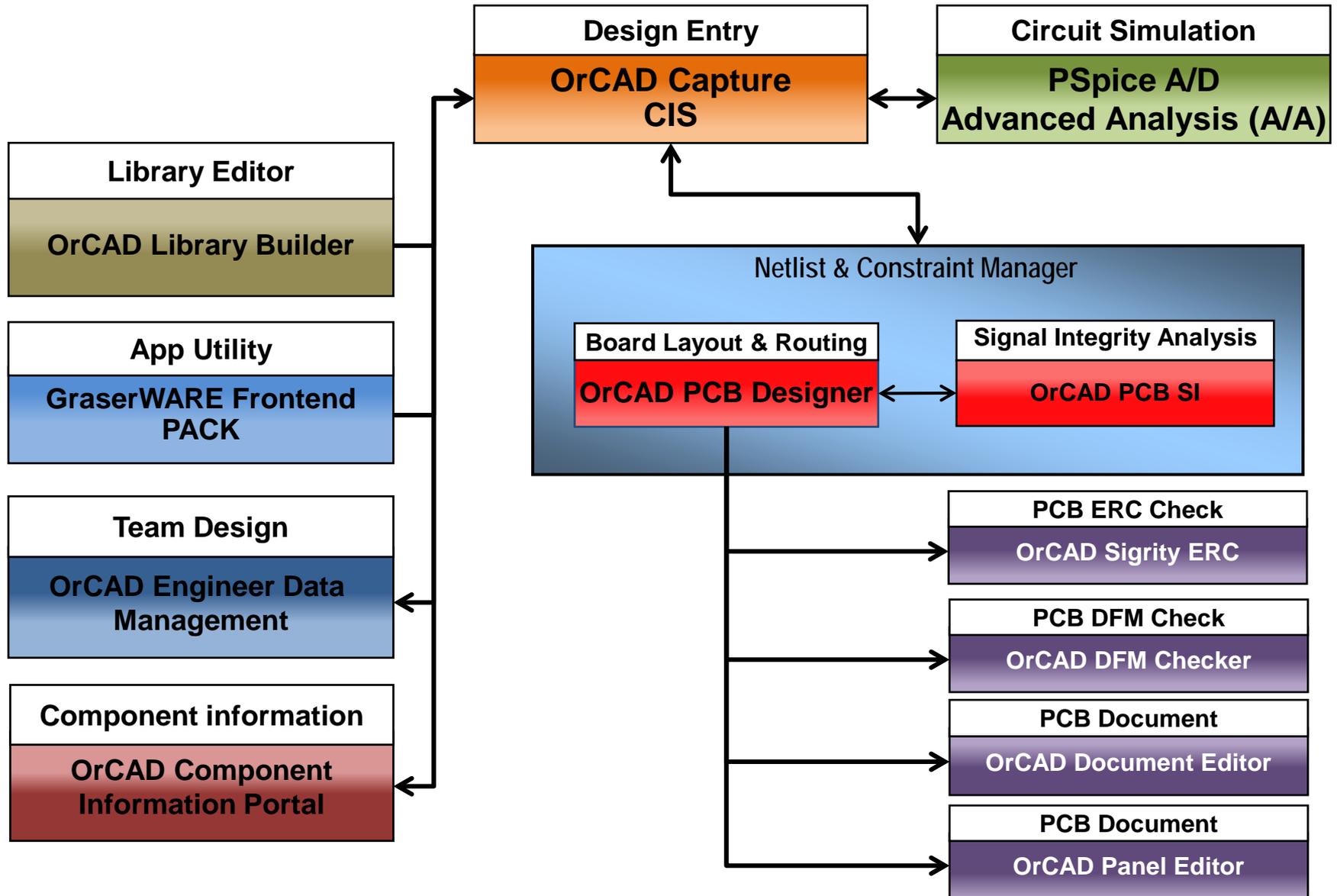
Topic

- OrCAD Capture / CIS What's New
- OrCAD Component Information Portal
- Circuit Design Challenges

OrCAD Capture / CIS What's New

# OrCAD Capture / CIS What's New

- Capture
  - View & Lite Mode Support
  - Schematic Page Name in Title Block
  - Mechanical Parts in Capture-Allegro Flow
  - Part Properties Display
  - Object Alignment in OrCAD Capture
 - Object Distribution in OrCAD Capture

OrCAD™
CADENCE PCB SOLUTIONS

OrCAD Capture CIS
version 16.6-2015

30th Anniversary Release

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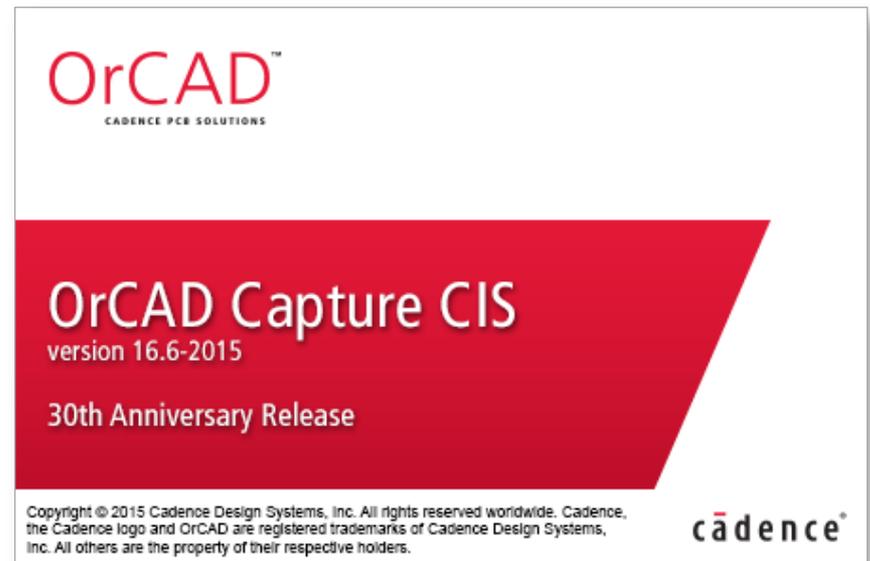
View & Lite Mode Support

- Capture new version support starts at view or lite mode
  - View mode : only preview schematic design
  - Lite Mode : more functions can be used
    - Search function
    - Part / Net properties preview
   - Full-featured operation under the limitations *(Lite Mode only)*
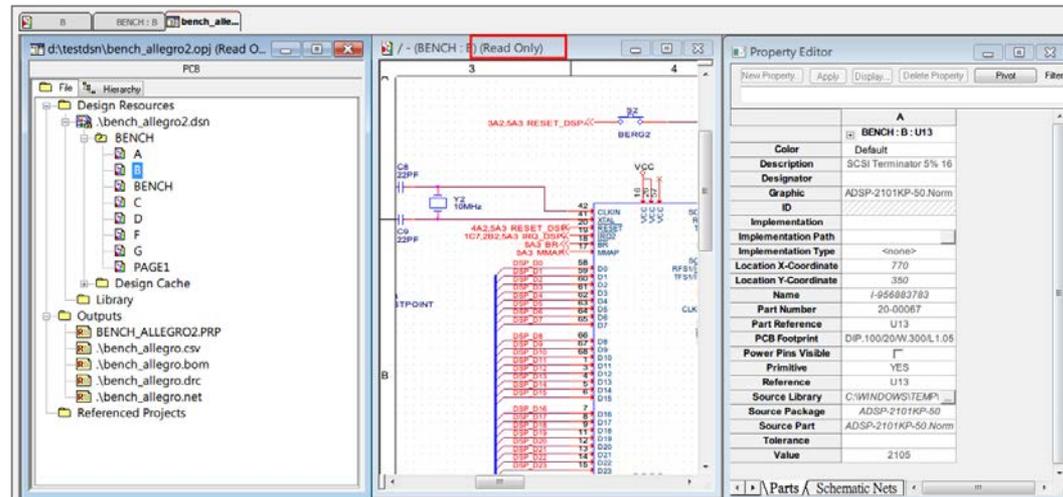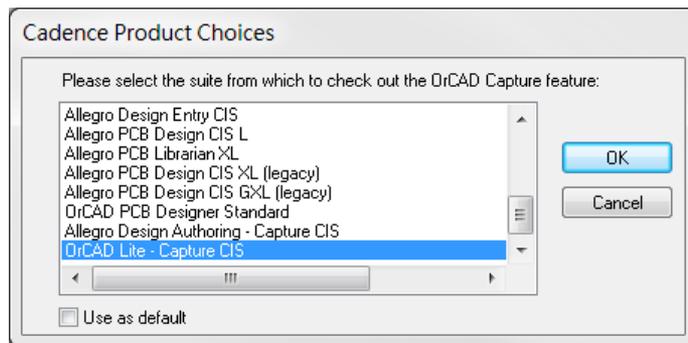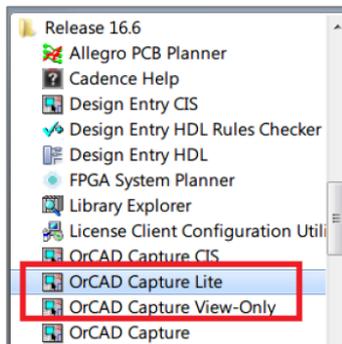
Schematic Page Name in Title Block

- Capture supports Schematic name and Page name on the title block property.

Mechanical Parts in Capture-Allegro Flow

- Capture supports zero pin mechanical part, mechanical holes, and fiducials in Capture - Allegro flow.

- Parts should have the property of CLASS=MECHANICAL.
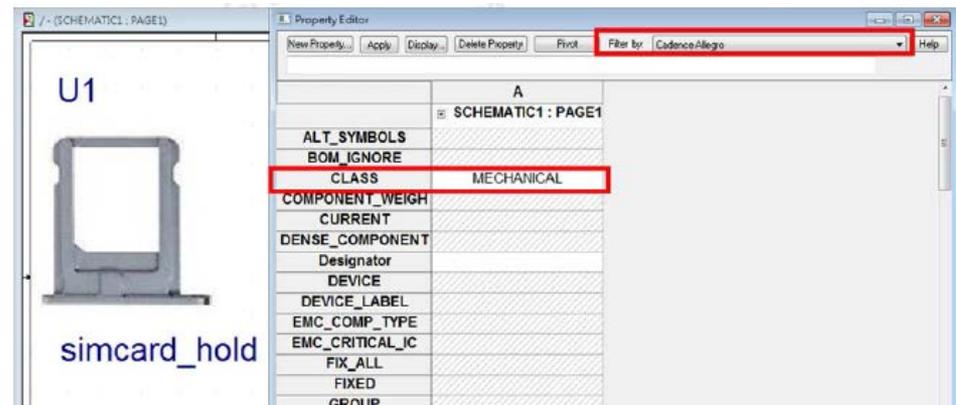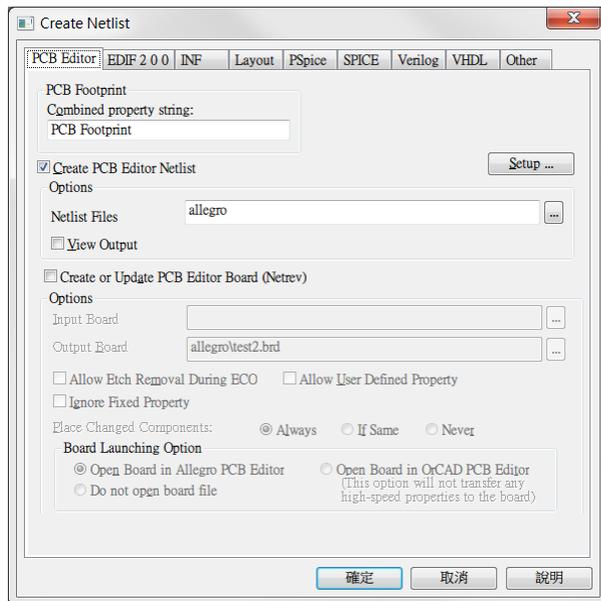
Part Properties Display

- New Display format in Display Properties dialog box
  - Value if Value Exists
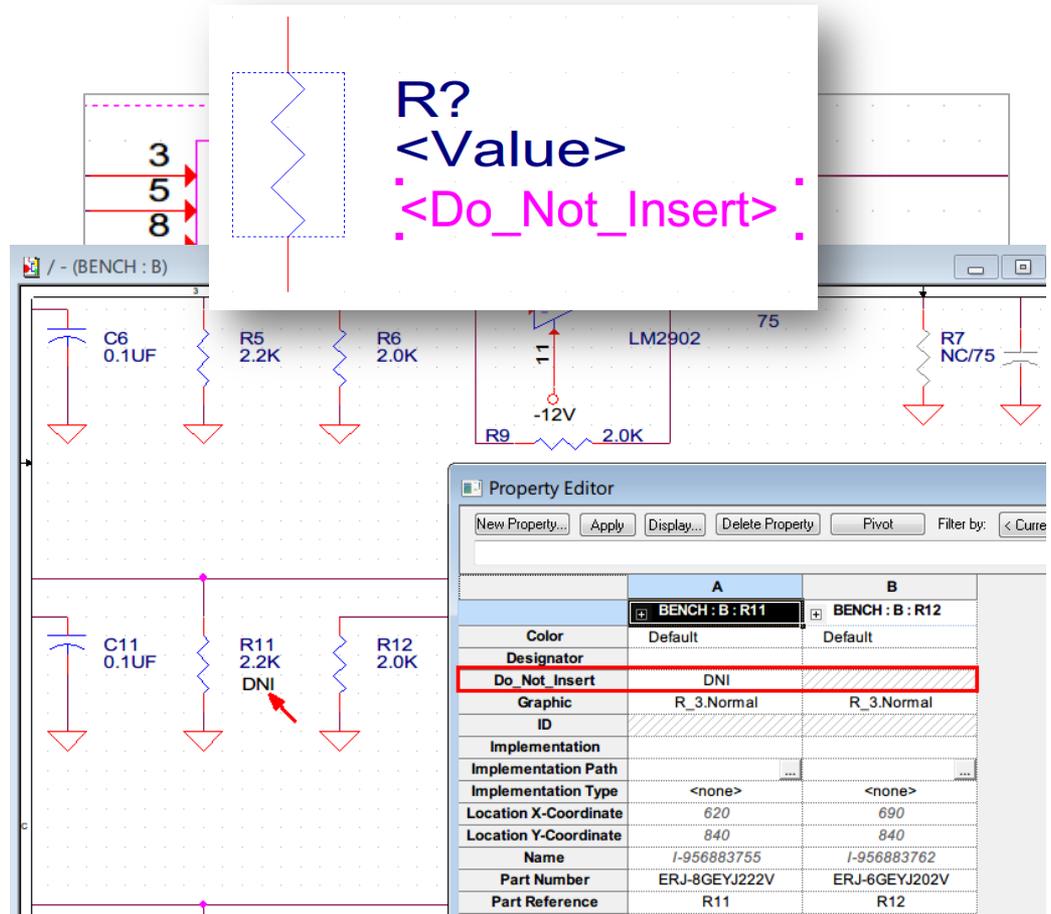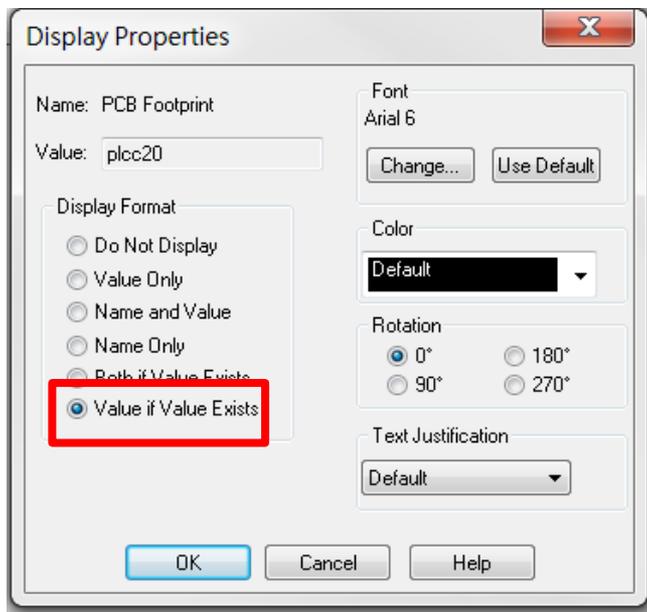
Object Alignment in Capture

- Alignment objects
  - Vertically (Top, Middle, and Bottom)
  - Horizontally (Left, Center, and Right)
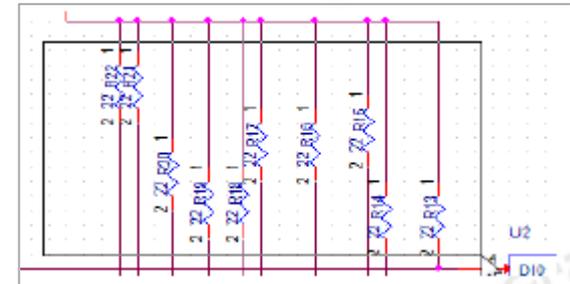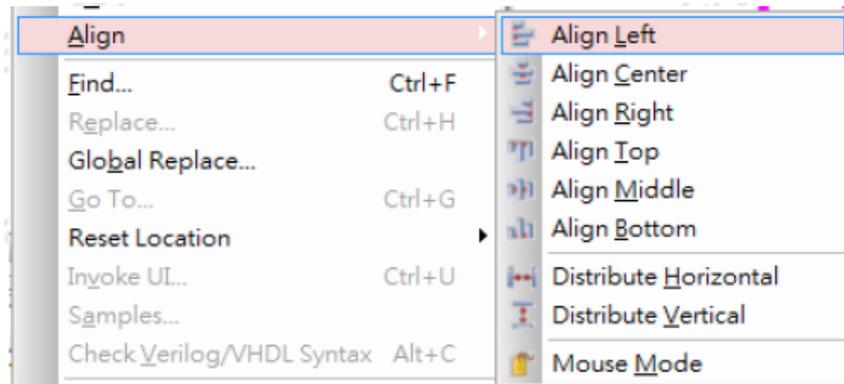
Object Distribution in Capture

- Distribute objects
  - Horizontally
  - Vertically
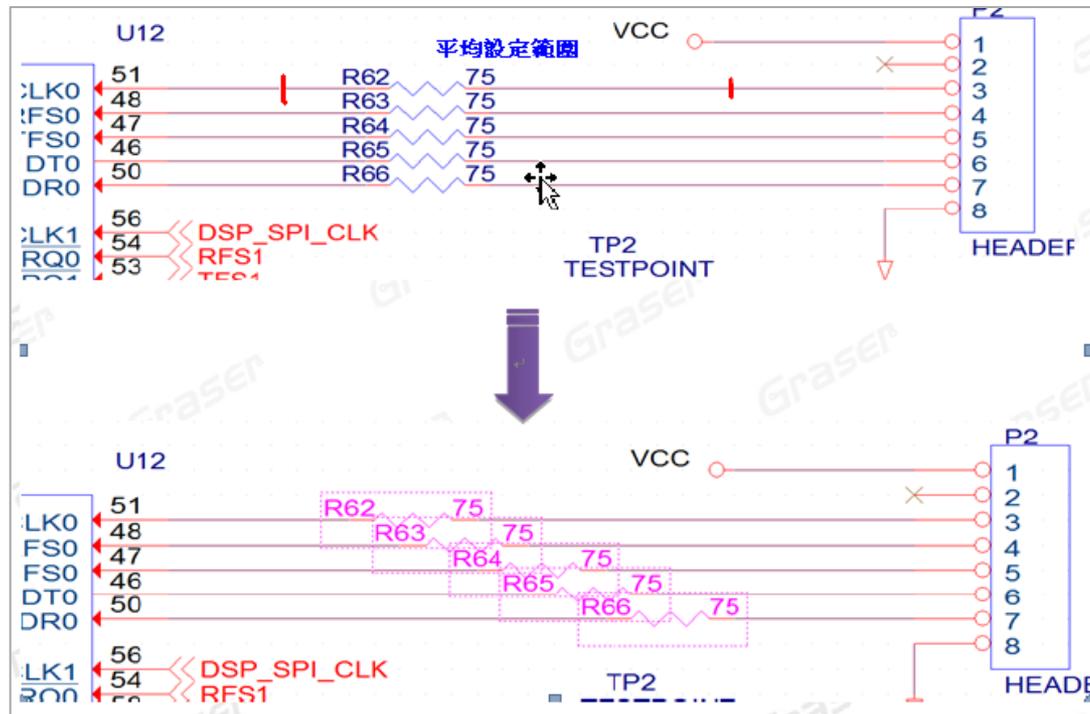
OrCAD Component Information Portal

Download Distributor Part Data

- Distributor integrations enable access to parametric data for millions of parts

- Get costing and availability data along with electrical characteristics

- Easily define multiple sources for your parts to avoid supply issues

Supported Distributors
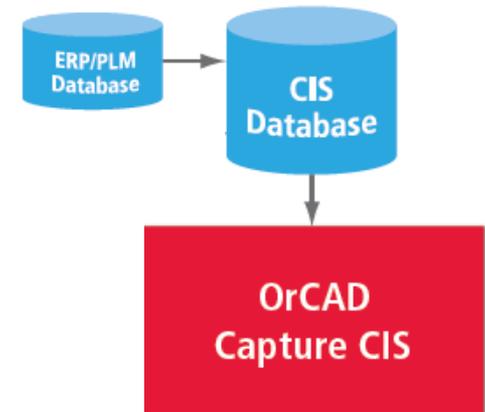
Integrated in OrCAD Capture

- CIP allows you to access and update component data without leaving Capture

New Part Introduction (NPI) Flow

- Add new parts in a controlled fashion

- CIP will flag the part and will send notifications to defined users who need to review and approve the part

- Engineers can use the part as a temp part in their design

- When the part is approved/rejected, part status will updated in engineers' view as well

PART_NUMBER	TMP-2
Description	CAP, Ceramic, SMD, 0.01 uF, 10 %, 5(
PCB Footprint	CAPC1608X87N
Number of Pins	2
Operating Temperature Minimum	-55 C
Package Height	0.87 mm
Company Part Status	Not Yet Approved
Equivalent Series Resistance	
Tolerance	10%
Implementation	
PSpiceTemplate	C^@REFDES %1 %2 C^@REFDES 0.01uF
CLASS	DISCRETE

New Part Introduction (NPI) Flow

- Temporary Part Flow promoting concurrency

New Part Introduction (NPI) Flow

- Capture CIS updates part status to synchronize Part_Number.

Circuit Design Challenges

Circuit Design Challenges

- ## How to Know
    - Circuit design parts with library pin difference?
    - Part status with database?
    - Capacitor de-rating of net voltage?

OrCAD Tcl / Tk Utilities

- Part Library Check Utility

- Design Part Check Utility

- Capacitor De-rating Check Utility

Part Library Check Utility

- Schematic Symbol & Footprint Check With Library (Database)
  - Library Symbol Pin Check
  - Footprint Name Check
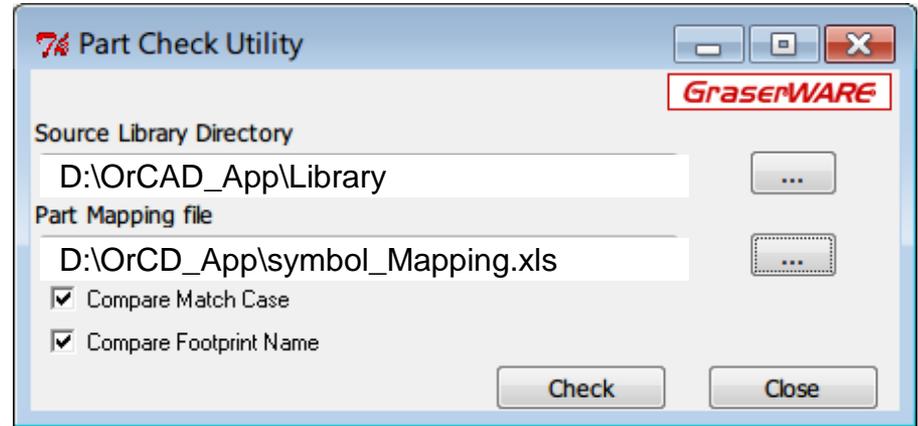
|	1	2	3	4	5
1	Part Number(SCH)	Part Reference(SCH)	Pcb FootPrint(SCH)	Pcb FootPrint(DB)	Check
30	80-00042	XT2	SCRY2_4D1X1D5XD85	SCRY2_4D1X1D5XD9	Failed
31	80-00043	Q25,Q6	SOT23	SOT23_1	SOT23
32	80-00044	U57	SOP8_1D27X6X1D75	SOP8_1D27X6X1D75_AO4413	SOP8_1D27X6X1D75
33	70-00002	9,U60,U95	SO8_MOS_1	DFN6_5D15X6D15X1D2_2	SO8_MOS_1
34	70-00003	G1	ESDSTRIP		Failed
35	70-00004	TP237,TP238	STP_RT30x50	STP_RT30x50	Pass
36	70-00005	H1,H10,H11,H12,H13			
37	70-00006	GCAP1			
38	70-00007	TP100,TP101,TP102,T			
39	80-00043	CPU1			
40	60-00006	LED10,LED9			
41	40-00007	CN8			
42	40-00008	CN4			
43	40-00009	J1,J4			
44	40-00010	CN12,CN13			

Library Compare | Footprint Compare

	1	2	3	4	5	6	7	8	9
1	Part Number(SCH)	Part Reference(SCH)	Schematic Part(SCH)	Pin Count(SCH)	Schematic Part(DB)	Pin Count(DB)	Pin Count Check	Pin Name Check	
398	80-00043	U59,U60,U95	BSC042N03LSG_2		N_MOS_5P_GSDZ_0	5		Failed	could not found library part
399	80-00044	PQ359,PQ509,Q400,Q4	N_MOS_0_A		N_MOS_0_A	3	Match	Match	
400	70-00002	Q1,Q20,Q21,Q22	2N7002		2N7002	3	Match	Match	
401	70-00003	Q10,Q11,Q12,Q124,Q13	2N7002		2N7002	3	Match	Source Package different from Sc	
402	70-00004	Q16	MOS_P0		P_MOS_SOT-23_0_A	3	Match	Failed	
403	70-00005	PQ210,PQ230,PQ250,PC	MOS_SON-8-N2_DUA		MOS_SON-8-N2_DUAL-N	8	Match	Match	
404	70-00006	G1	CPCI-ESD-STRIP		CPCI-ESD-STRIP	3	Match	Failed	
405	70-00007	TP237,TP238	TP-2		TP-2	1	Match	Match	
406	80-00043	H1,H10,H11,H12,H13,H	HOLE_B		HOLE_B	1	Failed	could not found library part	
407	60-00006	GCAP1	EECEN0F204AK		EECEN0F204AK	2	Match	Match	
408	40-00007	TP100,TP101,TP102,TP	TP-2		TP-2	1	Match	Match	
409	40-00008	TP31,TP32,TP33,TP34,T	TP-2		TP-2	1	Match	Match	
410	40-00009	CPU1	HASWELL_BGA_EL		HASWELL_BGA_EL_15	1364	Match	Match	
411	40-00010	PCH1	HASWELL_BGA_EL	695			Failed	Source Package different from Sc	
412	40-00011	PJP210,PJP211,PJP230,J	HASWELL_BGA_EL	2			Failed	Source Package different from Sc	
413		TP1,TP10,TP11,TP12,TI	HASWELL_BGA_EL	1			Failed	Source Package different from Sc	

Design Part Check Utility

- ## How to know Design Part
  - Life cycle
  - End of life

Components De-rating Check Utility

- ## Design Component De-Rating Check
  - – Capacitor
  - – Resistor
  - – Inductor
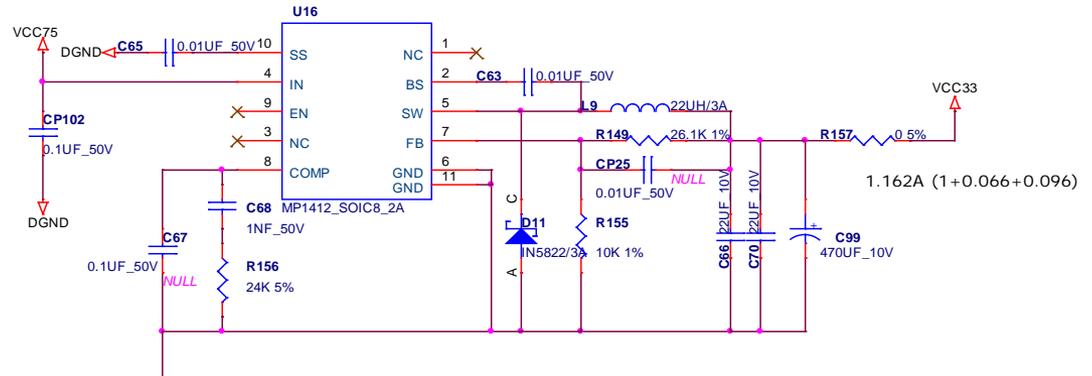
	1	2	3	4	5	6	7	8	9
1	Item	Part Number	Reference Part	Description	Component Specification(Watt, A, V)	Application(Watt,A,V)	De-rating(%)	Judge(C<=50%,L<=80%,R<=50)	Remark
2	1	26-401-928102	C1	Wire Wound	2KV	0V	0.00%	Pass	
3	2	26-401-121106	C169	Wire Wound	50V	21V	42.00%	Pass	
4	3	25-502-907477	C18	Wire Wound	35V	23.6V	67.43%	Failed	
5	4	25-502-907477	C19	Wire Wound	35V	23.6V	67.43%	Failed	
6	5	26-401-928102	C2	Wire Wound	2KV	25V	1.25%	Pass	
7	6	25-502-907477	C20	Wire Wound	35V	23.6V	67.43%	Failed	
8	7	26-400-121332	C206	Wire Wound	50V	1.5V	3.00%	Pass	
9	8	26-401-121106	C207	Wire Wound	50V	21V	42.00%	Pass	
10	9	25-502-907477	C21	Wire Wound	35V	23.6V	67.43%	Failed	
11	10	26-401-928102	C5	Wire Wound	2KV	25V	1.25%	Pass	
12	11	25-502-907477	C6	Wire Wound	35V	23.6V	67.43%	Failed	
13	12	26-400-121103	C63	Wire Wound	50V	0V	0.00%	Pass	
14	13	26-400-121103	C65	Wire Wound	50V	0V	0.00%	Pass	
15	14	26-403-404226	C66	Wire Wound	10V	3.3V	33.00%	Pass	
16	15	26-400-021102	C68	Wire Wound	50V	0V	0.00%	Pass	
17	16	25-502-907477	C7	Wire Wound	35V	23.6V	67.43%	Failed	
18	17	26-403-404226	C70	Wire Wound	10V	3.3V	33.00%	Pass	

工作表1 / 工作表2 / 工作表3

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2015
**User
Conference**
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Circuit Simulation Requirement & PSpice Simulation Solution

Circuit Simulation Requirement & PSpice Simulation Solution

- ## Why PSpice
  - – The Circuit Design Verification Challenge

- ## PSpice Solution
  - – Cadence OrCAD Design Solution Integration
  - – Mixed-Signal, Mixed Language and Mixed Domain Integrative Simulator
  - – PSpice Modeling Application
  - – Quality & Speed Performance

Why PSpice

The Circuit Design Verification Challenge

- **Design Trends**
  - Miniaturization
  - Complexity
  - Visualization Interfaces
  - Interconnected Systems

IOT

Medical

Automotive

Computing

Consumer Electronics

The Circuit Design Verification Challenge

- ## Design Verification Challenges
  - Power Management
  - Embedded Software
  - Digital Control Systems
  - Mixed Signal Designs
  - Use red when emphasizing words
  - High Speed & Performance
  - Quality

What's EDA TOOL supporting it ?

Product Creation

Design and Analysis

Constraint Driven PCB Design

Supply Chain Collaboration

Electrical Verification and Signoff

Concept

Co-Design and Co-Analysis

PSpice Solution

Cadence OrCAD Design Solution Integration

- Powerful and Widely Used Design Solution
  - Fast and intuitive schematic design entry, OrCAD Capture
  - Powerful component data management, OrCAD Capture CIS
  - Full-featured Mixed-Mode simulator, PSpice
  - Comprehensive PCB solution, OrCAD PCB Designer
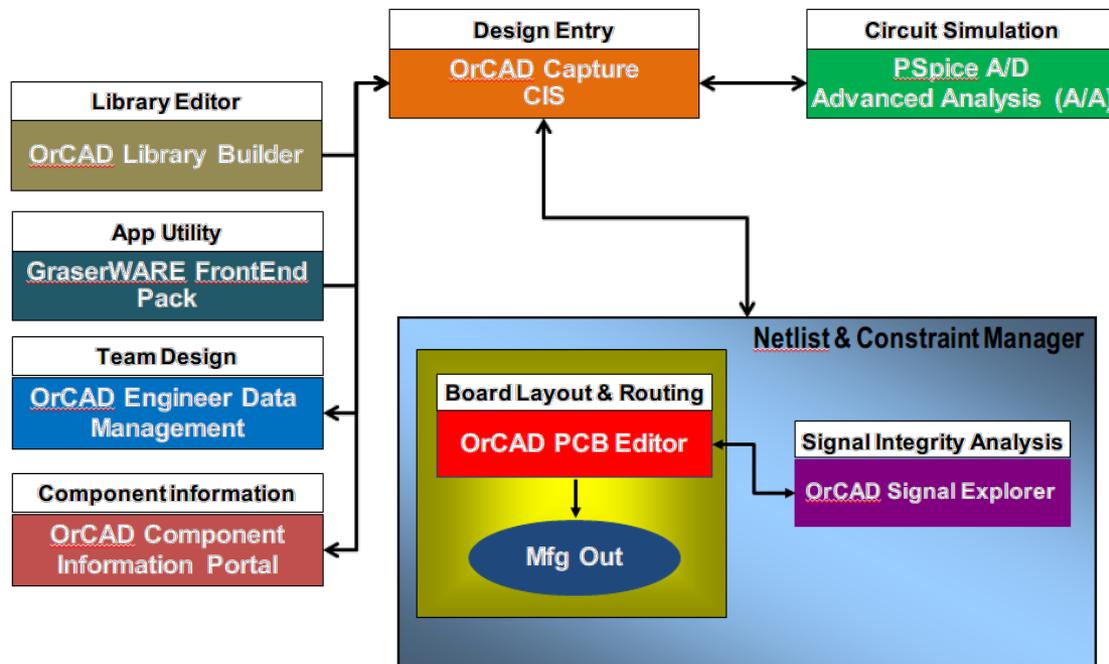
Mixed-Signal, Mixed Language and Mixed Domain Integrative Simulator

- PSpice
  - Integrates seamlessly with OrCAD Capture/ OrCAD Capture CIS
  - Fast, accurate analysis of analog and mixed-signal designs
  - Advanced analysis to increase performance and productive yield
  - Numerous PSpice model libraries
  - Supports C/C++, SystemC and Verilog-A
  - Various types of modeling creation
  - Co-simulation with MATLAB Simulink
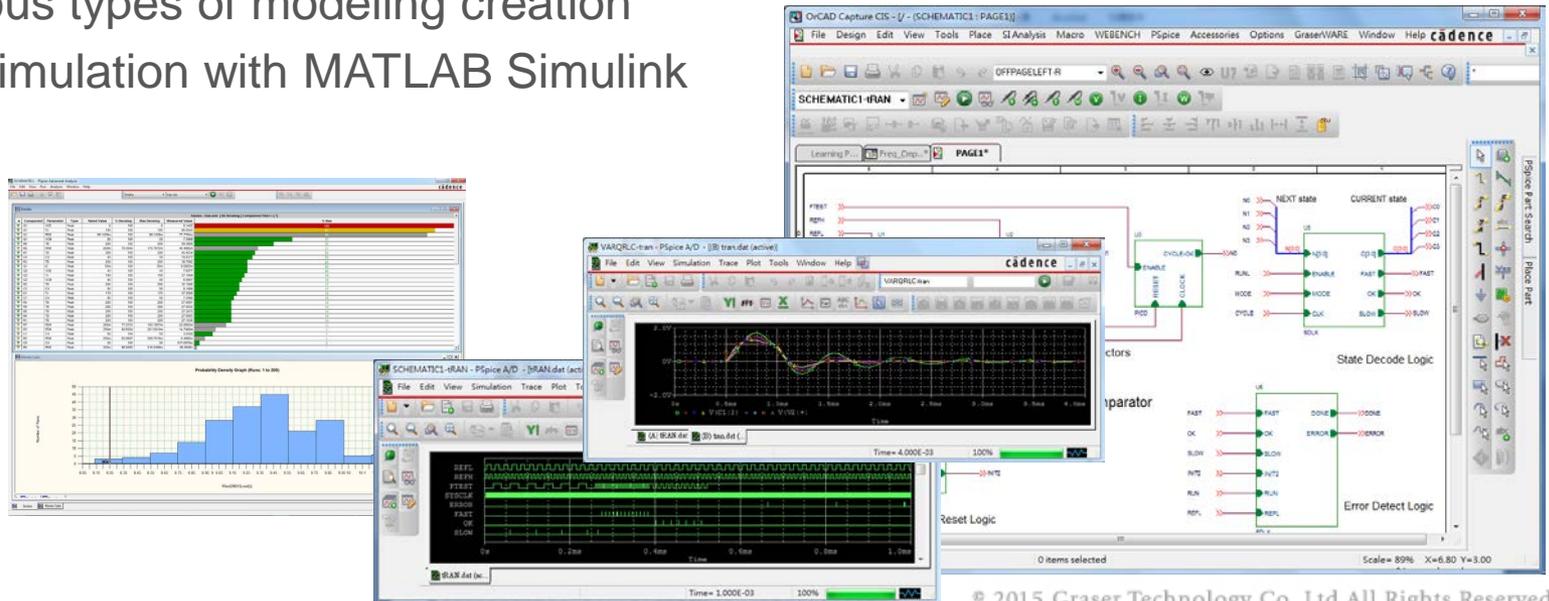
Mixed-Signal, Mixed Language and Mixed Domain Integrative Simulator

- ## PSpice Mixed Language Circuit Simulation
  - – Hardware/Software Co-Simulation
  - – Supports C/C++, SystemC and Verilog-A
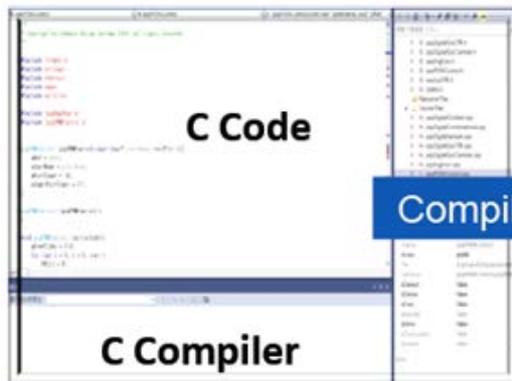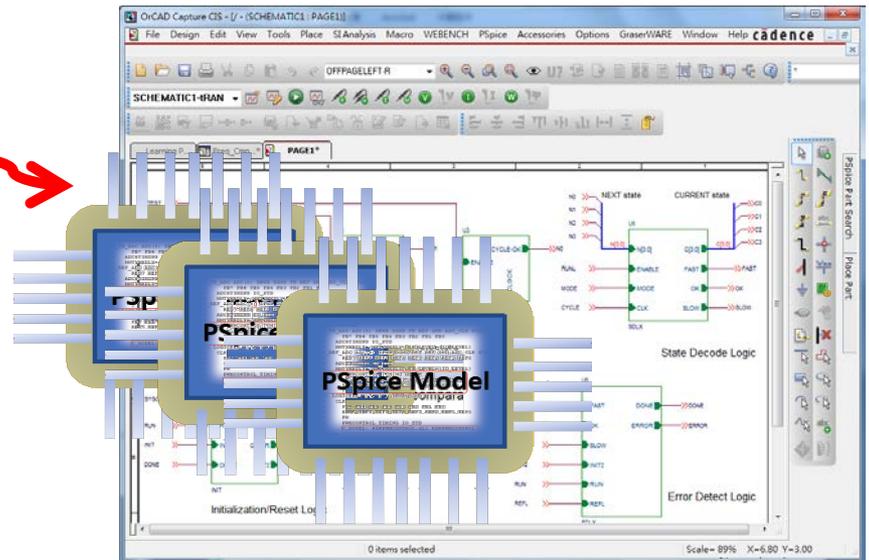
Mixed-Signal, Mixed Language and Mixed Domain Integrative Simulator

- ## PSpice Mixed Domain Integration
  - Systems Simulation
  - Integration with MATLAB Simulink brings two industry-leading simulation tools, electromechanical & electrical systems in a co-simulation environment.
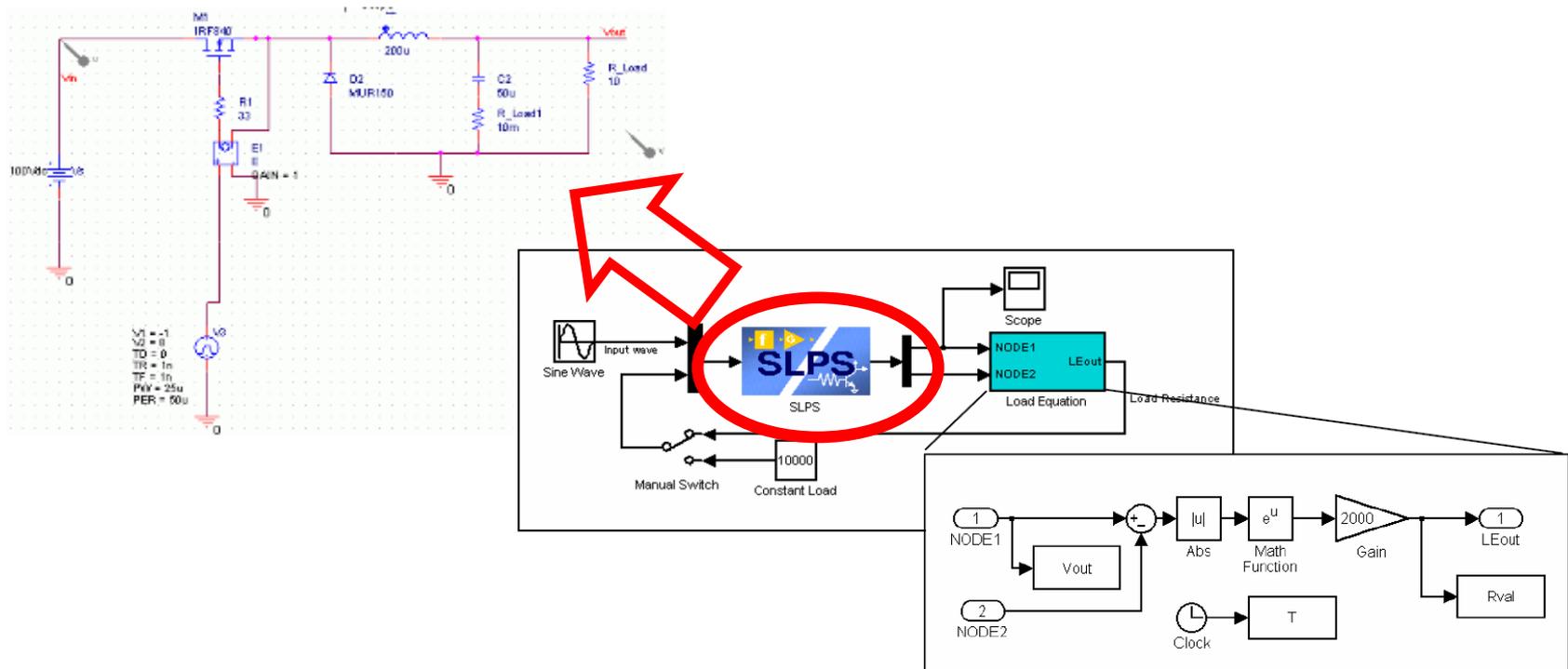
PSpice Modeling Application

- Quick & Easy methods to create and edit PSpice models
  - No Library Setup required in OrCAD Capture/Capture CIS schematic
  - Using parametric extraction algorithms
  - Edit existing PSpice instance properties
  - Device Type, Capacitor/Inductor/Transformer/Zener/Switch/TVS/VCO/LED
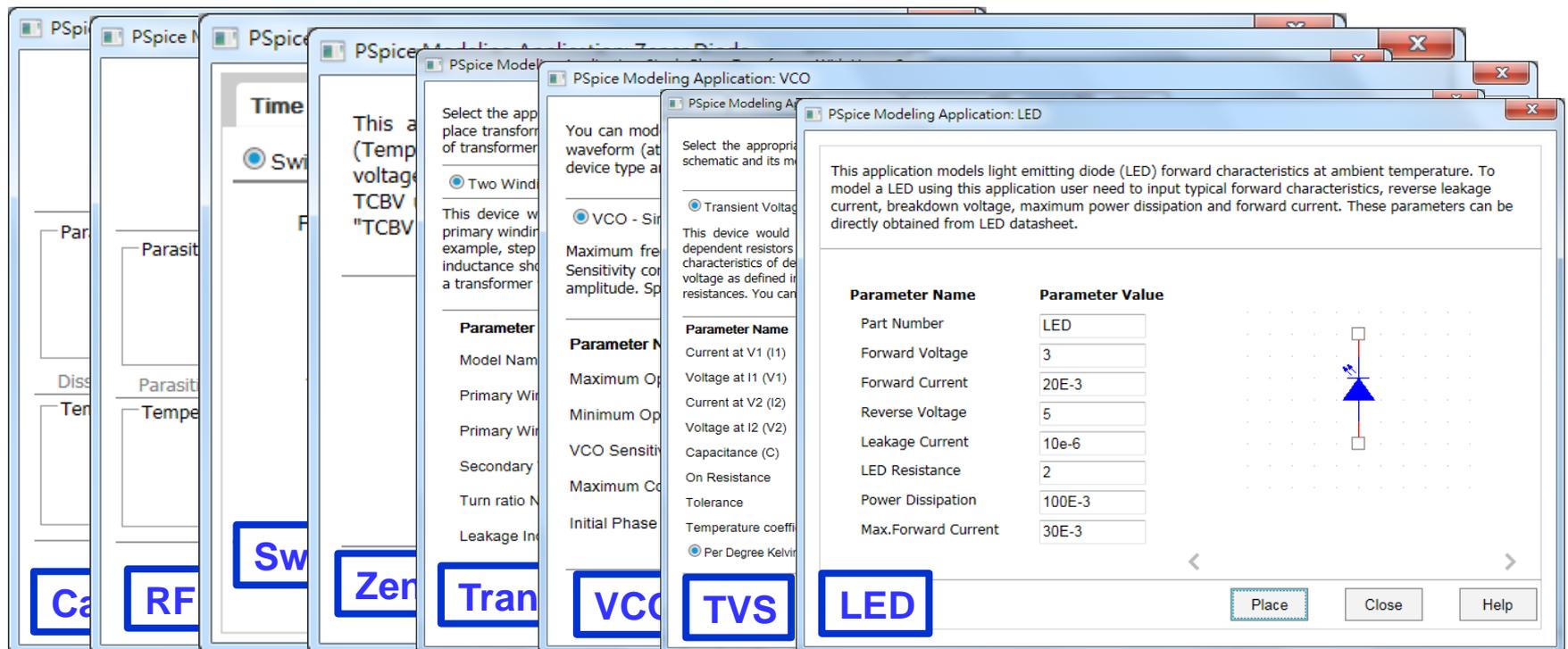
PSpice Modeling Application

- ## PSpice Sub-circuit Generation from IBIS Models
  - New IBIS Import supports for V-I curves and V-T curves.
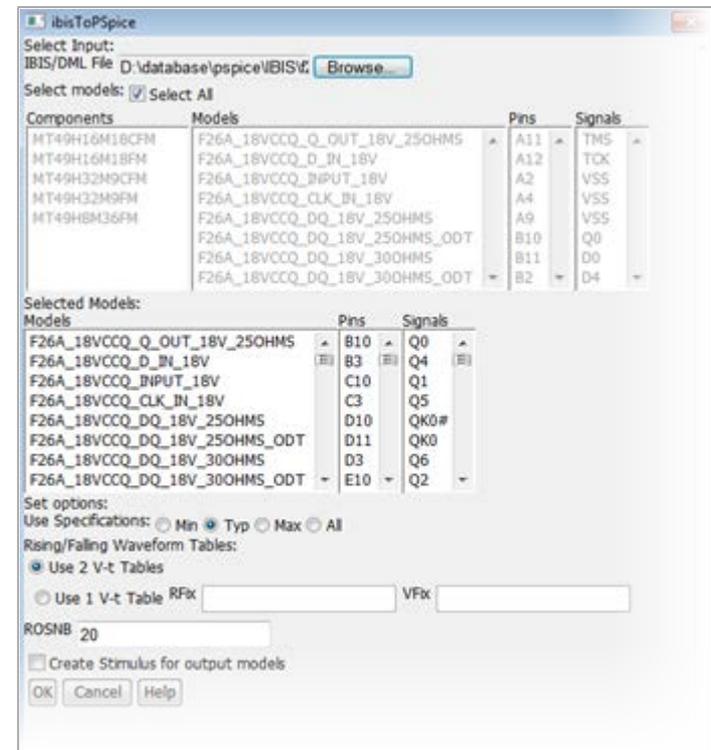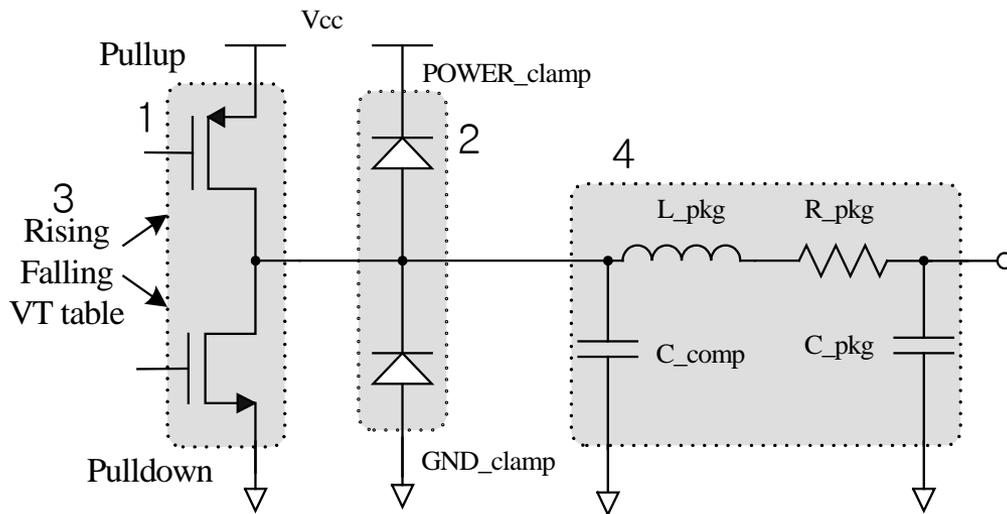
PSpice Modeling Application

- PSpice existing model library models
  - Offers more than 30,000 analog and mixed-signal models.
  - PSpice library includes parameterized models such as BJTs, JFETs, MOSFETs, IGBTs, SCRs, discretes, operational amplifiers, optocouplers, regulators, PWM controllers, and multipliers.

PSpice Modeling Application

- Get PSpice Models from device vendors / manufacturers

PSpice Modeling Application

- ## PSpice modeling service company
  - Supply every PSpice model
  - Passive components, capacitor, inductor, resister, transformer, connector, cable, FPC Line, and so on.
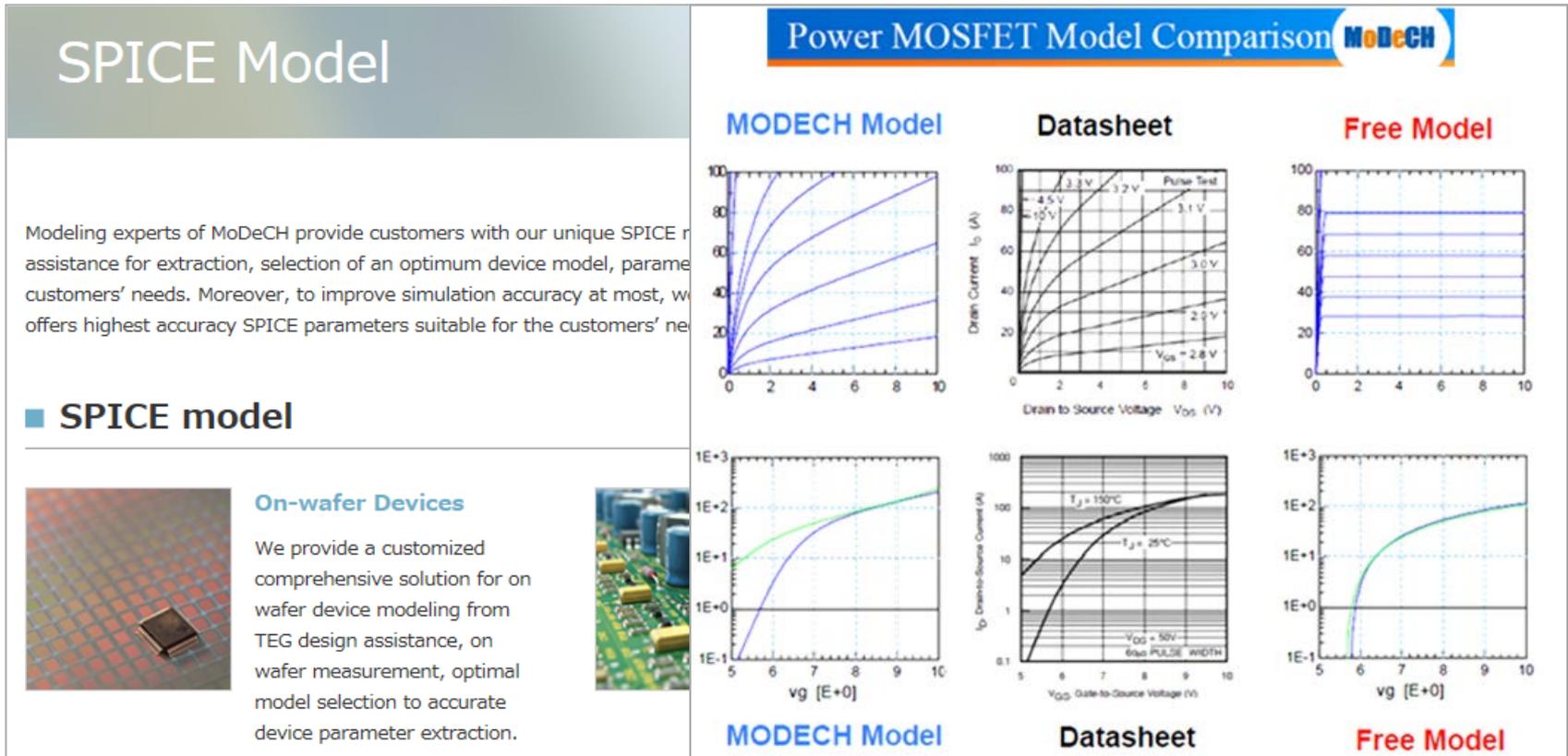
PSpice Advanced Analysis

- Increase design performance, yield, and reliability
  - Sensitivity identifies critical circuit components.
  - Optimizer optimizes key circuit components.
  - Parametric Plotter examines solution space through nested sweeps.
  - Monte Carlo analyzes statistical circuit behavior and yield .
 - Smoke detects component stress.
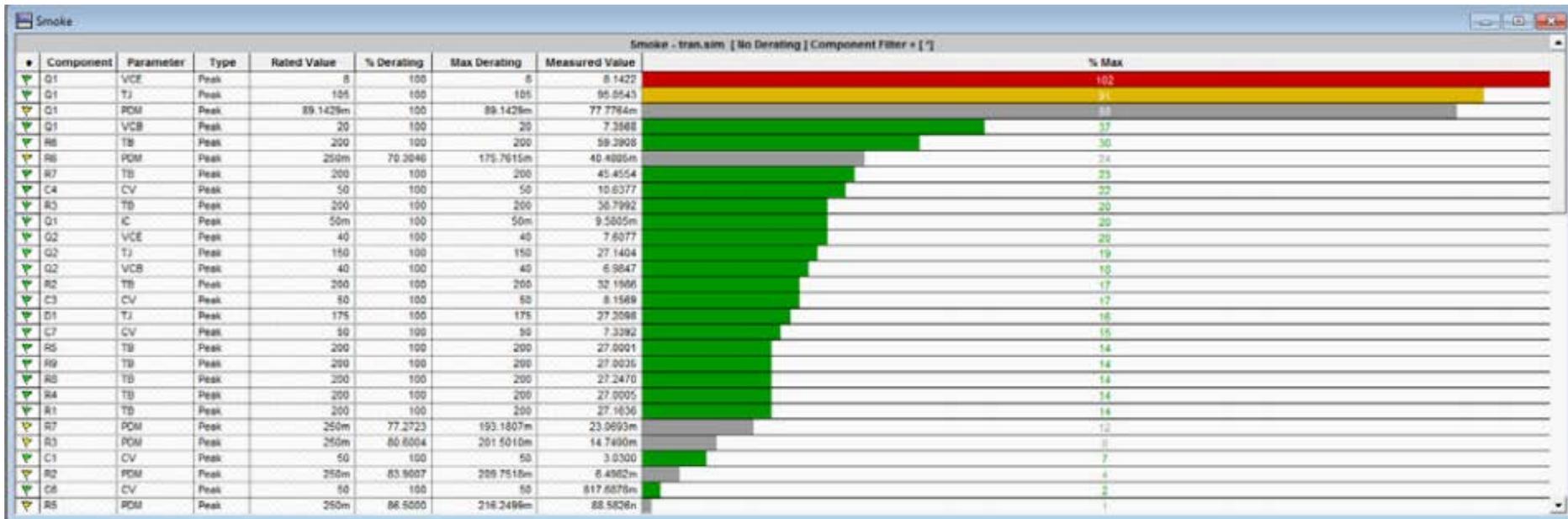
PSpice Summary

- ## Powerful and Widely Used Simulator

  – Integrates seamlessly with Cadence OrCAD Design Solution.

  – Full-featured mixed-Mode simulator

  – Extensive OrCAD PSpice model libraries & various types of modeling creation.

  – Be aware of pre-layout design risk & improve design performance, yield, and reliability.
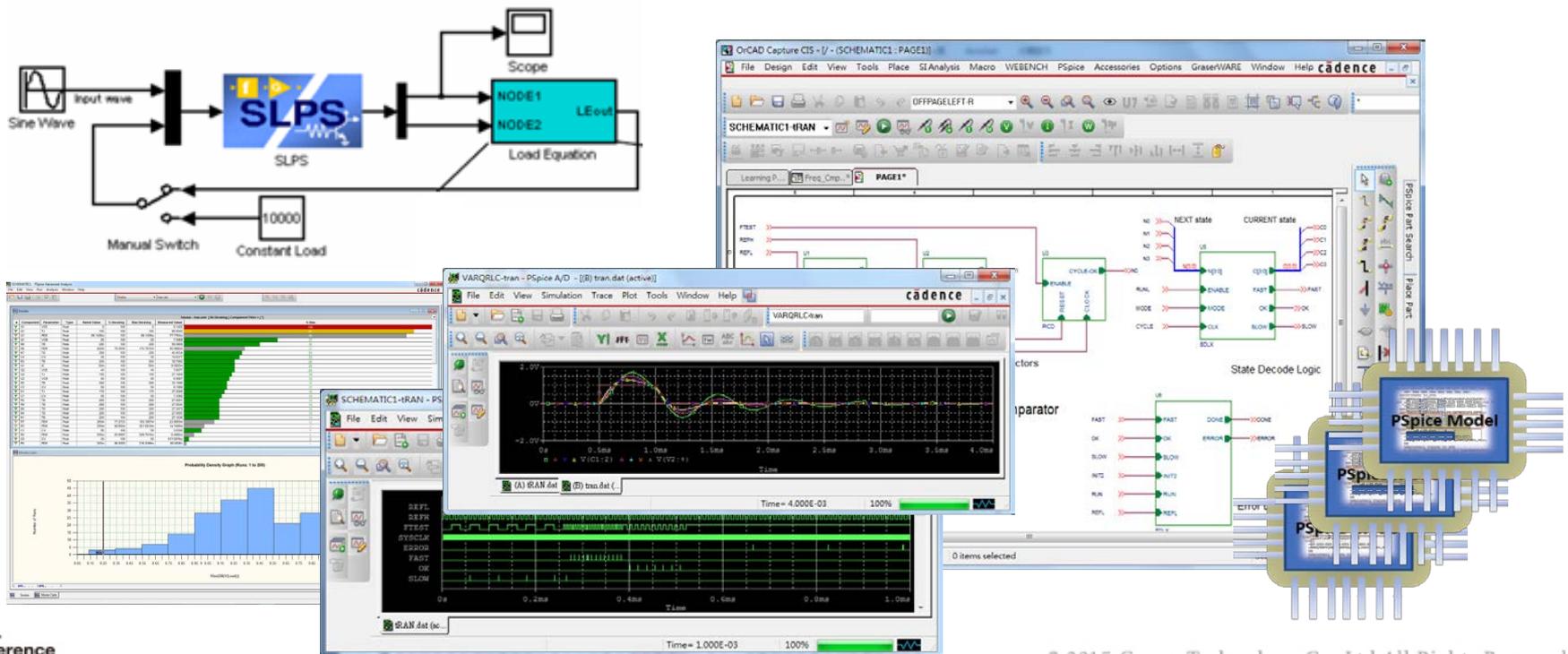
PSpice Hands-On Workshop

- PSpice Hands-on Workshop
  - Date, 20/Nov/2015

Full-featured Mixed-Mode PSpice simulation