Design and Analysis Challenges of Multi-Gigabit Transmission on Low Cost PCBs

Skipper Liang

Principle Application Engineer, ASI/SPB Taiwan
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Agenda

Problem/Challenge Today

3D Modeling

- ❑Why 3D
- ❑FEM – Finite Element Method
- ❑Inherent Defect of FEM
- ❑Cadence’ s “**Cut and Stitch**”
- ❑**Parallel Processing**

Massive Bit Transmission

- ❑BER – Bit Error Rate
- ❑Channel Response
- ❑Equalizer
- ❑Serial Link Analysis

Conclusions

Problem / Challenge Today

- High Speed Signal: PCIe, USB, SATA/SAS, HDMI, XFI, SFP
- Long Transmission Line, for example:

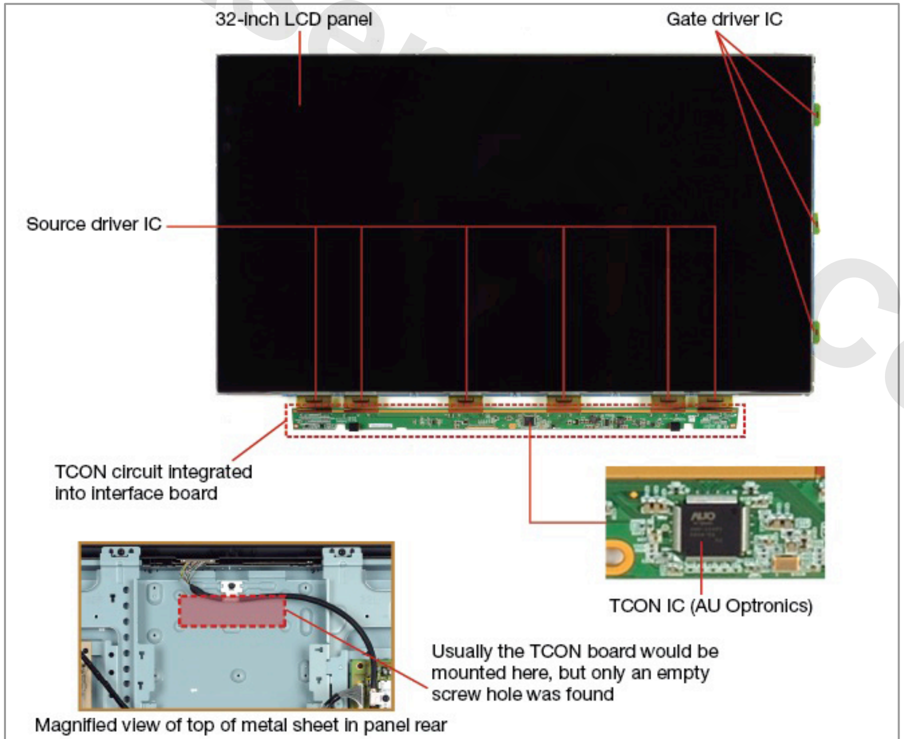
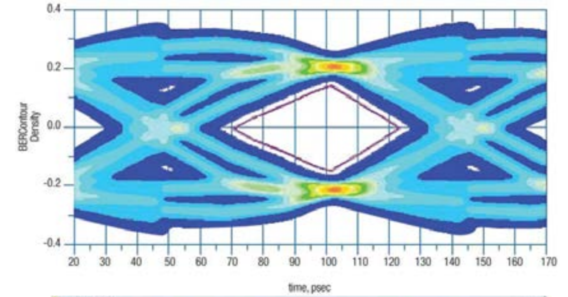


Fig 4 TCON Circuit Integrated into Interface Board The timing controller IC is mounted on the interface board, connected to the source driver IC. An empty screw hole was found where the TCON circuit board would normally be mounted. Textual explanations are guesses by *Nikkei Electronics*.

- Cost Concern: 2-layer pcb design

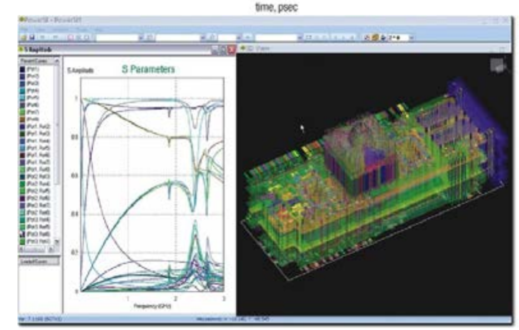
Problem / Challenge Today

- High Speed Signal: PCIe, USB, SATA/SAS, HDMI, XFI, SFP



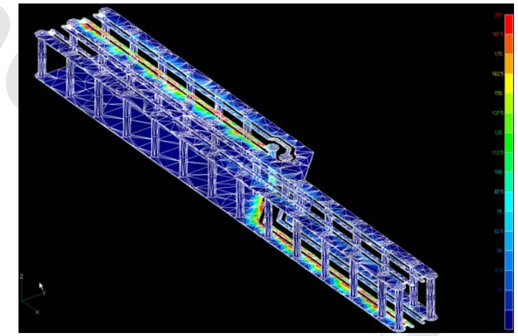
➡ A tool can help to simulate the behavior of a system over trillion bits transmission in a short time.

- Long Transmission Line



➡ A tool can help to model a big scale structure in a short time with high accuracy

- Cost Concern: 2-layer pcb design



➡ A **3D** tool can help to model in a short time with high accuracy

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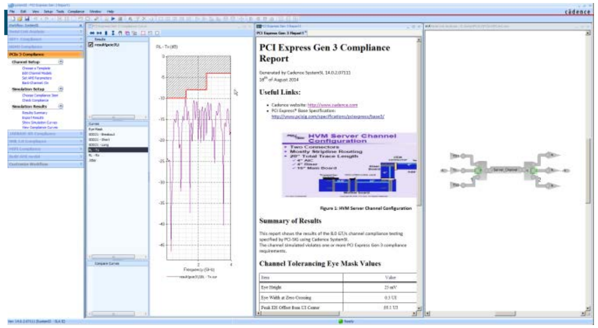
Problem / Challenge Today

A tool can help to simulate the behavior of a syste
over trillion bits transmission in a short time.

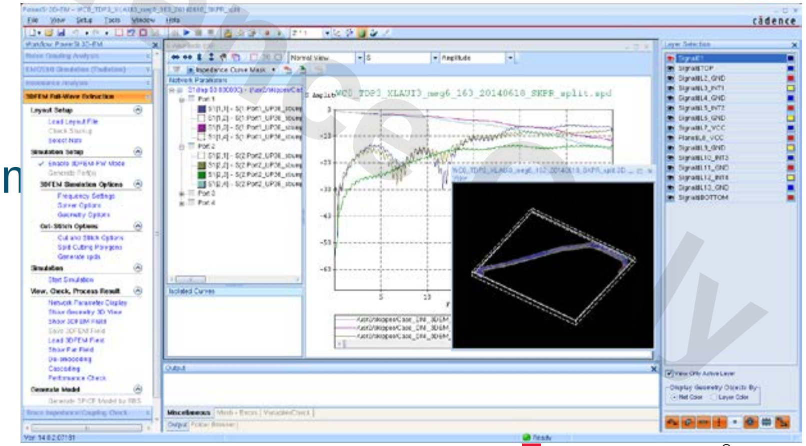
➡ System SI, SLA (Serial Link Analysis)



A tool can help to model a big scale structure in a short time with high accuracy

A **3D** tool can help to model in a short ti
high accuracy

➡ PowerSI 3DEM



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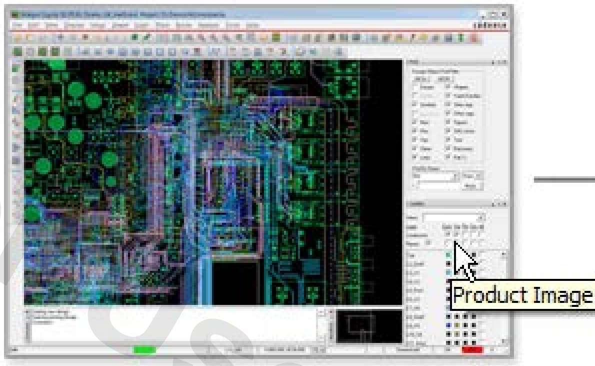
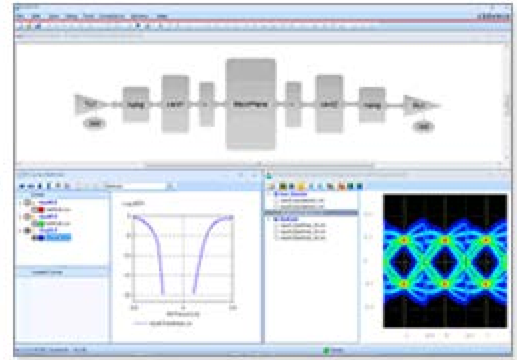
Problem / Challenge Today



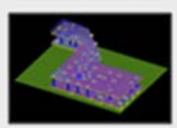


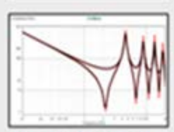
Serial Link SI
SIGR930

- System-level sim environment with channel simulation (AMI models)
- Full-wave 3D S-param layout extraction
- Via Wizard

PowerSI – 3D FEM
(SIGR311)

- Much faster (often 10x vs HFSS) with comparable accuracy
- Highly accurate low frequency solution (ex. lower than few MHz)
- Easy to use with geometry modeling and automated port setup

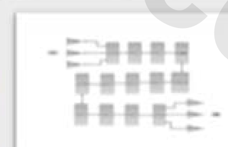


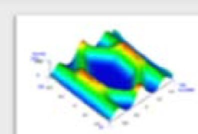


Differential pair in 6 layer package Results showing correlation with HFSS

SystemSI – SLA
(SIGR506)

- **SystemSI Serial Link Analysis** is an award-winning chip-to-chip analysis solution focuses on high-speed SerDes designs such as PCIe, HDMI, SFP+, Xaui, Infiniband, SAS, SATA, USB, and more.





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Conclusions

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Why 3D?

In 2.5D simulation tool

$$\nabla \times \vec{E} = \begin{vmatrix} \vec{x} & \vec{y} & \vec{z} \\ \frac{\partial}{\partial x} & \frac{\partial}{\partial y} & \boxed{\frac{\partial}{\partial z}} \\ \vec{E}_x & \vec{E}_y & \vec{E}_z \end{vmatrix} = -\mu \frac{\partial \vec{H}}{\partial t}$$

$$\nabla \times \vec{H} = \begin{vmatrix} \vec{x} & \vec{y} & \vec{z} \\ \frac{\partial}{\partial x} & \frac{\partial}{\partial y} & \boxed{\frac{\partial}{\partial z}} \\ \vec{H}_x & \vec{H}_y & \boxed{\vec{H}_z} \end{vmatrix} = \sigma \vec{E} - \varepsilon \frac{\partial \vec{E}}{\partial t}$$

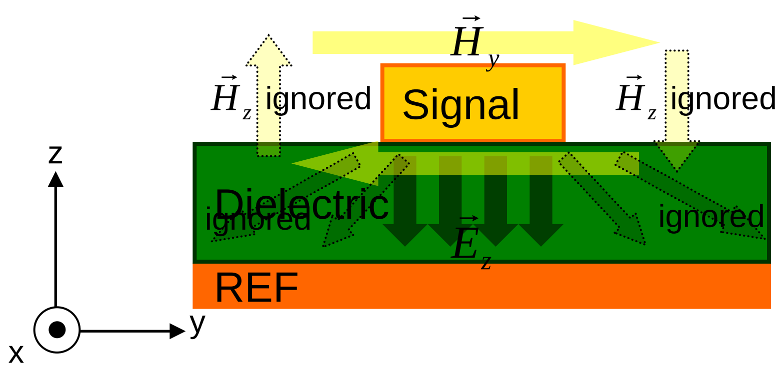
Assumed to be zero:

E_x, E_y, H_x, and H_y are constants along z-axis

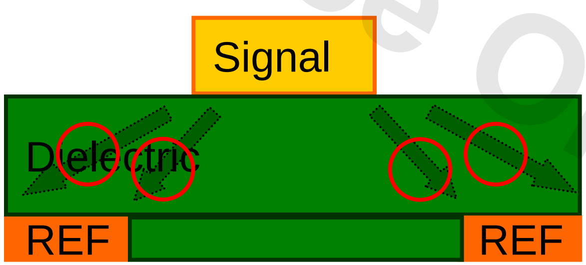
Assumed to be zero

1. No $\vec{E}_x$ 2. No $\vec{E}_y$ 3.No $\vec{H}_z$

Case 1. -> Can be solved by 2.5D tool



Case 2. -> Can't be solved by 2.5D tool (because the E-field is not purely along z-axis)



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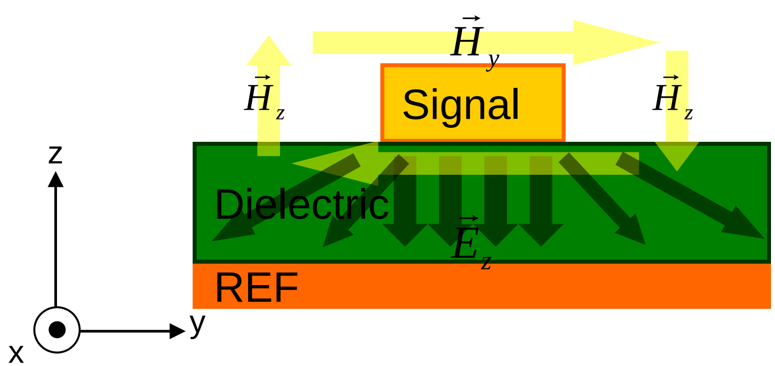
Why 3D?

<u>In 3D simulation tool</u>

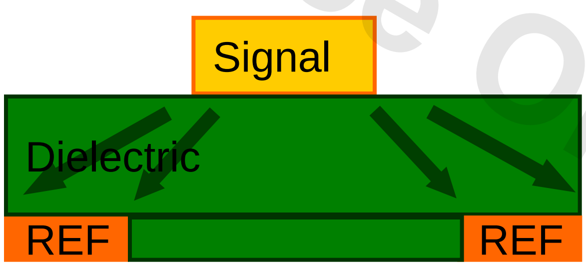
$$\nabla \times \vec{E} = \begin{vmatrix} \vec{x} & \vec{y} & \vec{z} \\ \dfrac{\partial}{\partial x} & \dfrac{\partial}{\partial y} & \dfrac{\partial}{\partial z} \\ \overrightarrow{E_x} & \overrightarrow{E_y} & \overrightarrow{E_z} \end{vmatrix} = -\mu \frac{\partial \vec{H}}{\partial t} \qquad \nabla \times \vec{H} = \begin{vmatrix} \vec{x} & \vec{y} & \vec{z} \\ \dfrac{\partial}{\partial x} & \dfrac{\partial}{\partial y} & \dfrac{\partial}{\partial z} \\ \overrightarrow{H_x} & \overrightarrow{H_y} & \overrightarrow{H_z} \end{vmatrix} = \sigma \vec{E} - \varepsilon \frac{\partial \vec{E}}{\partial t}$$

Every items will be involved in calculation.

Case 1. -> Can be solved by 3D tool



Case 2. -> Can be solved by 3D tool (because the E-field be divided into z-axis and y-axis)



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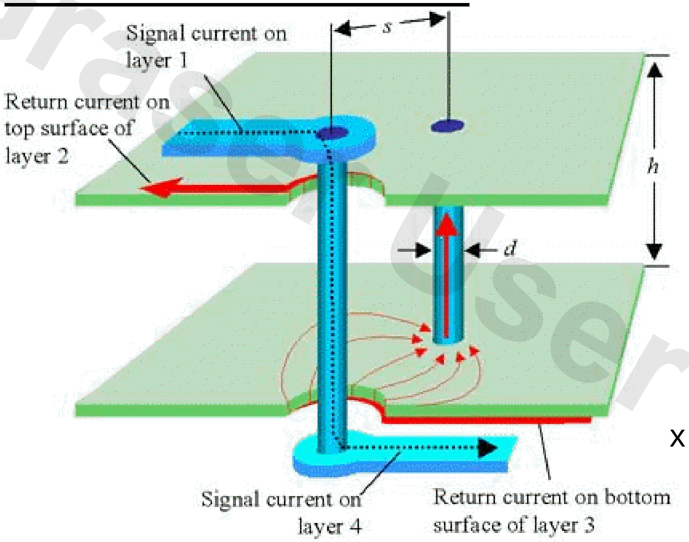
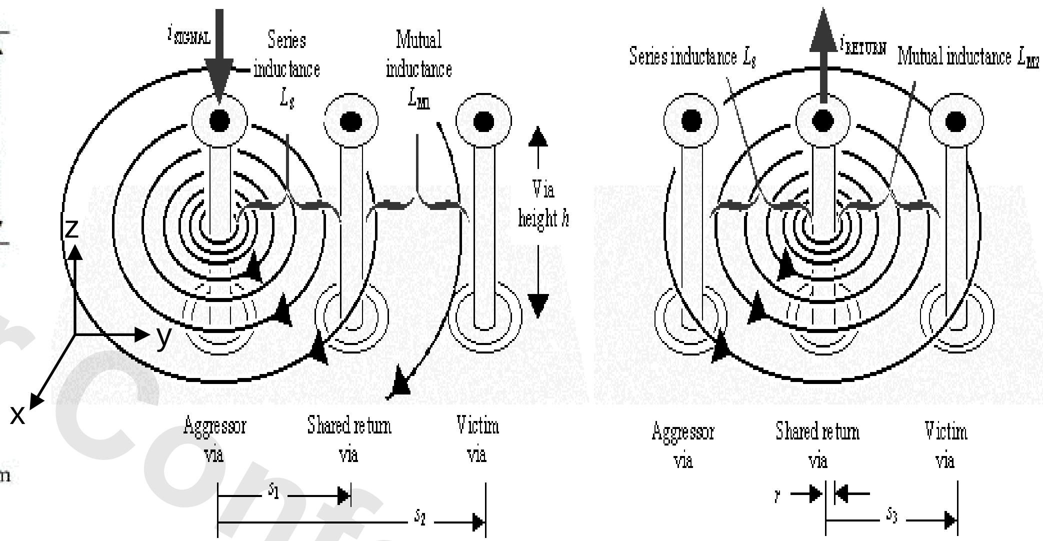
Why 3D? Other 2.5D tool's limit

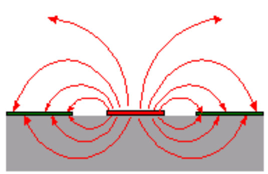
1. Reference to GND via

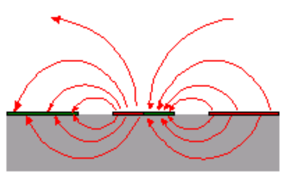


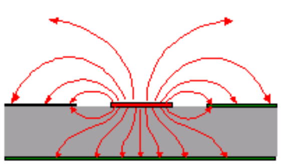
2. Crosstalk between vias



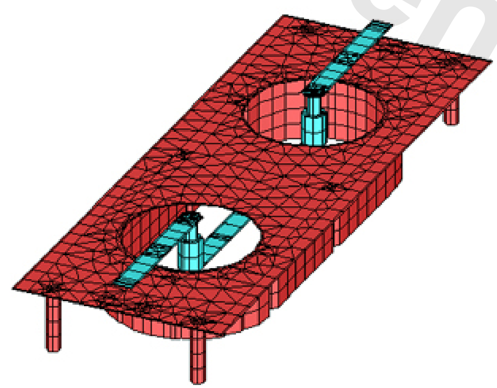
3. Coplanar traces


Coplanar even mode


Coplanar odd mode


Parasitic Microstrip Mode on conductor-backed coplanar line

4. Via with big antipad (trace without reference at antipad)



All these structures can't be solved by 2.5D tool in the full frequency range due to the E-field is purely in x- or y- direction, without z-direction.

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FEM – Finite Element Method

- *Finite Element Method* (FEM) is a numerical procedure to convert partial differential equations into a set of linear algebraic equations to obtain approximate solutions to boundary-value problems.

Maxwell Equations

$$\nabla\times\vec{E} = -j\omega\mu\vec{H}$$
$$\nabla\times\vec{H} = j\omega\varepsilon\vec{E} + \vec{J}$$
$$\nabla\cdot\left(\varepsilon\vec{E}\right) = \rho$$
$$\nabla\cdot\left(\mu\vec{H}\right) = 0$$

Helmholtz Equation

$$\nabla\times\frac{1}{\mu}\nabla\times\vec{E} - \omega^2\varepsilon\vec{E} = -j\omega\vec{J}$$

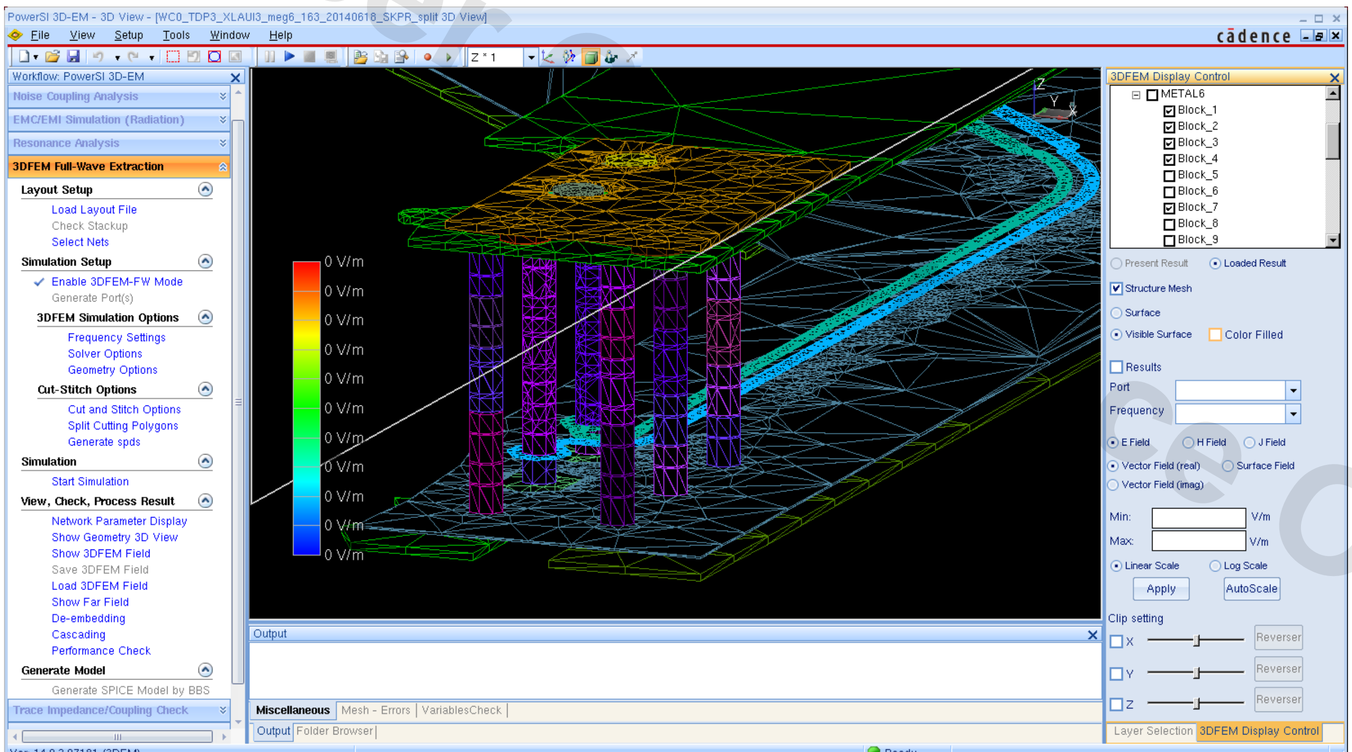
Using Galerkin's method to get a weak form:

$$[A]\{E\} = \{b\}$$

Where {b} is the port excitation

FEM – Finite Element Method

- The basic idea of the finite element method is to divide the solution domain into small sub-domains, which are called finite elements, and then use simple functions, such as linear and quadratic functions, to approximate the unknown solution over each element.



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Inherent Defect of FEM

- *DC Point –*

  Full-wave (solving Maxwell/Helmholtz equation) FEM equations are singular at DC, that is:

  $$[A]\{E\} = \{b\}$$ can't be solved at frequency=0

  Extra-interpolating is a commonly-adopted method by most tools.

  ➡ ***Risky!!***

  Cadence 3DEM uses another FEM solver (not Maxwell/Holmholtx equations) at DC point (that is, PowerDC)

- *Low Frequency Range –*

  Full-wave (solving Maxwell/Helmholtz equation) FEM equations are ill-conditioned at low frequency range.

  ➡ Longer simulation time and risk of non-reasonable result

  Cadence 3DEM uses another FEM solver (especially for low frequency conditioning algorithm) at low frequency range.

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Inherent Defect of FEM

- *Big Case -*

$$[A]\{E\} = \{b\}$$

If there're n-2 elements (E_2, E_3, …, E_{n-1}) to be solved, where E_1 and E_n are known boundary elements, the matrix operation could be expanded as the following:

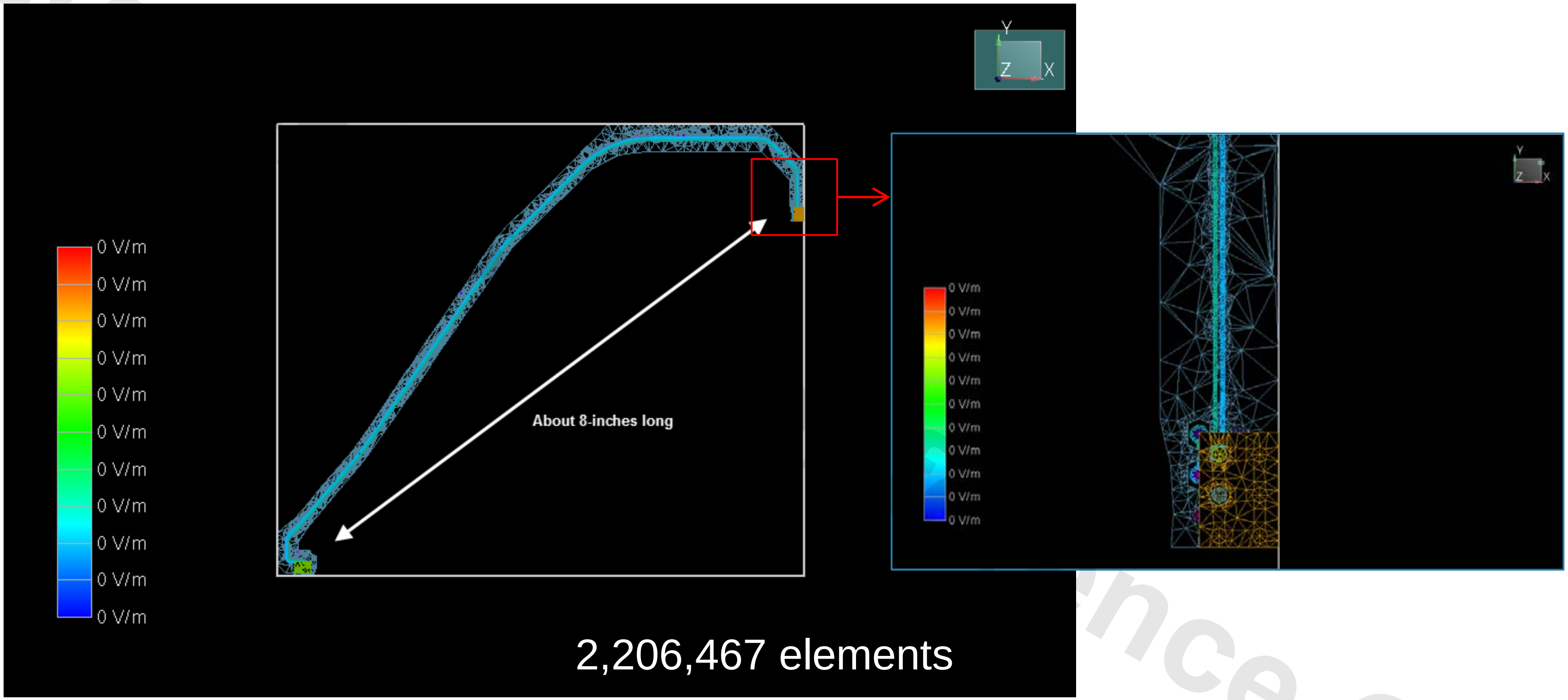
$$\text{n-2}\left\{\begin{bmatrix} A_{22} & A_{23} & \cdots & A_{2n-1} \\ A_{32} & A_{33} & \cdots & A_{3n-1} \\ \vdots & \vdots & & \vdots \\ A_{n-12} & A_{n-13} & \cdots & A_{n-1n-1} \end{bmatrix}\right. \cdot \begin{bmatrix} E_2 \\ E_3 \\ \vdots \\ E_{n-1} \end{bmatrix} = \begin{bmatrix} b_2 \\ b_3 \\ \vdots \\ b_{n-1} \end{bmatrix} - \begin{bmatrix} A_{21}E_1 + A_{2n}E_n \\ A_{31}E_1 + A_{3n}E_n \\ \vdots \\ A_{n-11}E_1 + A_{n-1n}E_n \end{bmatrix}$$

$$\underbrace{\qquad\qquad\qquad\qquad\qquad}_{\text{n-2}}$$

If there're **2***(n-2) elements to be solved, how big is the scale of this matrix operation? How many **times** the scale of the original matrix operation?

Inherent Defect of FEM

- *Big Case -*



More elements ➡ More simulation time, more hardware resource

Less elements ➡ Less simulation time, less hardware resource

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Cadence's "Cut and Stitch"

Besides the over-whelming advantages in DC and Low-Frequency range, which we just mentioned:

Inherent Defect of FEM

- *DC Point –*

  Full-wave (solving Maxwell/Helmholtz equation) FEM equations are singular at DC, that is:

  $[A]\{E\} = \{b\}$ can't be solved at frequency=0

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  ➡ Longer simulation time and risk of non-reasonable result

  Cadence 3DEM uses another FEM solver (especially for low frequency conditioning algorithm) at low frequency range.

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Now Cadence has a revolutionary method to speed up the simulation over big case , which is called -

Cut and Stitch

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Cadence’s “Cut and Stitch”

The whole idea is:

$$
n-2\left\{\underbrace{\begin{bmatrix} A_{22} & A_{23} & \cdots & A_{2n-1} \\ A_{32} & A_{33} & \cdots & A_{3n-1} \\ \vdots & \vdots & & \vdots \\ A_{n-12} & A_{n-13} & \cdots & A_{n-1n-1} \end{bmatrix}}_{n-2}\right. \cdot \begin{bmatrix} E_2 \\ E_3 \\ \vdots \\ E_{n-1} \end{bmatrix} = \begin{bmatrix} b_2 \\ b_3 \\ \vdots \\ b_{n-1} \end{bmatrix} - \begin{bmatrix} A_{21}E_1 + A_{2n}E_n \\ A_{31}E_1 + A_{3n}E_n \\ \vdots \\ A_{n-11}E_1 + A_{n-1n}E_n \end{bmatrix}
$$

$$
\frac{n-4}{2}\left\{\underbrace{\begin{bmatrix} A_{22} & A_{23} & \cdots & A_{2\frac{n-2}{2}} \\ A_{32} & A_{33} & \cdots & A_{3\frac{n-2}{2}} \\ \vdots & \vdots & & \vdots \\ A_{\frac{n-2}{2}2} & A_{\frac{n-2}{2}3} & \cdots & A_{\frac{n-2}{2}\frac{n-2}{2}} \end{bmatrix}}_{\frac{n-4}{2}}\right. \cdot \begin{bmatrix} E_2 \\ E_3 \\ \vdots \\ E_{\frac{n-2}{2}} \end{bmatrix} = \begin{bmatrix} b_2 \\ b_3 \\ \vdots \\ b_{\frac{n-2}{2}} \end{bmatrix} - \begin{bmatrix} A_{21}E_1 + A_{2\frac{n}{2}}E_{\frac{n}{2}} \\ A_{31}E_1 + A_{3\frac{n}{2}}E_{\frac{n}{2}} \\ \vdots \\ A_{\frac{n-2}{2}1}E_1 + A_{\frac{n-2}{2}\frac{n}{2}}E_{\frac{n}{2}} \end{bmatrix}
$$

$$
\frac{n-4}{2}\left\{\underbrace{\begin{bmatrix} A_{\frac{n+2}{2}\frac{n+2}{2}} & A_{\frac{n+2}{2}\frac{n+4}{2}} & \cdots & A_{\frac{n+2}{2}n-1} \\ A_{\frac{n+4}{2}\frac{n+2}{2}} & A_{\frac{n+4}{2}\frac{n+4}{2}} & \cdots & A_{\frac{n+4}{2}n-1} \\ \vdots & \vdots & & \vdots \\ A_{n-1\frac{n+2}{2}} & A_{n-1\frac{n+4}{2}} & \cdots & A_{n-1n-1} \end{bmatrix}}_{\frac{n-4}{2}}\right. \cdot \begin{bmatrix} E_{\frac{n+2}{2}} \\ E_{\frac{n+4}{2}} \\ \vdots \\ E_{n-1} \end{bmatrix} = \begin{bmatrix} b_{\frac{n+2}{2}} \\ b_{\frac{n+4}{2}} \\ \vdots \\ b_{n-1} \end{bmatrix} - \begin{bmatrix} A_{\frac{n+2}{2}\frac{n}{2}}E_{\frac{n}{2}} + A_{\frac{n+2}{2}n}E_n \\ A_{\frac{n+4}{2}\frac{n}{2}}E_{\frac{n}{2}} + A_{\frac{n+4}{2}n}E_n \\ \vdots \\ A_{n-1\frac{n}{2}}E_{\frac{n}{2}} + A_{n-1n}E_n \end{bmatrix}
$$

(When n is large enough,) ¼ hardware resource, ¼ simulation time

(When n is large enough,) ¼ hardware resource, ¼ simulation time

½ hardware resource, ½ simulation time

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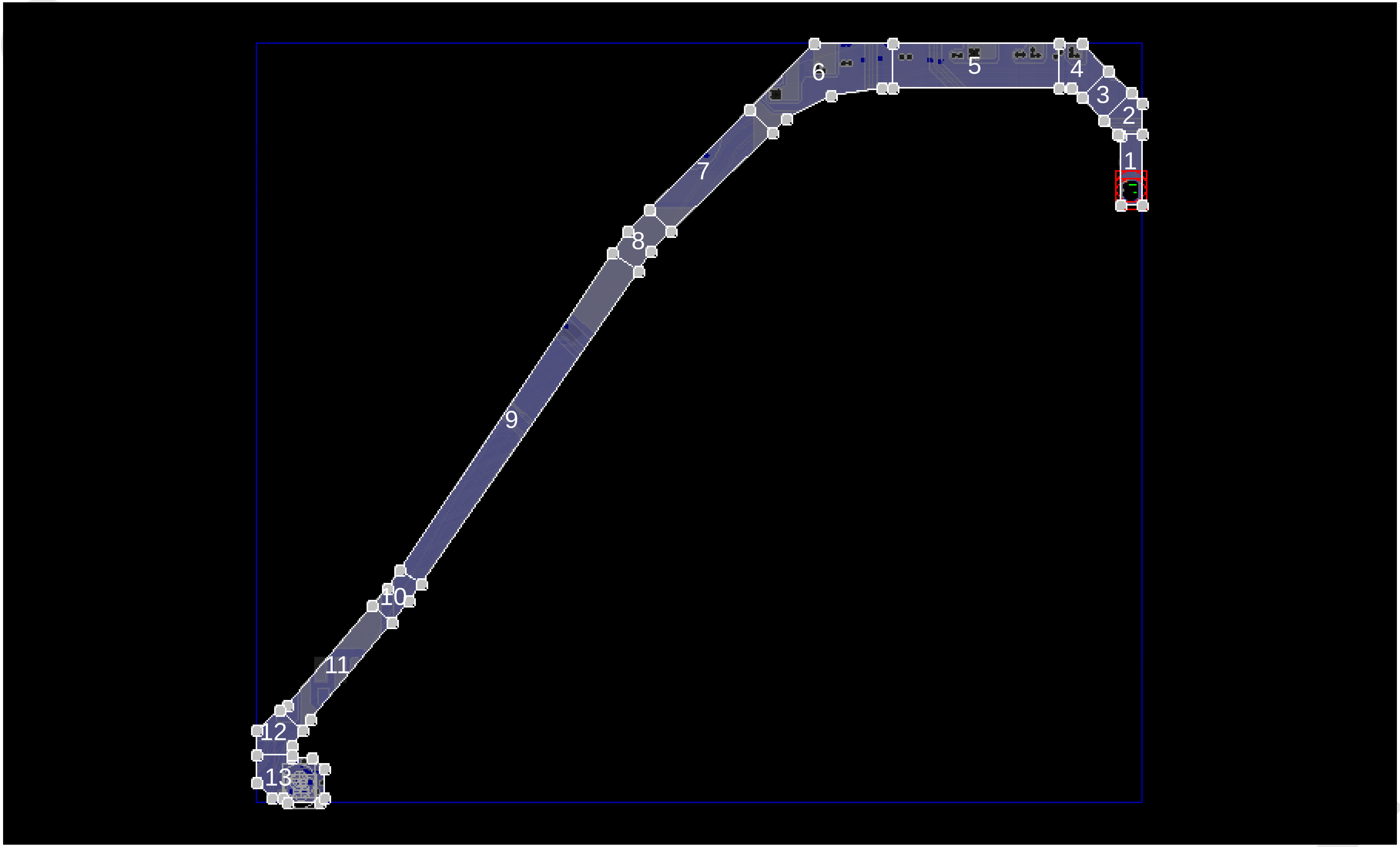
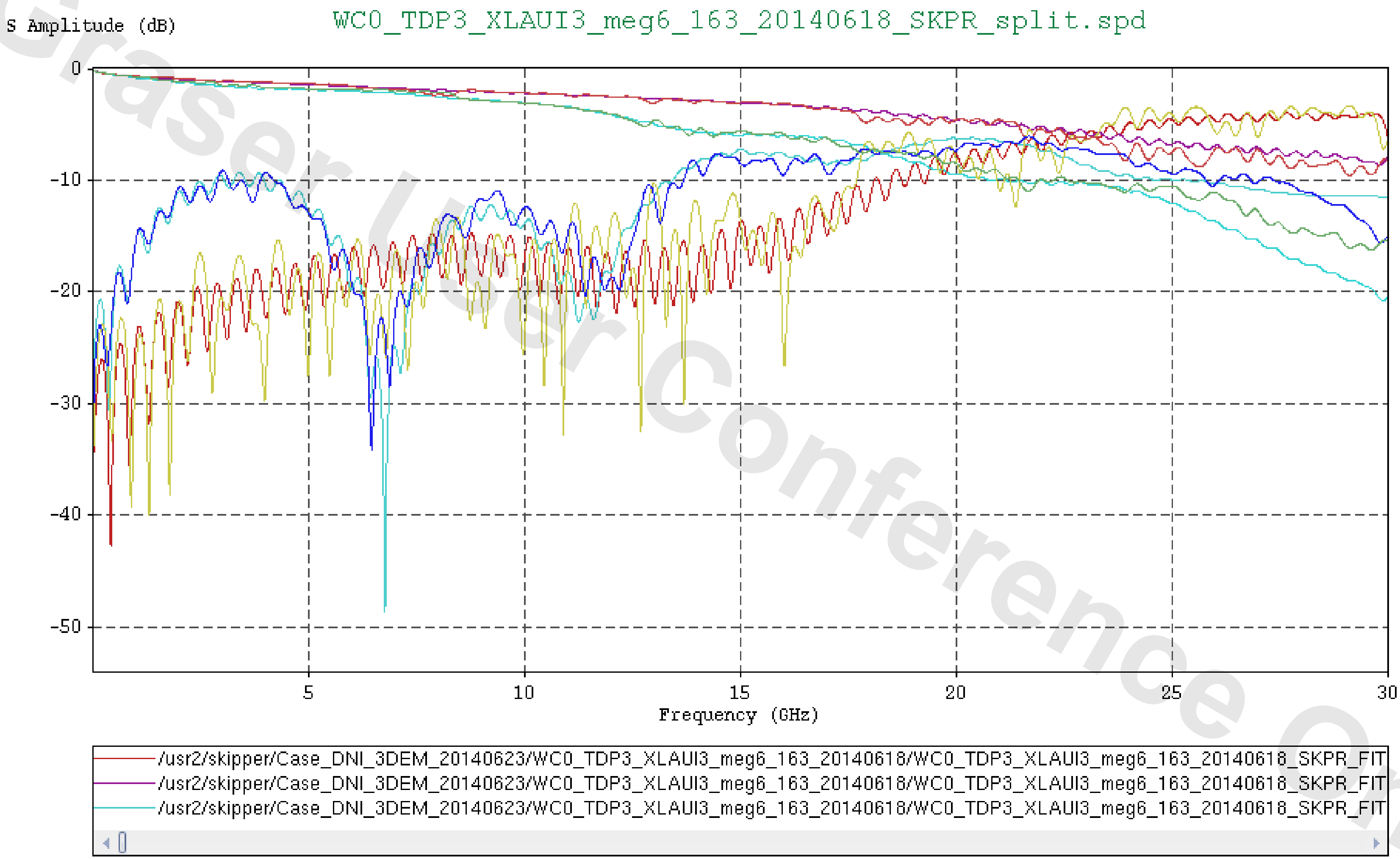
Cadence's "Cut and Stitch"



Cadence’s “Cut and Stitch”



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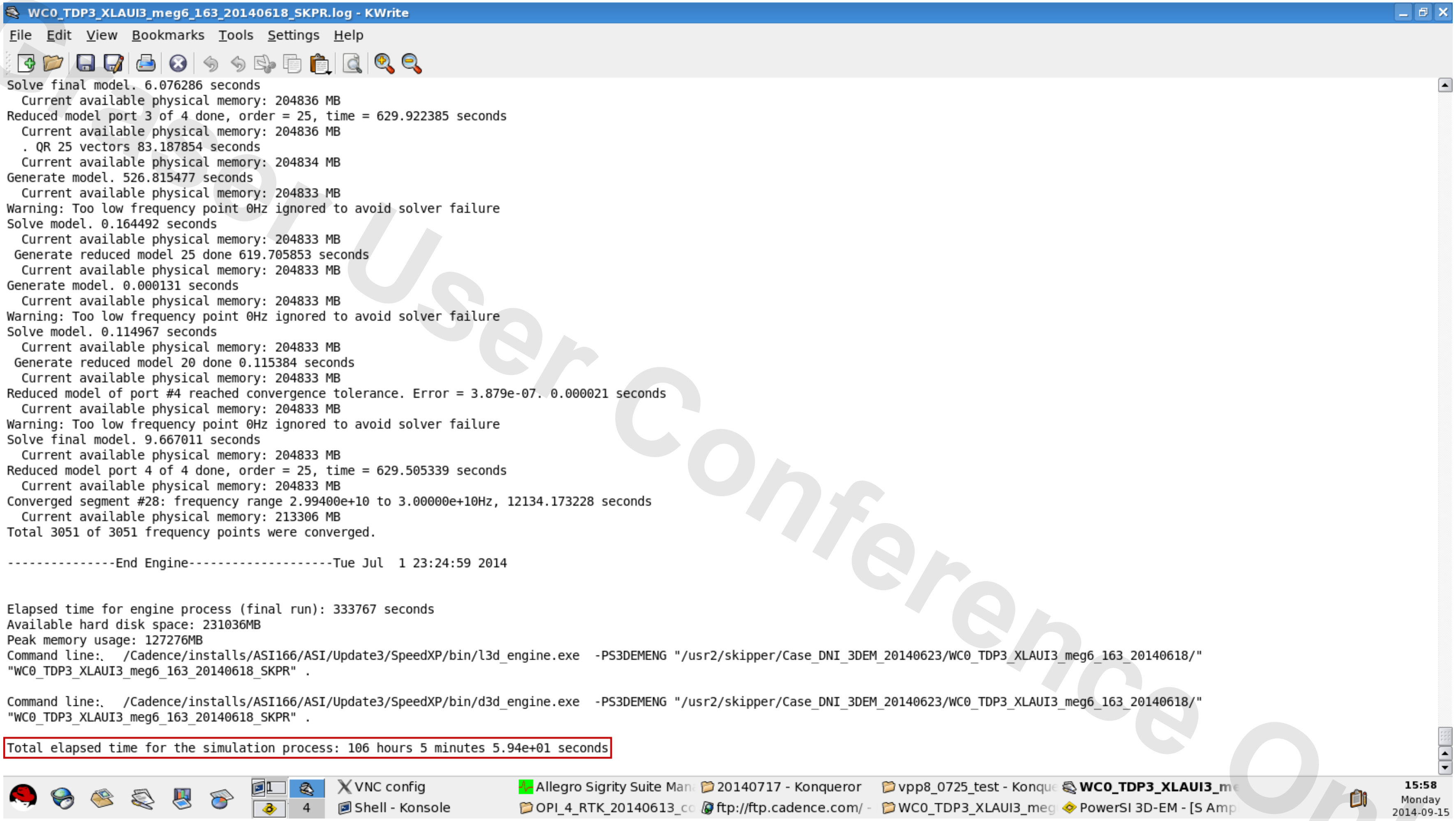
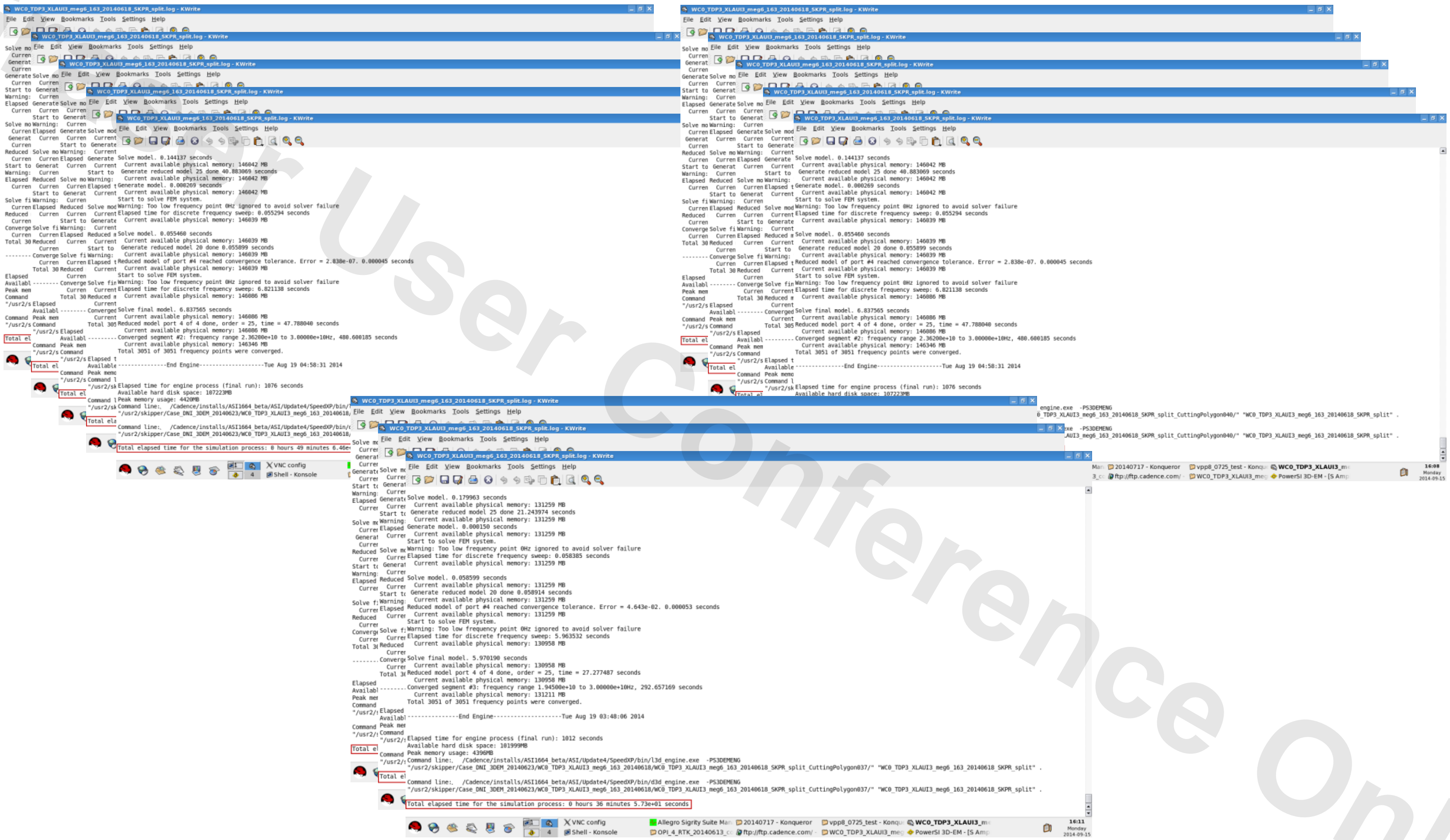
Cadence’ s “Cut and Stitch”




```
Solve final model. 6.076286 seconds
  Current available physical memory: 204836 MB
Reduced model port 3 of 4 done, order = 25, time = 629.922385 seconds
  Current available physical memory: 204836 MB
  . QR 25 vectors 83.187854 seconds
  Current available physical memory: 204834 MB
Generate model. 526.815477 seconds
  Current available physical memory: 204833 MB
Warning: Too low frequency point 0Hz ignored to avoid solver failure
Solve model. 0.164492 seconds
  Current available physical memory: 204833 MB
 Generate reduced model 25 done 619.705853 seconds
  Current available physical memory: 204833 MB
Generate model. 0.000131 seconds
  Current available physical memory: 204833 MB
Warning: Too low frequency point 0Hz ignored to avoid solver failure
Solve model. 0.114967 seconds
  Current available physical memory: 204833 MB
 Generate reduced model 20 done 0.115384 seconds
  Current available physical memory: 204833 MB
Reduced model of port #4 reached convergence tolerance. Error = 3.879e-07. 0.000021 seconds
  Current available physical memory: 204833 MB
Warning: Too low frequency point 0Hz ignored to avoid solver failure
Solve final model. 9.667011 seconds
  Current available physical memory: 204833 MB
Reduced model port 4 of 4 done, order = 25, time = 629.505339 seconds
  Current available physical memory: 204833 MB
Converged segment #28: frequency range 2.99400e+10 to 3.00000e+10Hz, 12134.173228 seconds
  Current available physical memory: 213306 MB
Total 3051 of 3051 frequency points were converged.

--------------End Engine-------------------Tue Jul  1 23:24:59 2014


Elapsed time for engine process (final run): 333767 seconds
Available hard disk space: 231036MB
Peak memory usage: 127276MB
Command line:.  /Cadence/installs/ASI166/ASI/Update3/SpeedXP/bin/l3d_engine.exe  -PS3DEMENG "/usr2/skipper/Case_DNI_3DEM_20140623/WC0_TDP3_XLAUI3_meg6_163_20140618/"
"WC0_TDP3_XLAUI3_meg6_163_20140618_SKPR" .

Command line:.  /Cadence/installs/ASI166/ASI/Update3/SpeedXP/bin/d3d_engine.exe  -PS3DEMENG "/usr2/skipper/Case_DNI_3DEM_20140623/WC0_TDP3_XLAUI3_meg6_163_20140618/"
"WC0_TDP3_XLAUI3_meg6_163_20140618_SKPR" .

Total elapsed time for the simulation process: 106 hours 5 minutes 5.94e+01 seconds
```

Original: 106hr, 5mins, 59.4seconds

Cadence’ s “Cut and Stitch”



Cut: **6hr, 48mins, 9.32seconds**

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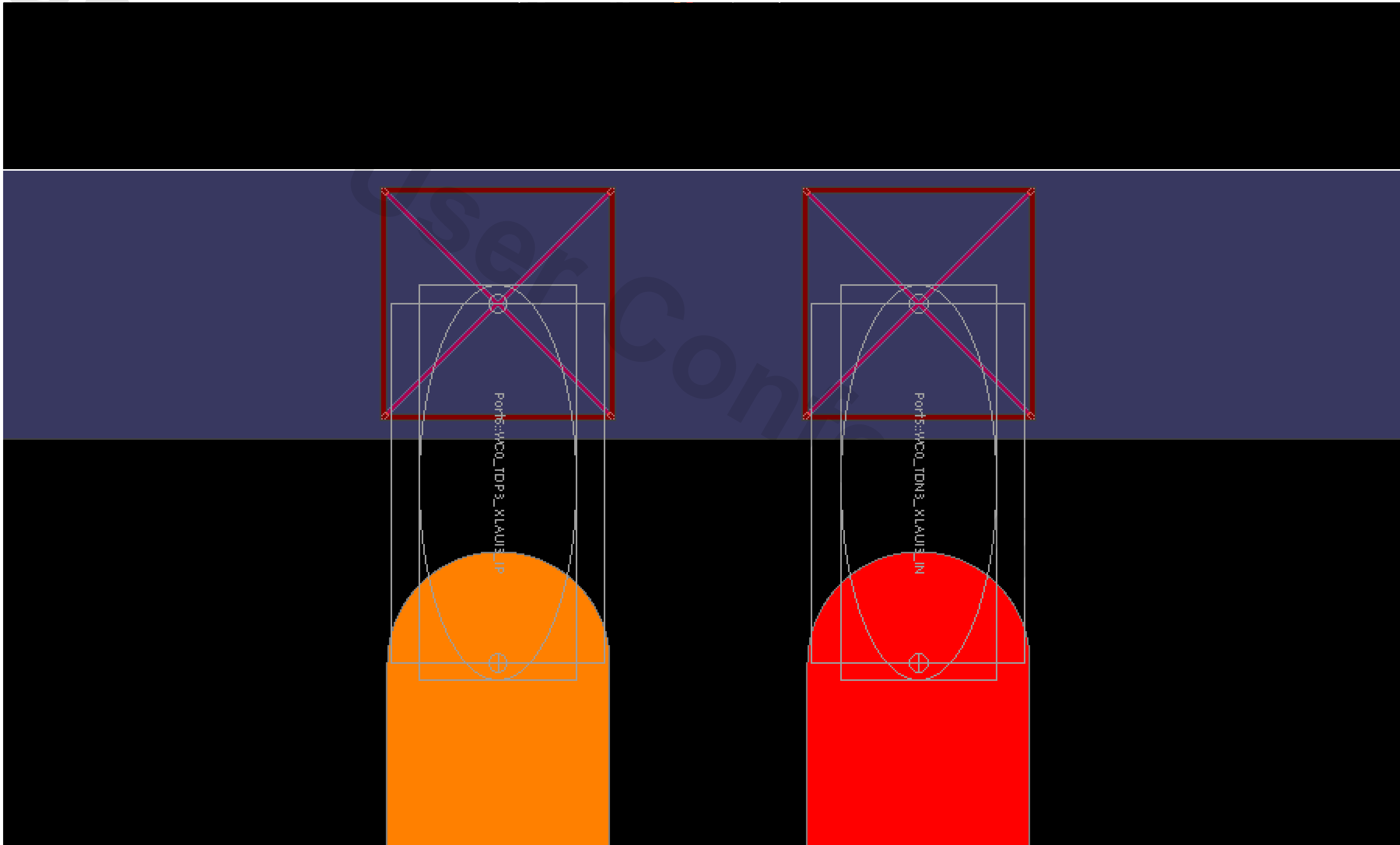
Cadence’s “Cut and Stitch”

What happened to the cutting edge?



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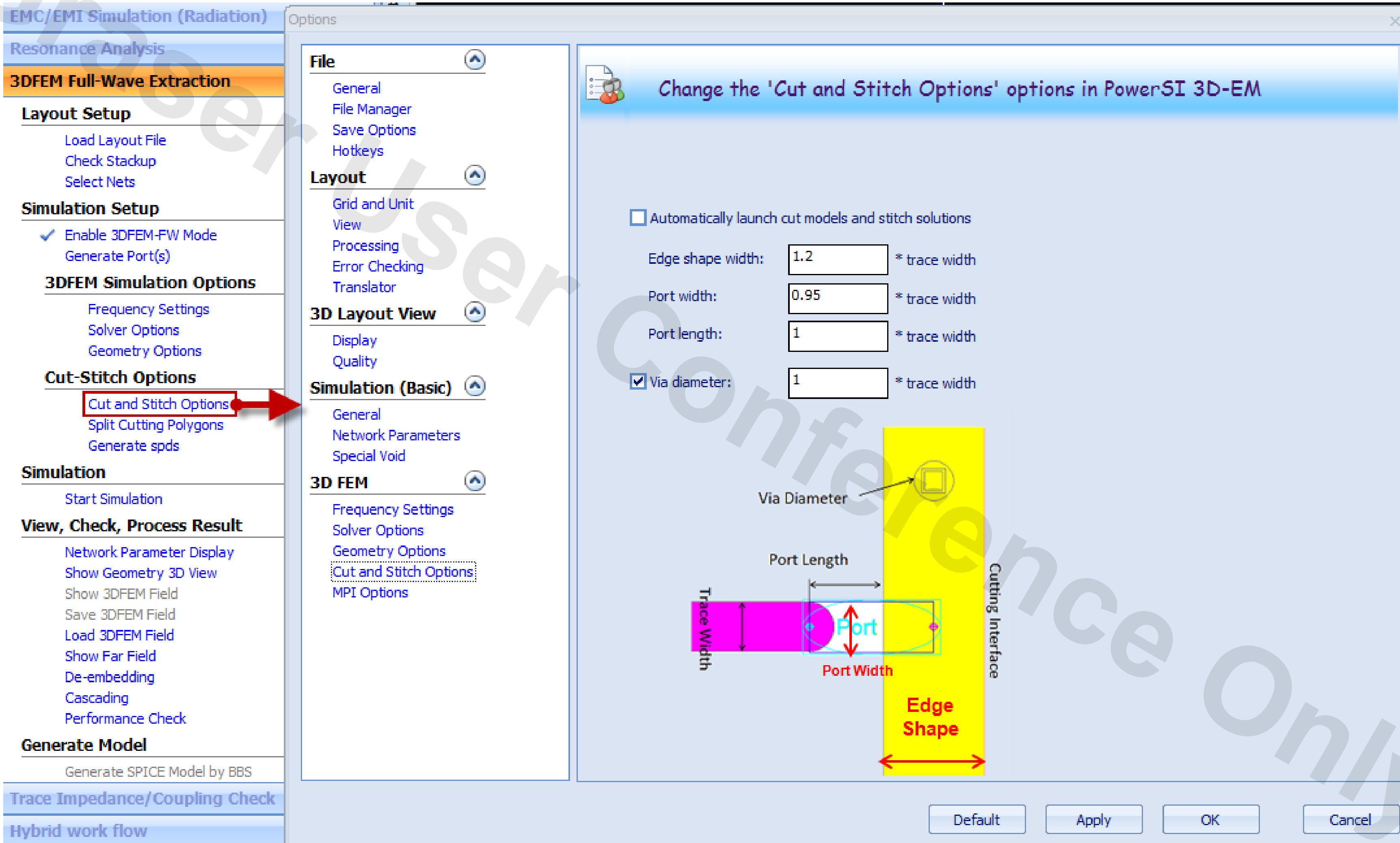
Cadence’ s “Cut and Stitch”

What happened to the cutting edge?



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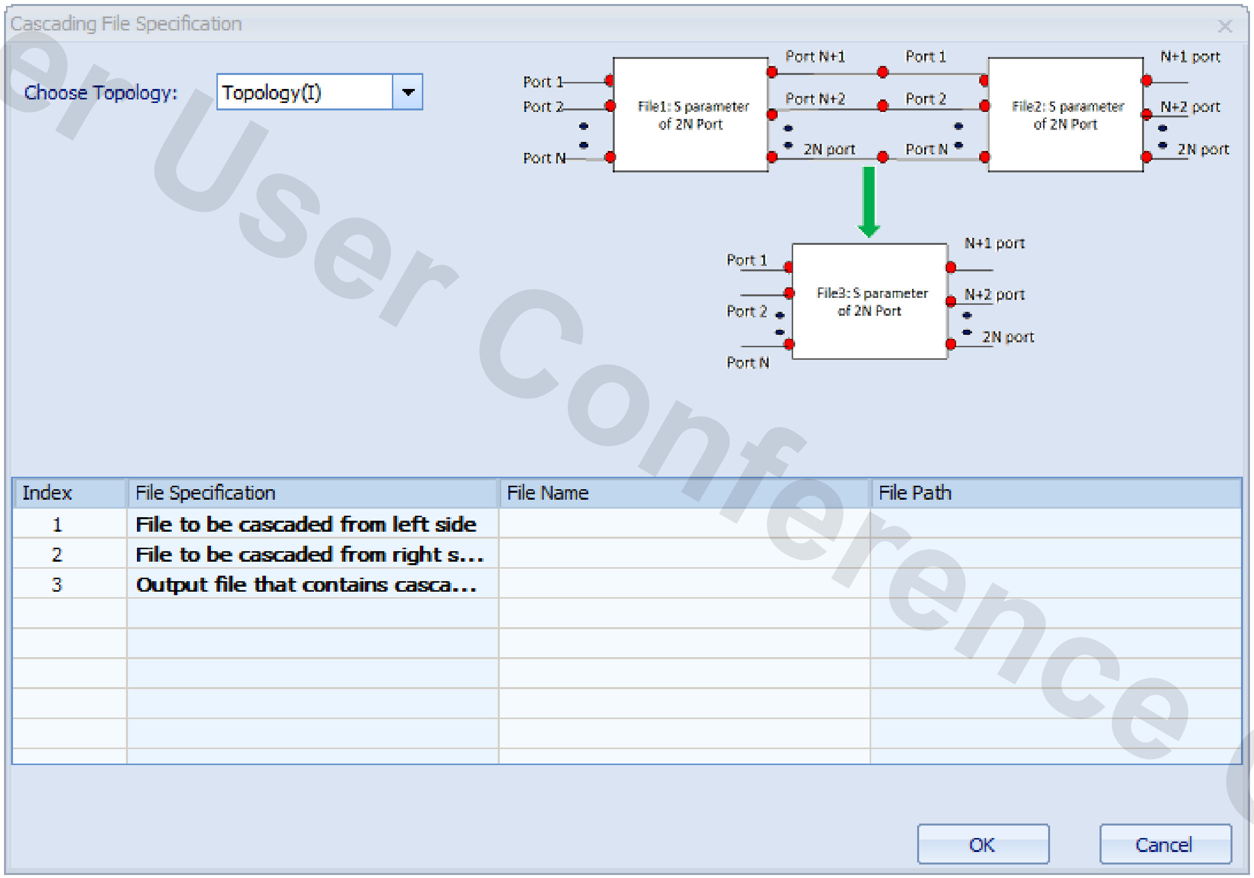
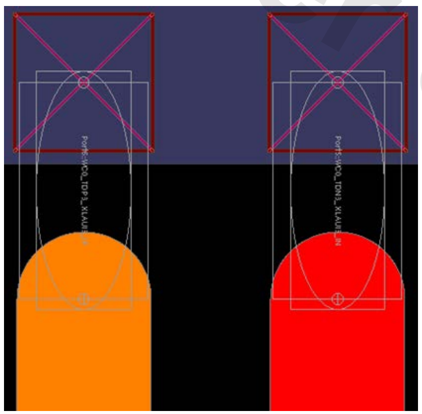
Cadence's "Cut and Stitch"

At the end, 3DEM will cascade the S-parameters to get the over-all behavior of the test case:

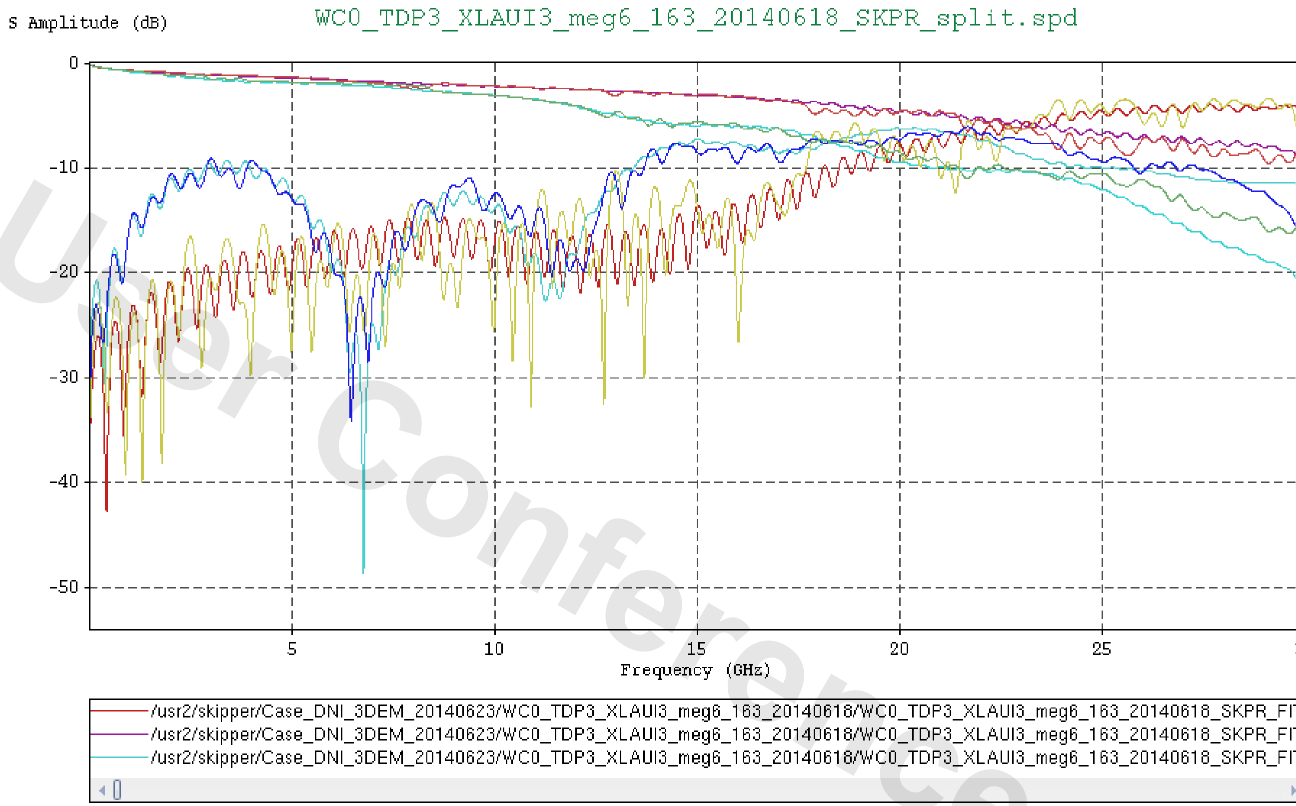


(This dialog window is for demonstration. During 3DEM cut-and –stitch simulation flow, you don't need to do this. 3DEM will do this automatically)

Cadence’s “Cut and Stitch”



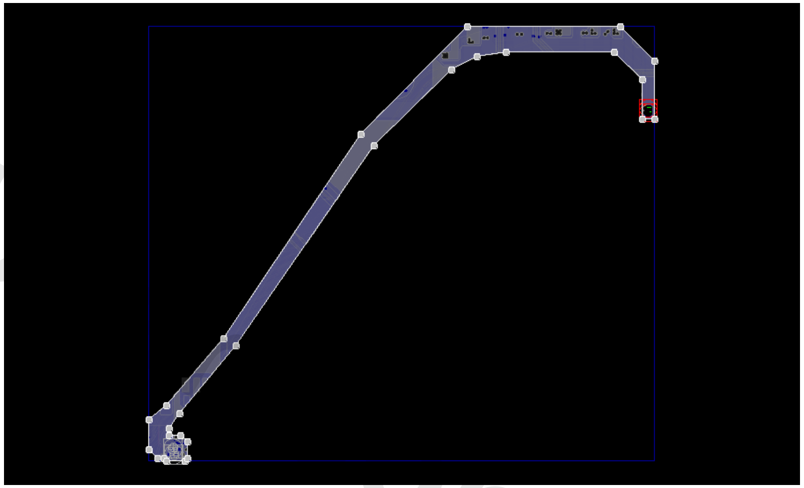
x 24
(13 sections, 12 cuts)



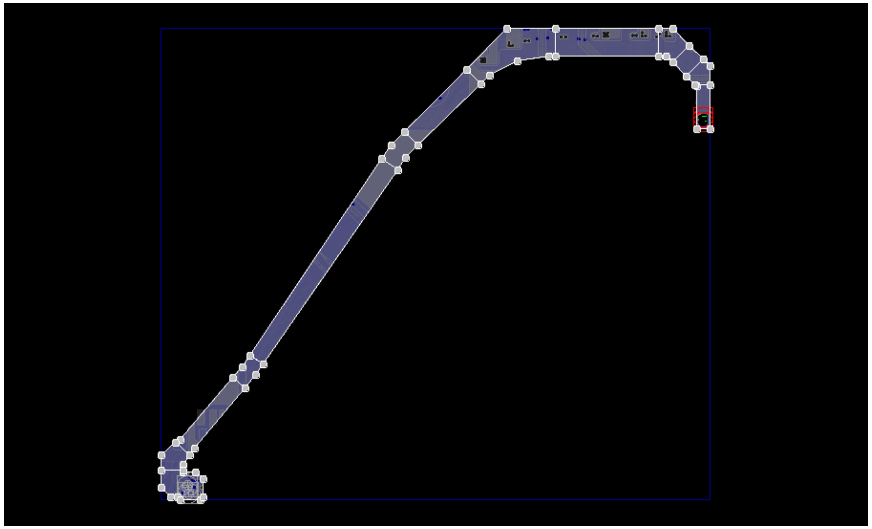
These lump-ports’ effect will cause the tiny difference between the cut-and stitch and the overall results.

Cadence’s “Cut and Stitch”

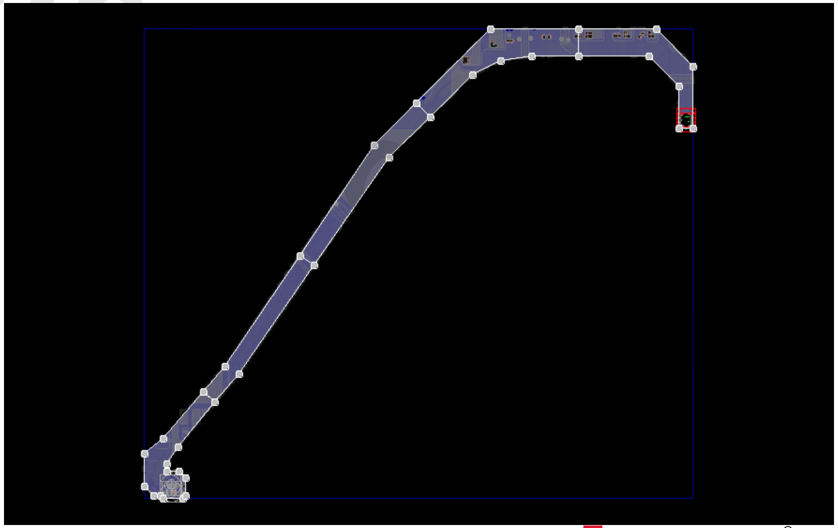
Cut in two different ways:



Case 1: 13 sections, 12 cuts

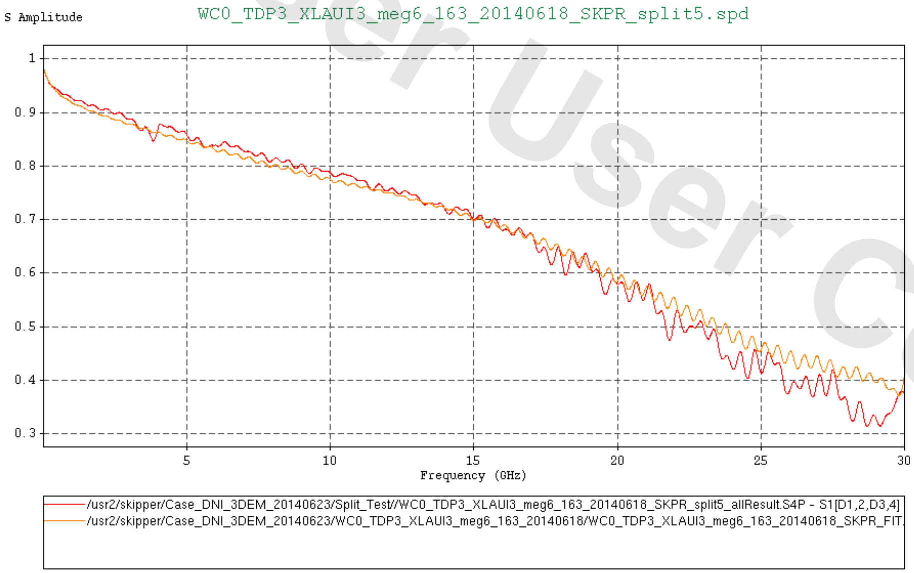


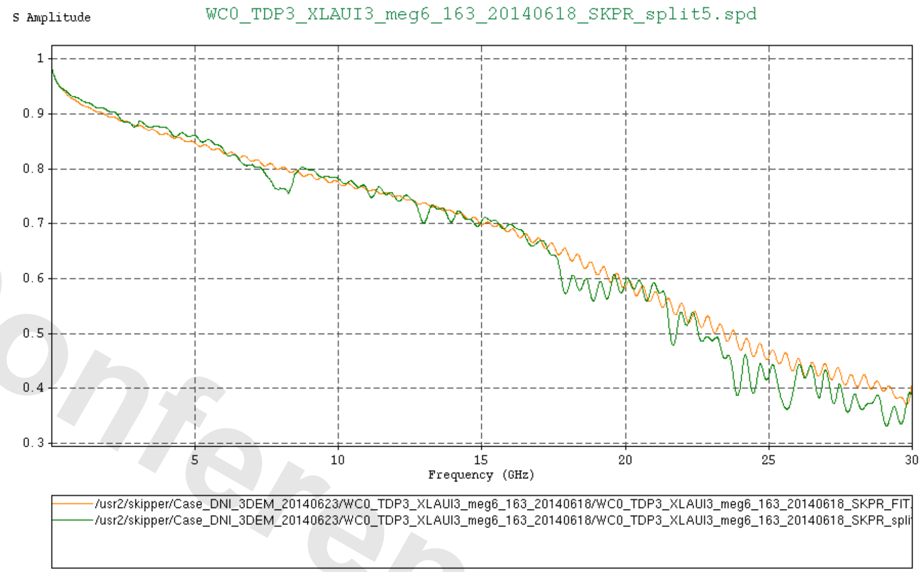
Case 2: 5 sections, 4 cuts



Cadence's "Cut and Stitch"

SDD21





4 Cuts Overall

13Cuts Overall

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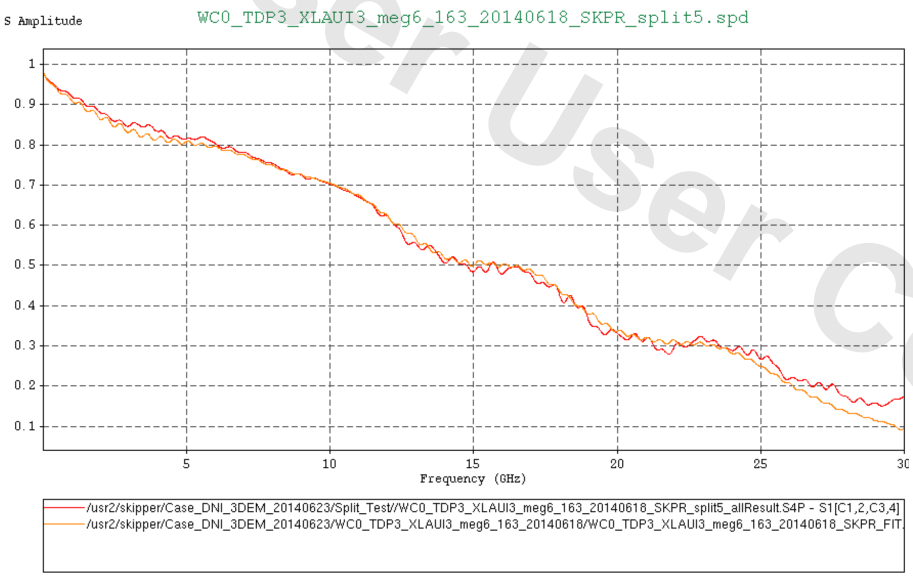
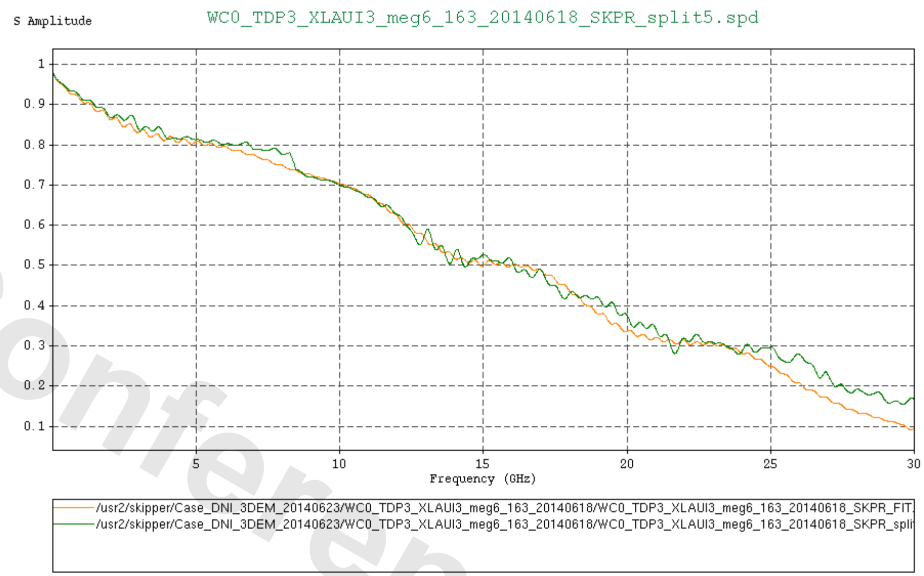
Cadence’ s “Cut and Stitch”

Scc21





4 Cuts Overall

13Cuts Overall

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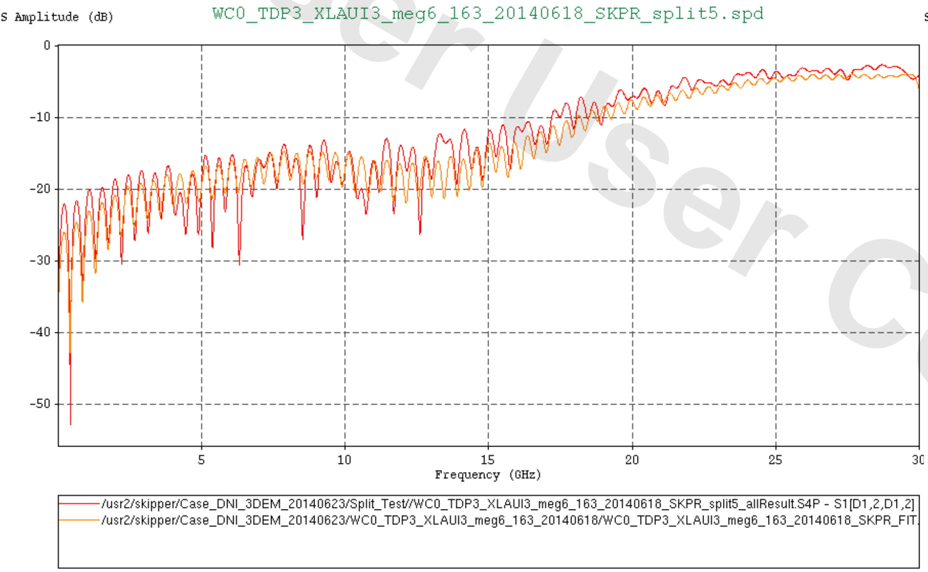
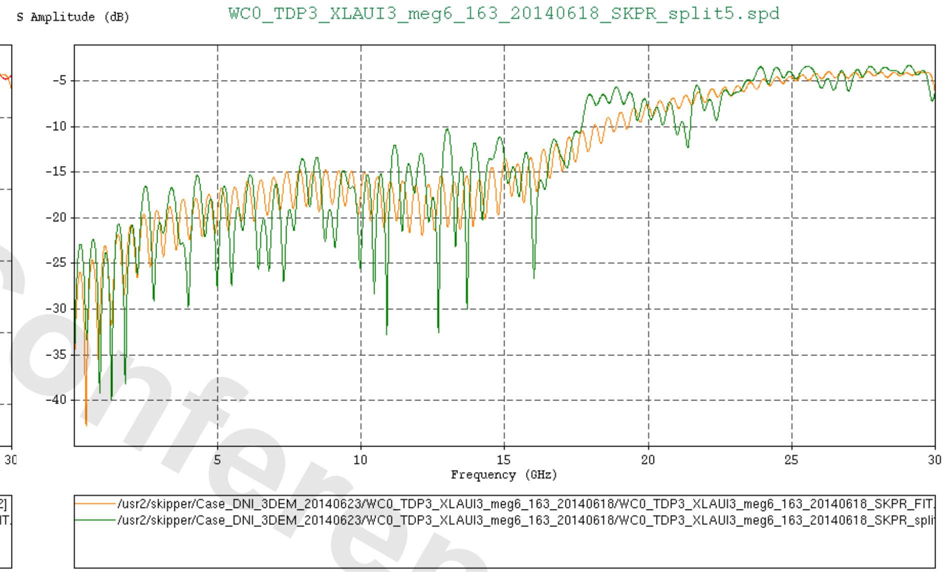
Cadence's "Cut and Stitch"

SDD11



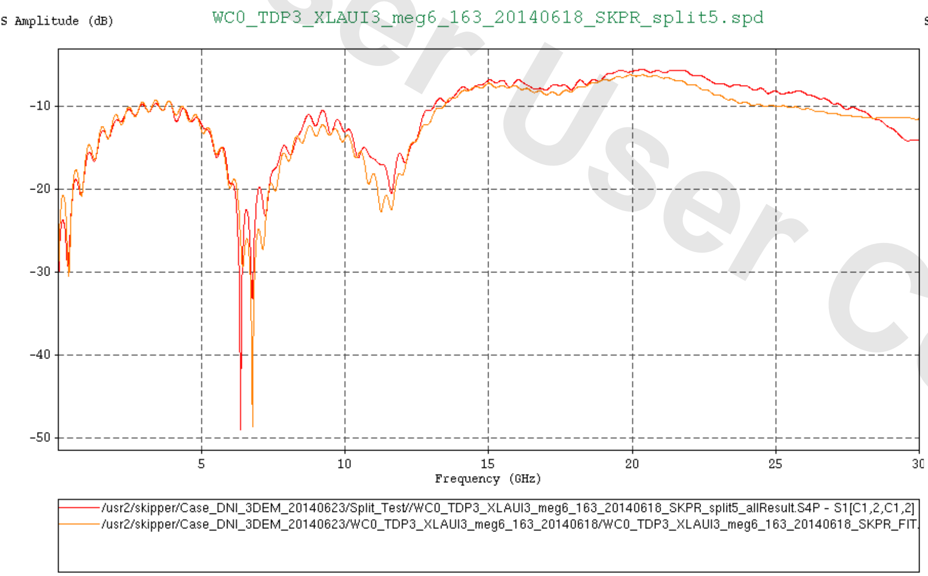


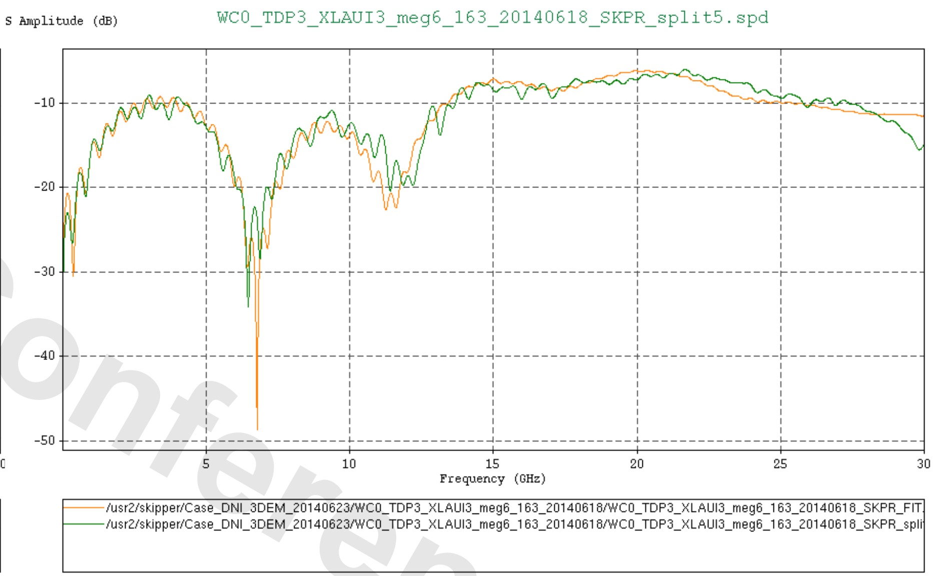
4 Cuts Overall

13Cuts Overall

Cadence’ s “Cut and Stitch”

Scc11



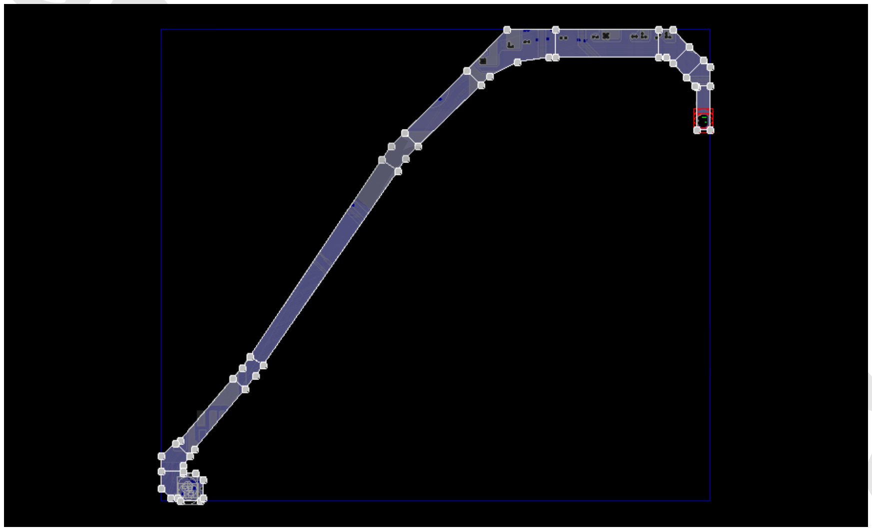


4 Cuts Overall

13Cuts Overall

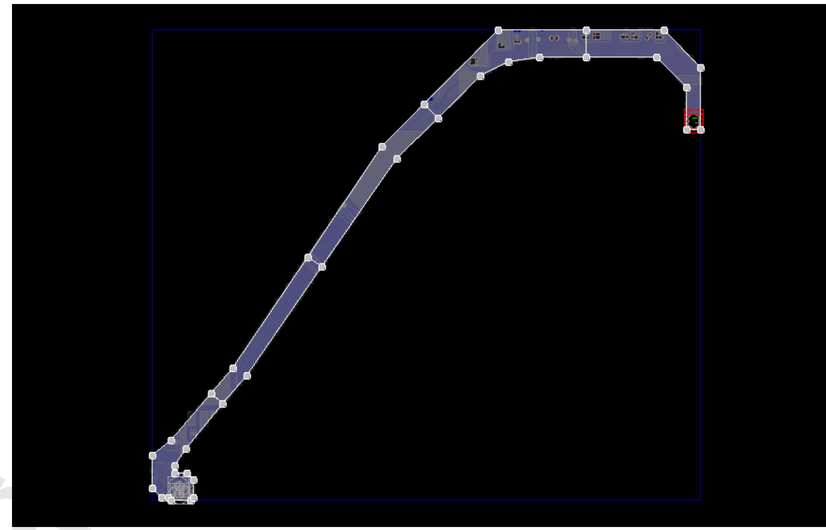
Cadence’s “Cut and Stitch”

Case 1: 13 sections, 12 cuts



6hr, 48mins, 9.32seconds

Case 2: 5 sections, 4 cuts



9hr, 34mins, 19.55seconds

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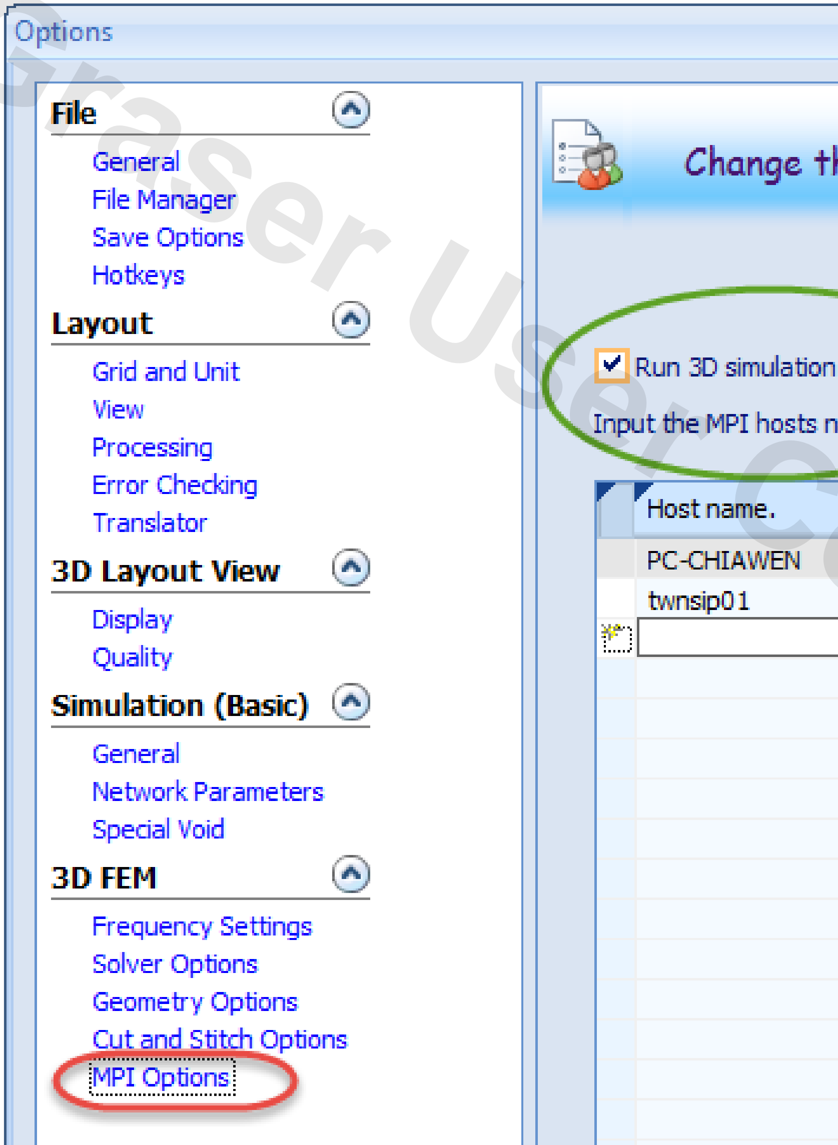
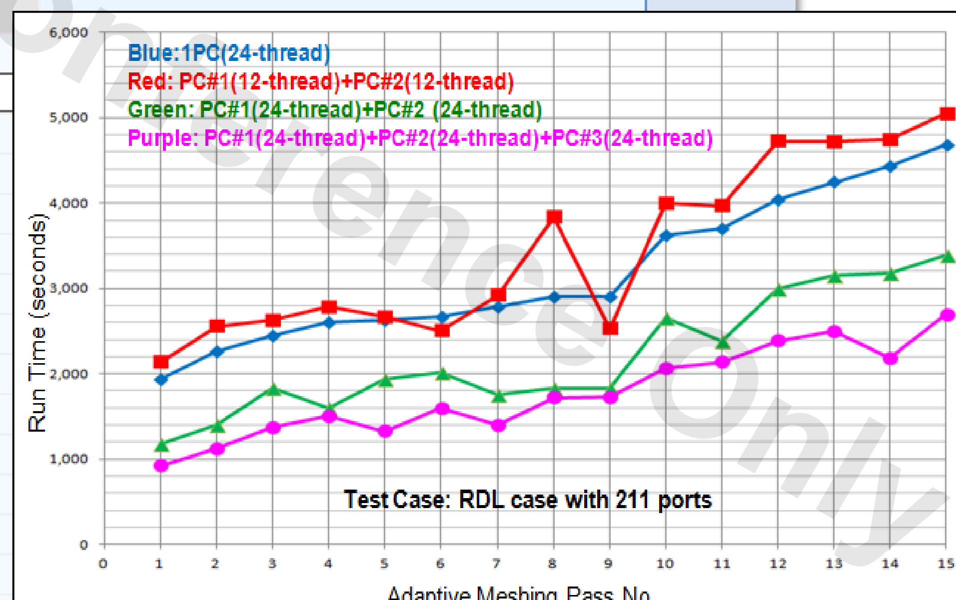
Parallel Processing



- 3D EM distributed computation is based on Message Passing Interface (MPI), by which the simulation time can be reduced dramatically.



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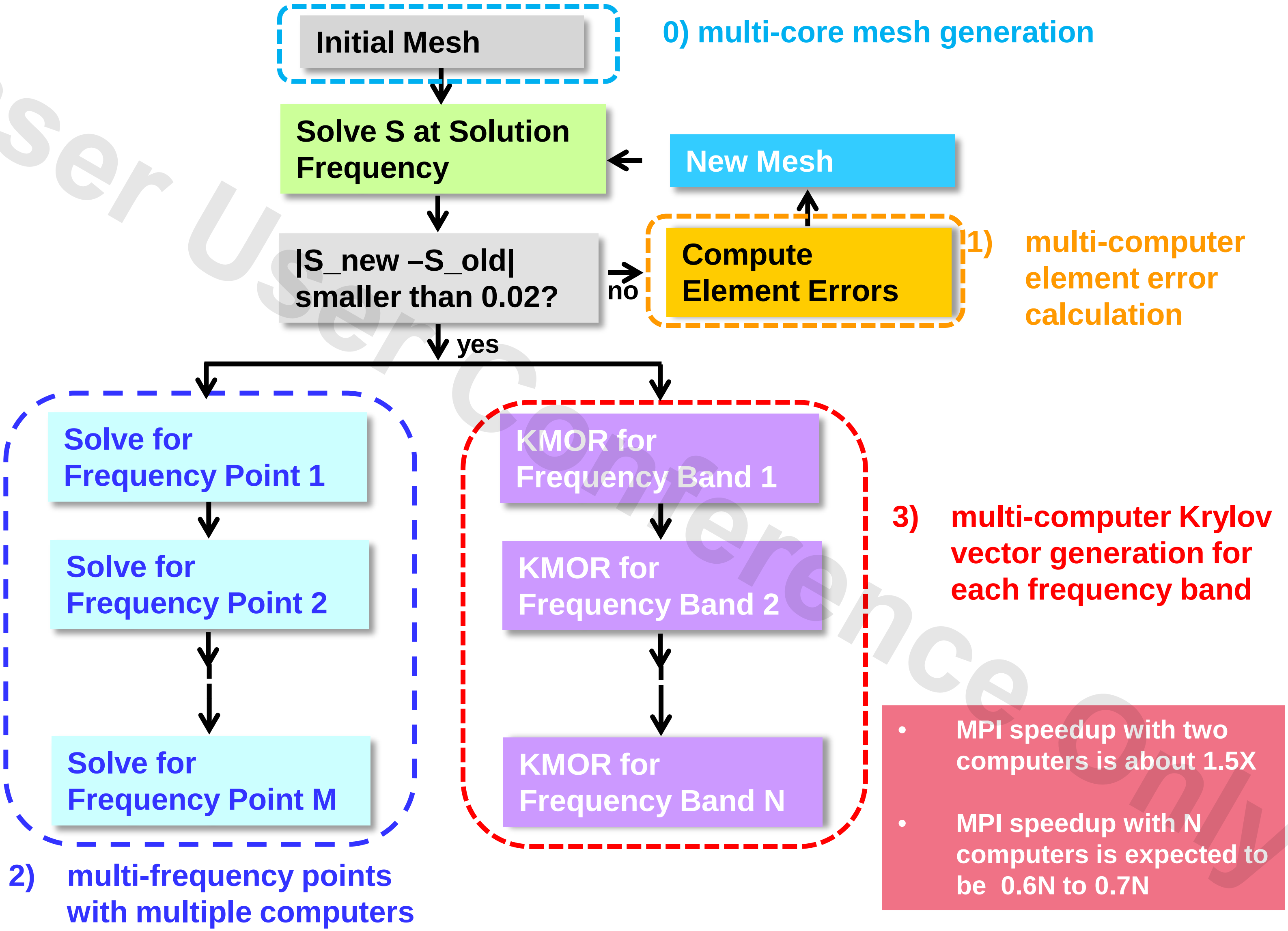
Parallel Processing



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Agenda

Problem/Challenge Today

3D Modeling
- ❑Why 3D
- ❑FEM – Finite Element Method
- ❑Inherent Defect of FEM
- ❑Cadence's "Cut and Stitch"
- ❑Parallel Processing

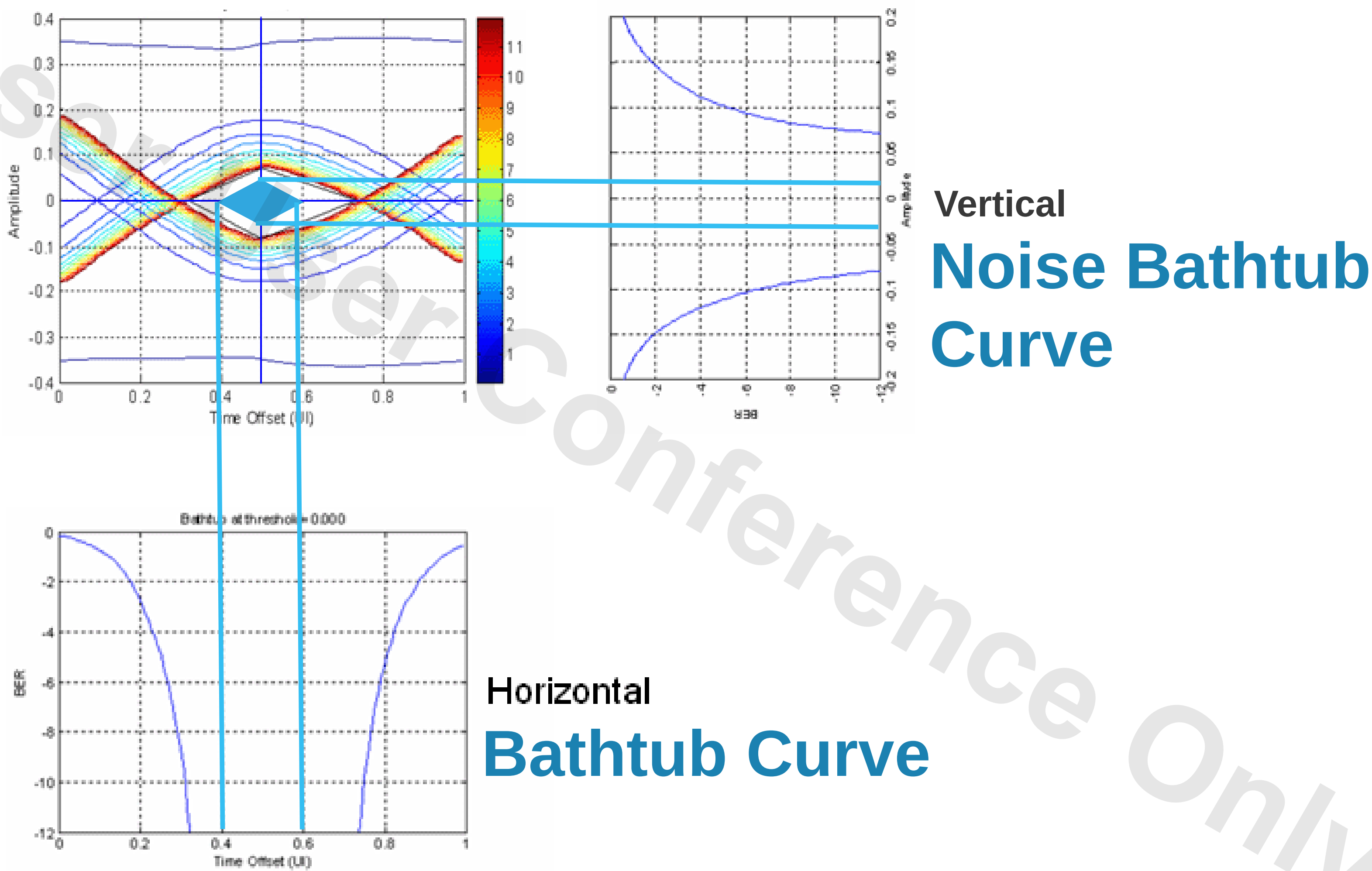
Massive Bit Transmission
- ❑BER – Bit Error Rate
- ❑Channel Response
- ❑Equalizer
- ❑Serial Link Analysis

Conclusions

BER-Bit Error Rate

- *Bit Error Rate* (BER) refers to the rate between error bits and total transferred bits. For example, to achieve BER less than 10^{-12}, you will try hard to make sure your system will meet one error bit (eye mask violation) after more than 10^{12} bits transferred.
- The most popular indicator for BER is “Bathtub Curve” and “Noise Bathtub Curve”.

BER-Bit Error Rate



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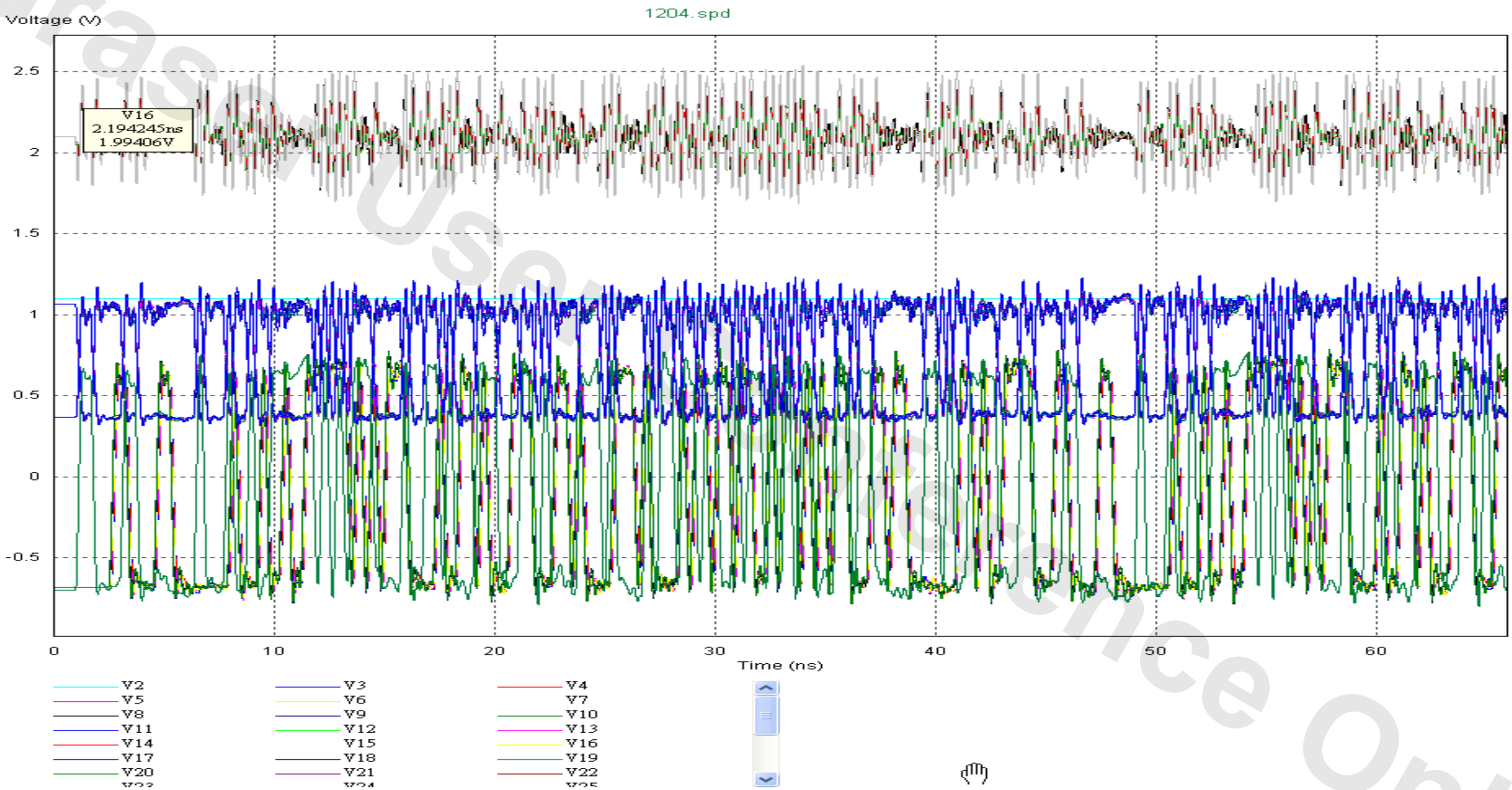
Channel Response

Using "**Circuit Simulator**":



128bits → 1hr 47min

1,000,000,000,000bits → ???

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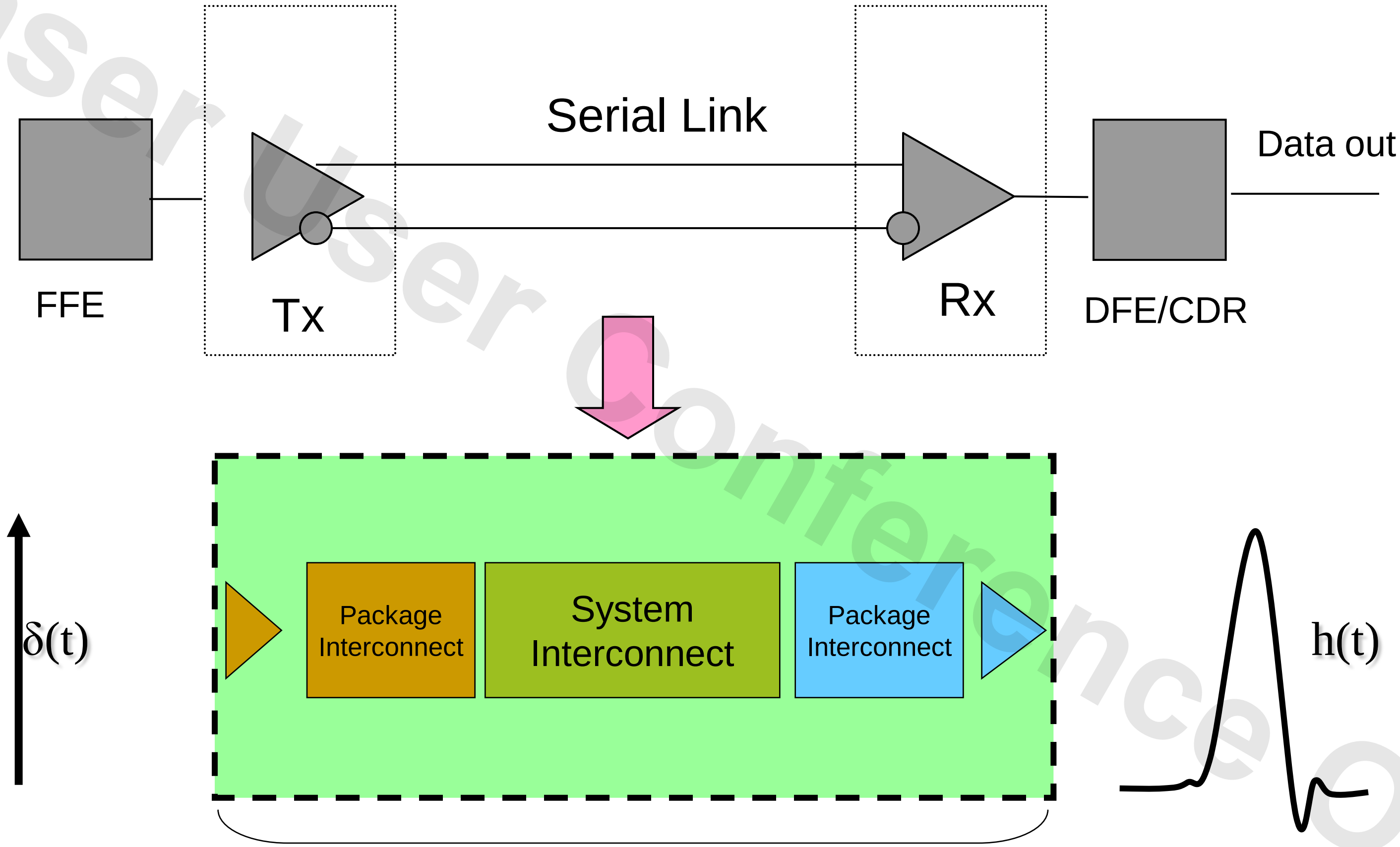
Channel Response



Channel's Impulse Response

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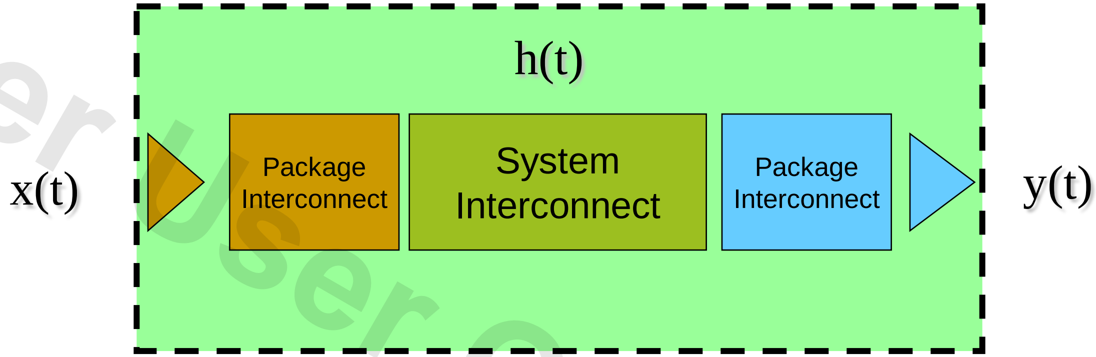
Channel Response

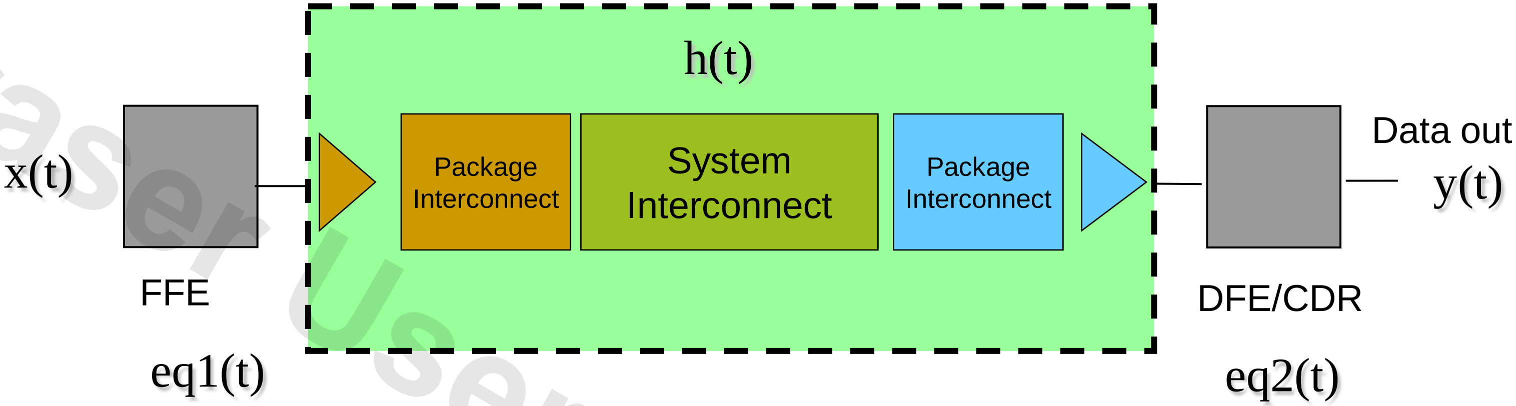


$$\mathbf{y}(t) = \mathbf{h}(t) * \mathbf{x}(t) = \int_{-\infty}^{\infty} \mathbf{h}(t-\tau)\mathbf{x}(\tau)d\tau$$

$$Y(f) = X(f) \cdot H(f)$$

Where $\mathbf{y}(t) \overset{F}{\equiv} Y(f), x(t) \overset{F}{\equiv} X(f), h(t) \overset{F}{\equiv} H(f)$

Equalizer



$$Y(f) = X(f) \cdot EQ1(f) \cdot H(f) \cdot EQ2(f)$$

An Ideal equalizer will compensate the distortion effect of the channel in the following way:

$$EQ1(f) \cdot EQ2(f) = H^{-1}(f)$$

Then:

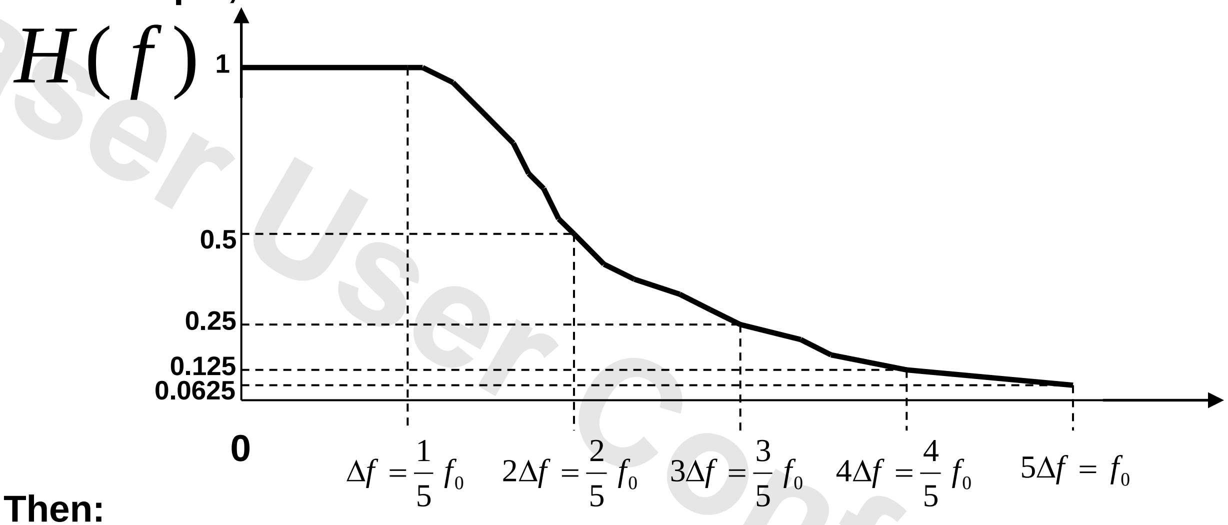
$$\begin{aligned} Y(f) &= X(f) \cdot EQ1(f) \cdot H(f) \cdot EQ2(f) \\ &= X(f) \cdot H(f) \cdot H^{-1}(f) = X(f) \end{aligned}$$

And

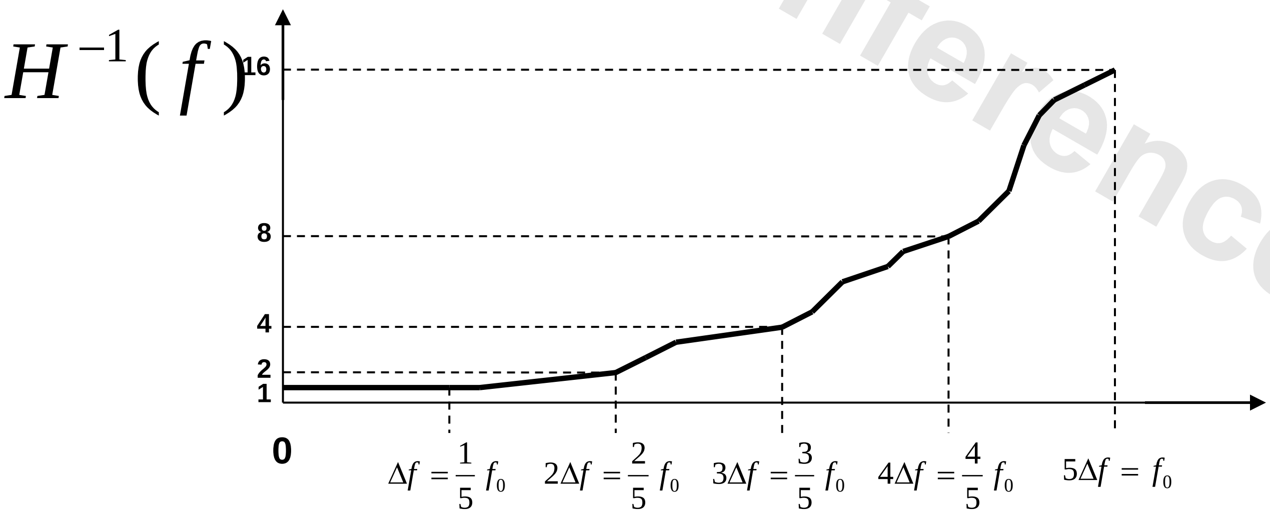
$$h(t) * h^{-1}(t) = \underbrace{\delta(t)}_{\text{Impulse}} \Leftrightarrow H(f) \cdot H^{-1}(f) = 1$$

Equalizer

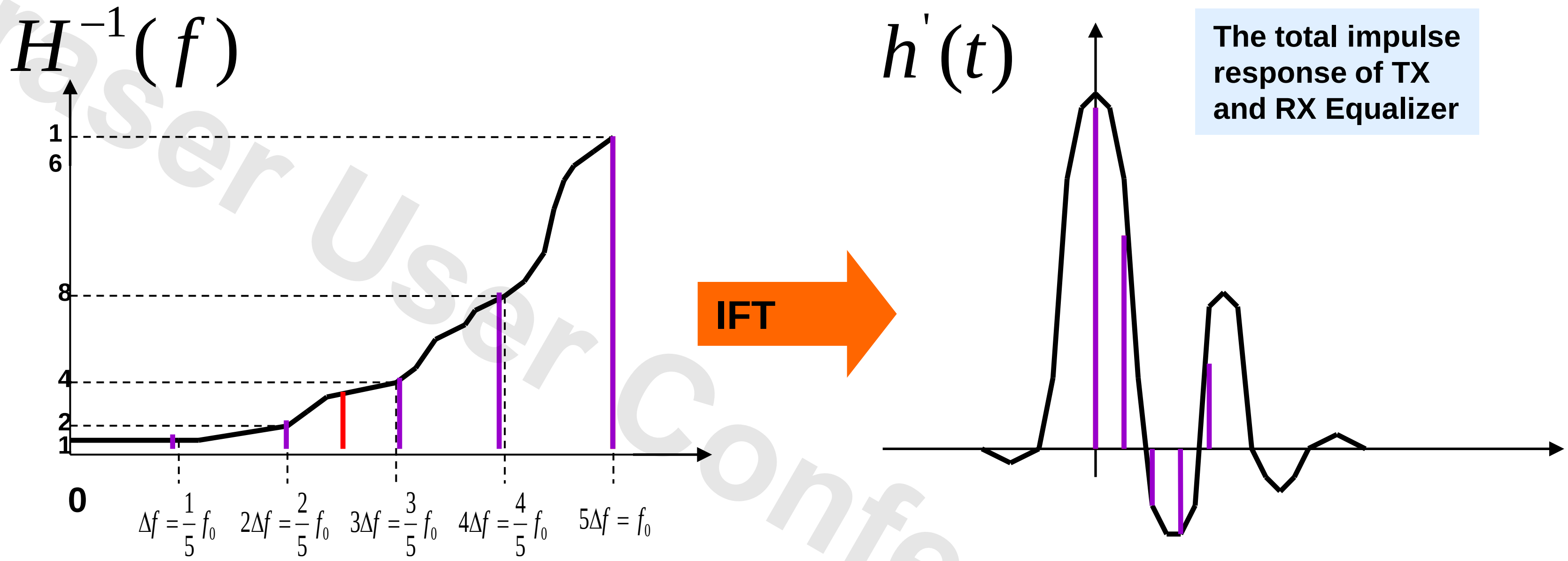
For Example, if:



Then:



Equalizer



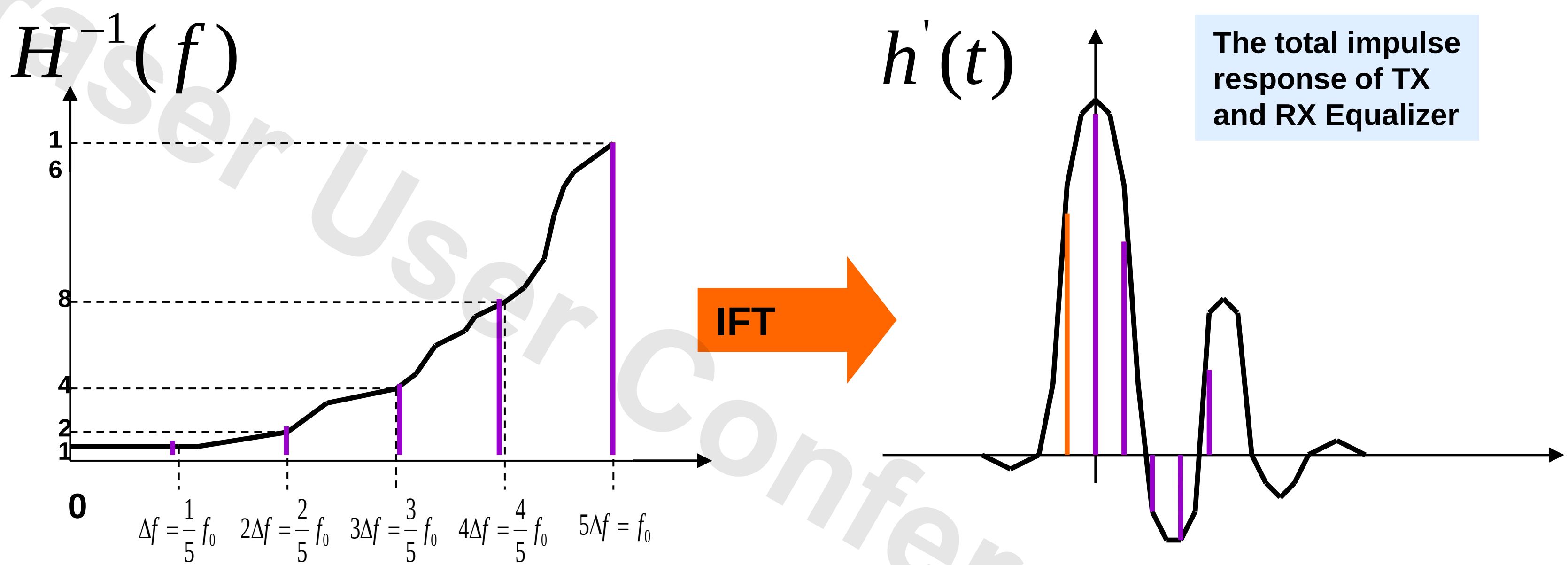
1. Select f_0; f_0 is the maximum frequency range where the spectrum of the signal take effect.
2. f_0 will decide the size of Δt on time axis, A.K.A "Tap".
3. Select how many post-taps you want to implement into your Equalizer.

2 taps?

5 taps?

The More Taps, The Better!!

Equalizer



4. Select how many pre-taps you want to implement into your Equalizer.

0 taps?

1 taps?

The More Taps, The Better!!

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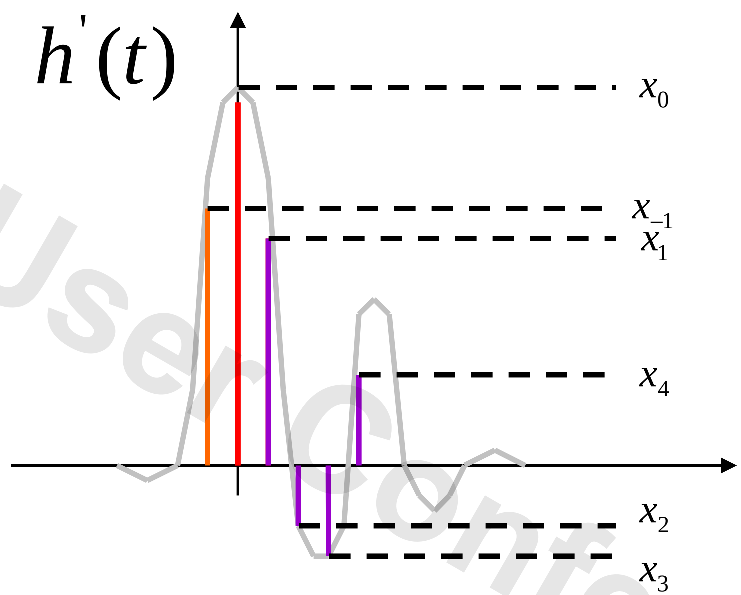
Equalizer



$$h_{Equalizer}(t) = \underbrace{x_{-1}\delta(t+\Delta t)}_{\text{Pre-Cursor}} + \underbrace{x_0\delta(t)}_{\text{Main-Cursor}} + \underbrace{x_1\delta(t-\Delta t) + x_2\delta(t-2\Delta t) + x_3\delta(t-3\Delta t) + x_4\delta(t-4\Delta t)}_{\text{Post-Cursor}}$$

Where:

$\delta(t)$ **is Dirac Delta Function, A.K.A Impulse**

Δt **is the size of a "Tap".**

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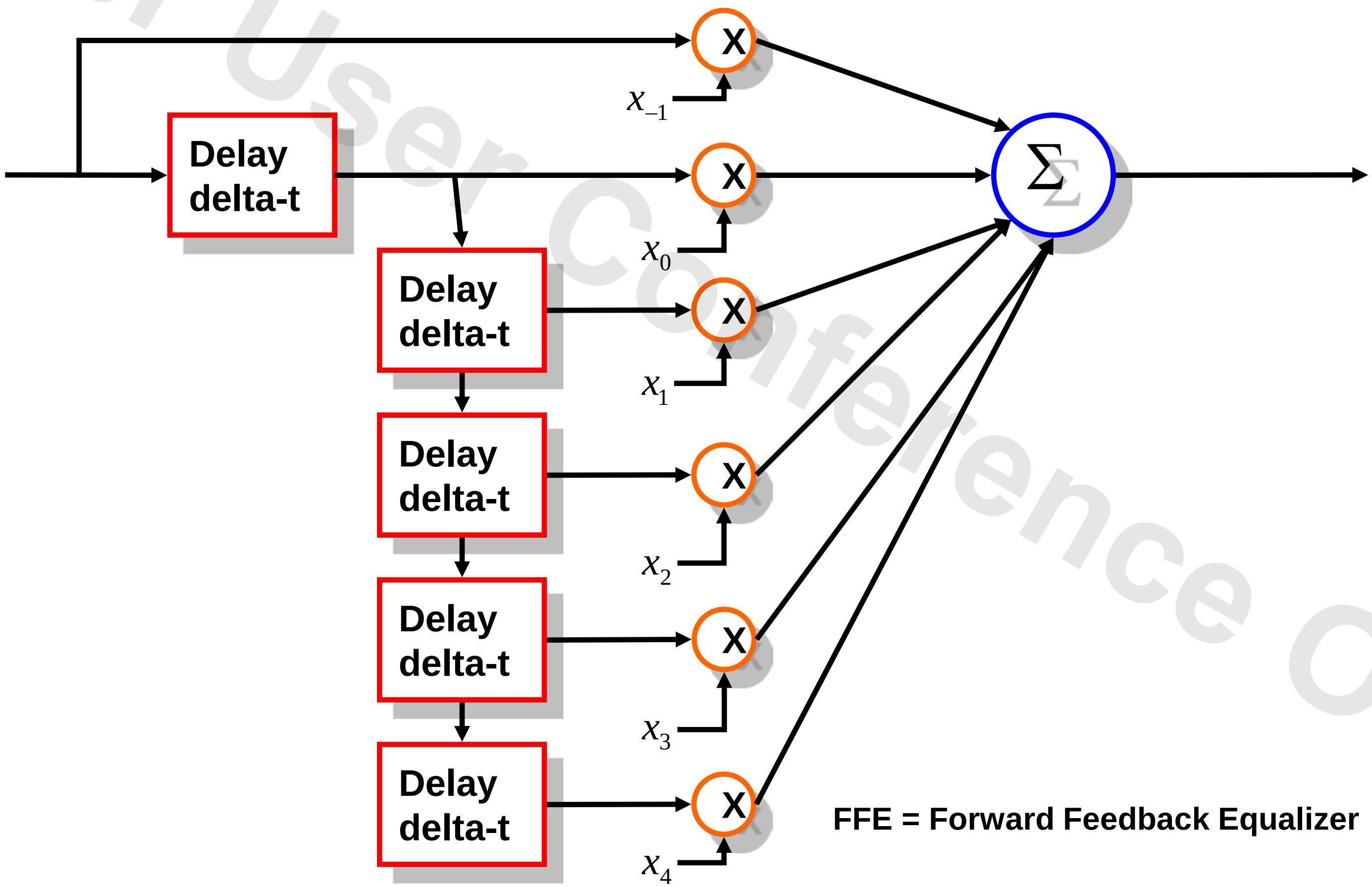
Equalizer

$$h_{Equalizer}(t) = x_{-1}\delta(t+\Delta t) + x_0\delta(t) + x_1\delta(t-\Delta t) + x_2\delta(t-2\Delta t) + x_3\delta(t-3\Delta t) + x_4\delta(t-4\Delta t)$$



FFE = Forward Feedback Equalizer

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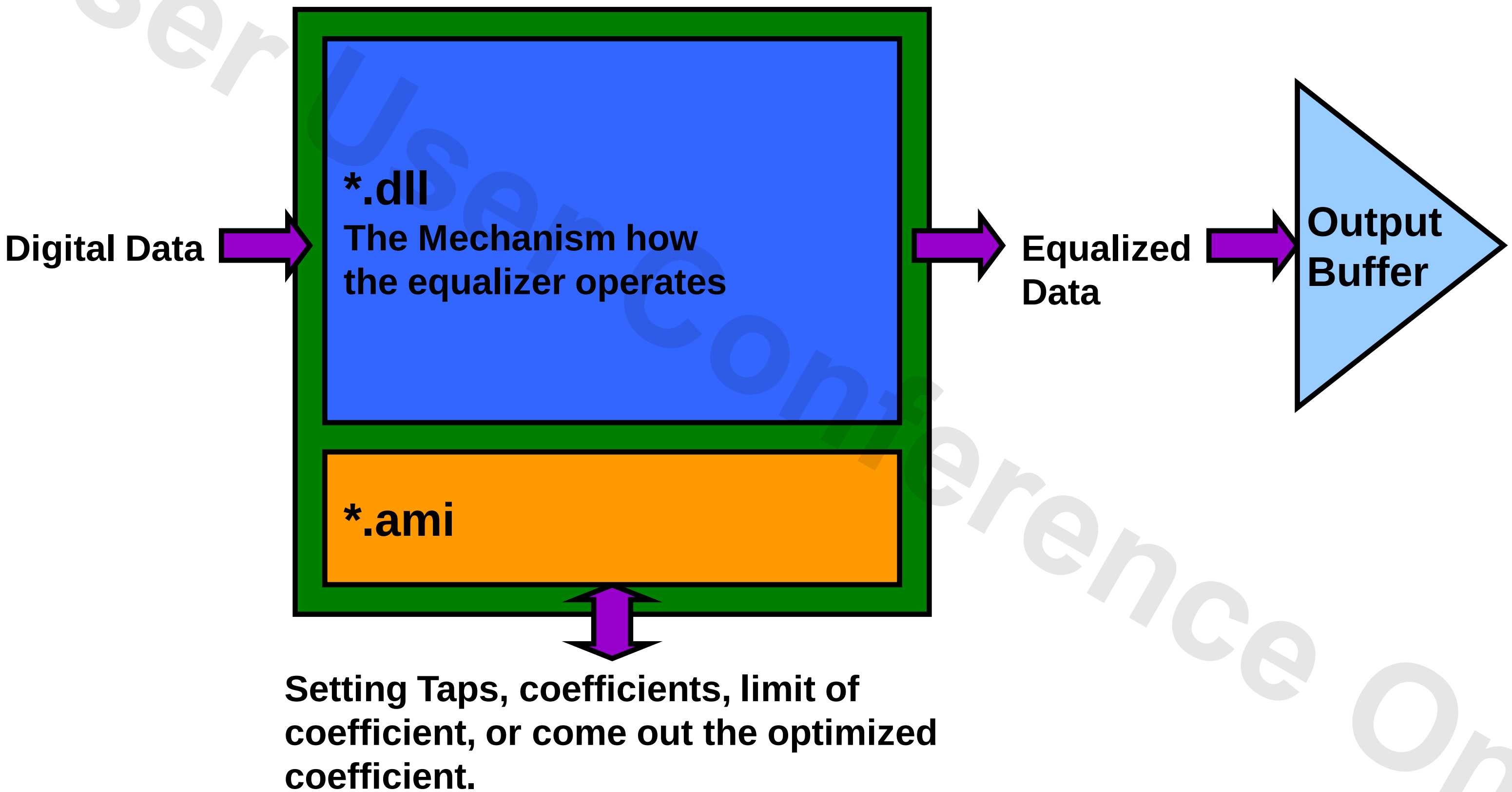
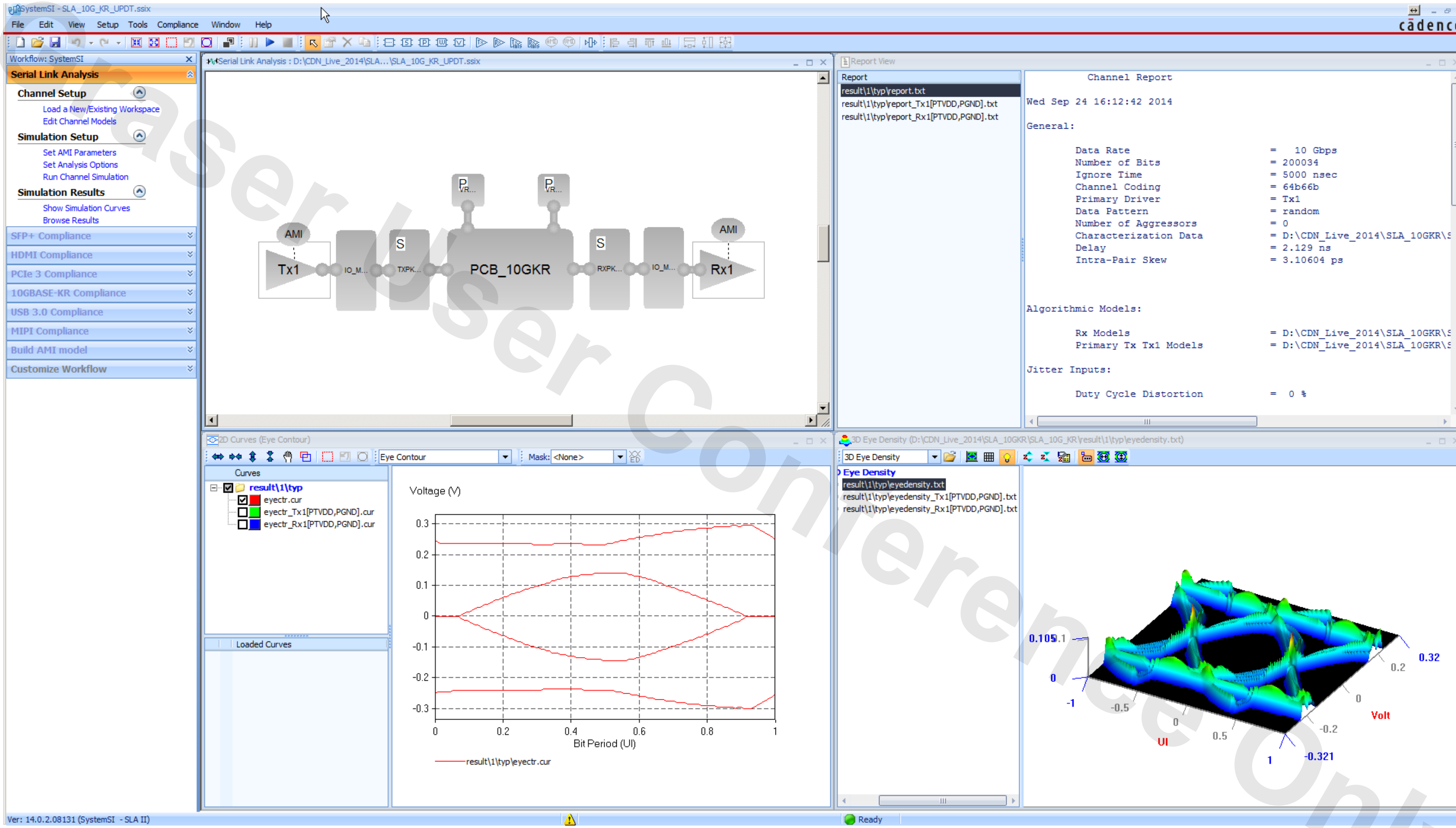
Equalizer

Mostly, a digital equalizer's behavior will be described by AMI model:



Serial Link Analyze



BER=1e-16 ➡ **15min**

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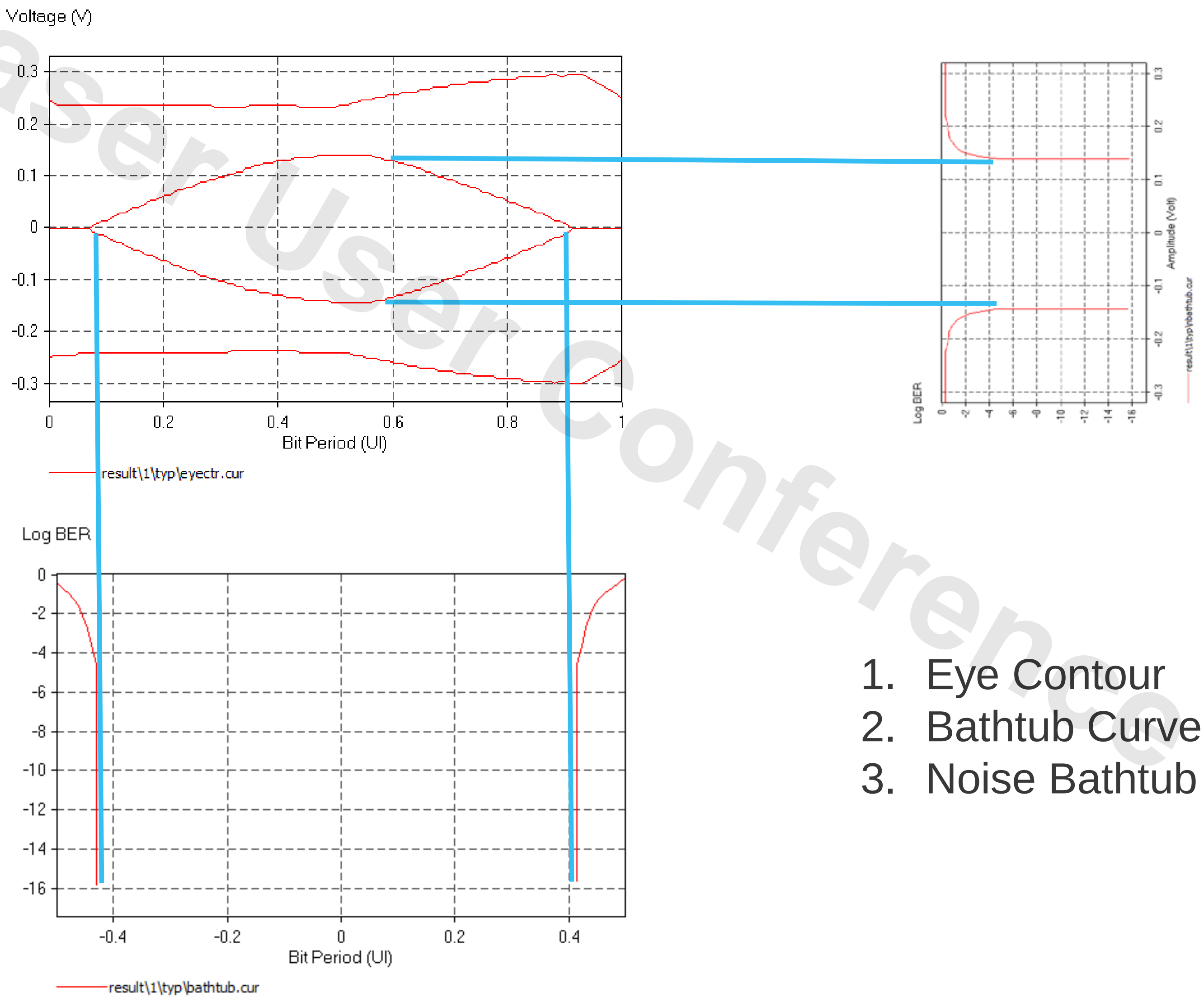
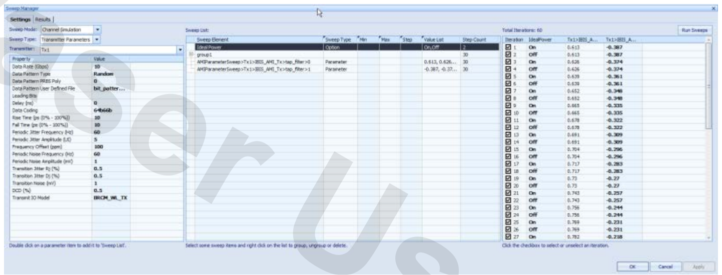
Serial Link Analyze

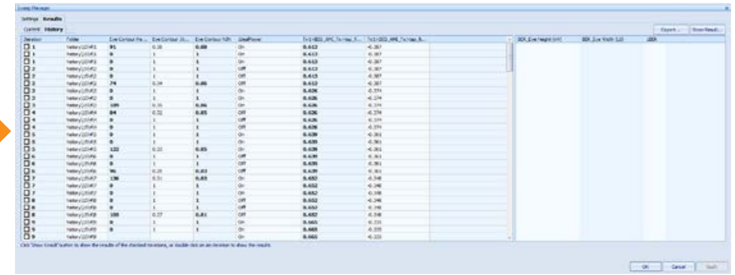


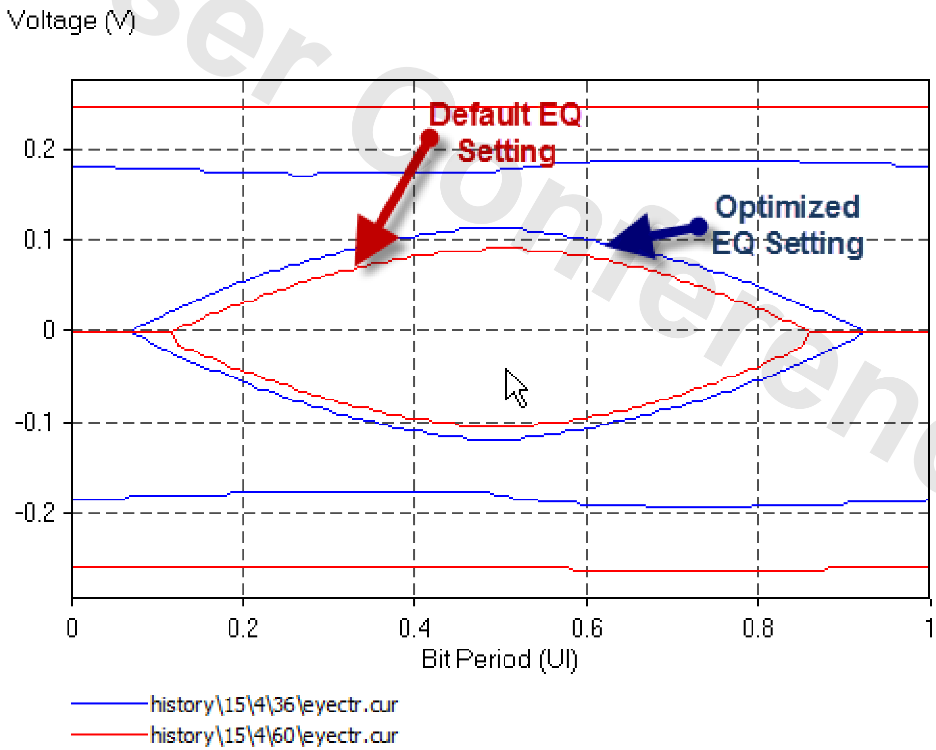
1. Eye Contour
2. Bathtub Curve
3. Noise Bathtub

Serial Link Analyze

Sweep Manager → Equalizer Optimization







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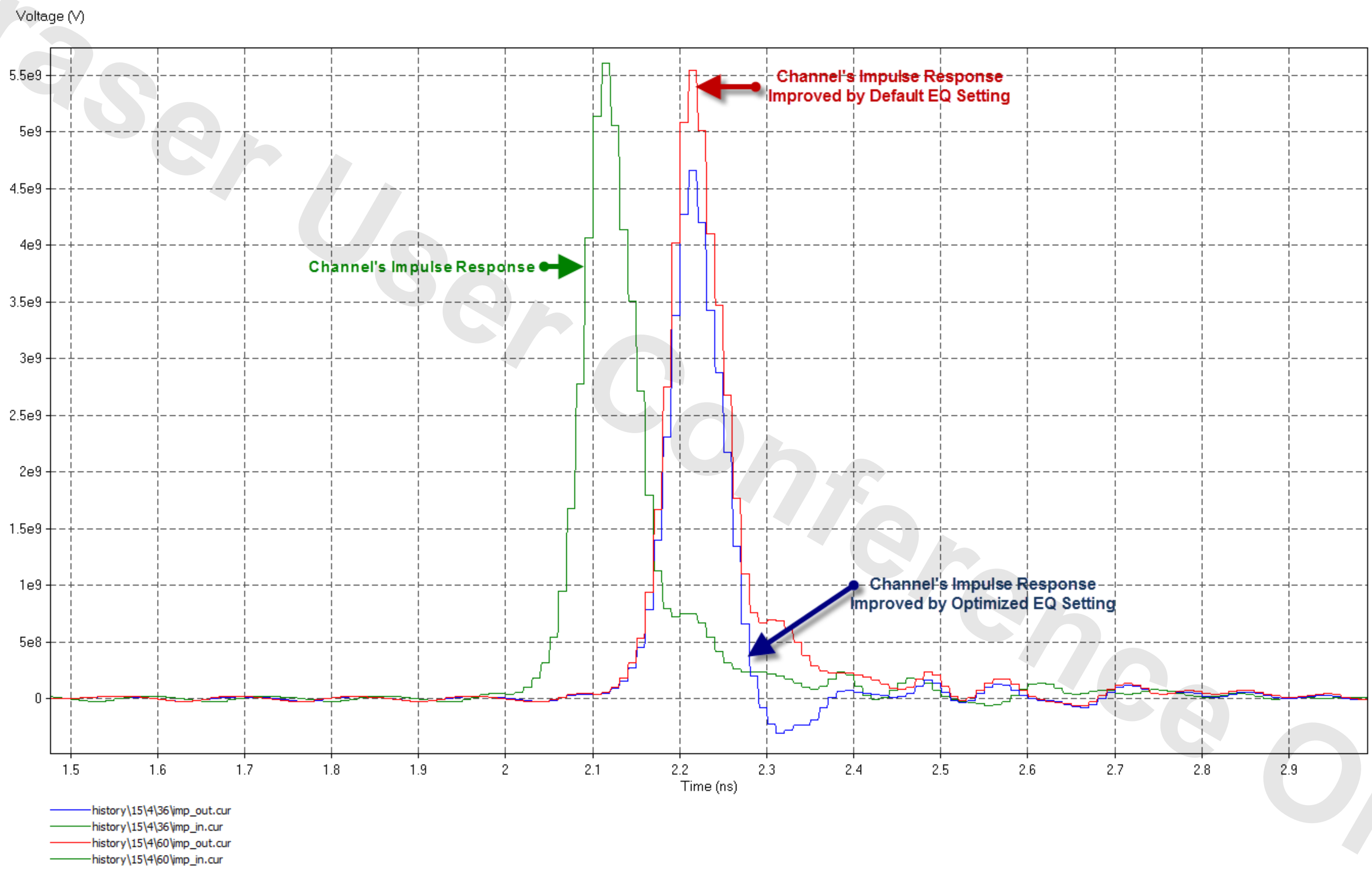
Serial Link Analyze



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Compliance Check

Printout ready

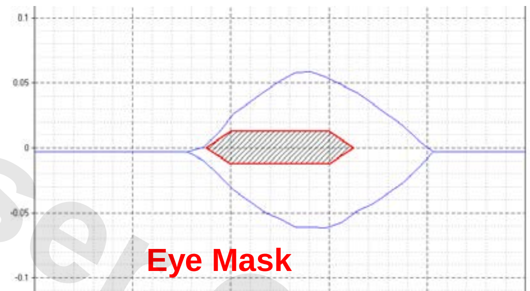
Hyperlinked to curves for easy access

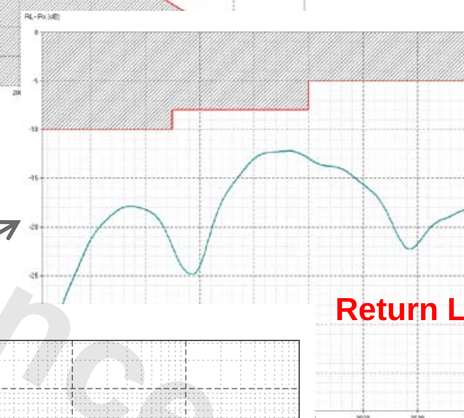
PCI Express Gen 3 Compliance Report

Generated by Cadence SystemSI, 13.0.a0.09122
19th of September 2013

Useful Links:

- Cadence website: http://www.cadence.com
- PCI Express® Base Specification: http://www.pcisig.com/specifications/pciexpress/base3/





Summary of Results

This report shows the results of the 8.0 GT/s channel compliance testing specified by PCI-SIG using Cadence SystemSI.
The channel simulated violates one or more PCI Express Gen 3 compliance requirements.

Channel Tolerancing Eye Mask Values

Item	Value	Simulation Results		Pass/Fail
Eye Height	25 mV	$V_{RX\text{-}CH\text{-}EH}$ (mV)	120.412	Pass
Eye Width at Zero Crossing	0.3 UI	$T_{RX\text{-}CH\text{-}EW}$ (UI)	0.463	Pass
Peak EH Offset from UI Center	±0.1 UI	$T_{RX\text{-}DS\text{-}OFFSET}$ (UI)	0.063	Pass
Range for DFE d_1 Coefficient	±30 mV	$V_{RX\text{-}DFE\text{-}COEFF}$ (mV)	28.844	Pass
Eye Mask		Eye Mask		Pass

Differential Insertion Loss

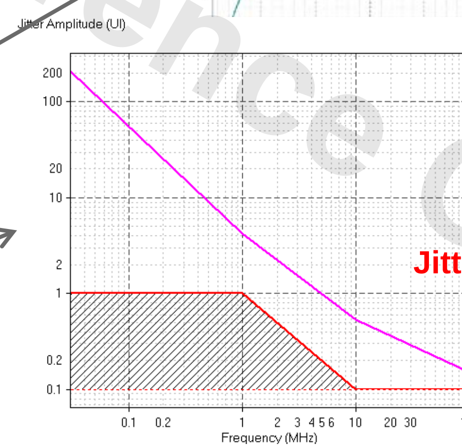
Item	Value	Simulation Results	Pass/Fail
Insertion Loss	Breakout Channel Only	SDD21 - Breakout	Fail
	Breakout + Short Calibration Channel	SDD21 - Short	Pass
	Breakout + Long Calibration Channel	SDD21 - Long	Fail

Differential Return Loss

Item	Value	Simulation Results	Pass/Fail
Tx Return Loss		RL - Tx	Fail
Rx Return Loss		RL - Rx	Pass

Stressed/Swept Jitter Test

Item	Value	Simulation Results	Pass/Fail
Stressed/Swept Jitter		Jitter	Pass



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Massive Bit Transmission
- ❑BER – Bit Error Rate
- ❑Channel Response
- ❑Equalizer
- ❑Serial Link Analysis

Conclusions

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Conclusions

- The demand to reduce cost while increasing performance is creating significant design challenges
- Modeling multi-gigabit data channels requires accurate 3D extraction techniques
- Utilizing cut and stitch along with parallel computing in an integrated design and analysis environment allows designers to tune multi-gigabit channels
- Connecting IBIS-AMI models to cascaded s-parameter models using high capacity simulation techniques can verify your interface is compliant with Serial Link standards
- Allegro Sigrity SI Base + System Serial Link SI Option accelerates your time to final product creation

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