System Level SI Testbench and DDR4 Design

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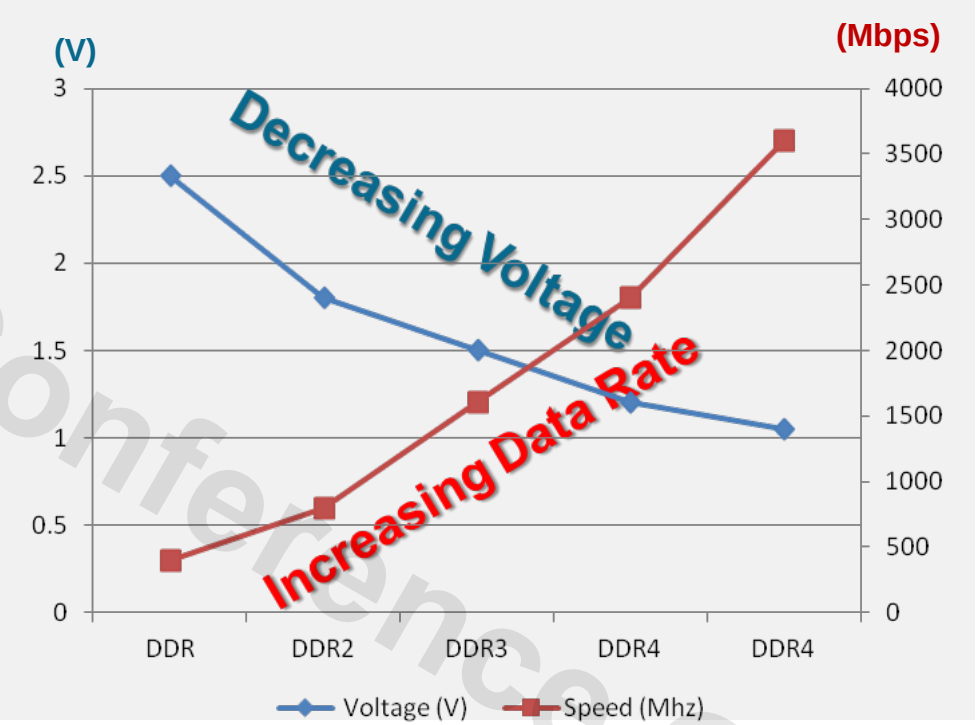
Agenda

- Introduction
- DDR4 Analysis Challenges
- Allegro Sigrity Solution
- Summary

Introduction

DDR Evolution

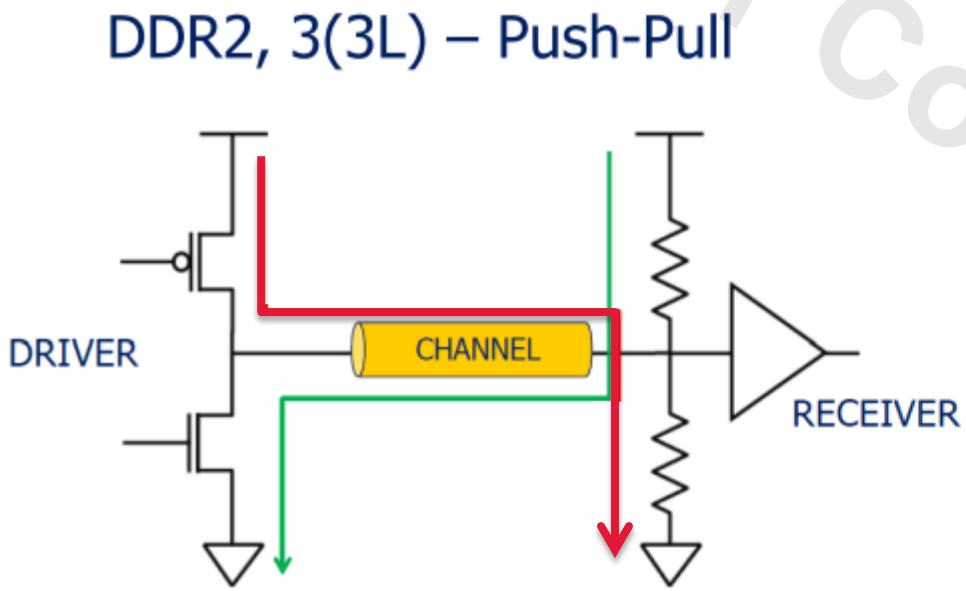
Features/Options	DDR4
Voltage (VDD/VDDQ/VPP)	1.2V/1.2V/2.5V
Vref Inputs	Internal
VREFDQ Calibration	Supported/Required
Data Rate - Mb/s	1600~3200
DQ IO	POD12
CMD/ADDR IO	CTT
Bank Group	4
Data Bus Write CRC	Supported
Data Bus Inversion (DBI)	Supported

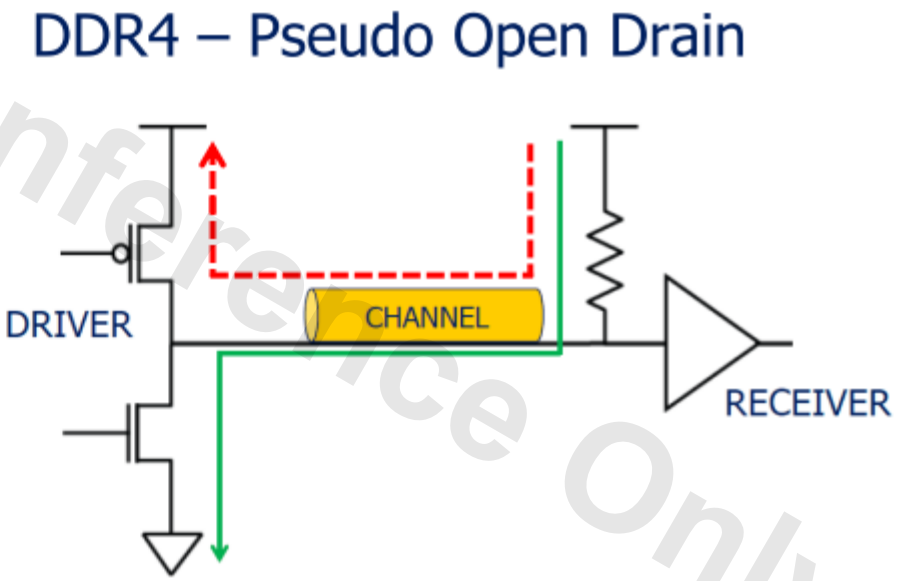


- **Timing budget = 93ps @ 2133 Mbps**
- **5% ripple tolerance down to 60 mV**
- **SSN effects impact timing and noise budget**

I/O Interface – Pseudo Open Drain

- DDR2, DDR3 consume power at state 1 and 0.
- DDR4 consumes power at state 0.

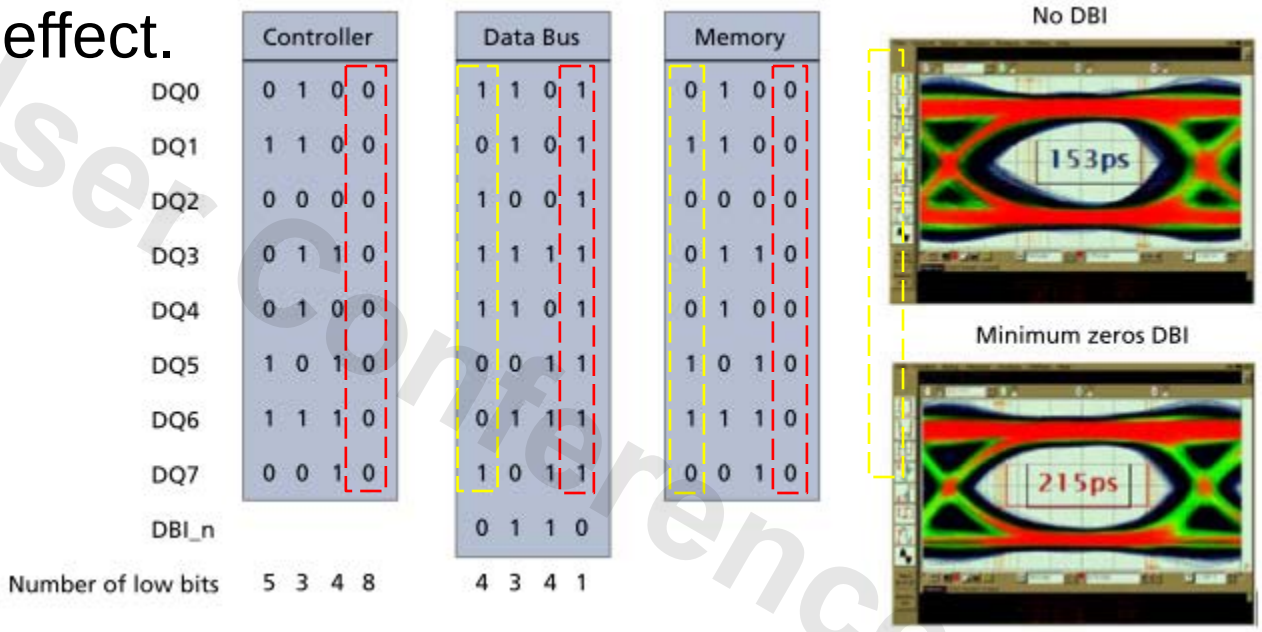




http://www.micron.com/-/media/documents/products/technical%20note/dram/tn_4003_ddr4_network_design_guide.pdf

Data Bus Inversion (DBI)

- Drives fewer bits LOW
- Enables fewer bits switching
- Minimizes SSO effect.

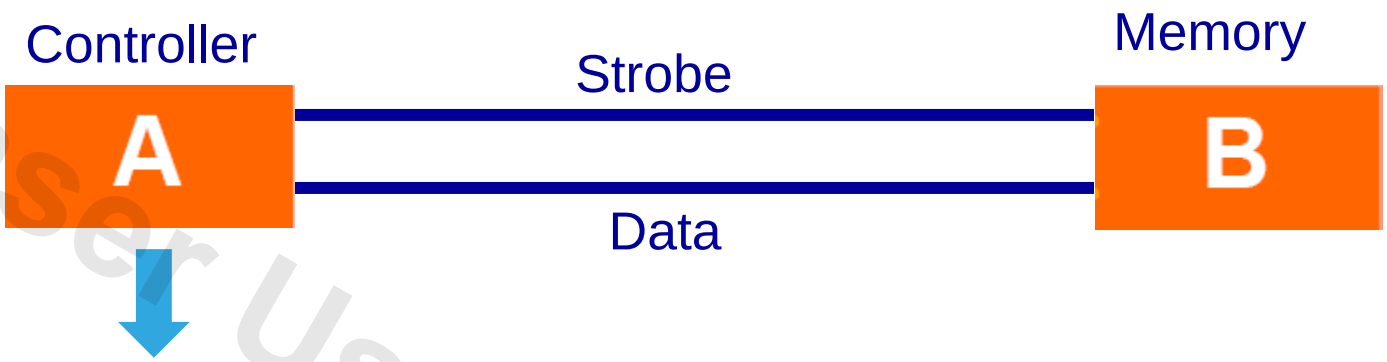


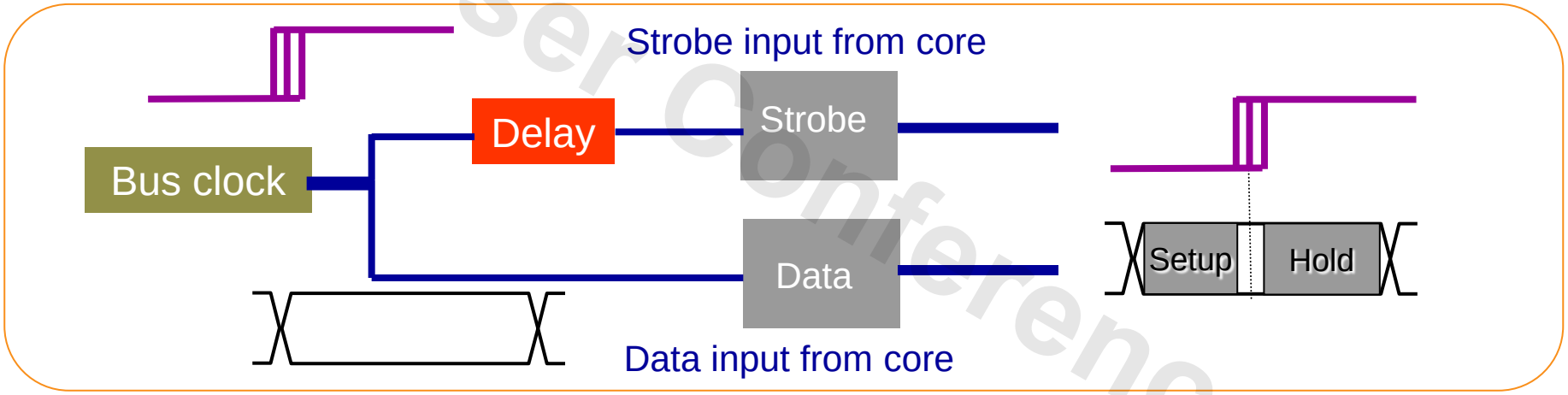
Read	Write
If more than four bits of a byte lane are LOW: – Invert output data – Drive DBI_n pin LOW	If DBI_n input is LOW, write data is inverted – Invert data internally before storage
If four or less bits of a byte lane are LOW: – Do not invert output data – Drive DBI_n pin HIGH	If DBI_n input is HIGH, write data is not inverted

http://www.micron.com/-/media/documents/products/technical%20note/dram/tn_4003_ddr4_network_design_guide.pdf

DDR4 Analysis Challenges

Source Synchronous Bus

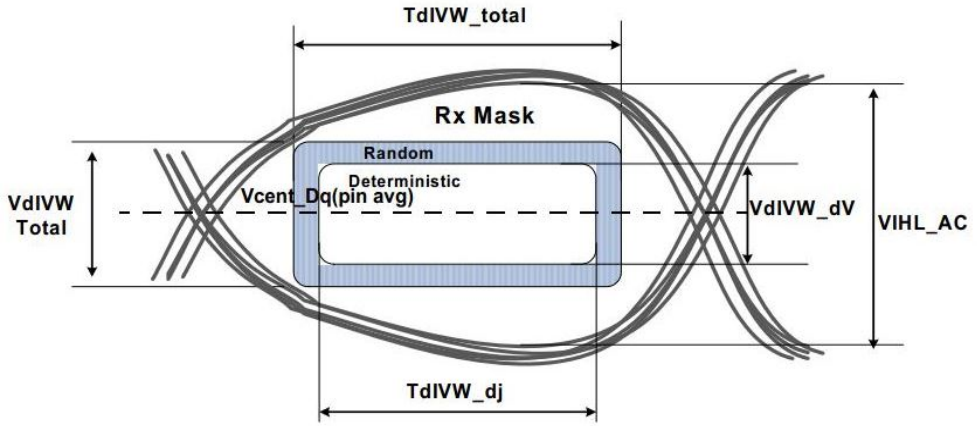


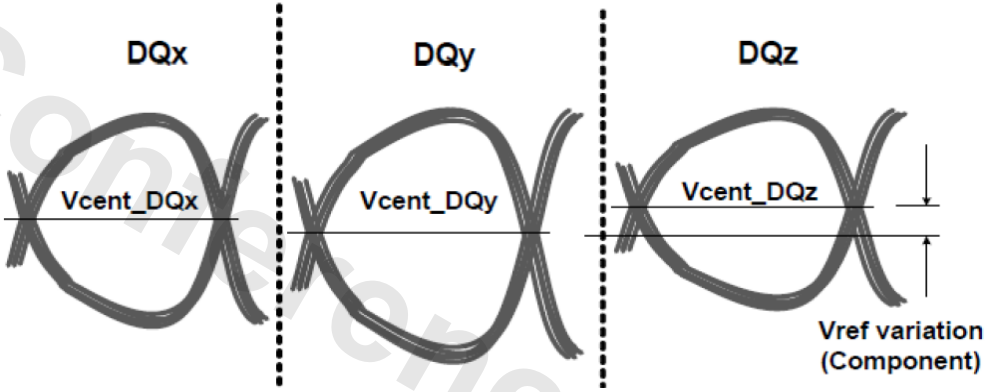


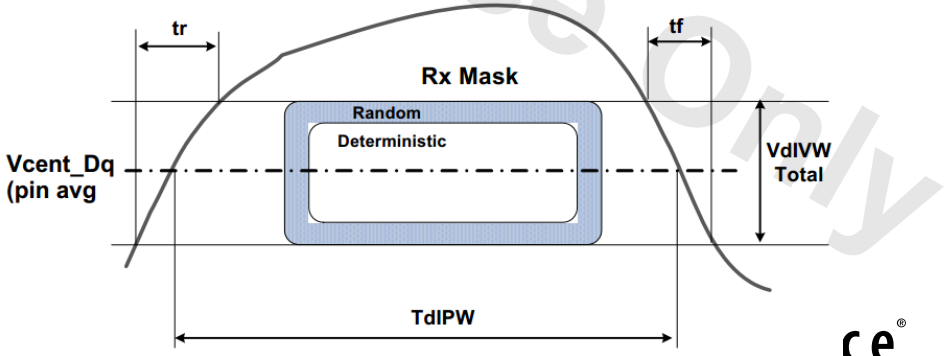
- Data & clock is instead of data & strobe in source synchronous system.
- Launched time for data and strobe at drivers are controlled by bus clock. Strobe launched lately by a delay unit.

DDR4 DQ Rx Compliance Mask

- DQ mask is instead of Step/Hold time.
- DDR4-2133
  - VdIVW_total/dv = 136 mv
  - TdIVW_total/dj = 0.2 UI
- Vcent_DQ(pin avg) is measuremed on-the-fly
- Input Slew Rate over VdIVW_total
  - SRIN_dIVW = 9 V/ns





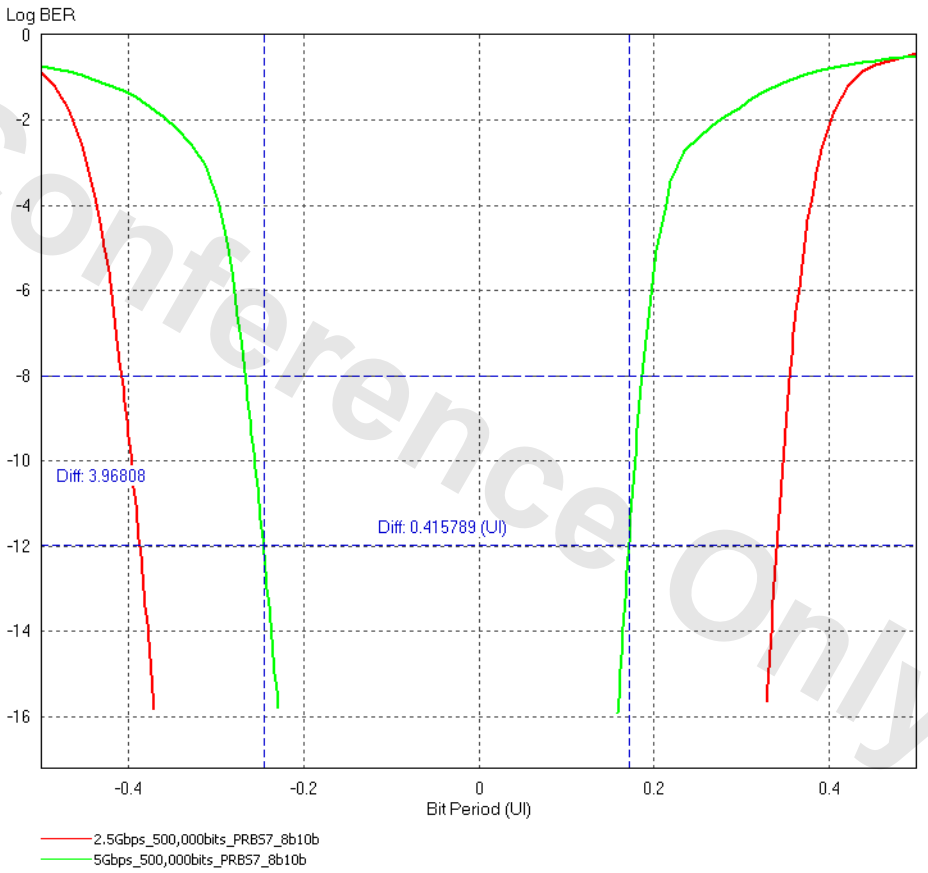


JEDEC DDR4 SPEC.

BER is Matter in DDR4

- DDR technology offers data rates of 3.2Gb/s or higher.
- Noise and jitter affect the signal integrity and its overall reliability.
- DDR4 spec defines the data-valid window in terms of a BER of 1E-16

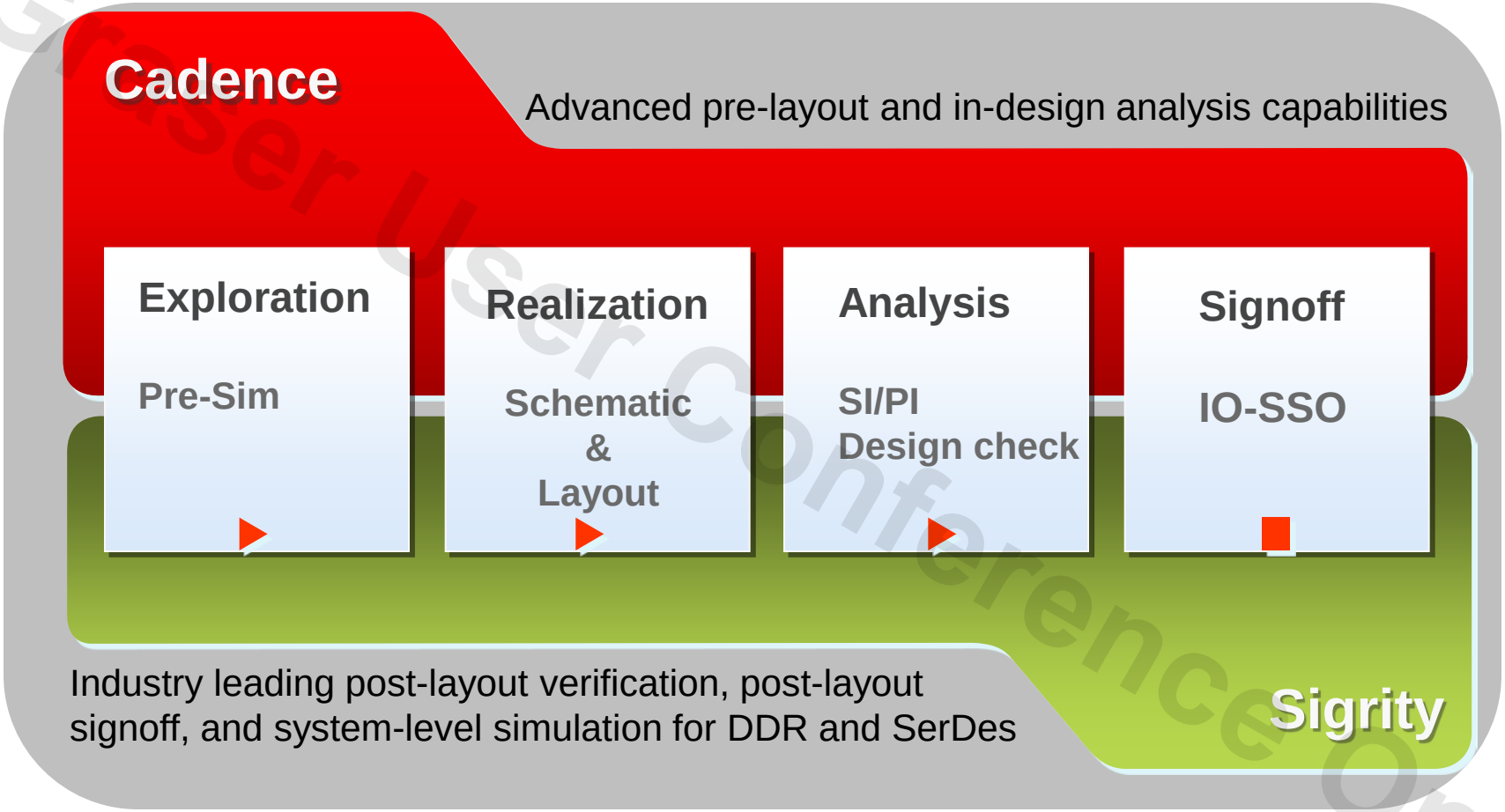
LONG LONG … TIME TO RUN MILLION BITS IN TD SIMULATION



Allegro Sigrity Solutions - Power Aware DDR4 Analysis

Front to Back DDR Design and Analysis

Allegro / OrCAD with Sigrity
Comprehensive Front-to-Back Solution



- Allegro Sigrity SI Base enables:
  - First order (ideal power/ground) analysis
- Allegro Sigrity SI Options enable:
  - Detailed sign-off analysis including 3D Full-Wave modeling

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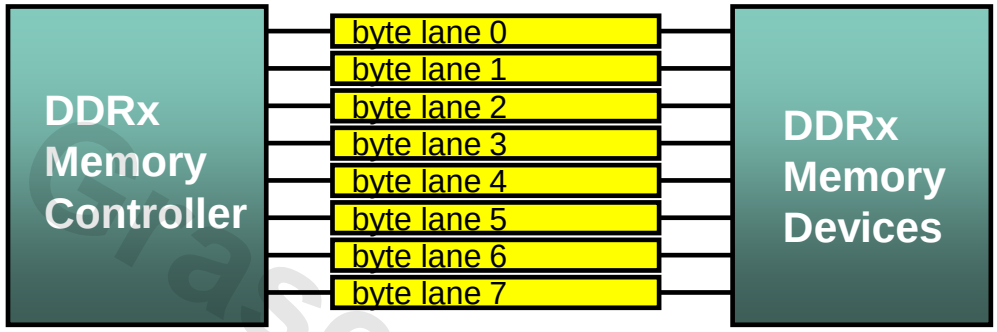

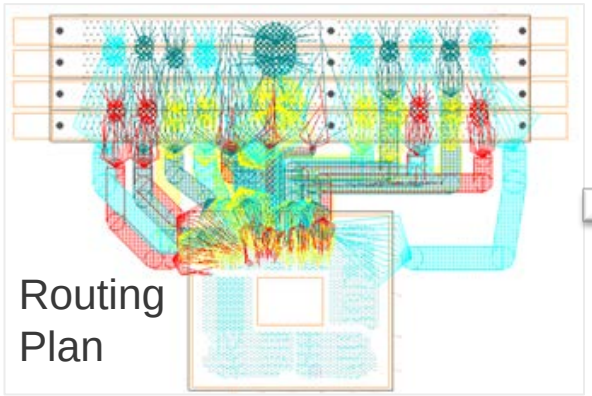

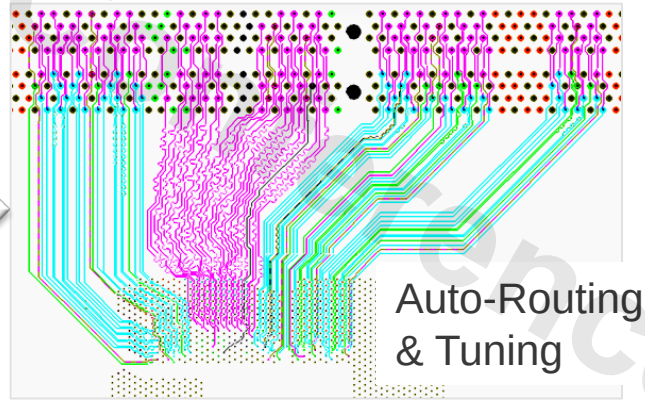

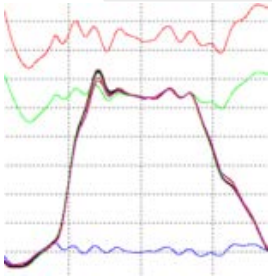

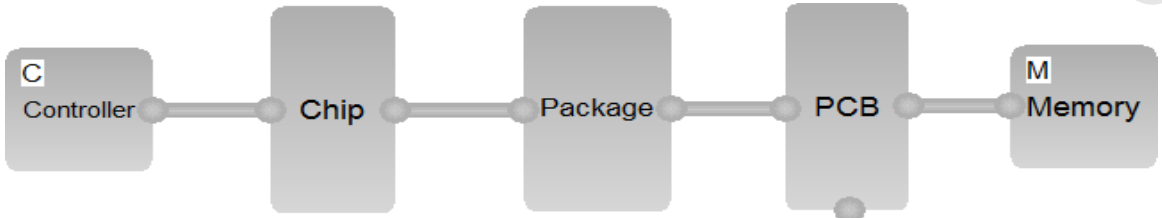

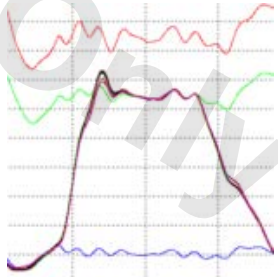

SSN/SSO Analysis in SystemSI

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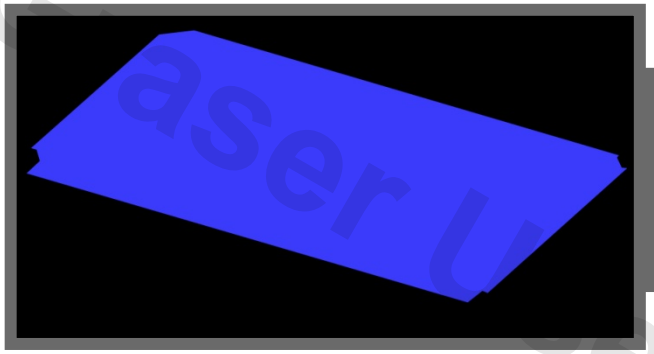
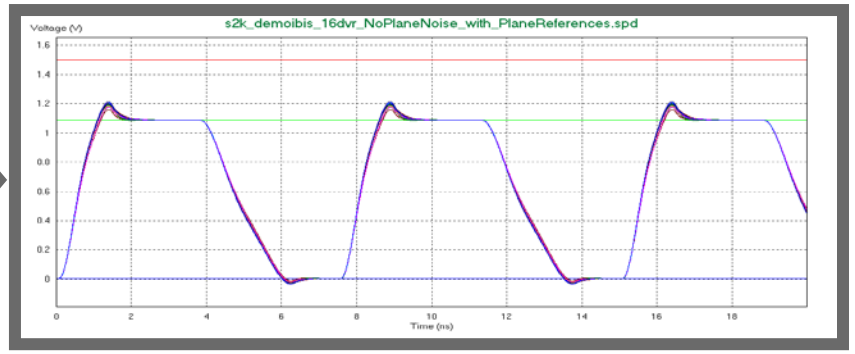
Signal Integrity with Power Aware

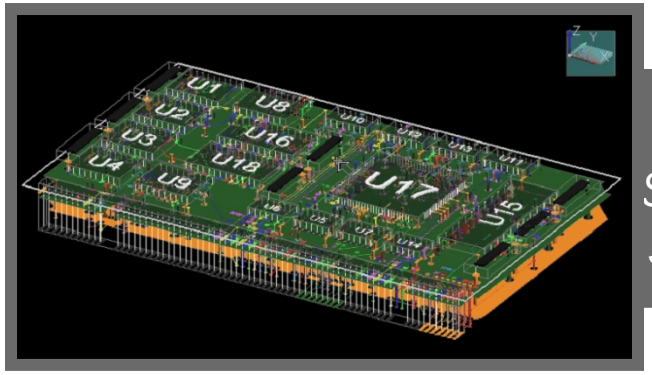


Signal data only

Predicts No SSN

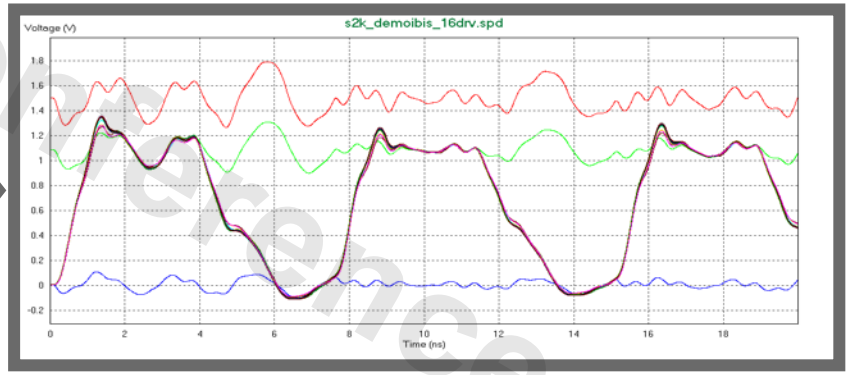


Simulation assuming ideal power delivery network



Signals, accurate planes, vias

Predicts Significant SSN Risk



Simulation with all power delivery effects

- Transmission line only analysis can't reveal the real signaling among ICs in current high speed parallel bus design.
- High-speed parallel bus with power-aware analysis can help to identify design defects and find out the root cause behind the problem.

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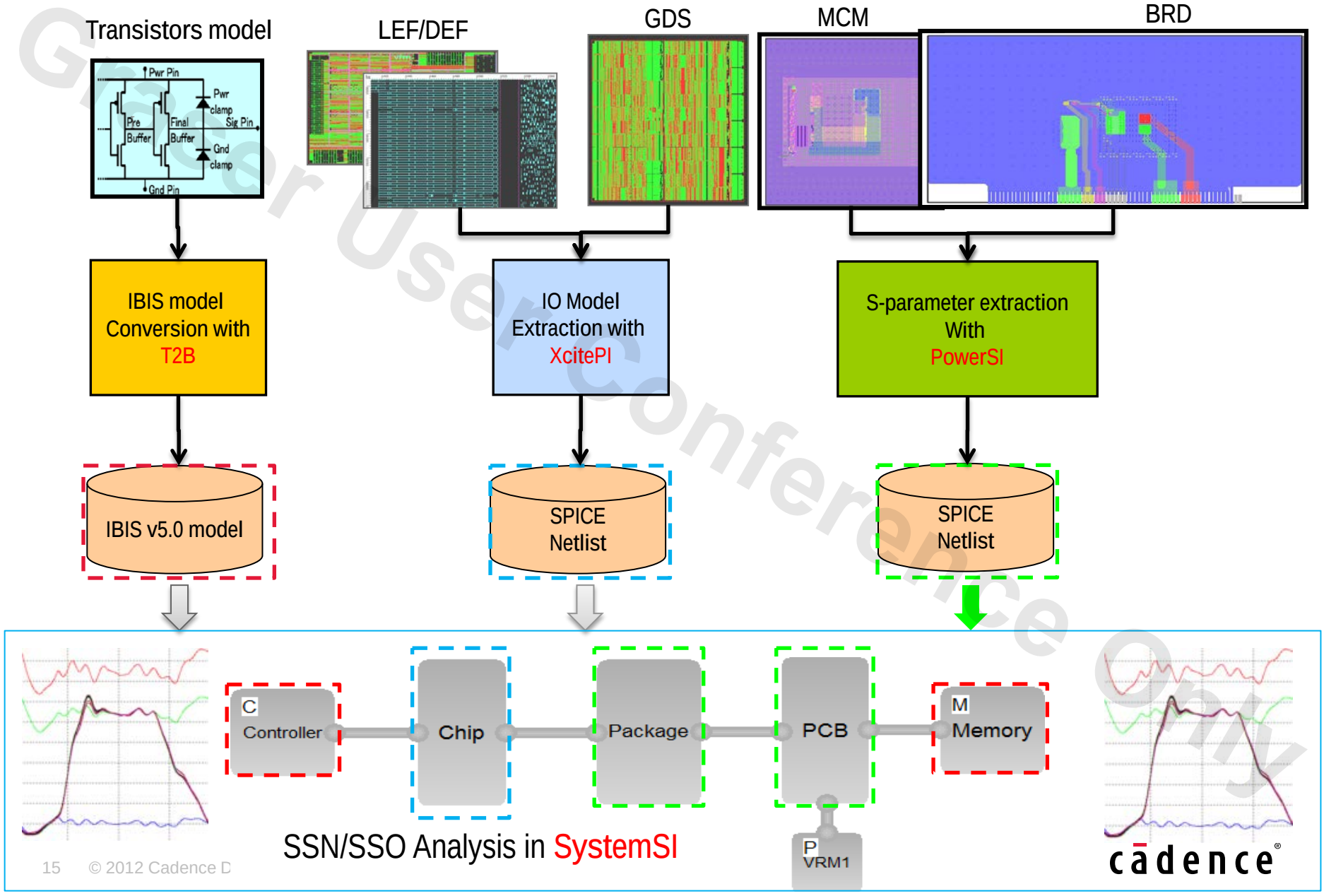
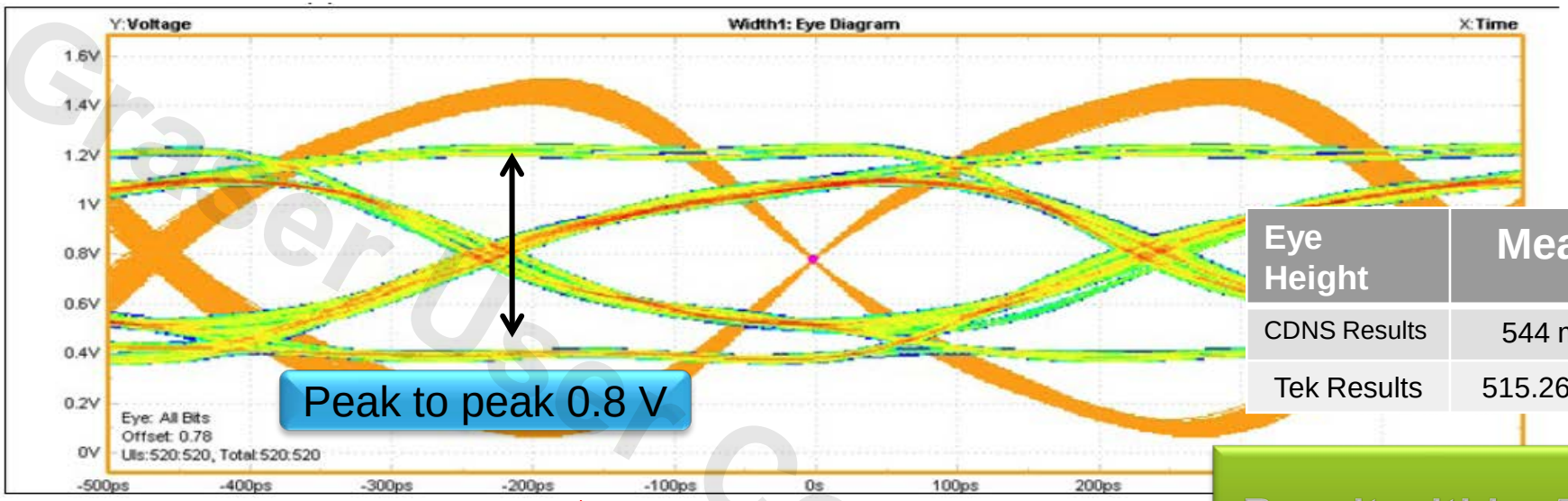
IO-SSN Simulation Flow



Validating the SSO simulation results

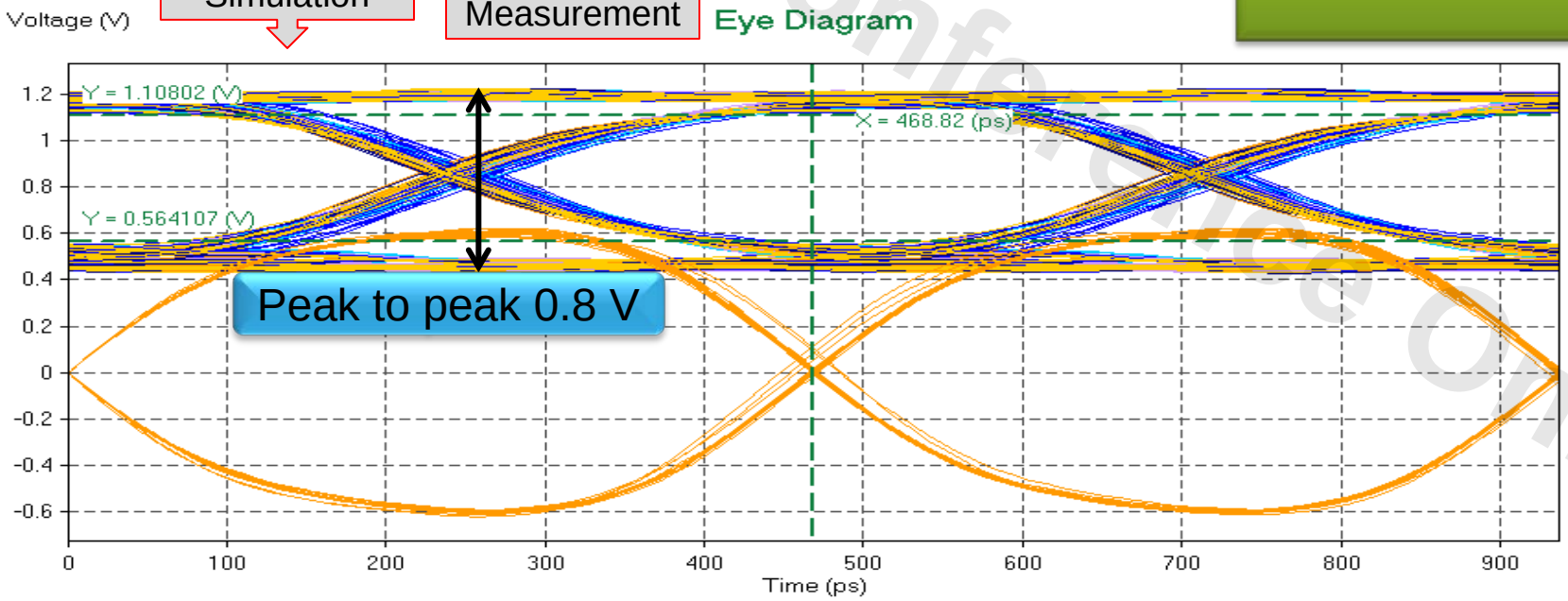


Eye Height	Mean
CDNS Results	544 mV
Tek Results	515.26 mV

Result within 5 %

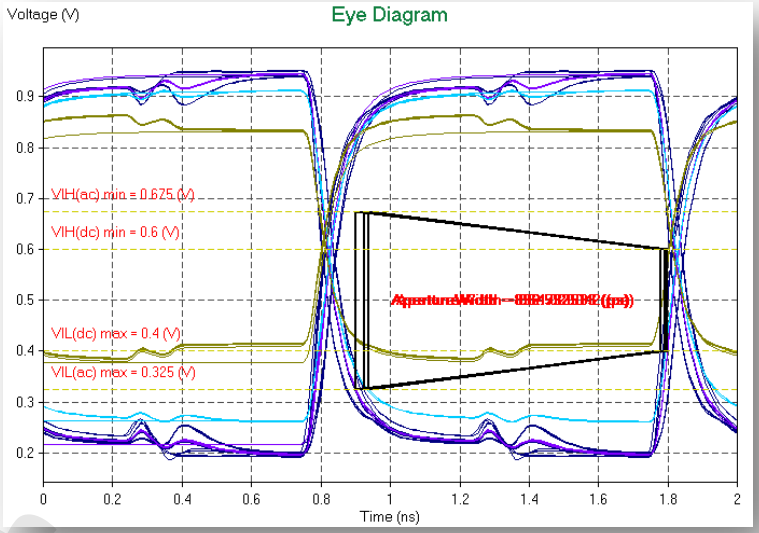
Simulation

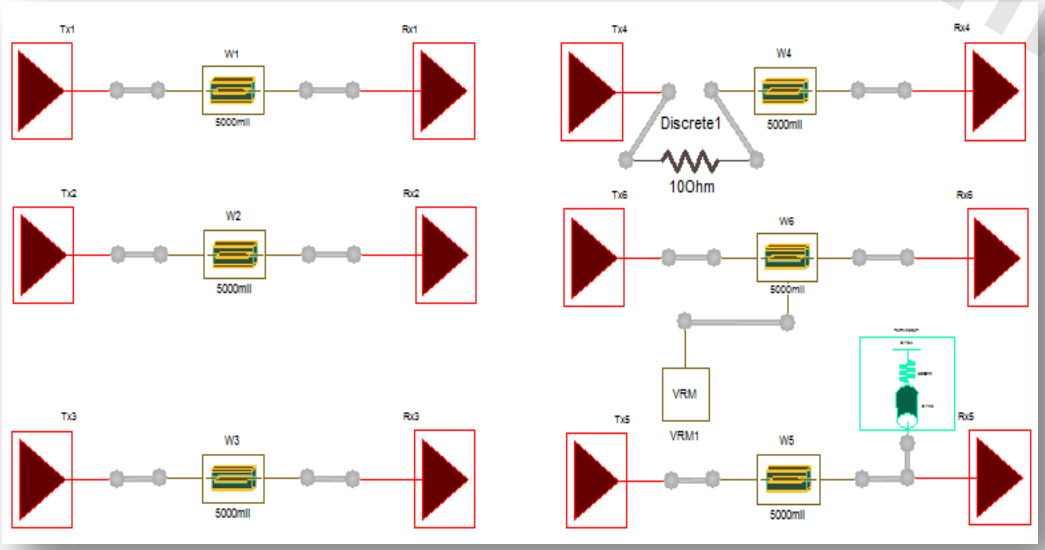
Measurement

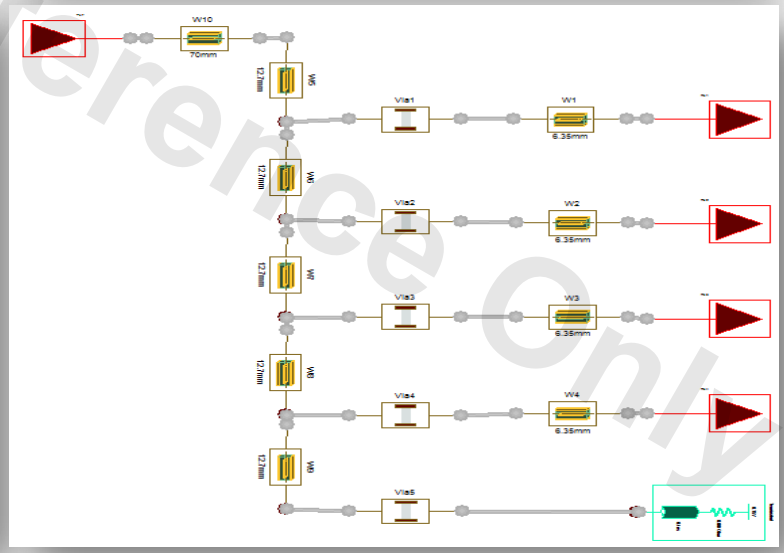


SystemSI Testbench - Quick Explore

- Multi-Topologies what-if analysis
- Varied built-in templates for Discrete, Terminator, Tline models.
- Supports AC, Trasient simulation

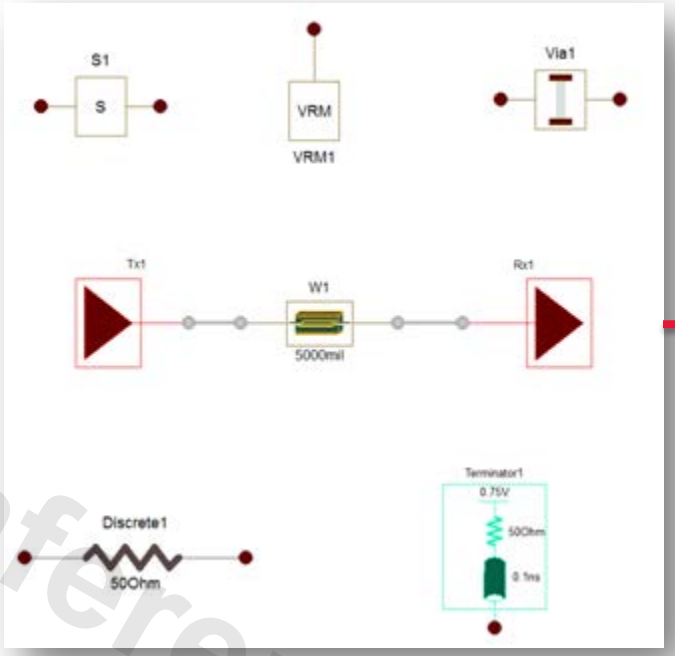


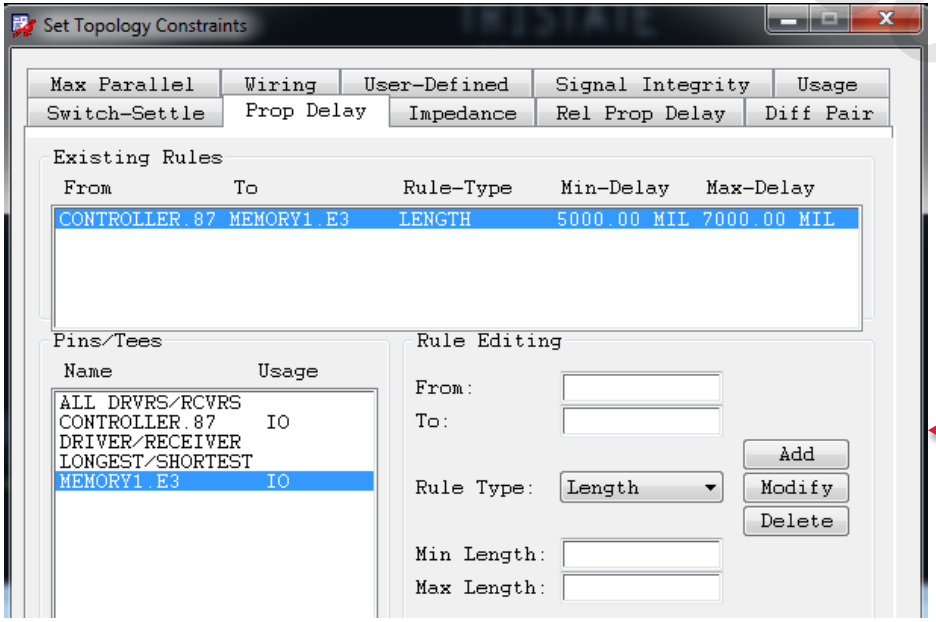


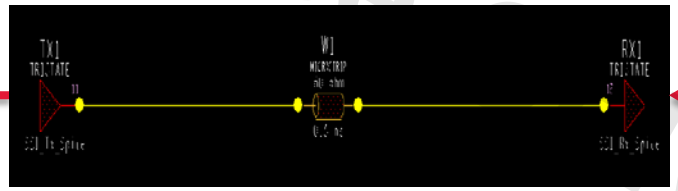


SystemSI Testbench – Constraint Driven Flow

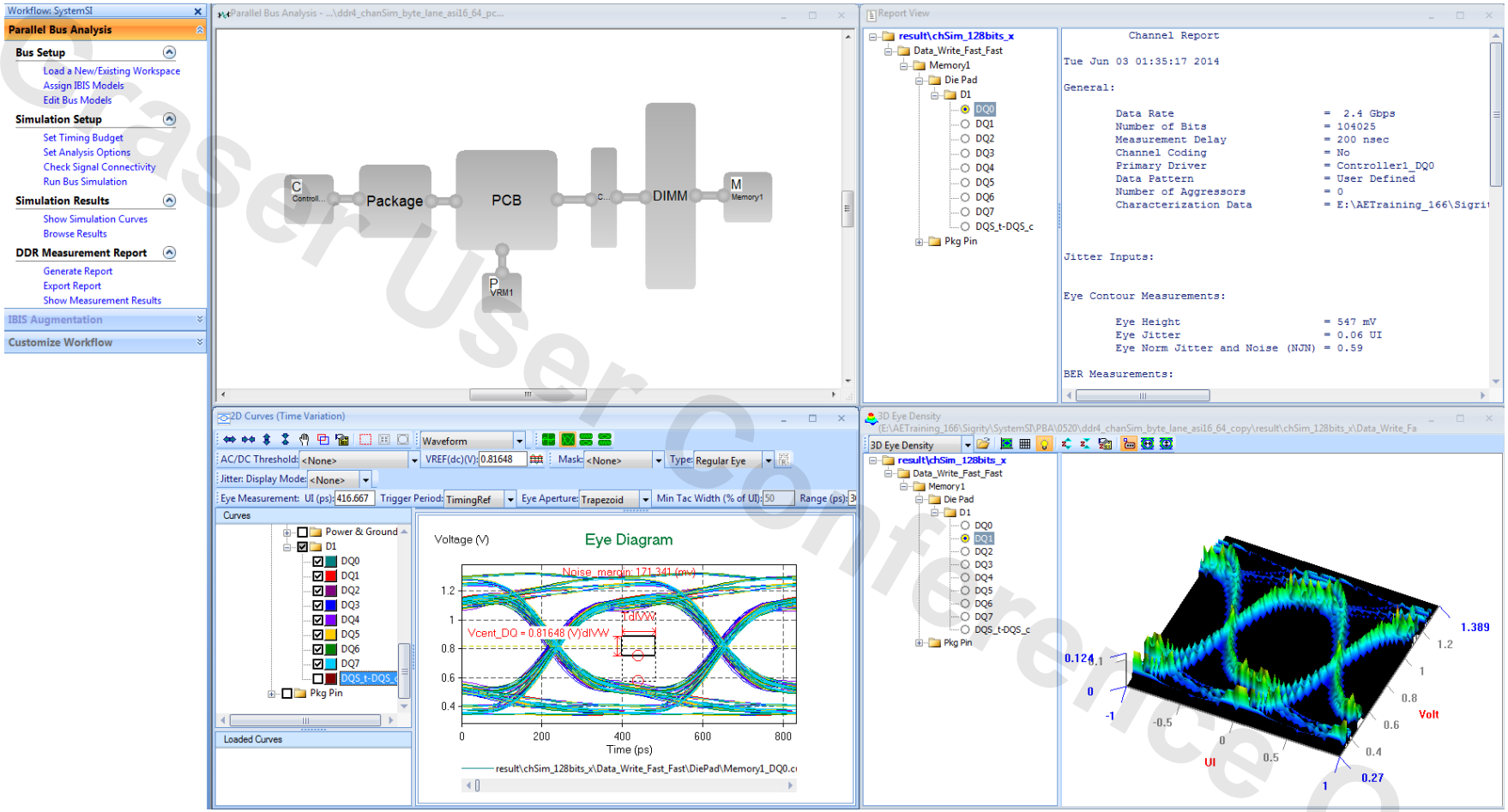
- Supports Constraint Driven flow by transform the topology to SigXP.
- Constraints can be embedded to drive physical layout.







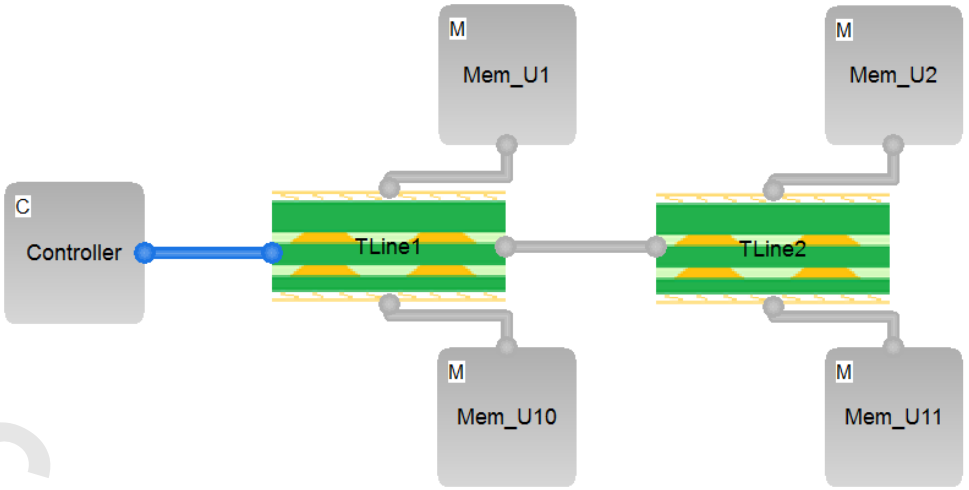
SystemSI - Parallel Bus Analysis

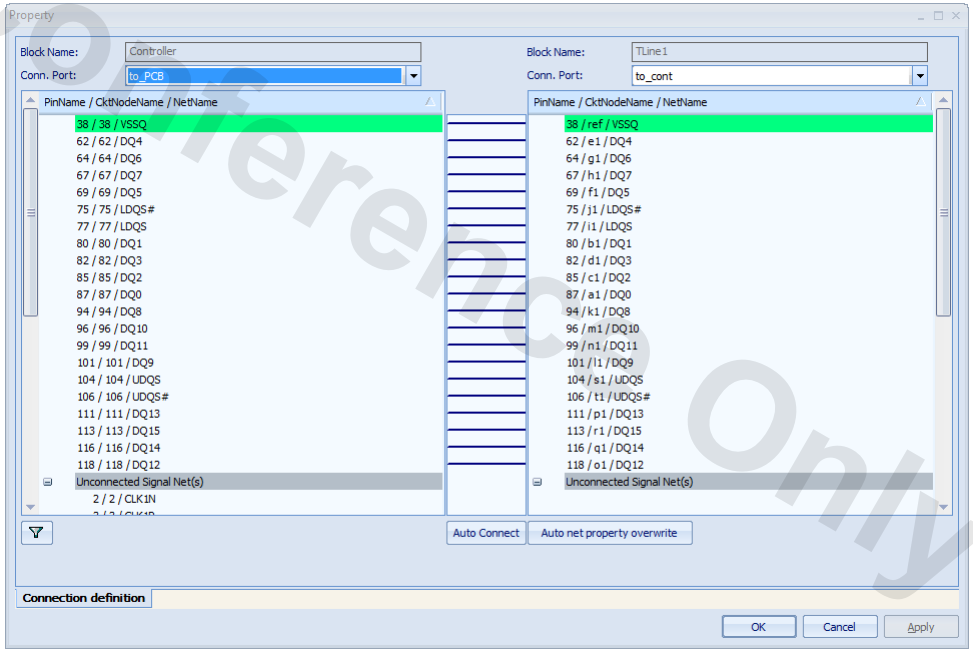


- Task orientation workflow
- Block based system level environment
- Sweep simulation to cover as many corners as you need.
- JEDEC based measurement Report

Model Connection Protocol Editor

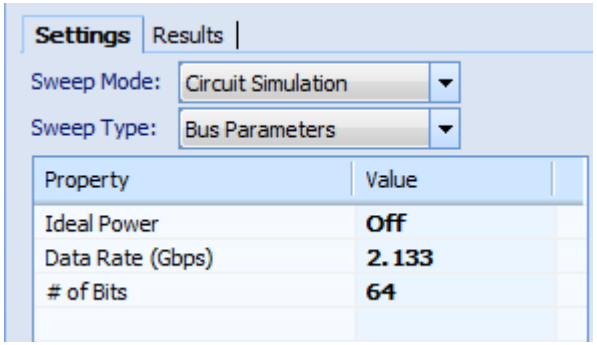
- MCP Header and Connection Editors enhance ease-of-use
- Given Pin-Node-Net mapping definitions
- Supports M to N nodes mapping.

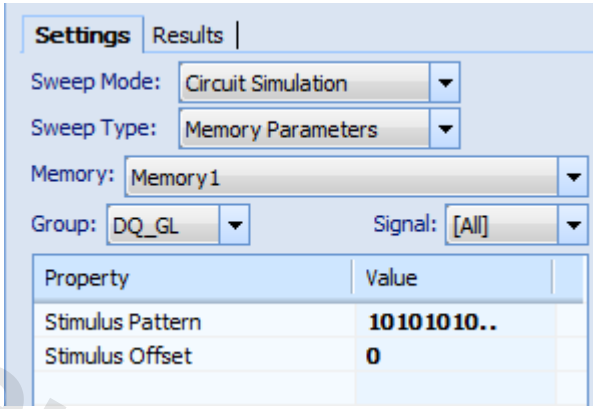


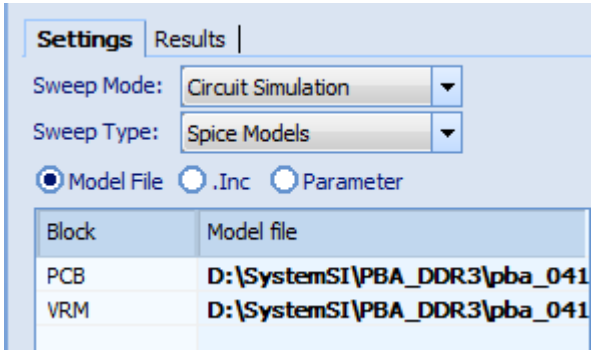


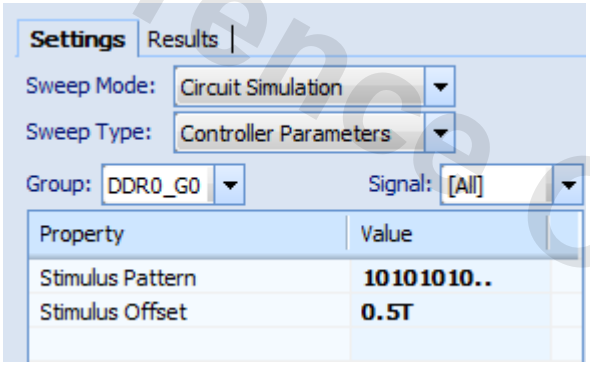
Sweep Capabilities

- Sweep mode
  - Circuit Simulation
  - Frequency Response
- Sweep type
  - Bus Parameters
  - Controller Parameters
  - Memory Parameters
  - Spice Models









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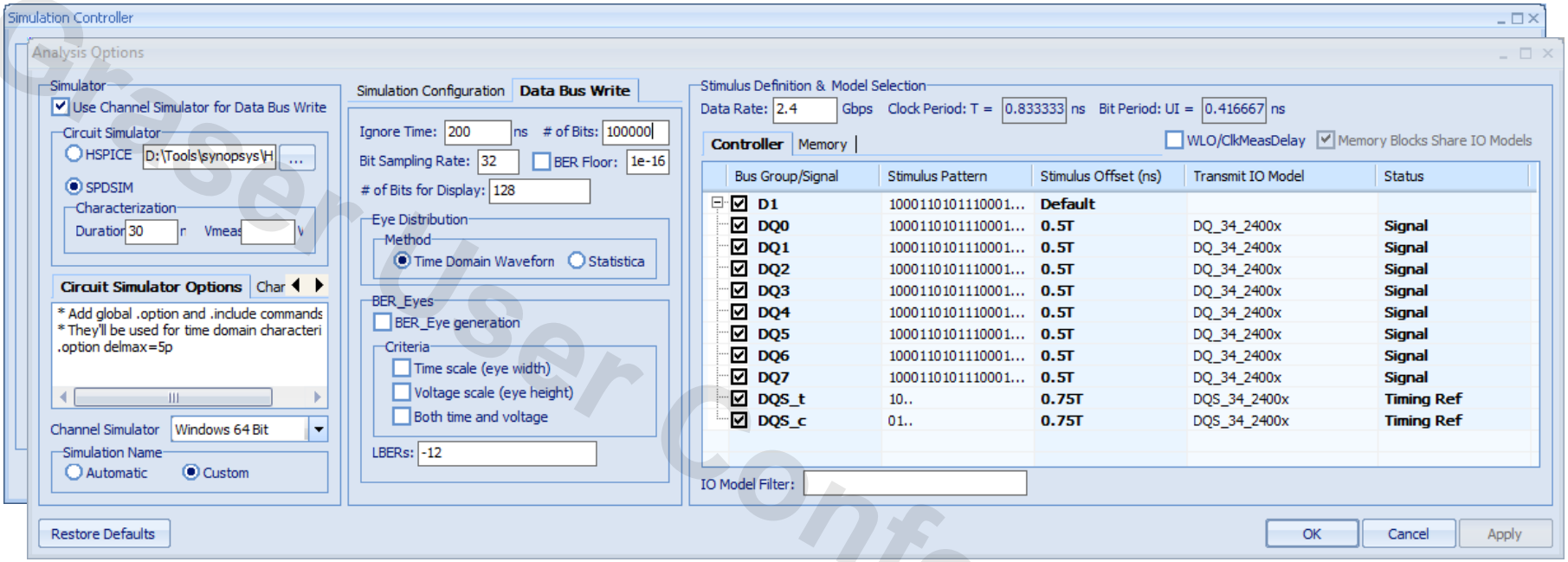
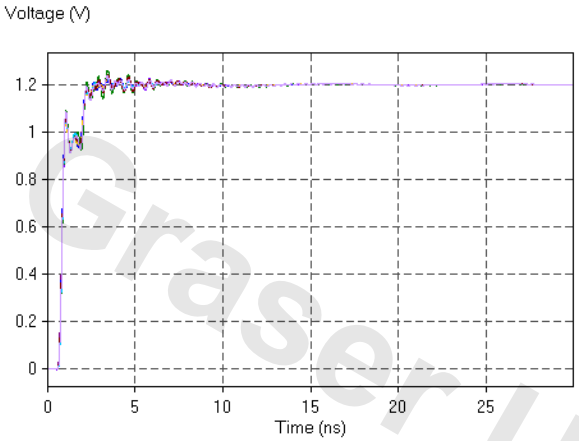
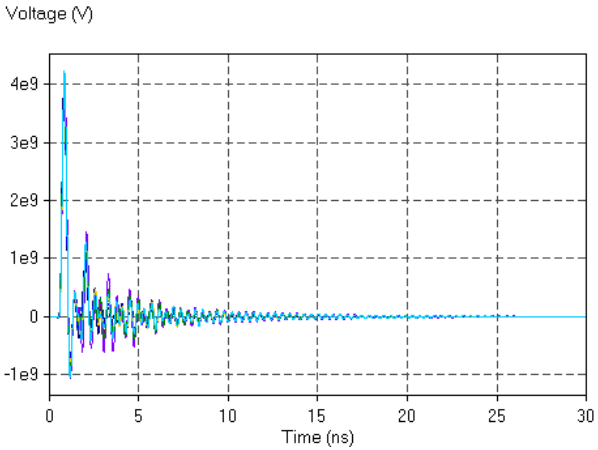
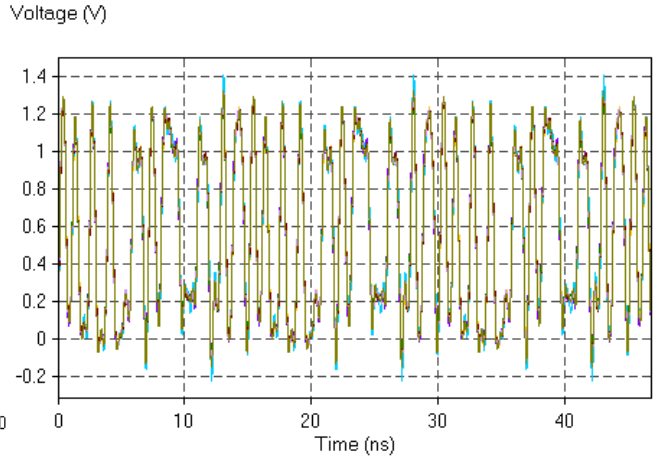
Analysis Options

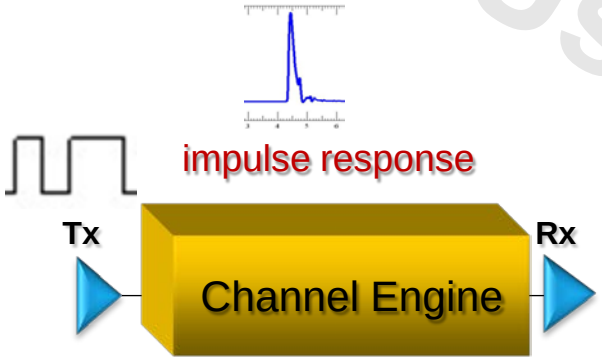


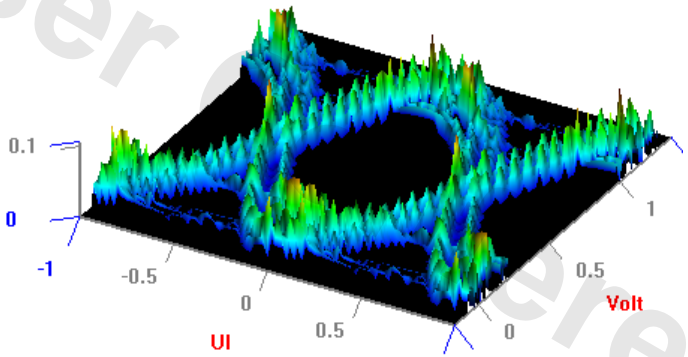
- Can simulate with SPDSIM or HSPICE
- Specify which Bus, Corner, and directionality (Read/Write)
- Specify which memory components to be active
- Define stimulus pattern to use for signals, random, or PRBS
- Specify Transmit, Receive, Standby IO models for bus
- Channel simulation engine is integrated



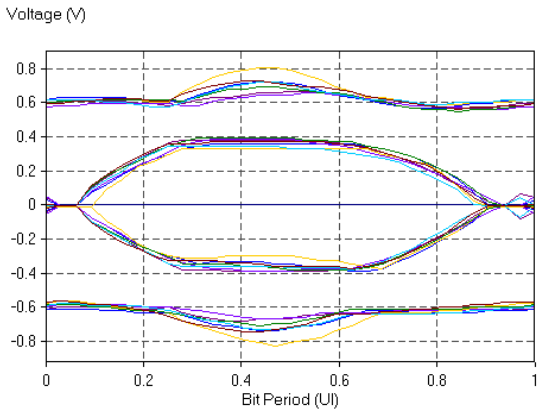


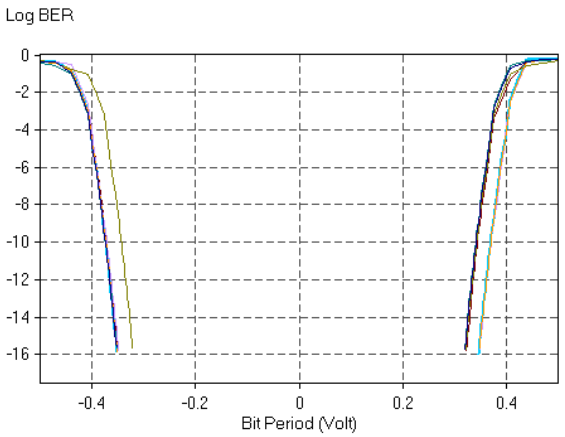


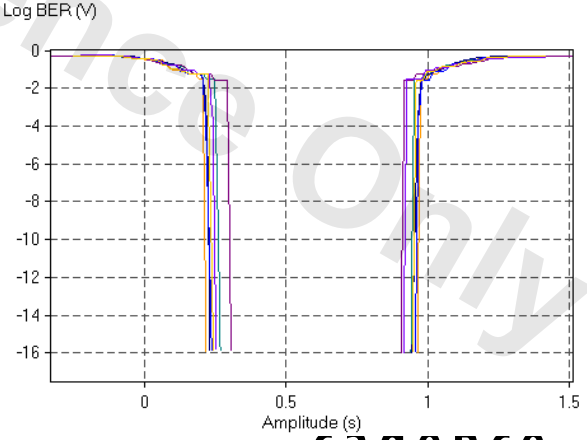




- Impulse Response
- Eye contour
- Bathtub curves
- Jitter/Noise aware







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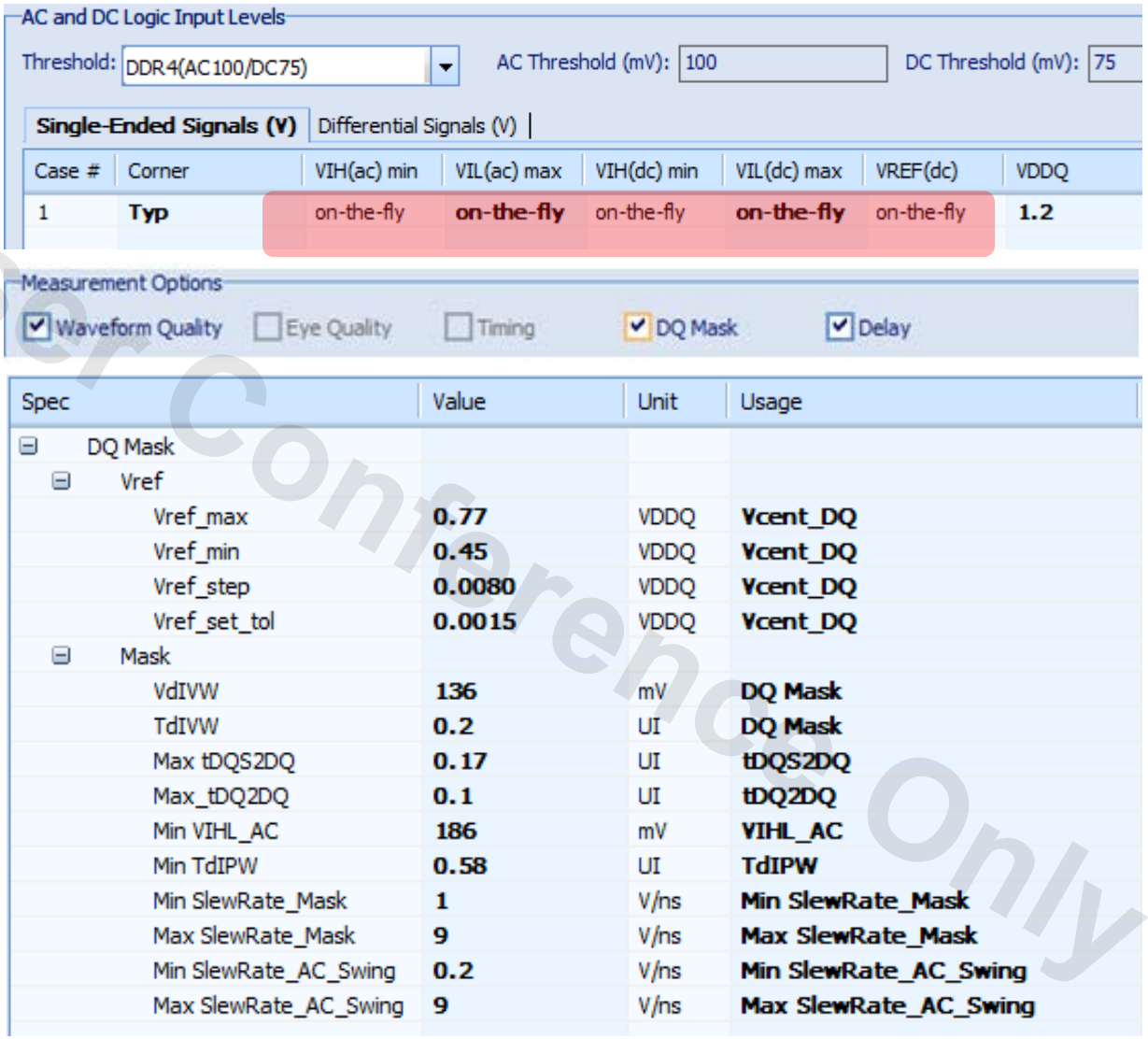
DDR4 Report Generator – JEDEC SPEC Aware

- DDR4 threshold
- Measure VREF on-the-fly
- DQ mask specification parameters



AC and DC Logic Input Levels

Threshold: DDR4(AC100/DC75) AC Threshold (mV): 100 DC Threshold (mV): 75

Single-Ended Signals (V) | Differential Signals (V)

Case #	Corner	VIH(ac) min	VIL(ac) max	VIH(dc) min	VIL(dc) max	VREF(dc)	VDDQ
1	Typ	on-the-fly	on-the-fly	on-the-fly	on-the-fly	on-the-fly	1.2

Measurement Options

☑ Waveform Quality ☐ Eye Quality ☐ Timing ☑ DQ Mask ☑ Delay

Spec	Value	Unit	Usage
DQ Mask			
Vref			
Vref_max	0.77	VDDQ	Vcent_DQ
Vref_min	0.45	VDDQ	Vcent_DQ
Vref_step	0.0080	VDDQ	Vcent_DQ
Vref_set_tol	0.0015	VDDQ	Vcent_DQ
Mask			
VdIVW	136	mV	DQ Mask
TdIVW	0.2	UI	DQ Mask
Max tDQS2DQ	0.17	UI	tDQS2DQ
Max_tDQ2DQ	0.1	UI	tDQ2DQ
Min VIHL_AC	186	mV	VIHL_AC
Min TdIPW	0.58	UI	TdIPW
Min SlewRate_Mask	1	V/ns	Min SlewRate_Mask
Max SlewRate_Mask	9	V/ns	Max SlewRate_Mask
Min SlewRate_AC_Swing	0.2	V/ns	Min SlewRate_AC_Swing
Max SlewRate_AC_Swing	9	V/ns	Max SlewRate_AC_Swing

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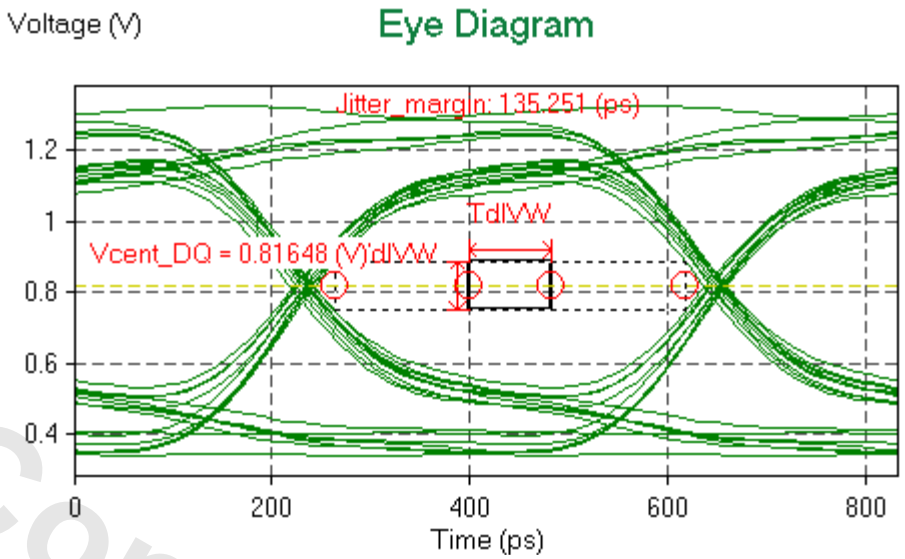
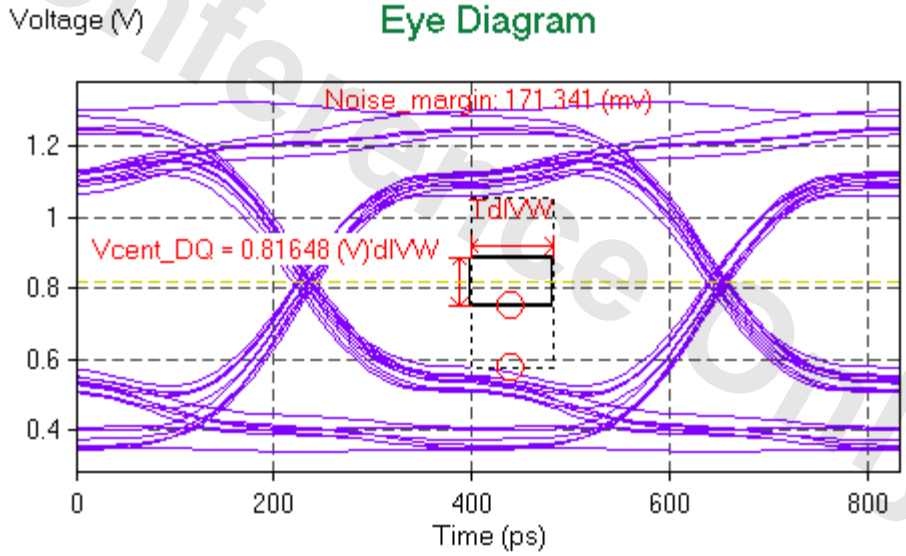
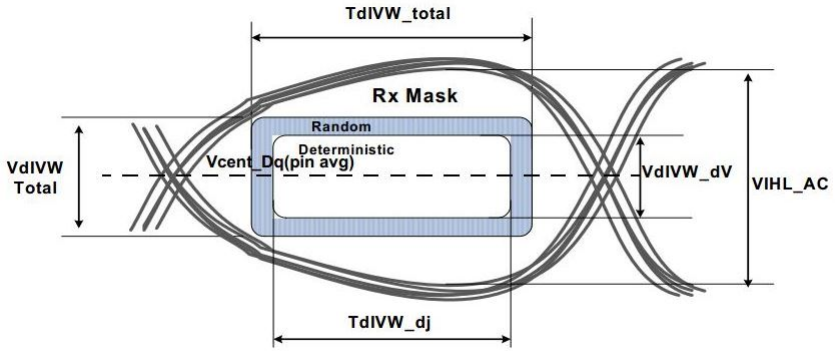
DQ Rx Mask Support in SystemSI for DDR4

- Derive Vcent_DQ level on-the-fly from raw waveforms for each DQ signal
- Automatically position and evaluate DQ mask vs. eye

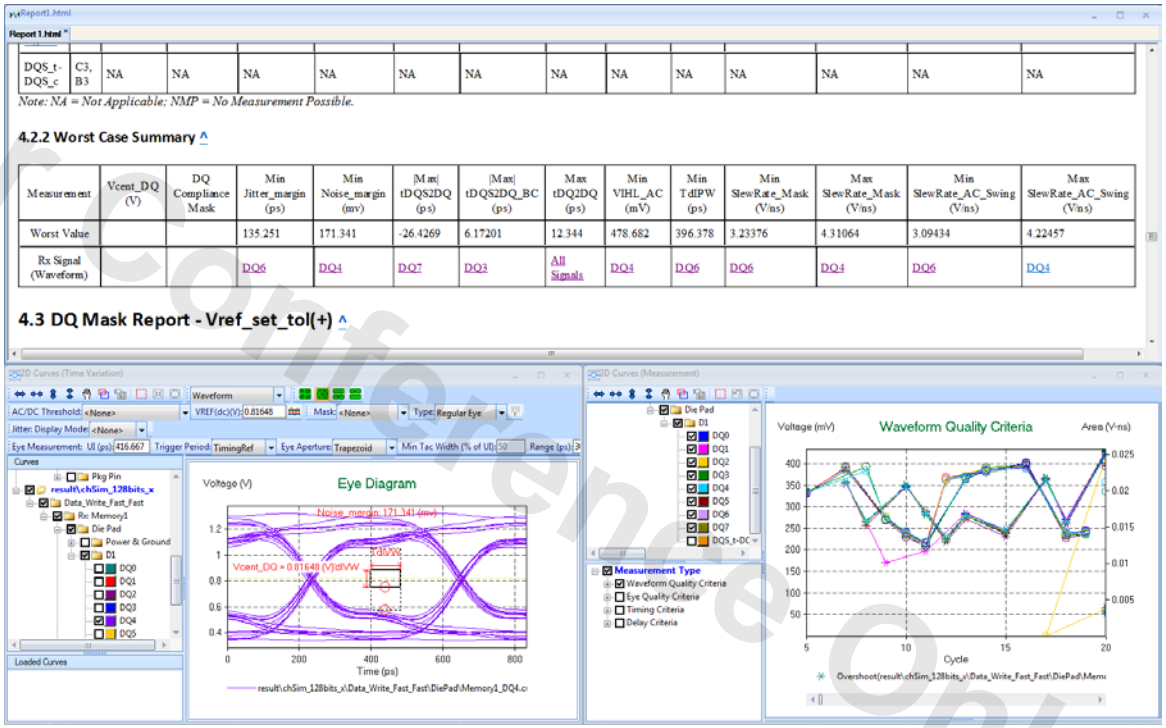






JEDEC Type Measurement Report

- Raw waveforms are automatically post-processed to take measurements
- Tabulated reports for:
  - Overshoot
  - Eye quality
  - Setup & hold
  - DQ Mask (DDR4)
  - Delays & skews



- Criteria plots, waveforms, eye diagrams all linked to reports

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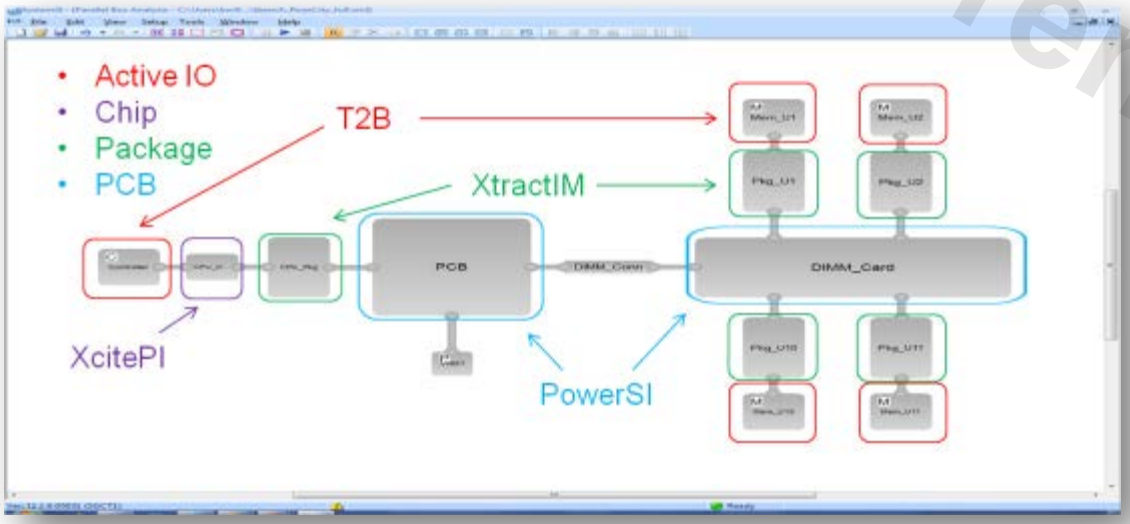
Summary

Power Aware Memory Interface Design and Analysis

Key features of Allegro Sigrity Power-Aware SI Option

- Allegro Sigrity Power-Aware SI addresses the challenges associated with **source synchronous bus design**
- Industry-leading **interconnect extraction and power-aware IBIS modeling** technology includes the non-ideal power and ground effects
- **Concurrent simulation** of signal, power, and ground accurately determine Setup and Hold margins
- Comprehensive, automated **JEDEC-based measurements and post-processing**
- **Easy-to-use environment** featuring popular memory interface compliance kits is highly integrated with layout allowing engineers to efficiently close on memory interface timing



Note: Package and Chip extraction technology sold separately from Allegro Sigrity Power-Aware SI Option

Summary

- DDR4 brings new challenges to signal and power integrity domains
  - Data rate jumps 50%
  - Power supply drops 20%
- Allegro Sigrity integration simplify analysis flow.
- Design check before TD simulation
- Power aware SSO analysis result close to real situation.
- New analysis techniques are required to evaluate Rx Mask for Data per JEDEC specifications.
- SERDES analysis technique is employed for BER calculation.
- JEDEC type compliance sign-off report for DDR4.

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