USER CONFERENCE Graser 2014 Oct 31 Taipei

An Alternative Approaching for Design Verification

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Graser®

Agenda

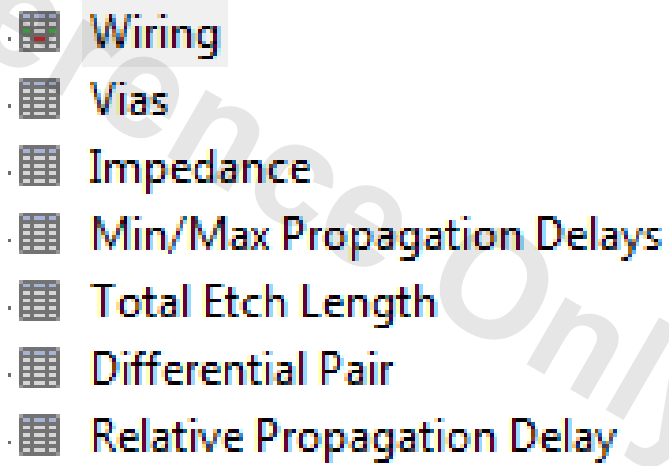
- What is DRC?
- What does DRC forget to tell you?
- What are Questions in Mind?
- Allegro SI Base with SPEED2000
- Allegro PI Base with OptimizePI

What is DRC?

What is DRC?

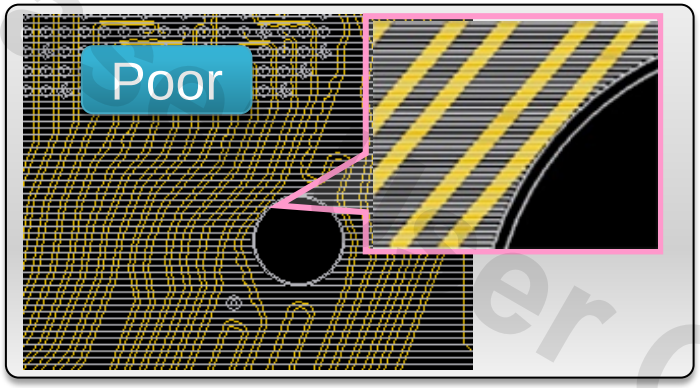
There are four types of net-based rules and one board base:

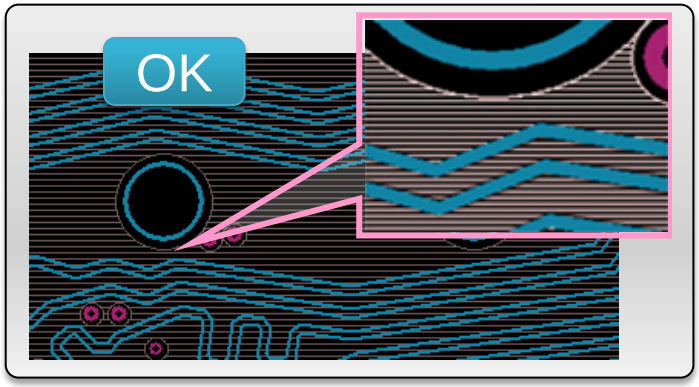
- Spacing Constraint Set: Clearances between lines, pads, vias, and copper areas (shapes) on different nets.
- Physical Constraint Set: Line width and layer restrictions
- Same Net Spacing Constraint Set: Clearances between lines, pads, vias, and copper areas (shapes) on the same net.
- Electrical Constraint Set: Performance characteristics (crosstalk and propagation delay).
- Design Manufacturing Checking: Soldermask, Package, Pastmask

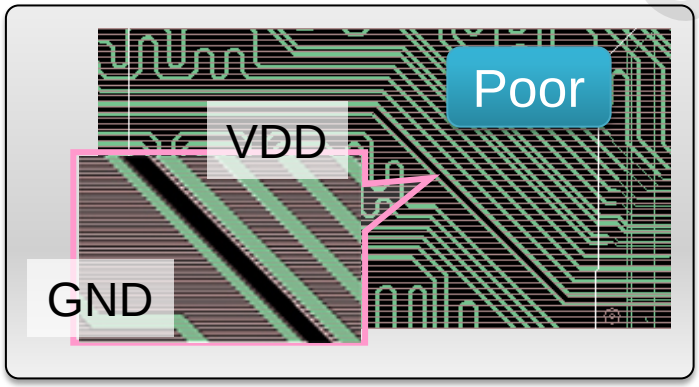


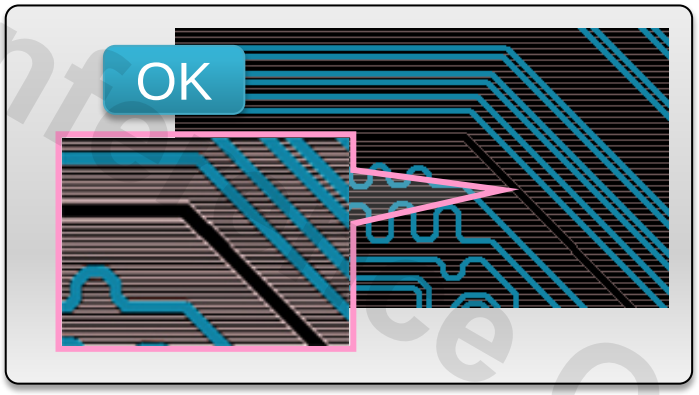
Spacing Constraint Set

Reference Plane Spacing Clearance



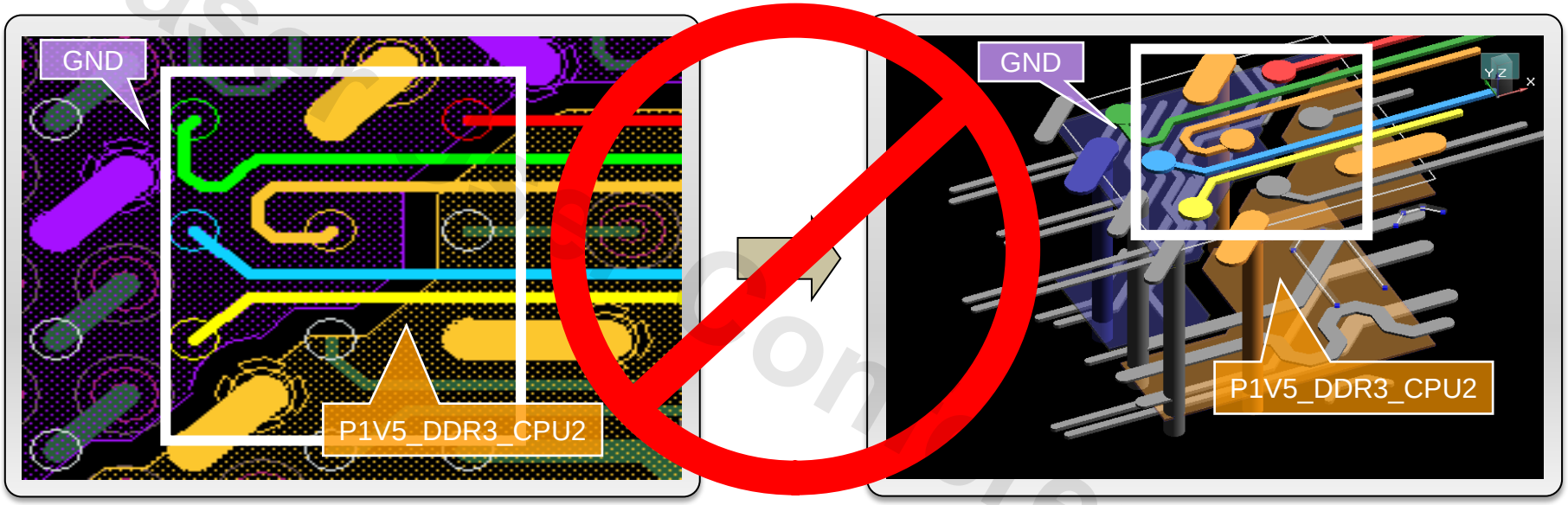






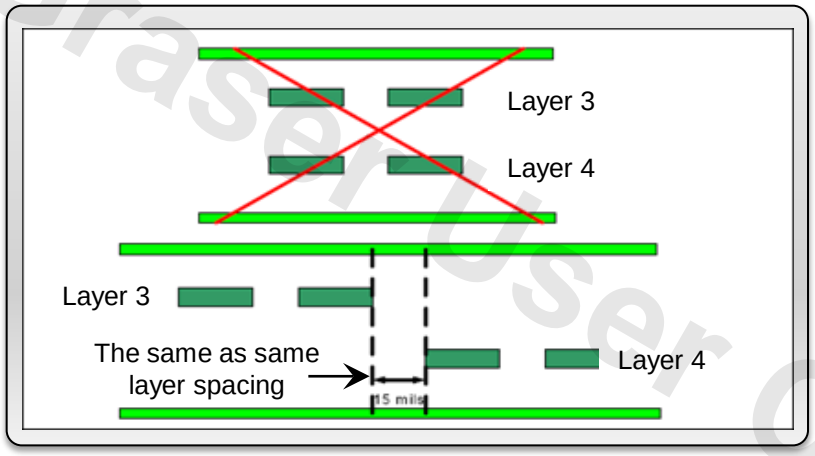
- EMI
- Impedance mismatch

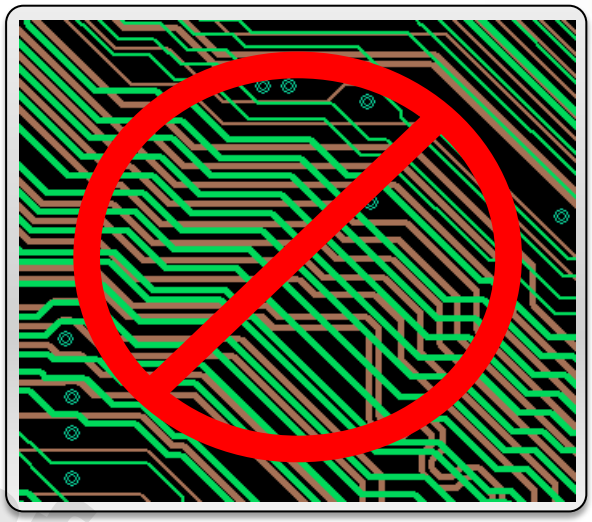
Plane Crossing



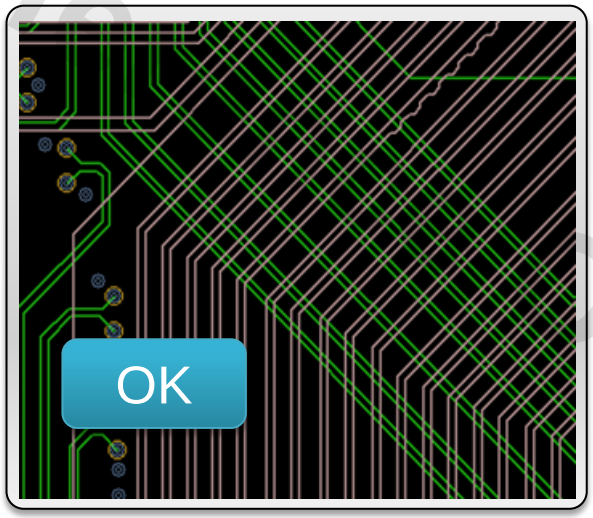
- EMI
- Return current path
- Impedance mismatch
- Signal degradation

Parallelism on Adjacent Layers

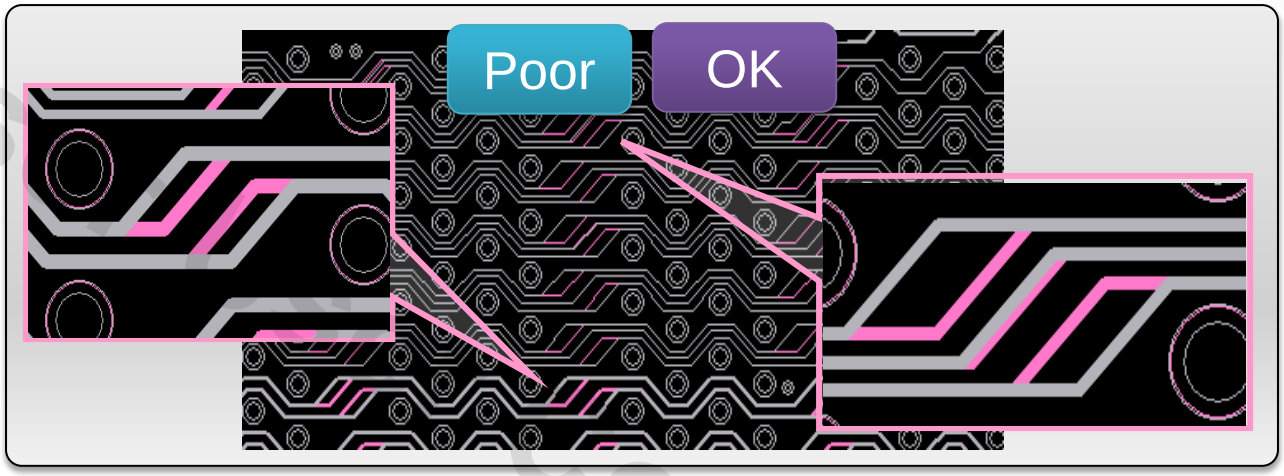


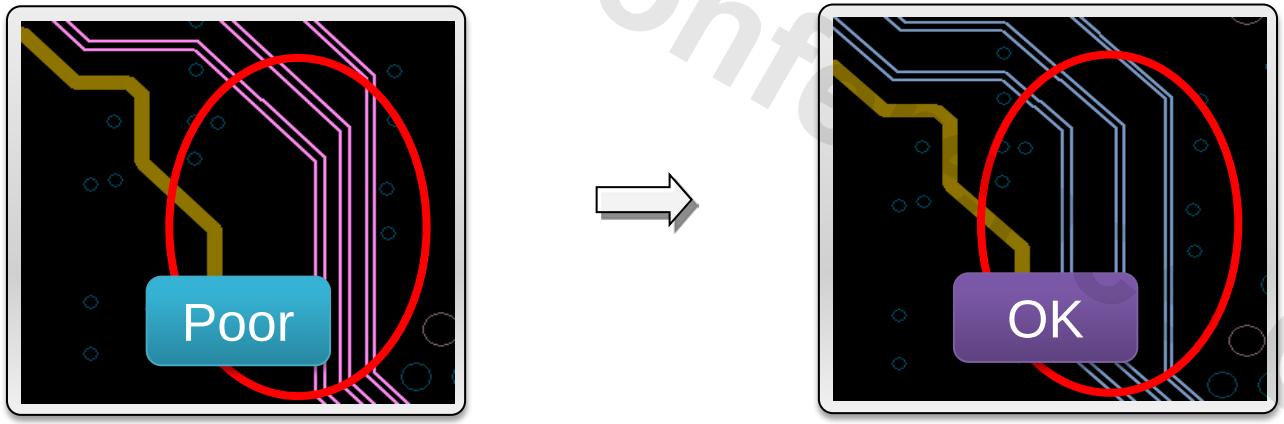


- Crosstalk



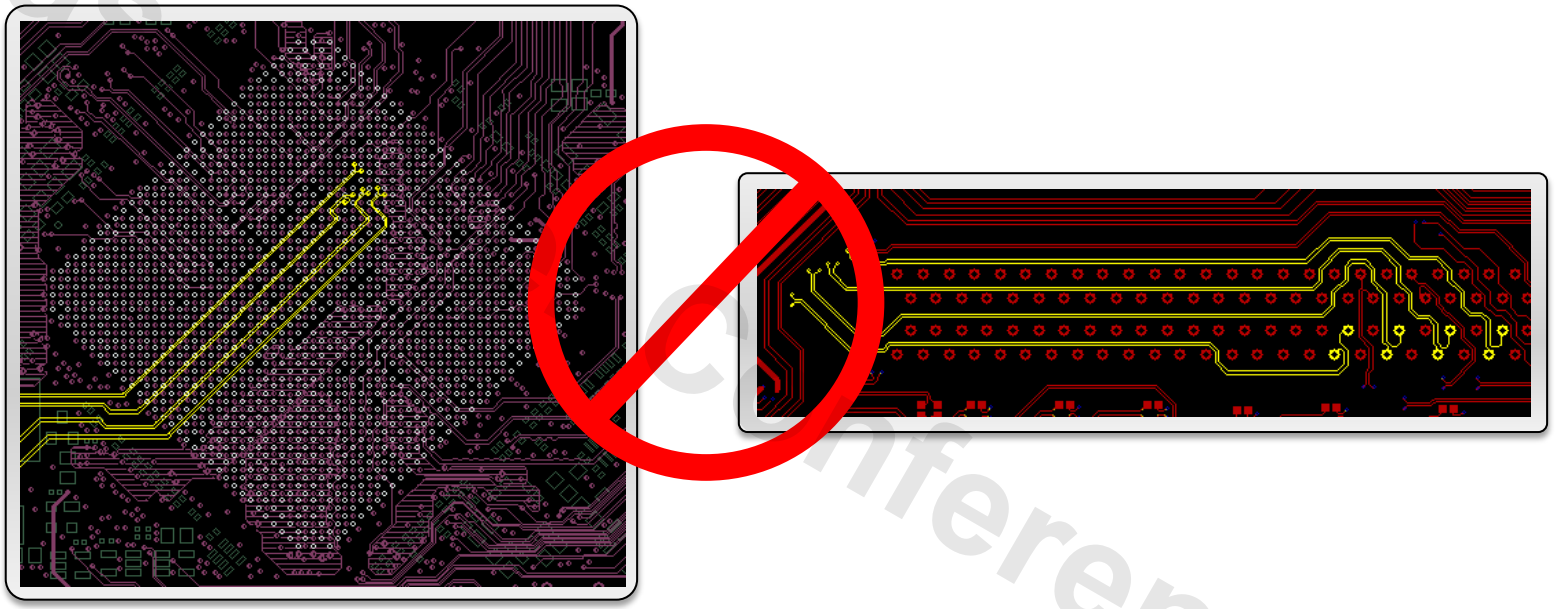
Trace Spacing Distribution





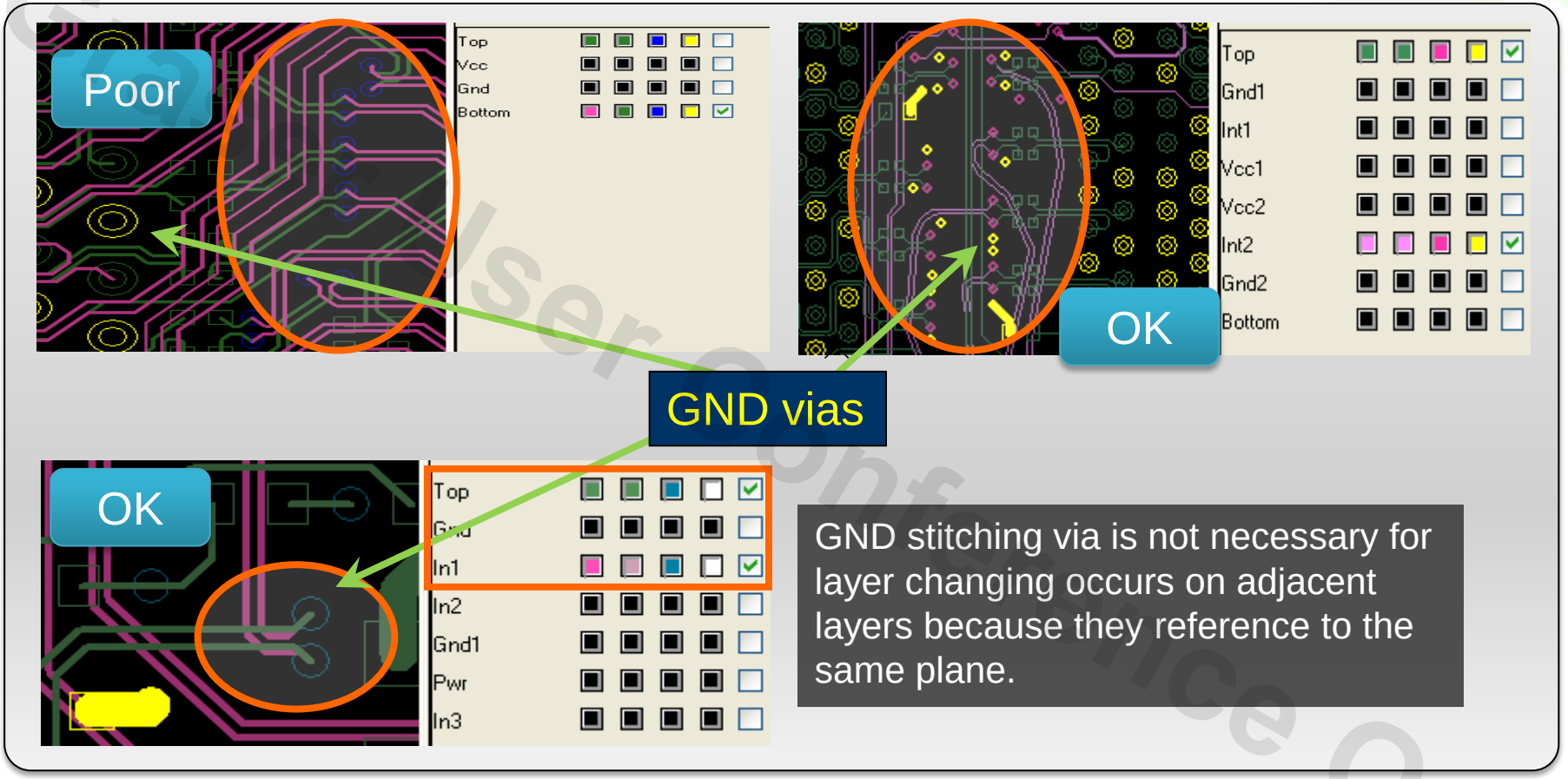
- Crosstalk

Routing in Connector/Breakout Area



- Impedance mismatch
- Crosstalk

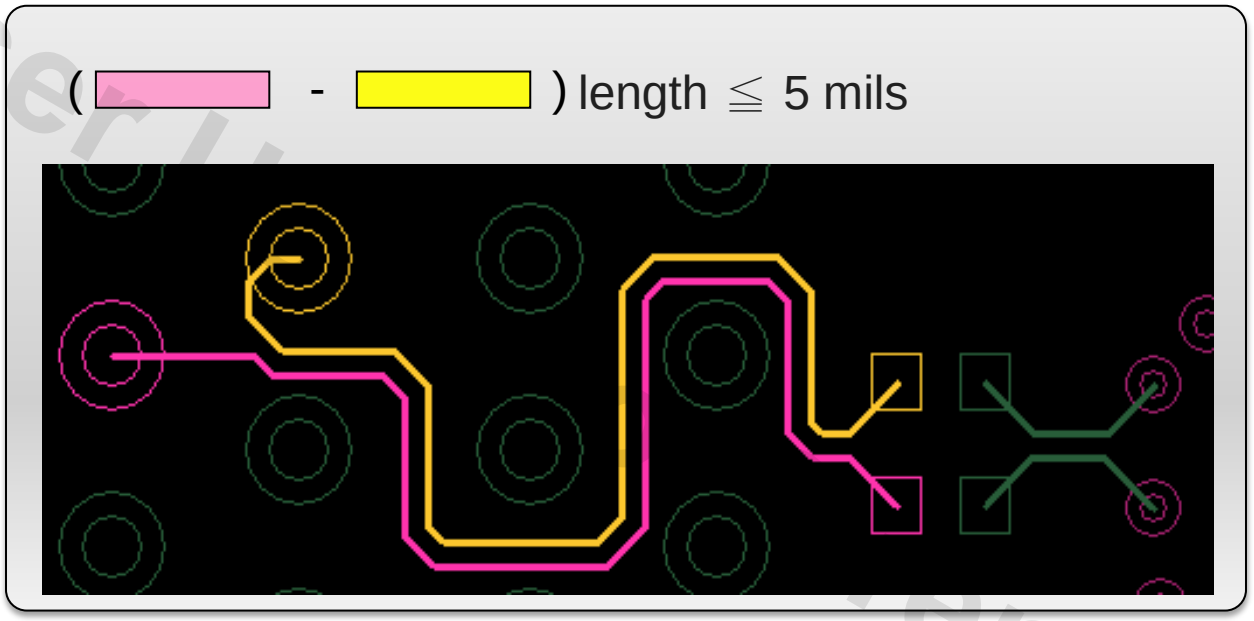
GND Stitching Vias



Return current path

- EMI
- Signal degradation

Cline Length Matching (diff. pair)

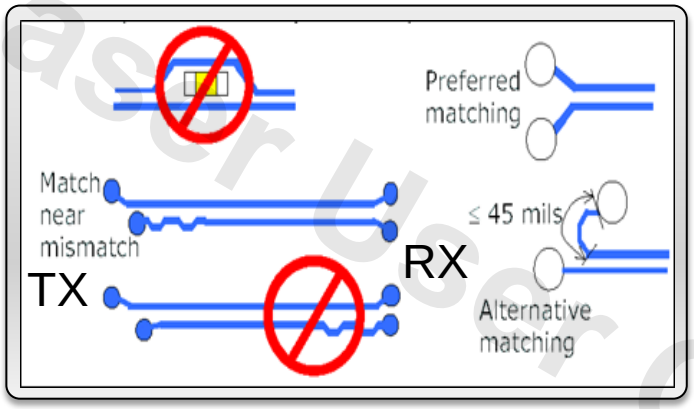


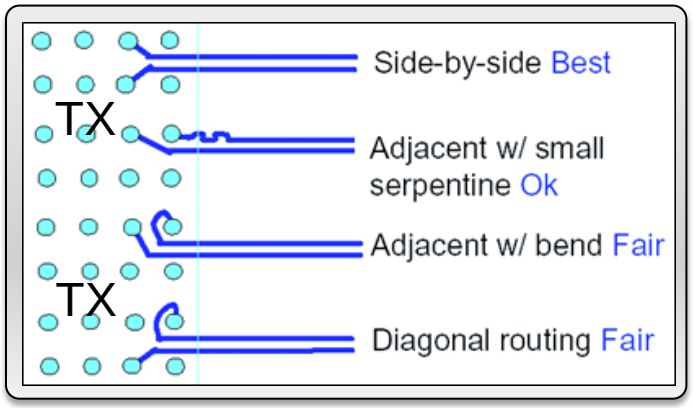
Common mode noise

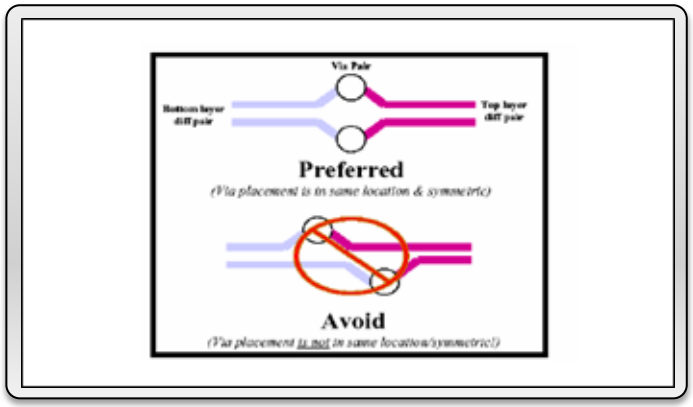
- EMI

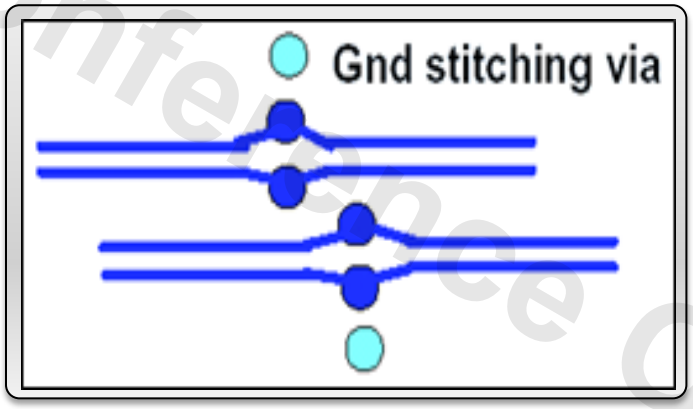
General Rules for Differential Pair

1/2







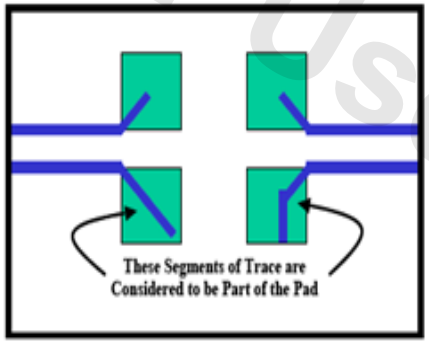


- Common mode noise
- Return current path

General Rules for Differential Pair

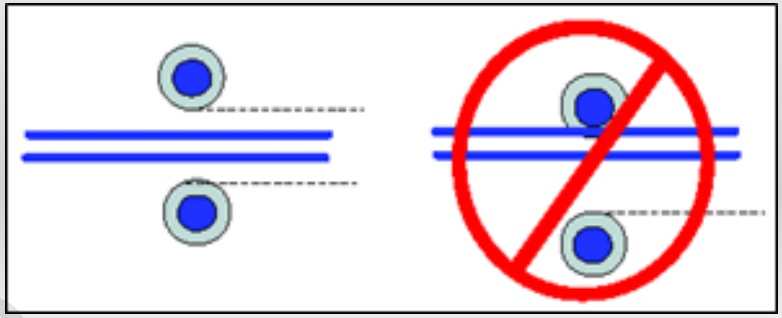
2/2

These segments of trace are considered to be part of the pad. Should be avoided.

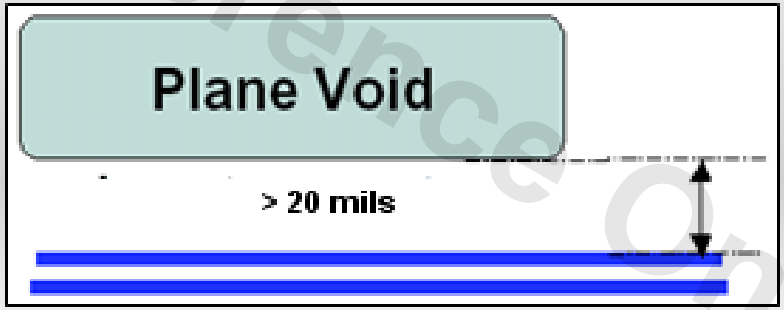


- Skew
- Impedance mismatch
- EMI

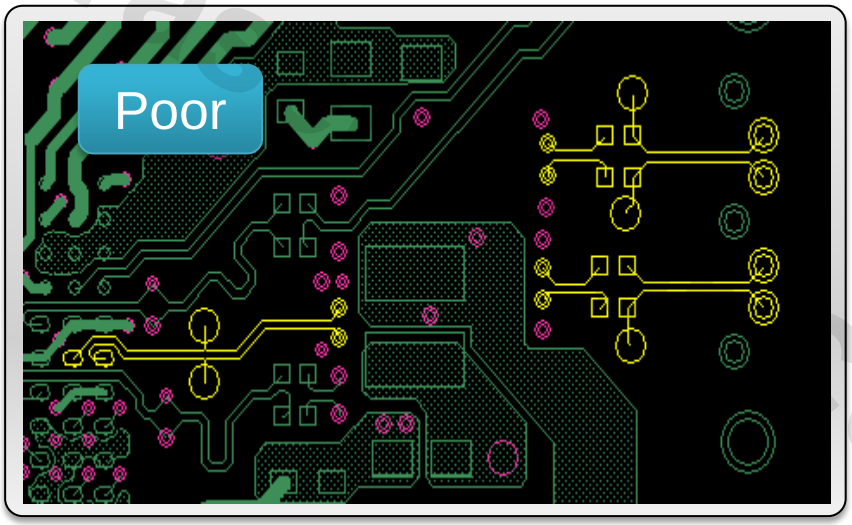
Avoid trace over anti-pad.

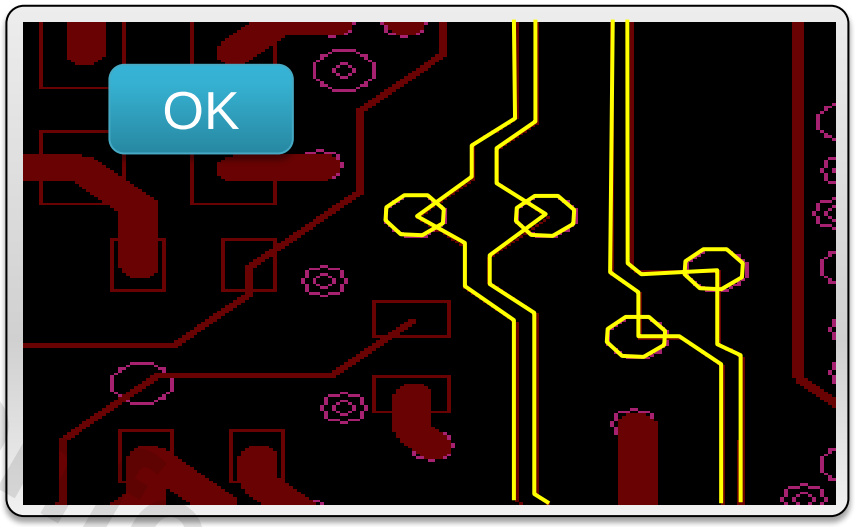


Clearance near plane void.



Test Point



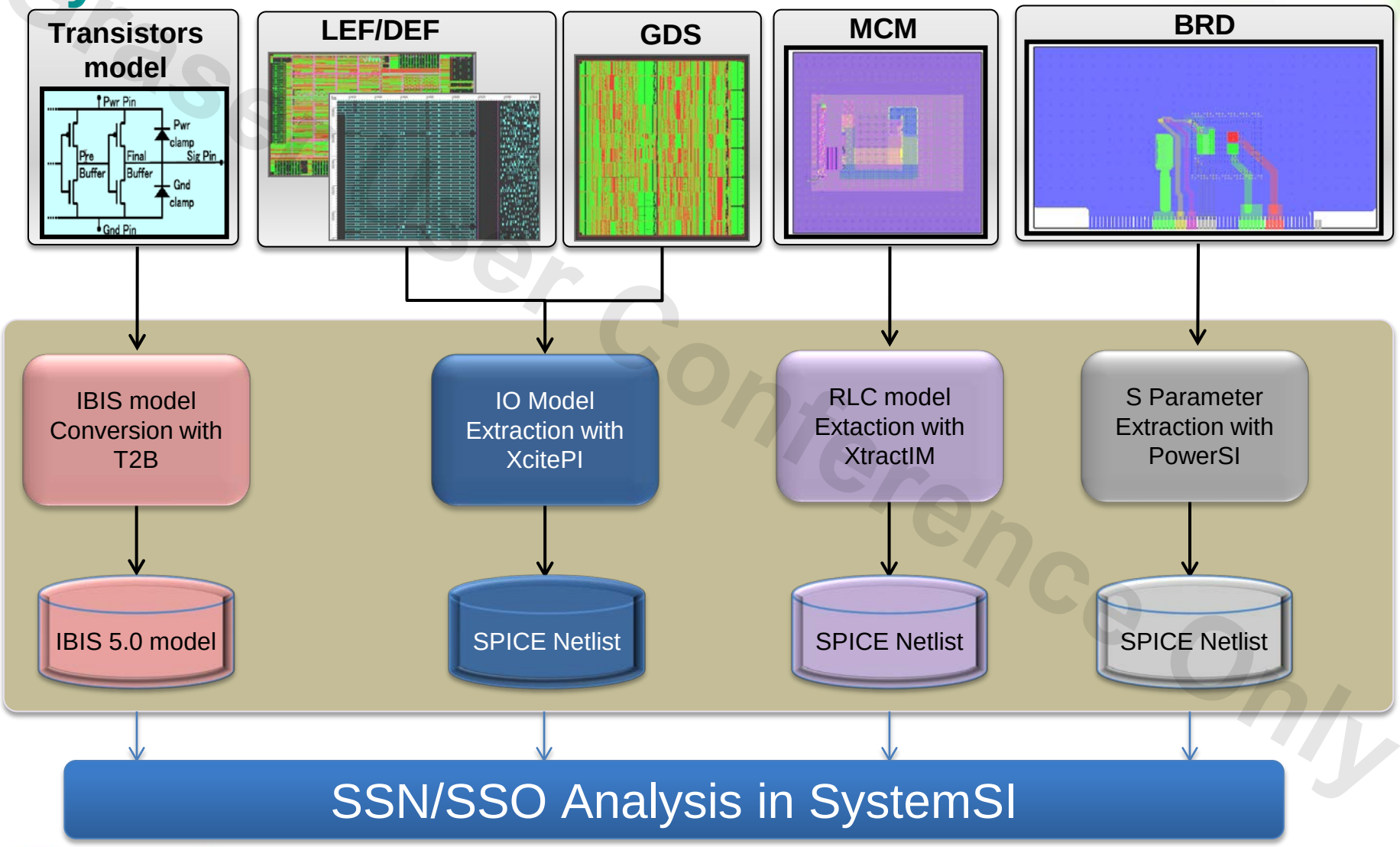


- Impedance mismatch
- Signal reflection

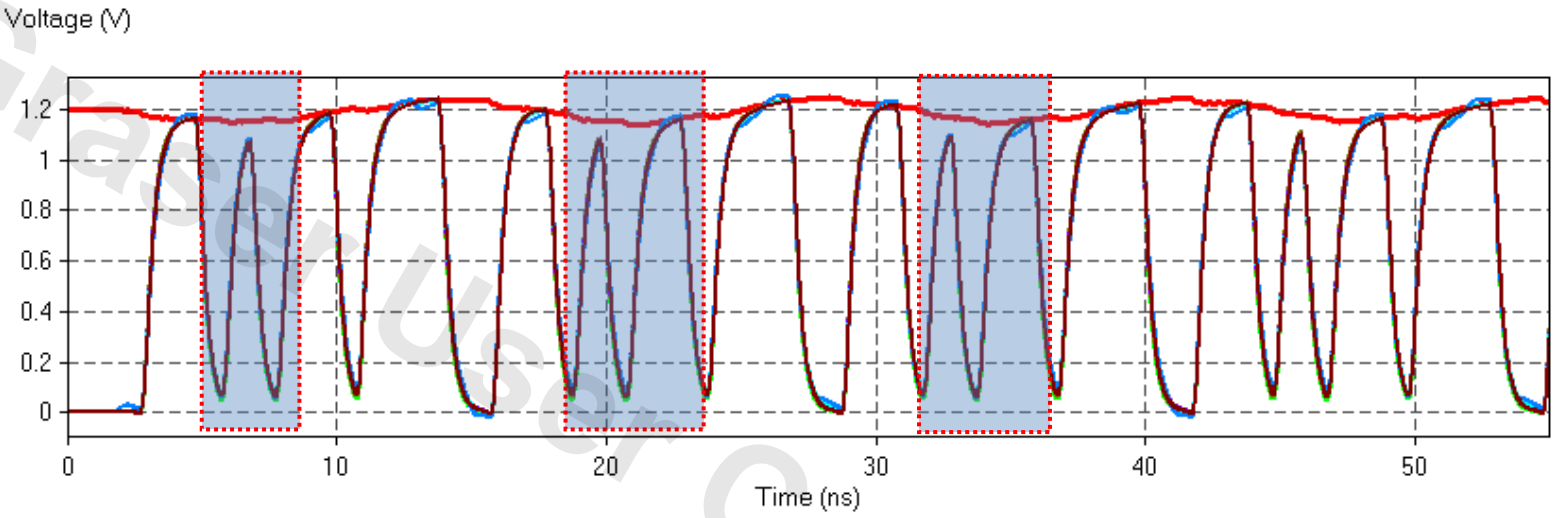
Even if DRC can't identify the problems , issues still occur!!

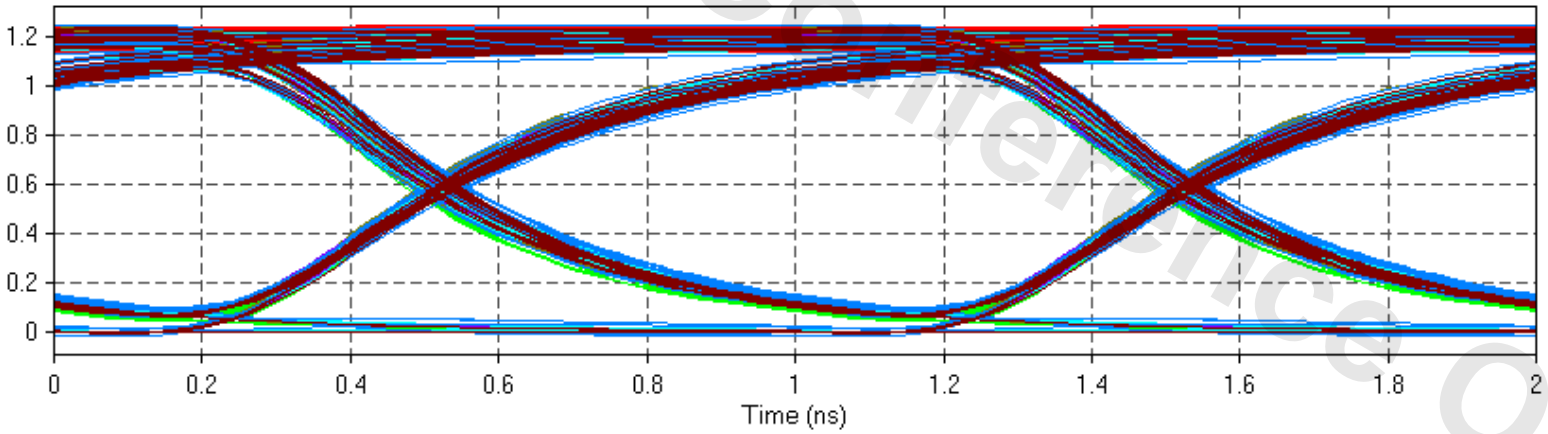
What does DRC forget to tell you?

Complex Simulation Flow for System Verification



Time Consuming for TD Simulation



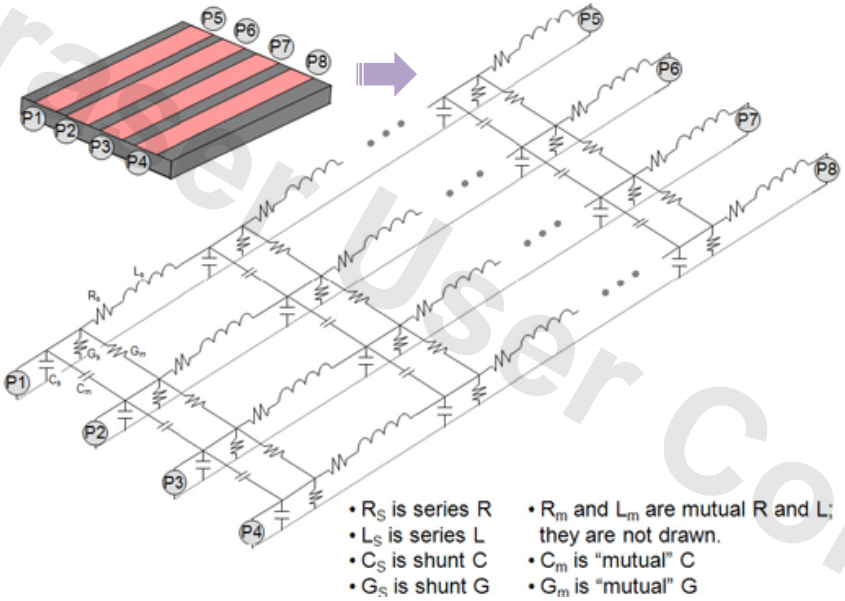


- In general, design sign-off is verified through TD simulation.
- Advanced SI/PI analysis completion relies on experienced and well trained engineer with EDA tools investment.

Simulation and Design Rule Check

- All designs is supposed to be 100% covered by simulation result.
- Simulation results will be derived into rules and applied to similar designs.
- The rest customized part will be covered by simulation.
- The DRC usually contains only the dimensions information, such as length, width, distance, spacing…etc.
- What does this dimension constraint/DRC forget to tell you?

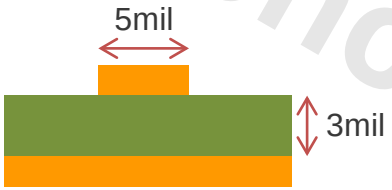
About SI – 1. RLGC information



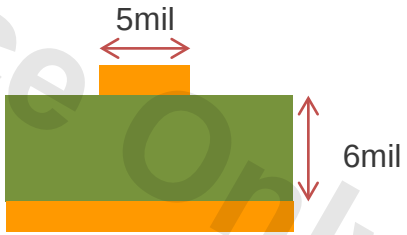
- The generation of equiv. RLGC circuit needs EM calculations.
- Simple design rule check for dimension will not tell you the RLGC value.
- Try to imagine the following case:

Question:
1. Are the DRC results of these 2 structures the same or different? **Same**
2. Do these 2 structures have the same or different RLGC properties? **Different**
3. Do these 2 structures have the same impedance or not?

Case 1:



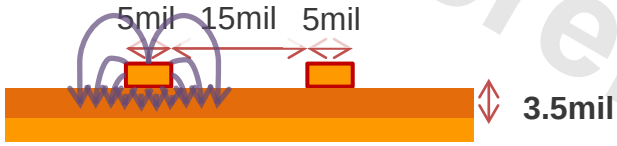
Case 2:



About SI – 2. Z_0 and Xtalk

Talking about crosstalk, you probably follow the 3W rule – set the spacing between adjacent traces to 3 times the width of the trace as the following:

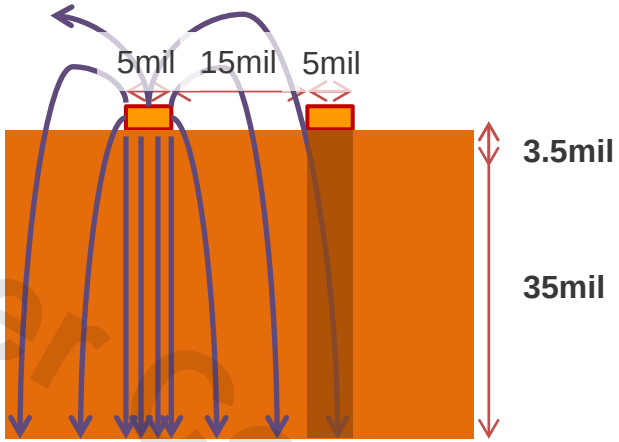
The 3W rule may works well for the following structure:



No DRC violation ➡ No Xtalk issue

About SI – 2. Z_0 and Xtalk

But if the stack-up looks like the following, will 3W rule still works well?



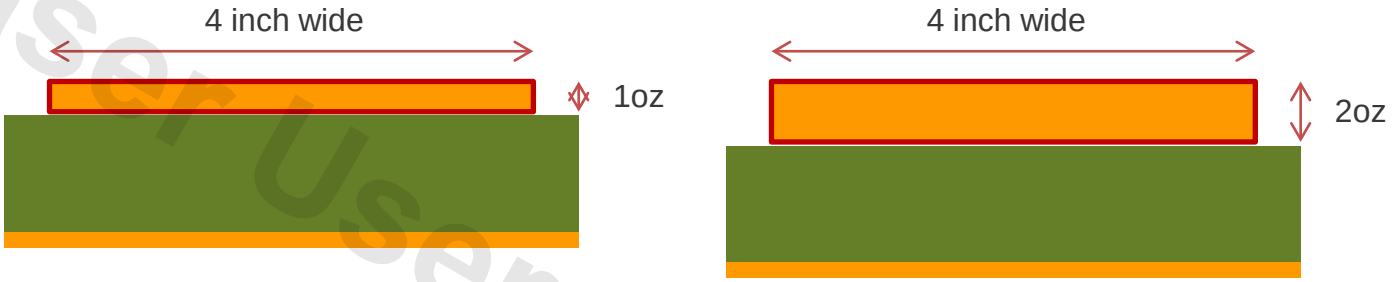
No DRC violation ➡ No Xtalk issue ?

Now, you're not satisfied with simply spacing constraint or the related **DRC** violation warning. You feel you probably need **simulation** or other way to tell you:

How Much the Coupling is

About PI – 1. IR Drop

- Question 1: 4inch for both 1oz copper and 2oz copper?

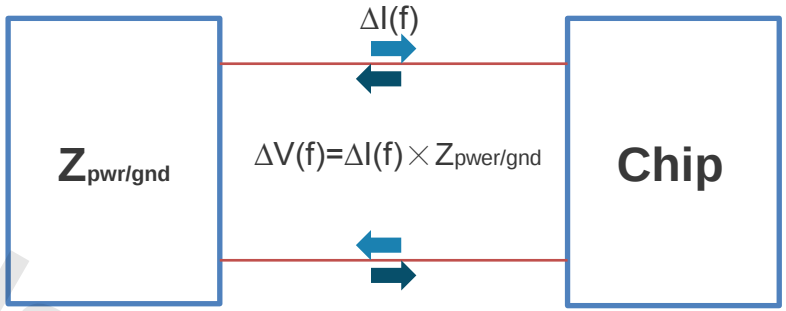


- Question 2: If there're multiple layers for the power delivery, how is the rule?
- Question 3: If the thickness of the layers used for power delivery is different, how is the rule?

Now, you're not satisfied with the simple thumb rule to set the width of power plane, and either, you don't want to use the related DRC violation to judge you design safe or not. You want to know the exact:

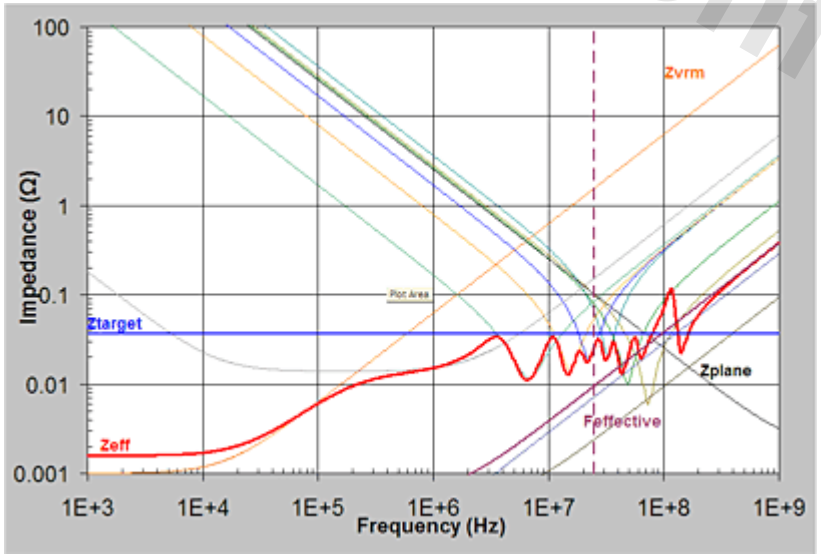
Current Density and IR Drop

About PI – 2. $Z_{PWR/GND}$



The lower $Z_{pwr/gnd}$ is, the better. $Z_{pwr/gnd}$ should be under Z_{target}, where:

$$Z_{target} = \frac{\Delta V_{allowed}}{\Delta I_{max}}$$



No constraint or DRC will help you to control the power ground impedance.

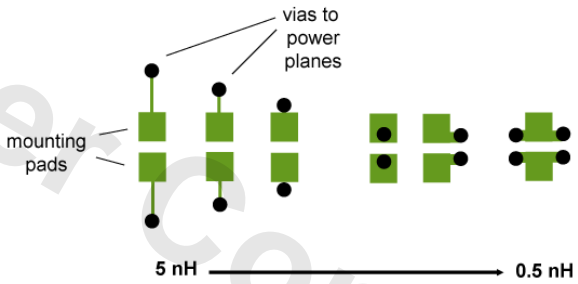
Now you want to have a design checking mechanism to tell you the excact value of $Z_{pwr/gnd}$ and if:

$$Z_{pwr/gnd} \leq Z_{target}$$

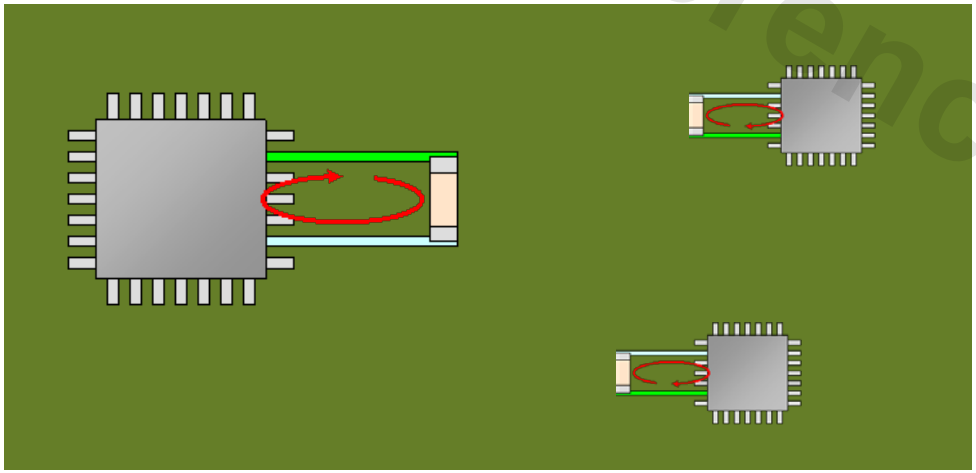
About PI – 3. Loop Inductance of Decap

Talking about loop inductance of DeCap, you would like to know:

- The loop inductance caused by capacitor pad layout:



The loop inductance caused by the current loop:



What are Questions in Mind?

What are Questions in Mind?

- DRC only provides the MINIMUM requirement of design.
- Does following design guide mean good design quality?
- Is it possible to help your customers to fix problem through TD simulation one by one?
- Will be a financial burden to own EDA tools and invest SI/PI engineers?

Any alternative to secure design quality without performing complex simulation?

What is Design Checking?

Design Checking Through EM Simulation

- All SI/PI issues we addressed can be reflected through electrical characteristic parameters, like R, Z, L, NEXT/FEXT coefficient…
- Post process EM simulation result (S-parameter) and provide more intuitive information to show design weakness for improvement.

Allegro SI Suite

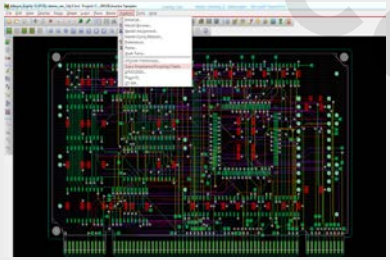
Allegro SI Base with SPEED2000

Highlights

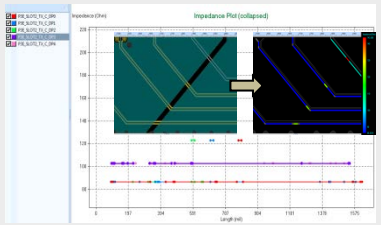
- Detailed Trace Impedance and Coupling check
- Provide SI Metrics Check
- Checking and Modifying in One Tool

Allegro SI

- Very powerful to do layout modification
- Unique function to do trace impedance check and coupling check in one tool
- Capability to import multiple layout format from EDA tools

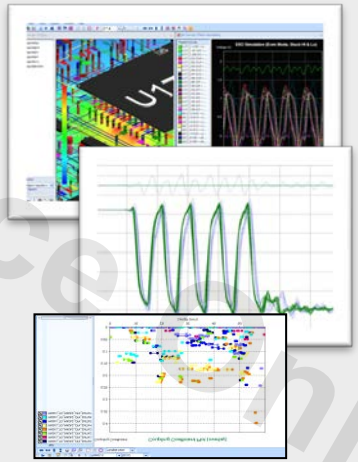


Trace Impedance and Coupling check

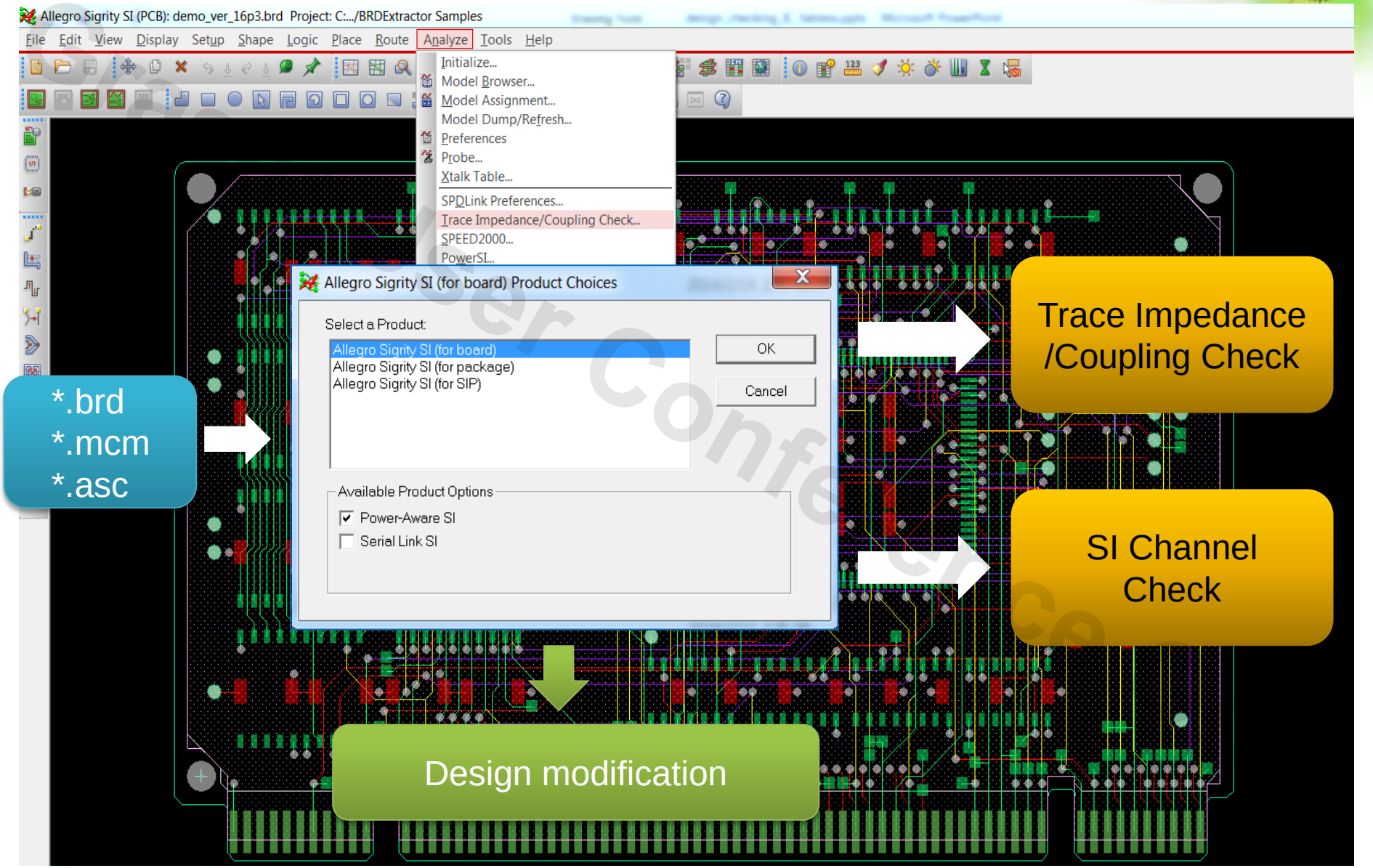


Speed2000

- Unique animation of transient field propagation across PCBs and packages
- Exceptional layout based signal integrity simulation including non-ideal power and ground systems
- Only solution for EMC simulation with non-linear drivers and receivers

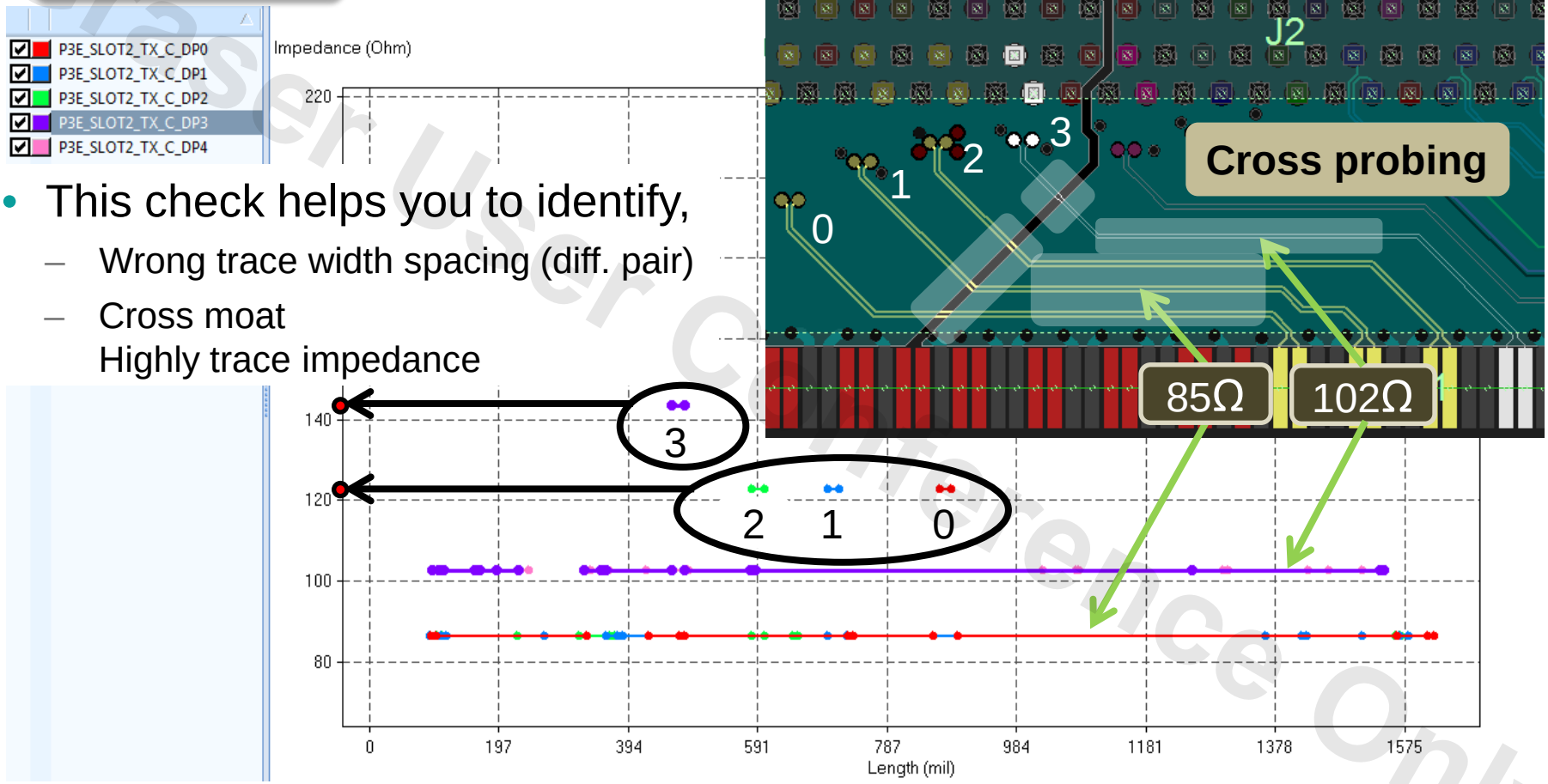


SI Checking Flow



Trace Impedance Check

Visual plot

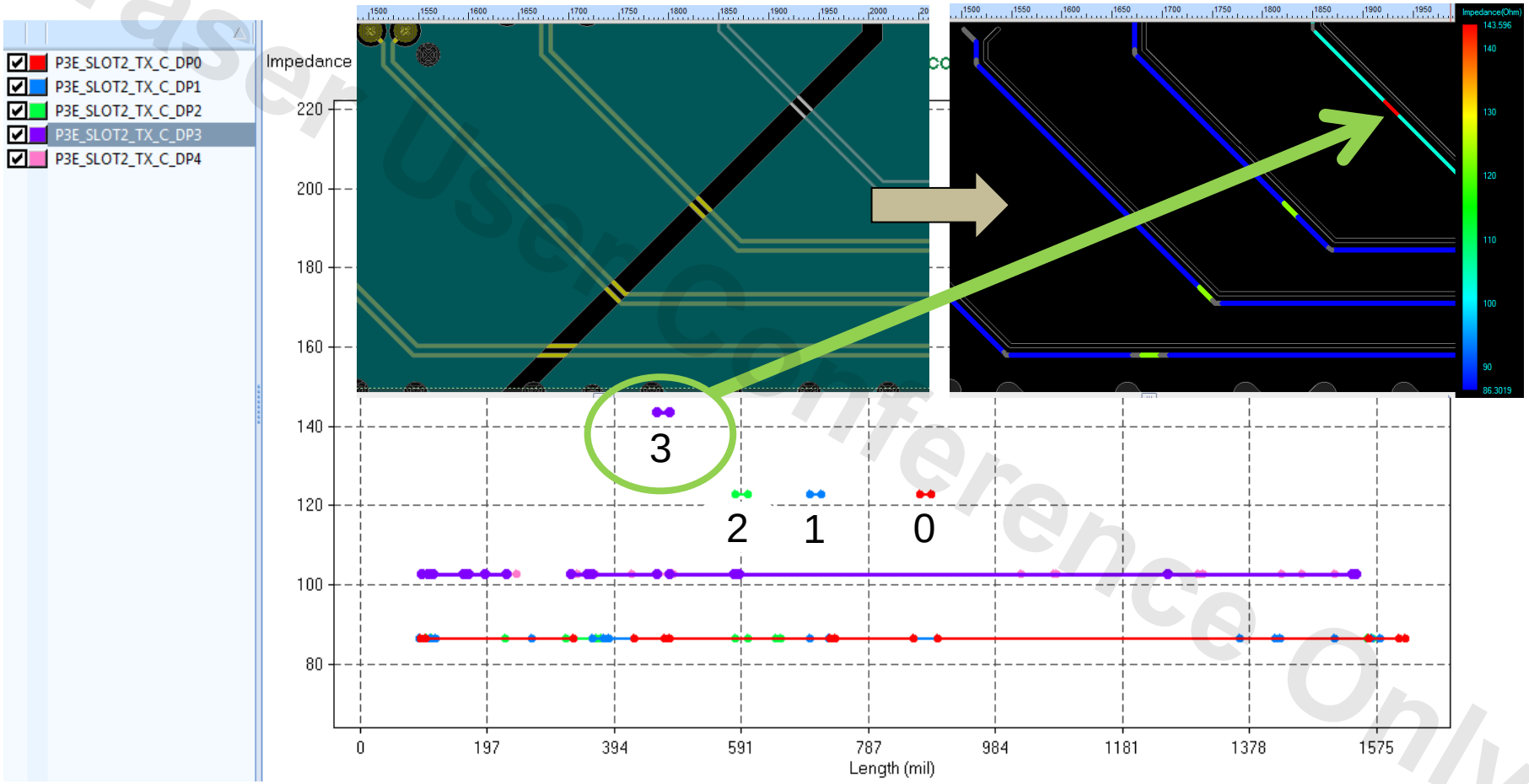


- This check helps you to identify,
  - Wrong trace width spacing (diff. pair)
  - Cross moat
    Highly trace impedance

- Visually or tabular result for trace impedance check that shows trace segments mismatch with target impedance.

Trace Impedance Check

Cross Probing



- Cross probing allows you to identify defects quickly.

Trace Impedance Check

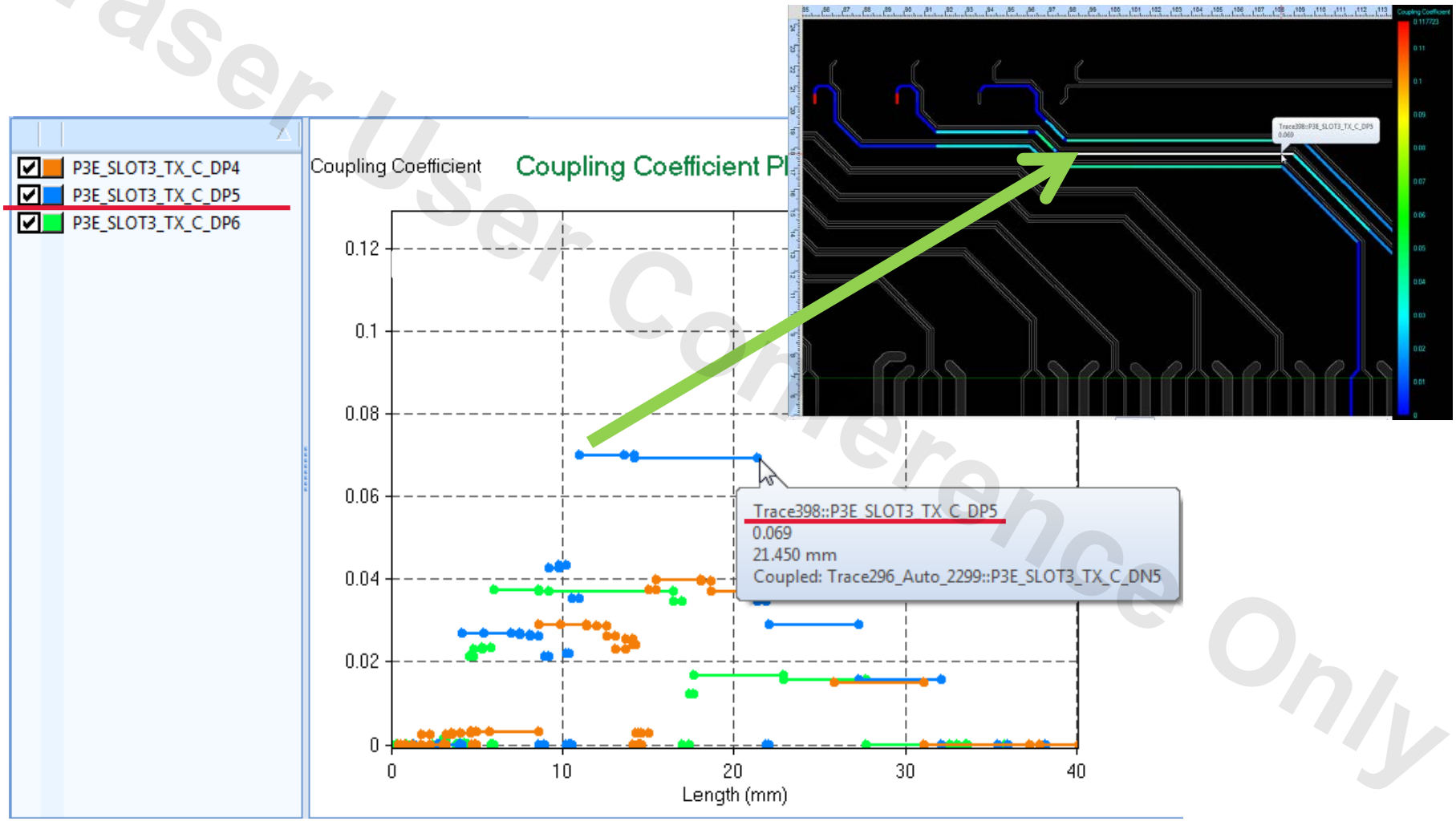
Tabular Results

Net count	Net name	No. of segments without reference	No. of trace reference discontinuities	No. of vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)	Dominant Impedance (Ohm)	Dominant Imp Length (%)	Trace total length (mil)	Trace delay(ns)
1	P3E_SLOT2_TX_C_DN0	1	3	2	144.946	56.449	56.449	92.921	1633.158	0.233
2	P3E_SLOT2_TX_C_DN1	1	3	2	144.946	56.449	56.449	93.168	1583.722	0.225
3	P3E_SLOT2_TX_C_DN2	1	3	2	144.946	56.449	56.449	93.186	1575.168	0.224
4	P3E_SLOT2_TX_C_DN3	1	3	2	153.005	63.836	63.836	93.074	1549.678	0.220
5	P3E_SLOT2_TX_C_DN4	1	1	2	63.836	63.836	63.836	94.228	1513.121	0.214
6	P3E_SLOT2_TX_C_DP0	1	3	2	144.946	56.449	56.449	92.923	1633.643	0.233
7	P3E_SLOT2_TX_C_DP1	1	3	2	144.946	56.449	56.449	93.221	1583.404	0.225
8	P3E_SLOT2_TX_C_DP2	1	3	2	144.946	56.449	56.449	93.184	1574.865	0.224
9	P3E_SLOT2_TX_C_DP3	1	3	2	153.005	63.836	63.836	93.059	1546.528	0.219
10	P3E_SLOT2_TX_C_DP4	1	1	2	63.836	63.836	63.836	94.221	1511.225	0.214
11	P3E_SLOT3_TX_C_DN0	1	1	1	56.449	56.449	56.449	94.142	1490.958	0.211
										0.208
										0.217
										0.209
										0.225
										0.214
										0.203
										0.212
										0.212
										0.209
										0.217
										0.210
										0.225
										0.214
										0.203
										0.212

- Cross moat?
- Any trace segment mismatch? Cross moat?
- Too much breakout neck length?
- Too much MS/SL routing difference in a group?
- The same trace length means the same trace delay?
- Routing on MS/SL has different trace delay.

Trace Coupling Check

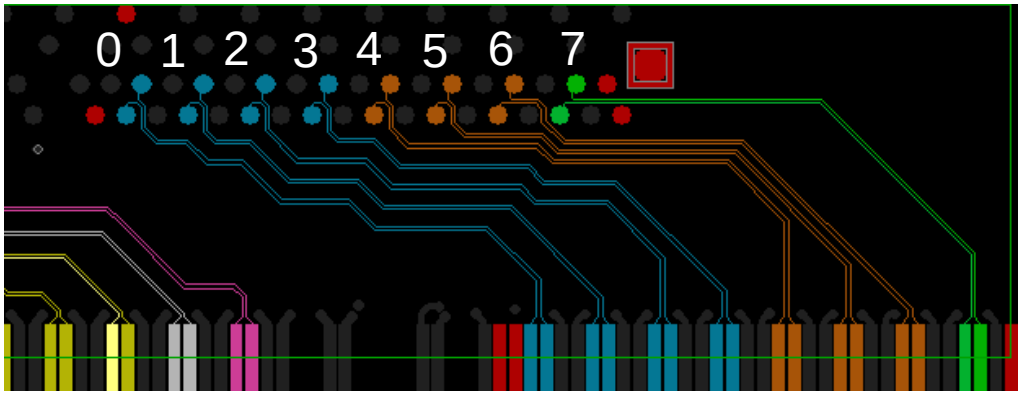
Cross probing helps to resolve issue intuitively



Trace Coupling Check

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
1	P3E_SLOT2_TX_C_DP0-P3E_SLOT2_TX_C_DN0	P3E_SLOT2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
2	P3E_SLOT2_TX_C_DP1-P3E_SLOT2_TX_C_DN1	P3E_SLOT2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
3	P3E_SLOT2_TX_C_DP2-P3E_SLOT2_TX_C_DN2	P3E_SLOT2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
4	P3E_SLOT2_TX_C_DP3-P3E_SLOT2_TX_C_DN3	P3E_SLOT2_TX_C_DN2	0.125%	6.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.125%	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

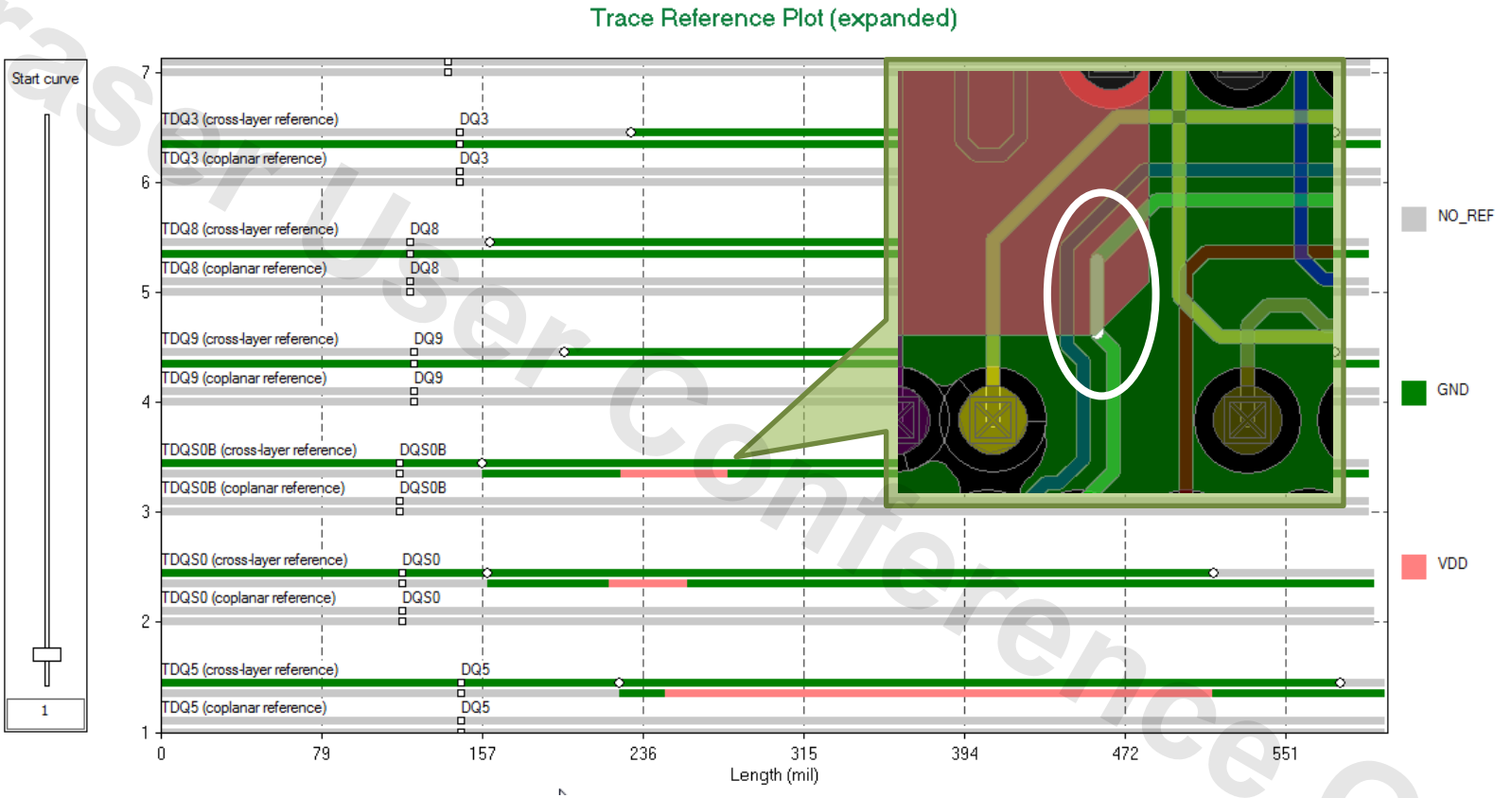
18X



Through this test, you will see,

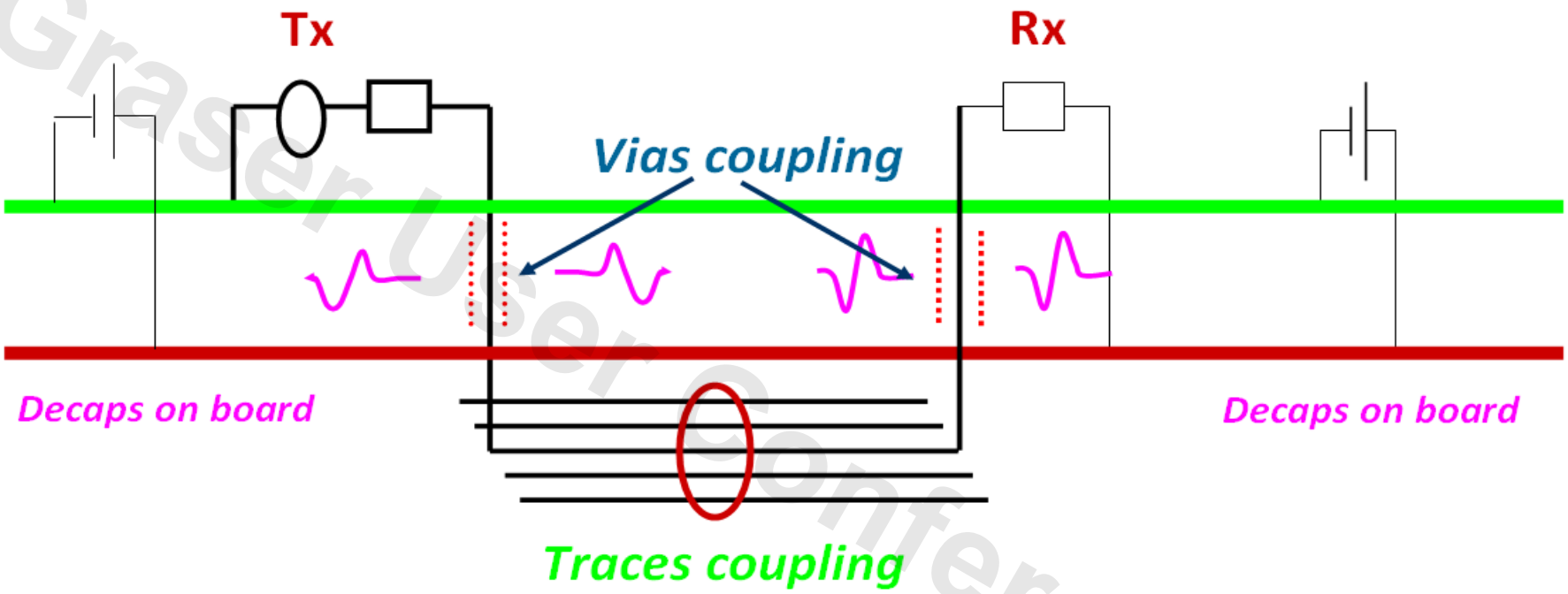
- Tight coupling pairs
- Max coupling aggressor
- Dangerous vs. safe coupling
  → **18X** (= 2.81% / 0.156%)

Trace Reference Check
(Including co-planar)



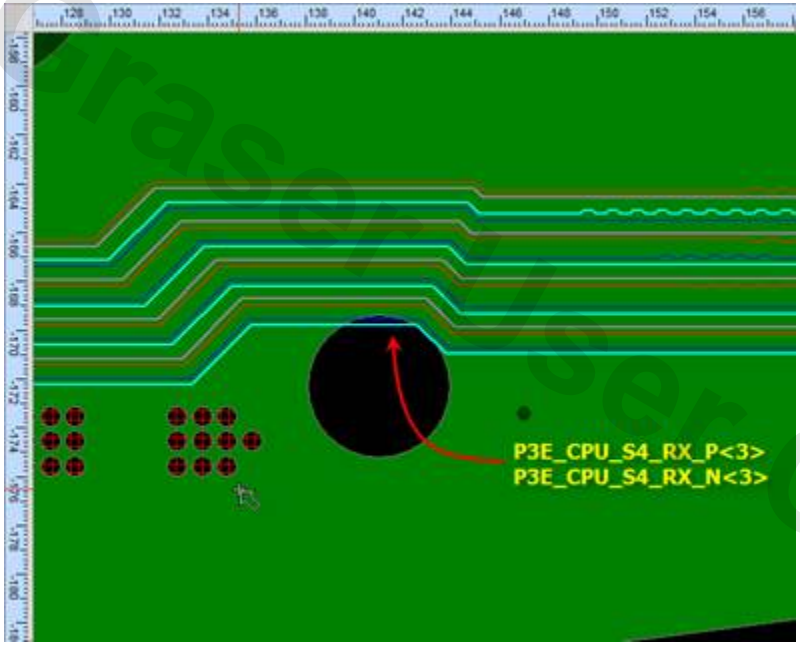
- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

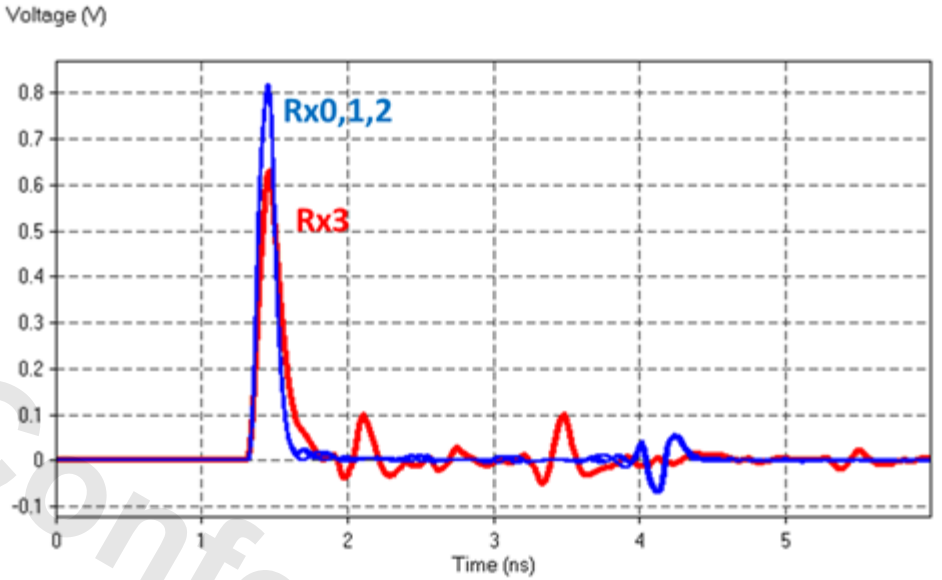
SI Channel Check

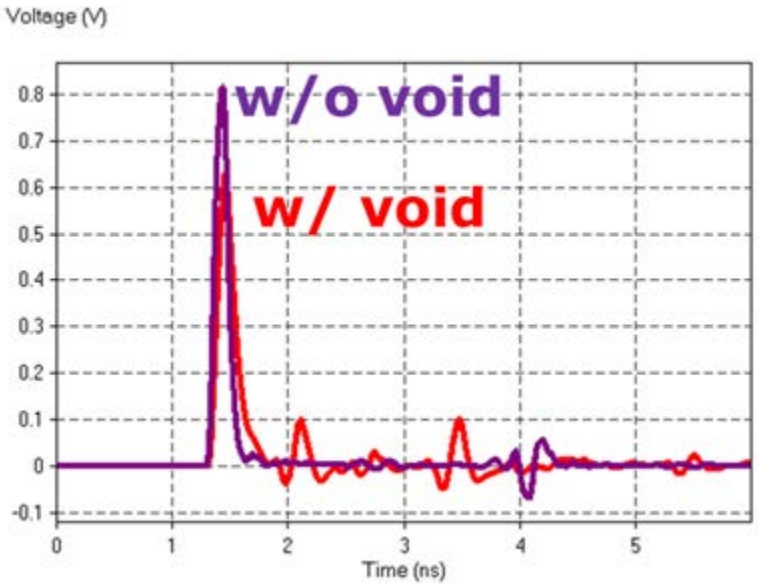


- Signal quality is affected by crosstalk among signals, EM coupling between signal and P/G planes and non-ideal return current path.
- The linear source and load are applied automatically for signal TD simulation
- Post process result waveforms (signal waveform, NEXT/FEXT waveforms) into signal to noise ratio for signal quality judgment

SI Channel Check







	INT_Sig	INT_ISI	INT_XTK	P-eye	P-ratio
RX3 w/ void	67.84	104.59	5.12	-41.87	0.62
RX3 w/o void	86.00	54.64	5.00	26.36	1.44

- An example shows the trace segment is over the void that causes impedance discontinuity and leads to worse signal quality

Allegro PI Suite

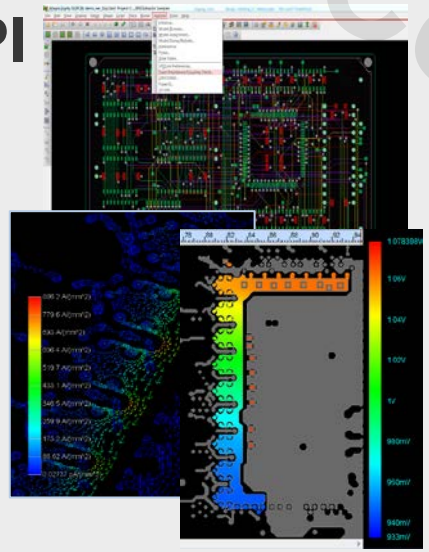
Allegro PI Base with OptimizePI

Highlights

- Detailed IR Drop Analysis
- Power Plane Impedance and Loop Inductance Analysis
- Automatic Report Generation

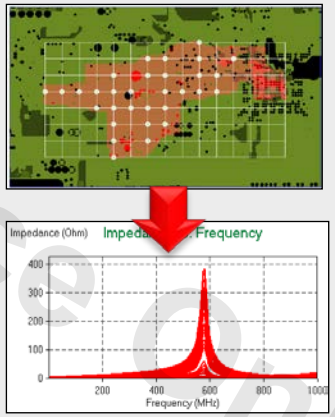
Allegro PI

- Very powerful to do layout modification
- Unique function to do IR drop analysis
- Capability to import multiple layout format from EDA tools.



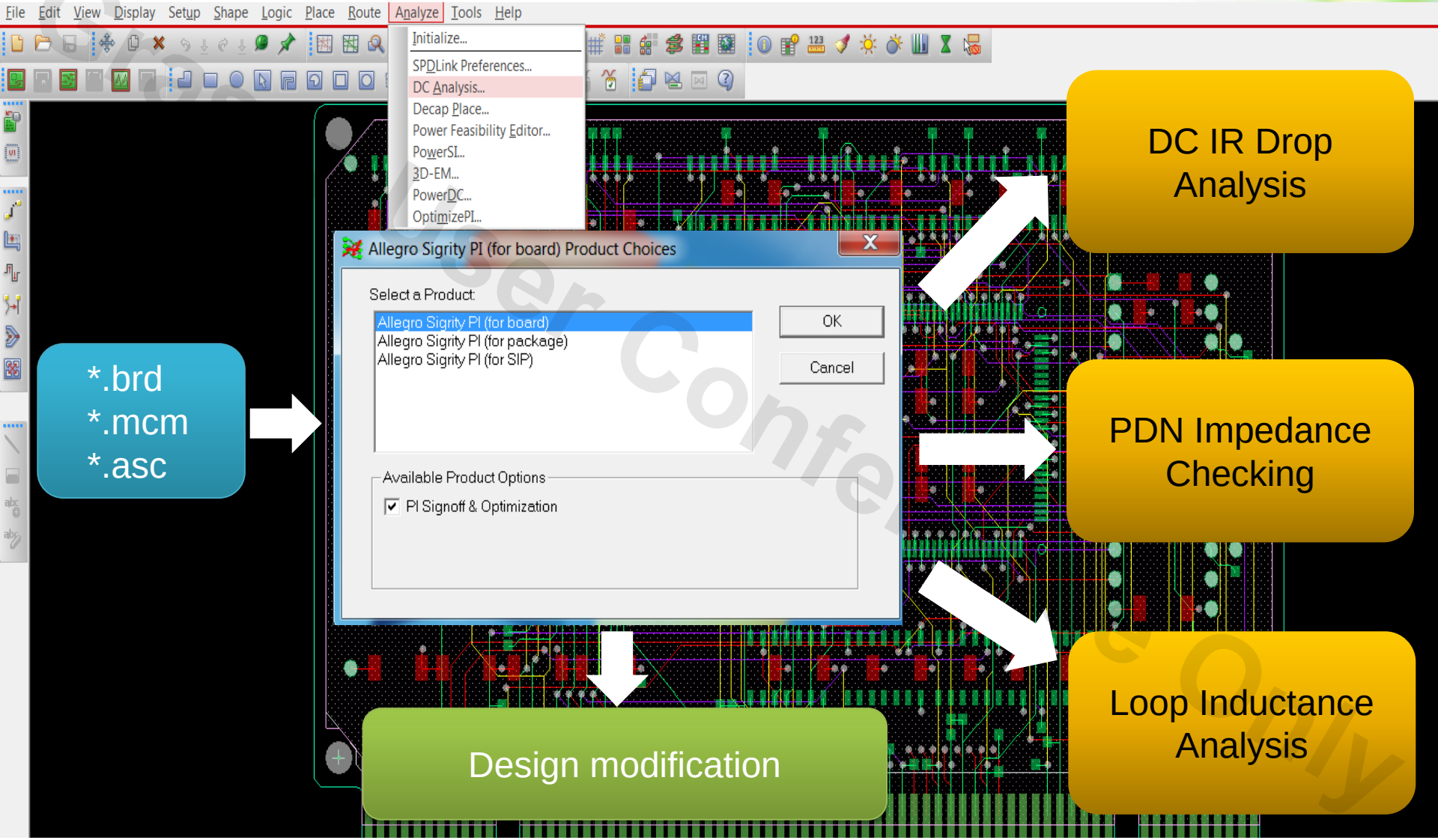
OptimizePI

- Automated decap optimization and verification features
- Clear presentation of economic benefits from decap optimization
- Flexibility in meeting targeted objectives (performance, cost, area …)



Automated positioning of EMI decaps

PI Checking Flow



DC IR Drop

3 Results

3.1 Electrical Results Table

VRM	VRM	VRM_J1_VCC_GND
	Nominal voltage (v)	1
	Actual current (A)	5
Sink	Sink	SINK_U17_VCC_GND
	Actual voltage (v)	0.969269
	Margin (v)	-0.0207306
	Fail/Pass	Fail

OpenXlsFile

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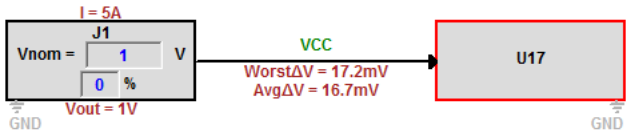
PowerDC Simulation Report

Date: 11:36 April 25, 2014

3.2 DC Analysis Block Diagram Result



Actual Voltage(V)	Voltage(V) referring to VRM	Current(A)	IR Drop Simulated	Specification	Pass/Fail
0.9693	0.9828	5	ΔVp = 17.2mV(1.7%) ΔVg = 13.6mV(<0.1%)	1 V + 1 % - 1 %	Fail_V

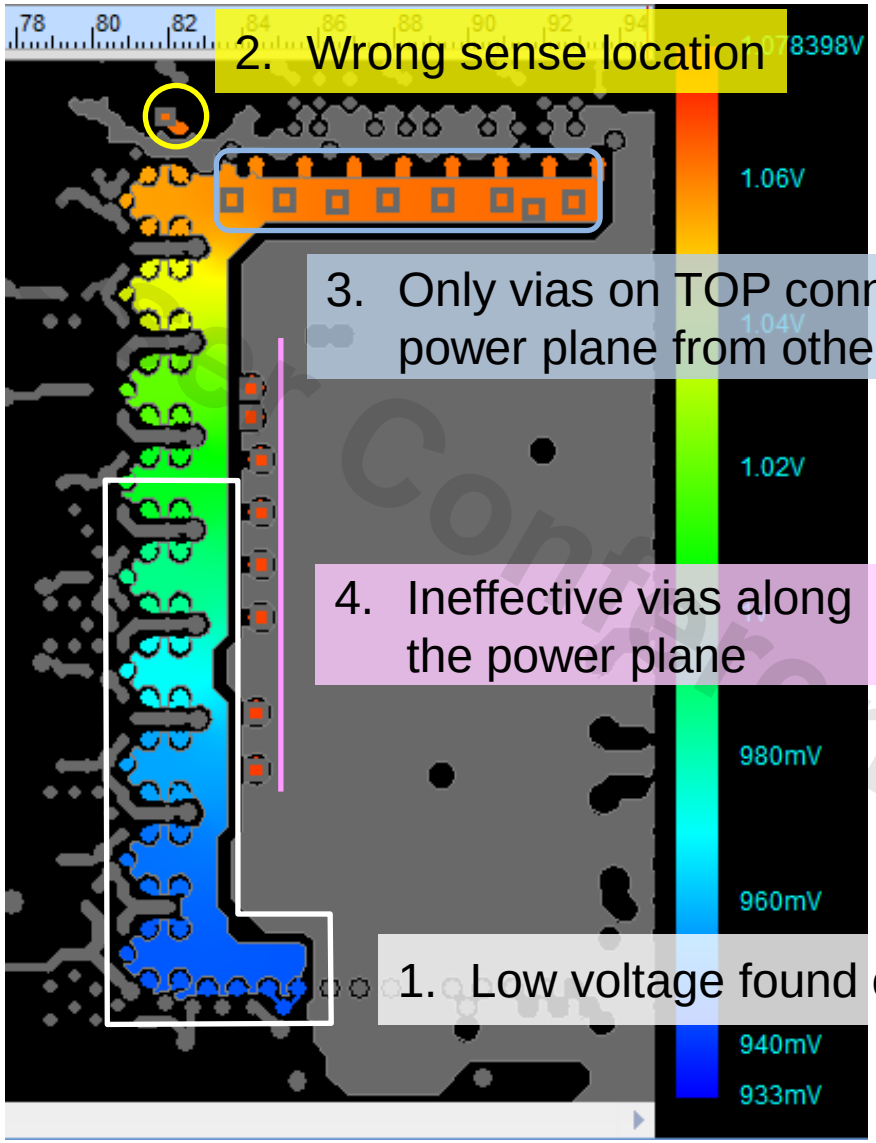
Note:

-----IRdrop on net is calculated on Power net only.

-----If a net has current flow from different sources, IRdrop is displayed with the largest IRdrop.

- Identify voltage drop on each pin of the IC
- Found design weakness through current density and vector
- Report generation for customer review

DC IR Drop – Electrical Analysis



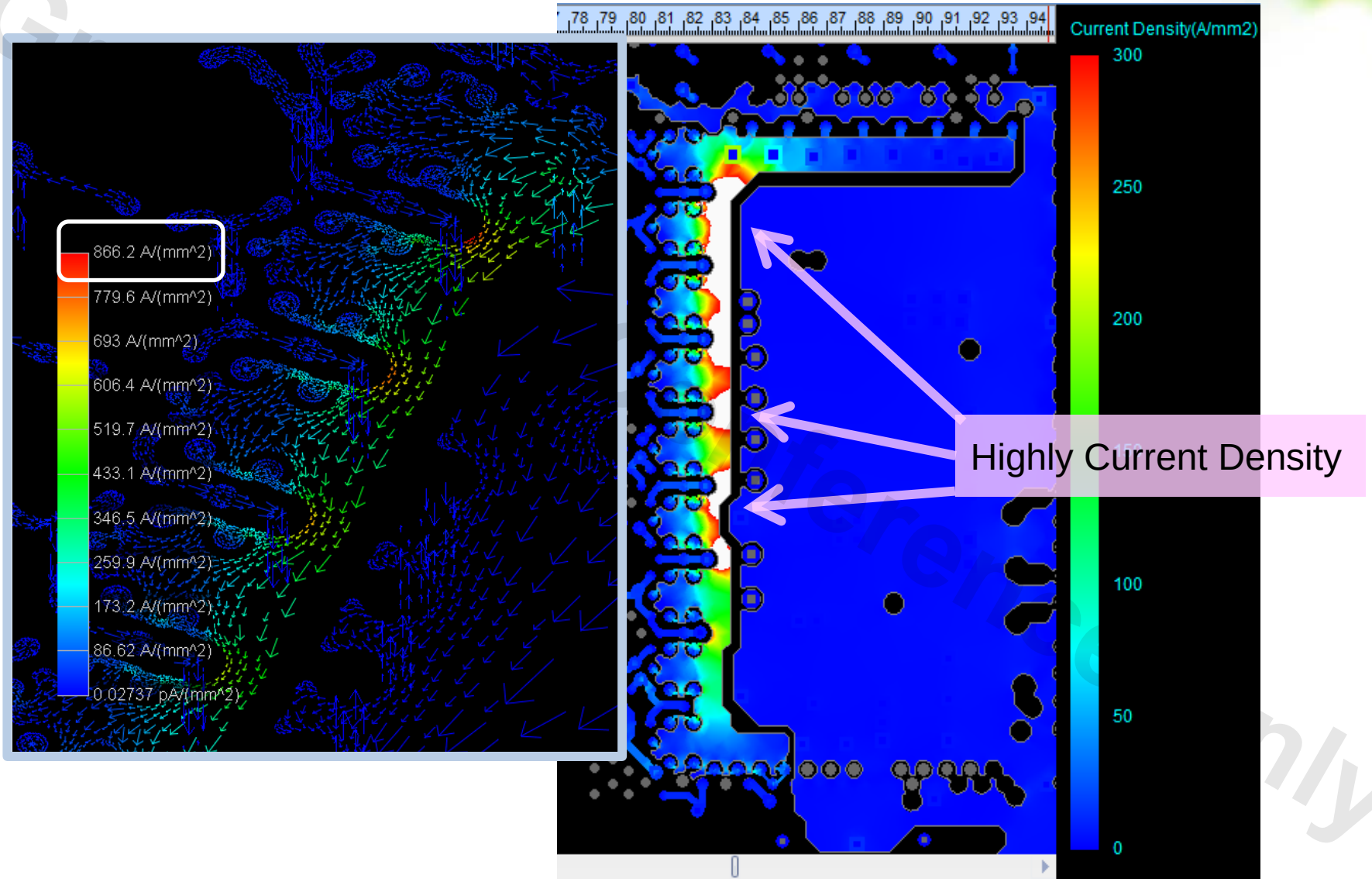
2. Wrong sense location

3. Only vias on TOP connecting power plane from other layers

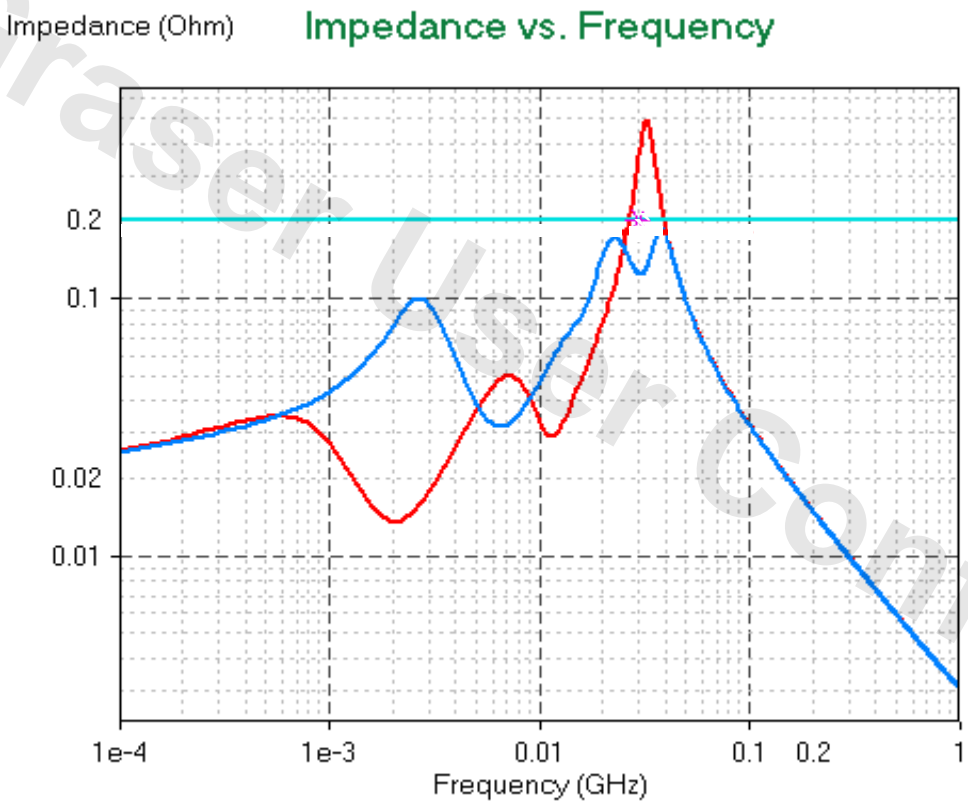
4. Ineffective vias along the power plane

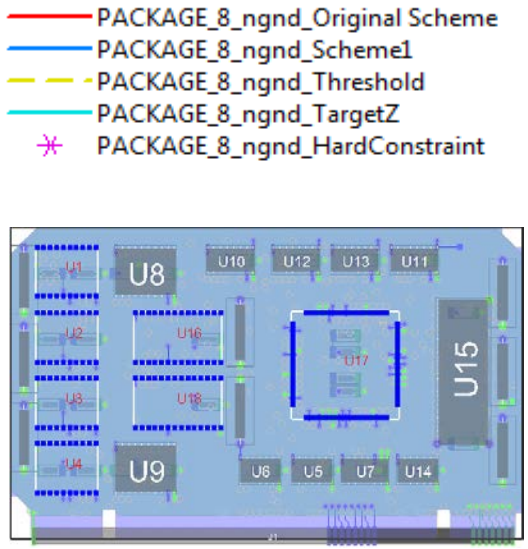
1. Low voltage found on bottom side

DC IR Drop – Current Distribution



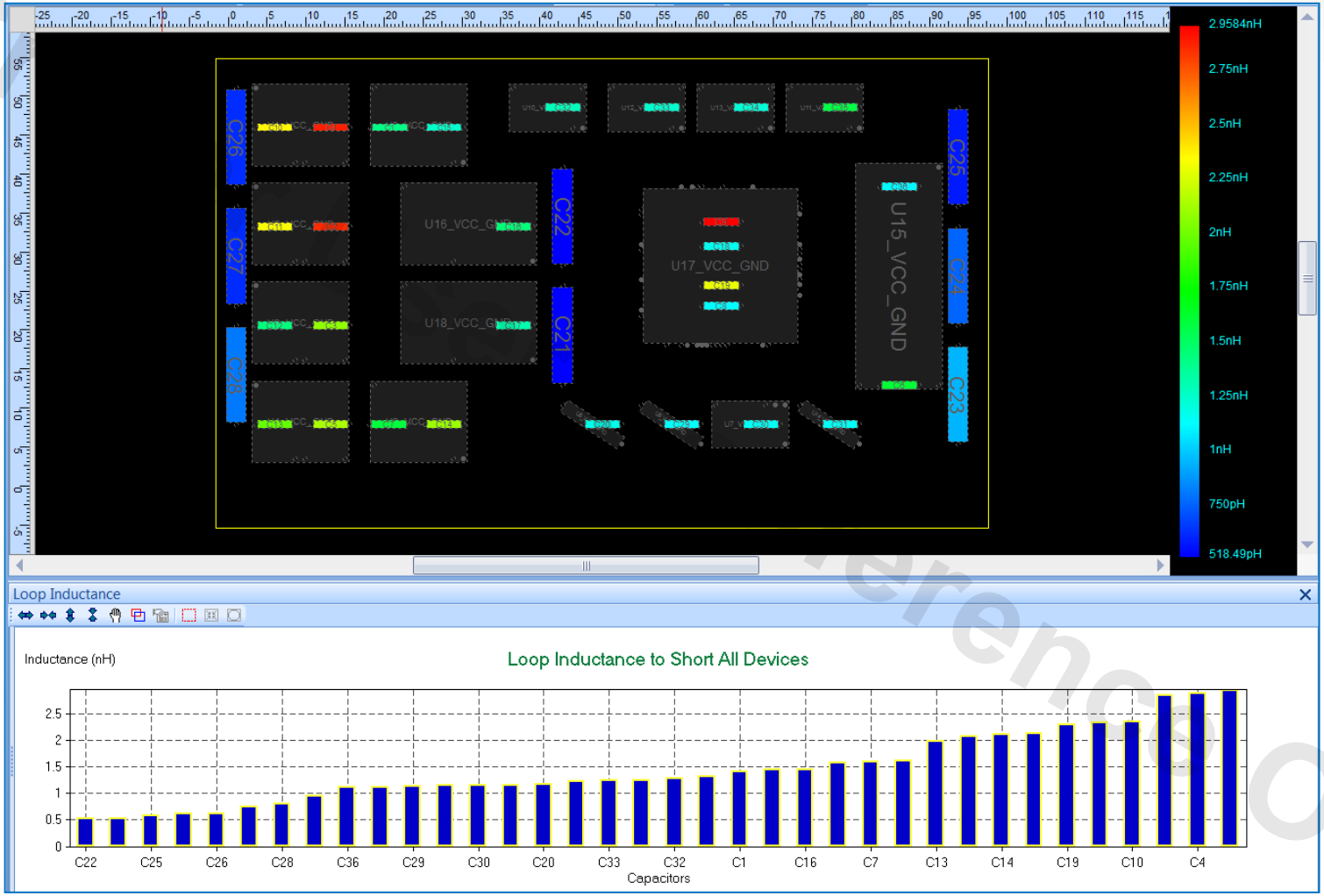
PWR/GND Impedance





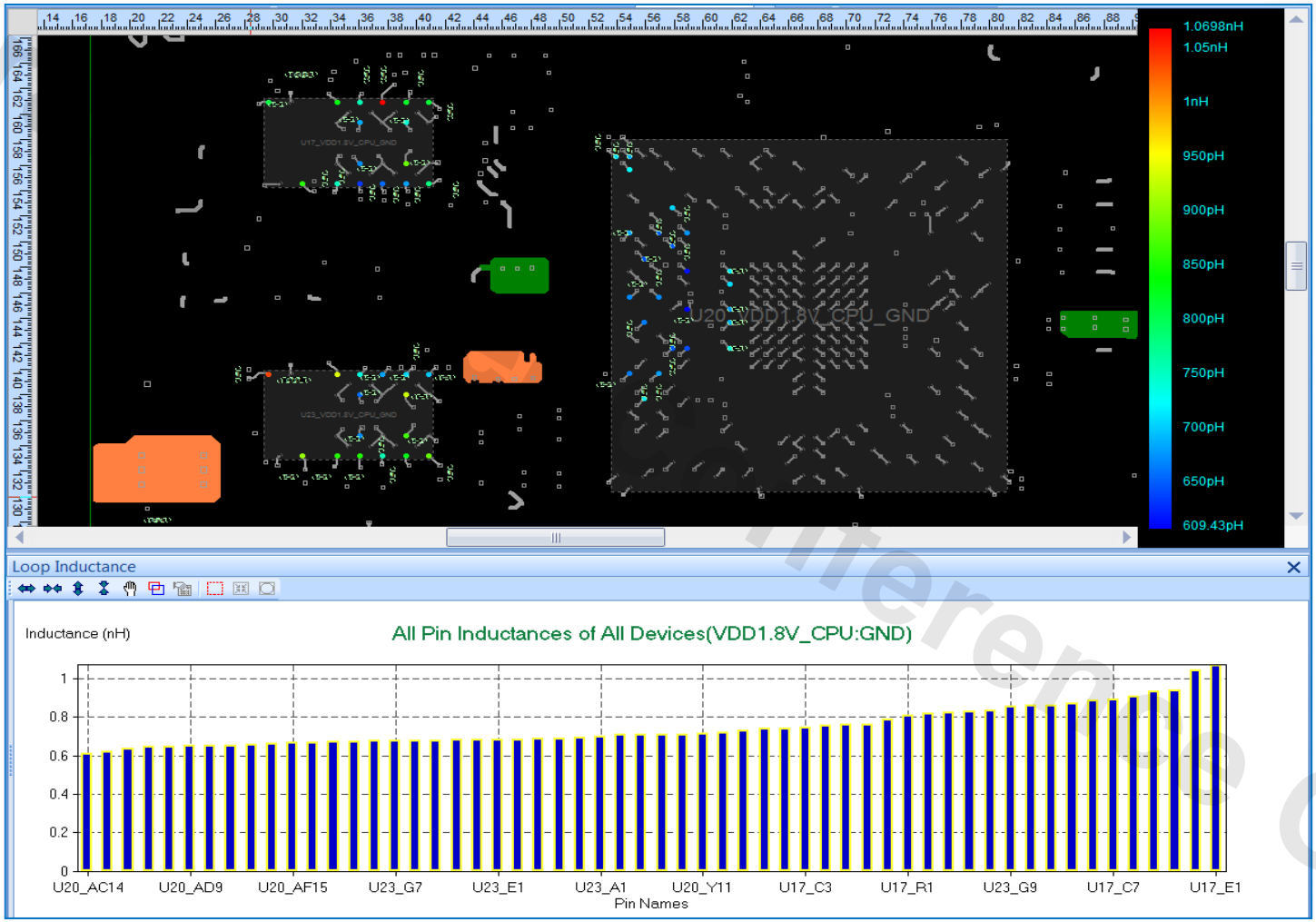
- Check PWR/GND plane impedance.
- Through gene calculation, optimize impedance by placing correct capacitors on correct location.
- Input and transfer impedance as indicators for power integrity analysis.

Decap Loop Inductance



- Check loop inductance (including trace escape from decap pads, vias and P/G loop to IC) for each decap

IC Device Power Pin Inductance



- Help to indentify the weak pins by measuring the inductance of each pin and analyzing the capacitors placement effect to pins.

Summary

- Either SI/PI design check or sign-off TD simulation can help to find out design potential risks or problems.
- Facing multiple customer boards design with secured design quality, design checking is an alternative with efficiency and cost balanced.
- Rather than geometry DRC rules check, EM based design check helps you to find out design problems and assess the consequence through what if.