PCB Power Delivery Design from DC to Mid-Frequency

Foxconn
Abby Chou

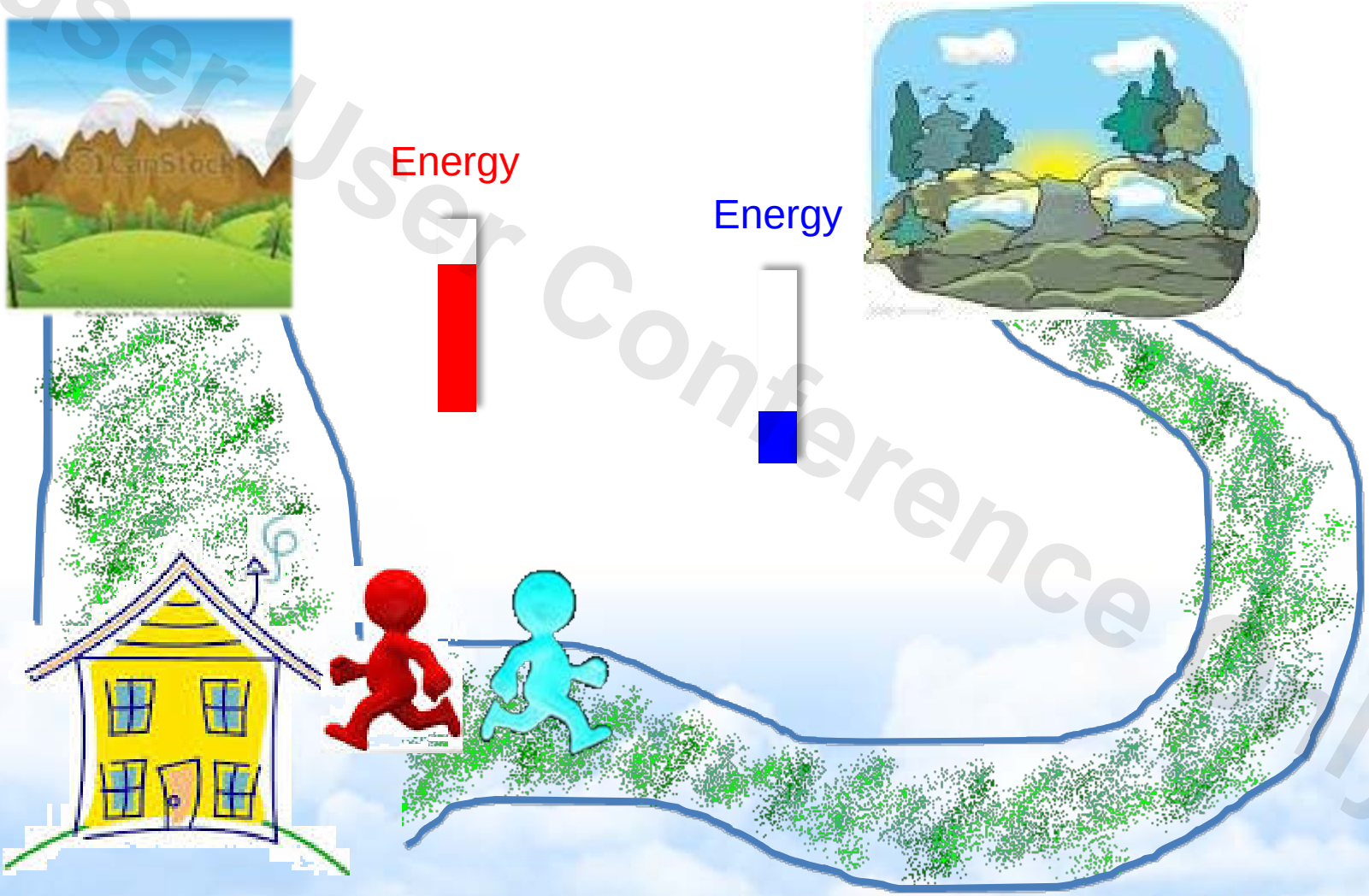
FOXCONN

Company Introduction

Founded	Headquarters	Employees	Products
February 1974	Tucheng District	1.23 million	Server Storage Mobile Phone Pad TV ⋮

Voltage Drop and Thermal Co-Simulation

Illustration for Voltage Drop



How to Calculate Resistance

- 40mil trace width for 1A current ?
  - Need to take ***cross-section area*** and ***length*** into consideration.

$$R_{Copper} = \rho \frac{L}{A} = \frac{1}{\sigma} \frac{L}{A}$$

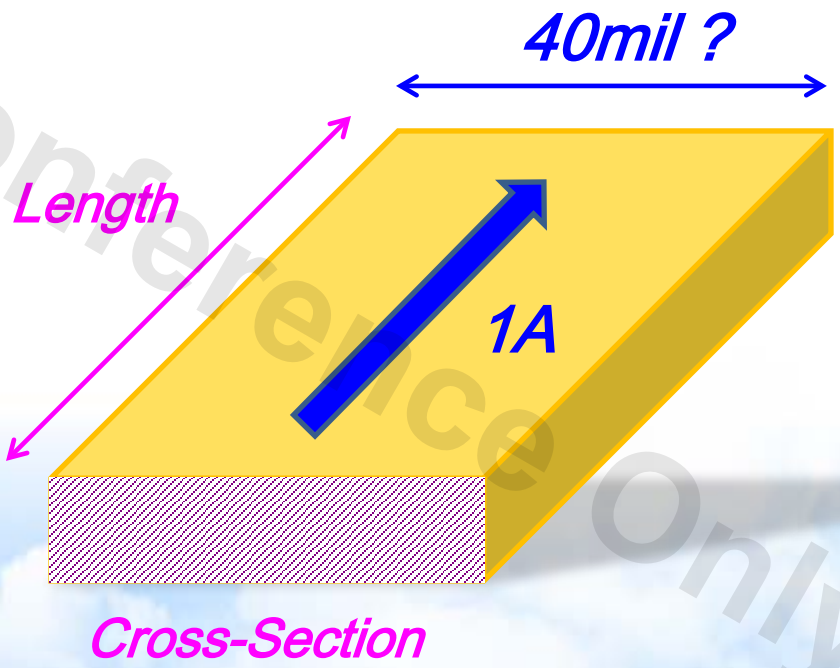
R : Resistance (Ω)

ρ : Resistivity (Ω*m)

σ : Conductivity (S/m)

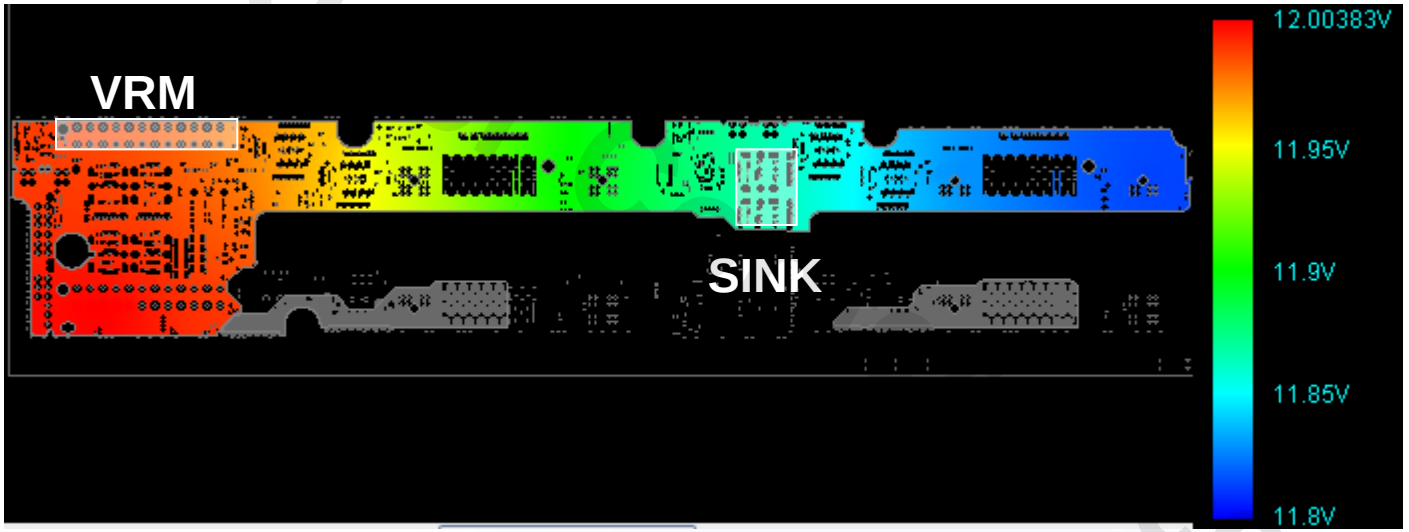
L : Length (m)

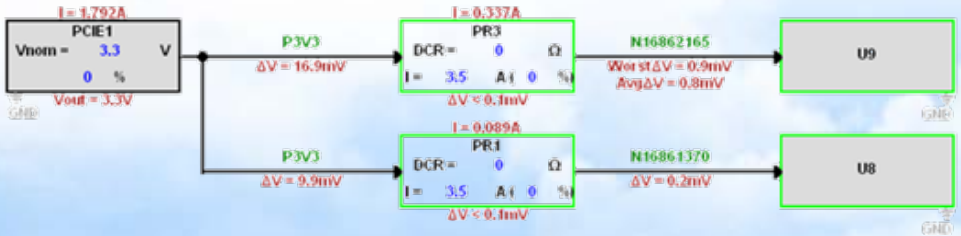
A : Cross-Section Area (m^2)



Analysis in PowerDC

❖ For the irregular shape, manual calculation by formula is difficult and simulation is necessary.

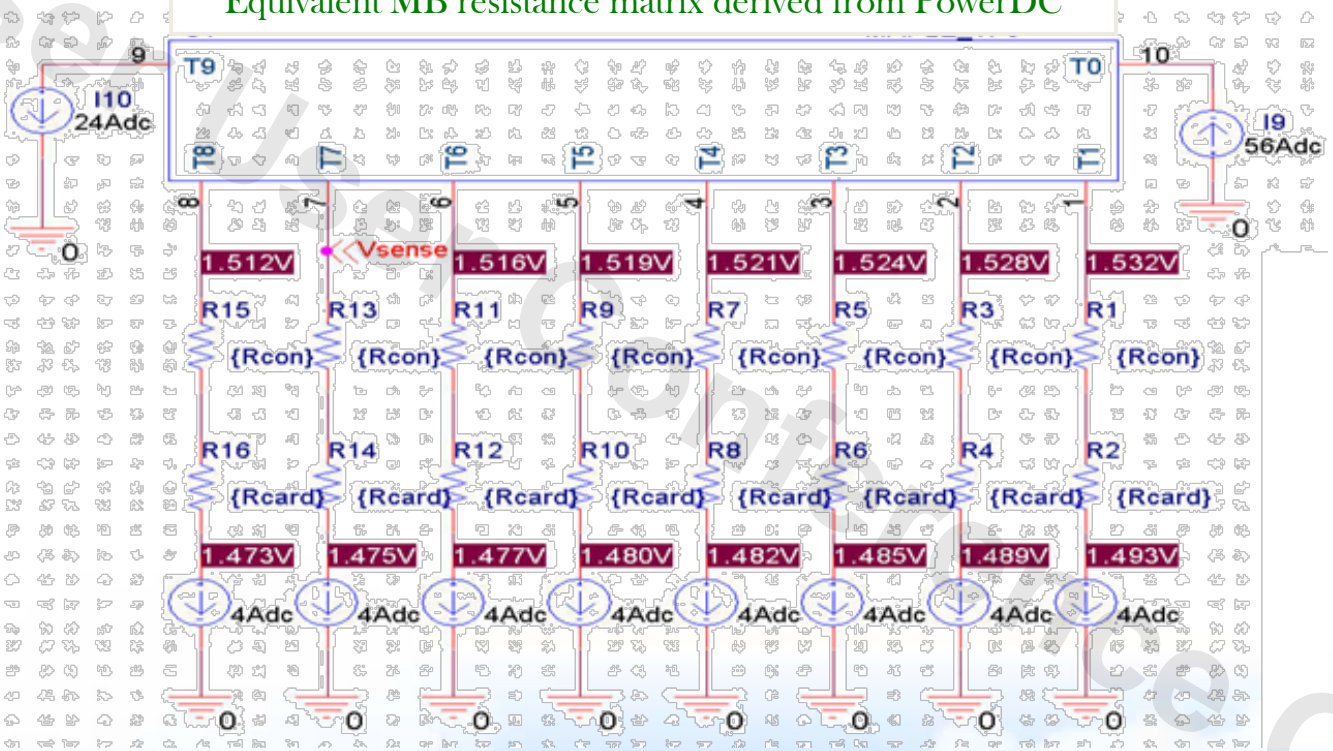




	Actual Voltage(V)	Voltage(V) referring to VRM	Current(A)	IR Drop Simulated	Specification	Pass/Fail
U9	3.282	3.282	0.337	ΔVp = 17.7mV(0.5%) ΔVg = 0.2mV(<0.1%)	3.3 V +5 % -5 %	Pass
U8	3.29	3.29	0.089	ΔVp = 10.2mV(0.3%) ΔVg = 0.2mV(<0.1%)	3.3 V +5 % -5 %	Pass

Voltage Drop Correlation

Equivalent MB resistance matrix derived from PowerDC



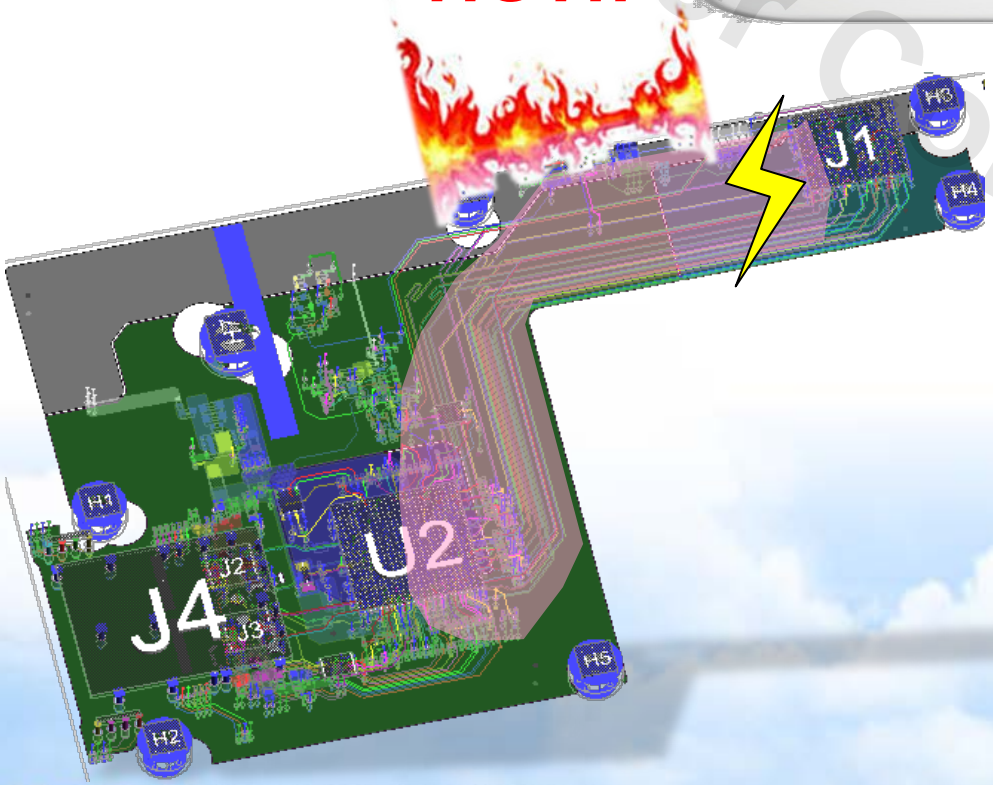
Voltage@AMB	FB1	FB2	FB3	FB4	FB5	FB6	FB7	FB8
Measured	1.474V	1.480V	1.477V	1.483V	1.481V	1.488v	1.487V	1.493v
Simulated	1.473V	1.475V	1.477V	1.480V	1.482V	1.485V	1.489V	1.493V

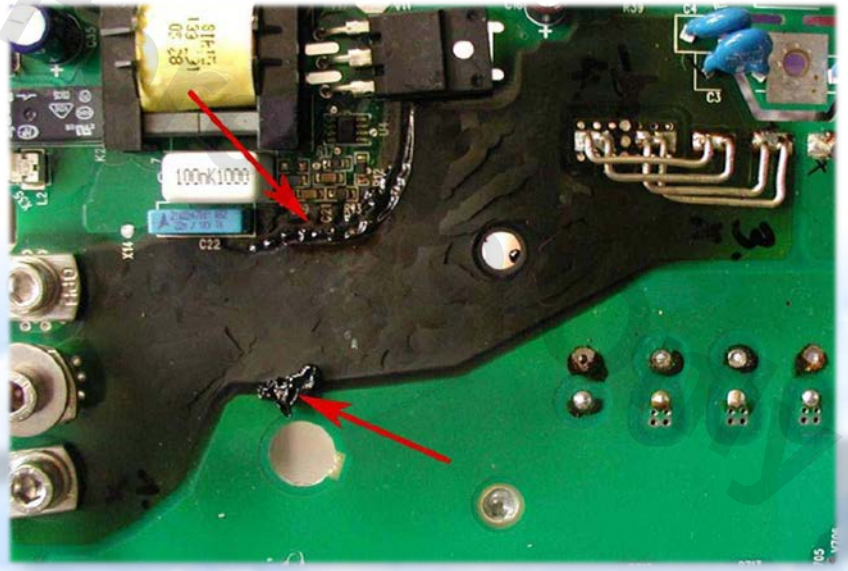
PCB Temperature

High Current Density

➡ High Temperature Rise

➡ PCB Burned

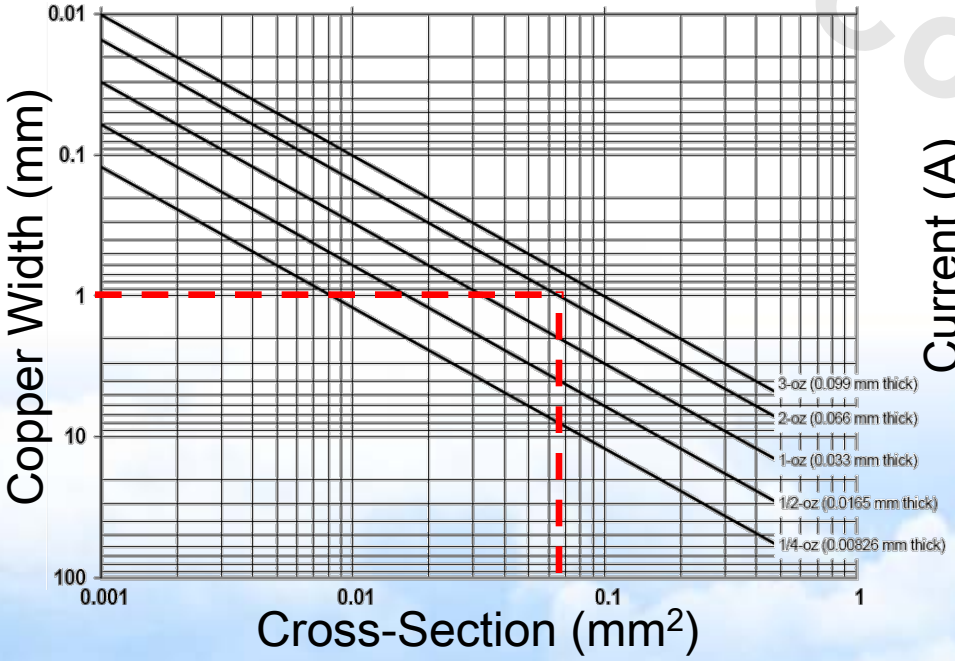




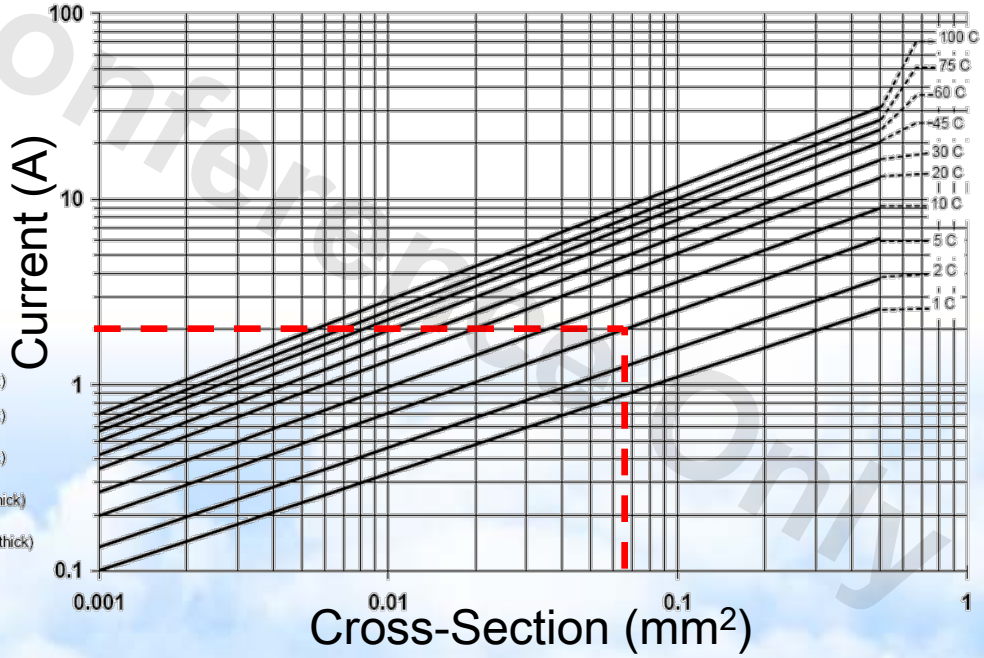
PCB Temperature Simulator

- PCB temperature become higher and more important due to the larger current.

Copper Width : 1mm, Cross-Section : 0.067mm^2



Current : 1.1A, PCB Temperature Rise : 5°C

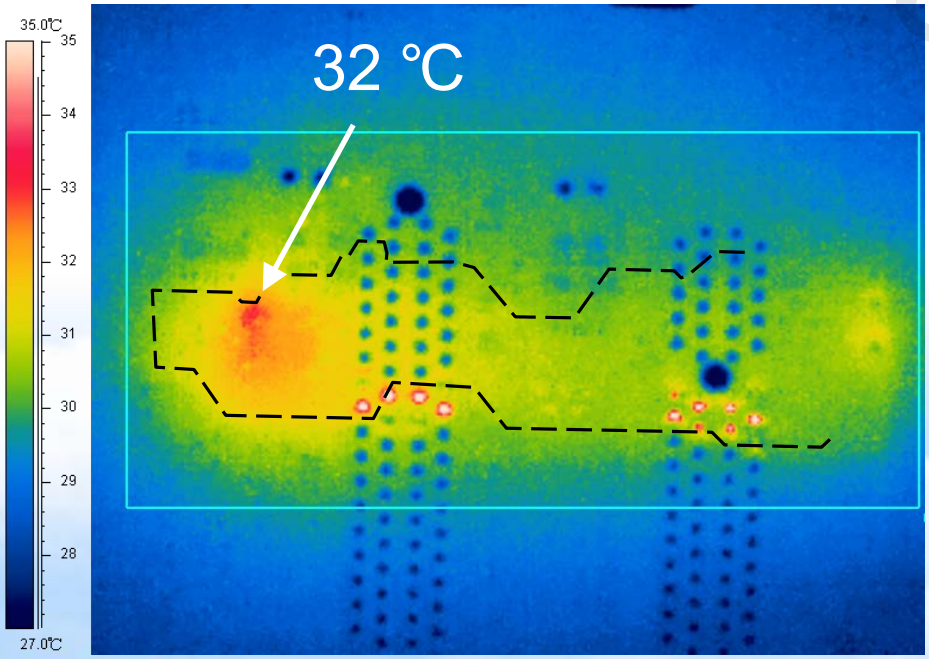


PCB Temperature Distribution

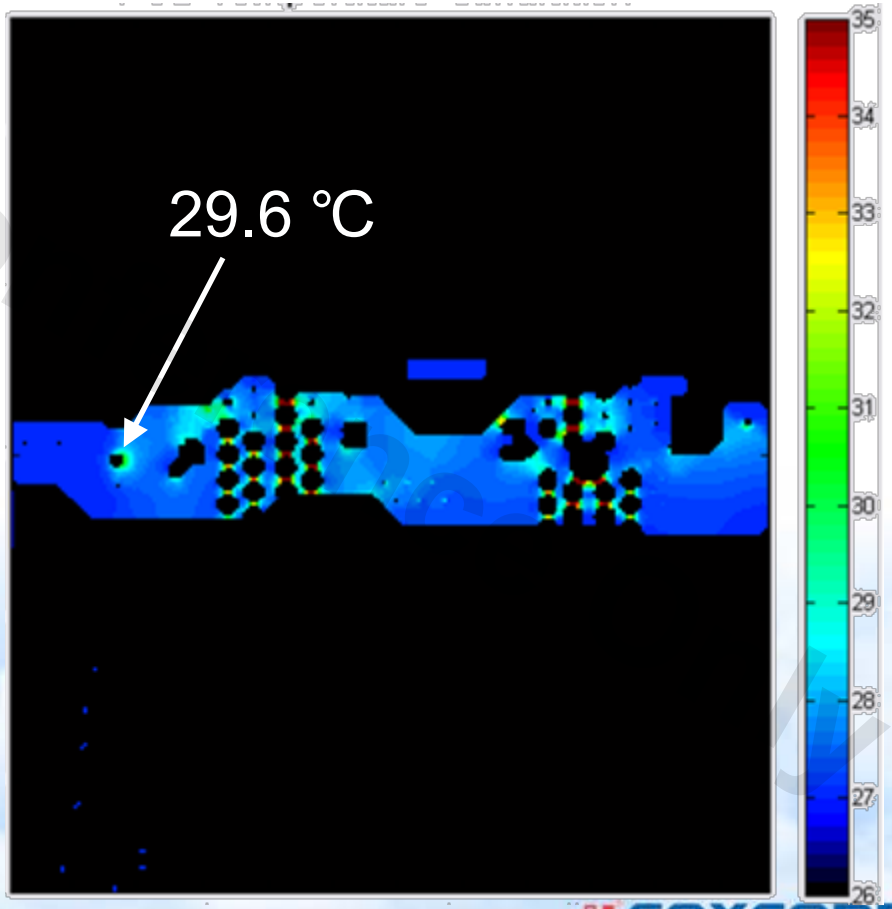
❖ Foxconn in-house tool can calculate PCB temperature distribution by using ***copper width***, ***cross-section*** and ***flowing current***. (Ref. doc. : IPC-2221, IPC-2152)

2℃ ~ 3℃ variation due to the ***air-flow*** and ***heat transfer***.

Infrared Ray Camera

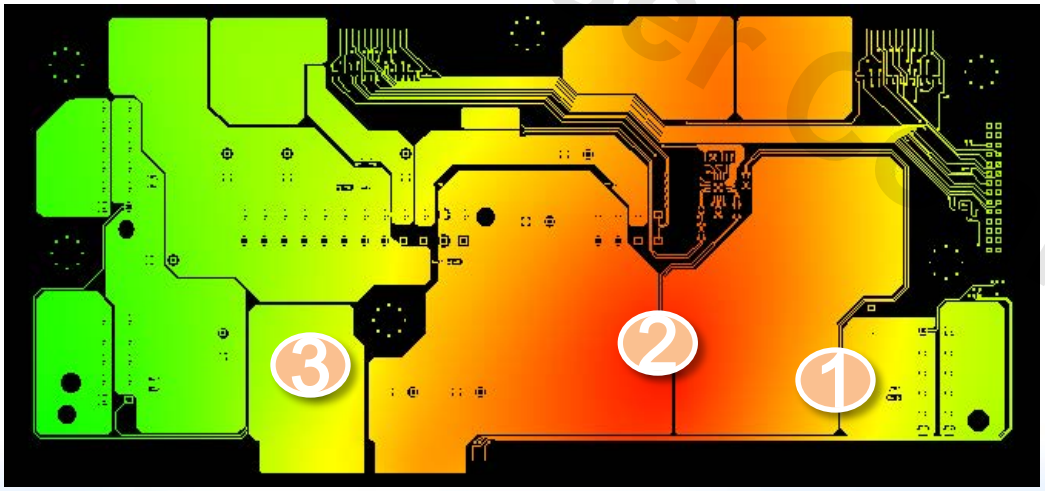


In-House Simulator



Temperature Simulation in PowerDC (1/2)

- Total power: 1400W



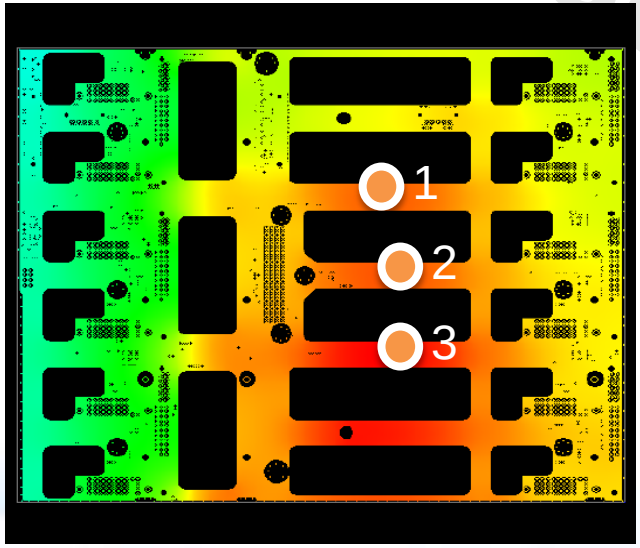
	Simulation	Measurement
1	51.3 ℃	52.6 ℃
2	55.8 ℃	58.3 ℃
3	47.6 ℃	50.9 ℃

Variation < 4℃

Temperature Simulation in PowerDC (2/2)

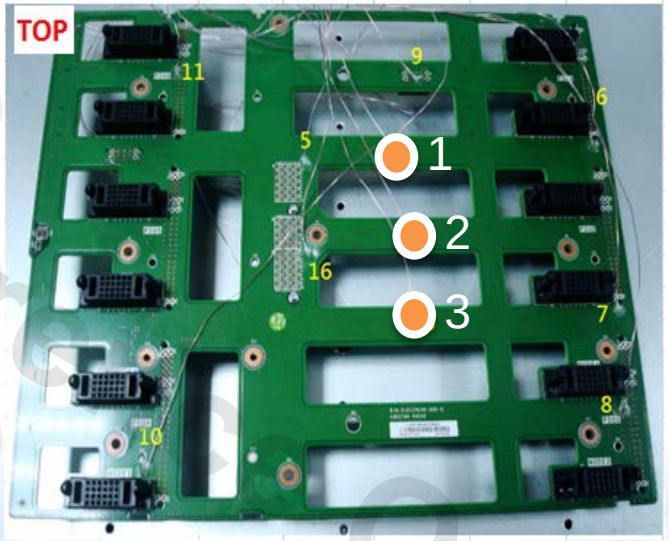
- Total power: 3900W

Simulation



133 ℃	1	131 ℃
132 ℃	2	127 ℃
137 ℃	3	133 ℃

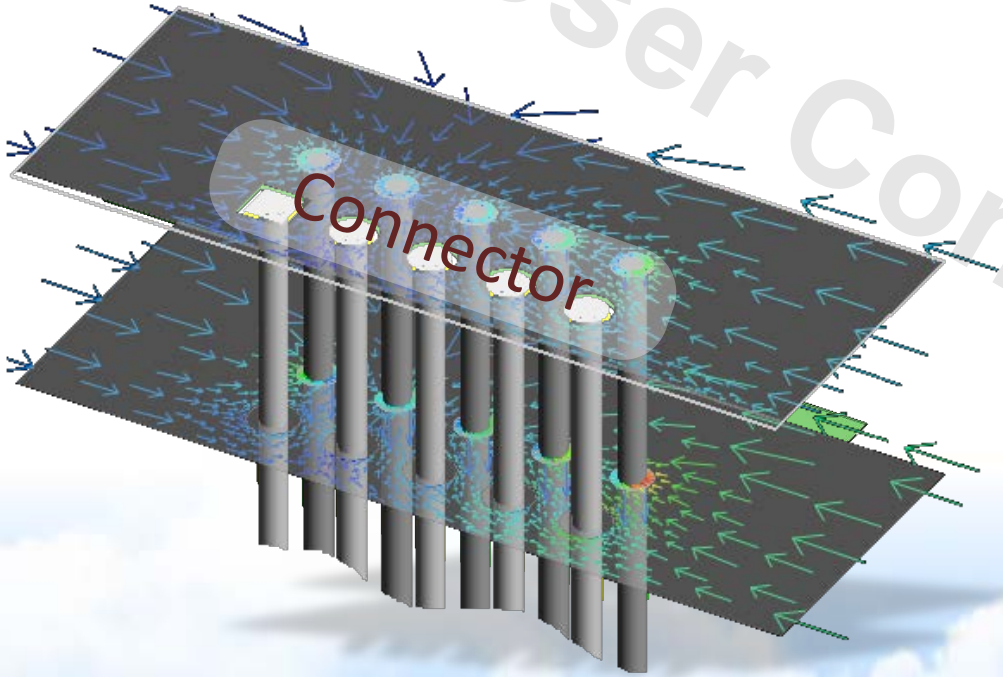
Measurement



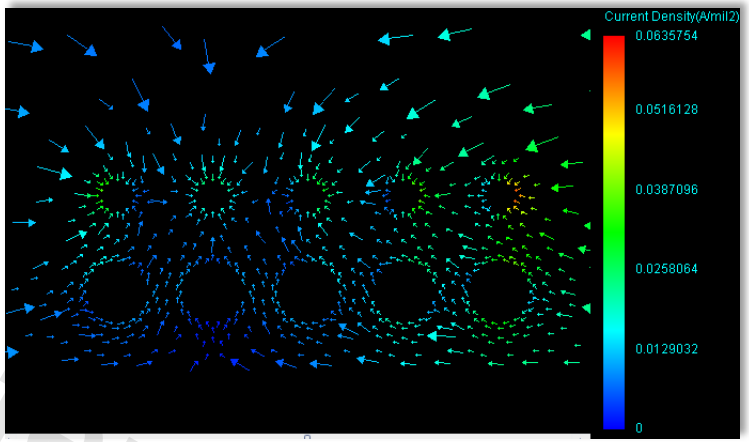
Variation < 5℃

Via Current Simulation in PowerDC (1/2)

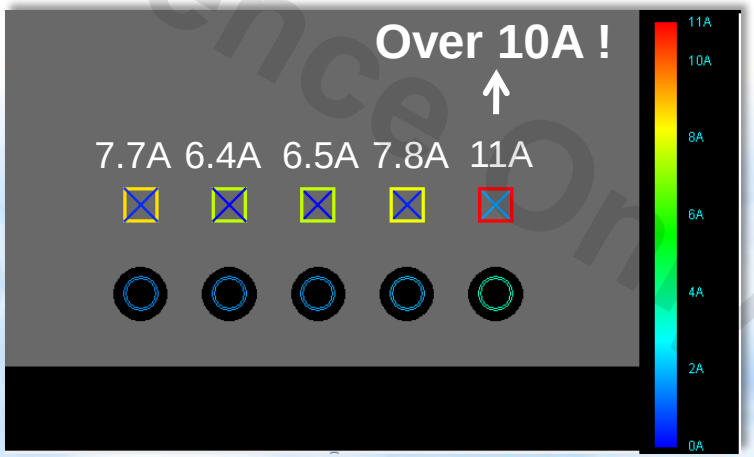
- The connector via current can not over 10A for thermal concern.



Current Vector & Density Plot

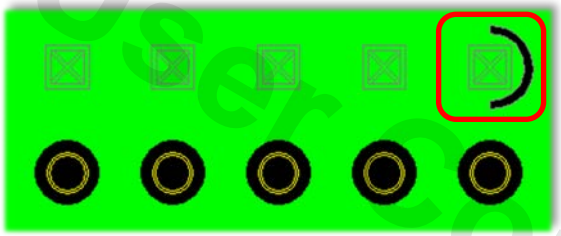


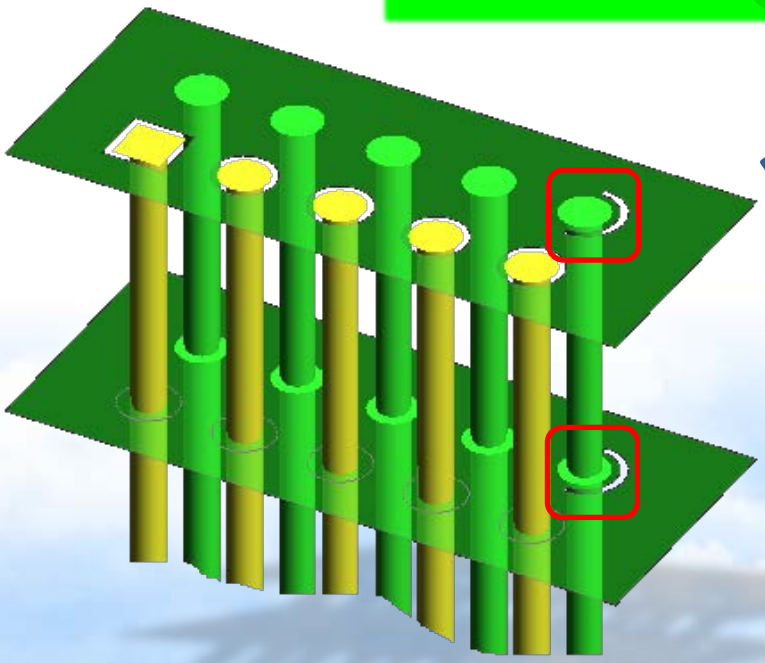
Via Current Plot



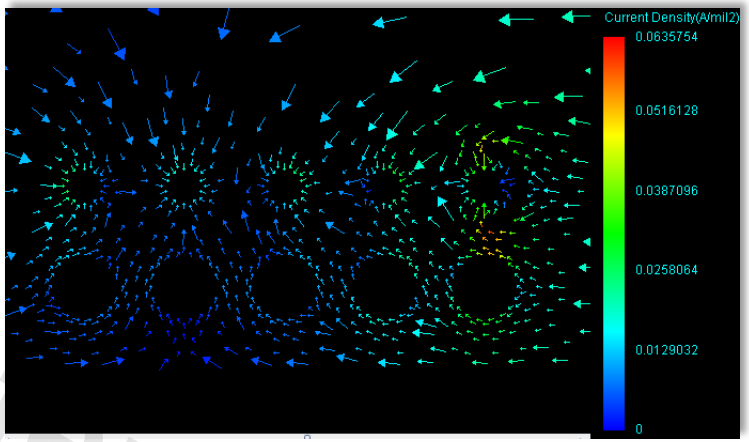
Via Current Simulation in PowerDC (2/2)

✓ Cut the shape to change path resistance for via current balancing purpose.

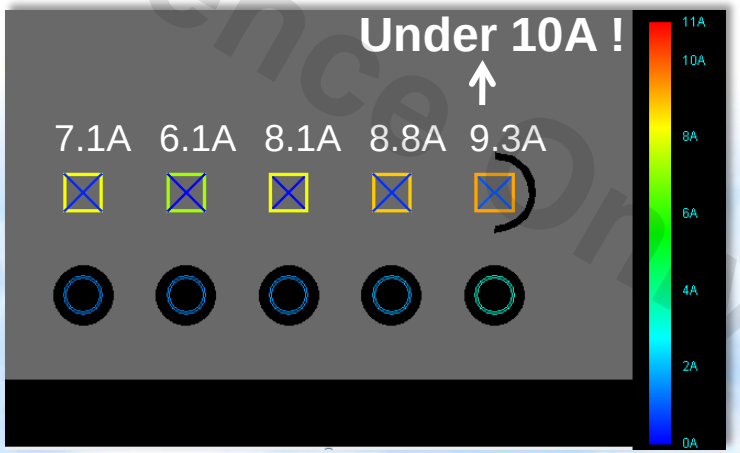




Current Vector & Density Plot

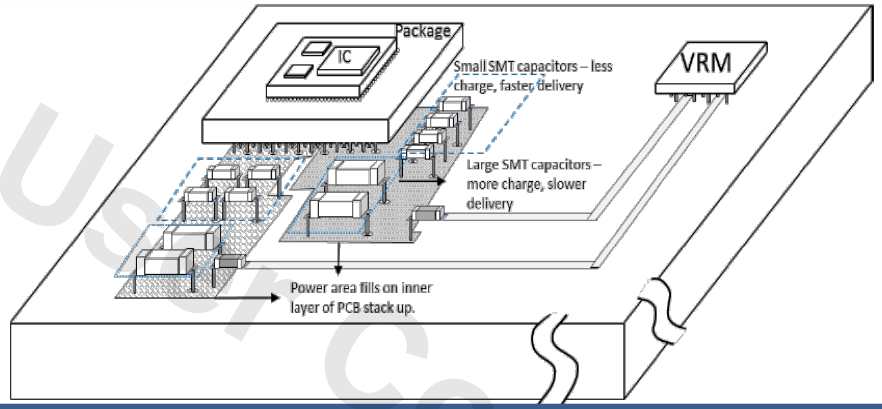


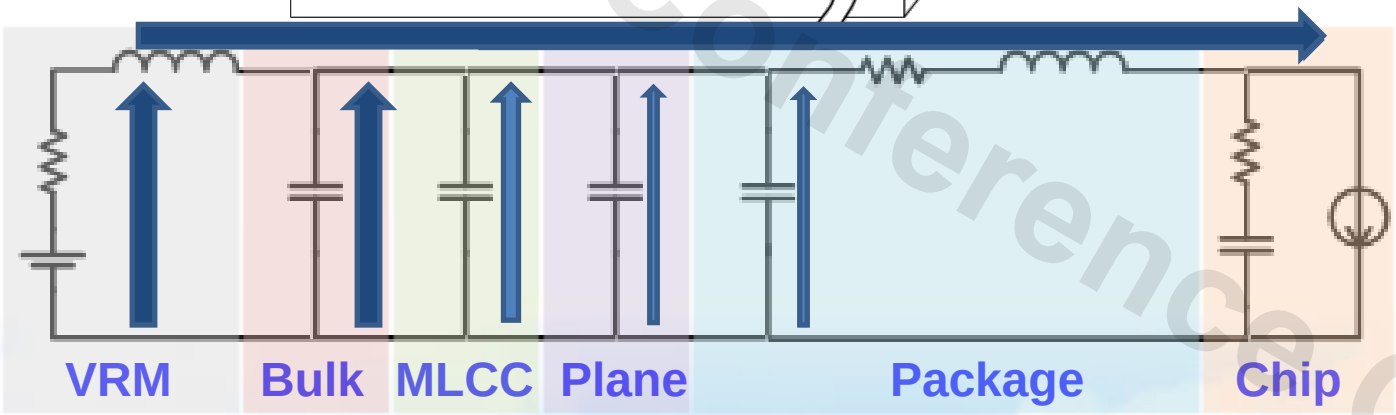
Via Current Plot

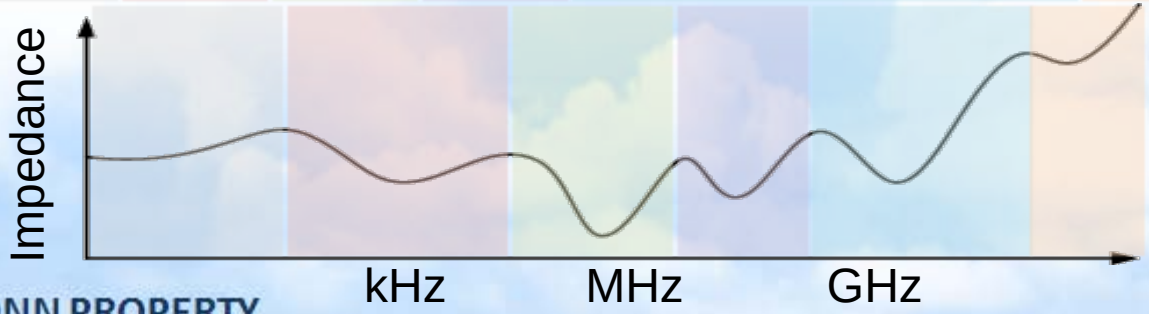


PDN AC Analysis

Power Delivery Network

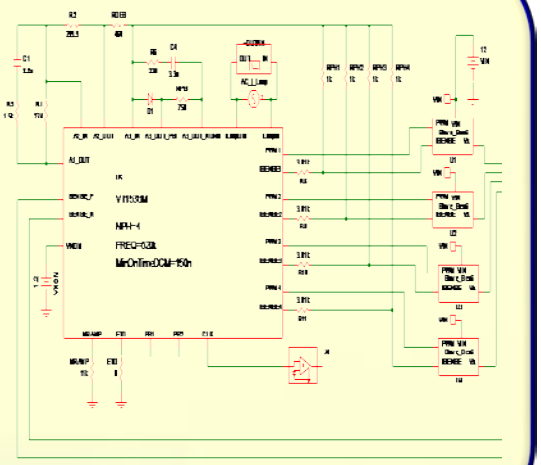




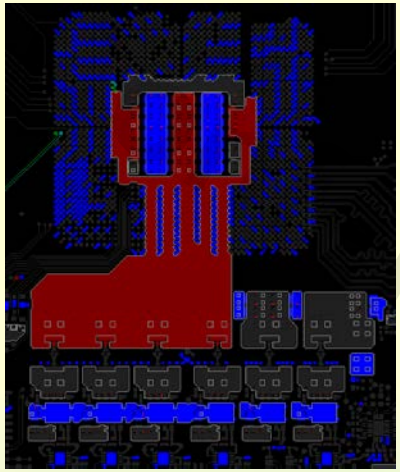


Transient Simulation

VR Model



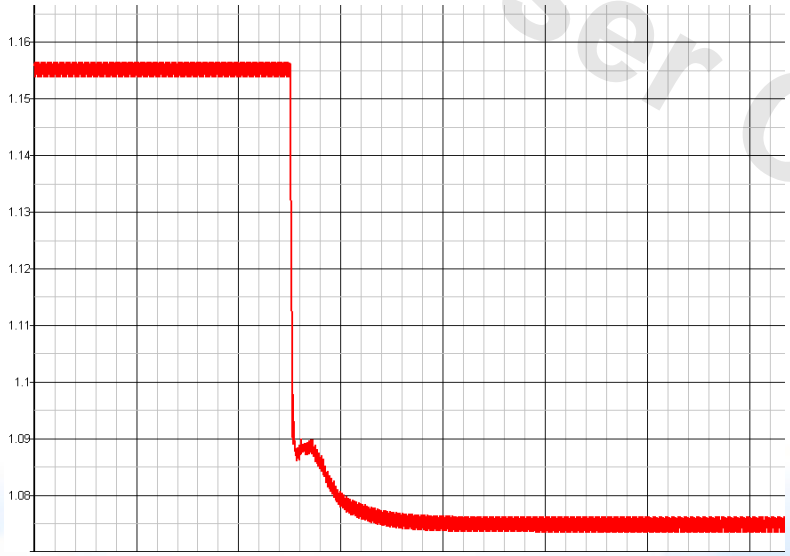
PDN extract by PowerSI



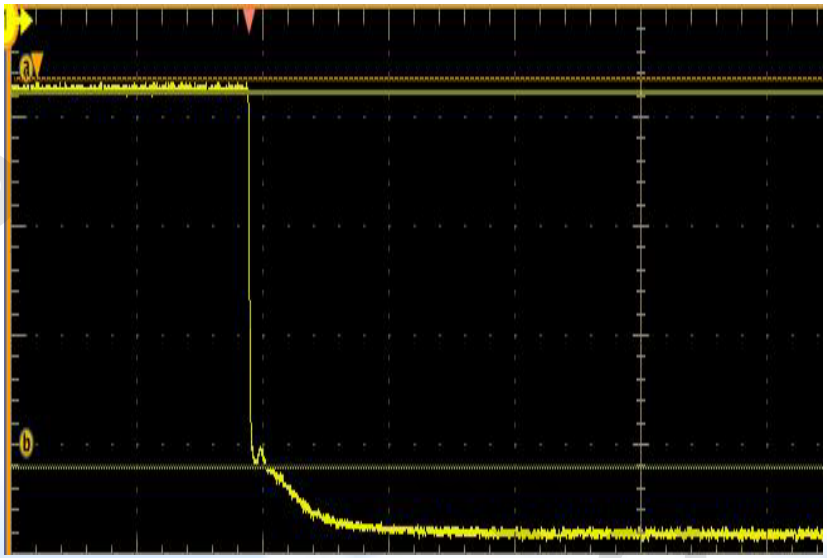
Load

Transient Voltage Correlation

Simulation



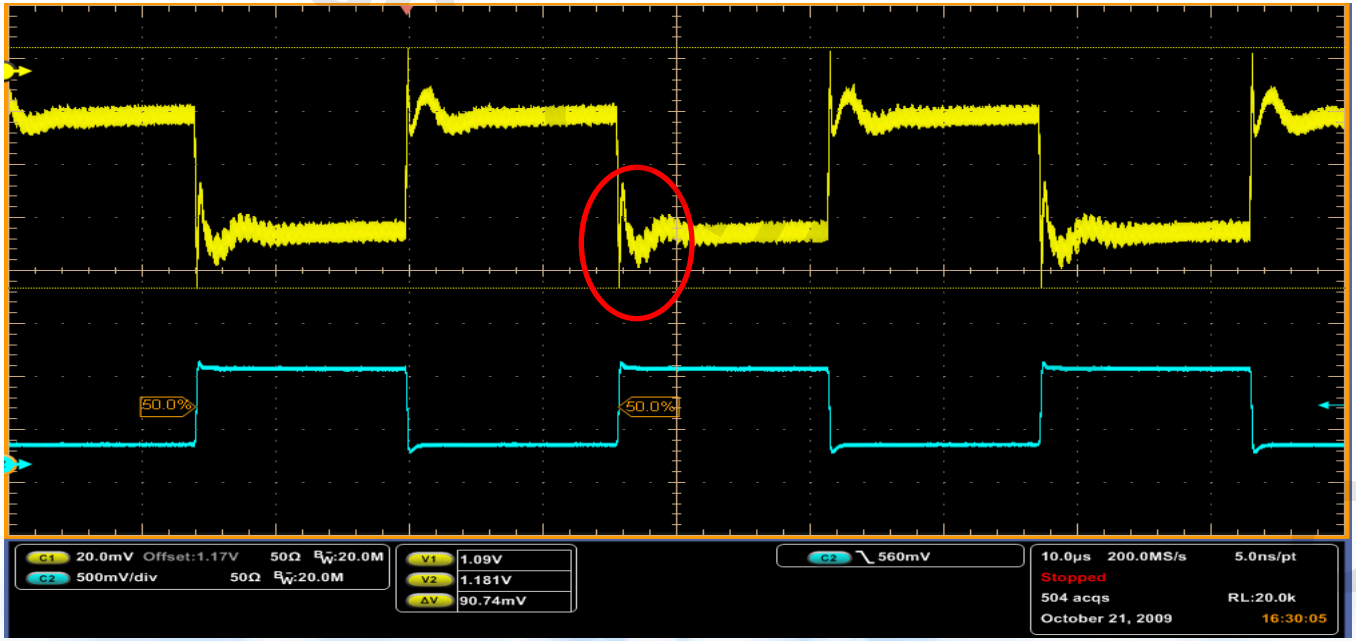
Measurement



	Measurement Value	Simulation Value	Difference
1st Voltage Spike	1.086V	1.0863V	0.3mV

Measurement Fail Issue

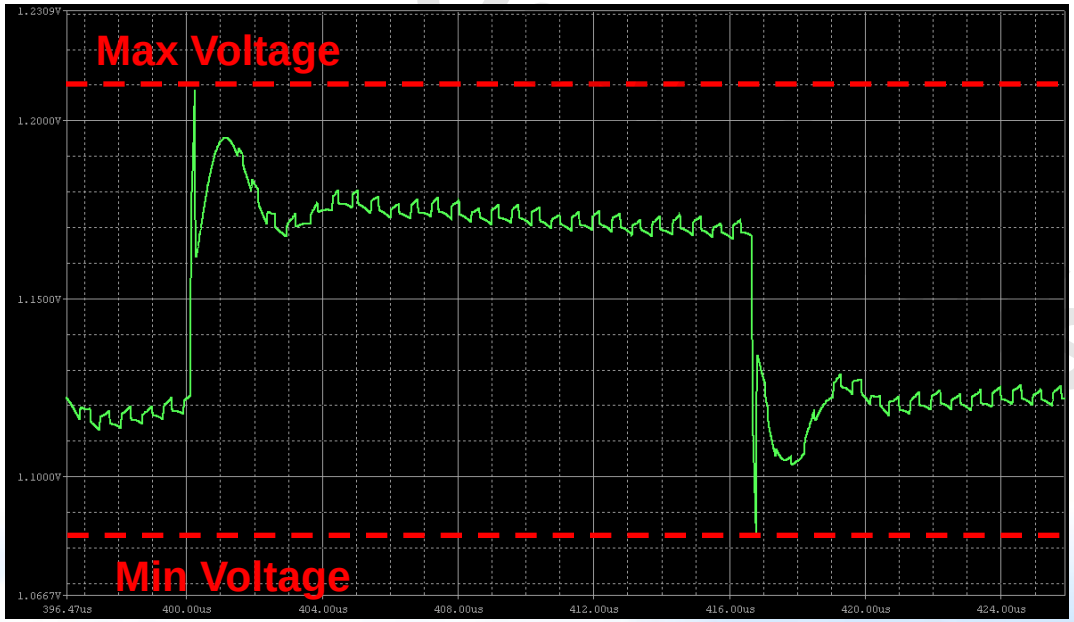
- The min voltage fail to meet specification.



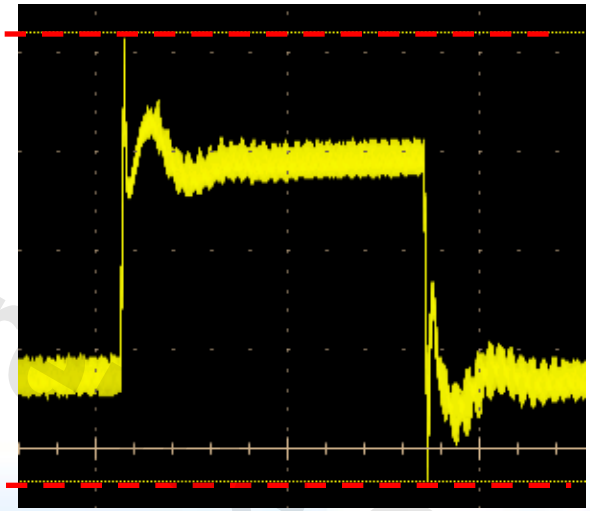
Transient Correlation - Original

- Using PowerSI to extract PDN model to get transient waveform.

Simulation Results



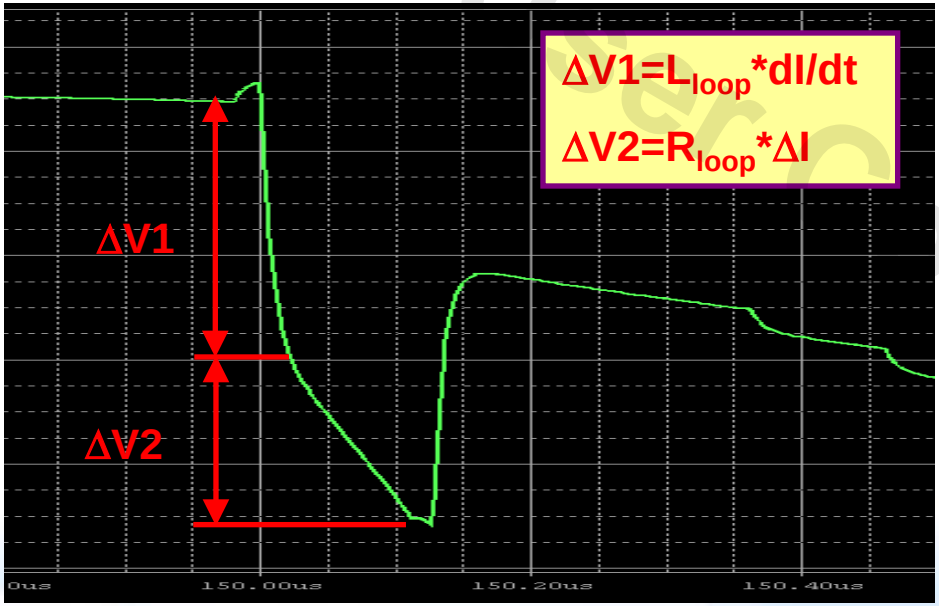
Measurement Results



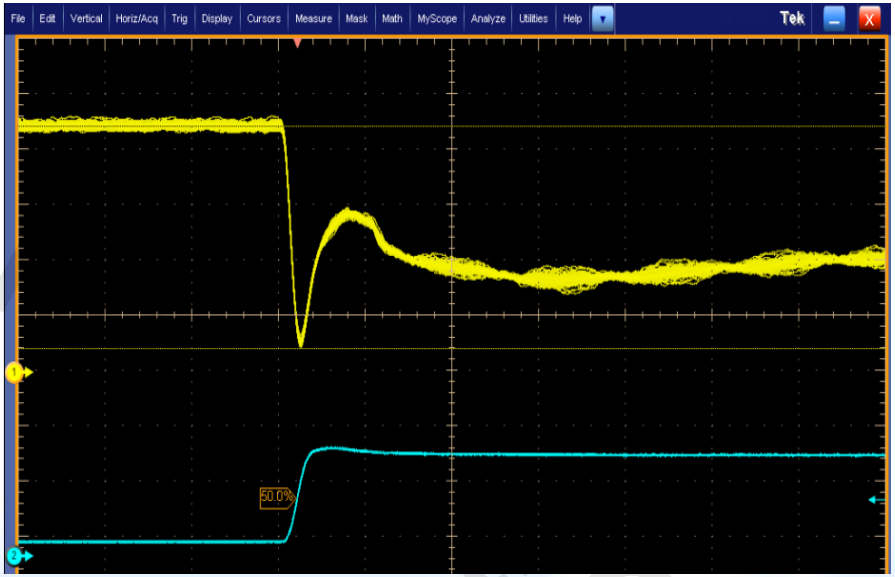
	Simulation	Measurement
Min Voltage (V)	1.089	1.090

Failure Issue Analysis

Simulation



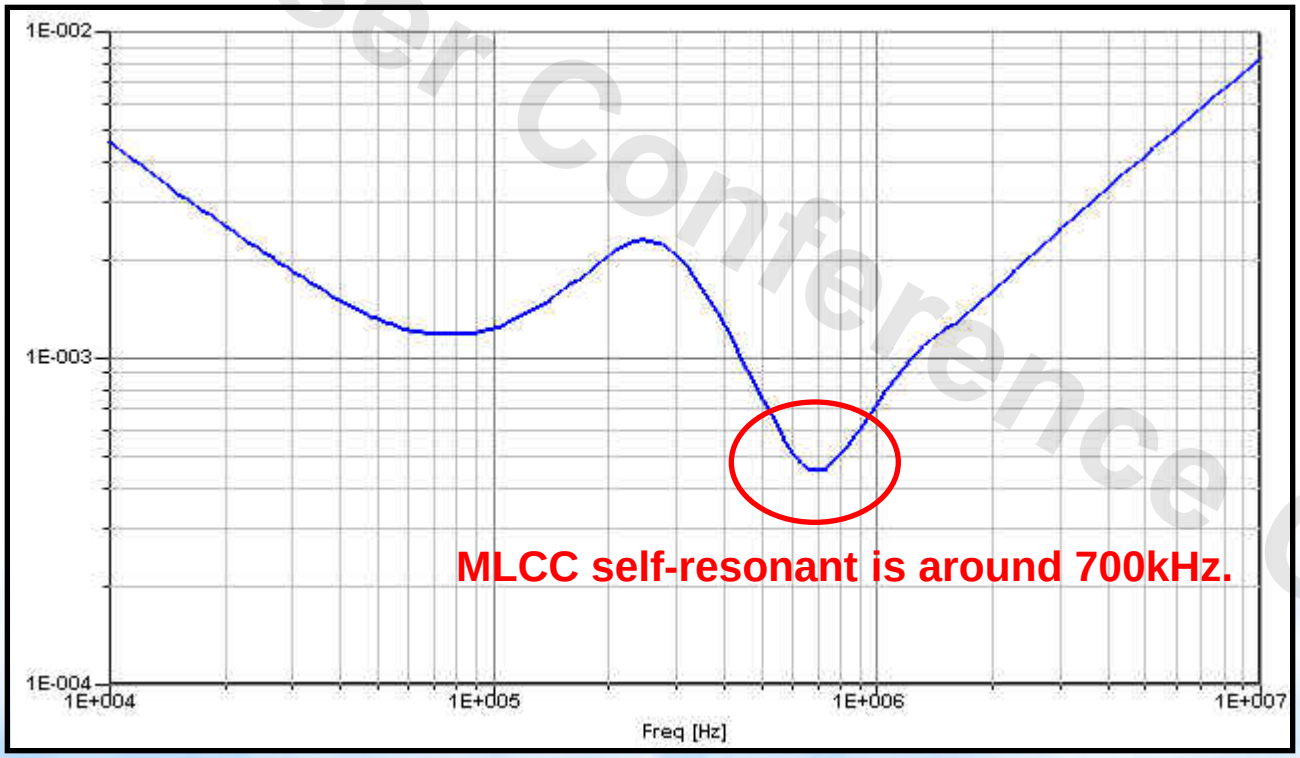
Measurement



◆ It can be found that the parasitic loop inductance dominates most of the droop. Thus it is necessary to inspect the loop inductance of board file.

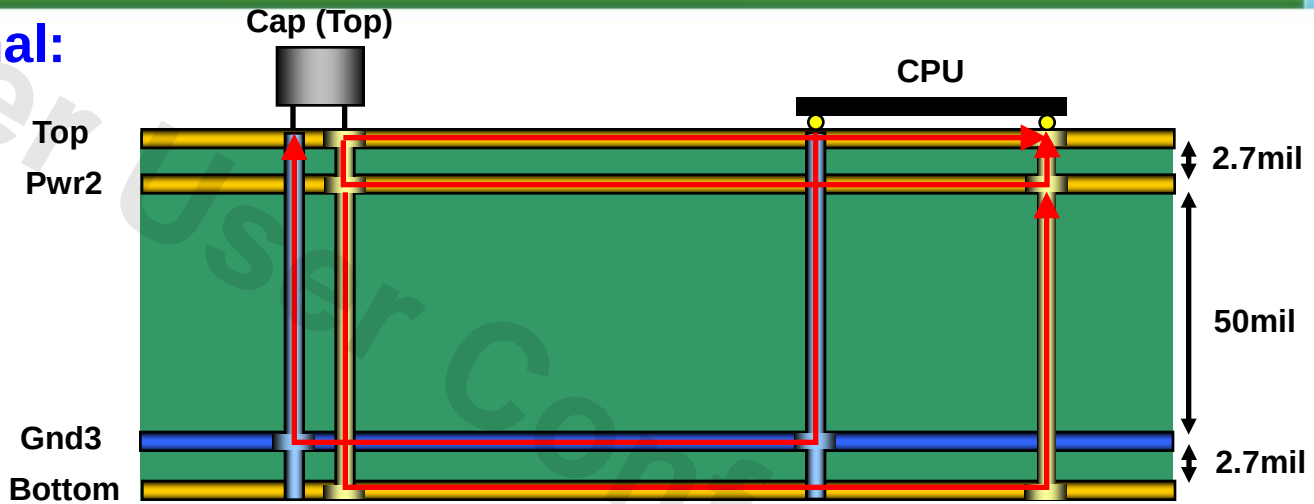
Impedance Analysis in PowerSI

◆ The original 22uF MLCC self-resonant frequency is 2.36MHz, but now it moves to 700kHz.



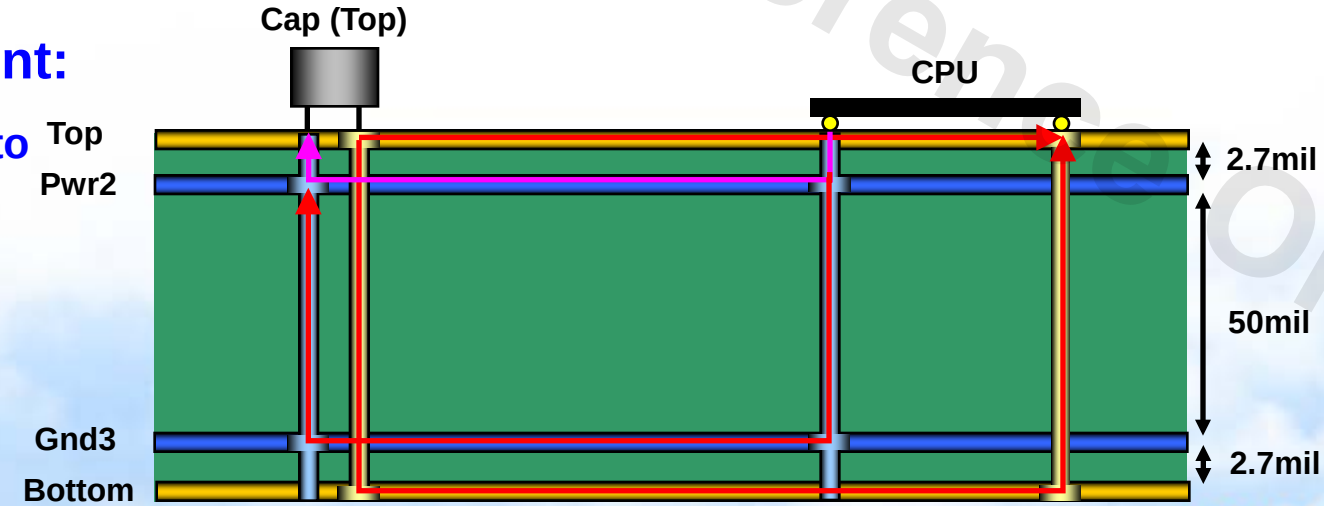
Current Loop Analysis

Original:

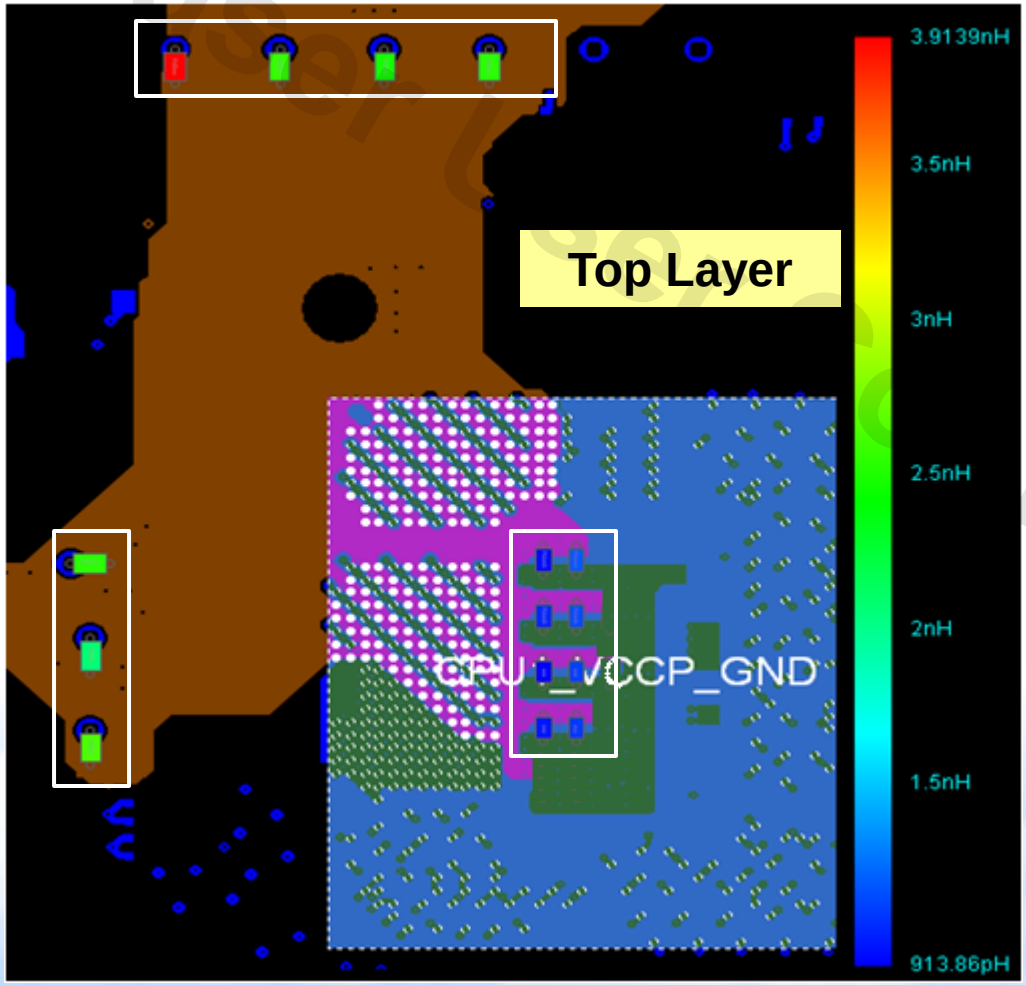


Improvement:

Change pwr2 to GND plane



Loop Inductance Analysis in OPI



Lacation				
Original Loop Inductance (nH)				
Improvement Loop Inductance (nH)				
PCE11	PCE12	PCE13	PCE14	
3.914	2.569	2.474	2.538	
1.291	0.976	0.888	1.026	

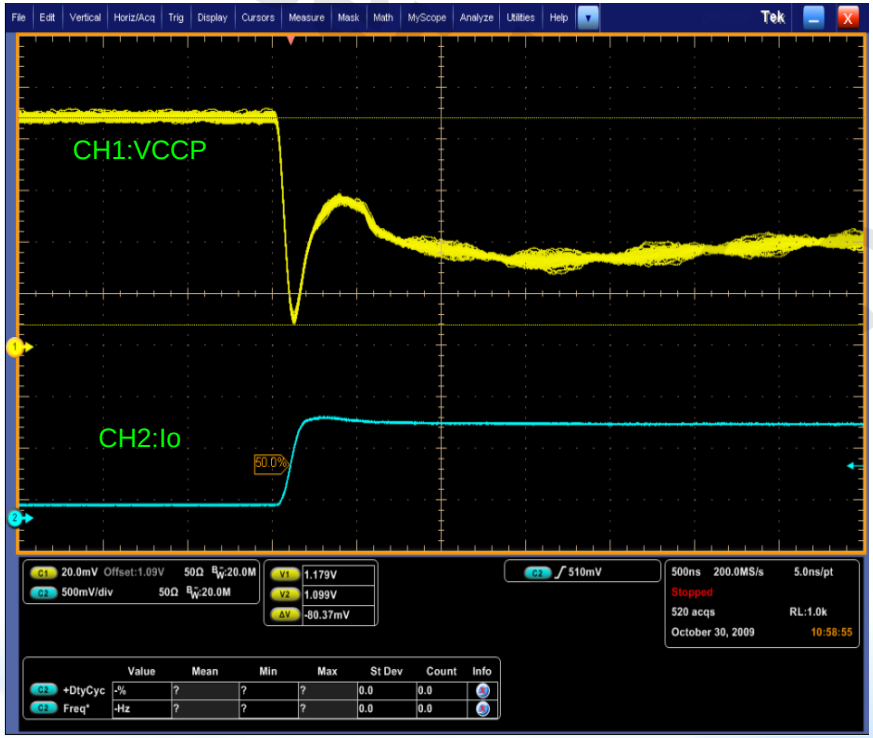
PCE18
2.541
0.878
PCE21
2.071
0.762
PCE23
2.640
1.148

PC110	PC111
0.944	1.176
0.542	0.868
PC118	PC119
1.030	1.137
0.717	1.130
PC129	PC130
0.914	1.104
0.690	0.966
PC139	PC140
0.981	1.084
0.884	1.047

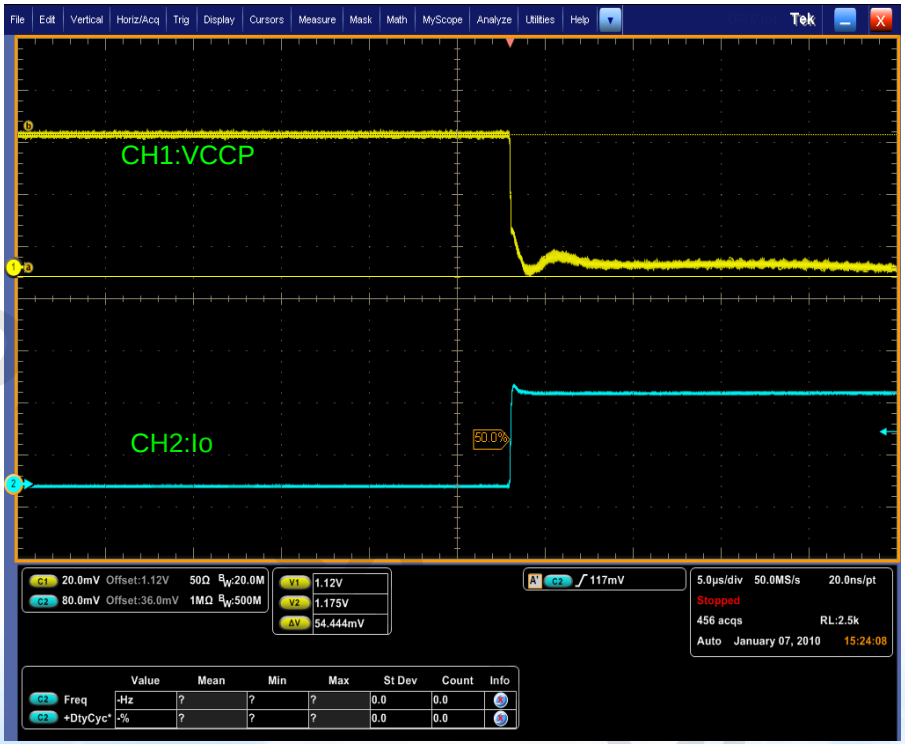
- For overall loop inductance, improvement case is better than original.

Measurement

Original Layout



After Modifying Layout



Spec. = 70mV	Original Layout	Modified Layout
Voltage Droop (mV)	80.32	54.44
Improvement	△V = 80.32 – 54.44 = 25.88 mV	

Summary

- Simulation tools can..
  - help designer to ensure design quality
  - predict validation results and has good correlation
  - verify designer's thought and find the best solution
  - more..

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THANK YOU

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