Cadence/Sigrity Stage 2
Single-Stop SI/PI Solution for Chip-Package-Board

An-Yu Kuo, PhD, Engineering Group Director, Sigrity R&D US
CDNLive
August 2014

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Agenda

- Leading-edge analysis technology integrated with Allegro
- Industry-renowned workflow
- Complete SI/PI/EMI solutions

- ✓ Hybrid solver
- ✓ 3D EM field solver
- ✓ 3D thermal solver
- ✓ 3D adaptive meshing
- ✓ Impulse response generator
- ✓ Fast channel simulation
- ✓ Parallel computing
- ✓ Transistor-to-behavior model generator
- ✓ S-parameter → SPICE macro model
- ✓ Multi-physics simulation
- ✓ Thermal-RC extraction
- ✓ ...

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Leading-edge analysis technology integrated with Allegro

Hybrid solver

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US005504423A

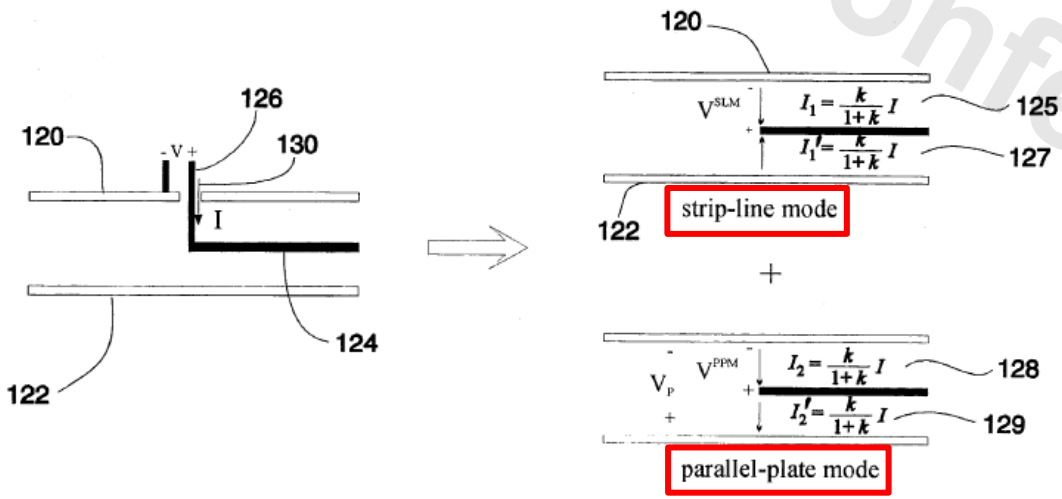
United States Patent [19]

Fang

[11] **Patent Number: 5,504,423**

[45] **Date of Patent: Apr. 2, 1996**

METHOD FOR MODELING INTERACTIONS IN MULTILAYERED ELECTRONIC PACKAGING STRUCTURES



- The patented mode decomposition algorithm allows users to solve large package and board designs with good accuracy and performance
- Good for both time- and frequency- domain simulations

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Leading-edge analysis technology integrated with Allegro

3D EM field solvers

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Full-Wave (FW)

$$\nabla \times \vec{E} = -j\omega\mu\vec{H}$$

$$\nabla \times \vec{H} = j\omega\varepsilon\vec{E} + \vec{J}$$

$$\nabla \cdot \left(\varepsilon\vec{E}\right) = \rho$$

$$\nabla \cdot \left(\mu\vec{H}\right) = 0$$

Quasi-Static (QS)

$$\nabla \times \vec{E} = -j\omega\mu\vec{H}$$

$$\nabla \times \vec{H} = \vec{J}$$

$$\nabla \cdot \left(\varepsilon\vec{E}\right) = \rho$$

$$\nabla \cdot \left(\mu\vec{H}\right) = 0$$

Static (S)

$$\nabla \times \vec{E} = 0$$

$$\nabla \times \vec{H} = \vec{J}$$

$$\nabla \cdot \left(\varepsilon\vec{E}\right) = \rho$$

$$\nabla \cdot \left(\mu\vec{H}\right) = 0$$

S **RLGC** **RC**

Large **ELECTRICALLY** **Small**

- Explicit FEM solvers for FW, QS, and S for different application needs
- Low-frequency stabilizer in FW engine
- Latest Krylov model order reduction for fast and accurate frequency sweep
- Super memory-efficient matrix solver
- Latest multi-grid technologies to handle huge models

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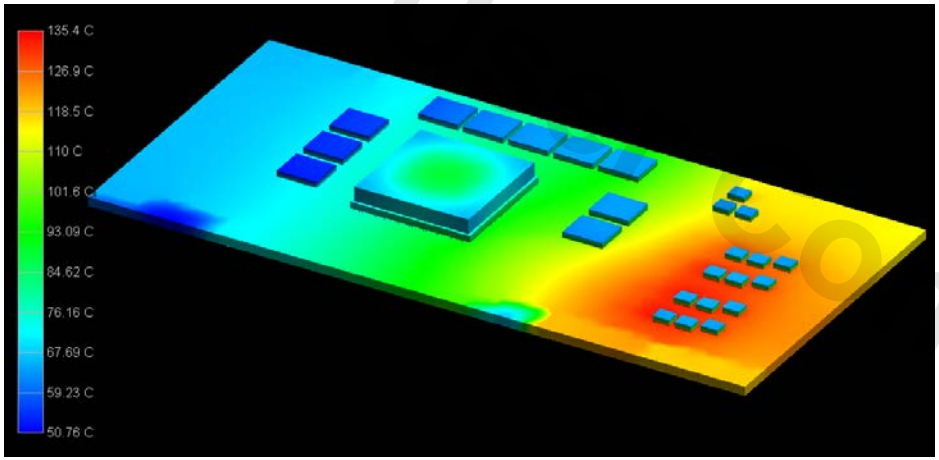
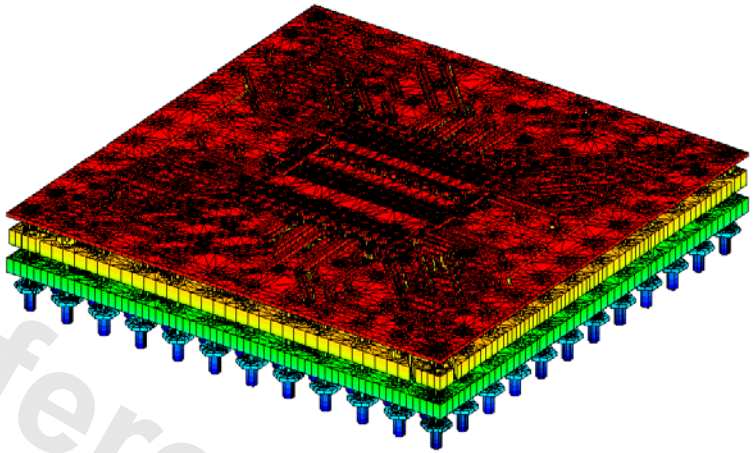
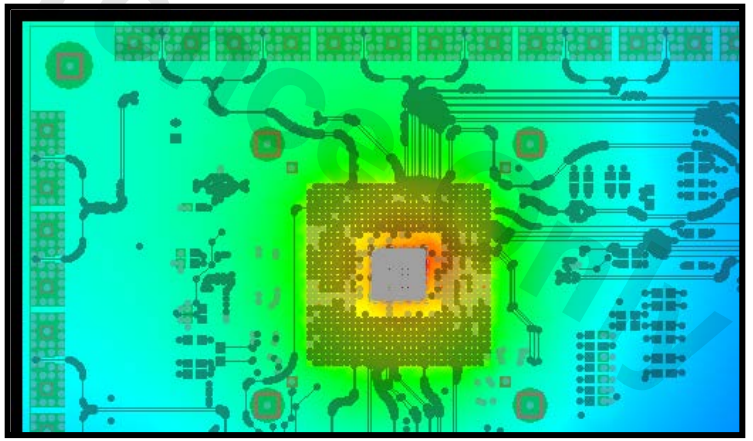
Leading-edge analysis technology integrated with Allegro

3D thermal solver

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right)+Q=\rho c \frac{\partial T}{\partial t}$$







- Steady-state and transient heat conduction with convection and radiation BCs
- Finite element method with adaptive meshing, model order reduction, and multi-grid method solver

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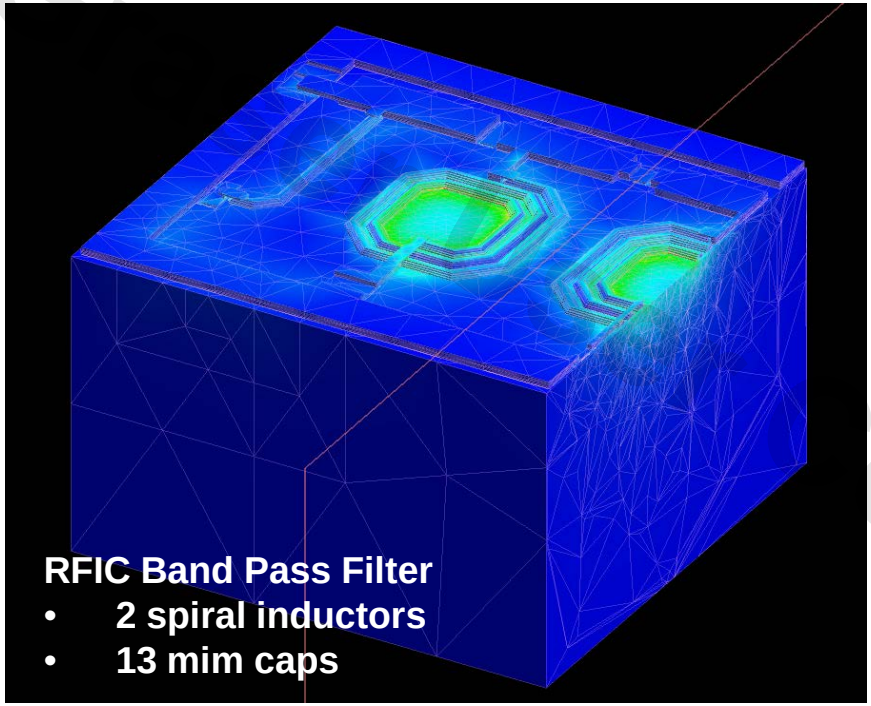
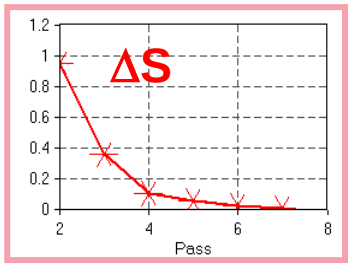
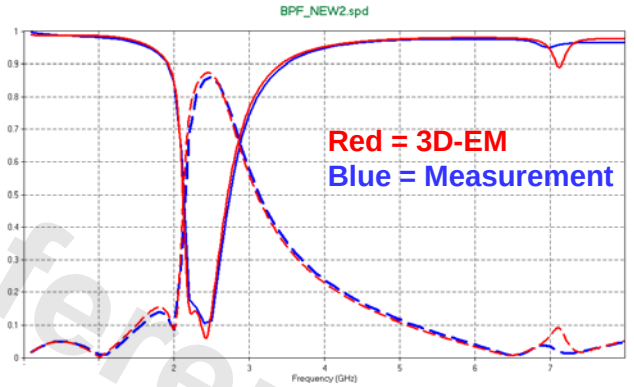
Leading-edge analysis technology integrated with Allegro

3D adaptive meshing for consistent accuracy

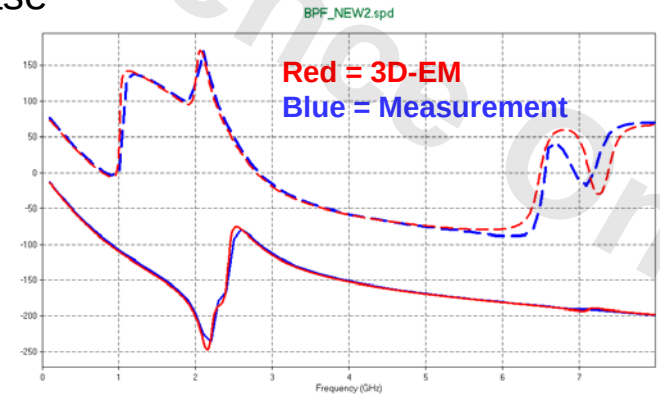




Magnitude



Phase



- Refine mesh based on solutions from previous mesh
- Elements with higher solution errors are refined
- Used in EM and thermal solvers

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Leading-edge analysis technology integrated with Allegro

Patented impulse response generation

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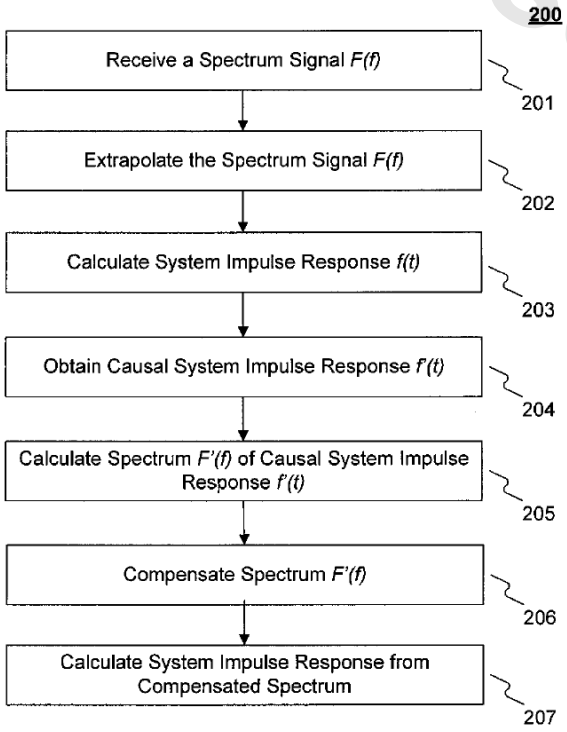
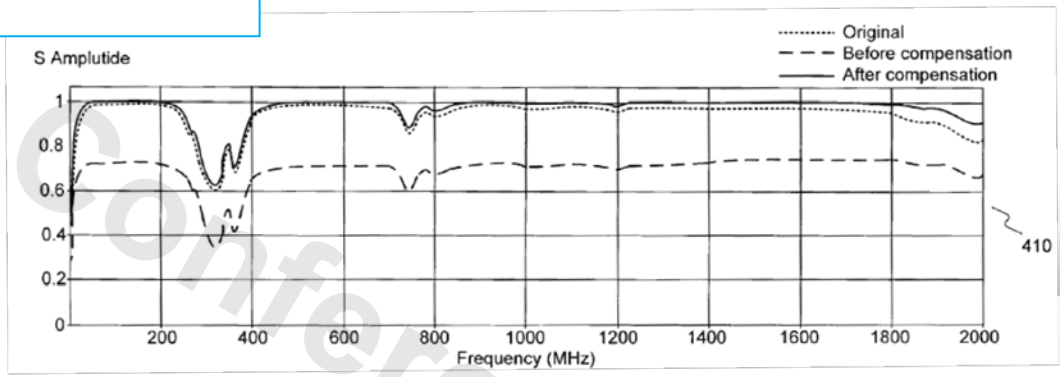
US008694568B2

(12) **United States Patent**
Li et al.

(10) **Patent No.: US 8,694,568 B2**
(45) **Date of Patent: Apr. 8, 2014**

(54) **METHOD FOR CALCULATING CAUSAL IMPULSE RESPONSE FROM A BAND-LIMITED SPECTRUM**





- The patented method generates a passive and casual time-domain impulse response from band-limited spectrum data
- Spectrum of the time-domain impulse response is almost identical to the original data
- This method is in time-domain simulations of S-parameters in Sigrity® tools

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Leading-edge analysis technology integrated with Allegro

Fast channel simulation for DDR4

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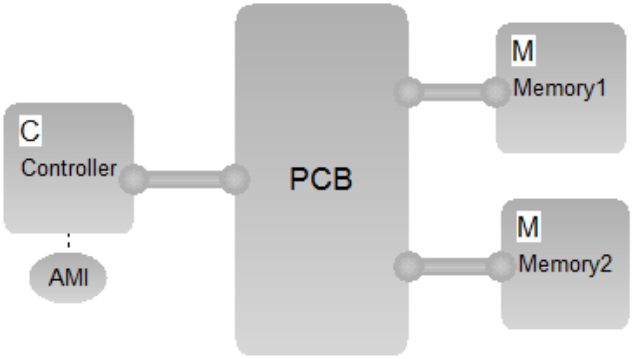
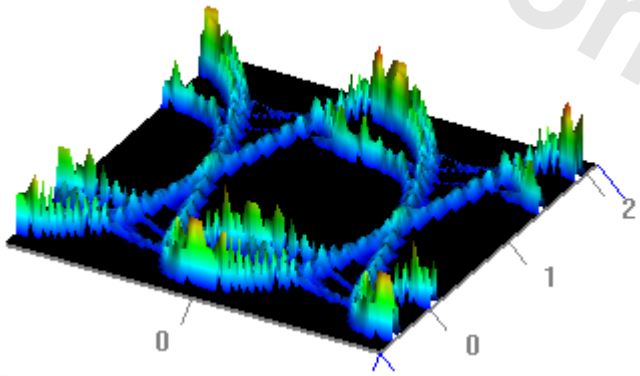
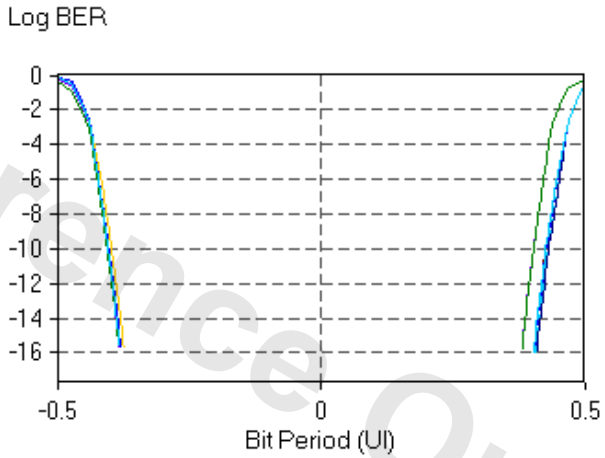
- Fast SSN channel characterization
  - Ability to run millions of bits
- Jitter and noise injection
- AMI modeling for adaptive equalization
- Bathtub curve and eye generation
- DQ mask and BER measurement and report







4.2.2 Worst Case Summary

Measurement	Vcent_DQ (V)	DQ Compliance Mask	Min Jitter_margin (ps)	Min Noise_margin (mv)	|Max| tDQS2DQ (ps)	|Max| tDQS2DQ_BC (ps)	Max tDQ2DQ (ps)	Min VIHL_AC (mV)	Min TdIPW (ps)	Min SlewRate_Mask (V/ns)	Max SlewRate_Mask (V/ns)	Min SlewRate_AC_Swing (V/ns)	Max SlewRate_AC_Swing (V/ns)
Worst Value			134.923	166.916	-33.1392	6.60106	13.2021	469.832	396.02	3.20676	4.32314	3.05877	4.2416
Rx Signal (Waveform)			DQ6	DQ4	DQ7	DQ3	All Signals	DQ4	DQ6	DQ6	DQ4	DQ6	DQ4

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Leading-edge analysis technology integrated with Allegro

Parallel computing

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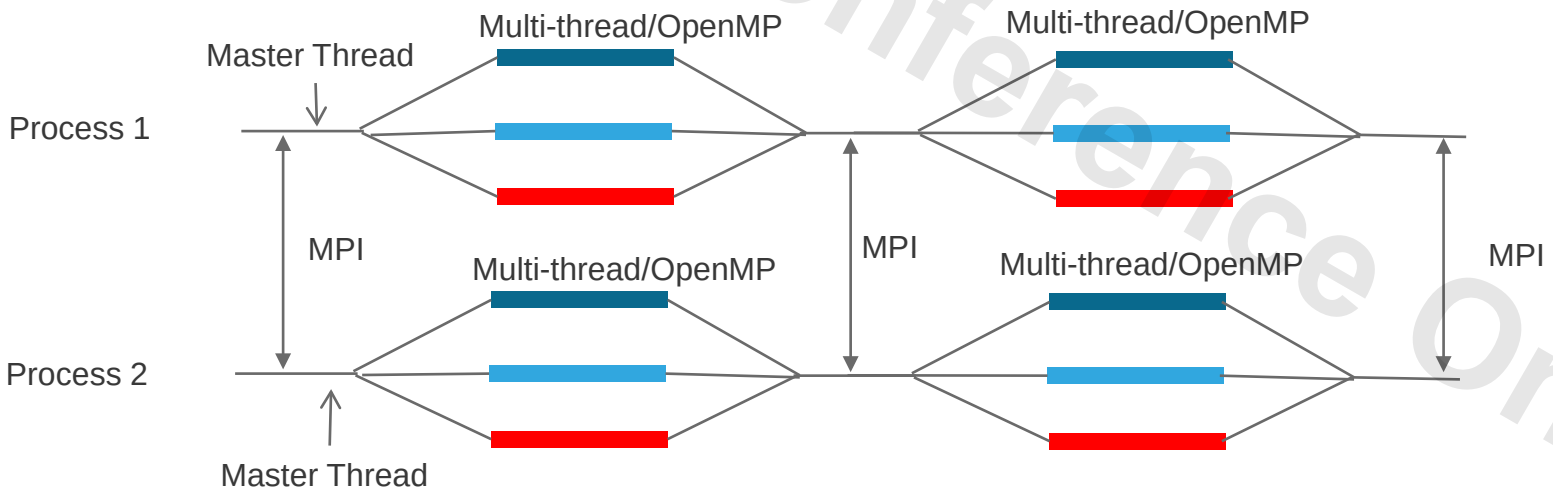
- **Threads model**
  - Multiple concurrent thread
  - OpenMP
- **Distributed**
  - Message Passing Interface (MPI)

- Distributed computing with MPI and OpenMP to leverage server farm capacity



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Leading-edge analysis technology integrated with Allegro

Transistor models → behavior model

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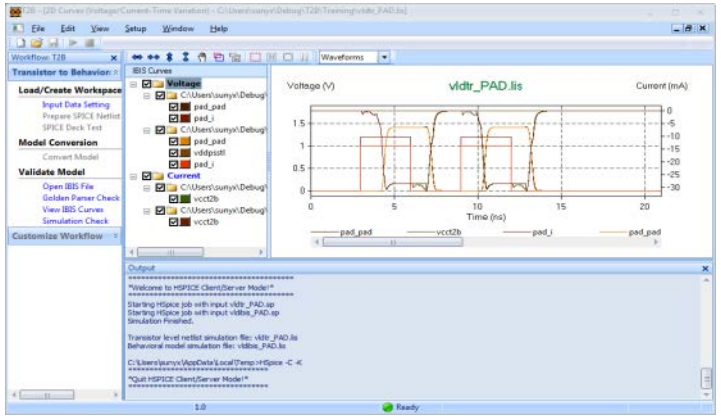
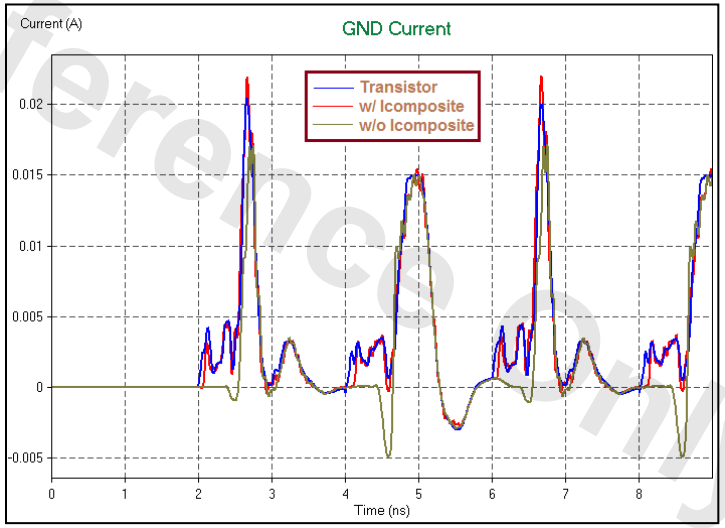
- Industry's most advanced tool for converting transistor models to power-aware IBIS
- Convenient GUI verifies conversion accuracy
- Simulation speed-up makes full bus simulations practical; this would otherwise take weeks
- Optional IBIS plus model provides additional level of accuracy



Built-in simulation check compares transistor to IBIS



Impact of pre-driver current

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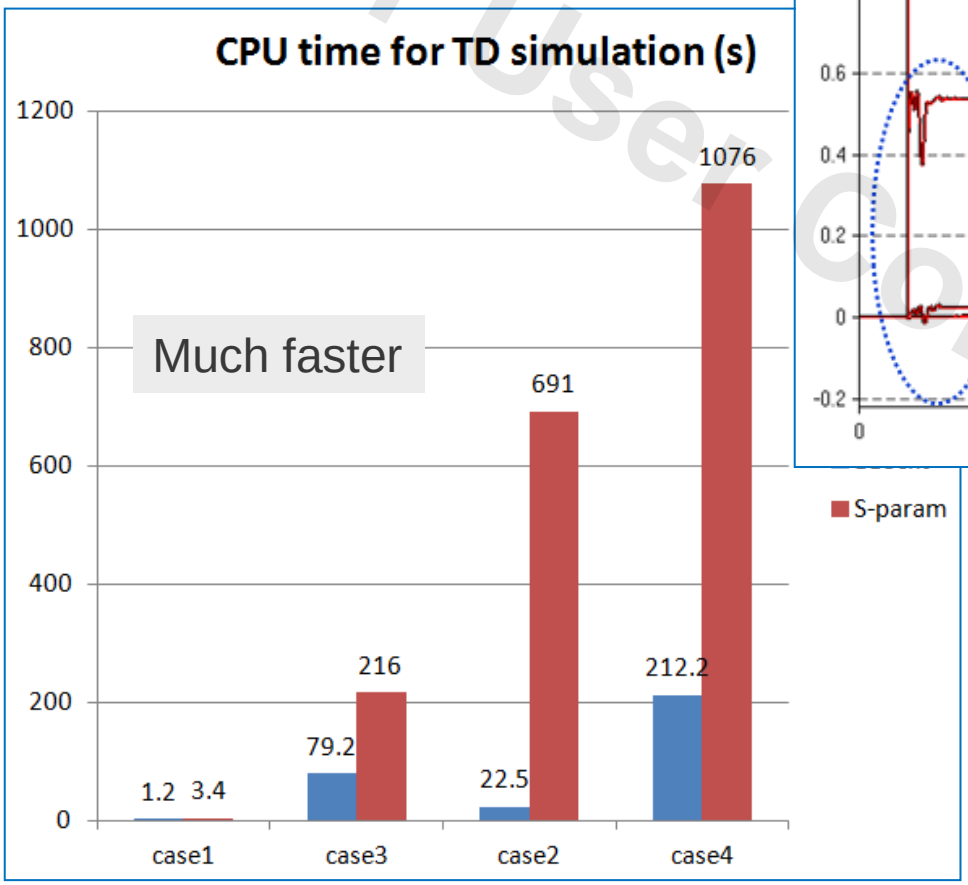
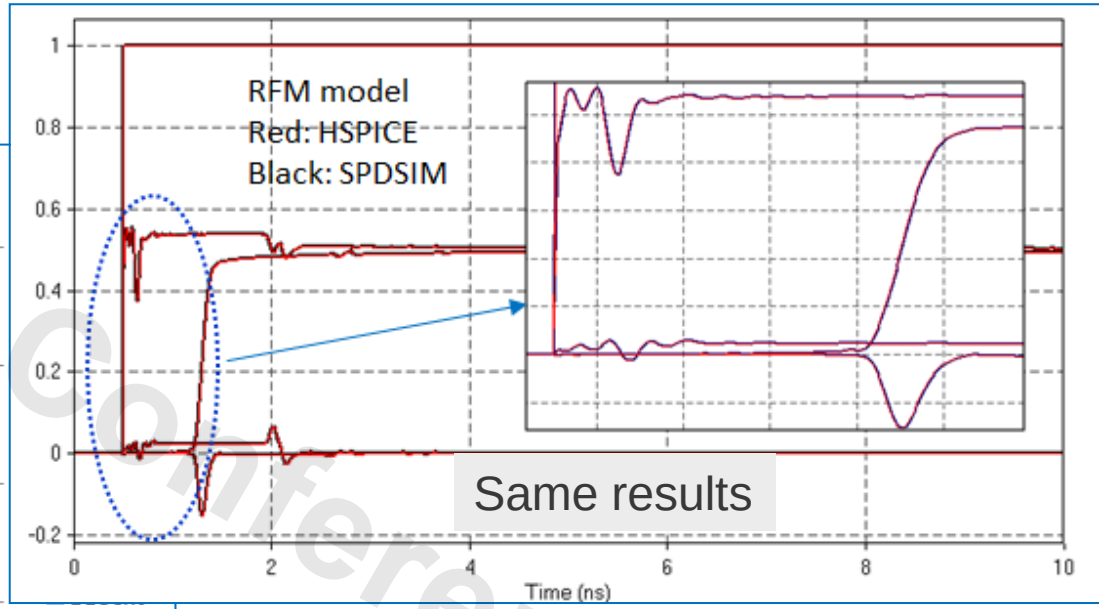
Leading-edge analysis technology integrated with Allegro

S-parameter → SPICE macro model





TD simulation using BBS circuit model runs faster

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Leading-edge analysis technology integrated with Allegro

Multi-physics simulations

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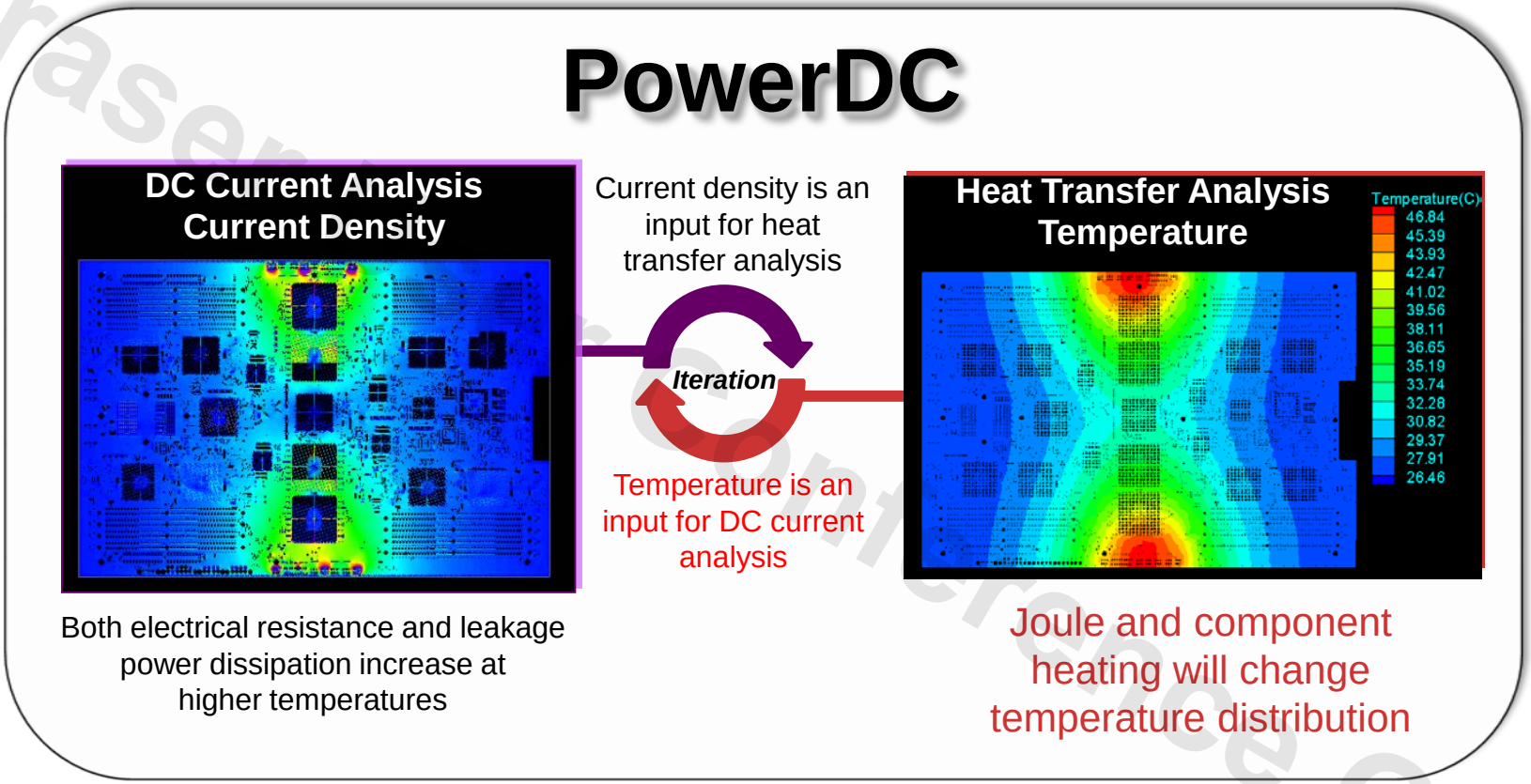

- The first integrated and automated electrical/thermal co-simulation tool to help designers meet the new design challenge

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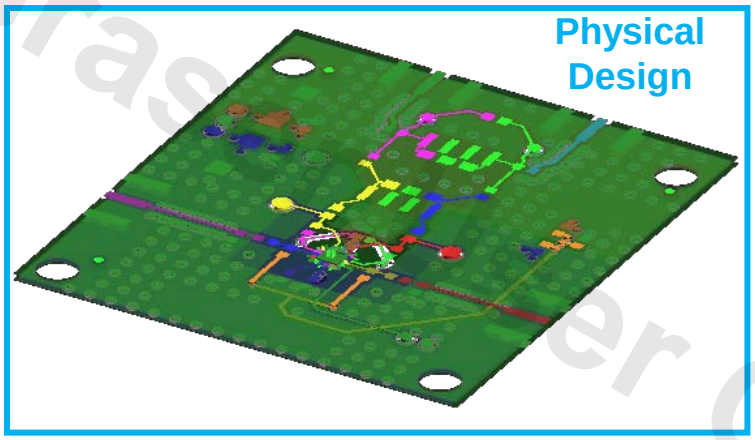
Leading-edge analysis technology integrated with Allegro

Thermal-RC extraction

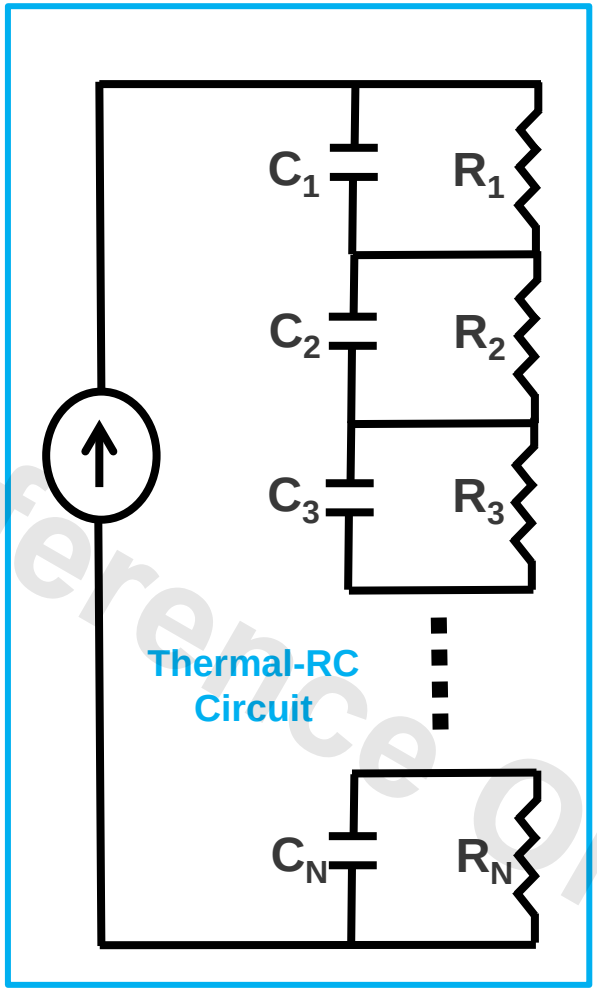


Finite Element Model

$$\nabla^T k \nabla T + Q = \rho c \frac{\partial T}{\partial t}$$

$$[K]\{T\} + [M]\frac{d\{T\}}{dt} = \{B\}$$

Patent Pending



- One-time thermal-RC extraction
- Multiple transient analyses with a circuit simulator

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Agenda

- Leading-edge analysis technology integrated with Allegro
- Industry-renowned workflow
- Complete SI/PI/EMI solutions

- ✓ Industry-leading workflows
- ✓ Direct interface with Allegro®/APD/SiP
- ✓ Many useful model setup wizards
- ✓ Many SI/PI utilities
- ✓ Automated signoff report generation
- ✓ …

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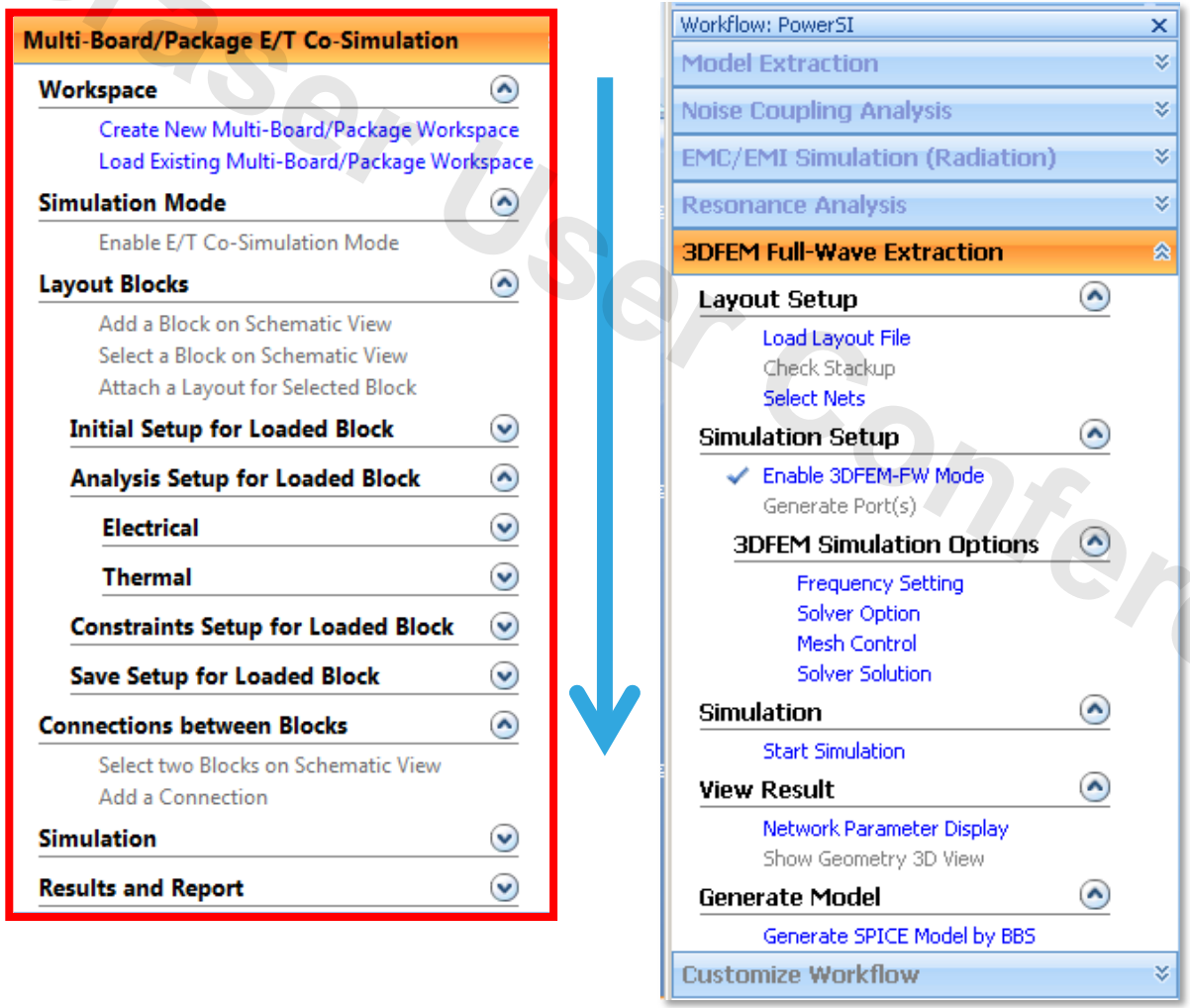
Meticulous implementation

Industry-leading workflows



- Various application-specific workflows for easy learning and usage

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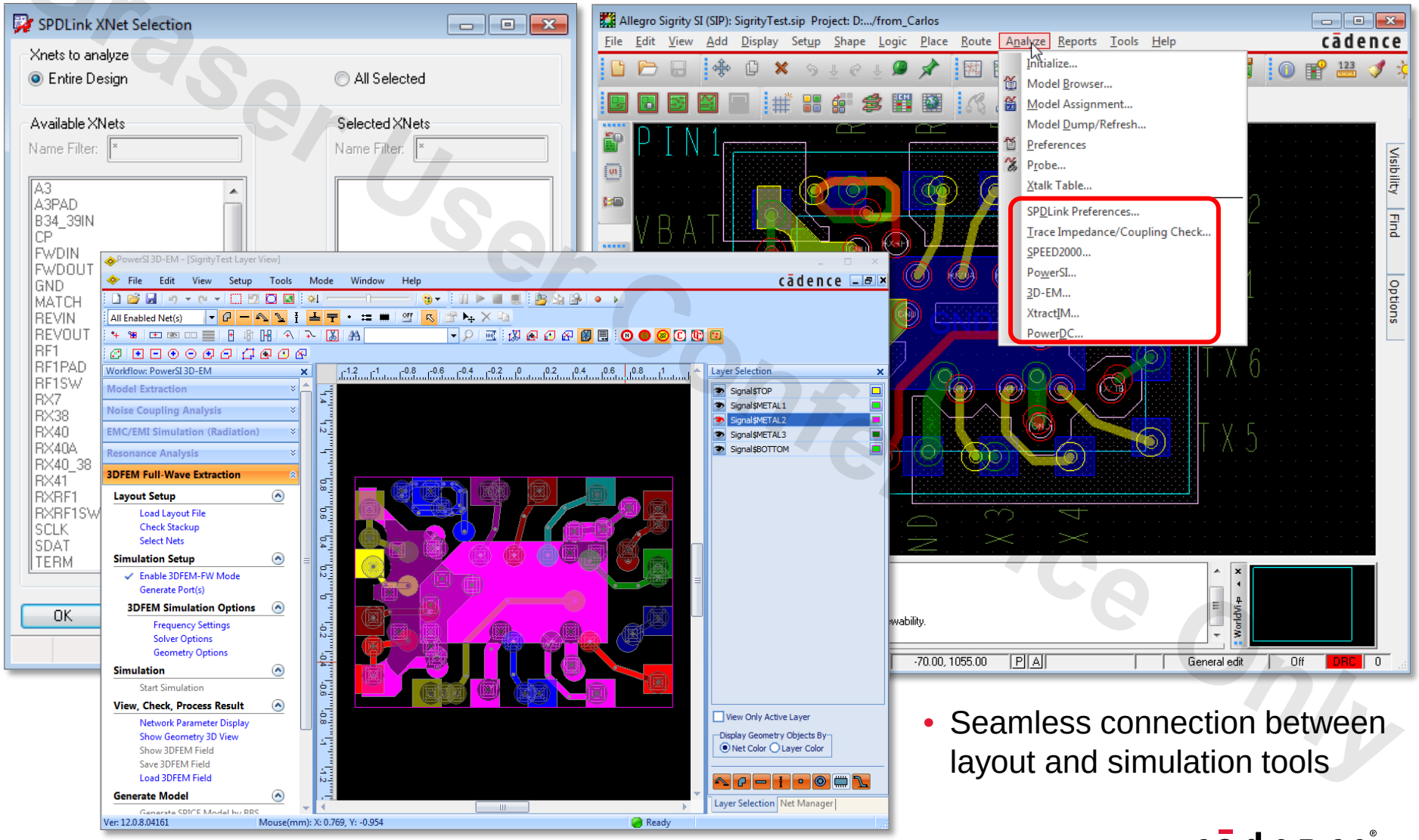
Meticulous implementation

Direct interface with Allegro/APD/SiP



- Seamless connection between layout and simulation tools

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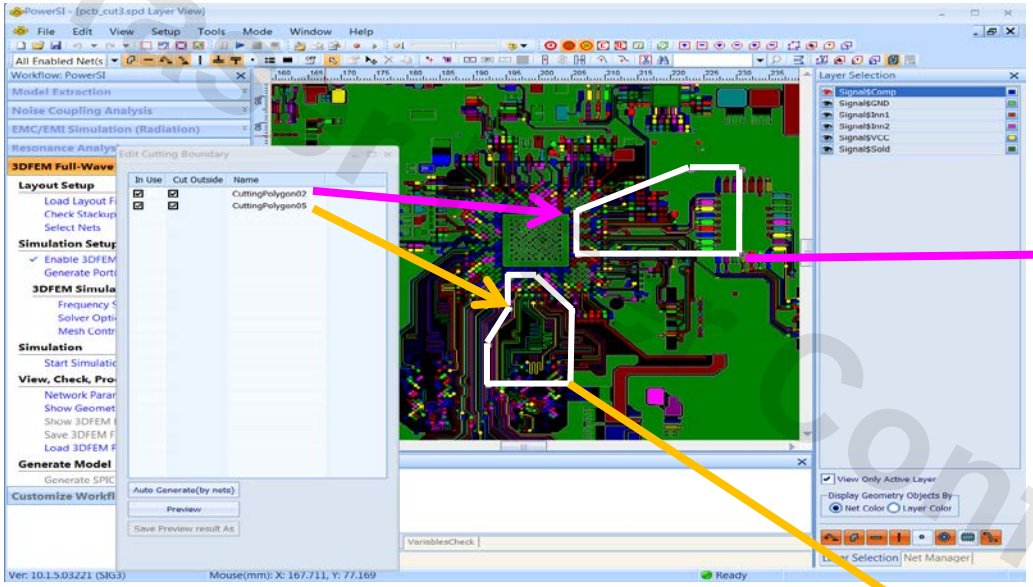
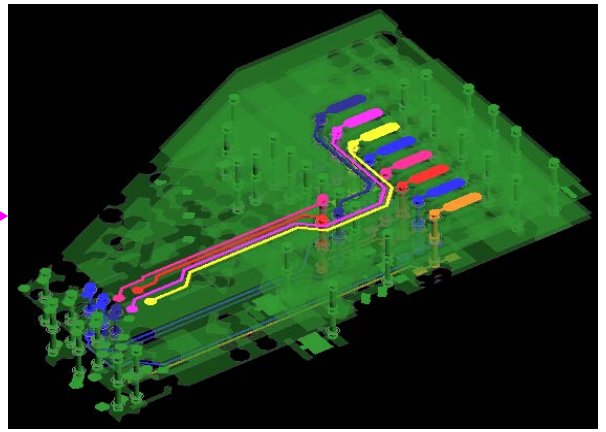
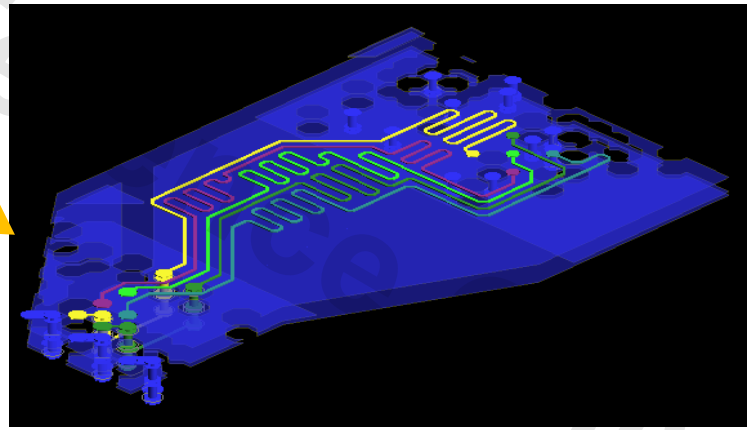
Meticulous implementation

Many useful model setup wizards



Geometry Cutting Wizard





- Port wizard for automated port setup
- Wizard for PCB fiber weaving and RFIC deep-trenched isolation patterns
- Sweeping manager for parametric sweep
- Automated model cutting by polygon
- Cut-stitch wizard for long signal lines
- VRM setup wizard
- **...**

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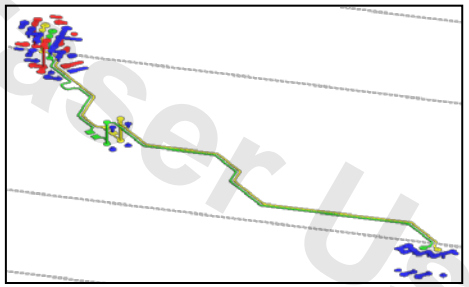
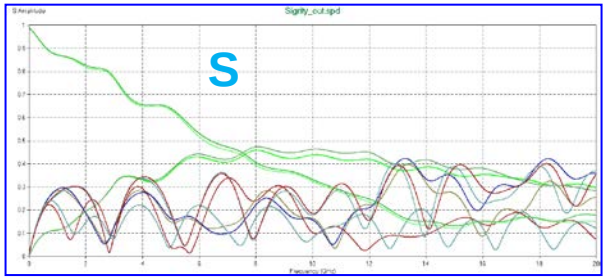
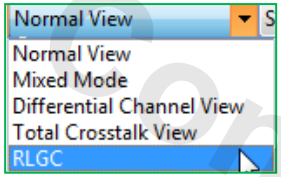
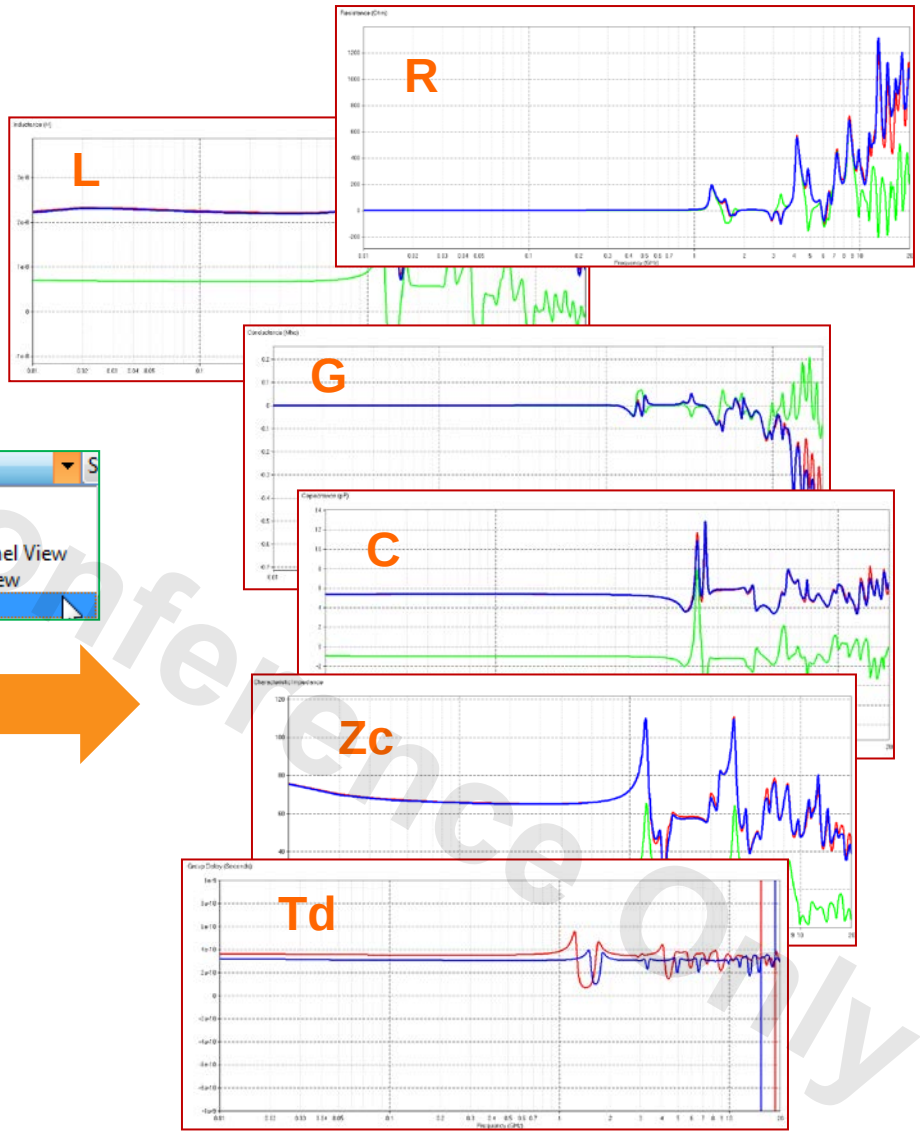
Meticulous implementation

Many useful SI/PI utilities









- S→RLGC
- S→TDR/TDT
- Cascading
- De-embedding
- …

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Meticulous implementation

Signoff report generation

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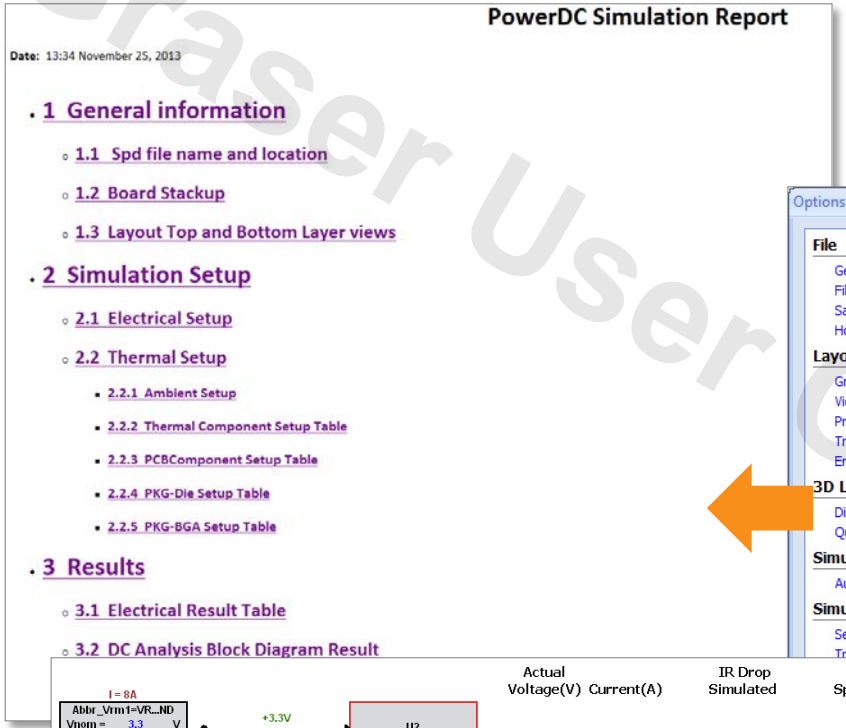
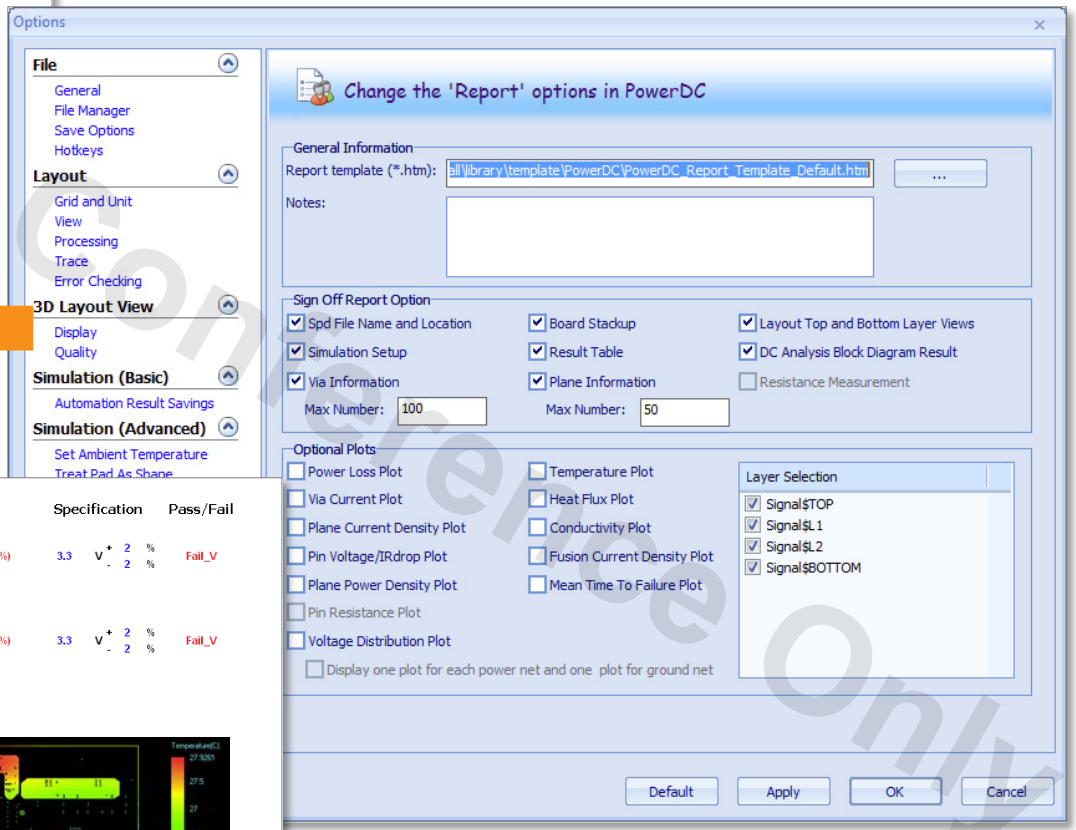
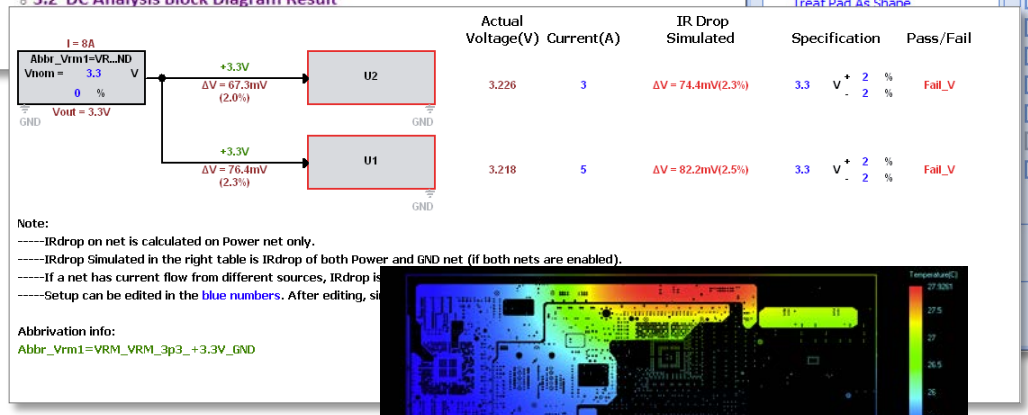
- Automated and configurable HTML report







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Agenda

- Leading-edge analysis technology integrated with Allegro
- Industry-renowned workflow
- Complete SI/PI/EMI solutions

- ✓ Layout checks
- ✓ Model-based high-speed bus simulation
- ✓ Layout-based time-domain simulation
- ✓ Layout-based frequency-domain simulation
- ✓ Decap placement optimization
- ✓ High-speed bus simulation
- ✓ Multi-board-package simulation
- ✓ *IOSSO*
- ✓ Chip-pkg-board co-simulation
- ✓ EMI/EMC simulation
- ✓ Electrical/thermal co-simulation
- ✓ Package thermal parameters extraction
- ✓ RFIC passive component extraction
- ✓ Different levels for different needs
- ✓ ….

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Complete solutions
Cover broad SI/PI/EMI needs

- Layout PDN design DC/AC check
  - DC check
  - AC check
- Layout SI check
  - Geometry-based physical check
  - Simulation-based electrical check
- PDN simulation
  - DC simulation and signoff
  - Electrical/thermal co-simulation
  - AC frequency domain simulation and optimization
  - Chip/PKG/PCB co-simulation
- Power-aware SI simulations
  - High-speed serial link simulation
  - Parallel bus simulation
  - Chip/PKG/board IOSSO co-simulation
- EMI simulation
  - Conductive EMI
  - Radiative EMI
  - EMC compliance check
- SI/PI/TI modeling
  - RFIC passive component extraction
  - Package thermal parameters extraction
  - Electrical/thermal
  - IBIS

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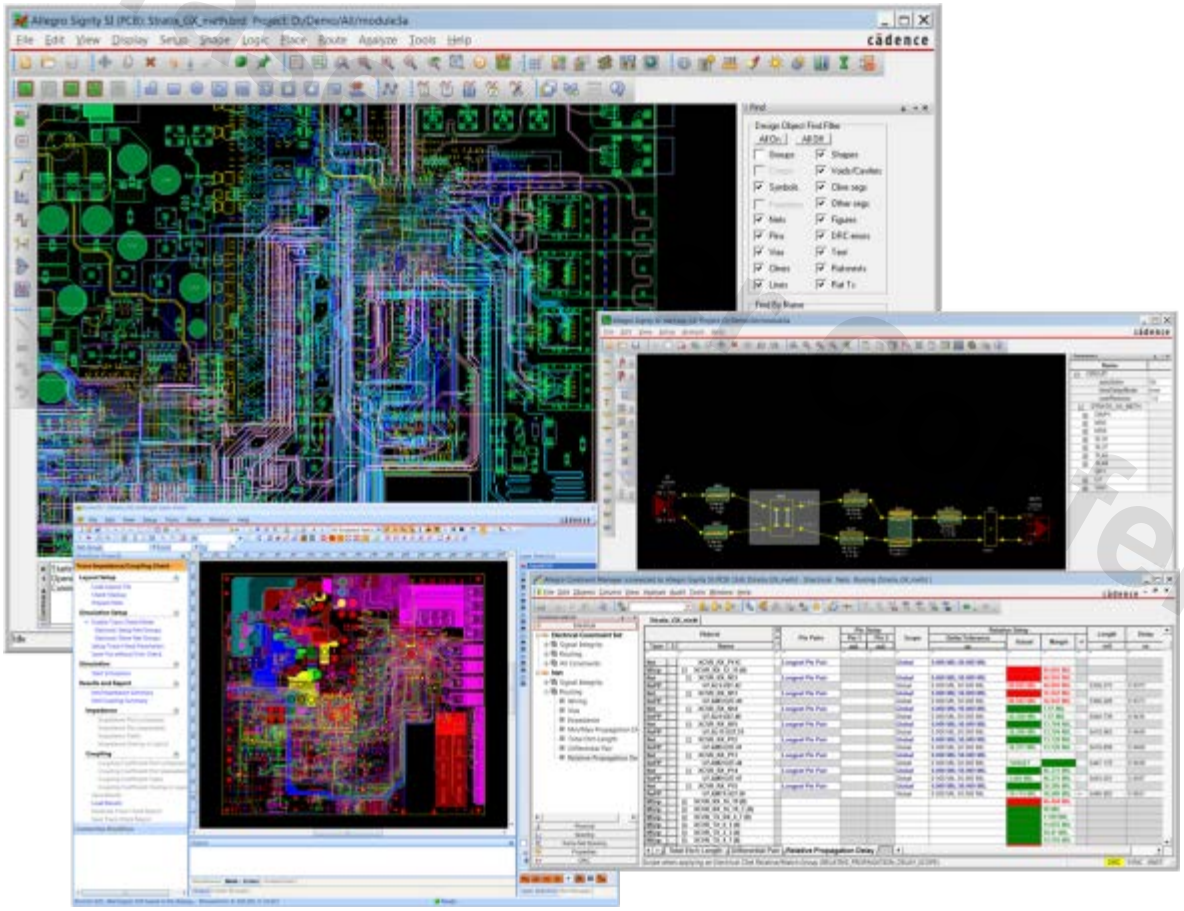
Allegro Sigrity SI and Allegro PCB Editor
Integrated high-speed design and analysis



Allegro Sigrity SI

No manual translation is required to analyze selected signals from the physical board or extract them into the SigXplorer module. Analysis results are reported in the same constraint manager used by Allegro PCB Editor. Coupled differential pairs and nets extended through discrete components (x-nets) are automatically identified, analyzed, and/or extracted.

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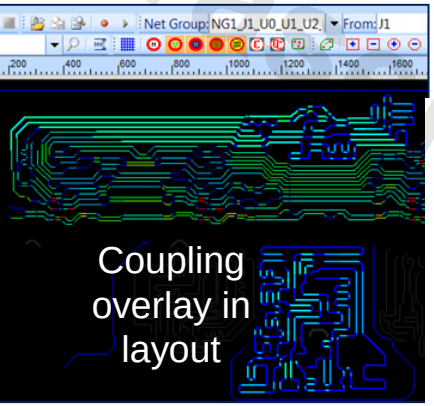
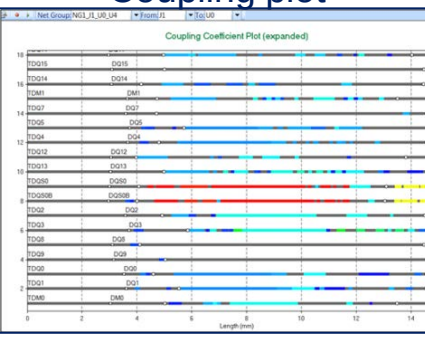
Complete solutions

Geometry-based and simulation-based layout checks



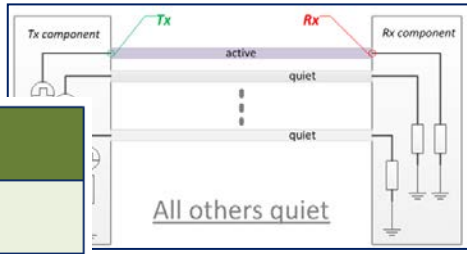
Coupling plot

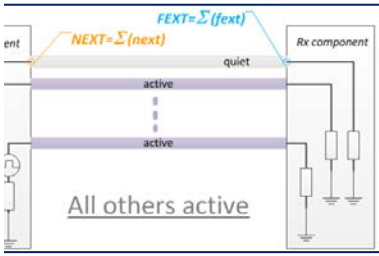


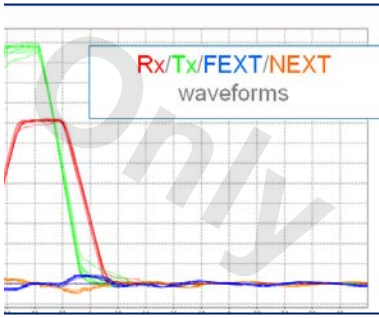
Coupling table

DRC……ERC

Trace Impedance/Coupling Check	SI Metrics Check
Geometry-based	Simulation-based
Micro, individual, segment-level view (coupling %, Ω & mm)	Macro, combined net-level, view (mv & ps)
Options Check all nets Check selected nets Check nets in net groups	**Options** Level-1 simulation Level-2 simulation Level-3 simulation
Results Coupling coefficient Impedance Trace reference Summary & detailed tables Expanded & collapsed plots Layout overlay Layout cross probing HTML report	**Results** Waveforms: Tx / Rx / NEXT / FEXT v_min & v_max SI performance metrics HTML report







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Complete solutions

Layout-based time-domain SI/PI simulation

- SPEED2000™ is industry's only layout-based time-domain SI/PI tool
- Five major workflows available for SI/PI analysis at level-1 to level-3

Workflow 1 General SI Simulation	Workflow 2 Trace Impedance/ Coupling Check	Workflow 3 SI Performance Metrics Check	Workflow 4 DDR Simulation	Workflow 5 Time-domain PDN Simulation
Mainstream SI *L1/L2 for fast sim* Easy to setup; Sim runs fast Waveforms & measurements	Geometry based Trace impedance, coupling & reference check for entire board or net groups Results tables; Results plots; Layout overlay; Layout x-probing	Simulation based *L1/L2 for fast sim* *L3 for non-ideal PDN* Loss, reflection, xtalk check, typically by net groups Waveforms; Xtalk v_max & v_min	Layout-based DDR simulation *L1/L2 for fast sim* *L3 for SSO* No s-parameter model needed for on-board DRAMs Waveforms & measurements	Layout-based TD PDN sim PDN chip-pkg-board co-sim with *-Voltus die mode* *- XcitePI IO model with die grid* Voltage / current distributions; dynamic noise propagation

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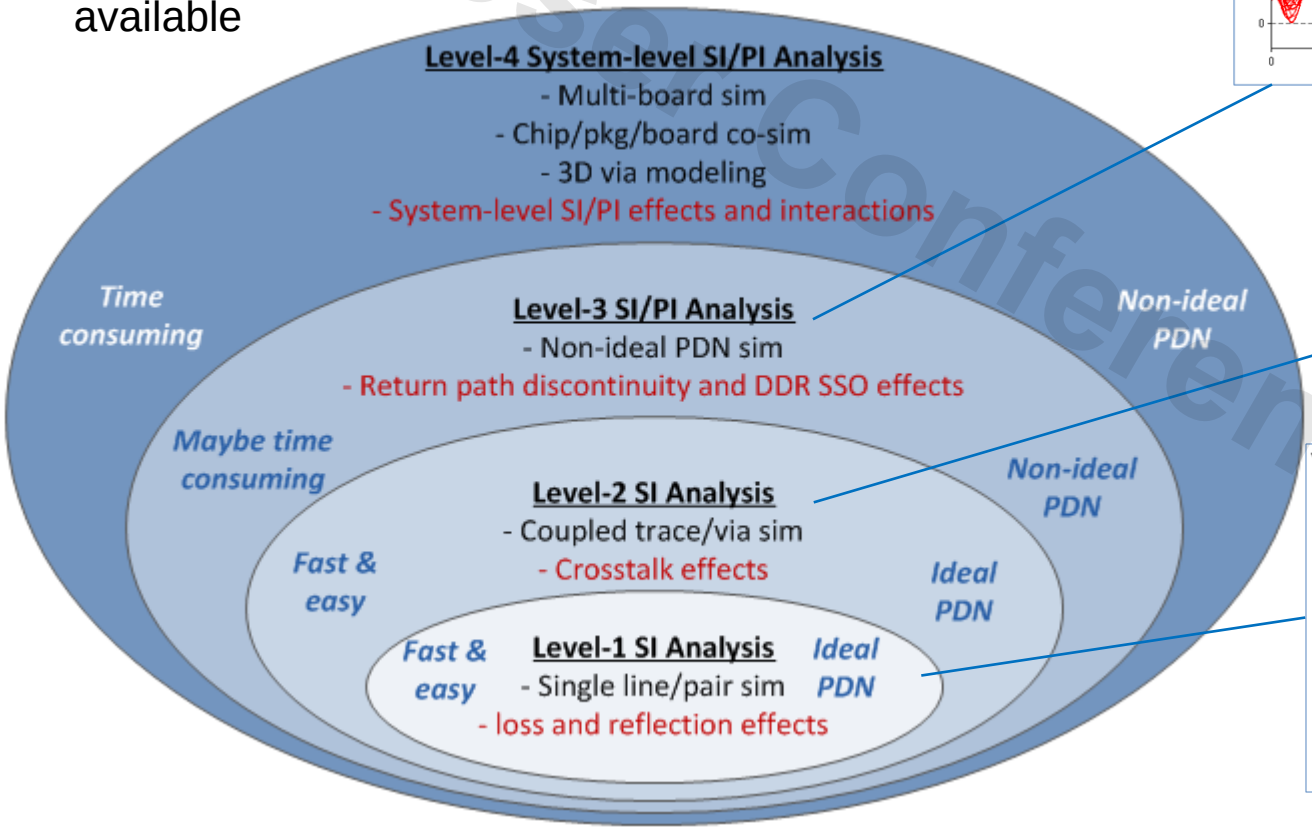
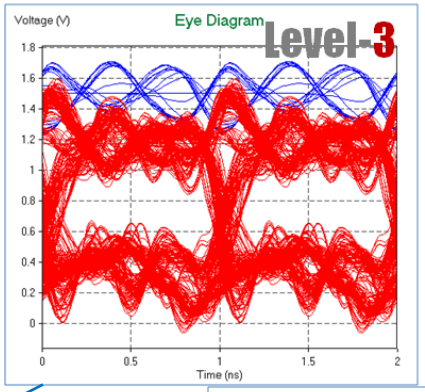
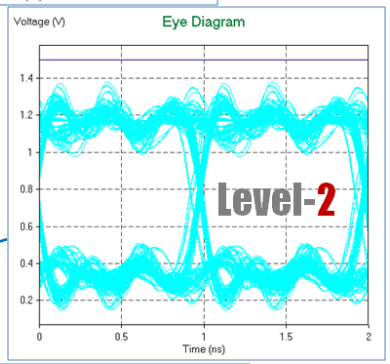
Complete solutions

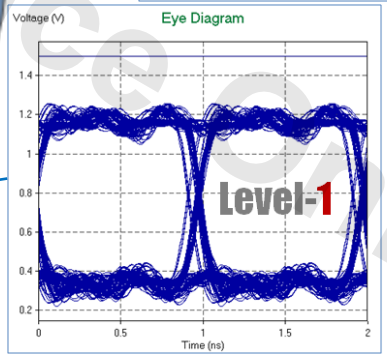
Different levels for different SI/PI/EMI needs

- Using Sigrity technology, SI/PI simulations can be done at 4 levels based on considerations of trace/via couplings and non-ideal PDN
- Both layout-based and model-based solutions are available









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Complete solutions

Layout-based frequency-domain SI/PI simulation

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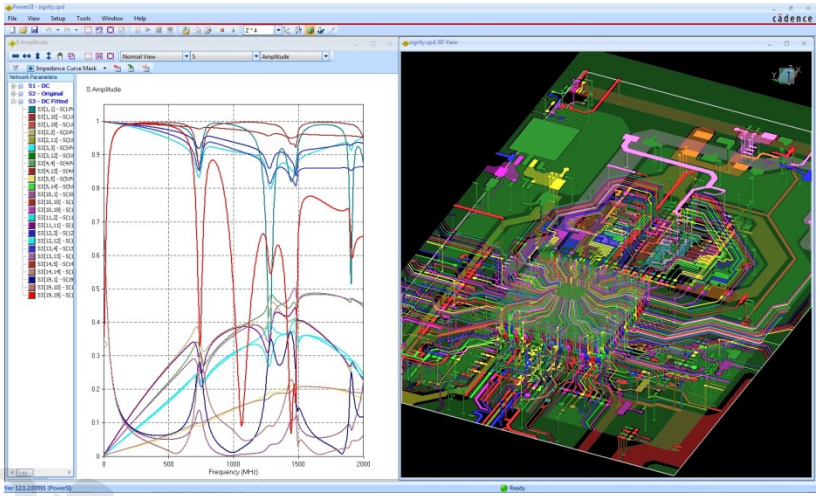
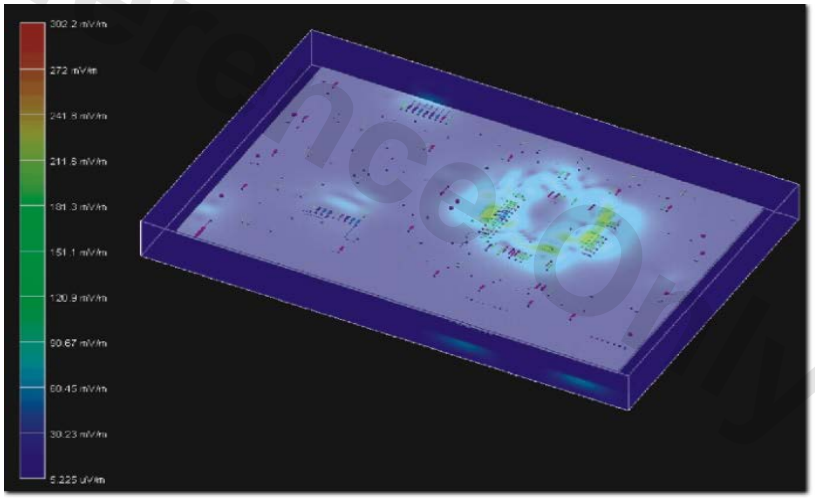
- Market leader and product of choice where power and signal integrity analysis is essential
- Highly accurate modeling of IC package and PCB structures
- Single-ended and mixed-mode results and post-processing
- Adaptive frequency sampling and intelligent result storage
- Supports component / circuit models with unlimited terminals
- Unique capability for ensuring accuracy down to DC with integrated PowerDC analysis
- Targeted workflows to streamline setup operations
- Integration with full wave 3D EM solver



Frequency domain SI, PI and EMC



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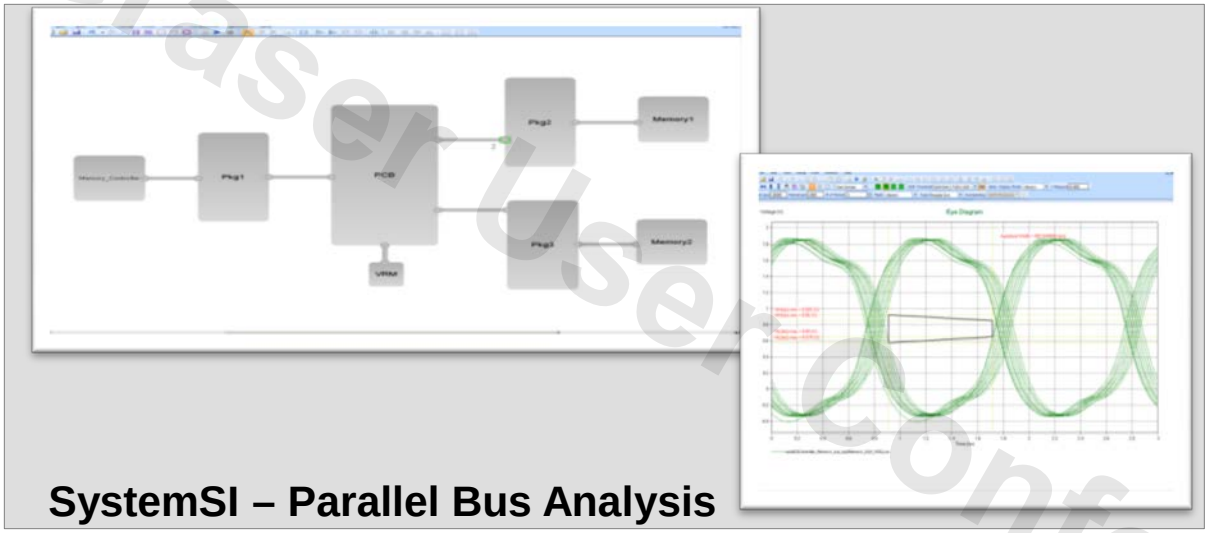
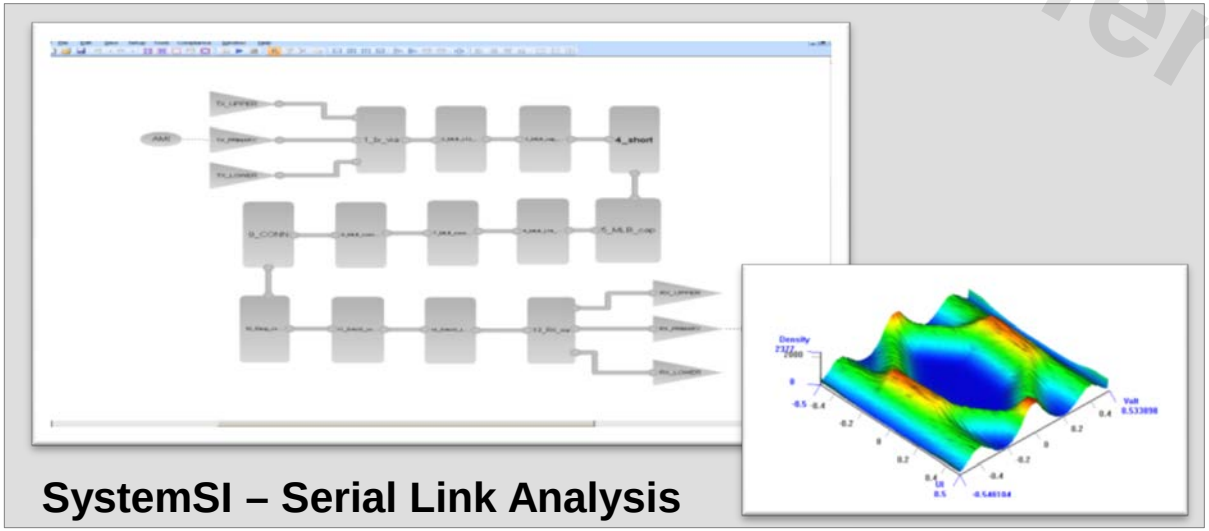
Complete solutions
High-speed bus simulation



SystemSI – Parallel Bus Analysis



SystemSI – Serial Link Analysis

- Simplified model connections with Model Connection Protocol (MCP) and block-wise editor
- IBIS and SPICE-based power-aware system-level modeling
- Concurrent, comprehensive simulation of both SI and PI effects
- Highly automated JEDEC-based measurement, reporting, and crossprobing capabilities for DDR interfaces
- Advanced channel simulation engine for high-capacity serial link simulation and BER analysis
- Comprehensive, parameterized AMI model library for modeling of advanced SerDes equalization

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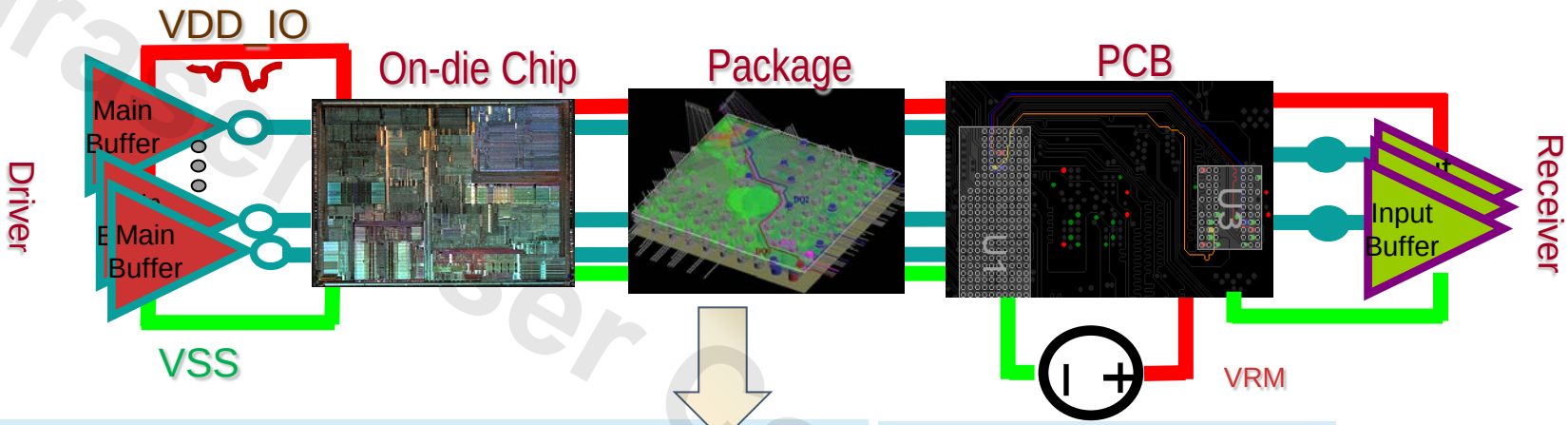
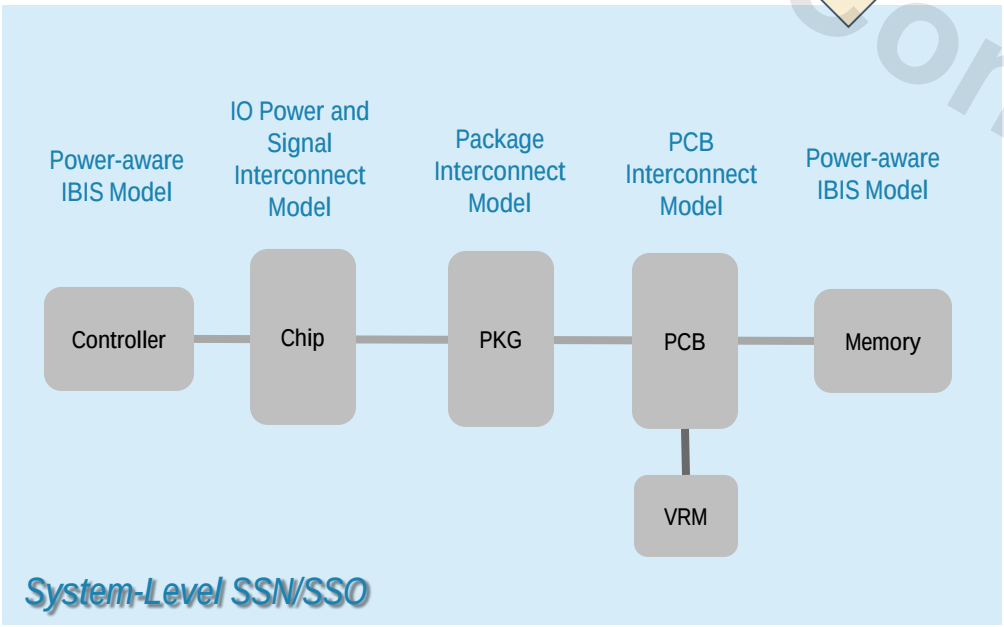
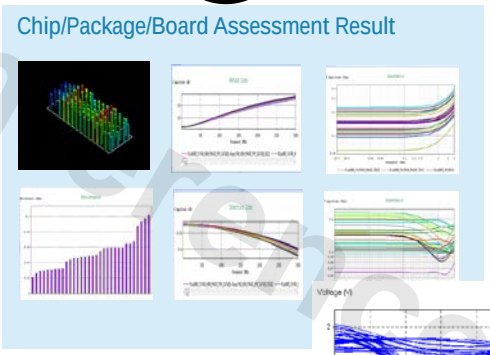
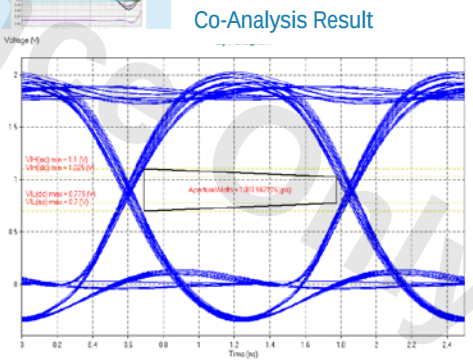
Complete solutions

IOSSO









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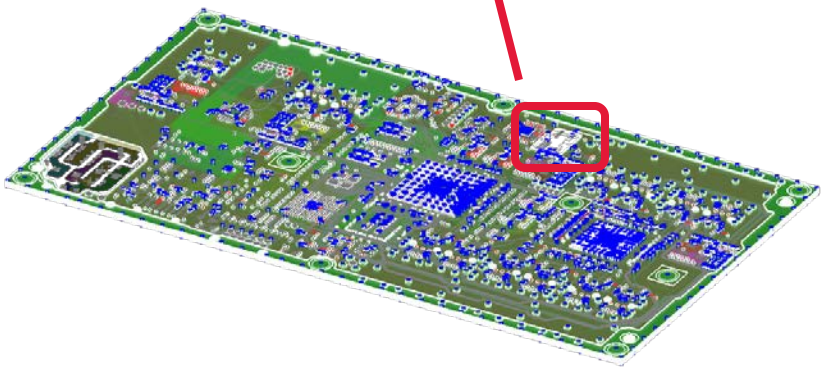
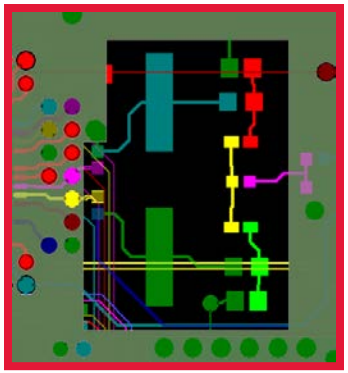
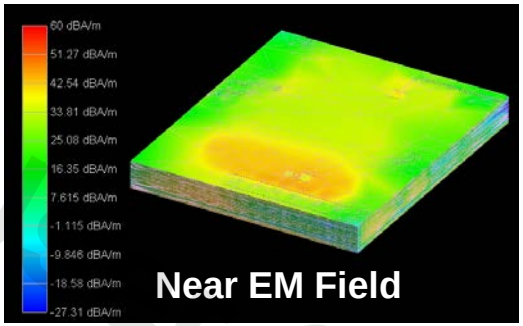
Complete solutions

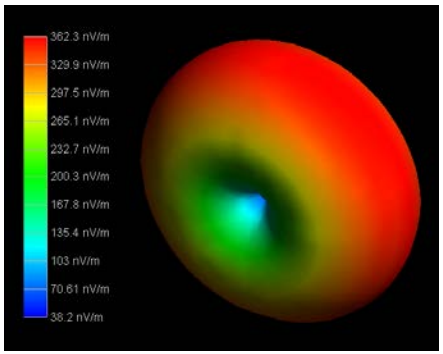
EMI/EMC

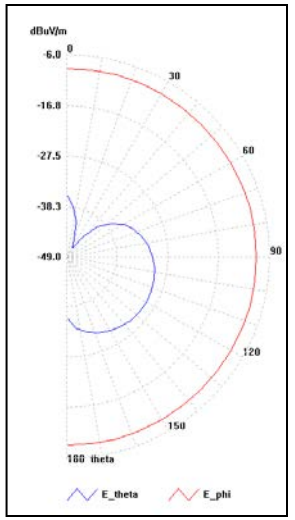


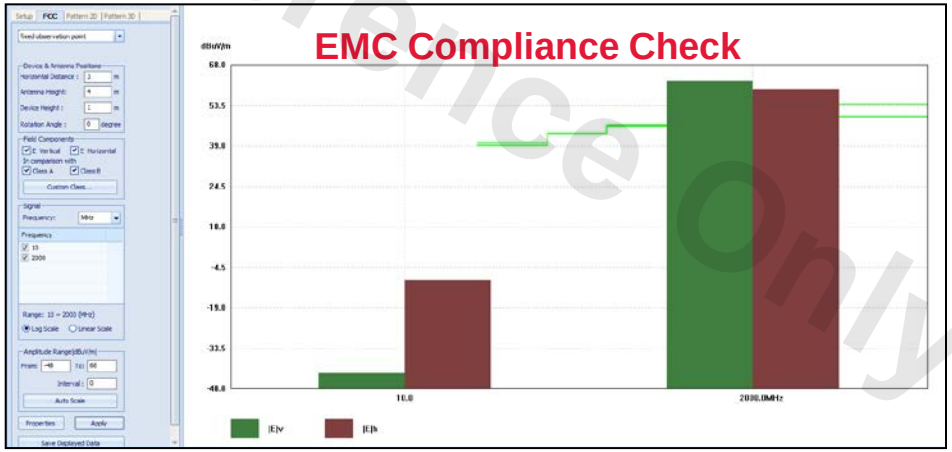




Far EM Field







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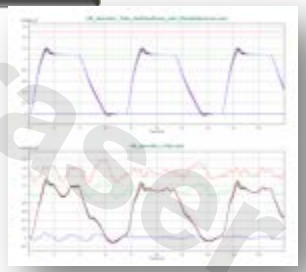
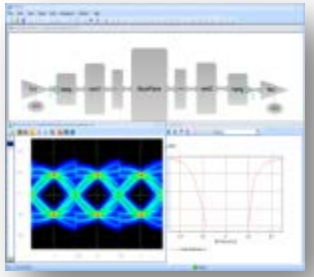
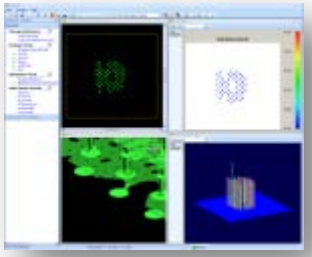
Allegro Sigrity SI Options







Power Aware SI Option

- SIGR011 Broadband SPICE®
- SIGR021 T2B™
- SIGR031 CAD Translators
- SIGR301 PowerSI™
- SIGR311 3D-EM
- SIGR401 SPEED2000™
- SIGR556 SystemSI™ – PBA II

Serial Link SI Option

- SIGR011 Broadband SPICE
- SIGR021 T2B
- SIGR031 CAD Translators
- SIGR301 PowerSI
- SIGR311 3D-EM
- SIGR506 SystemSI – SLA II

Package Assessment and Model Extraction Option

- SIGR031 CAD Translators
- SIGR201 PowerDC™
- SIGR311 3D-EM
- SIGR801 XtractIM™

Note: Each option is a single user license. Only one of the products listed in each option can be run at a time.

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Allegro Sigrity PI and Allegro PCB Editor
Integrated design and power analysis

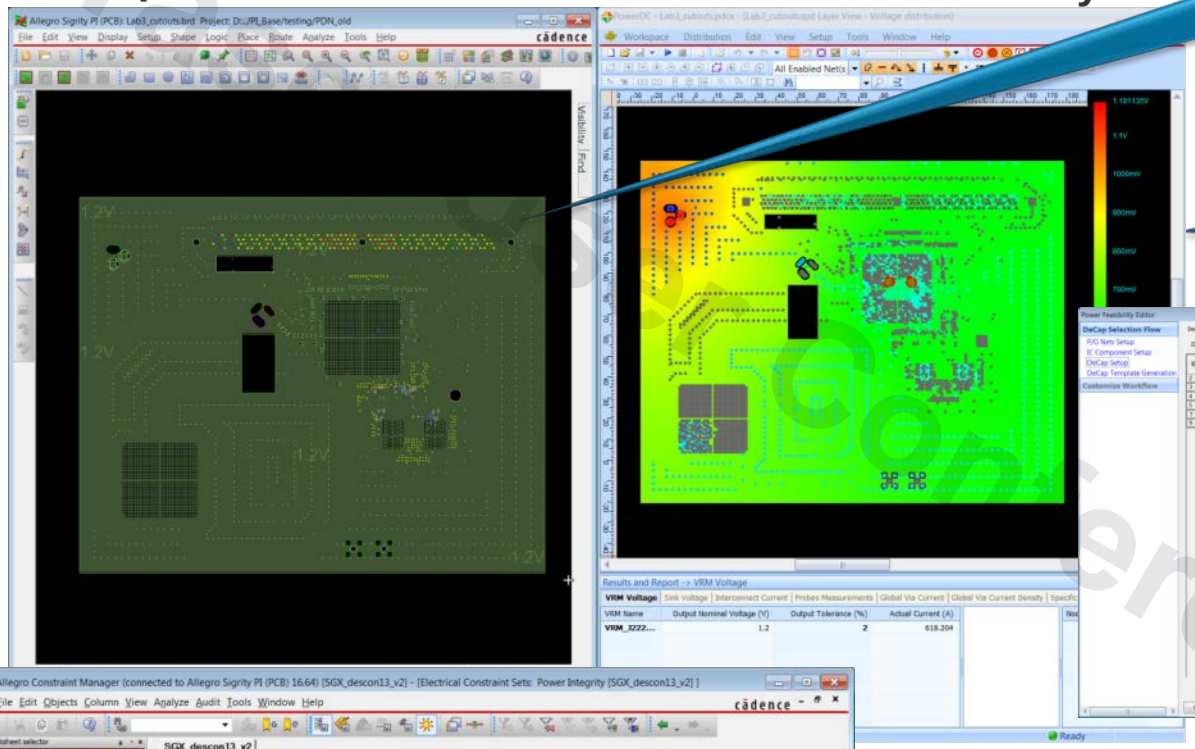
Optimization and Signoff Option
Package Assessment Option
Allegro Sigrity PI Base

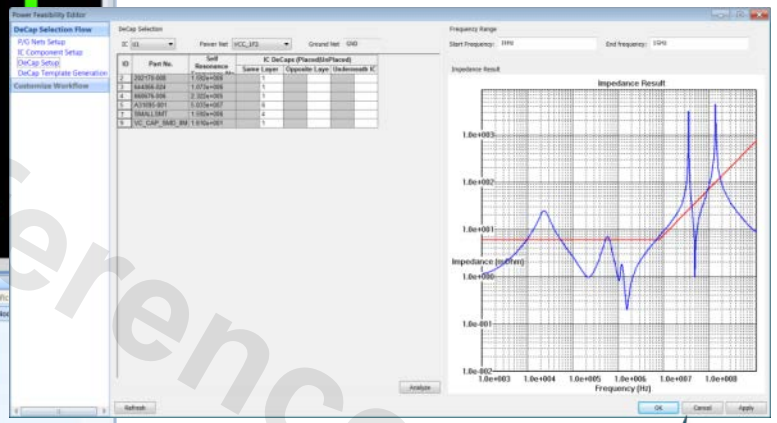
- Allegro based editor for .brd, .mcm, or .sip
- Layout editing and routing

- Sigrity technology with cross-probing to layout

Floorplanner

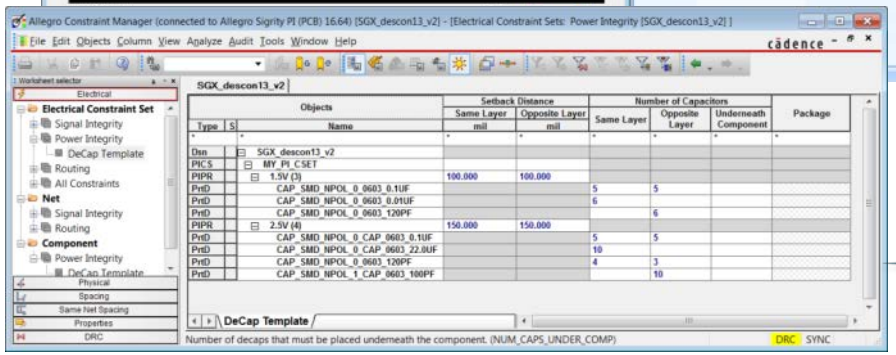
DC Analysis





Power Feasibility Editor

- New unique constraint driven DeCap flow



Constraint Manager

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Allegro Sigrity PI and Allegro PCB Editor
Constraint Driven Power Integrity

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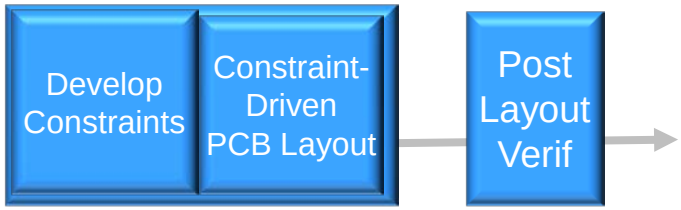
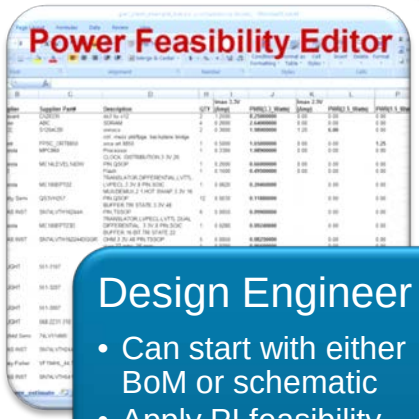
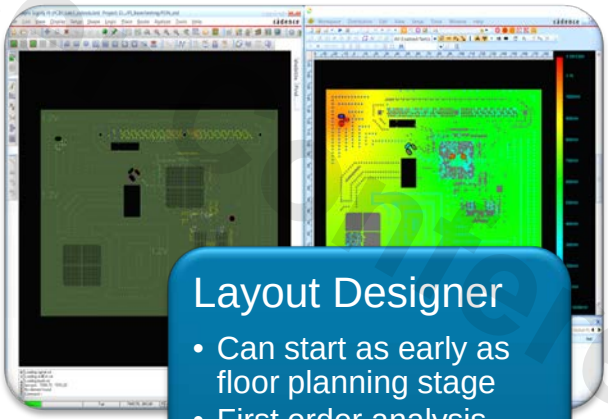




Design Engineer
- Can start with either BoM or schematic
- Apply PI feasibility studies for DeCap selection and PI constraint definition



Layout Designer
- Can start as early as floor planning stage
- First order analysis directly on layout
- Analyze, edit, re-analyze flow desired
- DeCap placement guidance and DRC

PI Engineer
- Can start at any stage
- Leverages setup and data from rest of team
- Signoff capable detailed analysis required

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Complete solutions

Decoupling capacitor optimization

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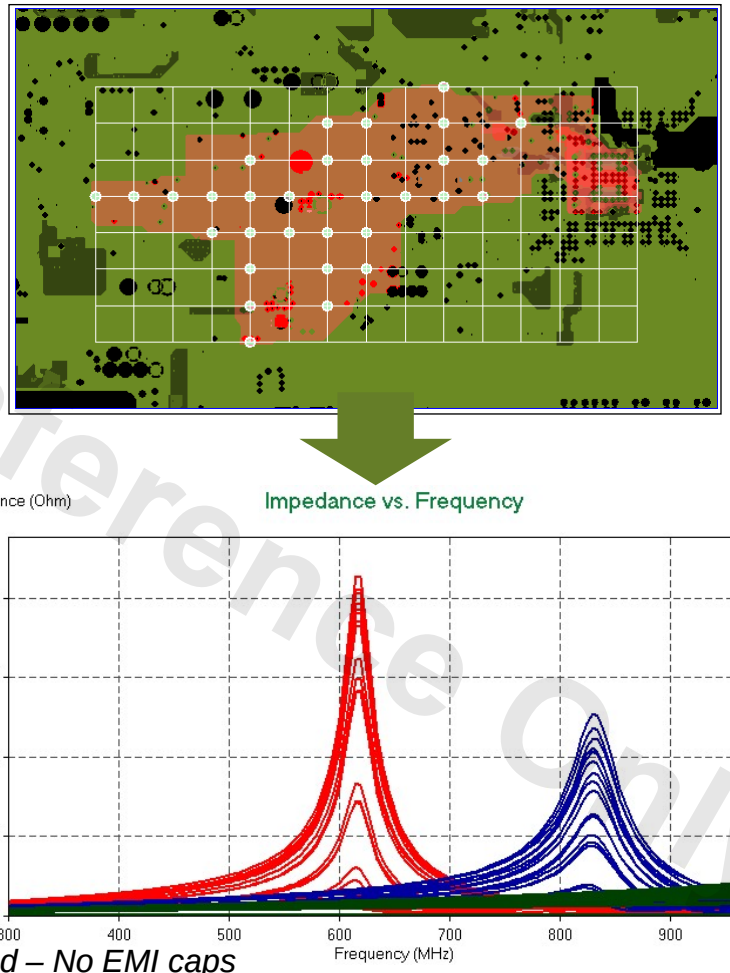
- Automated DeCap optimization of placement and value selection
- Multiple objectives: performance, cost, area, number
- Device impedance and EMI resonance checking
- DeCap loop inductance analysis to identify poorly mounted caps
- Device per-pin inductance checking and display

Automated positioning and selection of EMI decoupling capacitors



Red – No EMI caps
Blue – 1 cap; Green – 3 caps

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Complete solutions

Multi-board-package SI/PI simulations

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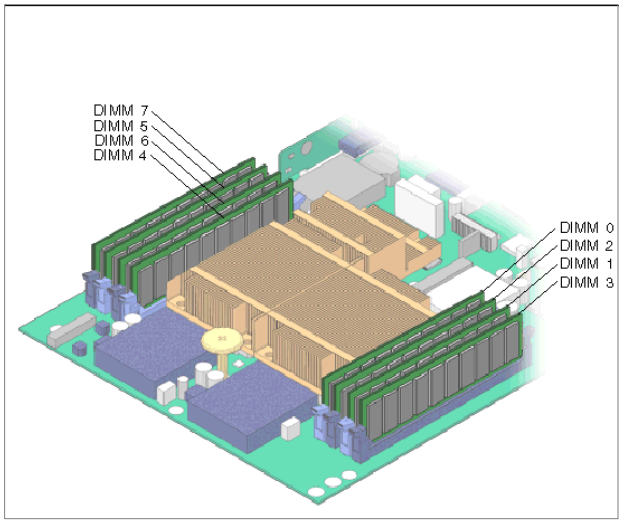
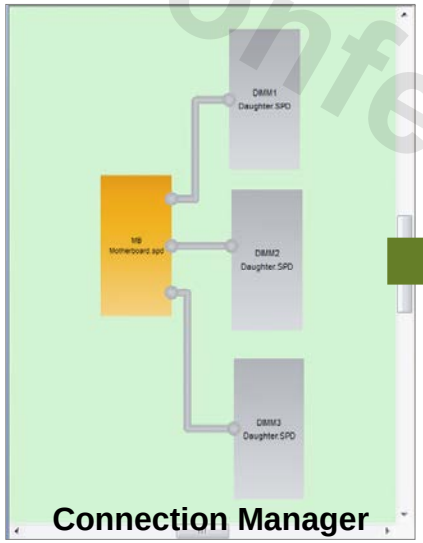
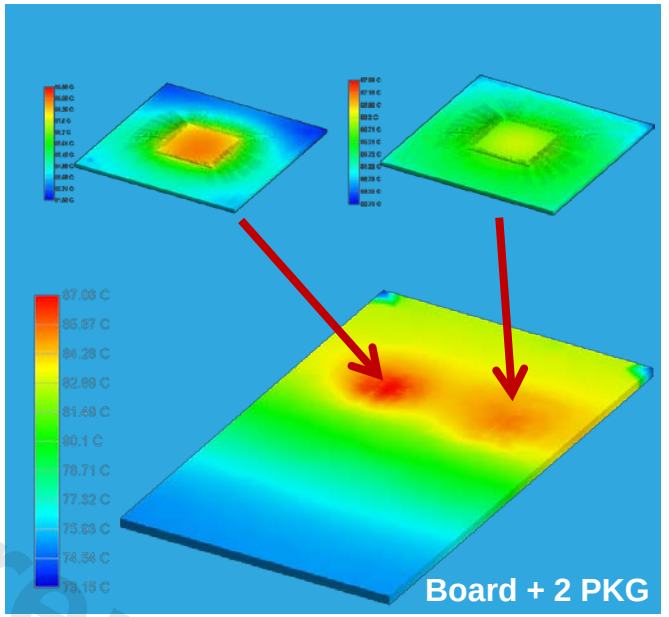
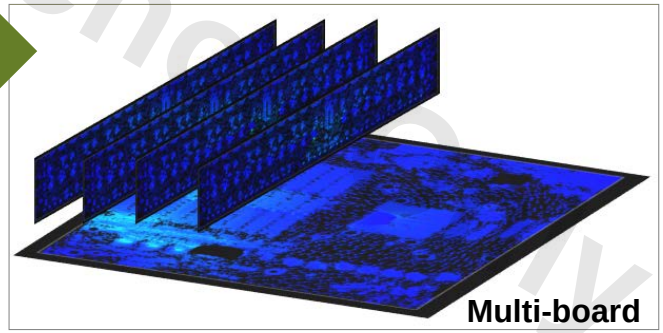
- Industry's first layout-based multi-board-package simulation flow









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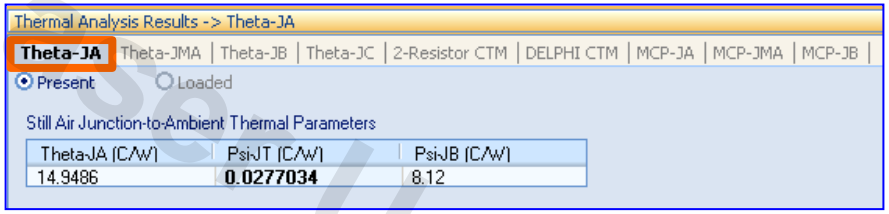
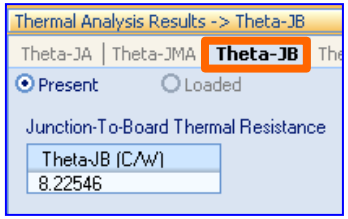
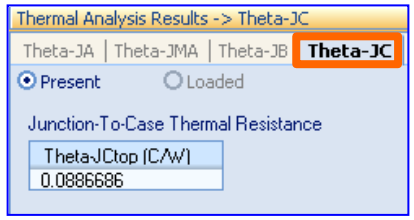
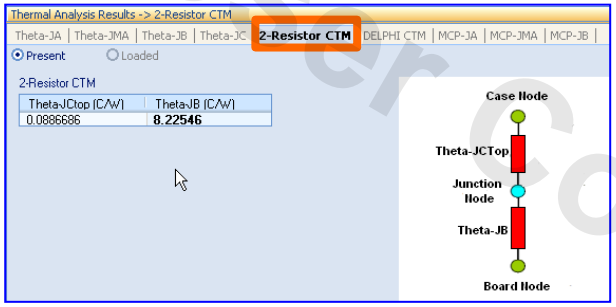
Complete solutions

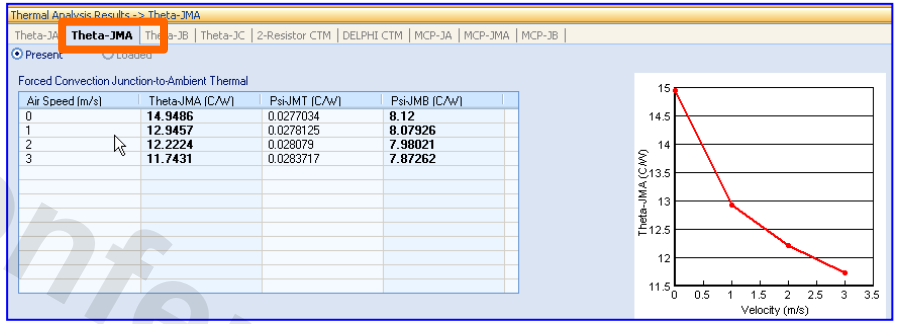
Extraction of package thermal parameters

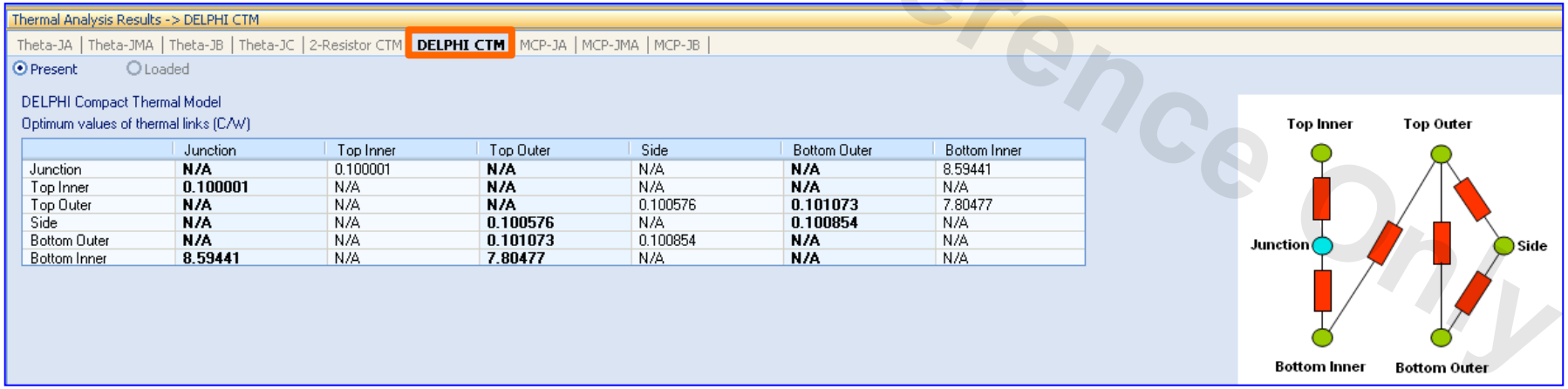












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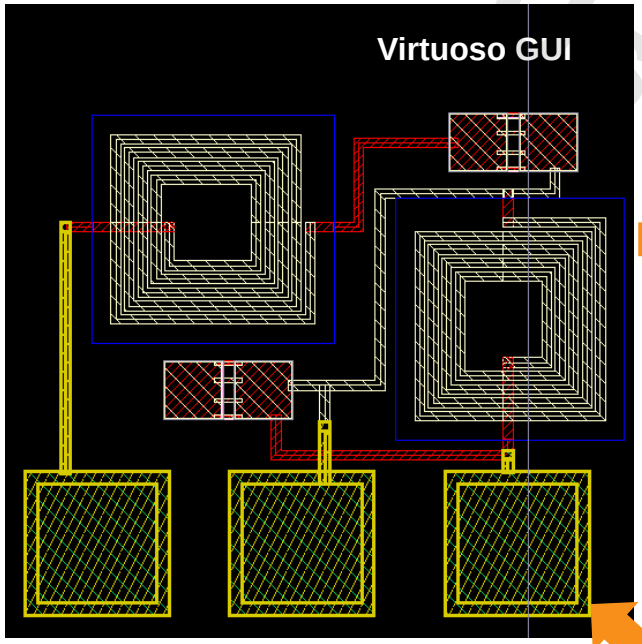
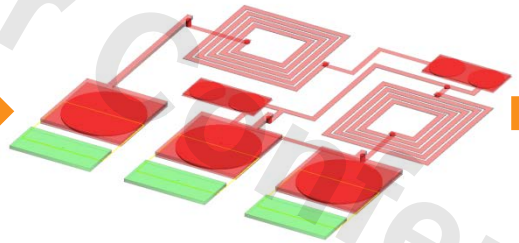
Complete solutions

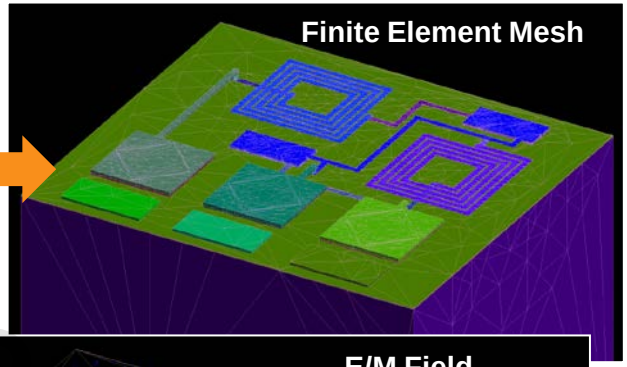
RFIC passive component extraction

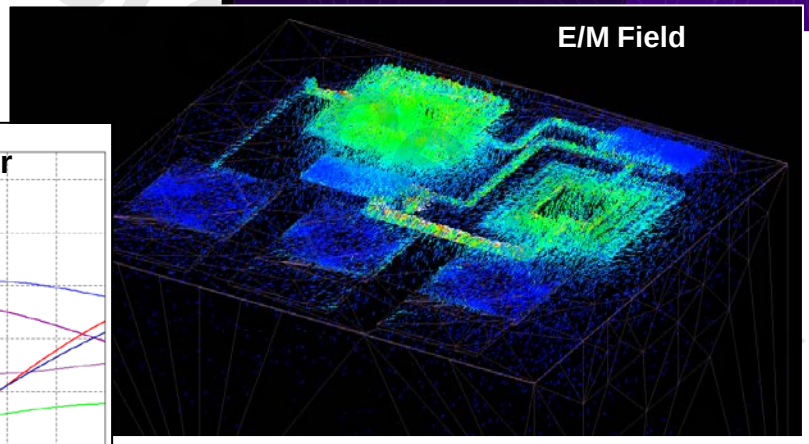
Virtuoso® GUI → Virtuoso Data of Selected Components → .spd file → 3DFEM engine

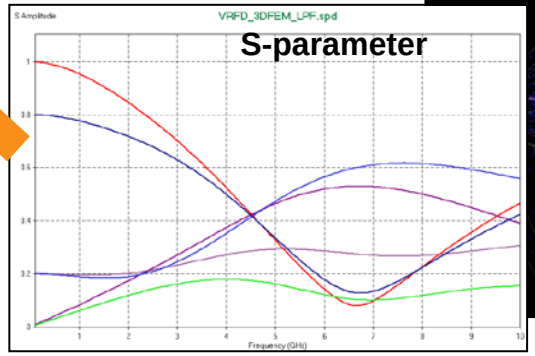


3D View of spd









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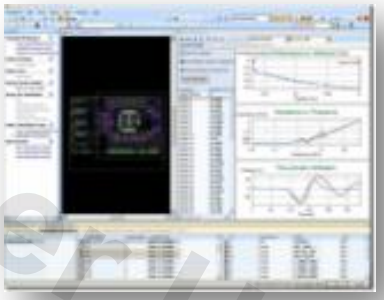
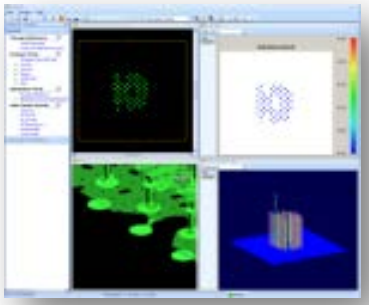
Allegro Sigrity PI Options





Power Integrity Signoff and Optimization Option

- SIGR031 CAD Translators
- SIGR051 OptimizePI
- SIGR201 PowerDC
- SIGR301 PowerSI
- SIGR311 3D-EM

Package Assessment and Model Extraction Option

- SIGR031 CAD Translators
- SIGR201 PowerDC
- SIGR311 3D-EM
- SIGR801 XtractIM

Note: Each option is a single user license. Only one of the products listed in each option can be run at a time.

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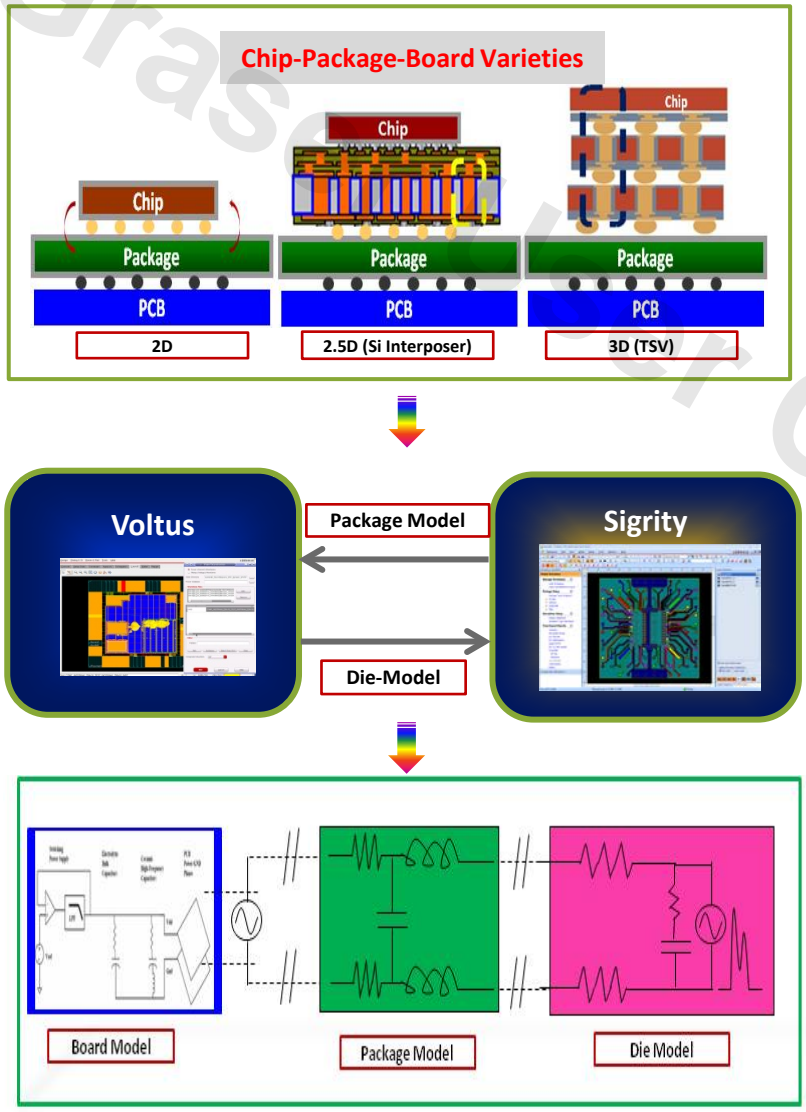
Complete solutions

Chip/package/board co-analysis



- Sigrity package model generation
  - XtractIM™ broadband SPICE format
  - PowerSI® S-parameter format
- Voltus™ die model generation
  - Broadband SPICE format
  - Frequency and time domains
  - Single-port and N-port (up to 100s)
- Sigrity MCP interface
  - Model connection protocol
  - Name- or location-based
- Complete power integrity solutions
  - Chip: Voltus solution + package model
  - System: PowerDC™ technology + die model

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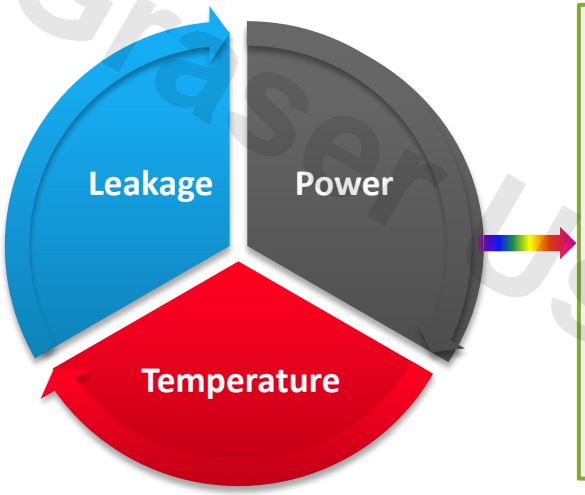
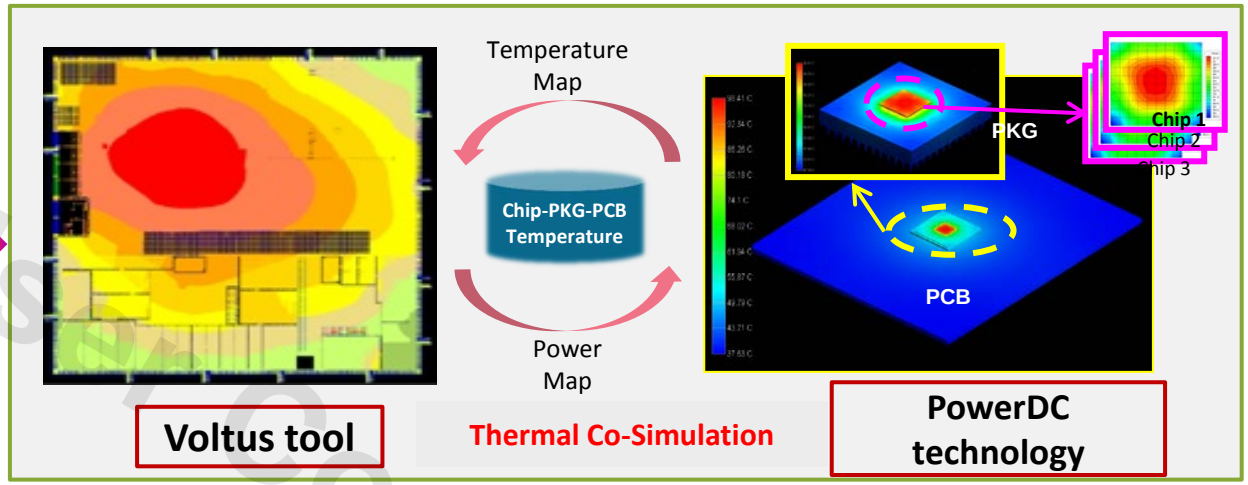
Complete solutions

Electrical/thermal co-analysis





- Thermal runaway
  - Positive feedback among chip's temperature, leakage, and power dissipation
  - Temperature-dependent IR-drop and EM
- Thermal simulation in "Voltus tool + PowerDC technology"
  - Voltus output: temperature and location-dependent "power map" file
  - PowerDC technology computes detailed temperature distribution for chip-PKG-PCB (T vs. time)
  - Voltus tool reads back "temperature map" file for EMIR convergence
  - Thermal view available in 2D/3D

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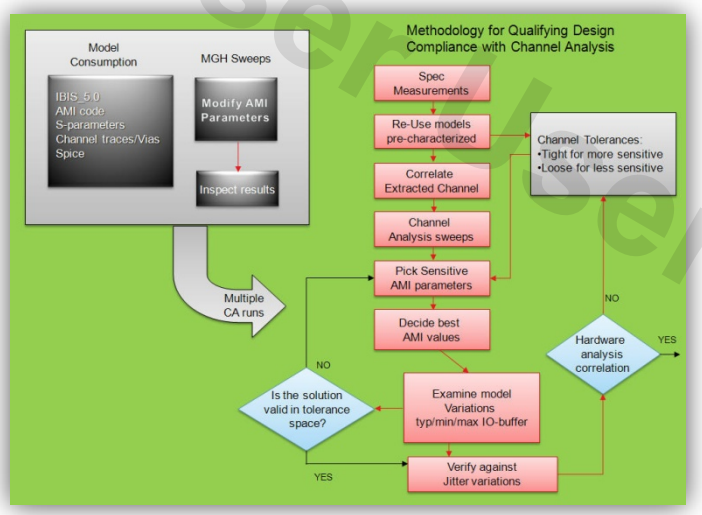
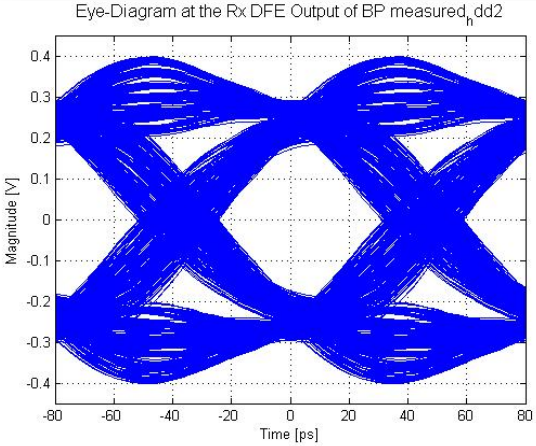
Complete solutions

A success story

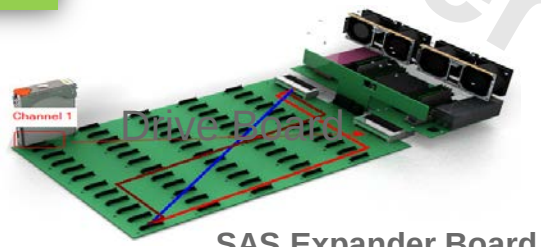
2011 DesignCon

12Gbps shown feasible





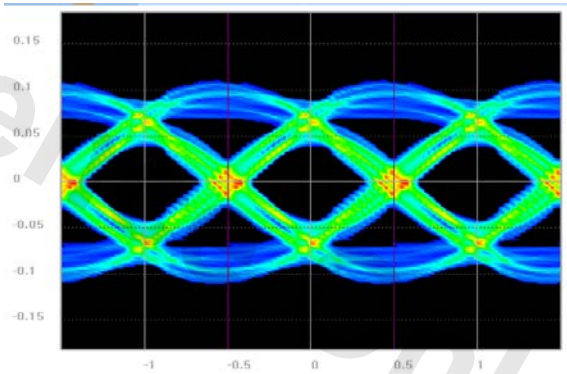
2012 Sigrity Acquisition



SAS Expander Board

2014 CDNLive

12Gbps confirmed



	Simulated	Measured	Hspice
eye height	80mv	78mv	83
eye width	56ps	58ps	61

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Summary

- From Geometry-based layout check to Level-3 simulation-based layout check
- From Mainstream level-1 SI simulation to Level-3 power-aware SI simulation
- From Parallel bus simulation to Serial link simulation
- From PDN DC simulation to PDN AC simulation to Decap optimization
- From Electrical simulation to Electrical / Thermal co-simulation
- From SI simulation to PI simulation to SI/PI/EMI co-simulation
- From IOSSO / PDN PCB level simulation to Chip/Pkg/Board co-simulation
- From Pkg electrical model generation to Thermal pkg parameters generation
- From BBS model extraction to RFIC passive component extraction
- From IBIS model generation to AMI model generation

SPEED2000 | PowerSI | 3D-EM
SystemSI | T2B | PowerDC
Broadband SPICE | OptimizePI
XtractIM | OrCAD PCB SI
XcitePI | IO-SSO solution
Allegro Sigrity SI Base + options
Allegro Sigrity PI Base + options

Cadence/Sigrity
is
your single stop SI/PI/EMI solutions
for
chip-package-board analysis

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Single-stop SI/PI solution for chip-package-board

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