USER CONFERENCE Graser® 2014 Oct 31 Taipei

2.5D/3D Design Solution

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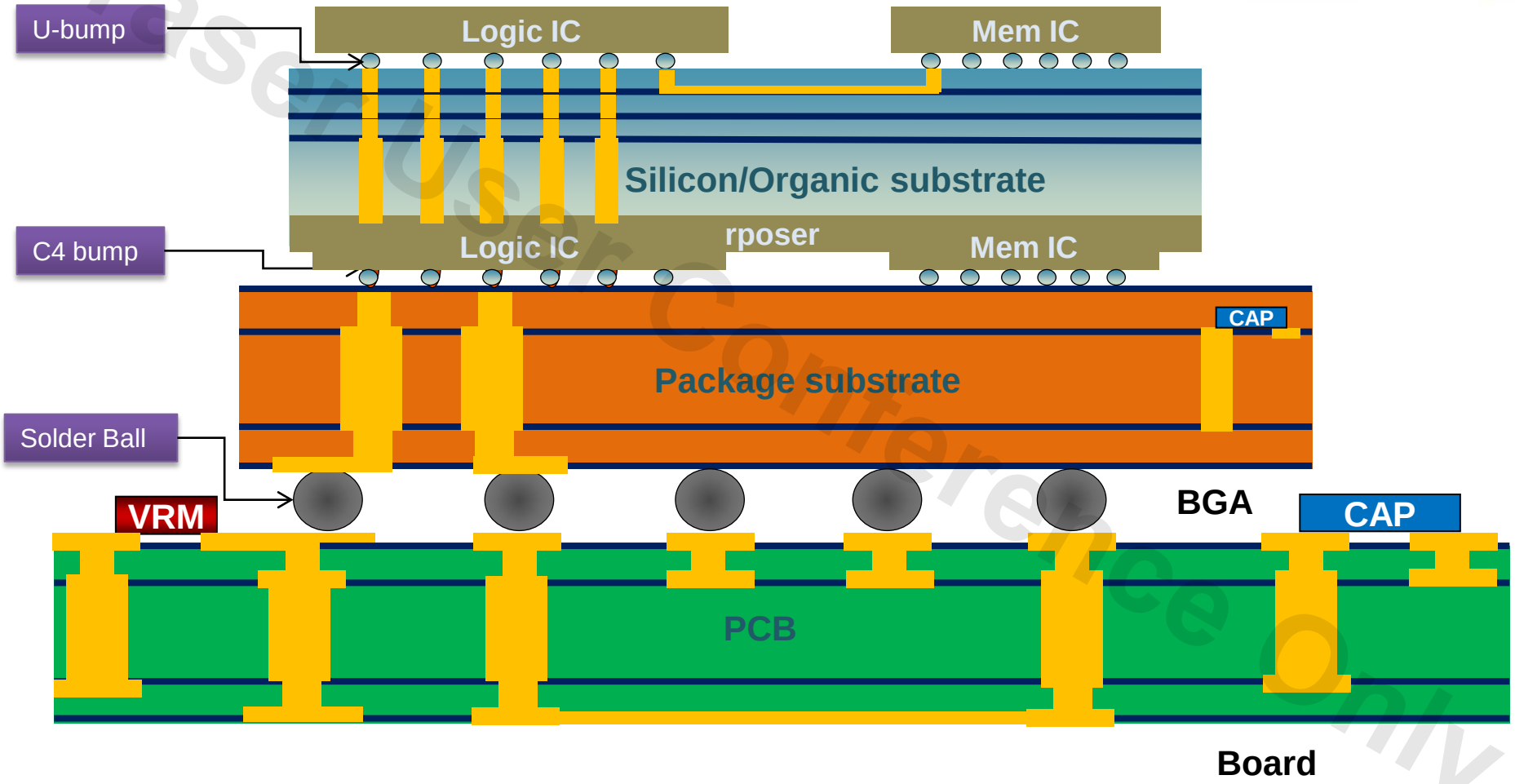
31/Oct/2014

Roadmap data is provided for informational purposes only and does not represent a commitment to deliver any of the features or functionality discussed

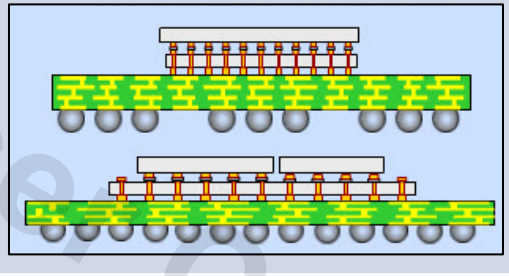
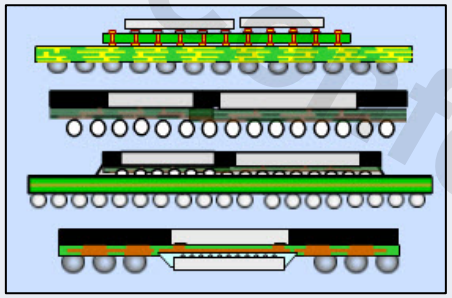
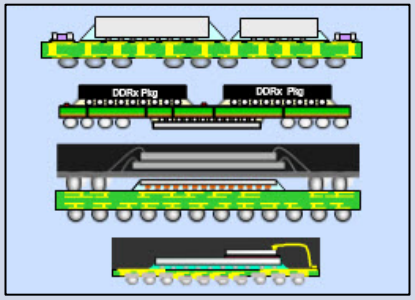
Graser®

Design Overview



Courtesy of TSMC

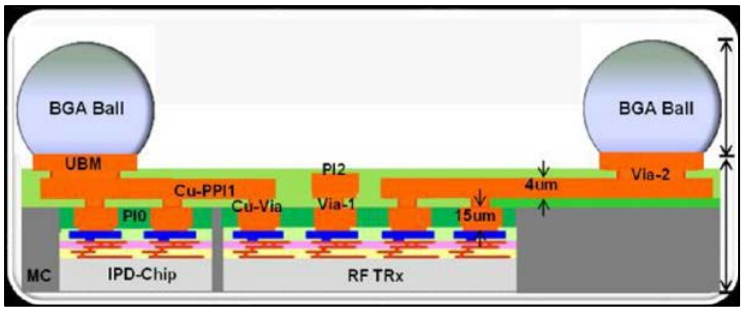
Multiple Pathways to 2.5D/3D Integration

Packaging Platform	Examples	Drivers / Applications
Silicon based interposers Die stacking with TSV		Silicon partitioning CPU/GPU – memory I/F High-end computing High-end networking Memory, FPGAs
Fan out wafer level Organic interposers		Silicon partitioning Logic/memory integration Mobile convergence AP, BB, modem, PMIC, RF Smart phones & tables
Conventional laminate build-up technologies		Multi-die integration Logic/memory integration Baseband, analog, RF, passive

Fan Out Wafer Level Package (FO-WLP)

Impact on the packaging eco-system

- FO-WLP is the fastest growing packaging segment
  - Benefits of cost, performance, thinner profile, & silicon partitioning
  - Technology of choice for HEC
- Lower risk/cost roadmap to 3D integration for some applications
- Emergence of traditional IC fabs into the packaging space
  - TSMC, Intel, Global Foundries, and others
- FO-WLP is considered a “middle-end” technology
  - Front-end IC fabs extending capabilities down into packaging space
  - Back-end OSATs extending capabilities up into wafer level space
  - Both are aggressively moving to support FO-WLP



TSMC’s InFo WLP

System Interconnect Planning –
A growing challenge

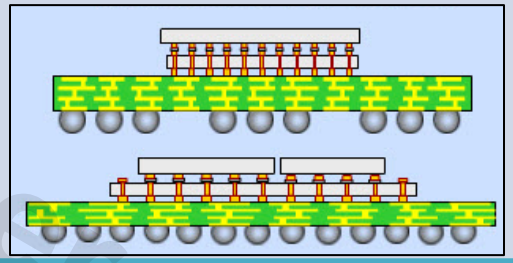
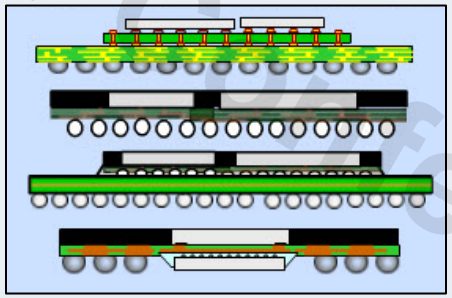
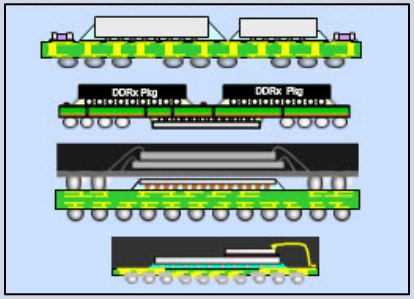
Drivers / Trends	Impact
Advanced nodes driving functional density and pin counts, or use of multi-substrate solutions	Unpredictable system cost and performance
Complexity and performance requirements of high-speed interfaces	Longer development cycles
Die to package net assignment becoming more challenging—PCB considerations	
Geographically diverse engineering teams and packaging resources	Clearly communicating design intent

The Impact of Advanced Packaging Technologies

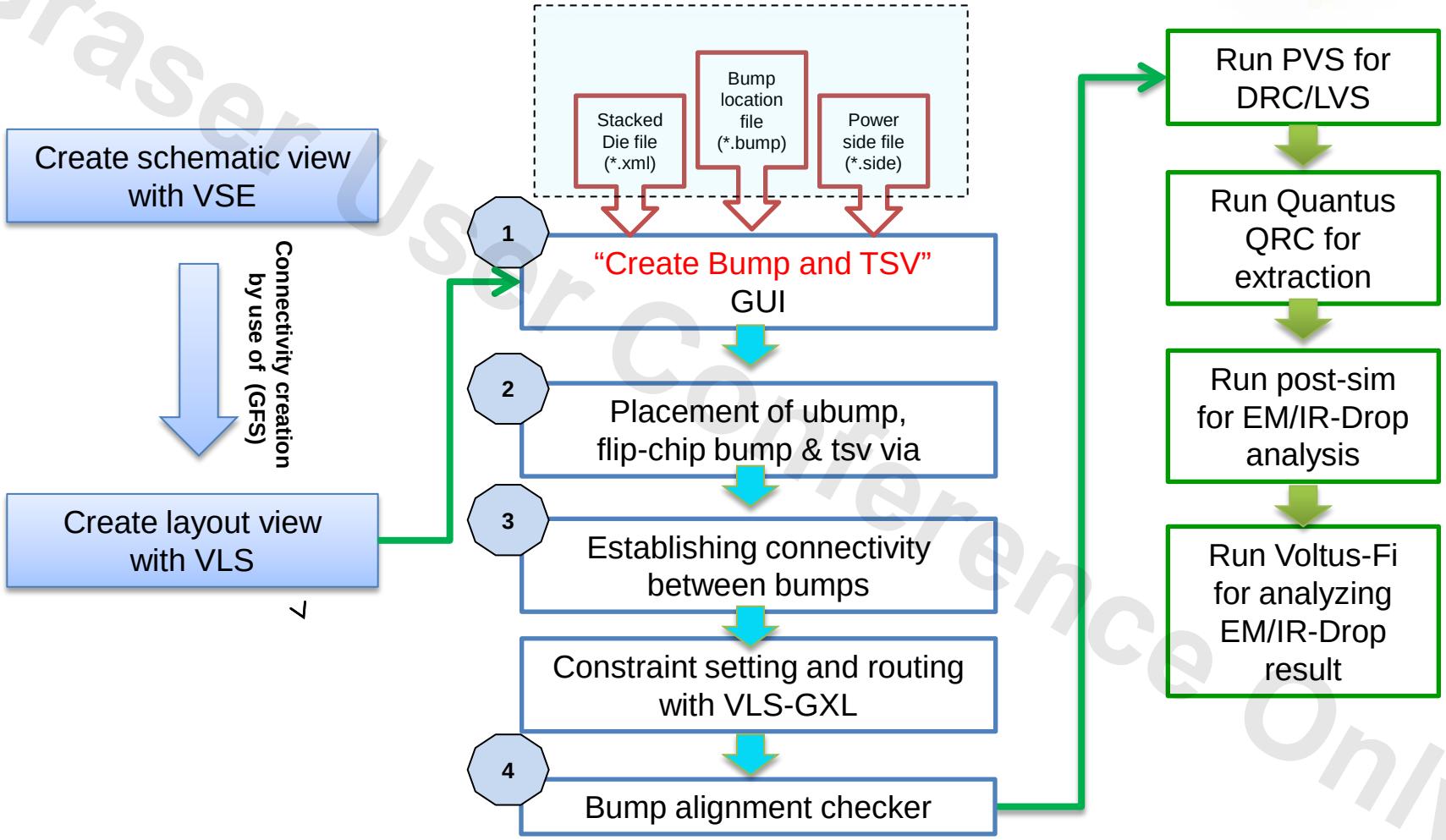
Driving new design requirements and functionality

- Co-design across multiple die, interposers and packages
  - Coordination of IOpads, bumps, RDL, ball pads, TMVs, etc…
  - Support from early planning through implementation
- Increasing complexity of high performance interfaces
  - DDR3, DDR4, PCI Express Gen 3, USB 3.0, etc…
  - Constraints, routing, and optimization
- Support for embedded die within the substrate
  - For both traditional laminate and FO-WLP technologies
- Potential for ‘silicon-like’ design rules and requirements
  - Via structures, metal density, routing, end-caps, etc…
  - Foundry supported PDKs & flows, GDSII manufacturing hand-off
- Multi-die implementation
  - Side-by-side, single-stack, and multi-stack
- Cu Pillar

Advanced Technology Planning & Implementation

Packaging Platform	Examples	Cadence Solutions
Silicon based interposers Die stacking with TSV		**Encounter / Virtuoso**
Fan out wafer level Organic interposers		**SIP Layout-XL OrbitIO APR**
Conventional laminate build-up technologies		

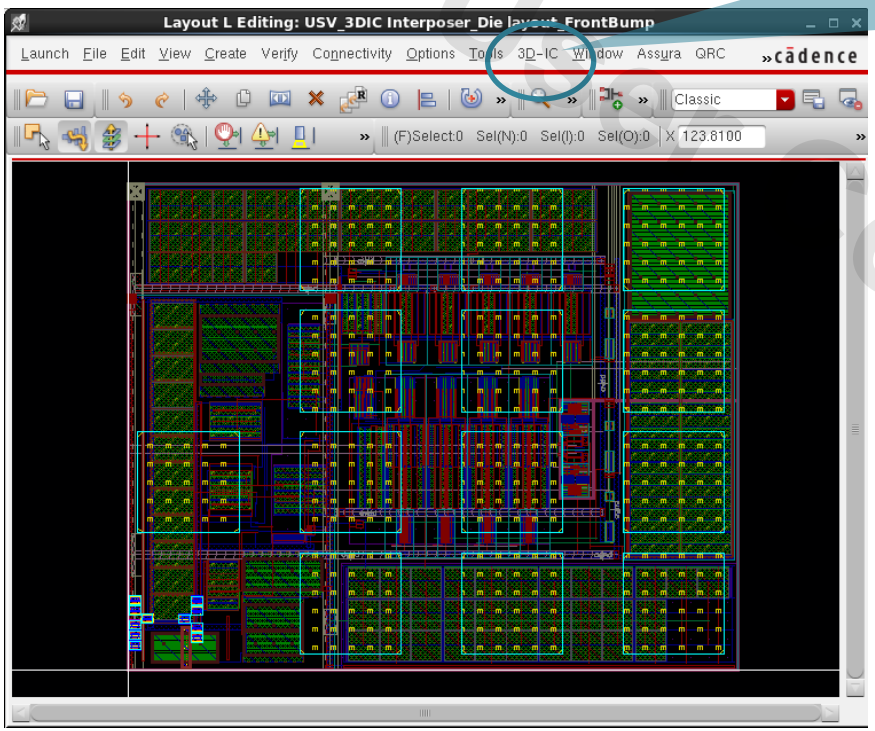
Custom 3D-IC Design Flow

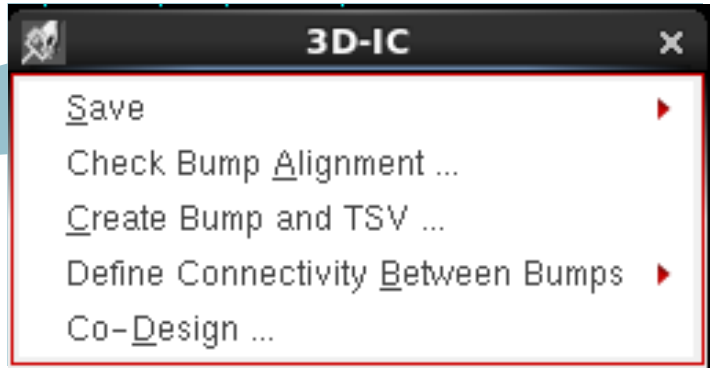


Note: 1+2+3+4 → 3D-IC features

What's Available in Virtuoso Specifics

- Virtuoso 6.1.6/ ICADV12.1

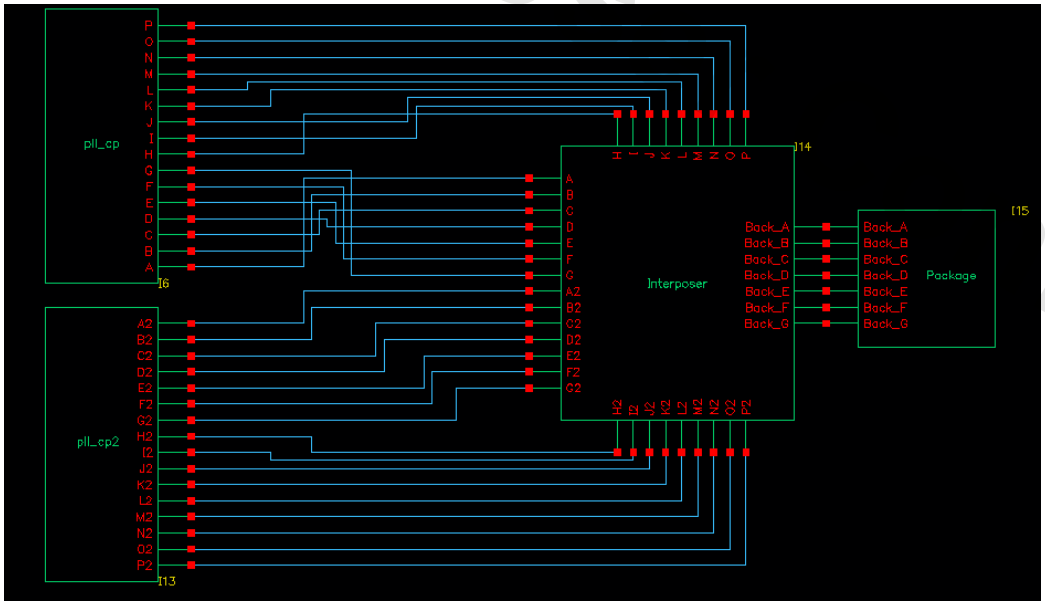


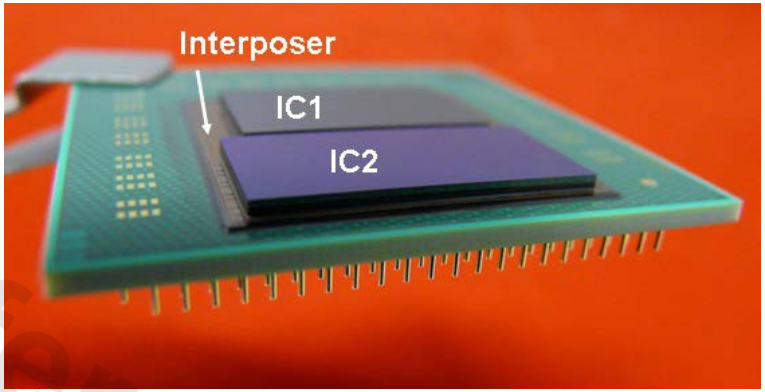


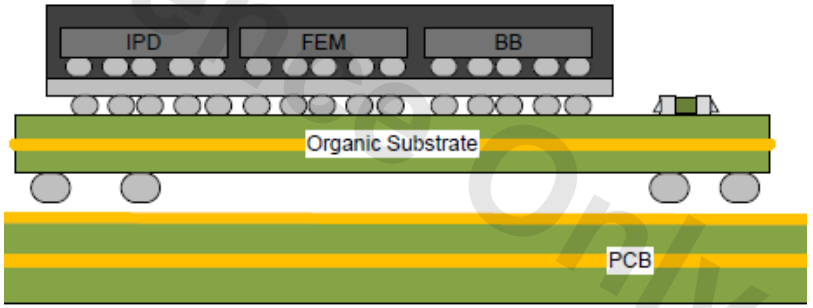
- Bump/TSV creation from adjacent die
- Auto-assign the Terminal to Bump
- Utilities to help resolve bump miss-alignment
- Export the Pad Locations/Bump Mapping File for performing the IR drop analysis

Wrapper Schematic

- Creating Wrapper in VSE
  - Top schematic storing connectivity from die to die/interposer.

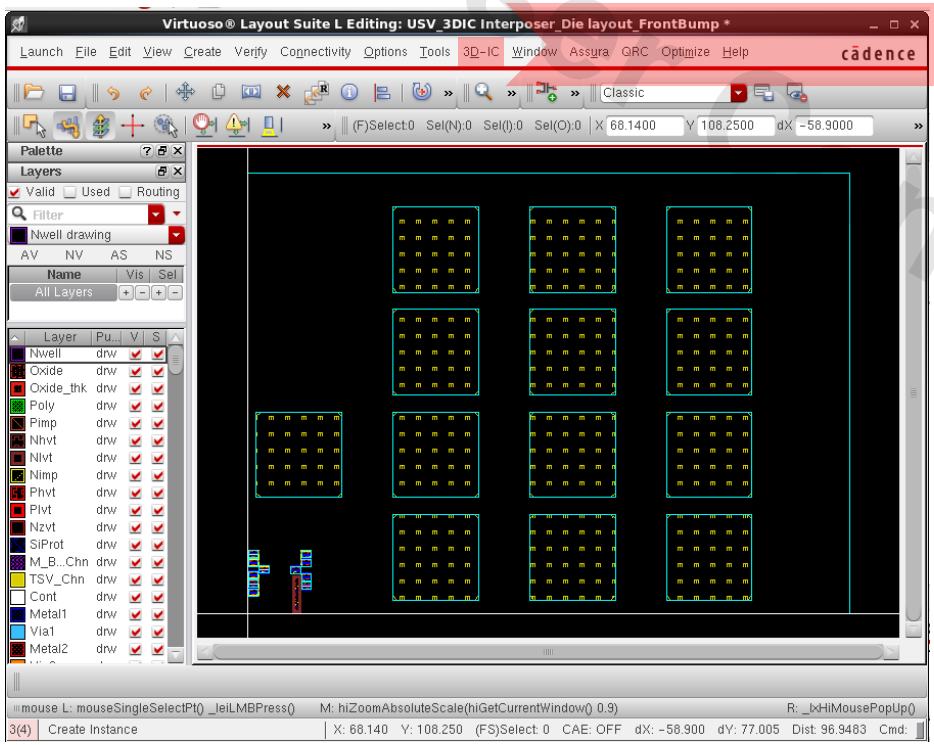


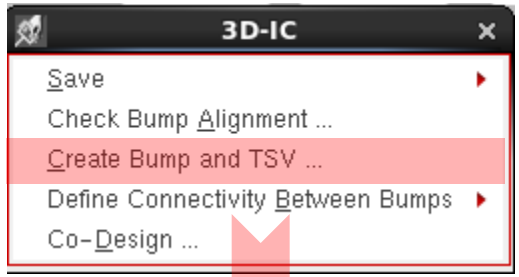


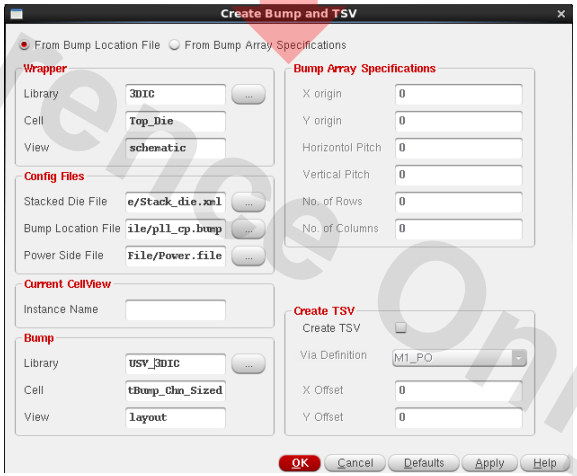


Creating Bump and TSV from VLS

- Create bumps by using a bump location file to transfer bump information from one die to the adjacent die.
- Create bump arrays on dies such as silicon interposers. You need to assign these bump instances to their respective terminals.

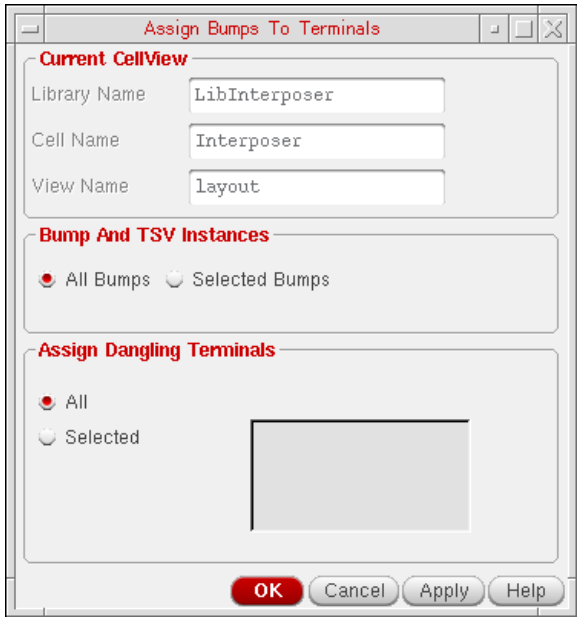


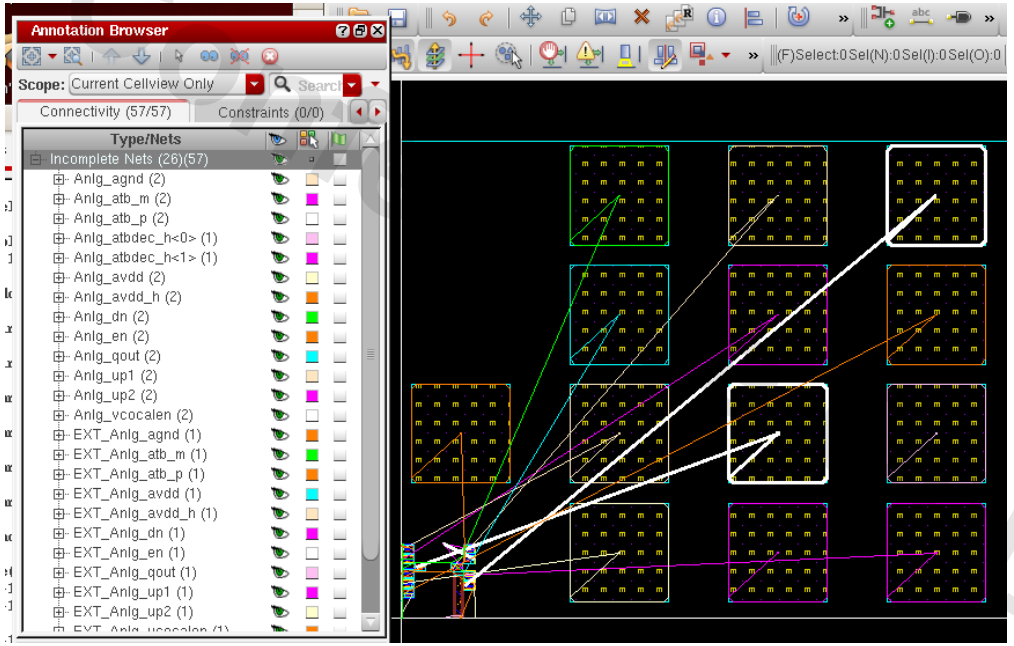




Establishing Connectivity Between Bumps

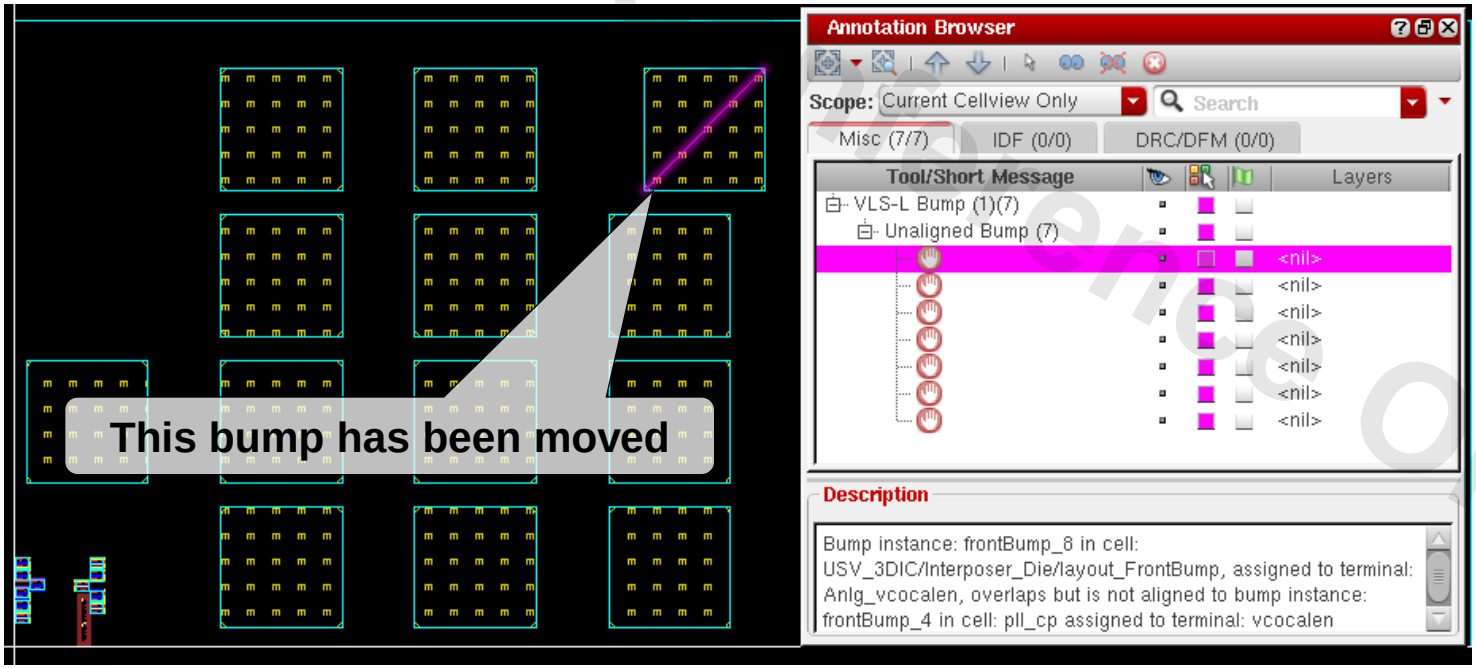
- After creating bumps and TSVs, you establish connectivity between bumps.
  - Assigning Bump Instances to Terminals
  - Moving PinFig Objects to Bumps
  - Creating Bump Labels





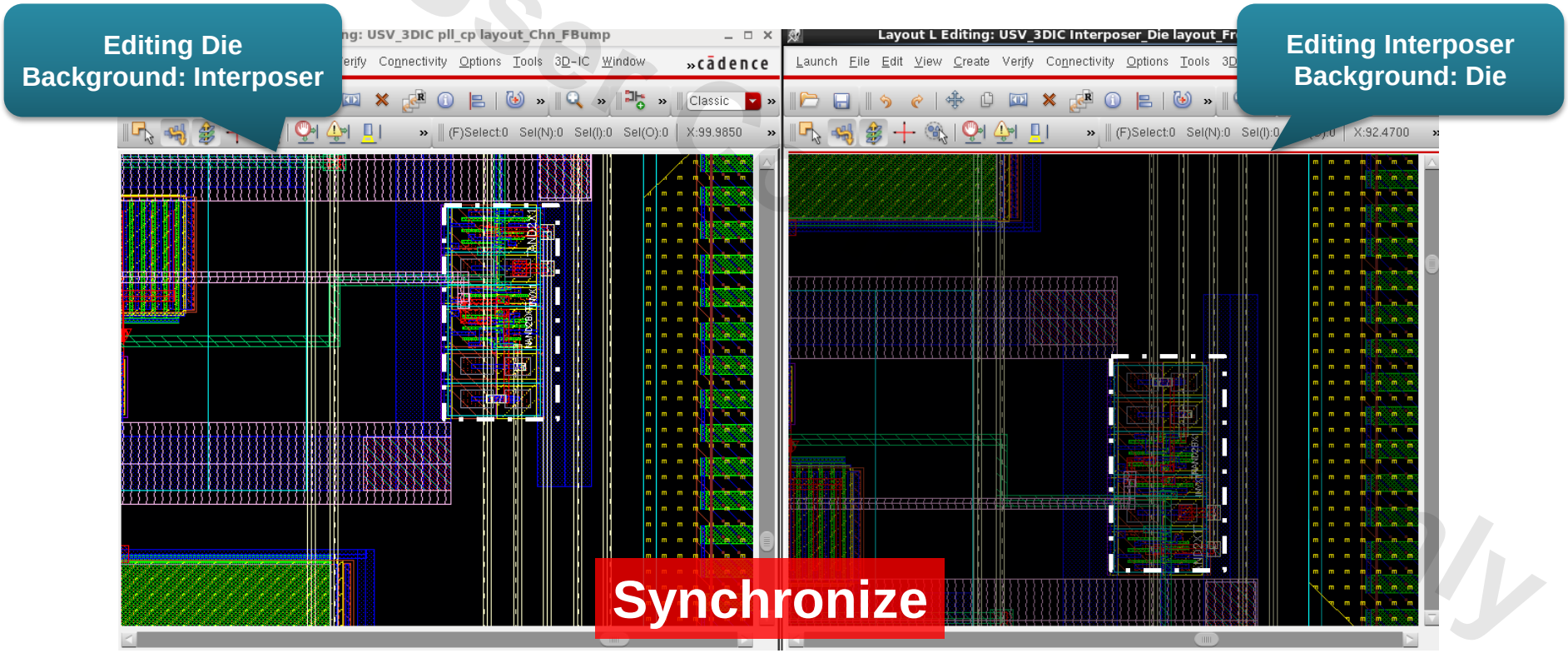
Bump Alignment Checker

- When making manual adjustments to the design, you may accidently move or delete a bump.
- This is integrated with Annotation Browser. So, you can see the list of misaligned bumps there with all relevant info.
- Using the “Check Bump alignment” to prevents this error condition from occurring.



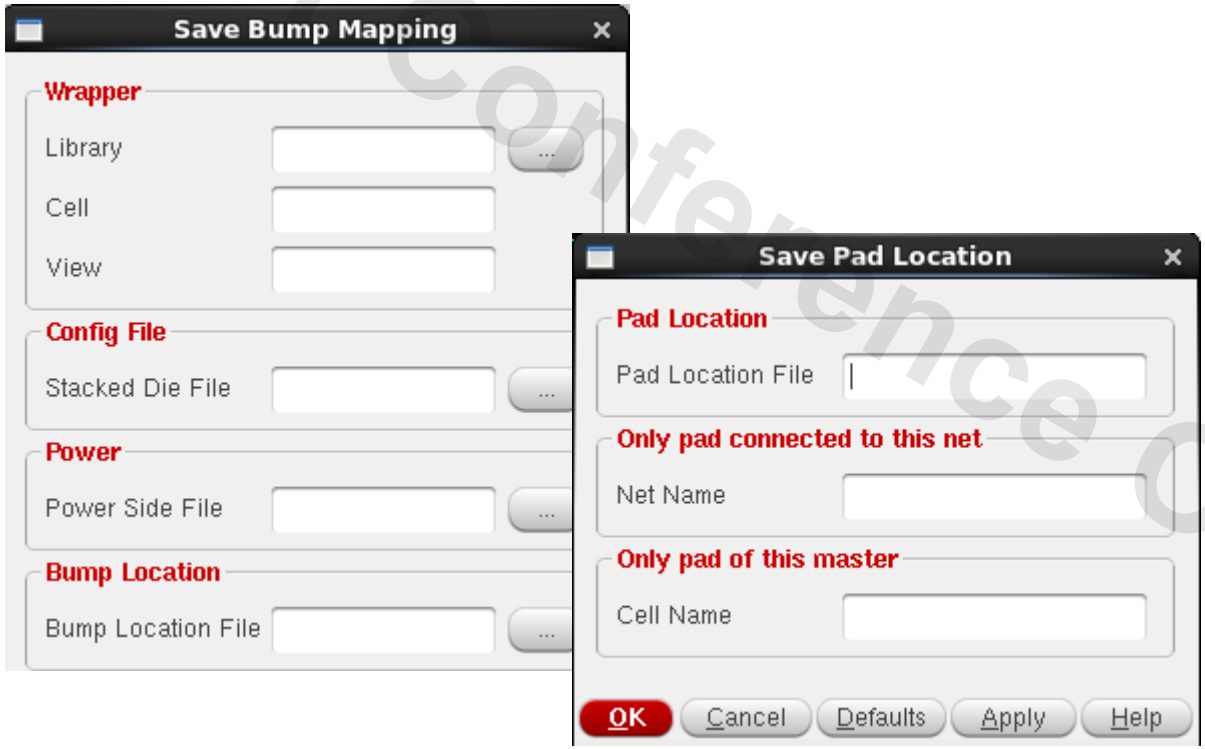
Using Co-Design

- This allows designer to see one die over another at the same time. For example, you can work on the Interposer actively in one window, with the die visible dimly in the background. And in the second window, it is reverse, i.e. the die is active with Interposer in background.



Saving Pad Location and Bump Mapping File

- Pad Locations
  - This file serves as an input for performing the IR drop analysis.
- Bump Mapping
  - This file will serve as an input for performing the IR drop analysis.



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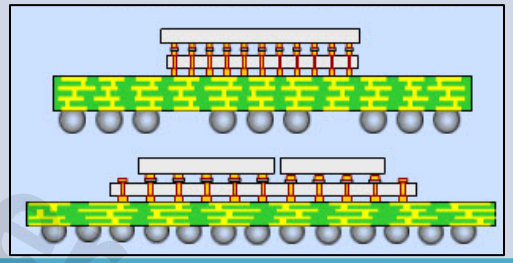
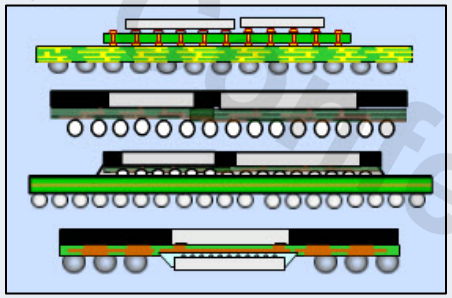
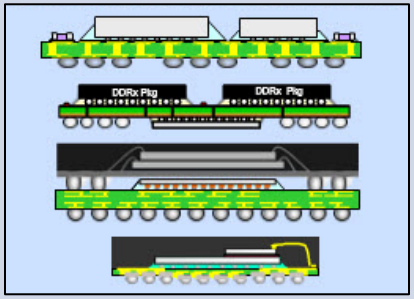
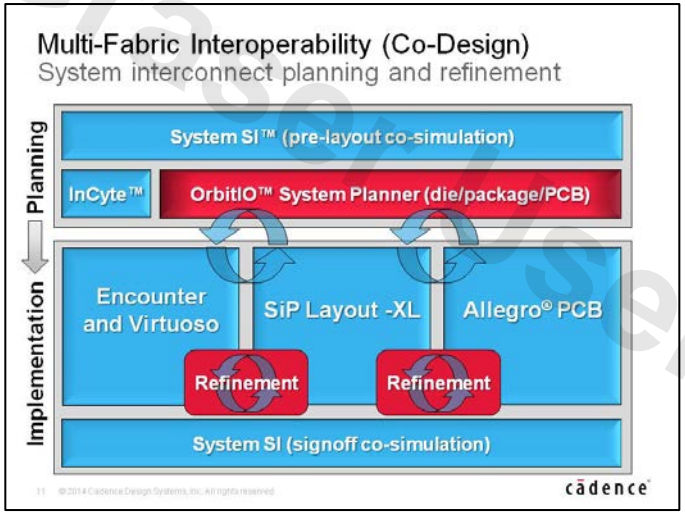
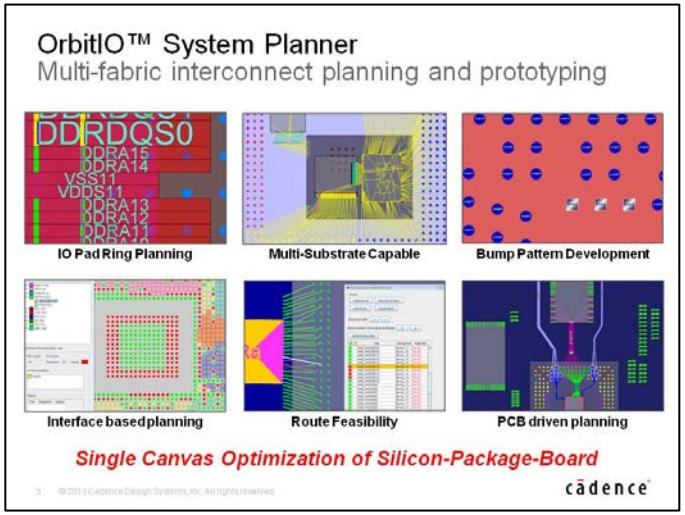
Silicon based interposers Die stacking with TSV		**Encounter / Virtuoso**
Fan out wafer level Organic interposers		**SIP Layout-XL OrbitIO APR**
Conventional laminate build-up technologies		

Technology Enablement – SPB 16.6

Multi-Fabric Planning and Prototyping (Co-Design)



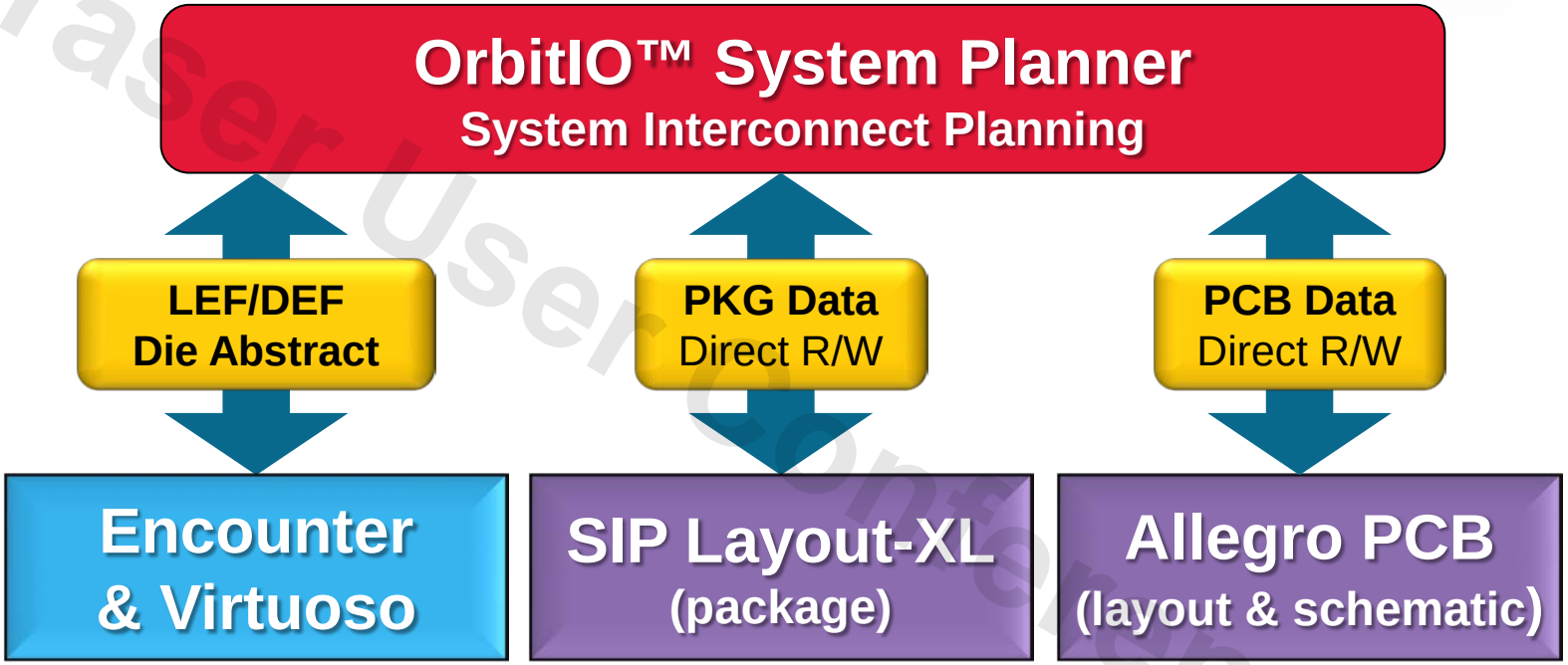


- Comprehensive co-design delivering interoperability across IC, interposer, package, and pcb
  - Rapid convergences across all fabrics
  - Delivering value and efficiency from early planning through implementation
- OrbitIO provides multi-fabric interconnect planning in a single-canvas environment
  - Dynamic full system view and data access
  - Top-down or bottom-up connectivity planning
- Easily plan and communicate design intent (including a route plan) between engineering groups or external design sources

OrbitIO

Technology Enablement – SPB 16.6

Interconnect planning for advanced technologies



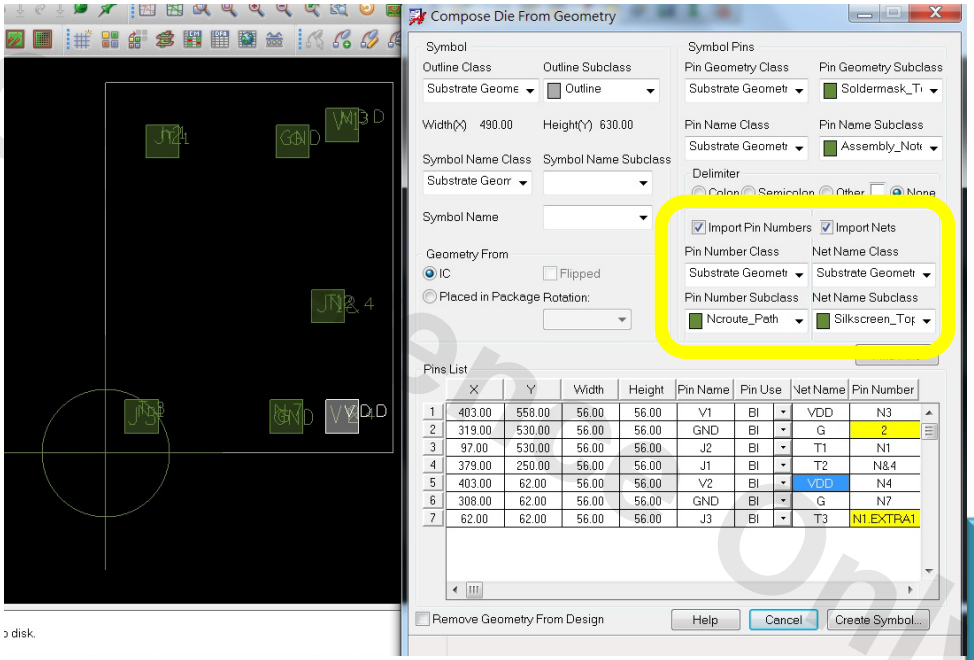
- Efficient planning of the multi-fabric elements between die, package, interposer, and PCB all within a single canvas
- Objective: produce well qualified design definitions ready for implementation

Technology Enablement – SPB 16.6

Wafer/Chip Scale Package Enhancements

Updates to *Compose Die from Geometry* combined with several productized beta features expedite the creation and management of die symbols from external data sources like DXF or GDSII.

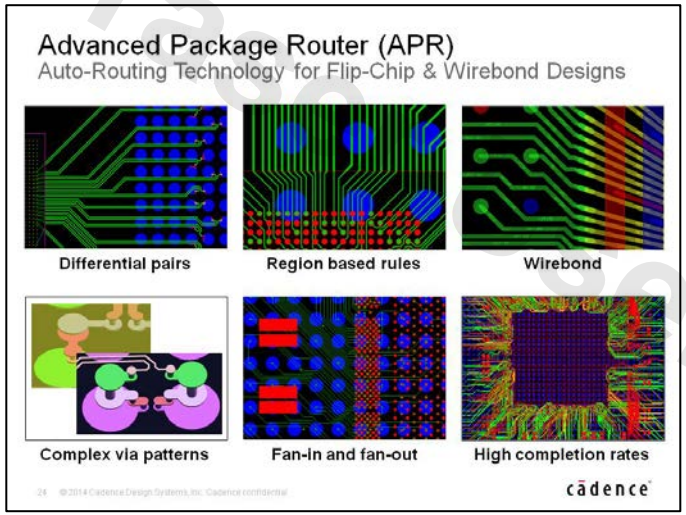
- *Compose Die from Geometry* updated to use additional information.
  - Added mapping for Pin Numbers and Net Names
  - Cross-probe highlight
- Productized commands to ease conversion of geometries into formal packaging content
  - Shape to cline
  - Shape to padstack
  - Shape to via

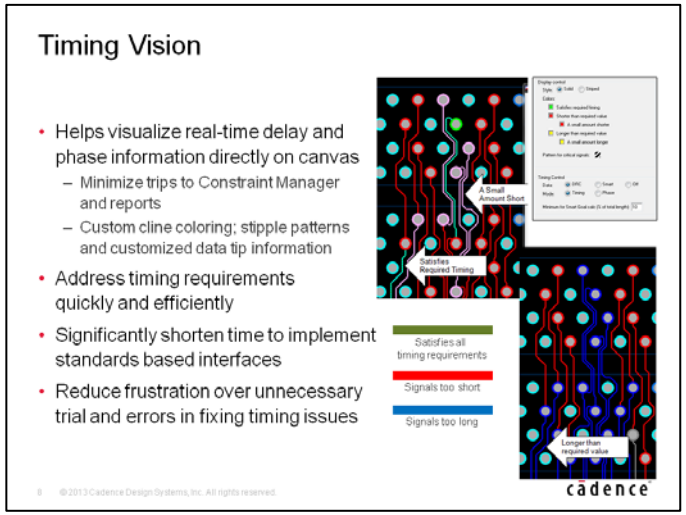


SIP Layout & APD

Technology Enablement – SPB 16.6

High performance routing and optimization





- Advanced Package Router (APR)
  - Sigrity technology to reduce design cycle-time of complex packages
  - High-speed constraint-aware, auto-routing of flip-chip and wirebond designs
- Auto-interactive routing technologies to plan, implement, and optimize high-performance interfaces
  - AiDT – auto-interactive delay tuning
  - AiPT – auto-interactive phase tuning
  - AiBT - auto-interactive breakout
  - Timing vision

Technology Enablement – 2015 and beyond

Overhaul of Layer Stack-Up and Pad Stacks

Layer Stack Overhaul

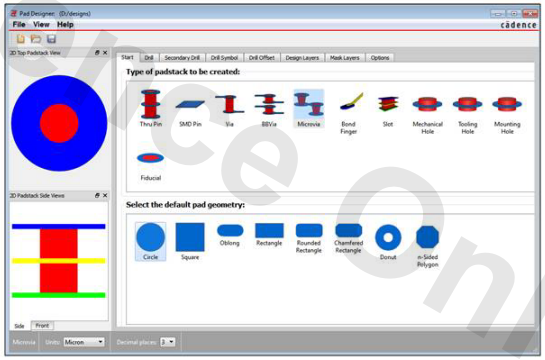
- 'Excel like' usability
- Single cross-section editor
  - Consolidates input sources
  - Detailed view of stack-up construction and drills
  - Embedded component setup
  - IPC2581 stack-up import/export
- Customer layer IDs (3 alphanumeric)
- User-defined columns
- Layer color match
- Expandable column view
- Thickness tolerances

cadence

- New editing environments for layer stack-up and pad stack definitions

Pad Stack Overhaul

- New unified pad editing environment
- Expanded number of shape primitives
- Support complex mask schemes
- Enhanced DRC support related to pads
- Adjacent layer keep-outs
- Numerous other enhancements



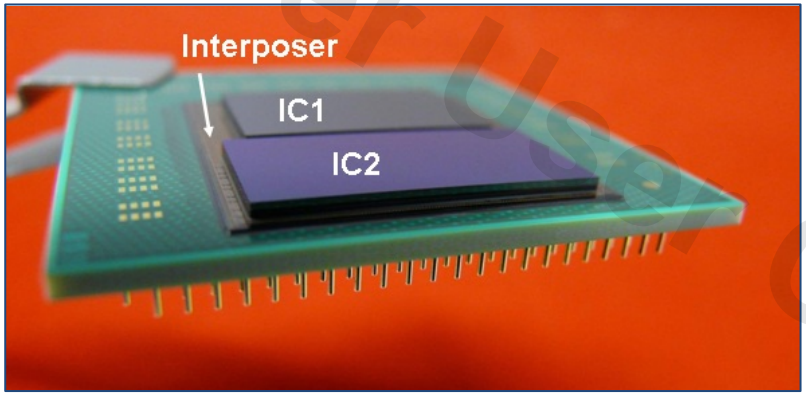
cadence

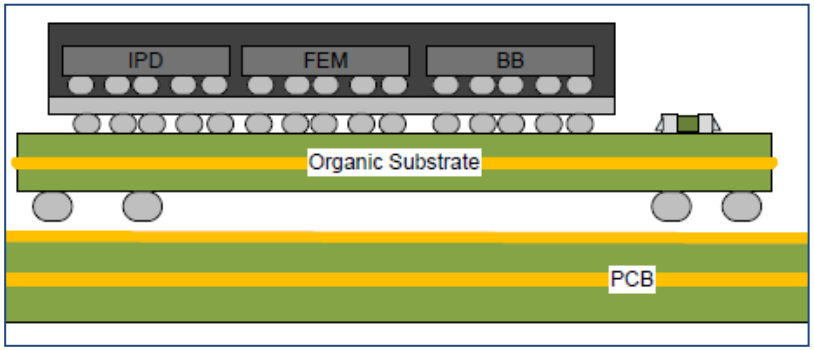
- Enhanced support for embedded die, Cu Pillar and complex via structures

SIP Layout & APD

Technology Enablement – 2015 and Beyond

Enhanced stacked application support

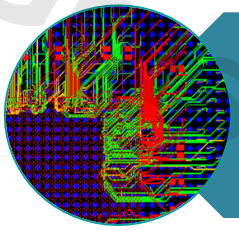




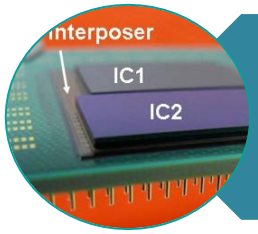
- Interposer support
  - New interposer design object
  - View complete stack-up in one database with ability to edit the individual substrates
- Dual sided pins
  - Pins on both sides of a die
  - Support for 2.5D / 3D
- 3D Viewing enhancements
  - Platform support
  - STEP model creation support

SIP Layout

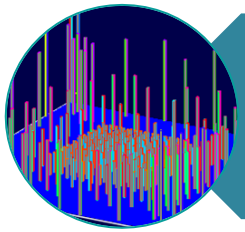
Summary



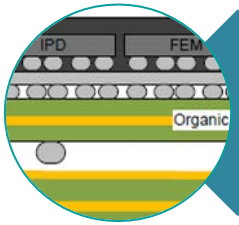
Cadence focuses on making you success



Innovative features to address advanced technologies like interposers, FO-WLP, 2.5/3D



Enhance design efficiency through automation and interoperability



Future directions are influenced by your requirements