USER CONFERENCE Graser 2014 Oct 31 Taipei

Miniaturization-Rigid-Flex Design with Allegro

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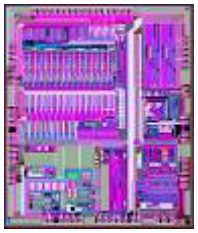
Graser®

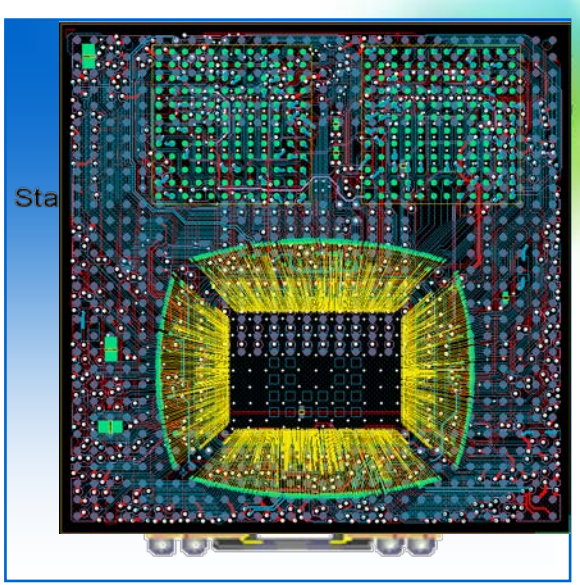
Rigid-Flex Design with Allegro

- Miniaturization
- Design Miniaturization through Rigid-Flex
- Rigid-Flex Design Flow

Miniaturization

Miniaturization





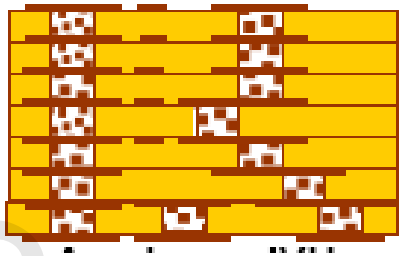
Stacked Die

- SoC – more functional density
- SiP – mixed technologies with memory
- Rigid-Flex circuits

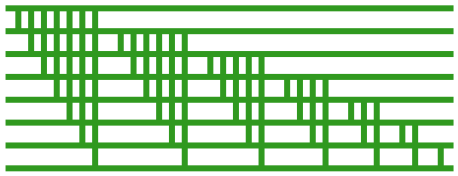
- Large Pin Count Devices
- BGAs with shrinking pin pitches
  - 1.0 mm → 0.8 mm → 0.5 mm
- High Density Interconnect

Design Miniaturization through Build-up Technology

- Complete Build-up
  - ALIVH, PALAP, B2it, …
  - ALIVH (Matsushita owned): All Layer Interstitial Via Hole
  - PALAP (DENSO Consortium) Patterned LAyup Process

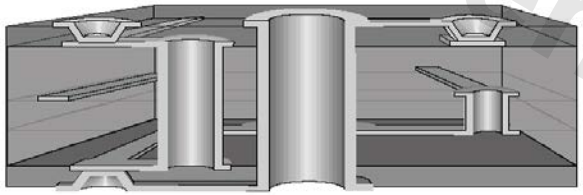


ALIVH

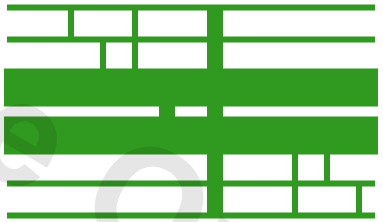


ALIVH – 8 Layers (28 combinations)

- Hybrid approach
  - Build-up with a core



Core+Build-up

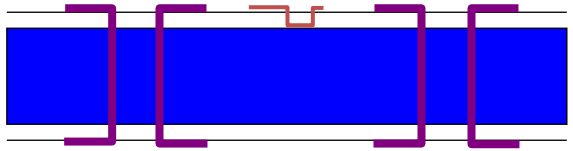


HDI – 2+4+2 (Max 8 comb)

Hybrid Approach

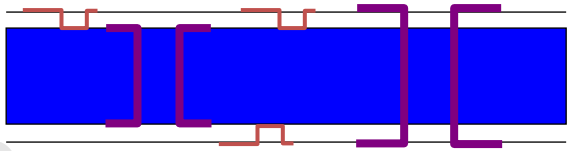
- Type I:
  - 1-C-0 or 1-C-1
  - Through vias and micro vias
  - No buried vias

Type I



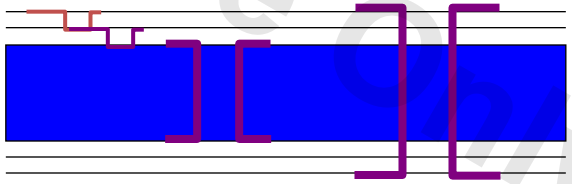
- Type II
  - 1-C-0 or 1-C-1
  - Through and Micro vias
  - Buried vias

Type II



- Type III
  - n-C-n (where n >= 2)
  - Through and Buried vias

Type III

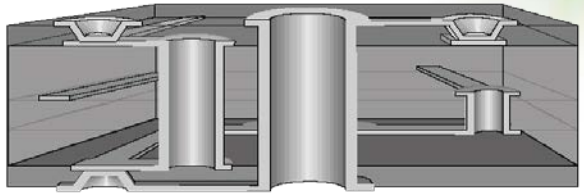


HDI Design Challenges

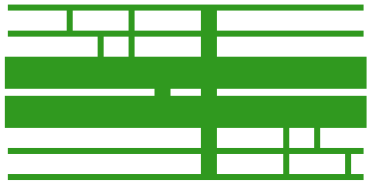
- Signal Integrity, Crosstalk, Power Delivery, SSO

- Physical Design
  - Fanout
  - Micro vs. Mechanically Drilled via
  - New Class of rules
    - Drill to Metal, Drill to Drill
    - Same Net DRCs
    - Via stack-up rules
  - Interactive etch editing
  - Display
  - Manufacturing prep

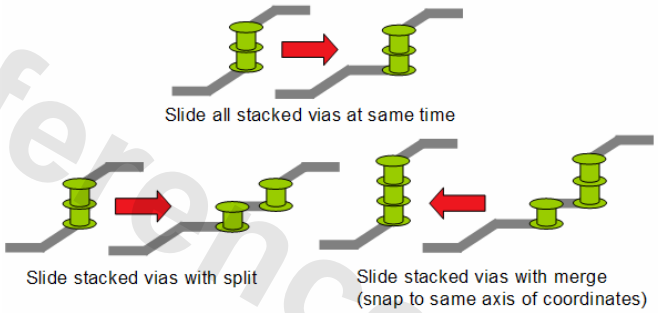
- Package-PCB Co-Design

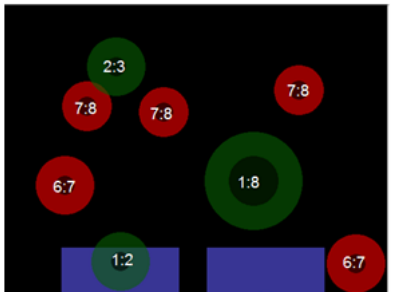


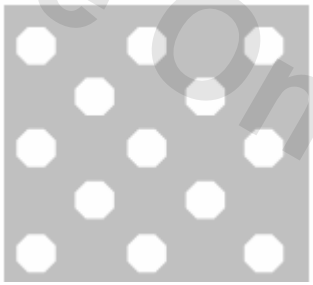
Core+Build-up
Hybrid approach



HDI – 2+4+2 (Max 8 comb)

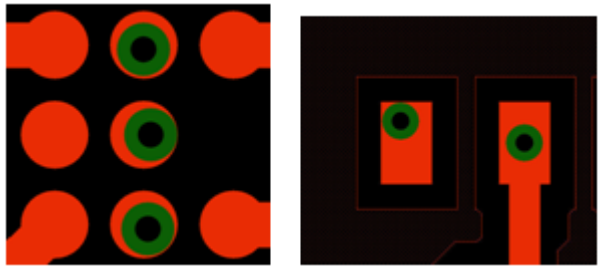




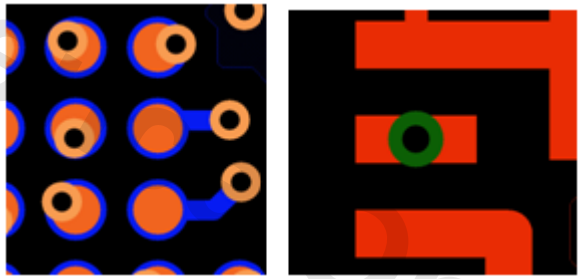


Fanout
Via in Pad

- Dense BGAs with shrinking pin pitch requires carefully throughout fanout



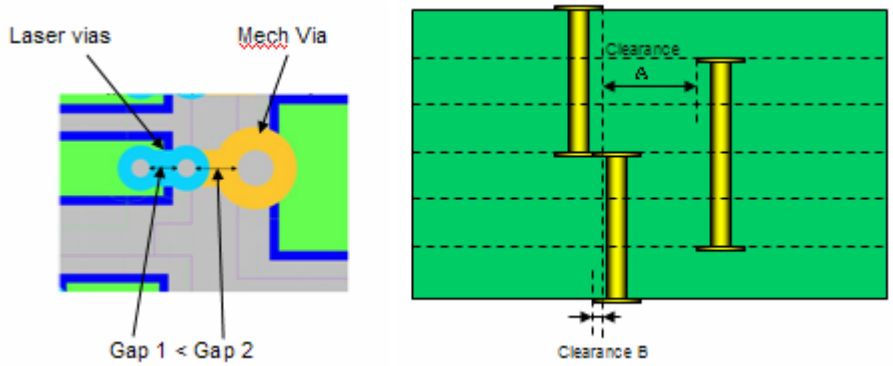
- Users moving to via-in-pad for two reasons
  - Better Power Delivery system performance
  - Better space utilization

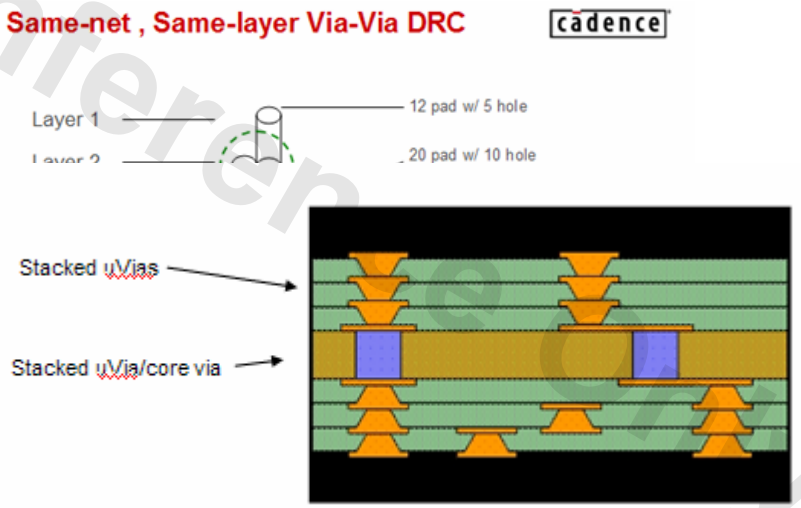


- Floating via
  - Complete via must be inside the SMD pad
  - Via Center must be inside the SMD pad
- Override by component instance

New Via Type, Rules and Controls Needed

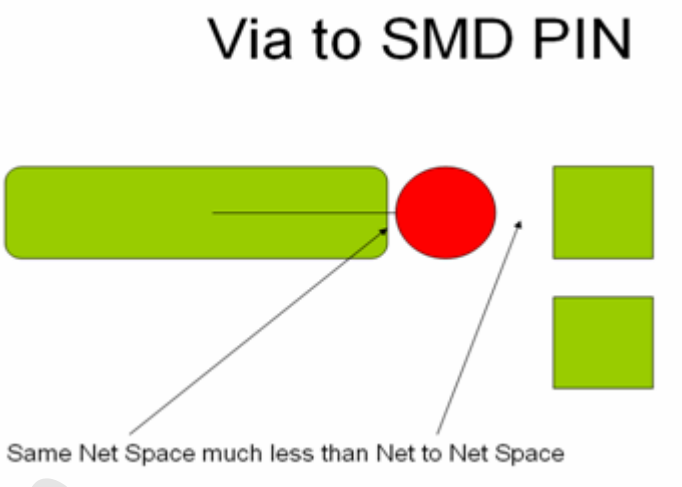
- System must be able to differentiate microvia from mechanically drilled vias
  - Support same net and net-net DRC conditions
- New rules and controls
  - Microvia spacing to all other etch elements
  - Controls for via tangency
  - Rules for pad overlap
  - Support rules for via stacking



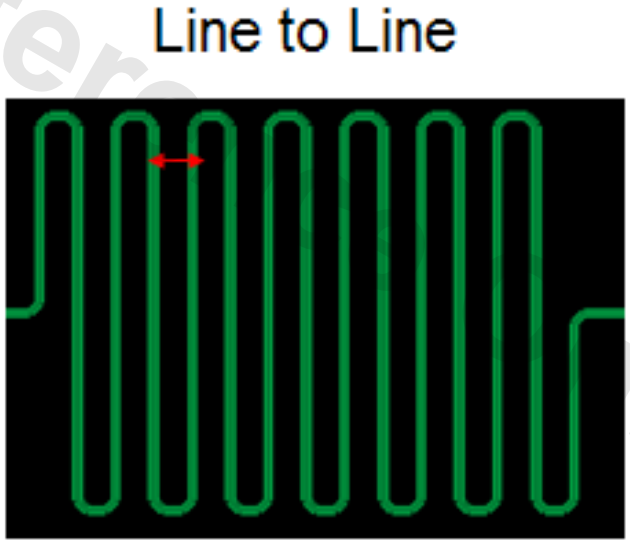


Same Net DRC

- Difference Same Net from Net to Net Spacing DRCs



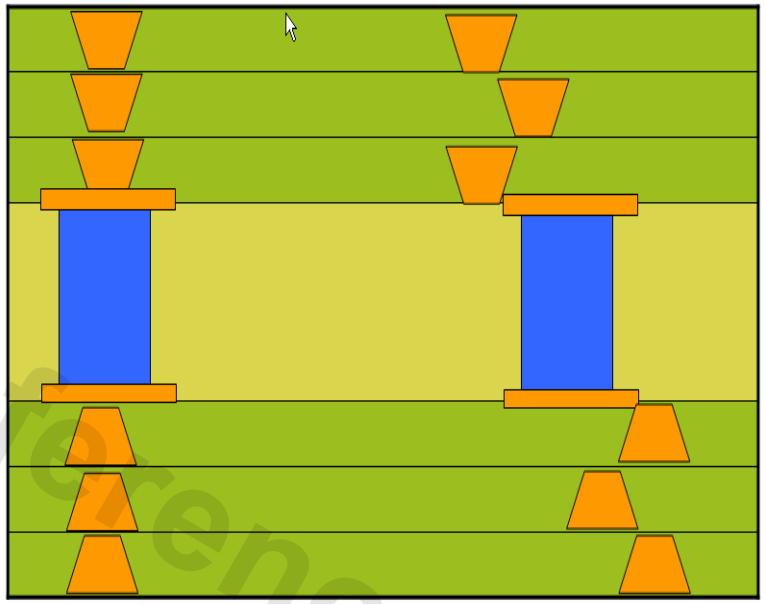
- Same Net values are typically less than net-net
  - (different net) Pin to Via = 6 mils
  - Same Net Pin to Via = 3 mils



- Different for reporting same net DRC error (Display, reports)

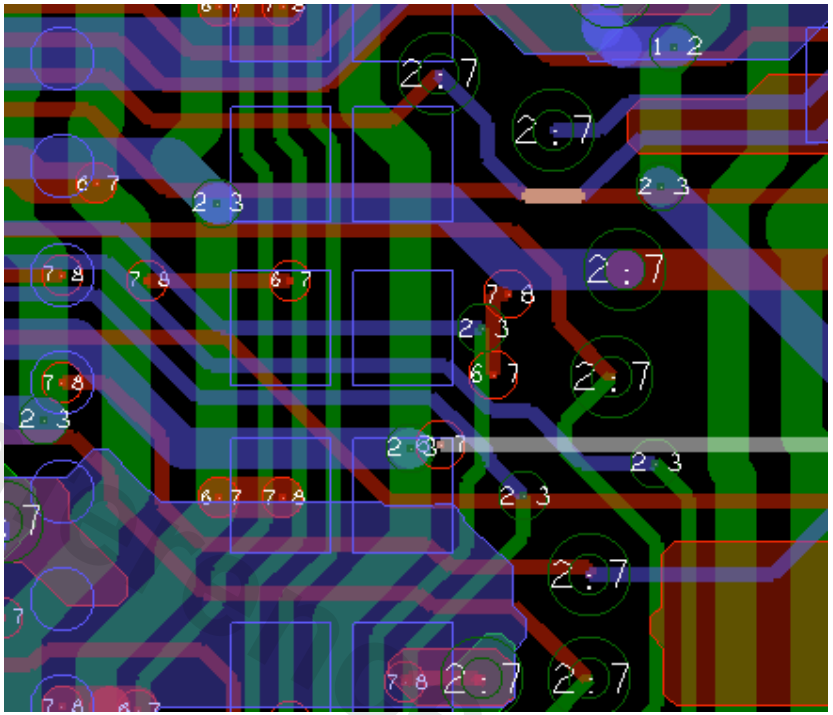
Adding uVia Structures

- Optimize the process of adding micro-vias and core-vias based on user defined rules
- Traverse multiple layers with as few clicks as possible
- Treat structure as group entity
- Semi–interactive model for staggered pattern



Via Span Display

- Designs that utilize B/B vias present a problem for a user in trying to determine what layers a via connects to
- Color coding is currently used but on designs with a high concentration of via types, mapping colors to layer spans becomes difficult to remember
- The additional nomenclature within the bounds of the via pad will help aid in the determination of the span
- Allow users to control size, color for the nomenclature



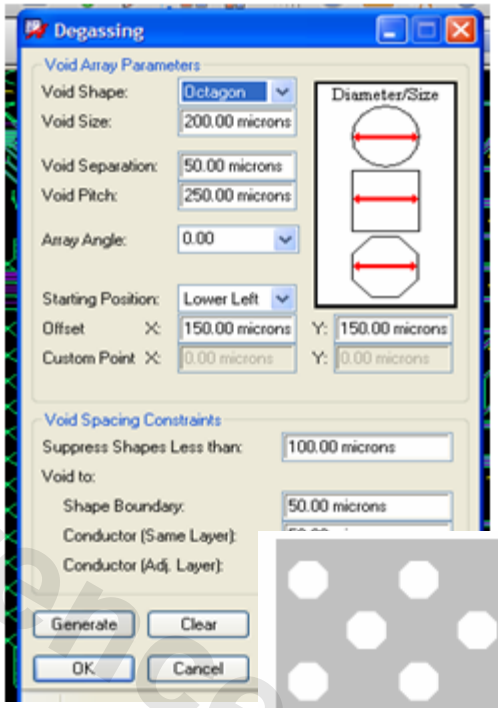
Via Hole Plugging

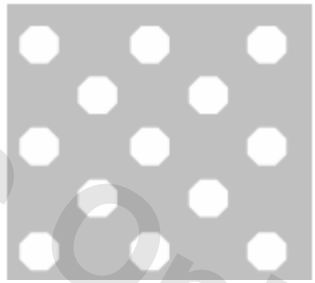
- Via hole plugging/filling becomes standard on most high density boards
- Via holes can be plugged with conductive or non conductive material
- Thru vias are typically plugged from one side of the board. They assist in creating a tight vacuum for test fixtures
- Vias in Pad can be filled from either side of the board, usually with a conductive paste

Degassing

- Perforation of power and shielding shapes with a grid of voids, with the intent of gaining additional adhesion and allow gases to escape between layers during the manufacturing process of the package

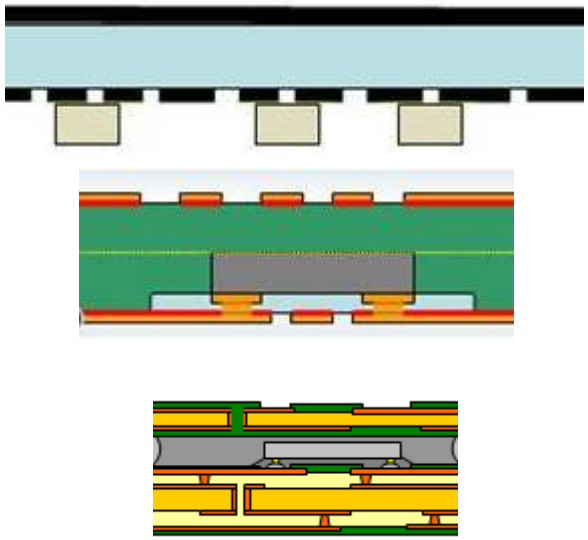
- Used to prevent build-up layer de-lamination

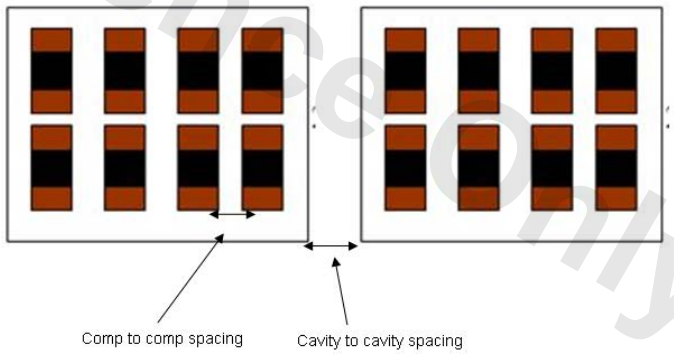




Miniaturization through Embedded Components

- Specify layers for embedding packaged components
- New DRCs for embedded devices
- Constraint-driven place and route
  - Move components to inner layers
  - Support for connecting to devices on inner layers
- Manufacturing outputs for layers with embedded devices

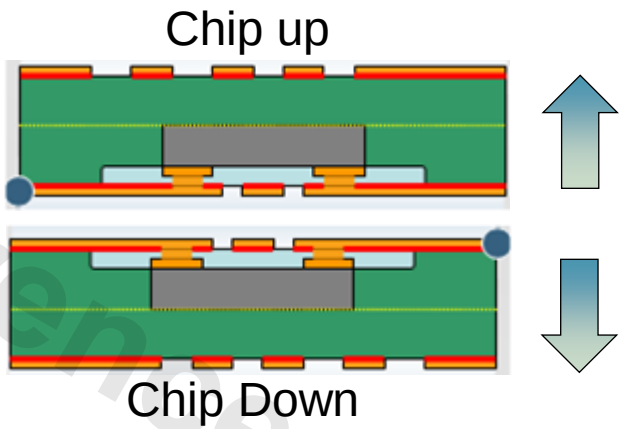




Embedded Component Design

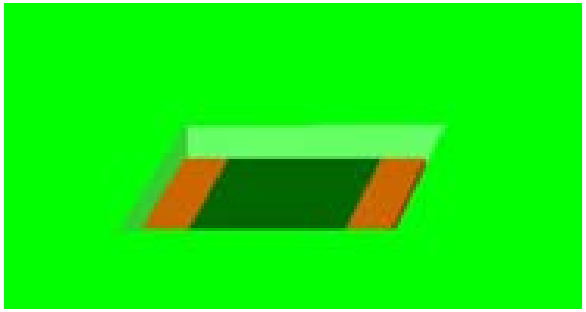
- Front-end driven
  - “Embed required” (hard) or “embed optional” (soft)
  - Ensures only qualified components get embedded
  - Alt symbol support
  - Backend to support symbol instance overrides

- PCB design implementation
  - Stack-up driven (chip-up, chip-down)
  - Cavity support
  - Package geometry support on internal layers
  - DRC
    - Comp to comp
    - Comp to cavity
    - Height within cavity
  - Router integration
  - Manufacturing output



Embedded Components in a Cavity

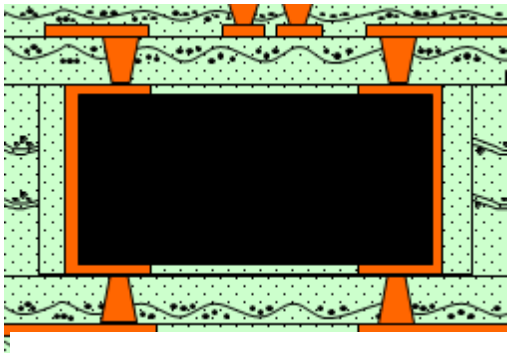
- Package symbol driven
  - New class “Cavity Outline”
  - Legacy place bound used as fallback
  - Keep-out properties



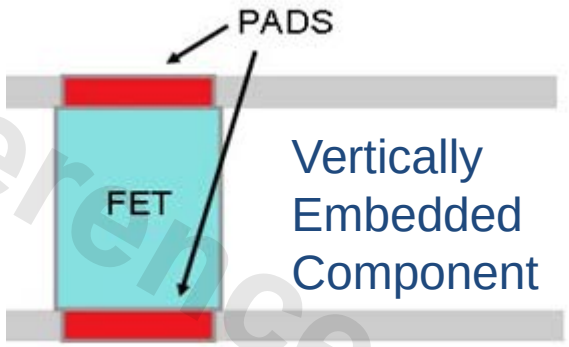
- User-defined cavities
  - Manually entered
  - Can span multiple layers
  - Represents as dynamic fill
    - Merge capability
  - Checks under consideration
    - Max cavity area
    - Max comps within cavity

Advanced Miniaturization Techniques

- Dual-sided components



- Vertical components



- Support for embedding in dielectric on 2-layer boards

Develop differentiated products

Design Miniaturization through Rigid-Flex

Rigid-Flex
Necessary for Products in Many Market Segments

- Consumer electronics
- Mil/Aero
- Medical
- Automotive
- …

Allegro Allows Multiple Board Outlines for Rigid or Flex Sections

Well this is one of the reasons why Motorola Mobile Devices switched to **Cadence Allegro** 3 years ago. Allegro allows multiple outlines like flex outlines or rigid outlines, external soldermask layers and internal full or partial coverlay layers and so on...

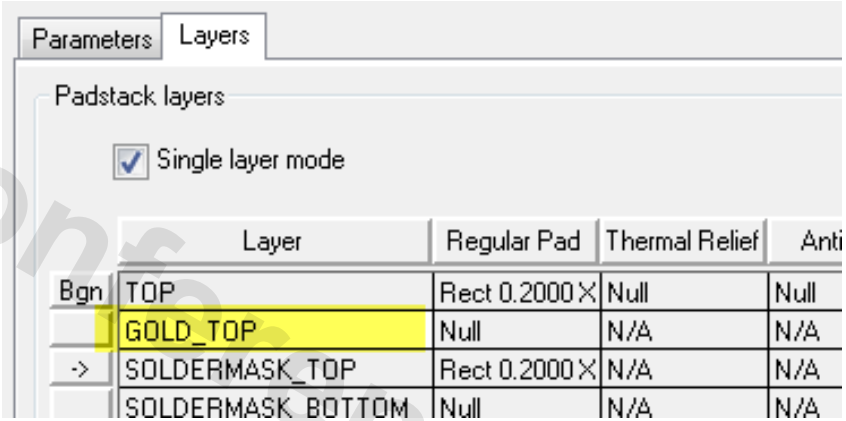
Philippe Gleizes
Flex Circuit Design Manager
Motorola Mobile Devices
600 North U.S. Highway 45
Libertyville, IL 60048

http://forums.mugweb.org/showflat.php?Cat=&Board=ExpeditionRE&Number=4390&Searchpage=1&Main=4382&Words=+Dieseldog&topic=&Search=true

- "Motorola adopts Allegro for Flex Design capability"
- This was a limitation of our competition

Custom Pad Definitions for Rigid-Flex Layers

- Allegro PCB Editor allows up to 16 User Defined layers can be added to the padstack definition
  - Plug
  - Cap
  - Gold

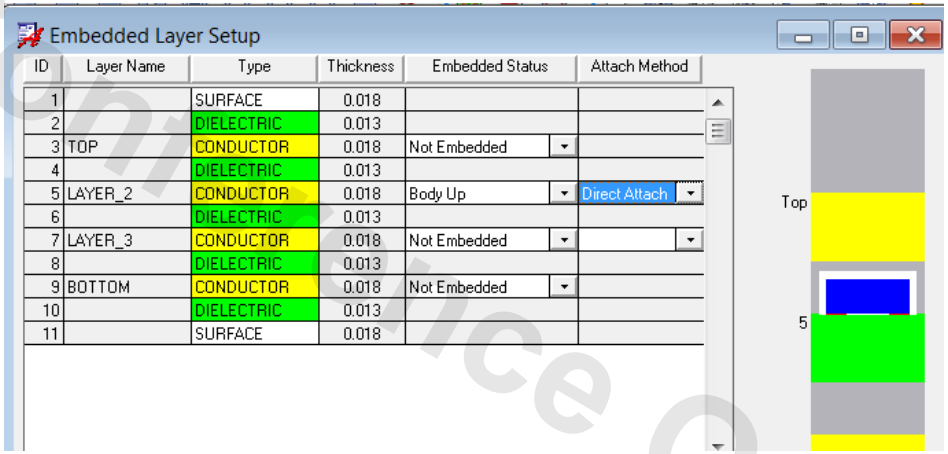


- Plans to increase to 32 in new release

Place Components Directly on Flex Layers

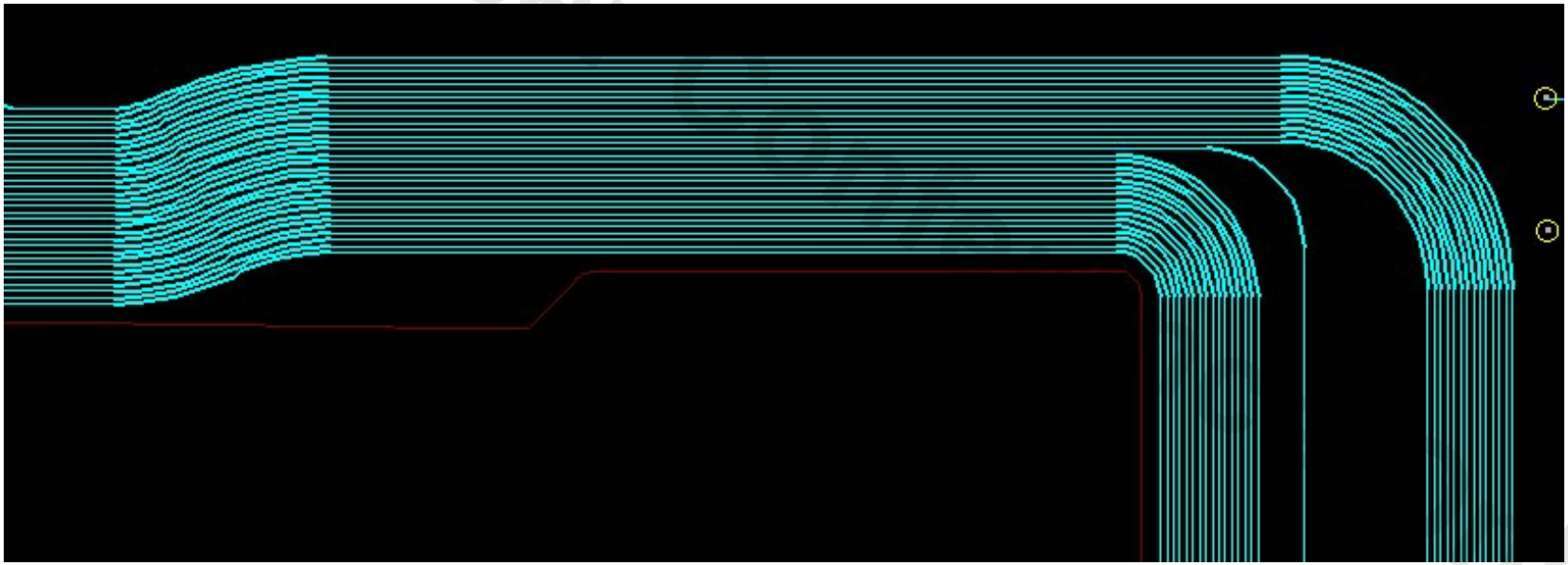
- No special pad editing or complicated work-arounds required with PCB Miniaturization Option

- Drop component to layer defined as “flex” using embedded component functionality



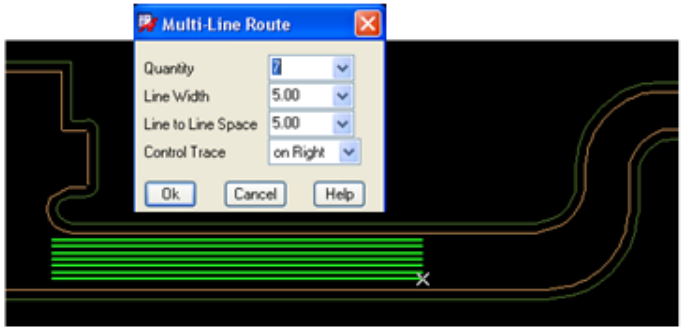
Fast Interconnect Routing on Flex

- Curved Corners
  - Support in both Add Connect and Slide functions

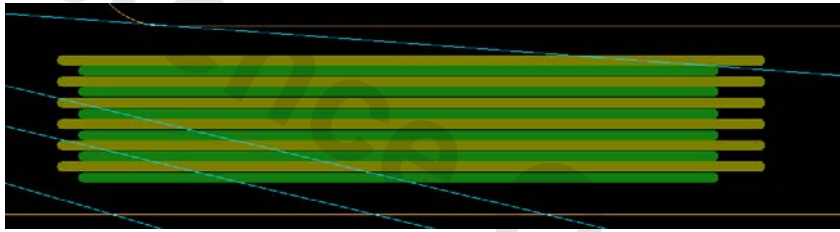


Multi-line Flex Router Interconnect Flow Planning

- Multi-line Flex router permits users to quickly add ‘trunk of bus’ for real estate planning
  - Includes line of different width (guard trace/signals)
  - “Contour locking” (lock onto guard trace or route keep-in area)

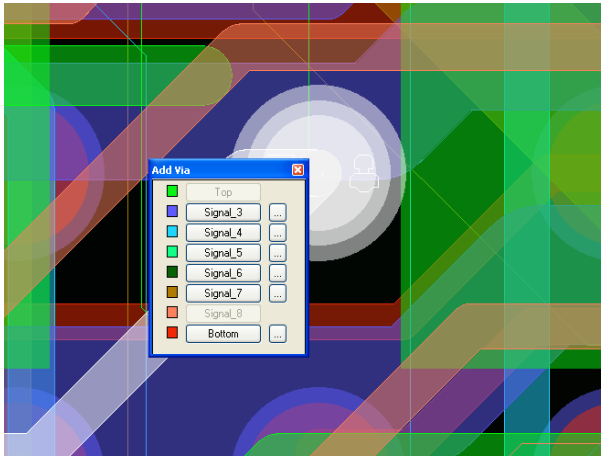


- User configurable for maximum productivity
  - Contour lock option
  - Arc option
  - User defines line and space
  - Once satisfied, connects the end points to their destination pins
  - Effective in preventing “I-Beam” routing on Flex
    - I-Beam construction increases stiffness through bend areas of flex.

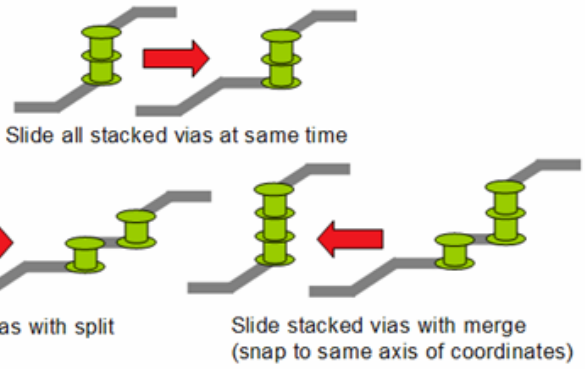


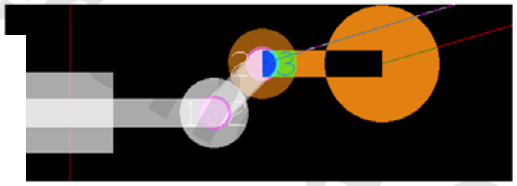
Best in Class Support for HDI Routing, DRC

- Staggered vias
- Stacked vias
- Inset vias
- Any Layer via
- Via in pad
- Via labels
- NC Drill automation for all HDI via combinations

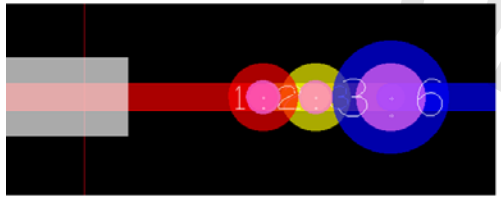


Adding of stacked vias used “working layer model”





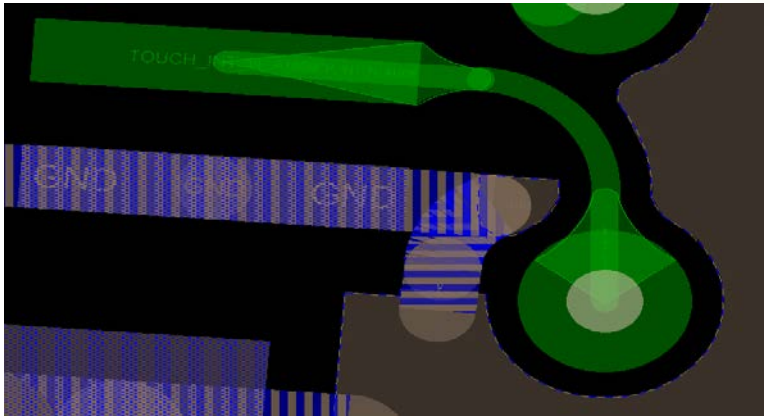
Adding staggered vias



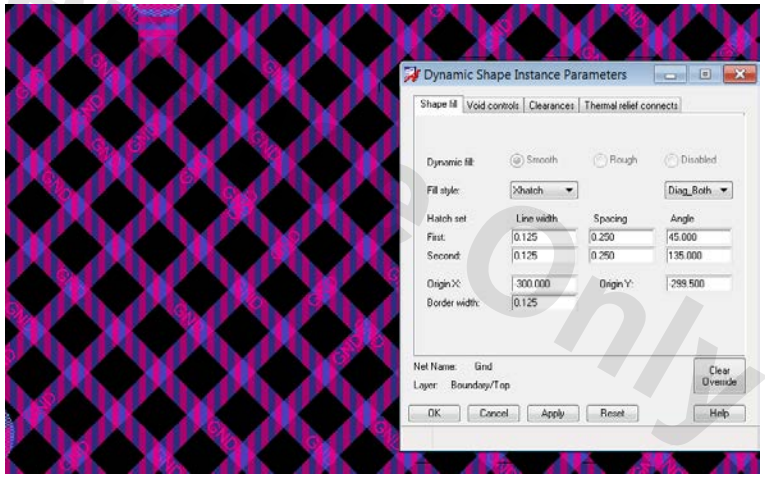
Adding Inset vias

Fillets and Cross Hatch Improve Reliability, Flexibility

- Fillets or teardrops
  - increases pad area
  - distribute stresses evenly at the junction
  - Straight or curved fillets
  - Dynamic option: Add or delete as your route into pin or via

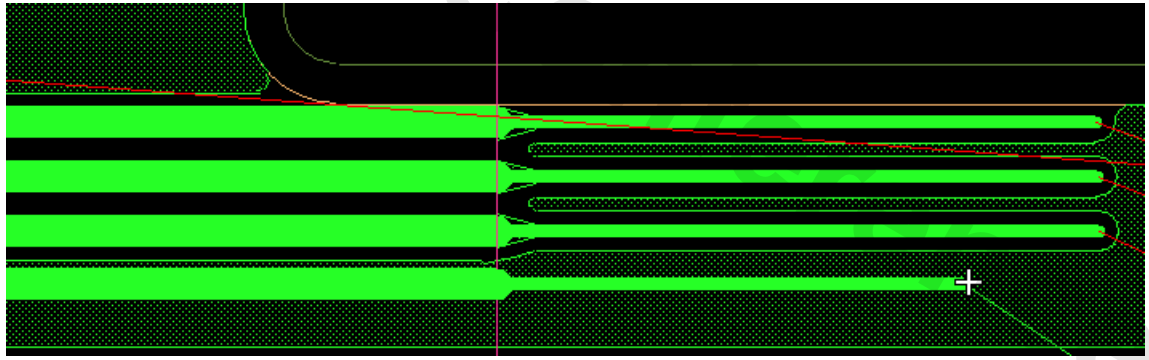


- Cross-Hatch shapes are used to decrease weight and increase flexibility
  - Allegro offers both “Static” and “Dynamic” fill options



Shape Based Fillet to “Taper” Line Width

- Shape based fillet designed to “taper” line width changes along route path
  - Automatically added at the point of a line width change



Rigid-Flex Design Flow

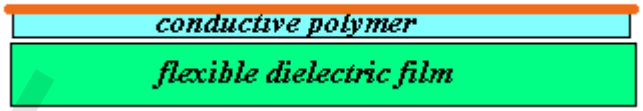
Rigid-Flex Design Flow

- Flexible Circuit Technology
- Material Used for Flex/Rigid-Flex Design
- Board Outline
- Design Guidelines for Flex Circuits

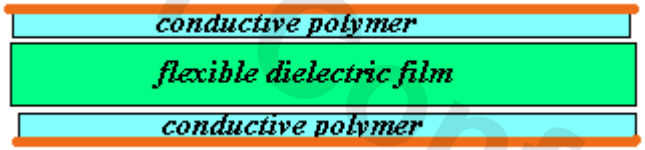
Flexible Circuit Technology

Flex circuits

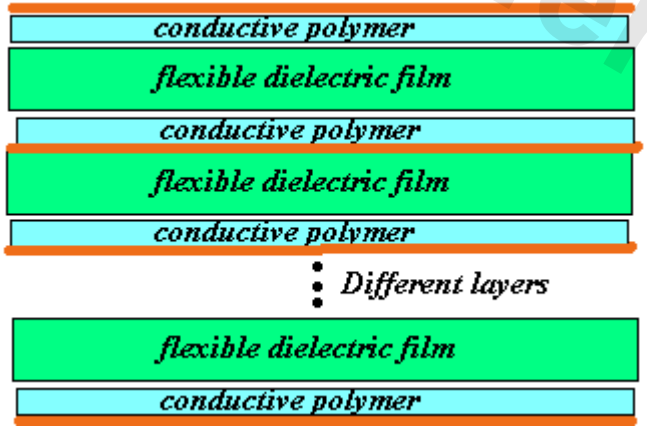
- Single layer



- Double layer

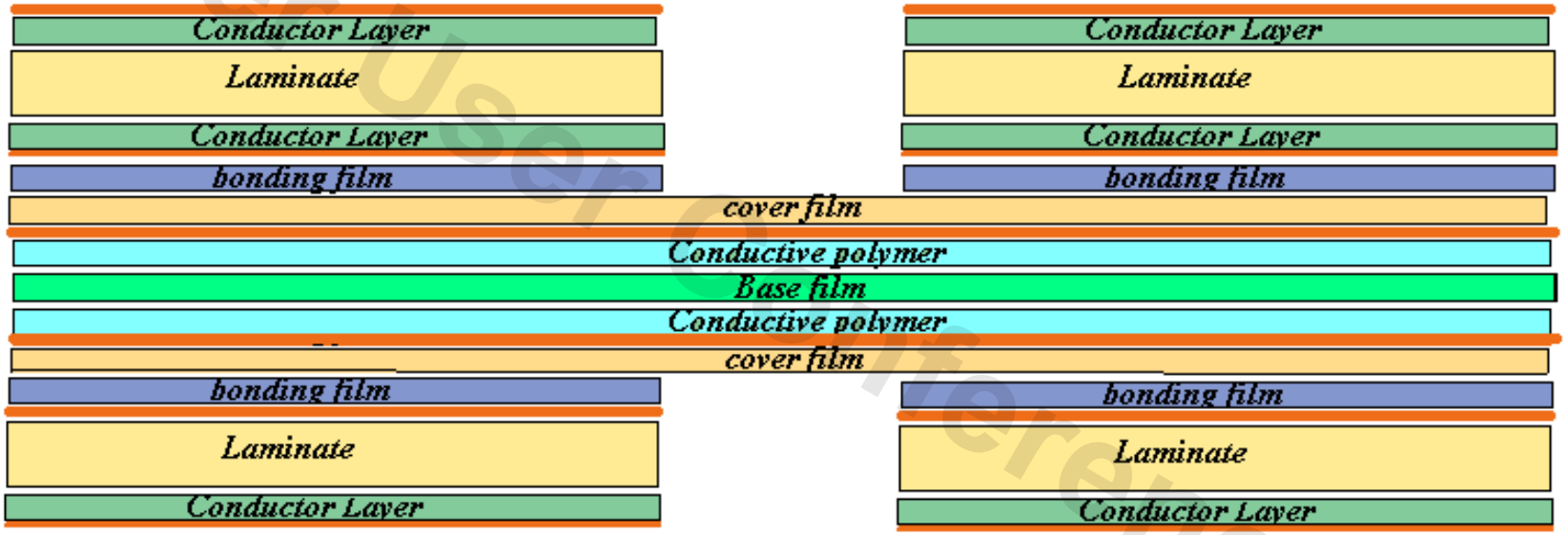


- Multi layer



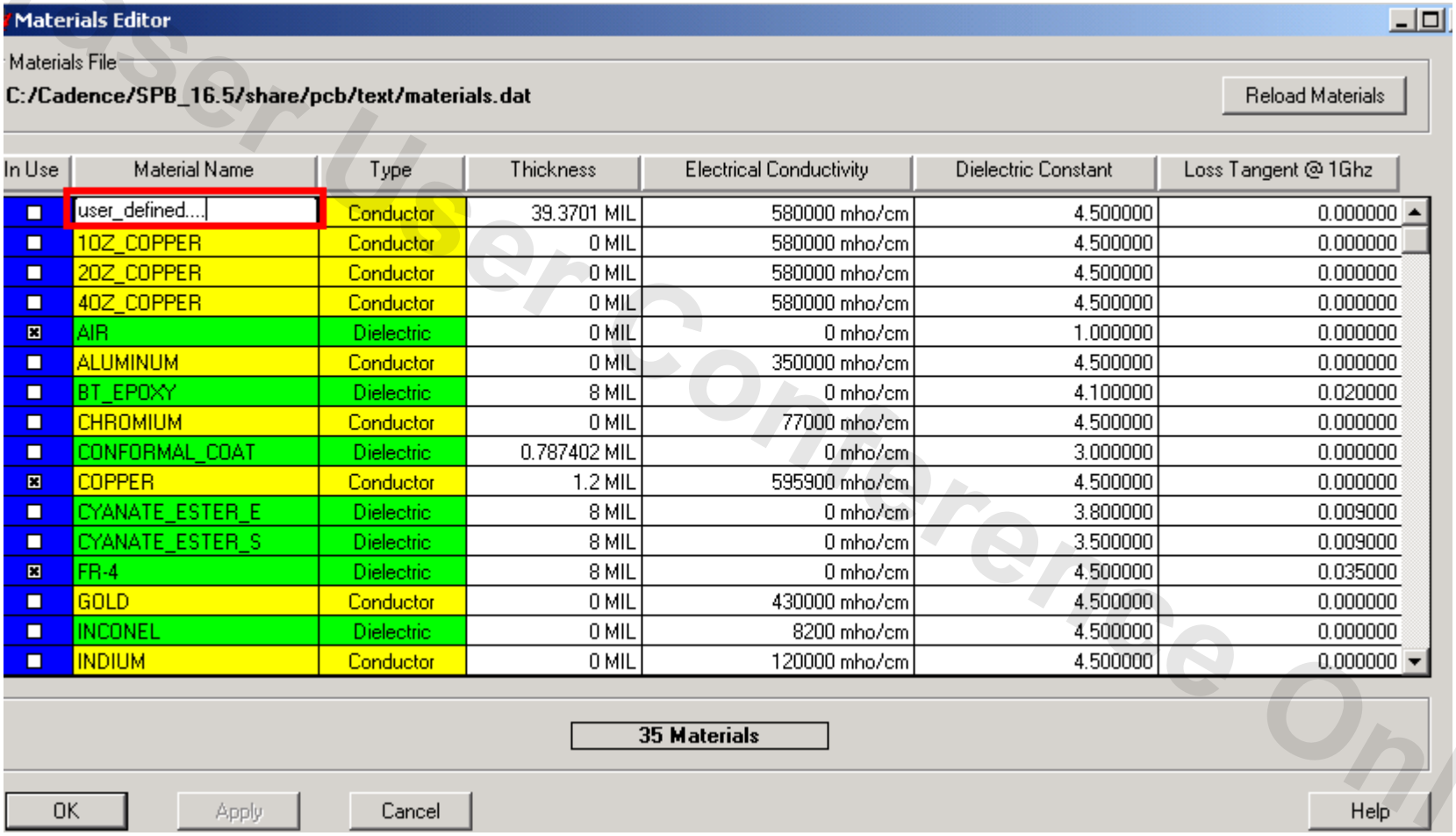
Flexible Circuit Technology

Rigid flex



- This structure is combination of flex circuits placed on rigid as well as on flexible substrates. These are laminated together into a single structure

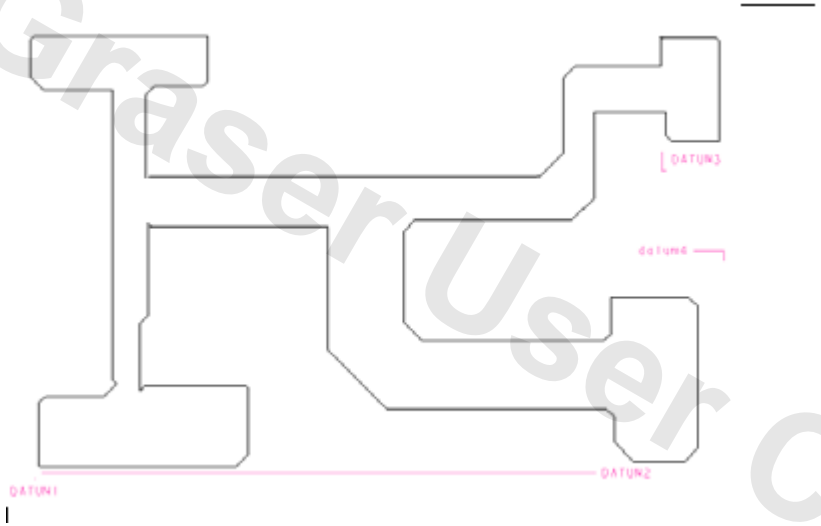
Material Used for Flex/Rigid-Flex Design



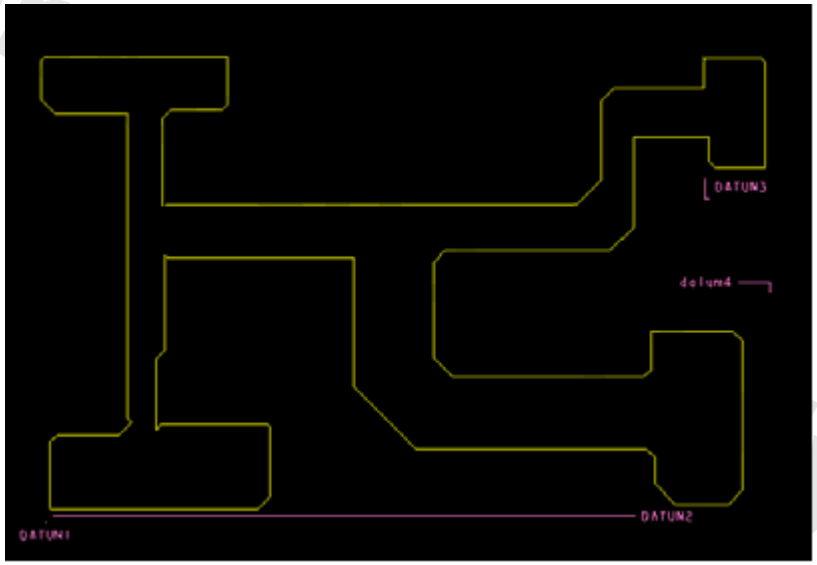
In Use	Material Name	Type	Thickness	Electrical Conductivity	Dielectric Constant	Loss Tangent @ 1Ghz
☐	user_defined....	Conductor	39.3701 MIL	580000 mho/cm	4.500000	0.000000
☐	1OZ_COPPER	Conductor	0 MIL	580000 mho/cm	4.500000	0.000000
☐	2OZ_COPPER	Conductor	0 MIL	580000 mho/cm	4.500000	0.000000
☐	4OZ_COPPER	Conductor	0 MIL	580000 mho/cm	4.500000	0.000000
☒	AIR	Dielectric	0 MIL	0 mho/cm	1.000000	0.000000
☐	ALUMINUM	Conductor	0 MIL	350000 mho/cm	4.500000	0.000000
☐	BT_EPOXY	Dielectric	8 MIL	0 mho/cm	4.100000	0.020000
☐	CHROMIUM	Conductor	0 MIL	77000 mho/cm	4.500000	0.000000
☐	CONFORMAL_COAT	Dielectric	0.787402 MIL	0 mho/cm	3.000000	0.000000
☒	COPPER	Conductor	1.2 MIL	595900 mho/cm	4.500000	0.000000
☐	CYANATE_ESTER_E	Dielectric	8 MIL	0 mho/cm	3.800000	0.009000
☐	CYANATE_ESTER_S	Dielectric	8 MIL	0 mho/cm	3.500000	0.009000
☒	FR-4	Dielectric	8 MIL	0 mho/cm	4.500000	0.035000
☐	GOLD	Conductor	0 MIL	430000 mho/cm	4.500000	0.000000
☐	INCONEL	Dielectric	0 MIL	8200 mho/cm	4.500000	0.000000
☐	INDIUM	Conductor	0 MIL	120000 mho/cm	4.500000	0.000000

Material Editor Window

Board Outline

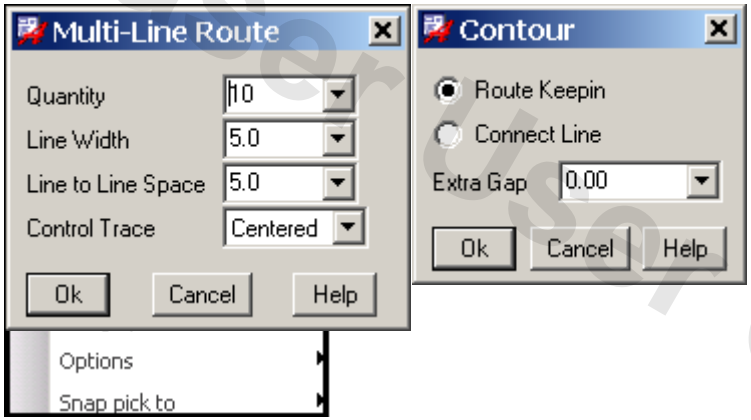


- Allegro PCB Editor can import IDX, DXF, and IDF files that contain the outline, cutouts, and other mechanical features that are critical to the design.



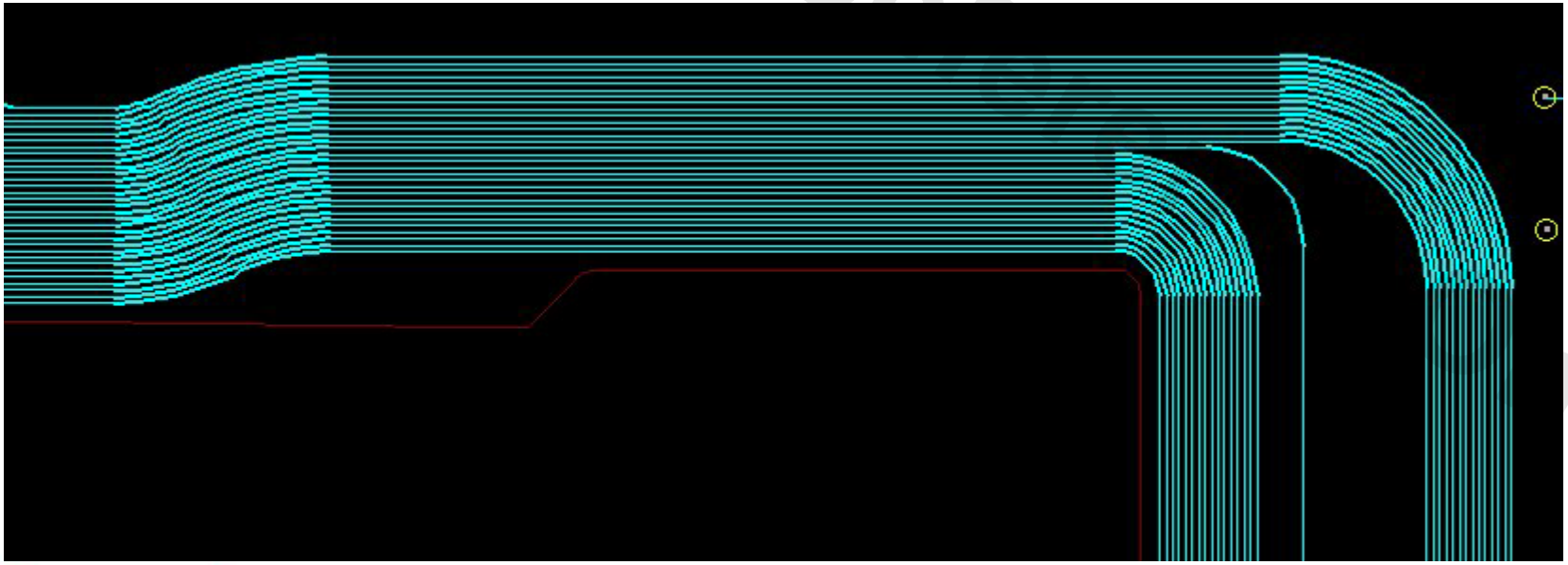
Design Guidelines for Flex Circuits

Conductor Routing



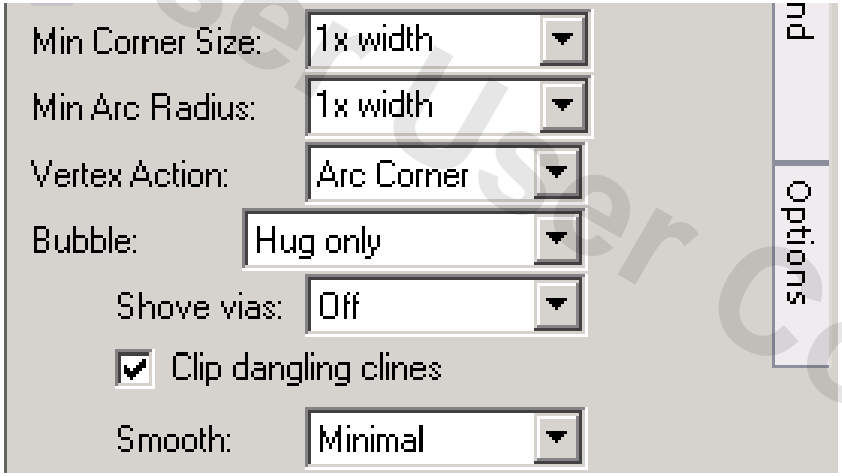
a. Multiline Routing

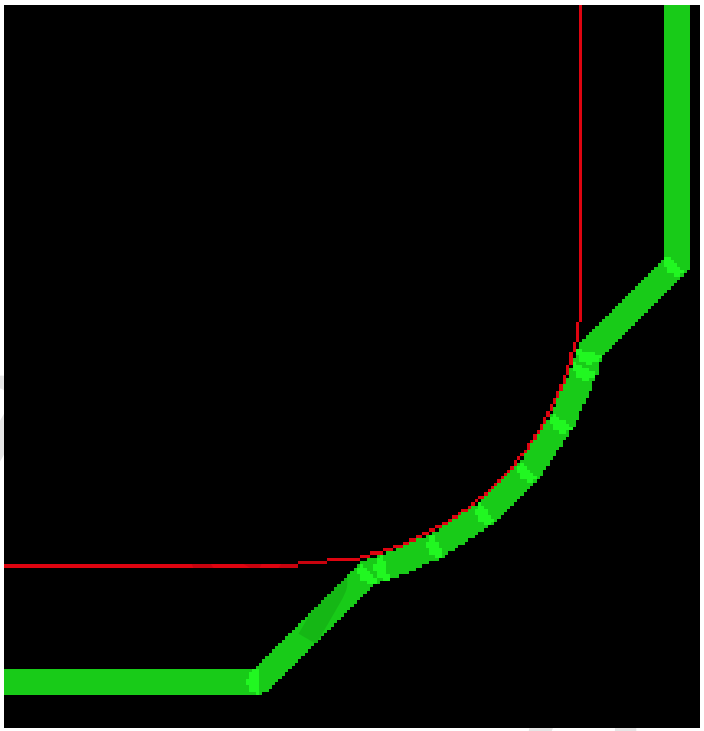
b. Hug-Contour



Design Guidelines for Flex Circuits

Conductor Routing

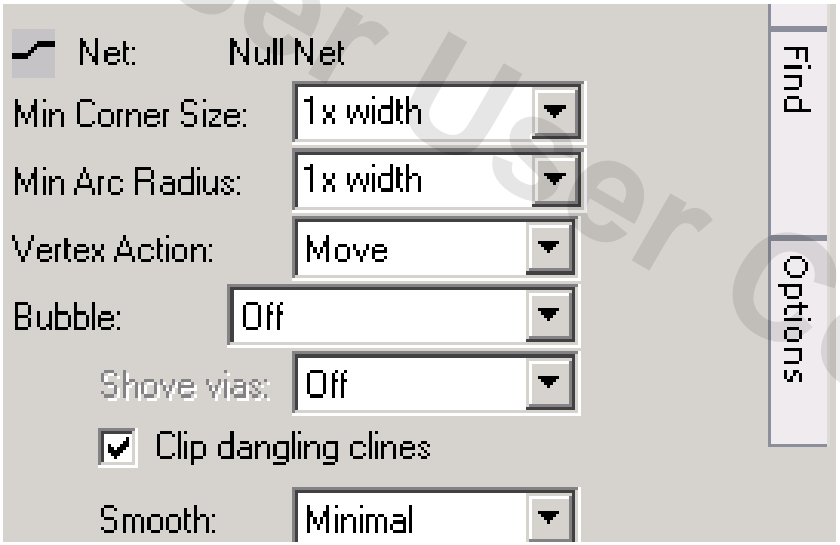


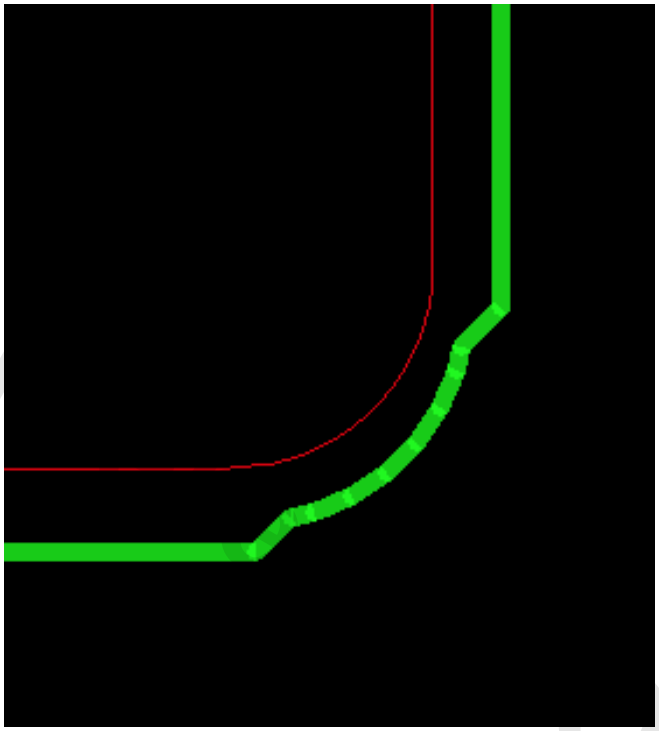


Arc Editing option with vertex action as Arc Corner

Design Guidelines for Flex Circuits

Conductor Routing



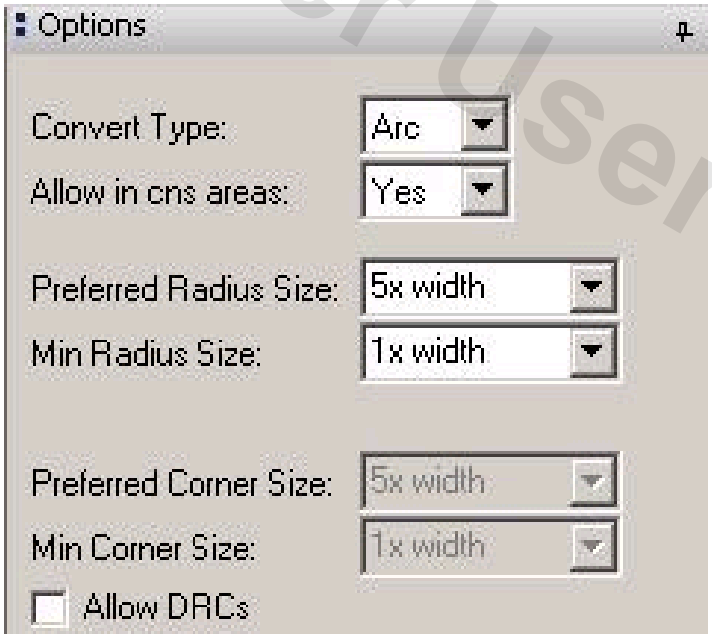


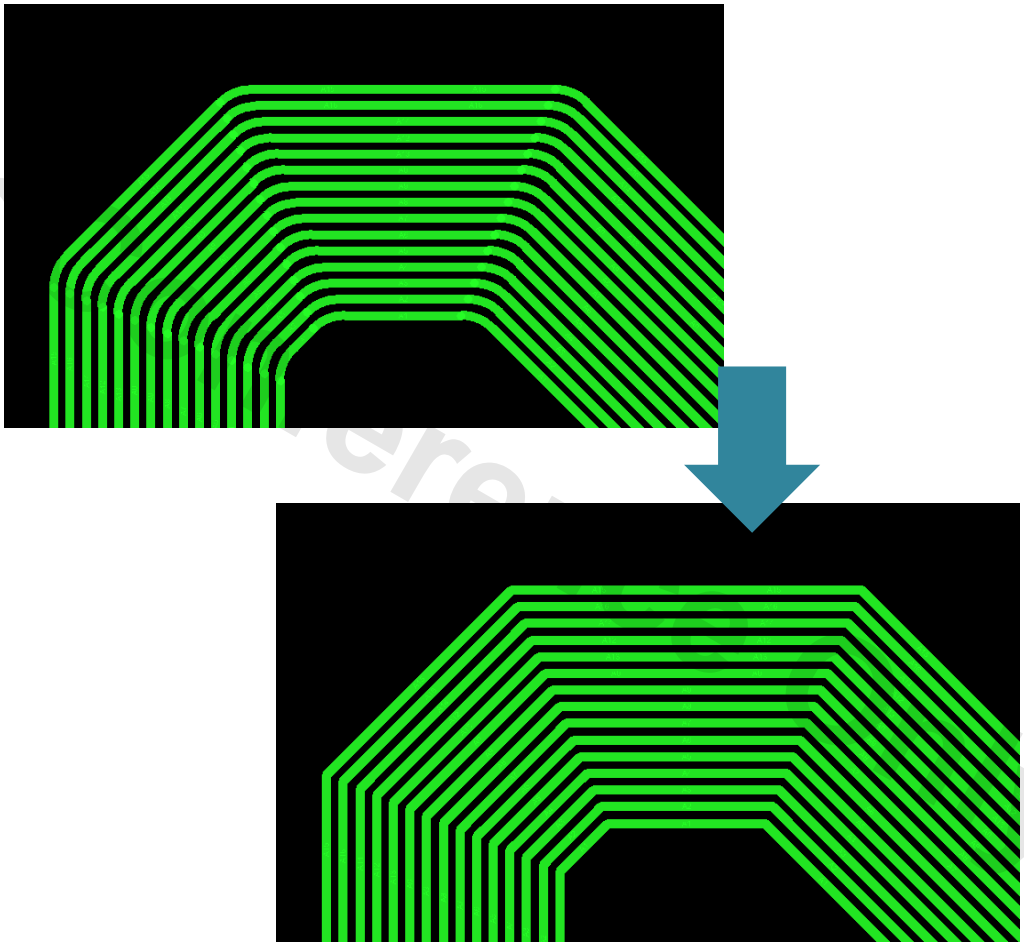
Arc Editing slide with vertex action as Move

Design Guidelines for Flex Circuits

Conductor Routing

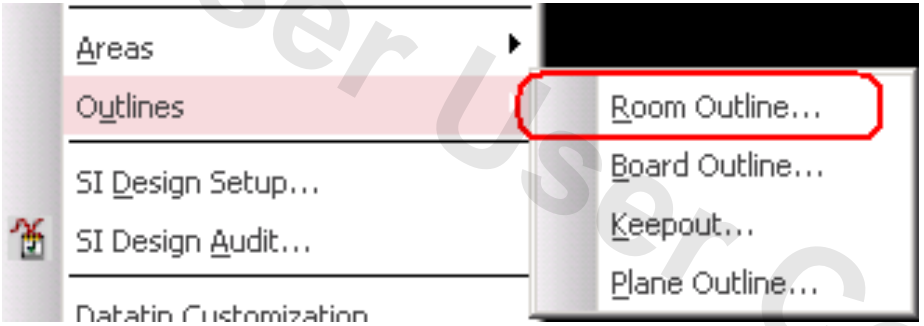
Auto Interactive Convert Corner (AiCC)

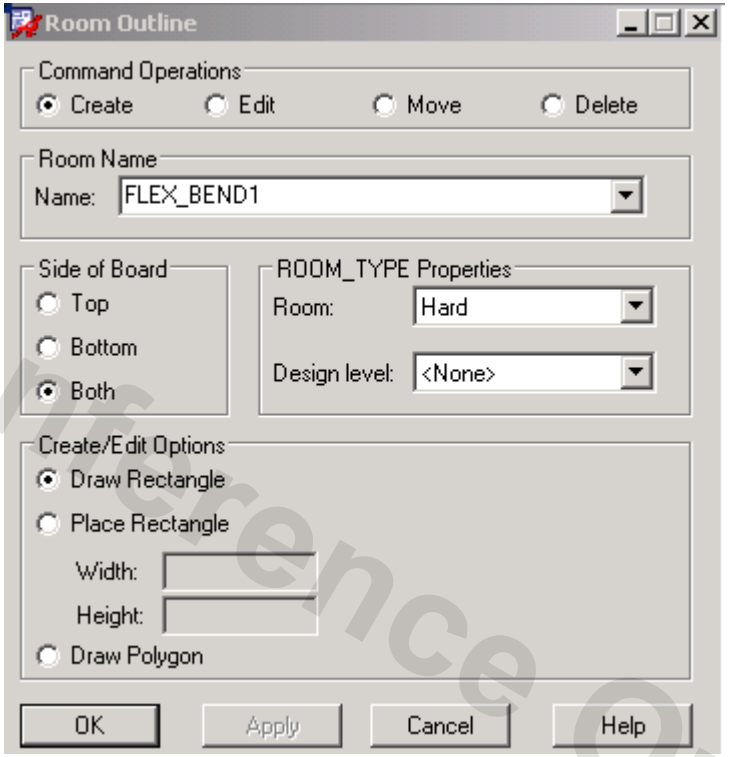




Design Guidelines for Flex Circuits

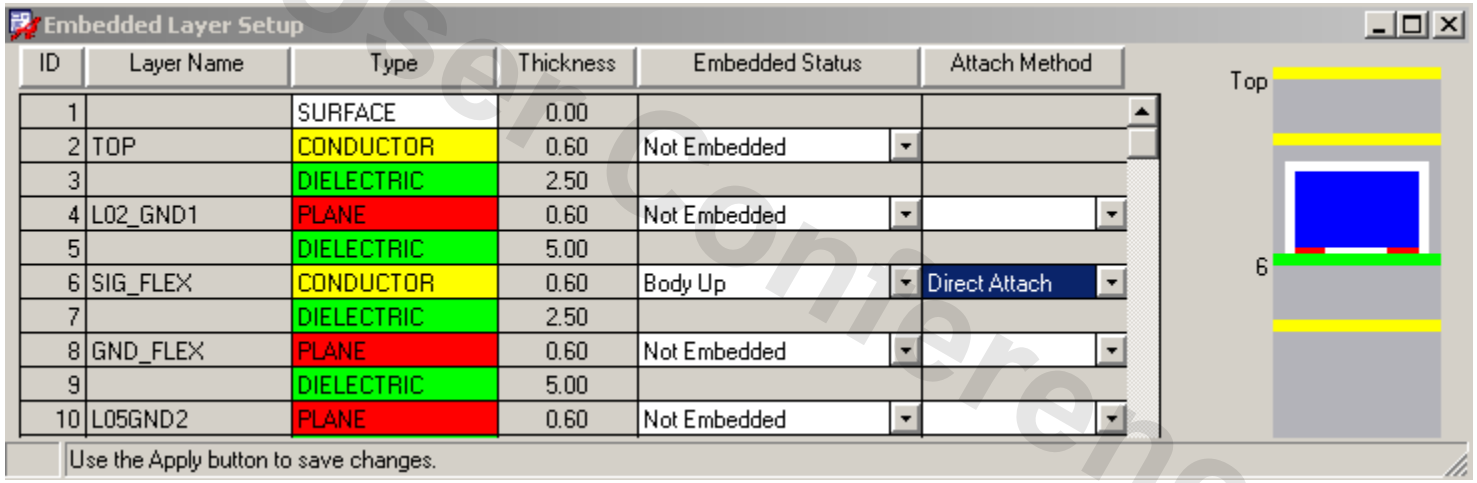
Placement of Components Using Rooms





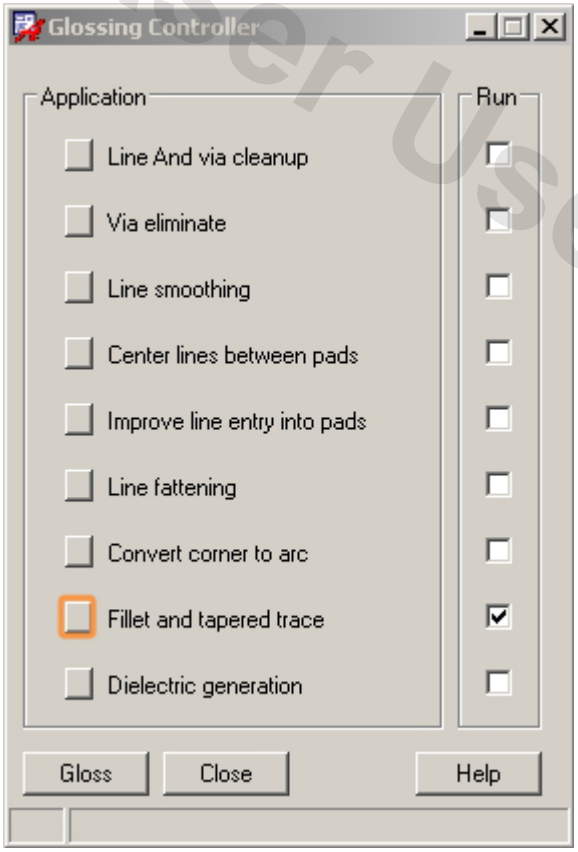
Design Guidelines for Flex Circuits

Placement of Components Using Embedded Functionality

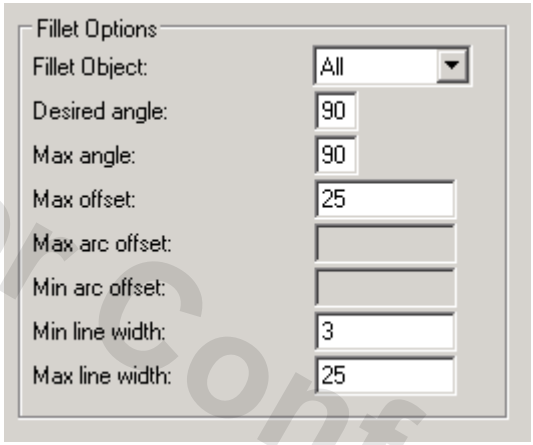


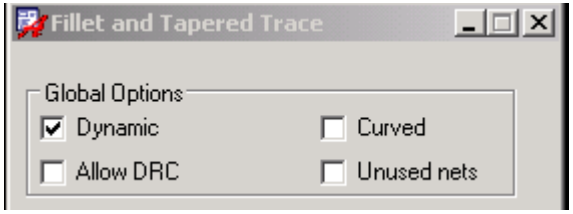
Design Guidelines for Flex Circuits

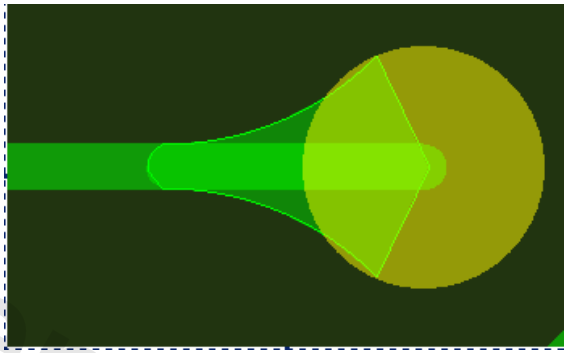
Filleting Pads and Traces

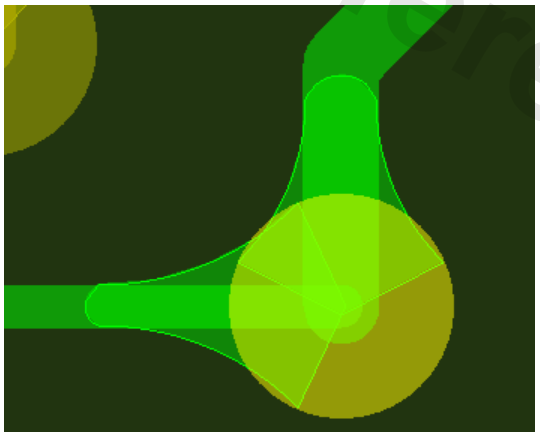


Gloss option with Filleting





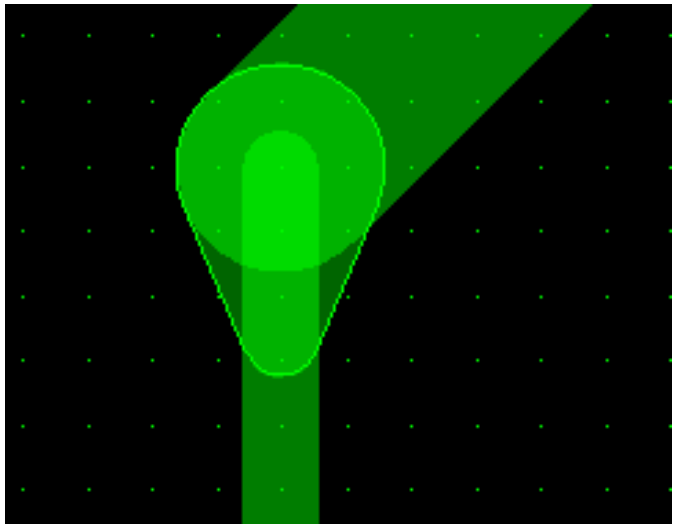




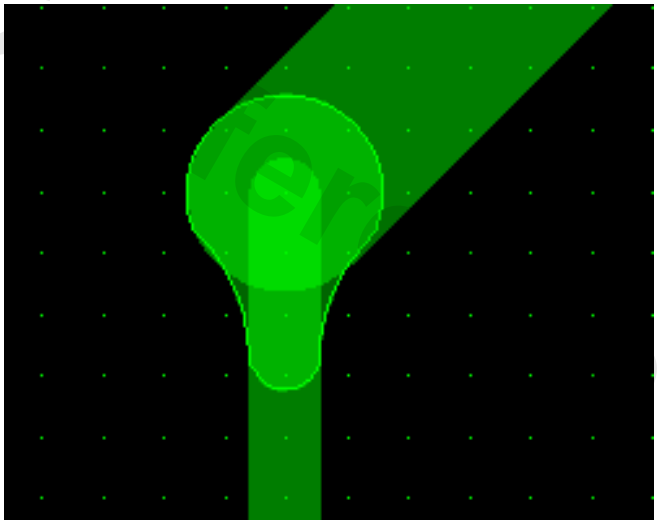
Design Guidelines for Flex Circuits

Filleting Pads and Traces

Tapered Trace



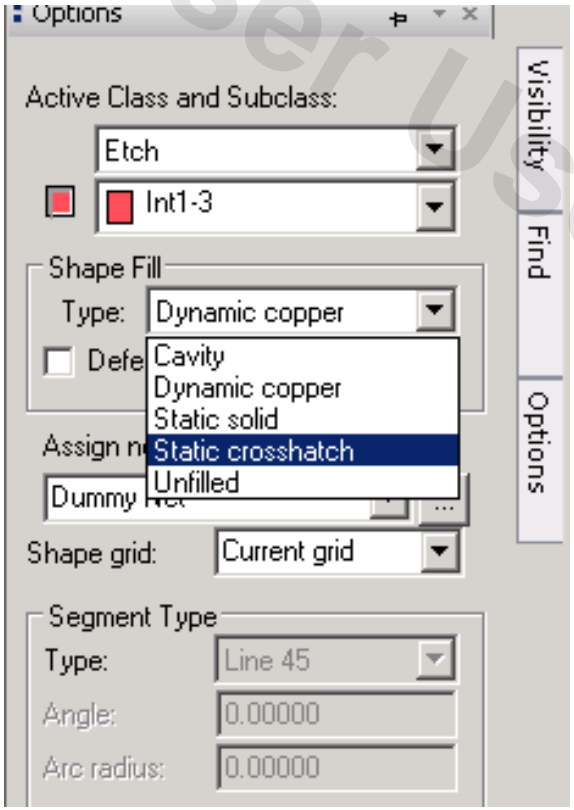
Without curve

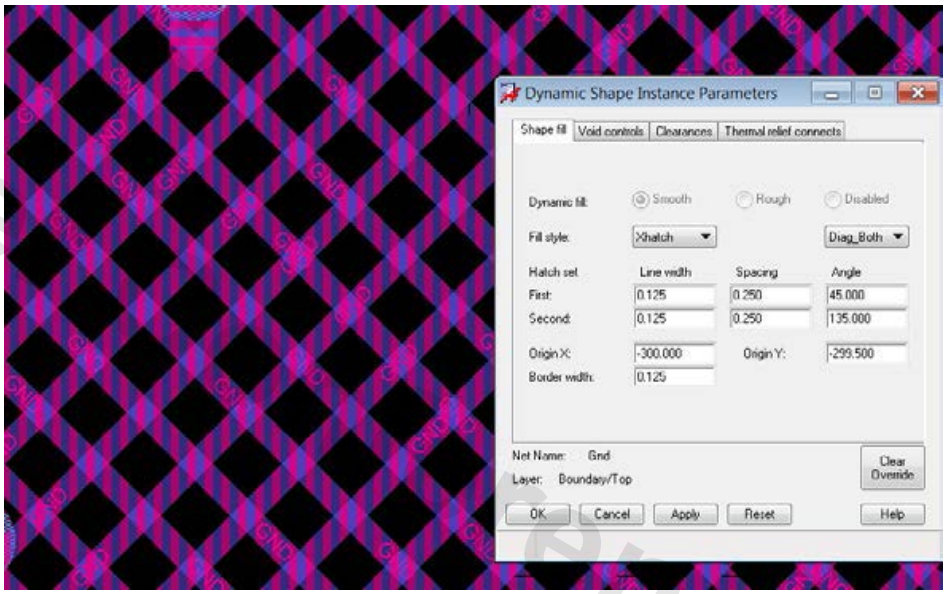


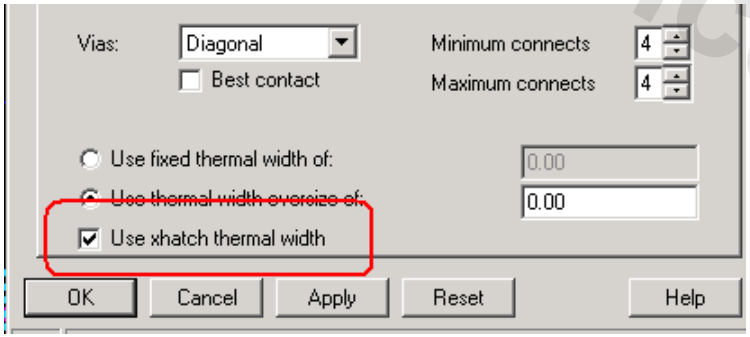
With curve

Design Guidelines for Flex Circuits

Shape Shielding

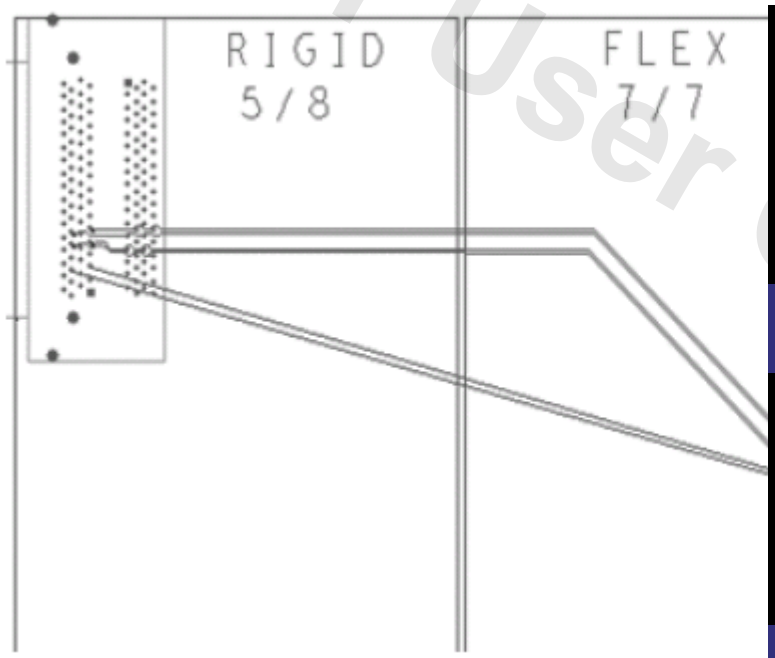


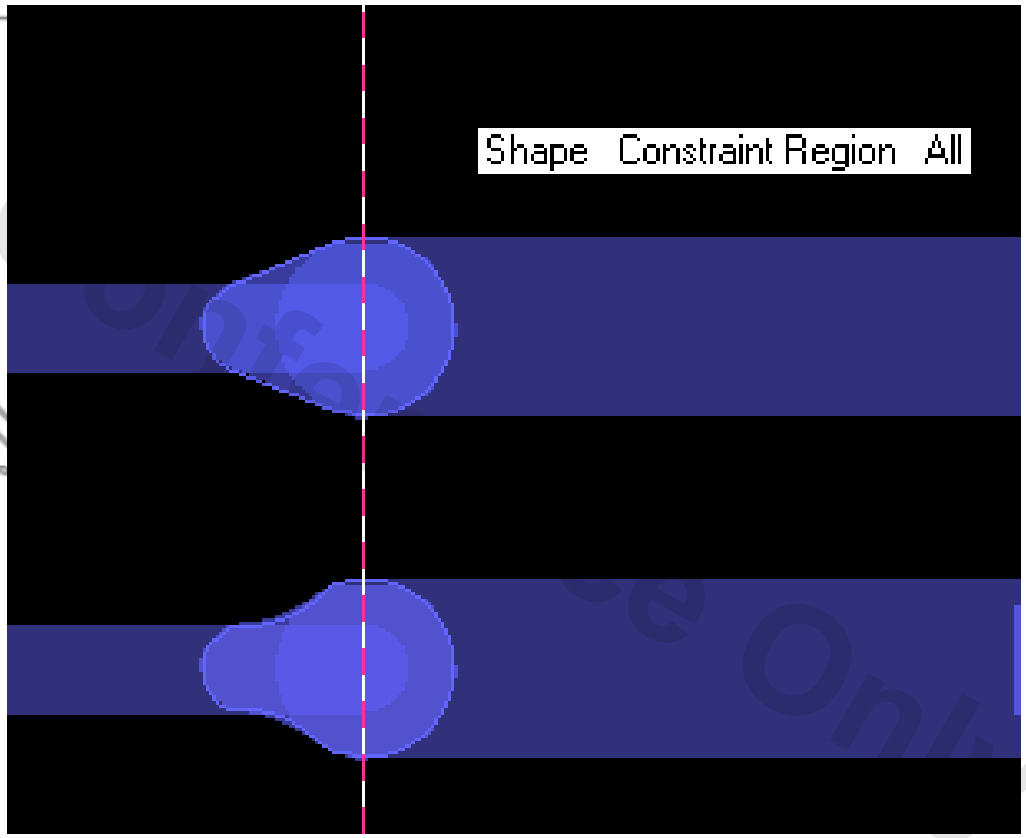




Design Guidelines for Flex Circuits

Region Rules for Trace width and Spacing





Design Guidelines for Flex Circuits

Restricting Via Type by Region Area

Type	Objects	Neck		Differential Pair Gap		Vias	BB Via Stagger	
		Min Width	Max Length	Primary	Neck		Min	Max
		mil	mil	mil	mil		mil	mil
Dsn	⊟ module6_CM	0.00	0.00			V26C14P_BGA	5.00	0.00
Rgn	BGA_1MM					VIA019		

- Constraint regions can be used to control the types of vias that are used within specific areas of design.