

#### Miniaturization-Rigid-Flex Design with Allegro

Jonathan Lee / Graser 31/Oct/2014



#### **Rigid-Flex Design with Allegro**



- Design Miniaturization through Rigid-Flex
- Rigid-Flex Design Flow



# Miniaturization

#### **Miniaturization**

- SoC more functional density
- SiP mixed technologies with memory
- **Rigid-Flex circuits**





**Stacked Die** 









- Large Pin Count Devices
- BGAs with shrinking pin pitches
  - $-1.0 \text{ mm} \rightarrow 0.8 \text{ mm} \rightarrow 0.5 \text{ mm}$
- **High Density Interconnect**



### **Design Miniaturization through Build-up Technology**

#### Complete Build-up

- ALIVH, PALAP, B2it, ...
- ALIVH (Matsushita owned): All Layer Interstitial Via Hole
- PALAP (DENSO **Consortium**) Patterned LAyup Process
- C - -- -- 1 19. **2**11 11 **ALIVH**





Core+Build-up



Hybrid approach

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- Build-up with a core



#### **Hybrid Approach**



### **HDI Design Challenges**

- Signal Integrity, Crosstalk, Power Delivery, SSO
- Physical Design
  - Fanout
  - Micro vs. Mechanically Drilled via
  - New Class of rules
    - Drill to Metal, Drill to Drill
    - Same Net DRCs
    - Via stack-up rules
  - Interactive etch editing
  - Display

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- Manufacturing prep
- Package-PCB Co-Design



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#### Fanout Via in Pad

- Dense BGAs with shrinking pin pitch requires carefully throughout fanout
- Users moving to via-in-pad for two reasons
  - Better Power Delivery system performance
  - Better space utilization
- Floating via

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- Complete via must be inside the SMD pad
- Via Center must be inside the SMD pad
- Override by component instance









# New Via Type, Rules and Controls Conference of the Needed

- System must be able to differentiate microvia from mechanically drilled vias
  - Support same net and net-net DRC conditions
- New rules and controls

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- Microvia spacing to all other etch elements
- Controls for via tangency
- Rules for pad overlap
- Support rules for via stacking



#### Same Net DRC

 Difference Same Net from Net to Net Spacing DRCs

- Same Net values are typically less than net-net
  - (different net) Pin to Via = 6 mils
  - Same Net Pin to Via = 3 mils

 Different for reporting same net DRC error (Display, reports)





#### **Adding uVia Structures**

- Optimize the process of adding micro-vias and core-vias based on user defined rules
- Traverse multiple layers with as few clicks as possible
- Treat structure as group entity
- Semi-interactive model for staggered pattern

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### Via Span Display

- Designs that utilize B/B vias present a problem for a user in trying to determine what layers a via connects to
- Color coding is currently used but on designs with a high concentration of via types, mapping colors to layer spans becomes difficult to remember
- The additional nomenclature within the bounds of the via pad will help aid in the determination of the span
- Allow users to control size, color for the nomenclature

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### Via Hole Plugging

- Via hole plugging/filling becomes standard on most high density boards
- Via holes can be plugged with conductive or non conductive material
- Thru vias are typically plugged from one side of the board. They assist in creating a tight vacuum for test fixtures
- Vias in Pad can be filled from either side of the board, usually with a conductive paste



#### Degassing

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- Perforation of power and shielding shapes with a grid of voids, with the intent of gaining additional adhesion and allow gases to escape between layers during the manufacturing process of the package
- Used to prevent build-up layer delamination

Progassing	
-Void Array Parame	eters
Void Shape:	Octagon V Diameter/Size
Void Size	200.00 microns
TONS SIEC.	
Void Separation:	50.00 microns
Void Pitch:	250.00 microns
Array Angle:	0.00
Starting Position:	Lower Left 🔽
Offset X:	150.00 microns Y: 150.00 microns
Custom Point X:	0.00 microns Y: 0.00 microns
-Void Spacing Cor	nstraints
Suppress Shapes	Less than: 100.00 microns
Void to:	
Chang Rounda	50 00 minutes
Shape Bounda	sy. 50.00 microns
Conductor (Sar	me Layer:
Conductor (Ad)	Layer):
Generate	Clear
	Caucal

# Miniaturization through Embedded

- Specify layers for embedding packaged components
- New DRCs for embedded devices
- Constraint-driven place and route
  - Move components to inner layers
  - Support for connecting to devices on inner layers
- Manufacturing outputs for layers with embedded devices









#### **Embedded Component Design**

#### Front-end driven

- "Embed required" (hard) or "embed optional" (soft)
- Ensures only qualified components get embedded
- Alt symbol support
- Backend to support symbol instance overrides
- PCB design implementation
  - Stack-up driven (chip-up, chip-down)
  - Cavity support
  - Package geometry support on internal layers
  - DRC

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- Comp to comp
- Comp to cavity
- Height within cavity
- Router integration
- Manufacturing output



Chip up

Chip Down

# Embedded Components in a Cavity

- Package symbol driven
  - New class "Cavity Outline"
  - Legacy place bound used as fallback
  - Keep-out properties
- User-defined cavities

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- Manually entered
- Can span multiple layers
- Represents as dynamic fill
  - Merge capability
- Checks under consideration
  - Max cavity area
  - Max comps within cavity

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### Advanced Miniaturization Techniques

Dual-sided components

Vertical components



FET

ADS

Vertically

Embedded

Component

 Support for embedding in dielectric on 2-layer boards

#### **Develop differentiated products**







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### **Necessary for Products in Many Market**

- **Consumer electronics**
- Mil/Aero

**Rigid-Flex** 

**Segments** 

- Medical
- Automotive





### Allegro Allows Multiple Board Outlines

Well this is one of the reasons why Motorola Mobile Devices switched to **Cadence Allegro** 3 years ago. Allegro allows multiple outlines like flex outlines or rigid outlines, external soldermask layers and internal full or partial coverlay layers and so on...

#### Philippe Gleizes

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Flex Circuit Design Manager Motorola Mobile Devices 600 North U.S. Highway 45 Libertyville, IL 60048



- "Motorola adopts Allegro for Flex Design capability"
- This was a limitation of our competition



### Custom Pad Definitions for Rigid-Flex

- Allegro PCB Editor allows up to 16 User Defined layers can be added to the padstack definition
  - Plug
  - Cap
  - Gold

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Parame	ters Layers								
Padst	ack layers								
Single layer mode									
	Layer	Regular Pad	Thermal Relief	Anti					
Bgn	TOP	Rect 0.2000 X	Null	Null					
	GOLD_TOP	Null	N/A	N/A					
	GOLD_TOP SOLDERMASK_TOP	Null Rect 0.2000 X	N/A N/A	N/A N/A					

• Plans to increase to 32 in new release

### Place Components Directly on Flex Layers

- No special pad editing or complicated work-arounds required with PCB Miniaturization Option
- Drop component to layer defined as "flex" using embedded component functionality

Embedded Lay	er Setup	Thickness	Embedded Statu	ıs	Attach Method			
	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,							
	SURFACE	0.018				- <b>*</b>		
2	DIELECTRIC	0.013				=		
3 TOP	CONDUCTOR	0.018	Not Embedded	-		-		
4	DIELECTRIC	0.013				.		
5 LAYER_2	CONDUCTOR	0.018	Body Up	-	Direct Attach 💌		Top	
6	DIELECTRIC	0.013					100	
7 LAYER_3	CONDUCTOR	0.018	Not Embedded	-	+	i I		
8	DIELECTRIC	0.013						
9 BOTTOM	CONDUCTOR	0.018	Not Embedded	-				
10	DIELECTRIC	0.013						
11	SURFACE	0.018					5	
						-		

#### Fast Interconnect Routing on Flex

#### Curved Corners

Support in both Add Connect and Slide functions





### Multi-line Flex Router Interconnect Flow Planning

- Multi-line Flex router permits users to quickly add 'trunk of bus' for real estate planning
  - Includes line of different width (guard trace/signals)
  - "Contour locking" (lock onto guard trace or route keep-in area)
- User configurable for maximum productivity
  - Contour lock option
  - Arc option

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- User defines line and space
- Once satisfied, connects the end points to their destination pins
- Effective in preventing "I-Beam" routing on Flex
  - I-Beam construction increases stiffness through bend areas of flex.







### Best in Class Support for HDI Routing, CONFERENCE Graser LINE OF CONFERENCE Graser LINE OF CONFERENCE Graser LINE OF CONFERENCE CONF

- Staggered vias
- Stacked vias
- Inset vias
- Any Layer via
- Via in pad
- Via labels
- NC Drill automation for all HDI via combinations



Adding of stacked vias used "working layer model"







Adding Inset vias



### Fillets and Cross Hatch Improve Reliability, Flexibility

#### Fillets or teardrops

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- increases pad area
- distribute stresses evenly at the junction
- Straight or curved fillets
- Dynamic option: Add or delete as your route into pin or via
- Cross-Hatch shapes are used to decrease weight and increase flexibility
  - Allegro offers both "Static" and "Dynamic" fill options







### Shape Based Fillet to "Taper" Line Width

- Shape based fillet designed to "taper" line width changes along route path
  - Automatically added at the point of a line width change







# **Rigid-Flex Design Flow**

#### **Rigid-Flex Design Flow**

- Flexible Circuit Technology
- Material Used for Flex/Rigid-Flex Design
- Board Outline
- Design Guidelines for Flex Circuits



#### Flexible Circuit Technology Flex circuits

Single layer

conductive polymer flexible dielectric film

Double layer

conductive polymer flexible dielectric film

conductive polymer

Multi layer

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conductive polymer flexible dielectric film

conductive polymer

flexible dielectric film

conductive polymer

Different layers

flexible dielectric film

conductive polymer

### Flexible Circuit Technology Rigid flex

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 This structure is combination of flex circuits placed on rigid as well as on flexible substrates. These are laminated together into a single structure

### Material Used for Flex/Rigid-Flex Design

Materials File

#### C:/Cadence/SPB\_16.5/share/pcb/text/materials.dat

In Use	Material Name	Туре	Thickness	Electrical Conductivity	Dielectric Constant	Loss Tangent @ 1Ghz	
	user_defined	Conductor	39.3701 MIL	580000 mho/cm	4.500000	0.000000 🗖	•
	10Z_COPPER	Conductor	0 MIL	580000 mho/cm	4.500000	0.000000	
	20Z_COPPER	Conductor	0 MIL	580000 mho/cm	4.500000	0.00000	
	40Z_COPPER	Conductor	0 MIL	580000 mho/cm	4.500000	0.000000	
×	AIR	Dielectric	0 MIL	0 mho/cm	1.000000	0.000000	
	ALUMINUM	Conductor	0 MIL	350000 mho/cm	4.500000	0.000000	
	BT_EPOXY	Dielectric	8 MIL	0 mho/cm	4.100000	0.020000	
	CHROMIUM	Conductor	0 MIL	77000 mho/cm	4.500000	0.000000	
	CONFORMAL_COAT	Dielectric	0.787402 MIL	0 mho/cm	3.000000	0.000000	
×	COPPER	Conductor	1.2 MIL	595900 mho/cm	4.500000	0.000000	
	CYANATE_ESTER_E	Dielectric	8 MIL	0 mho/cm	3.800000	0.009000	
	CYANATE_ESTER_S	Dielectric	8 MIL	0 mho/cm	3.500000	0.009000	
×	FR-4	Dielectric	8 MIL	0 mho/cm	4.500000	0.035000	
	GOLD	Conductor	0 MIL	430000 mho/cm	4.500000	0.000000	
	INCONEL	Dielectric	0 MIL	8200 mho/cm	4.500000	0.000000	
	INDIUM	Conductor	0 MIL	120000 mho/cm	4.500000	0.000000	•
				35 Materials		0,	

OK

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Cancel

Help

CONFER

**Reload Materials** 

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#### Material Editor Window

#### **Board Outline**



 Allegro PCB Editor can import IDX, DXF, and IDF files that contain the outline, cutouts, and other mechanical features that are critical to the design.



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# **Design Guidelines for Flex Circuits**



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# Design Guidelines for Flex Circuits Conference Construction Conductor Routing

Min Corner Size:	1x width 💌	ם	
Min Arc Radius:	1x width 💌		
Vertex Action:	Arc Corner 💽	0	
Bubble: Hu	g only 📃	ptio	
Shove vias:	Off 🗾	л И	
🔽 Clip dang	ling clines		
Smooth:	Minimal 🗾 💌		



Arc Editing option with vertex action as Arc Corner



# **Design Guidelines for Flex Circuits**





Arc Editing slide with vertex action as Move



# **Design Guidelines for Flex Circuits**

#### Auto Interactive Convert Corner (AiCC)





	Oreas		📴 Room Outline
	Outlines	Room Outline	Command Operations • Create O Edit O Move O Delete
*	SI <u>D</u> esign Setup SI Design <u>A</u> udit Datatin Customization	Board Outline Keepoùt Plane Outline	Room Name   Name:   FLEX_BEND1     Side of Board   Top   Bottom   Both     Create/E dit Options   Oraw Rectangle   Place Rectangle   Width:   Height:   Draw Polygon     OK     Apply   Cancel

#### **Design Guidelines for Flex Circuits** Placement of Components Using Embedded Functionality

🎾 Eml	bedded Layer Setu	P				
ID	Layer Name	Туре	Thickness	Embedded Status	Attach Method	Тор
1		SURFACE	0.00		▲	
2	TOP	CONDUCTOR	0.60	Not Embedded		
3		DIELECTRIC	2.50			
4	L02_GND1	PLANE	0.60	Not Embedded		
5		DIELECTRIC	5.00			
6	SIG_FLEX	CONDUCTOR	0.60	Body Up 💽	Direct Attach 📃 💌	0
7		DIELECTRIC	2.50			
8	GND_FLEX	PLANE	0.60	Not Embedded		
9		DIELECTRIC	5.00			
10	L05GND2	PLANE	0.60	Not Embedded		
U	se the Apply button to	) save changes.				





Line smoothing	
Center lines between pads	
Improve line entry into pads	
Line fattening	
Convert corner to arc	
Fillet and tapered trace	
Dielectric generation	
Gloss Close	Help

Gloss option with Filleting

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### **Design Guidelines for Flex Circuits**



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				Shape fill Void or	ontrois Clearances	Thermal relief co	onnects	
				Dynamic fill:	() Smooth	Rough	() Disabled	
	199		120	Fill style:	Xhatch 💌		Diag_Both 💌	
				Halch set	Line with	Spacent	Arrele	
			NAV.	First	0.125	0.250	45.000	
				Second	0.125	0.250	135.000	
				Origin X:	-300.000	Origin Y:	-299.500	
		6 AG		Border width:	0.125		1	
$\diamond$	$\mathbf{X}$			Net Name: Grid Layer: Bounday/ OK. Car	Top cel Apply	Reset	Clear Ovenide Help	
Ò	X	8		Net Name: Gnd Layer: Boundary/ OK. Car	Top cel Apply	Reset	Clear Ovenide Help	
Vias:	Diagonal		Minimum	Net Name: Grid Layer: Boundary/ OK Car Connects	Top cel Apply 7	Reset	Clear Ovenide Heb	
Vias:	Diagonal Best contac		Minimum Maximum	Net Name: Grid Layer: Boundary/ OK Car Connects in connects	Top cel Apply 4 4	Reset	Clear Ovenide Heb	
Vias:	Diagonal Best contac	v t of:	Minimum Maximum	Net Name: Grid Layer: Boundary/ OK Car connects n connects	Top cel Apply 4 4	Reset	Clear Ovenido Heb	
Vias:	Diagonal Best contac	t of:	Minimum Maximum	Net Name: Grid Laver: Boundary/ OK Car connects connects	Top cel Apply 4 4 4	Reset	Clear Ovenido Help	





#### **Design Guidelines for Flex Circuits** Restricting Via Type by Region Area

			N	eck	ck Differential Pair Gap			88 Via Stagger	
Туре		Objects	Min Width	Max Length	Primary	Neck	Vias	Min	Max
			mil	mil	mil	mil		mil	mil
Dsn	B	module6_CM	0.00	0.00			V26C14P_BGA	5.00	0.00
Rgn		BGA_1MM					VIA019		

 Constraint regions can be used to control the types of vias that are used within specific areas of design.

Edit Via List	an the -	databases		_	Vie kete			
lect a via from the library	or the	database:			Via list:			 -
Name 4	Start	End		-	Name	Start	End	 Remove
102X118R	TOP	TOP		_	BB1-2	TOP	SIGNAL_2	
109N	TOD	TOD			BB2-3	SIGNAL_2	SIGNAL_3	<u>Up</u>
14C_SM110	TOP	TOP			DB-CORES-0	SIGNAL_3	SIGNAL_D	Down
1669760	TOP	TOP			000-7	SIGNAL_0	BOTTOM	
18764D SMT22768D	TOP	TOP			VTA019	TOP	BOTTOM	011
20C SMT24	TOP	TOP			TOP-STG3-SKIP	TOP	STGNAL 3	OK
2200_311124	TOP	TOP			101-3103-3111	IOF	STONAL_S	Cancel
36X50R	TOP	TOP						
38C22P VHDM NT M	TOP	BOTTOM		-				<u>H</u> elp
				<u> </u>				
Filter								Purge
Show vias from the lib	rary							
<ul> <li>Show vias from the <u>d</u>a</li> </ul>	tabase							
ilter by name:		-						
	881-2	NN2-3 NN-CORE3-6	Add	TOP-SIC3-SKIP	6		ewer Options	Hide viewer
#2 TOP Conductor #3 Dielectric #4 SIGNAL_2 Conductor #5 Dielectric #5 SIGNAL_3 Conductor #7 Dielectric #8 SIGNAL_4 Conductor #9 Dielectric #10 SIGNAL_5 Conductor	<b>V</b> 1	Ī		1				

