USER CONFERENCE Graser 2014 Oct 31 Taipei

High-Speed Interface Driven PCB Design

(Net Group, Aixx, Floorplanning…etc)

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Topic – Chapter One

- An Interface Example – DDRx
- An Example: Timing Relationship for DDR3
- Case Description
  - Routing condition
  - Using features
- Before Interactive Routing
  - You must define well
  - You might need to define well

Topic – Chapter Two

- Net Groups
  - CPU[0]_BANK[0]
  - CHNLA_ADDR_CMD
  - CHNLB_ADDR_CMD
  - CHNLA_CLOCKS
  - CHNLB_CLOCKS
  - CHNLA_CTRL
  - CHNLB_CTRL
  - CHNLA_DATA
  - CHNLB_DATA
- Plan
  - 1st CLOCKS
  - 2nd Target Pre-routing
  - 3rd ADDR CMD & CLTR
  - 4th DATA
- Routing Result
- Conclusion
- What Else?

Topic – Chapter Three

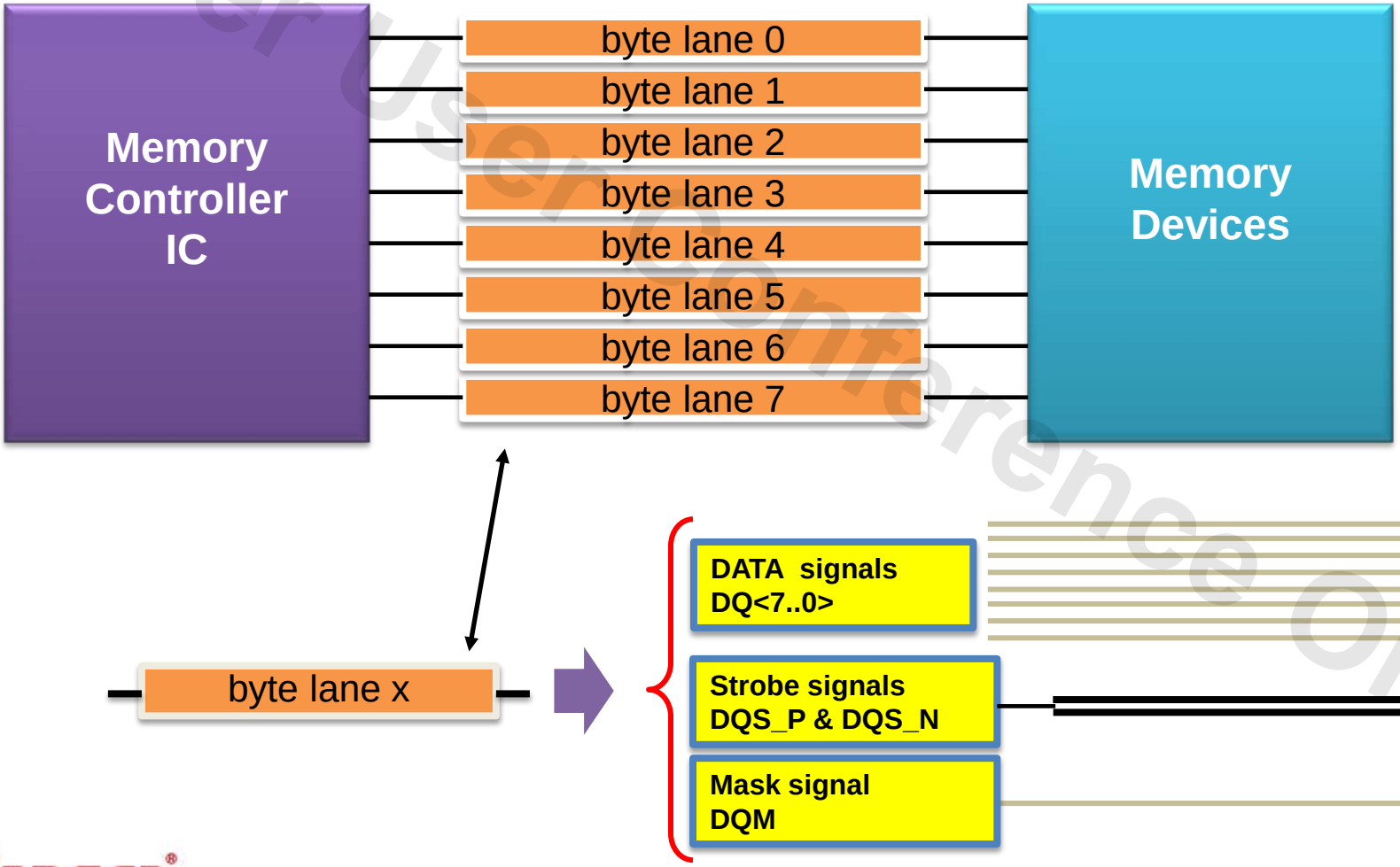
- Routing Flow

- Optimize
  - Timing vision
  - Auto-interactive Delay Tune (AiDT)
  - Auto-interactive Phase Tune (AiPT)
  - Auto-interactive Add Connect (AiAC)
  - Auto-interactive Convert Corner (AiCC)
  - Auto-interactive Breakout (AiBT)
  - Auto-interactive Trunk Routing (AiTR)

Chapter One

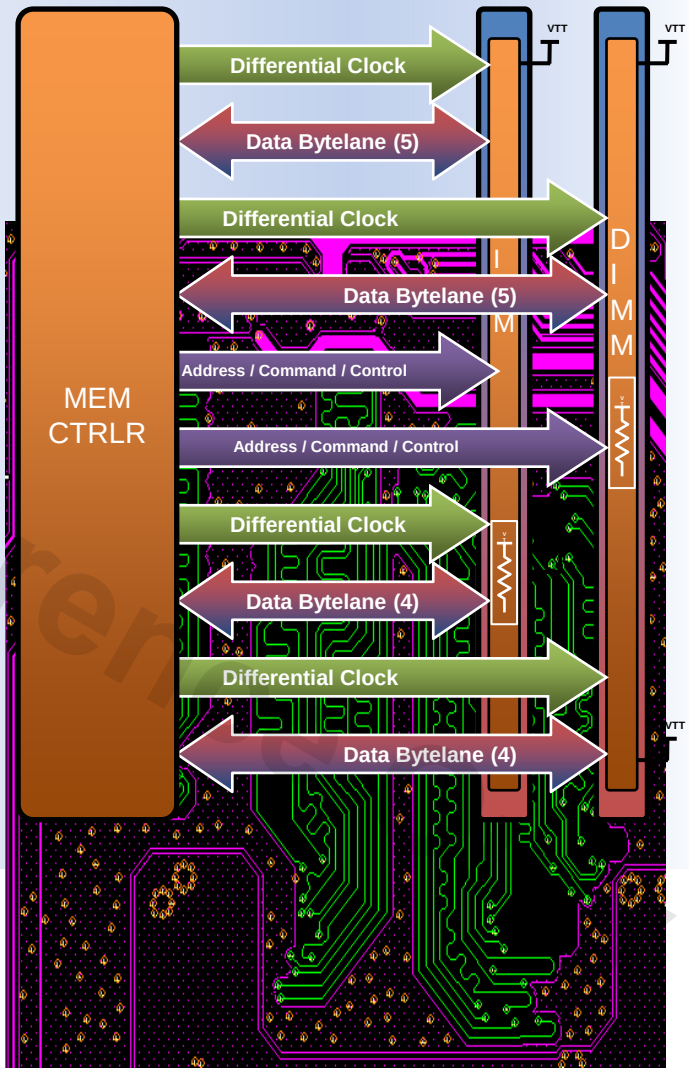
An Interface Example - DDRx

- PCB designers need to connect interfaces quickly and easily
- Today's interfaces cannot be modeled in single-level hierarchy

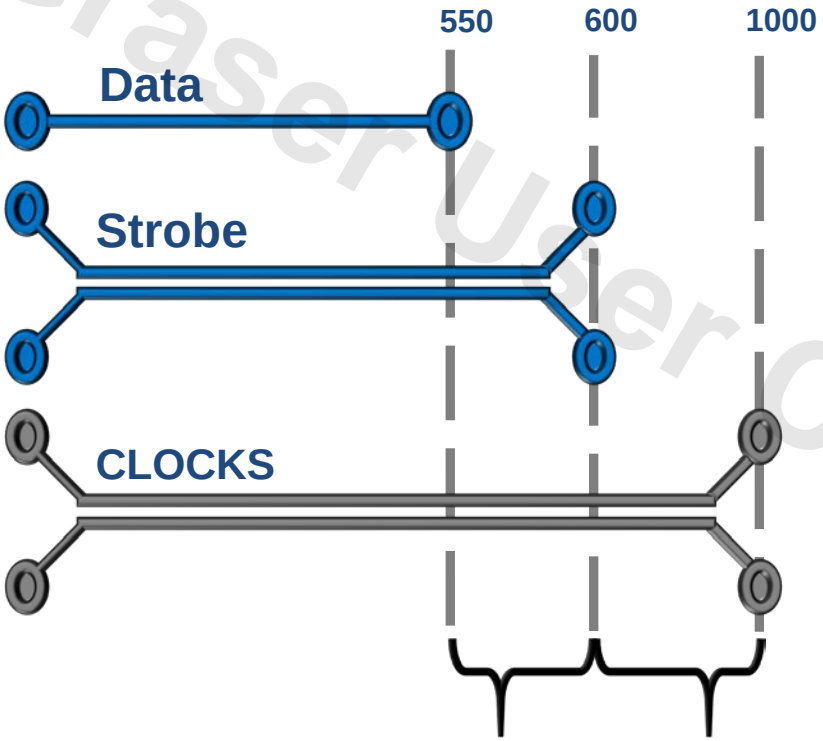


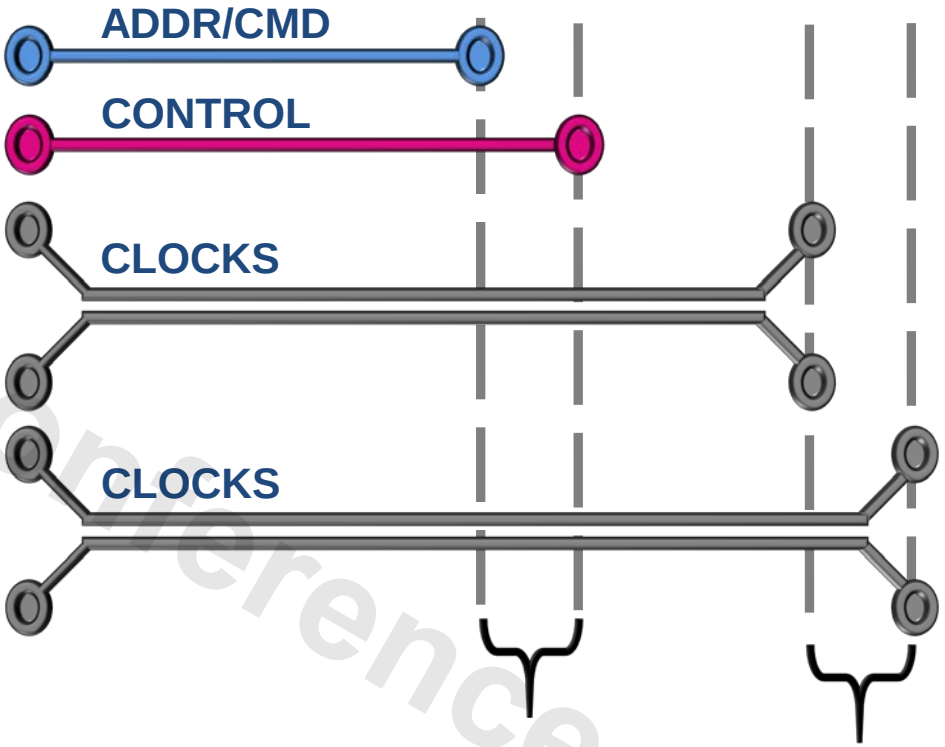
Timing closure on advanced high-speed interfaces is iterative, frustrating, and time consuming

- Market demands products that are faster, have more bandwidth, and use less power
- Increasing use of standards-based interfaces
  - DDR2 → DDR3 → DDR4
  - PCI Express® Gen1 → Gen2 → Gen3
  - Supply voltage: 1.8V → 1.5V → 1.2V
- Increasingly sensitive signals
  - Ripples through power supply
  - Crosstalk
- Complex set of electrical and layout implementation constraints



An Example: Timing Relationship for DDR3

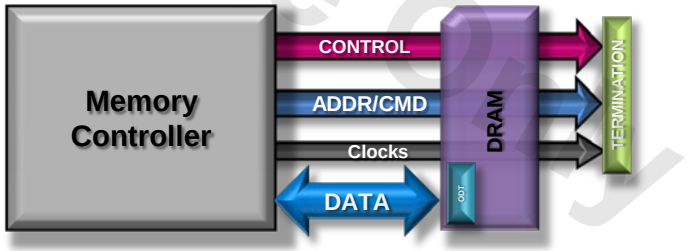




- Complex matching requirements
- 4 sets of clocks, 8 sets of strobes
- Match CLKs, strobes, and data

  AND

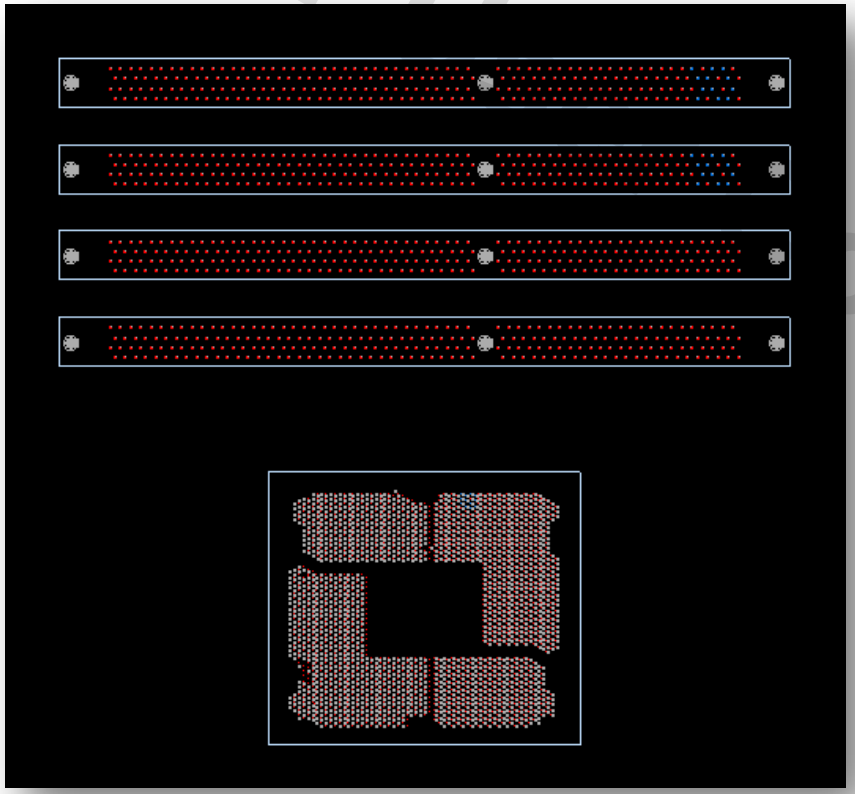
  Match CLKs, ADDR/CMD, and CONTROL



Case Description

- Routing Condition : DDR Portion

Area:



Critical Signal:

Net Group:

CPU[0]_BANK[0]-CHNLA_ADDR_CMD (24)
CPU[0]_BANK[0]-CHNLB_ADDR_CMD (24)
CPU[0]_BANK[0]-CHNLA_CLOCKS (8)
CPU[0]_BANK[0]-CHNLB_CLOCKS (8)
CPU[0]_BANK[0]-CHNLA_CTRL (16)
CPU[0]_BANK[0]-CHNLB_CTRL (16)
CPU[0]_BANK[0]-CHNLA_DATA (90)
CPU[0]_BANK[0]-CHNLB_DATA (90)

Total: 276 nets

Stackup: 12 layers

Case Description

- Using features
  - Allegro PCB Designer v16.6 s034
  - Design Planning Option
  - High-Speed Option

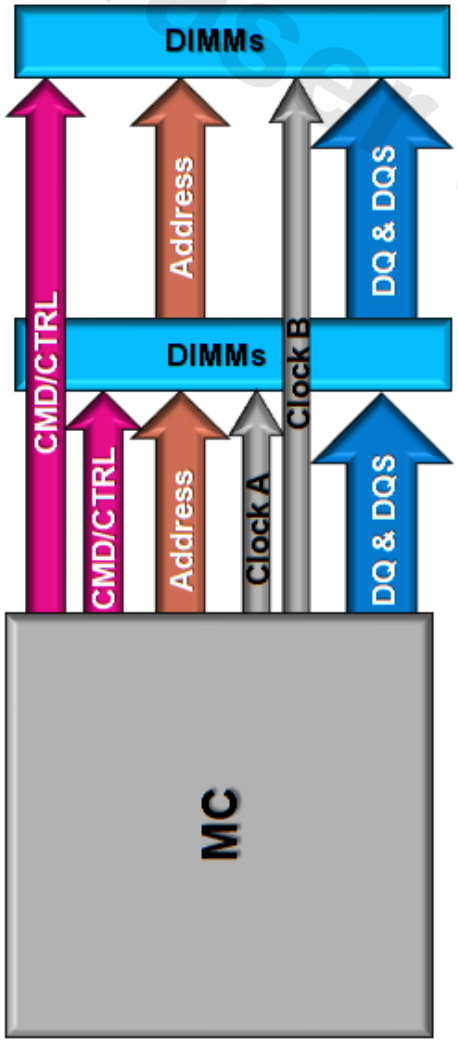
Before Interactive Routing

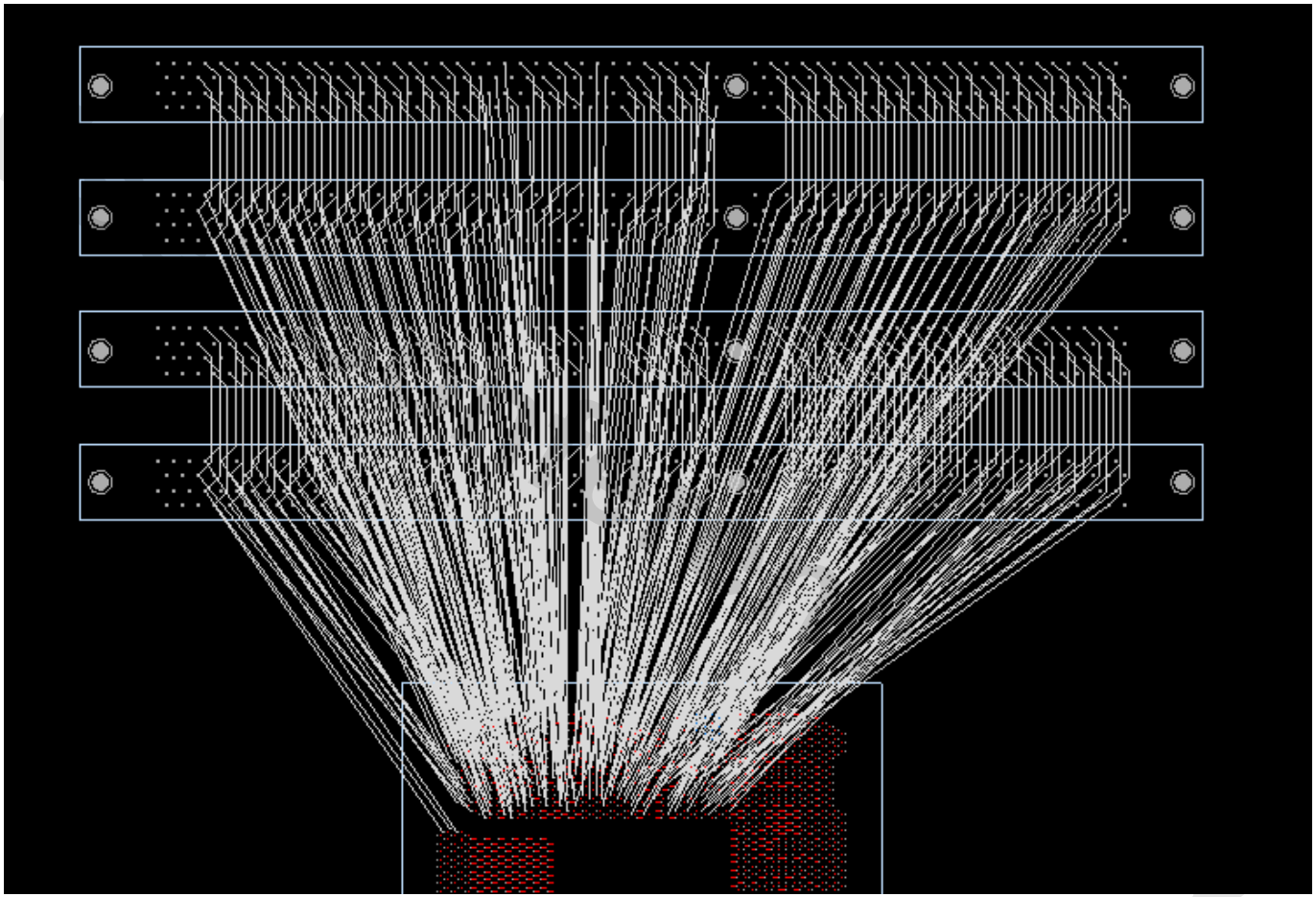
- You **must** define well
  - Constraints
  - Regions
  - Keep in/out areas
  - Fanout
  - Routing layer
- You might need to define well
  - Cooper in power plane layers

Chapter Two

Net Groups (Enhanced by QIR#5)

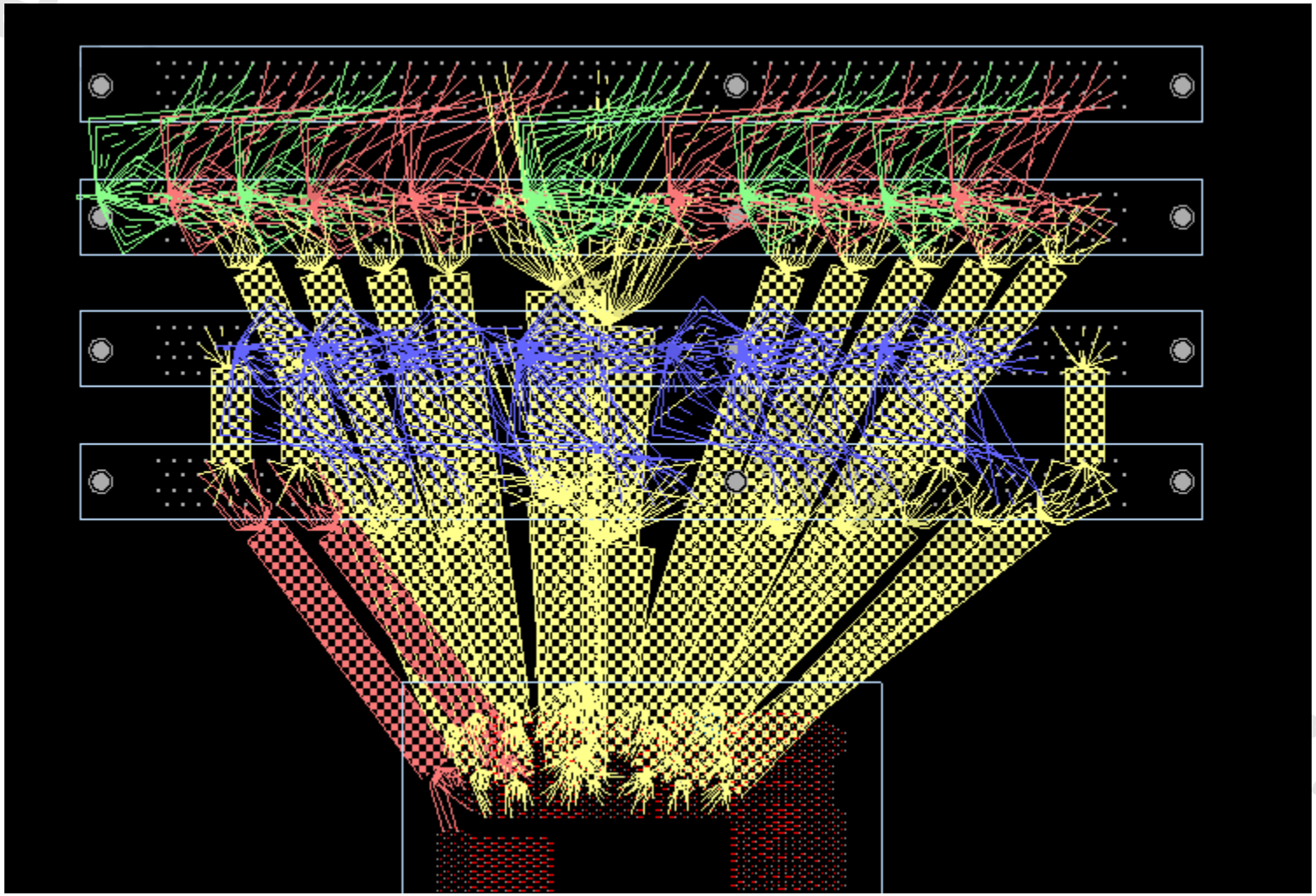
CPU[0]_BANK[0]





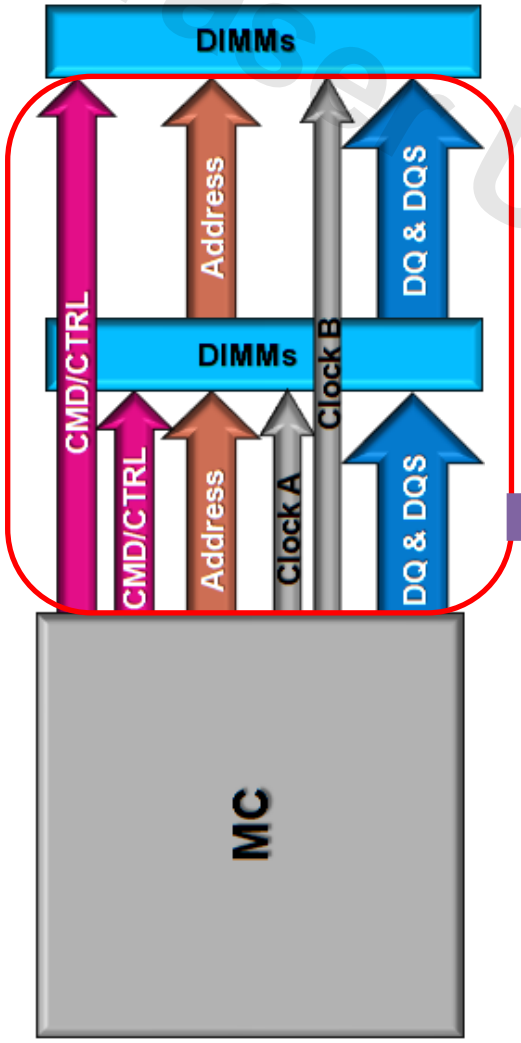
Net Groups

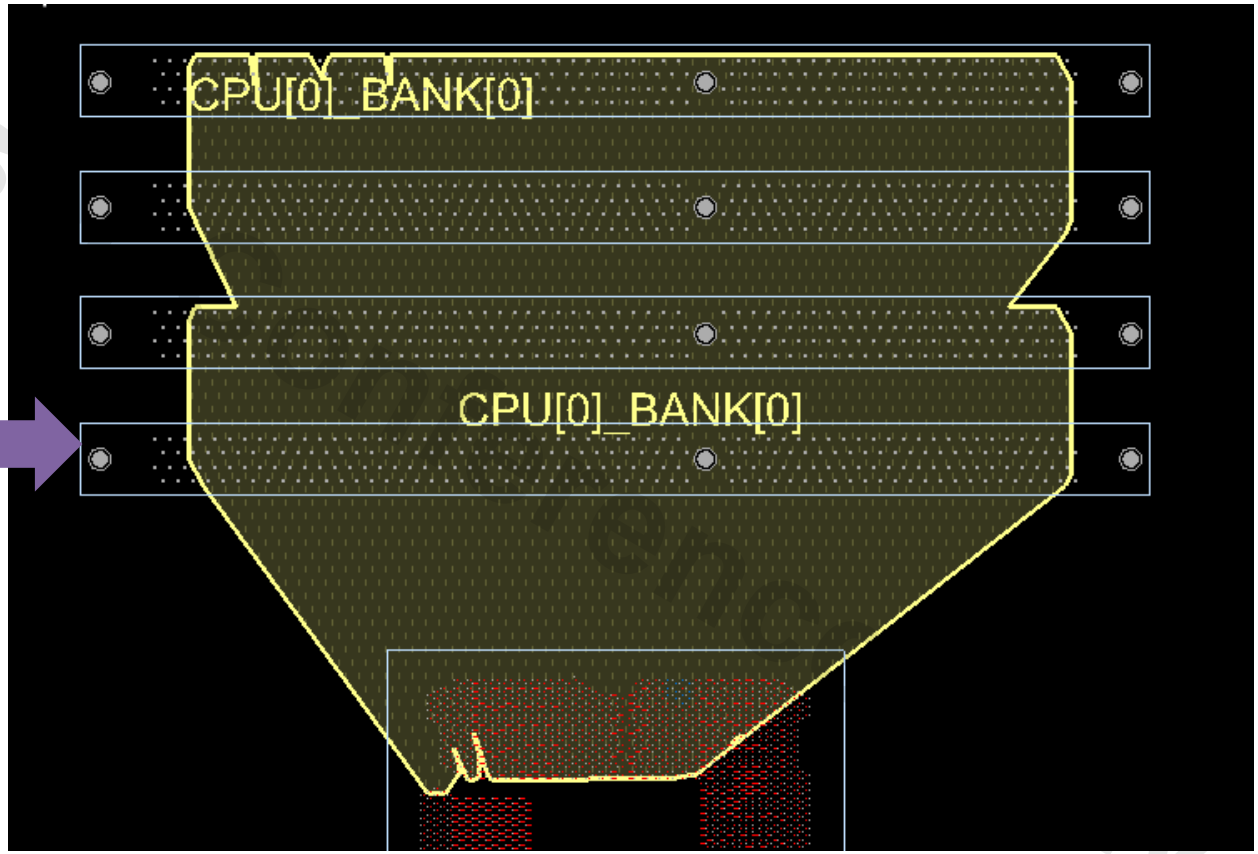
CPU[0]_BANK[0]



Net Groups

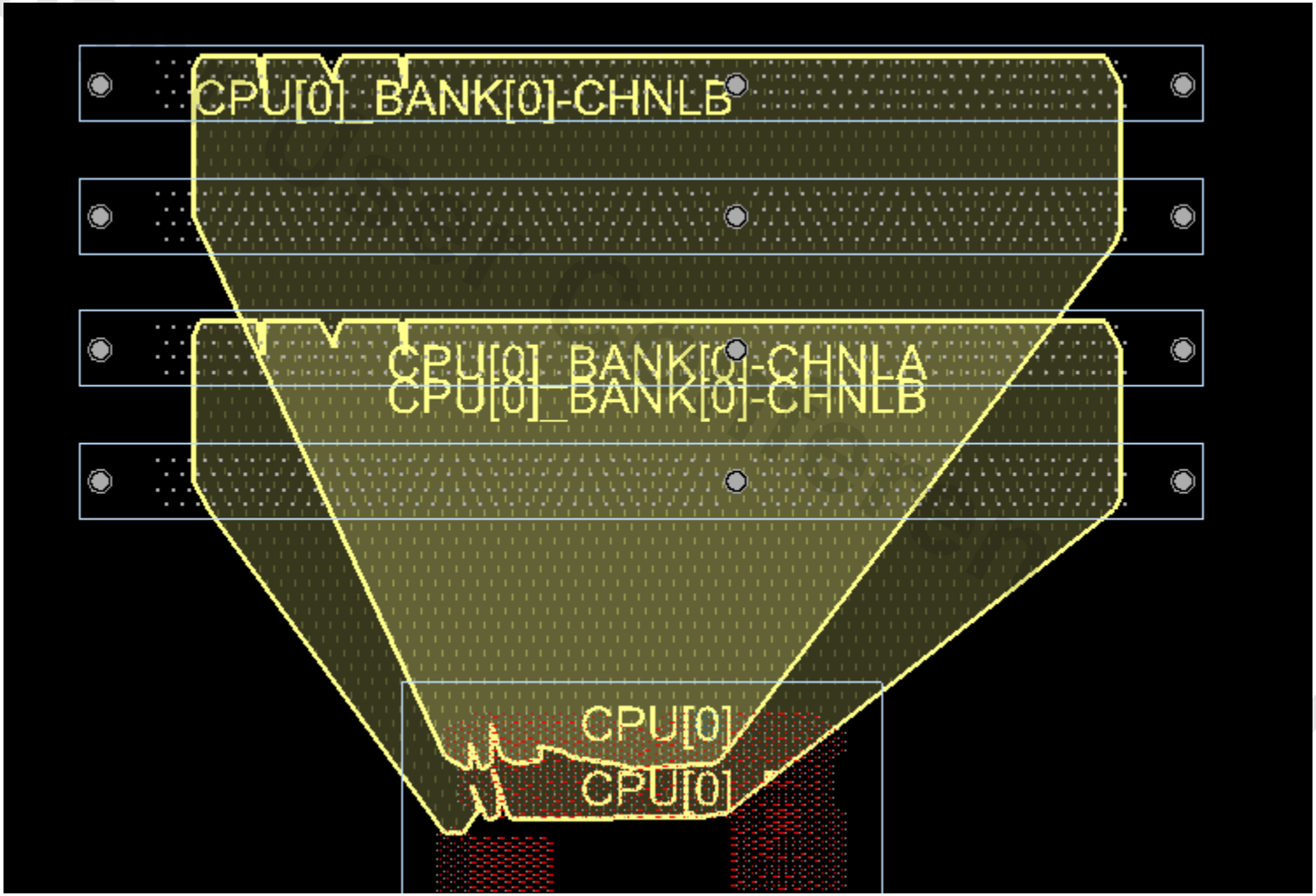
CPU[0]_BANK[0] – Hierarchy : Top Level





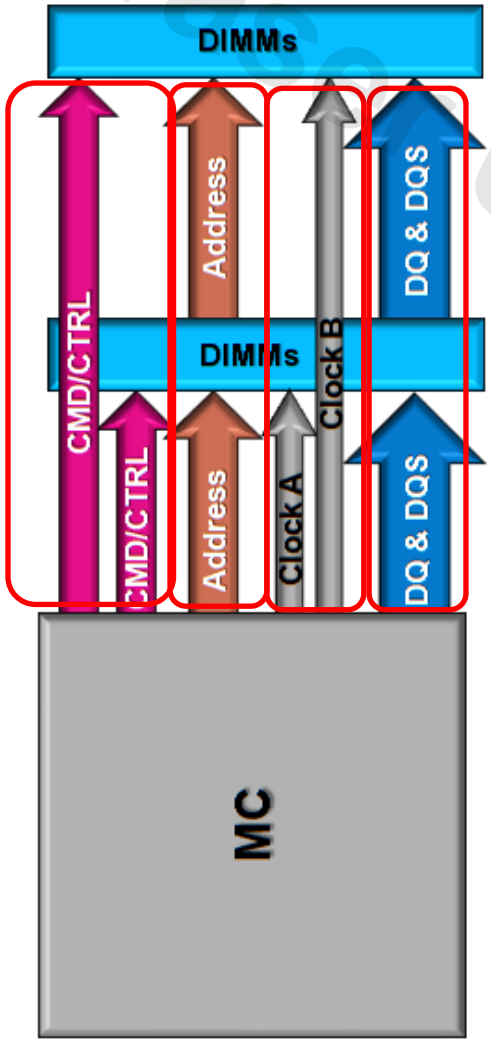
Net Groups

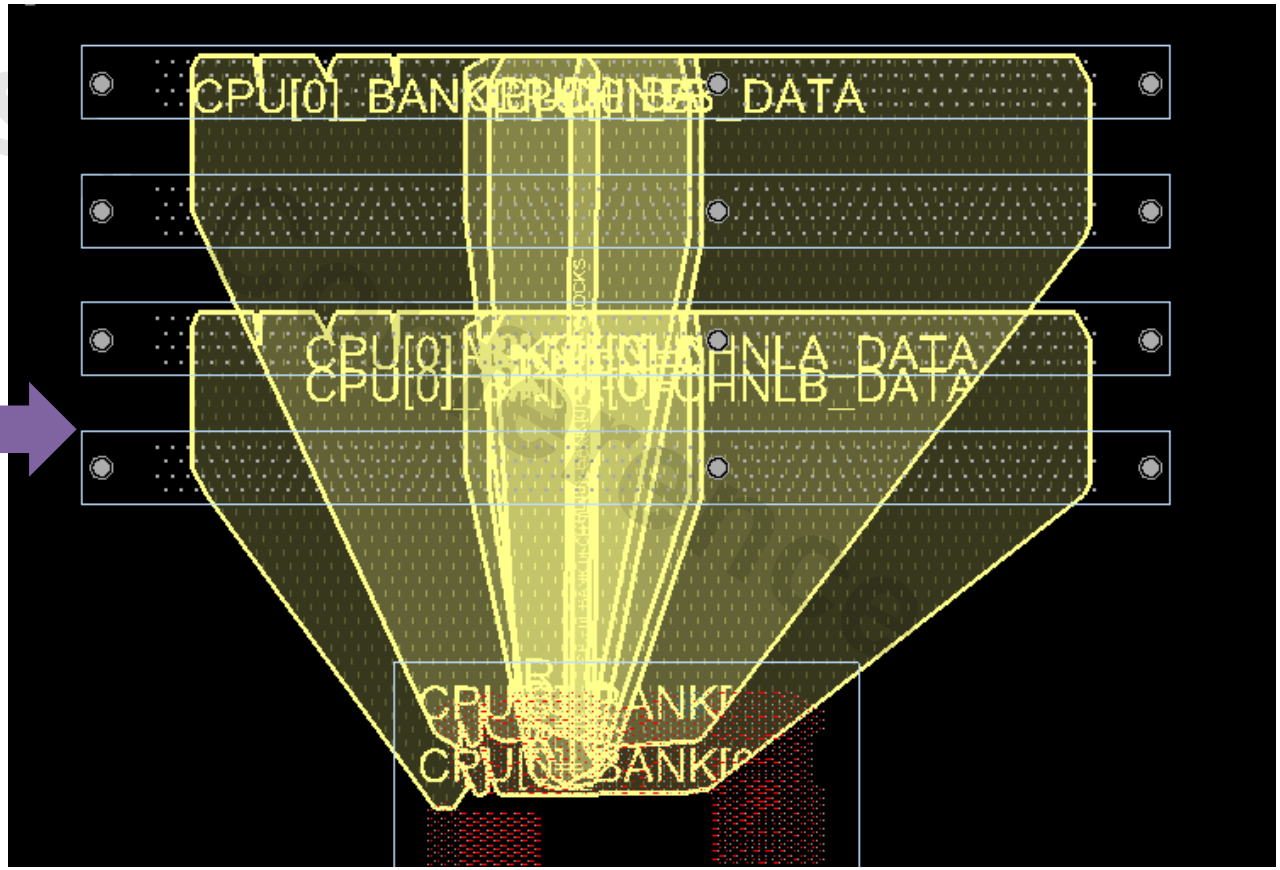
CPU[0]_BANK[0] – Down Hierarchy



Net Groups

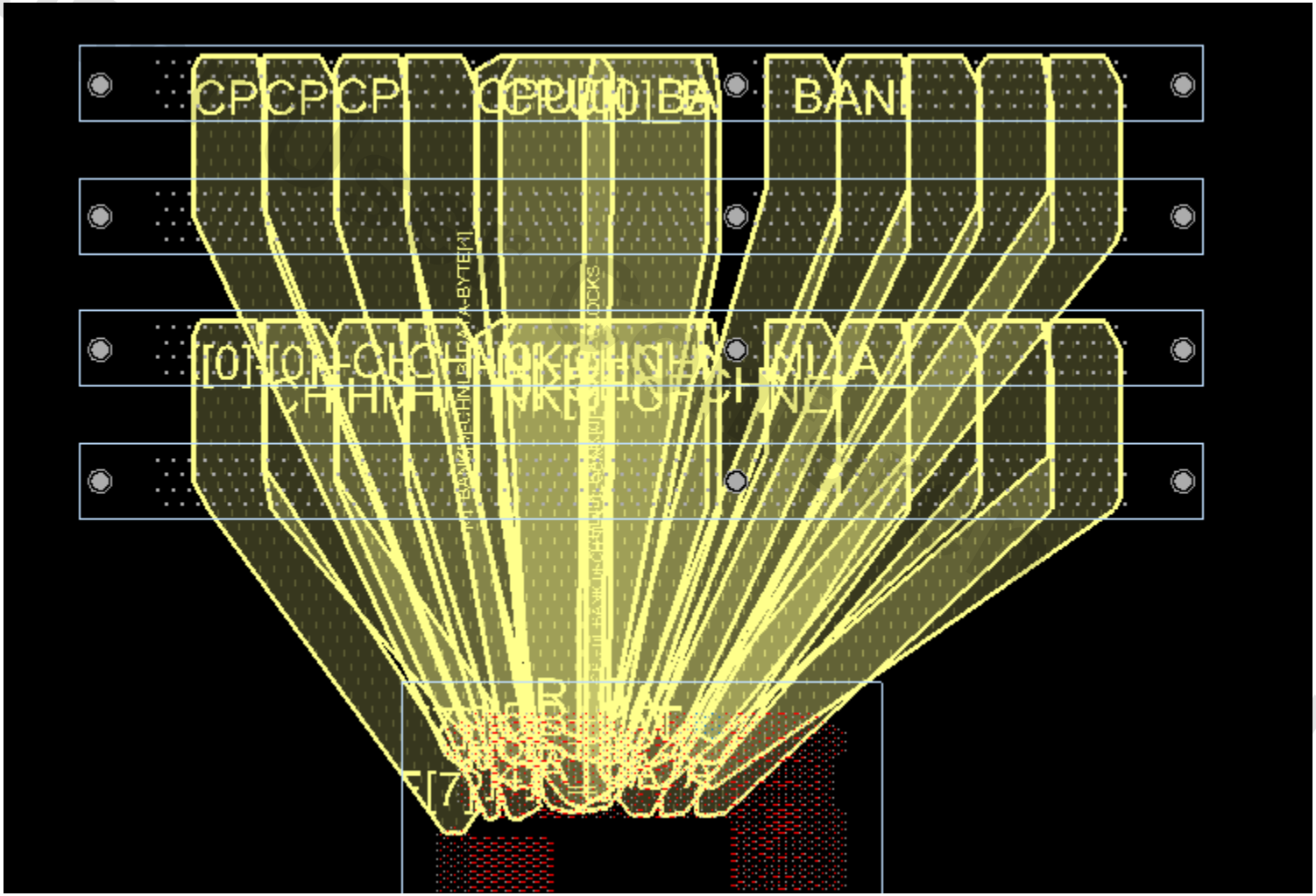
CPU[0]_BANK[0] – Down Hierarchy : Mid Level





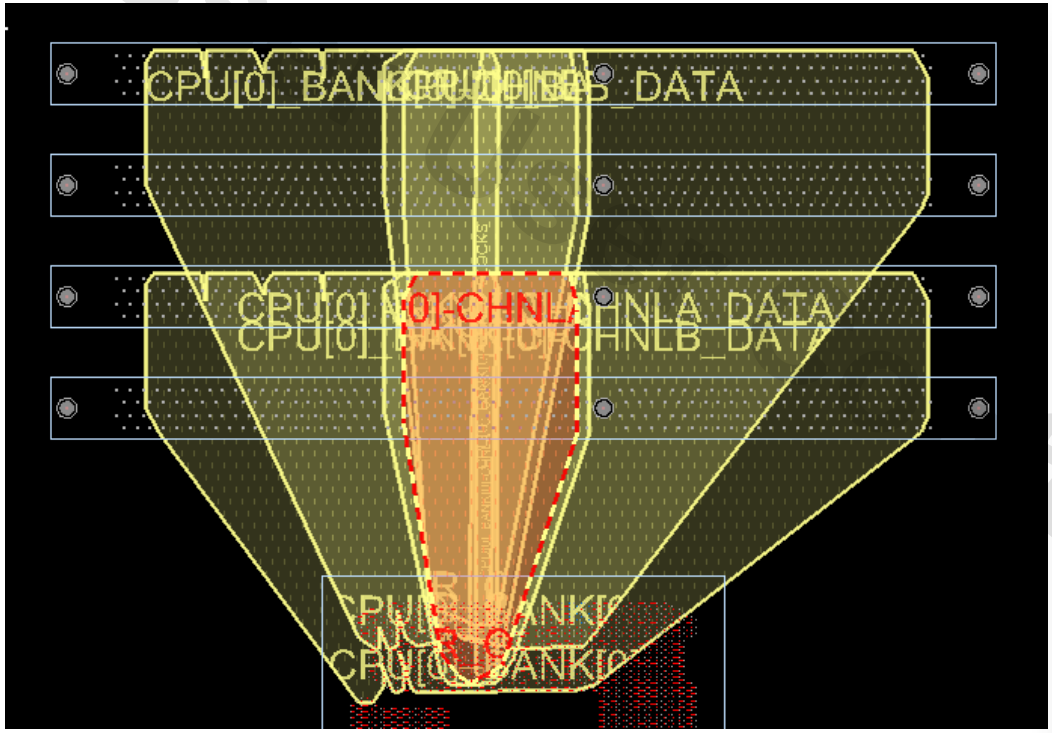
Net Groups

CPU[0]_BANK[0] – Hierarchy : Bottom Level



Net Groups

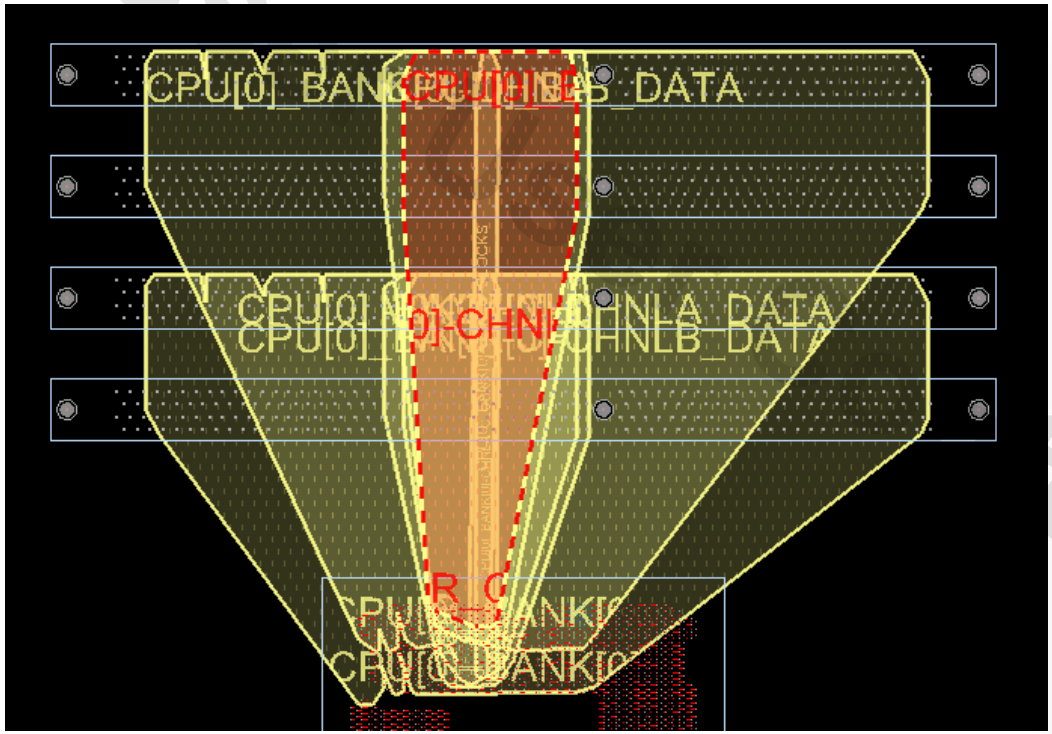
CPU[0]_BANK[0]-CHNLA_ADDR_CMD



Objects		
Type	S	Name
*		*
NGrp		CPU[0]_BANK[0]-CHNLA_ADDR_CMD (24)
Net		CPU0_BANK0-CHNLA_BA0
Net		CPU0_BANK0-CHNLA_BA1
Net		CPU0_BANK0-CHNLA_BA2
Net		CPU0_BANK0-CHNLA_CAS_N
Net		CPU0_BANK0-CHNLA_MA_PAR
Net		CPU0_BANK0-CHNLA_MA0
Net		CPU0_BANK0-CHNLA_MA1
Net		CPU0_BANK0-CHNLA_MA2
Net		CPU0_BANK0-CHNLA_MA3
Net		CPU0_BANK0-CHNLA_MA4
Net		CPU0_BANK0-CHNLA_MA5
Net		CPU0_BANK0-CHNLA_MA6
Net		CPU0_BANK0-CHNLA_MA7
Net		CPU0_BANK0-CHNLA_MA8
Net		CPU0_BANK0-CHNLA_MA9
Net		CPU0_BANK0-CHNLA_MA10
Net		CPU0_BANK0-CHNLA_MA11
Net		CPU0_BANK0-CHNLA_MA12
Net		CPU0_BANK0-CHNLA_MA13
Net		CPU0_BANK0-CHNLA_MA14
Net		CPU0_BANK0-CHNLA_MA15
Net		CPU0_BANK0-CHNLA_PAR_ERR_N
Net		CPU0_BANK0-CHNLA_RAS_N
Net		CPU0_BANK0-CHNLA_WE_N

Net Groups

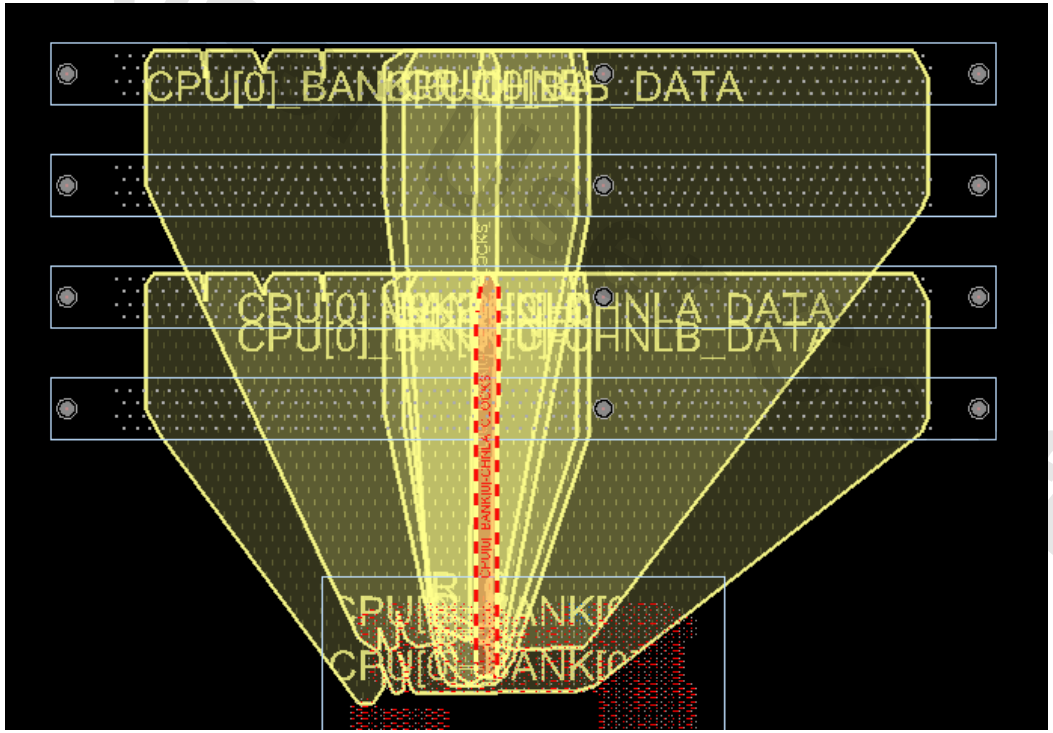
CPU[0]_BANK[0]-CHNLB_ADDR_CMD



Objects		
Type	S	Name
*		*
NGrp		⊟ CPU[0]_BANK[0]-CHNLB_ADDR_CMD (24)
Net		⊞ CPU0_BANK0-CHNLB_BA0
Net		⊞ CPU0_BANK0-CHNLB_BA1
Net		⊞ CPU0_BANK0-CHNLB_BA2
Net		⊞ CPU0_BANK0-CHNLB_CAS_N
Net		⊞ CPU0_BANK0-CHNLB_MA_PAR
Net		⊞ CPU0_BANK0-CHNLB_MA0
Net		⊞ CPU0_BANK0-CHNLB_MA1
Net		⊞ CPU0_BANK0-CHNLB_MA2
Net		⊞ CPU0_BANK0-CHNLB_MA3
Net		⊞ CPU0_BANK0-CHNLB_MA4
Net		⊞ CPU0_BANK0-CHNLB_MA5
Net		⊞ CPU0_BANK0-CHNLB_MA6
Net		⊞ CPU0_BANK0-CHNLB_MA7
Net		⊞ CPU0_BANK0-CHNLB_MA8
Net		⊞ CPU0_BANK0-CHNLB_MA9
Net		⊞ CPU0_BANK0-CHNLB_MA10
Net		⊞ CPU0_BANK0-CHNLB_MA11
Net		⊞ CPU0_BANK0-CHNLB_MA12
Net		⊞ CPU0_BANK0-CHNLB_MA13
Net		⊞ CPU0_BANK0-CHNLB_MA14
Net		⊞ CPU0_BANK0-CHNLB_MA15
Net		⊞ CPU0_BANK0-CHNLB_PAR_ERR_N
Net		⊞ CPU0_BANK0-CHNLB_RAS_N
Net		⊞ CPU0_BANK0-CHNLB_WE_N

Net Groups

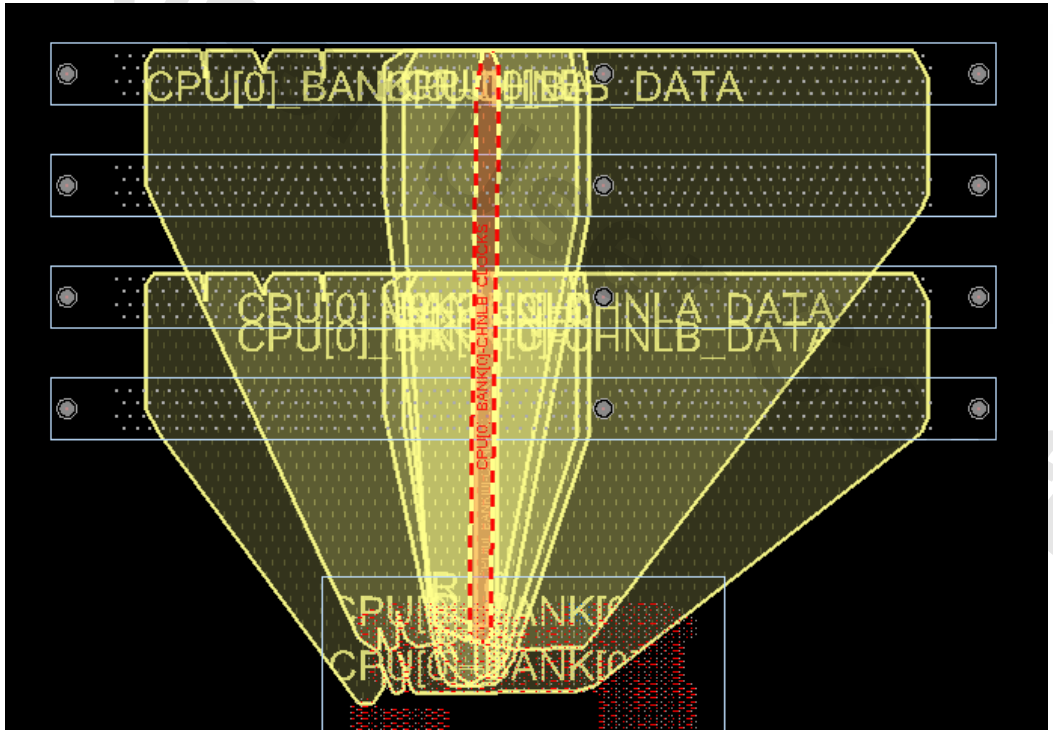
CPU[0]_BANK[0]-CHNLA_CLOCKS



Objects		
Type	S	Name
*		*
NGrp		⊟ CPU[0]_BANK[0]-CHNLA_CLOCKS (4)
DPr		⊞ CPU0_BANK0-CHNLA_CK_0
DPr		⊞ CPU0_BANK0-CHNLA_CK_1
DPr		⊞ CPU0_BANK0-CHNLA_CK_2
DPr		⊞ CPU0_BANK0-CHNLA_CK_3

Net Groups

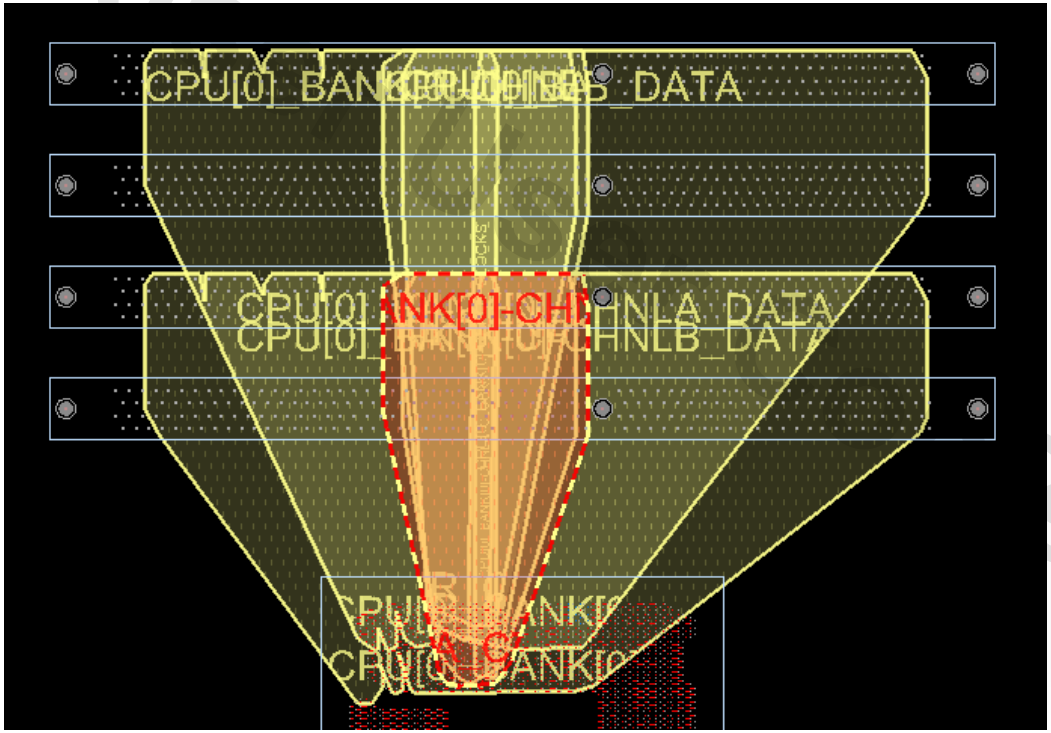
CPU[0]_BANK[0]-CHNLB_CLOCKS



Objects		
Type	S	Name
*		*
NGrp		⊟ CPU[0]_BANK[0]-CHNLB_CLOCKS (4)
DPr		⊞ CPU0_BANK0-CHNLB_CK_0
DPr		⊞ CPU0_BANK0-CHNLB_CK_1
DPr		⊞ CPU0_BANK0-CHNLB_CK_2
DPr		⊞ CPU0_BANK0-CHNLB_CK_3

Net Groups

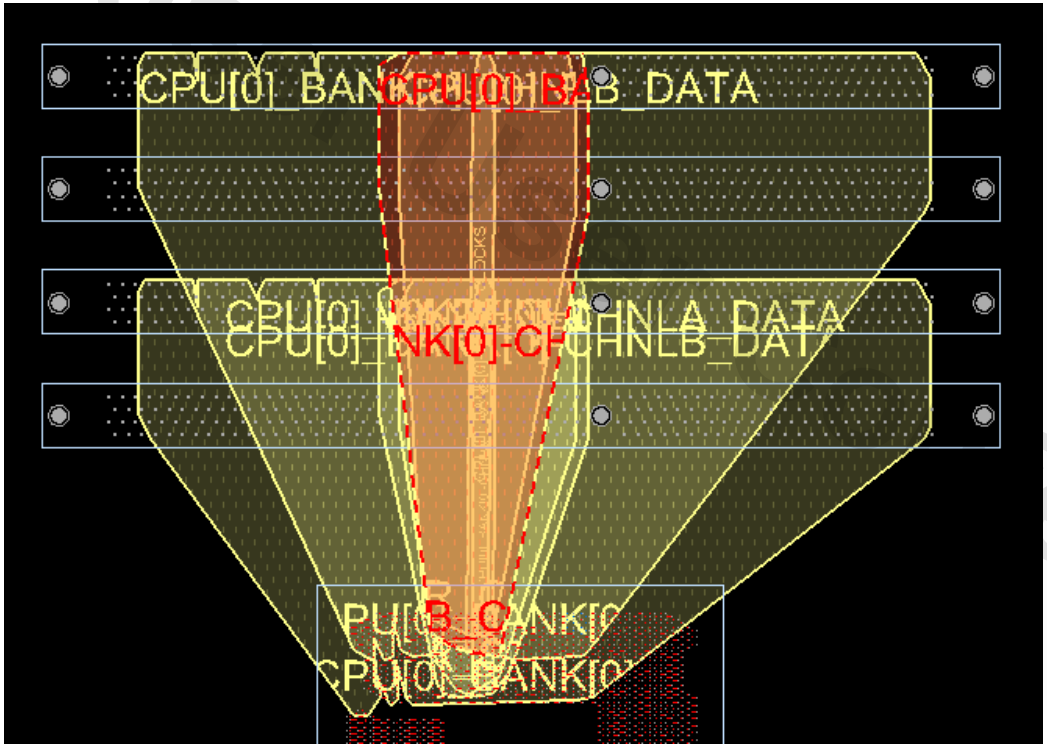
CPU[0]_BANK[0]-CHNLA_CTRL



Objects		
Type	S	Name
*		*
NGrp		⊟ CPU[0]_BANK[0]-CHNLA_CTRL (16)
Net		⊞ CPU0_BANK0-CHNLA_CKE0
Net		⊞ CPU0_BANK0-CHNLA_CKE1
Net		⊞ CPU0_BANK0-CHNLA_CKE2
Net		⊞ CPU0_BANK0-CHNLA_CKE3
Net		⊞ CPU0_BANK0-CHNLA_CS_N0
Net		⊞ CPU0_BANK0-CHNLA_CS_N1
Net		⊞ CPU0_BANK0-CHNLA_CS_N2
Net		⊞ CPU0_BANK0-CHNLA_CS_N3
Net		⊞ CPU0_BANK0-CHNLA_CS_N4
Net		⊞ CPU0_BANK0-CHNLA_CS_N5
Net		⊞ CPU0_BANK0-CHNLA_CS_N6
Net		⊞ CPU0_BANK0-CHNLA_CS_N7
Net		⊞ CPU0_BANK0-CHNLA_ODT0
Net		⊞ CPU0_BANK0-CHNLA_ODT1
Net		⊞ CPU0_BANK0-CHNLA_ODT2
Net		⊞ CPU0_BANK0-CHNLA_ODT3

Net Groups

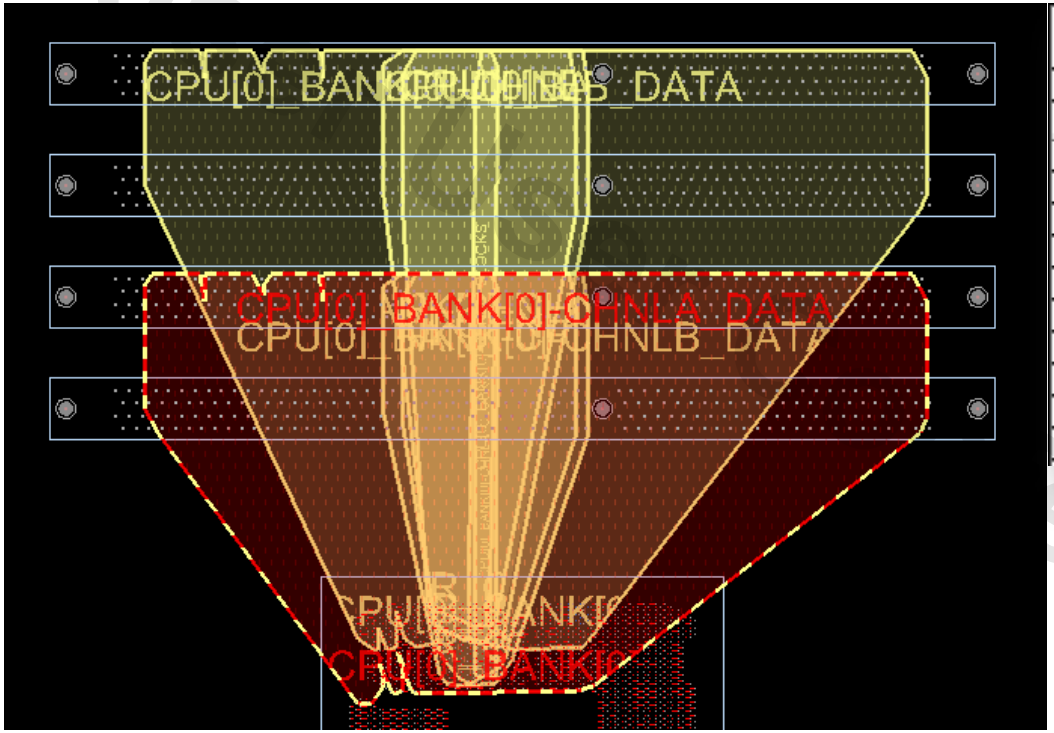
CPU[0]_BANK[0]-CHNLB_CTRL



Objects		
Type	S	Name
*		*
NGrp		⊟ CPU[0]_BANK[0]-CHNLB_CTRL (16)
Net		⊞ CPU0_BANK0-CHNLB_CKE0
Net		⊞ CPU0_BANK0-CHNLB_CKE1
Net		⊞ CPU0_BANK0-CHNLB_CKE2
Net		⊞ CPU0_BANK0-CHNLB_CKE3
Net		⊞ CPU0_BANK0-CHNLB_CS_N0
Net		⊞ CPU0_BANK0-CHNLB_CS_N1
Net		⊞ CPU0_BANK0-CHNLB_CS_N2
Net		⊞ CPU0_BANK0-CHNLB_CS_N3
Net		⊞ CPU0_BANK0-CHNLB_CS_N4
Net		⊞ CPU0_BANK0-CHNLB_CS_N5
Net		⊞ CPU0_BANK0-CHNLB_CS_N6
Net		⊞ CPU0_BANK0-CHNLB_CS_N7
Net		⊞ CPU0_BANK0-CHNLB_ODT0
Net		⊞ CPU0_BANK0-CHNLB_ODT1
Net		⊞ CPU0_BANK0-CHNLB_ODT2
Net		⊞ CPU0_BANK0-CHNLB_ODT3

Net Groups

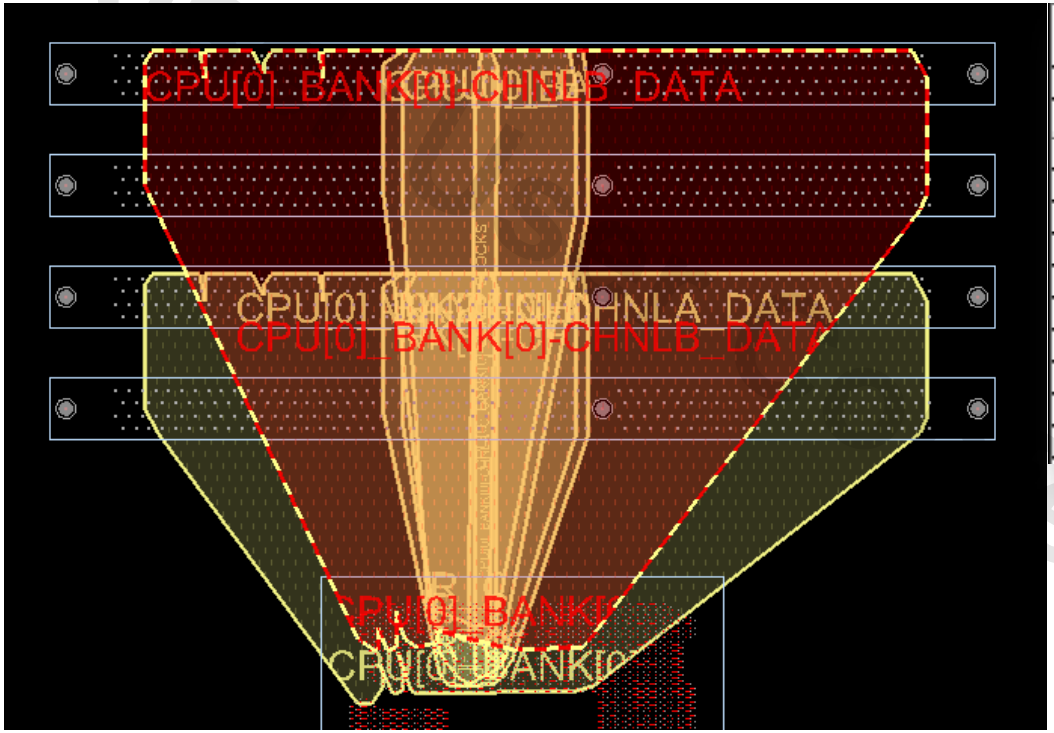
CPU[0]_BANK[0]-CHNLA_DATA



Objects		
Type	S	Name
*		*
NGrp		⊟ CPU[0]_BANK[0]-CHNLA_DATA (9)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[0] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[1] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[2] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[3] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[4] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[5] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[6] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-BYTE[7] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLA_DATA-ECC (10)

Net Groups

CPU[0]_BANK[0]-CHNLB_DATA

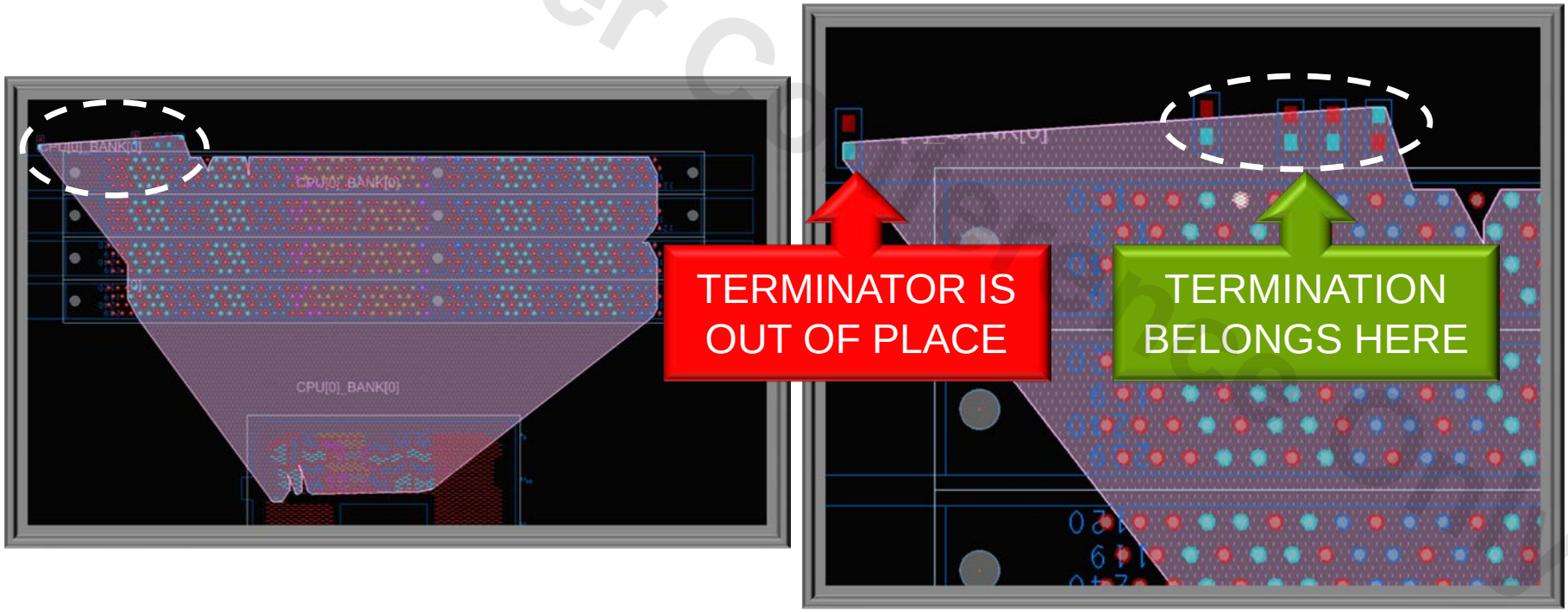


Objects		
Type	S	Name
*		*
NGrp		⊟ CPU[0]_BANK[0]-CHNLB_DATA (9)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[0] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[1] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[2] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[3] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[4] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[5] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[6] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-BYTE[7] (10)
NGrp		⊞ CPU[0]_BANK[0]-CHNLB_DATA-ECC (10)

Net Groups and Placement

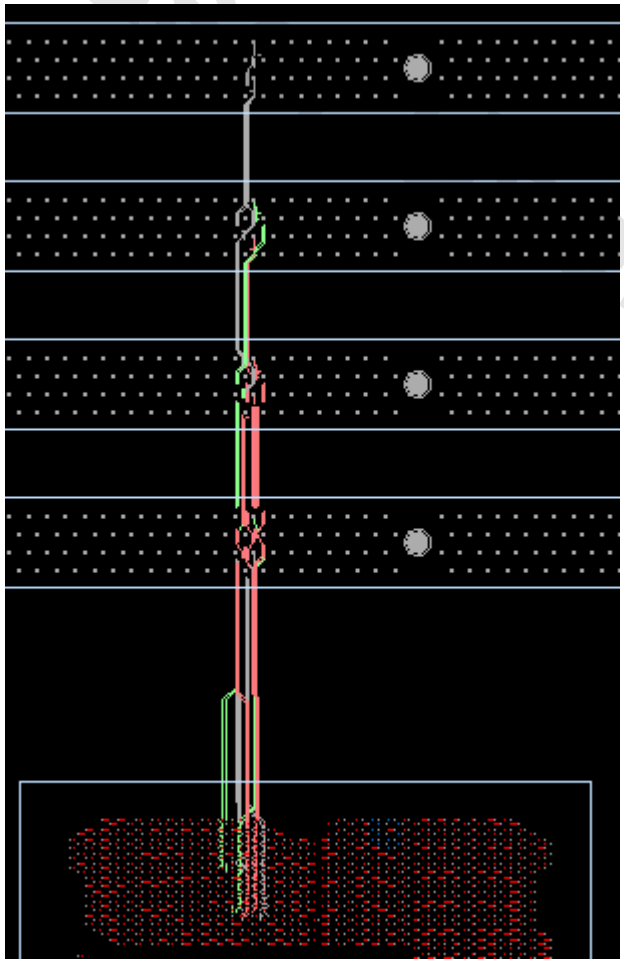
Quick and easy way to “verify” your placement

- The container gives you a way to visualize the overall “routing domain” of the interface
- Visual placement checks let you see parts “out-of-place”
  - The polygon envelops **ALL** the pins of nets in the net group



Plan (Design Planning Option)

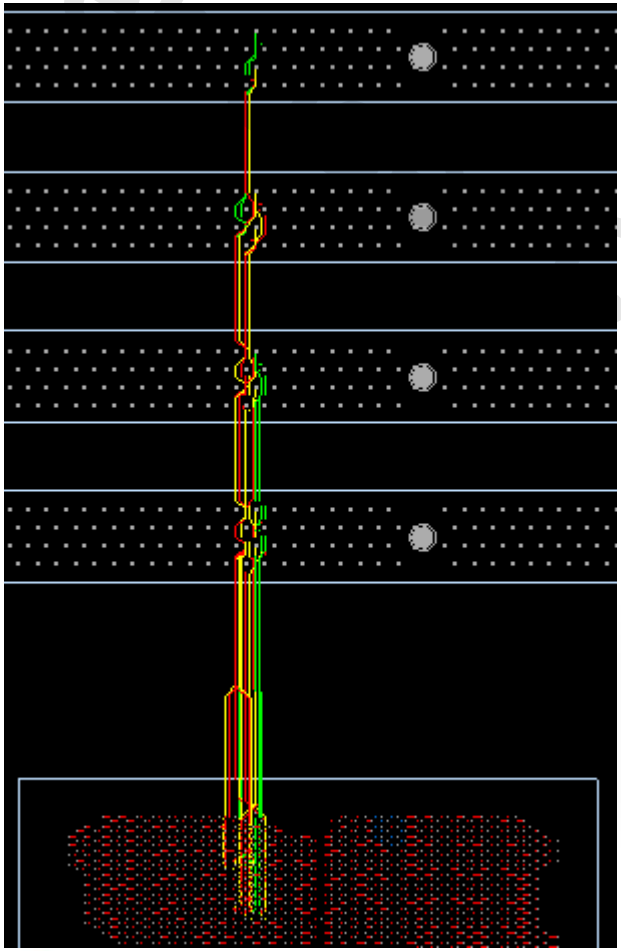
1st CLOCKS (Channel A & B)

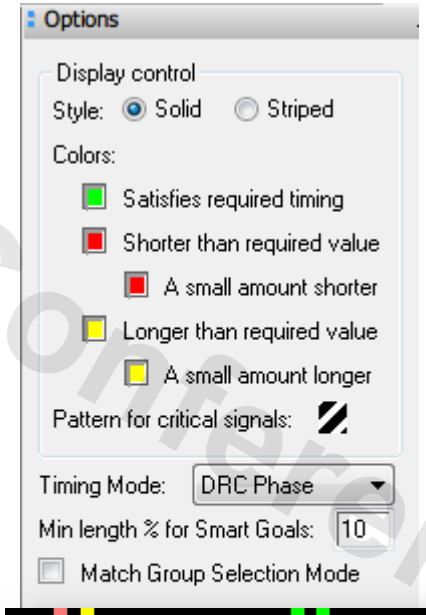


```
INFO (SPGRE-16): Status: Topological planning completed normally
INFO (SPGRE-16):   Number of rats scheduled = 16
INFO (SPGRE-16):   Number of spatial unroutes for scheduled rats = 0
INFO (SPGRE-16):   Number of topological unroutes for scheduled rats = 0
INFO (SPGRE-16):   Number of crossings on scheduled rats = 0
INFO (SPGRE-16):   Number of clearance on scheduled rats = 0
INFO (SPGRE-16):   Number of electrical violations on sceduled rats = 27
INFO (SPGRE-16):   Number of timing constraints on scheduled rats = 32
INFO (SPGRE-16):   Number of timing constraint violations on scheduled rats = 15
INFO (SPGRE-16):   DiffPair Uncoupled Plan Length = 1225.584 MIL
INFO (SPGRE-16):   DiffPair Gather Plan Length = 1203.927 MIL
INFO (SPGRE-16):   DiffPair Phase Mismatch = 300.889 MIL
INFO (SPGRE-16):   Number of DiffPair Unroutes = 0
INFO (SPGRE-16):   Number of vias on scheduled rats = 16
INFO (SPGRE-16):   Routed length of scheduled rats = 42299.679 MIL
INFO (SPGRE-16):   Percent complete on scheduled rats =  100.00%
INFO (SPGRE-16):   Execution time = 66 seconds
INFO (SPGRE-16):   Memory currently in use = 158804 KB
```

Plan (Design Planning Option)

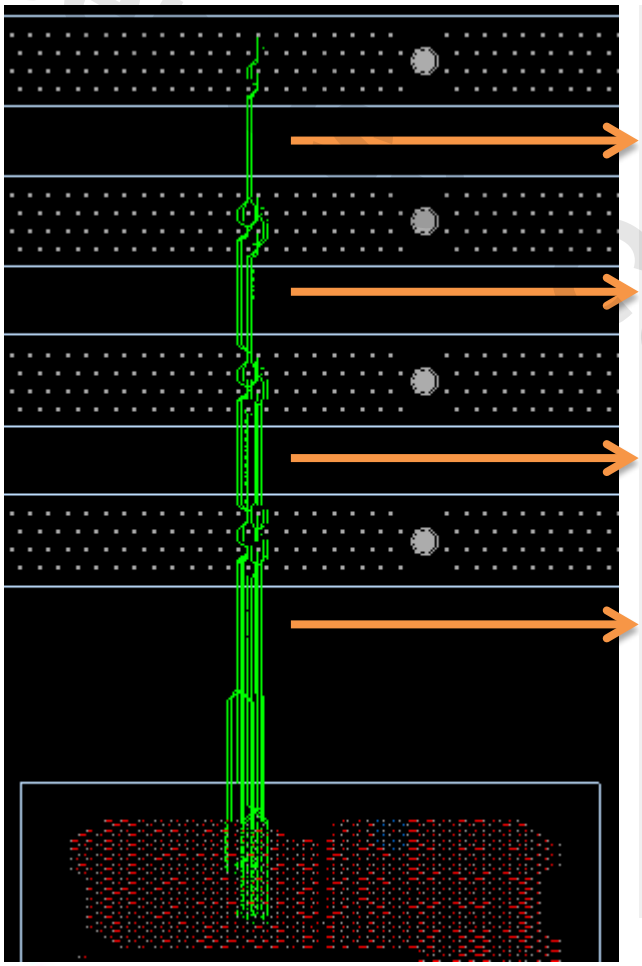
1st CLOCKS (Channel A & B)
- Timing vision (High-Speed option)

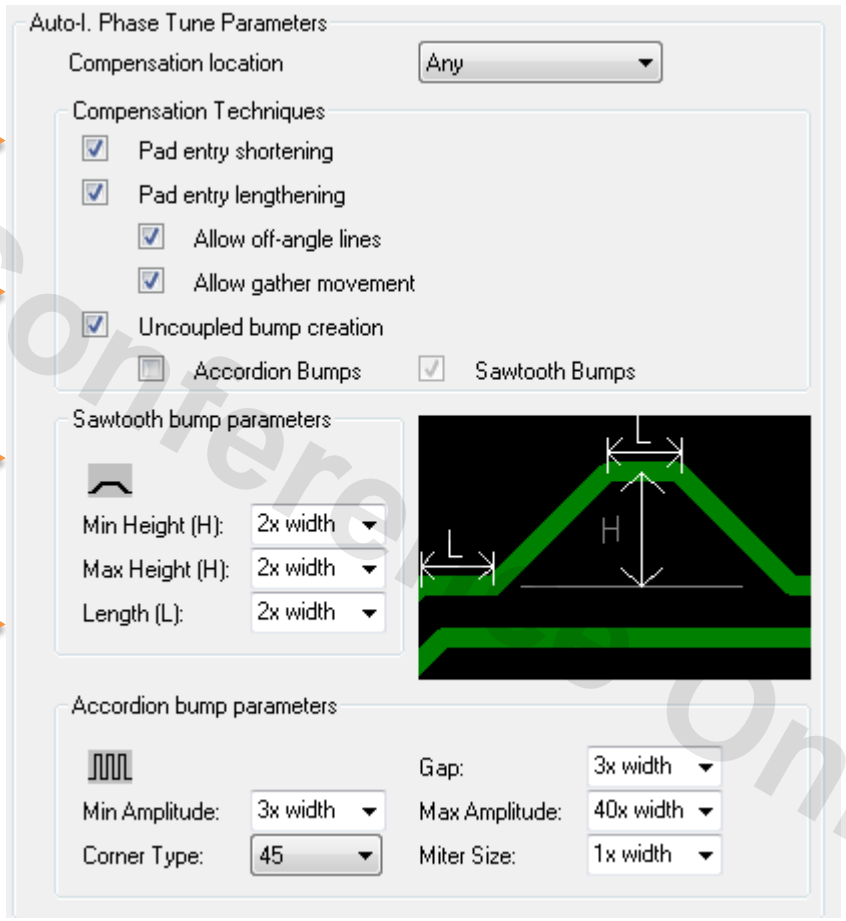




Plan (Design Planning Option)

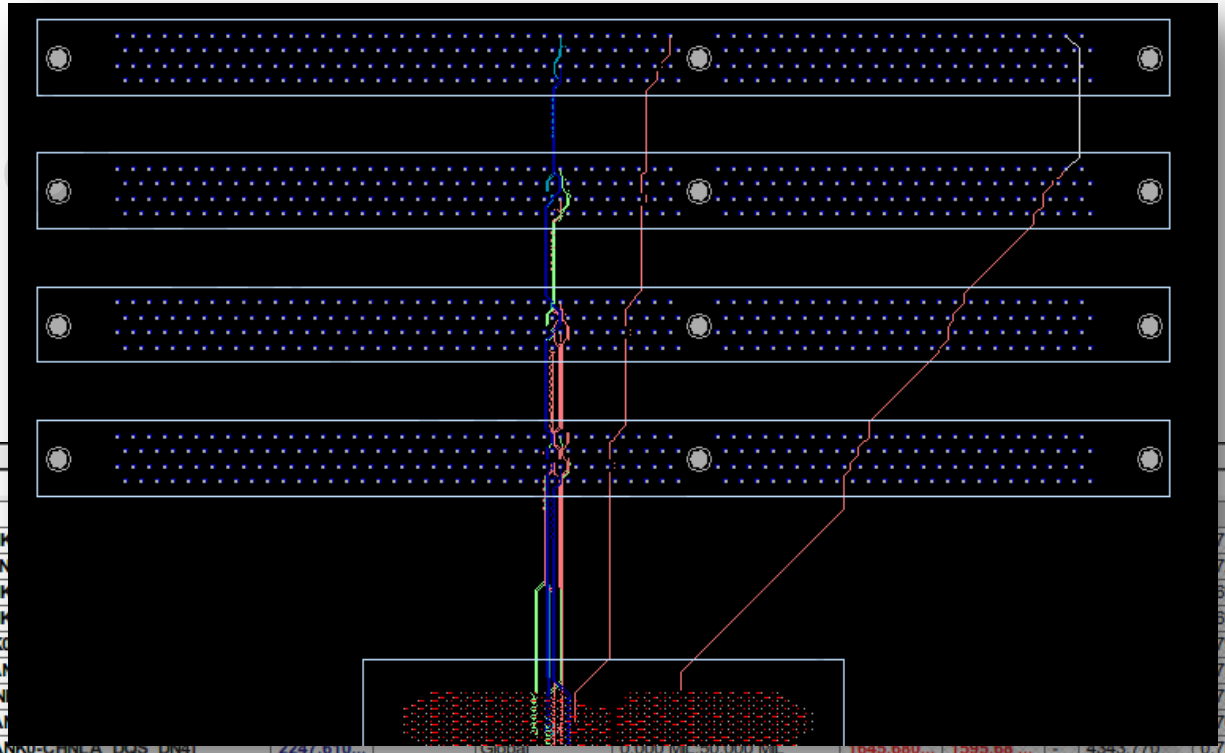
1st CLOCKS (Channel A & B)
- AiPT (High-Speed option)





Plan (Design Planning Option)

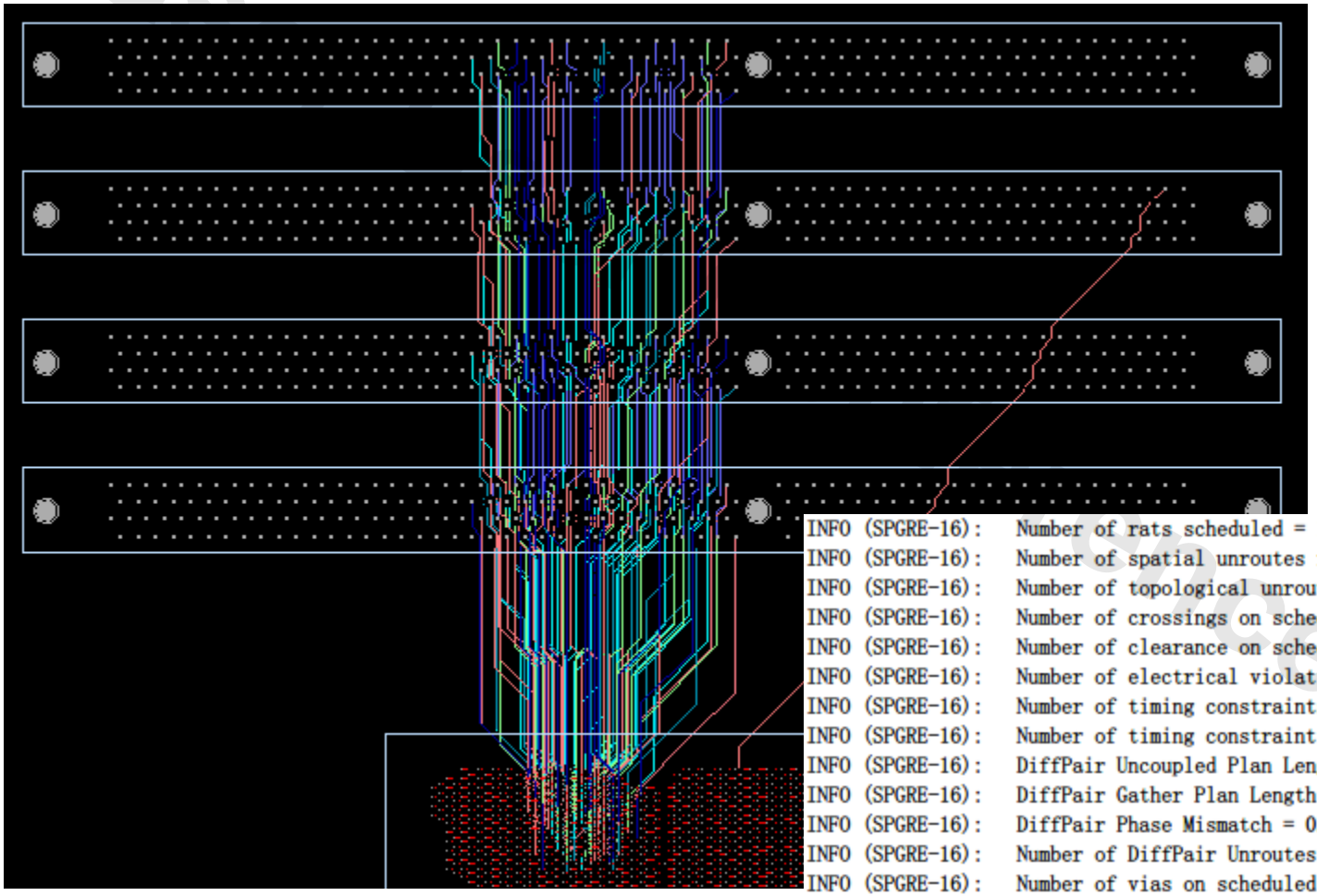
2nd Target pre-routing



Type	S	Name									ns
*		*									
MGrp		DRVR_TO_DIMM (264)									
PPr		U95.R17:DIMM5.71 [CPU0_BANK									7180
PPr		U95.L17:DIMM5.190 [CPU0_BAN									7244
PPr		U95.P24:DIMM5.52 [CPU0_BANK									6928
PPr		U95.T16:DIMM5.74 [CPU0_BANK									6984
PPr		U95.T38:DIMM5.6 [CPU0_BANK0									7964
PPr		U95.AD38:DIMM5.15 [CPU0_BA									7591
PPr		U95.W31:DIMM5.24 [CPU0_BAN									7503
PPr		U95.AA33:DIMM5.33 [CPU0_BA									7600
PPr		U95.AC11:DIMM5.84 [CPU0_BANK0-CHNLA_DQS_DN4]	2247.610...		Global	0.000 MIL:50.000 MIL	1645.680...	1595.66 ...	-	4345.770	0.7544
PPr		DIMM5.93:U95.AB8 [CPU0_BANK0-CHNLA_DQS_DN5]		2003.140...	Global	0.000 MIL:50.000 MIL	1734.720...	1684.72 ...	-	4254.730	0.7416
PPr		U95.U11:DIMM5.102 [CPU0_BANK0-CHNLA_DQS_DN6]	1564.89 ...		Global	0.000 MIL:50.000 MIL	1739.740...	1689.74 ...	-	4249.710	0.7464
PPr		U95.A39:DIMM7.4 [CPU0_BANK0-CHNLB_DQ1]	1428.890...		Global	TARGET	TARGET			5989.450	1.061
PPr		U95.AB28:DIMM5.42 [CPU0_BANK0-CHNLA_DQS_DN8]	1642.300...		Global	0.000 MIL:50.000 MIL	1763.550...	1713.55 ...	-	4225.900	0.7328
MGrp		DRVR_DIMM_CLK (48)						2248.3 MIL			
PPr		U95.AA25:DIMM5.50 [CPU0_BANK0-CHNLA_CKE0]	1008.32 ...		Global	0.000 MIL:50.000 MIL	1844.290...	1794.29 ...	-	3203.580	0.5574
PPr		U95.T26:DIMM5.169 [CPU0_BANK0-CHNLA_CKE1]	1008.38 ...		Global	0.000 MIL:50.000 MIL	2163.960...	2113.96 ...	-	2883.910	0.5000
PPr		U95.U27:DIMM6.50 [CPU0_BANK0-CHNLA_CKE2]	879.94 MIL		Global	0.000 MIL:50.000 MIL	1457.670...	1407.67 ...	-	3590.200	0.6285
PPr		U95.J25:DIMM8.50 [CPU0_BANK0-CHNLB_CKE2]	1099.410...		Global	TARGET	TARGET			5047.870	0.8874
PPr		U95.Y24:DIMM5.185 [CPU0_BANK0-CHNLA_CK_DN0]	1098.09 ...		Global	0.000 MIL:50.000 MIL	2295.024...	2245.02 ...	-	2752.846	0.4572

Plan (Design Planning Option)

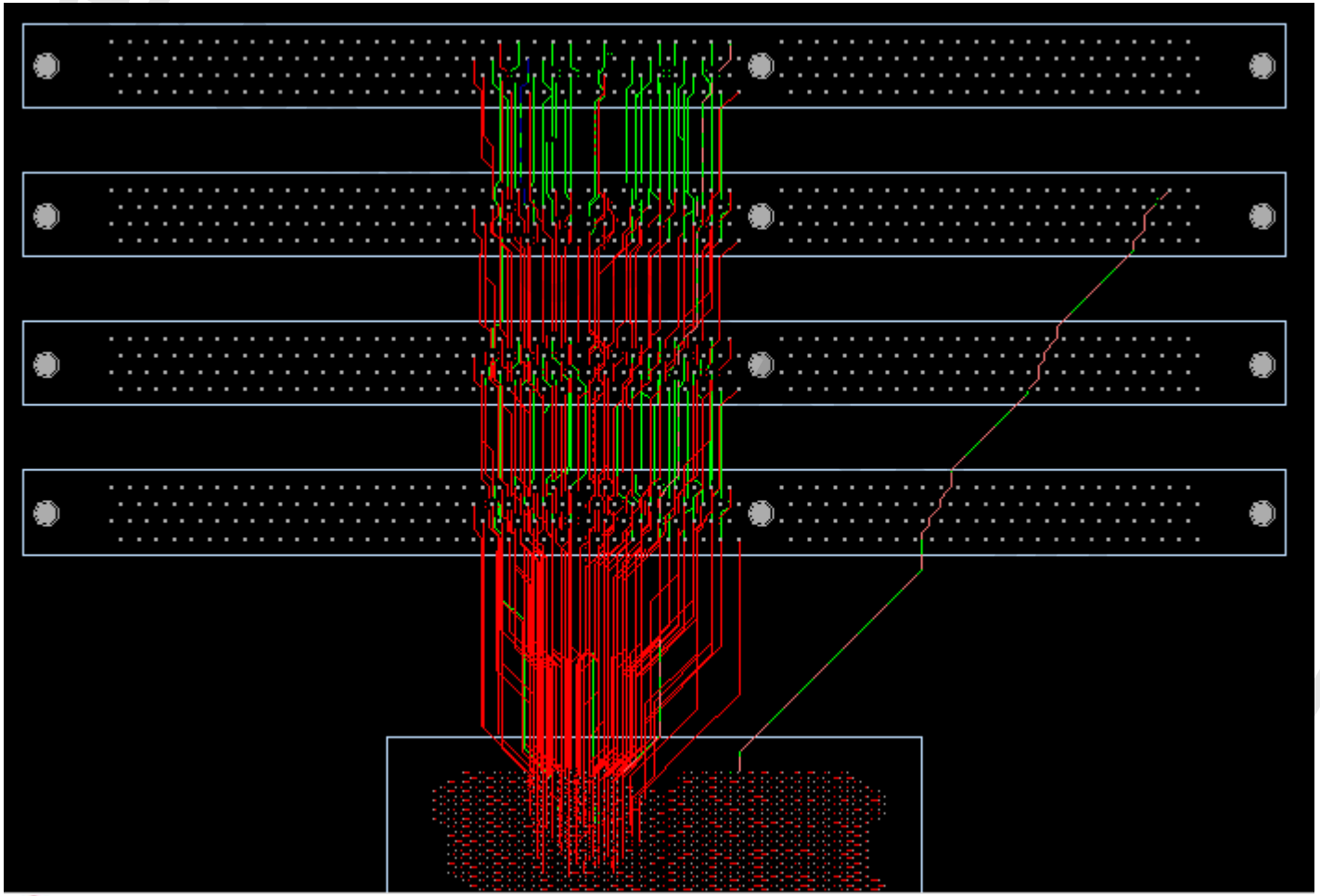
3rd ADDR CMD & CTRL (Channel A & B)



```
INFO (SPGRE-16):   Number of rats scheduled = 128
INFO (SPGRE-16):   Number of spatial unroutes for scheduled rats = 0
INFO (SPGRE-16):   Number of topological unroutes for scheduled rats = 0
INFO (SPGRE-16):   Number of crossings on scheduled rats = 0
INFO (SPGRE-16):   Number of clearance on scheduled rats = 0
INFO (SPGRE-16):   Number of electrical violations on sceduled rats = 78
INFO (SPGRE-16):   Number of timing constraints on scheduled rats = 256
INFO (SPGRE-16):   Number of timing constraint violations on scheduled rats = 78
INFO (SPGRE-16):   DiffPair Uncoupled Plan Length = 0.000 MIL
INFO (SPGRE-16):   DiffPair Gather Plan Length = 0.000 MIL
INFO (SPGRE-16):   DiffPair Phase Mismatch = 0.000 MIL
INFO (SPGRE-16):   Number of DiffPair Unroutes = 0
INFO (SPGRE-16):   Number of vias on scheduled rats = 80
INFO (SPGRE-16):   Routed length of scheduled rats = 221625.204 MIL
INFO (SPGRE-16):   Percent complete on scheduled rats =  100.00%
INFO (SPGRE-16):   Execution time = 63 seconds
INFO (SPGRE-16):   Memory currently in use = 201123 KB
```

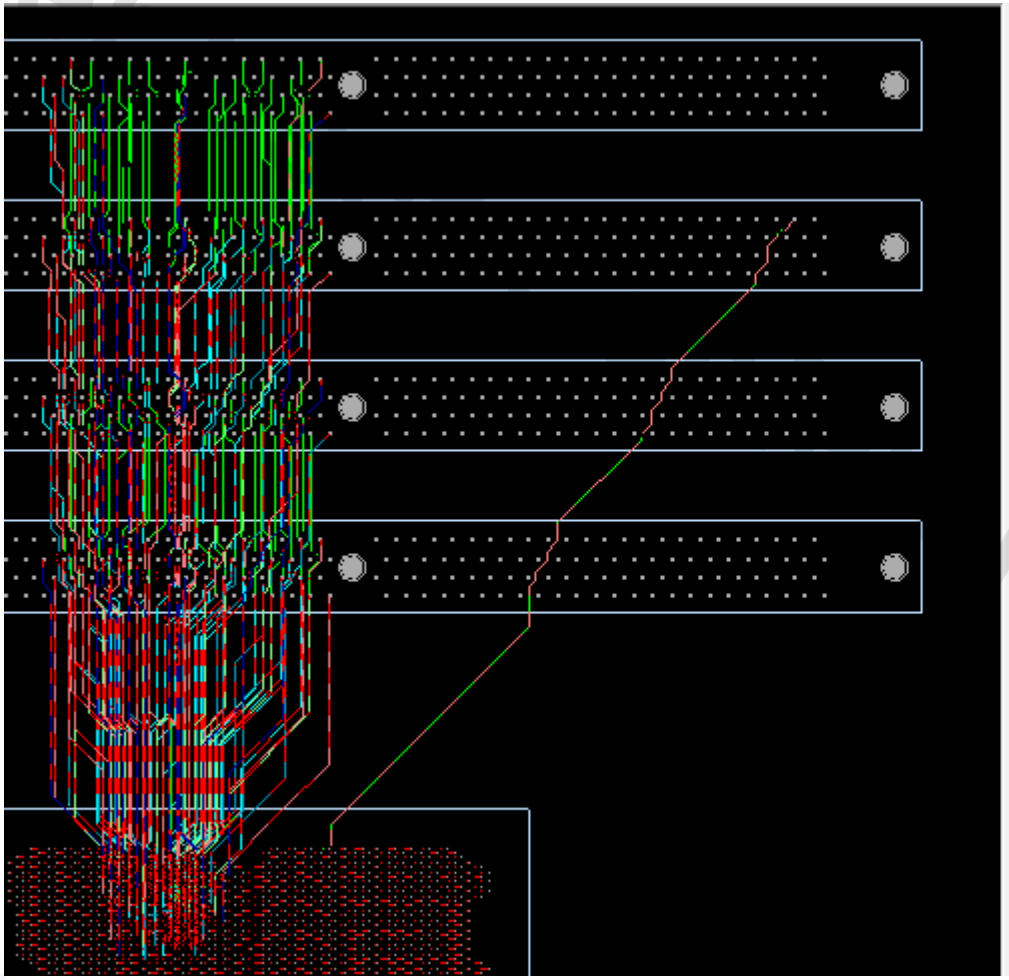
Plan (Design Planning Option)

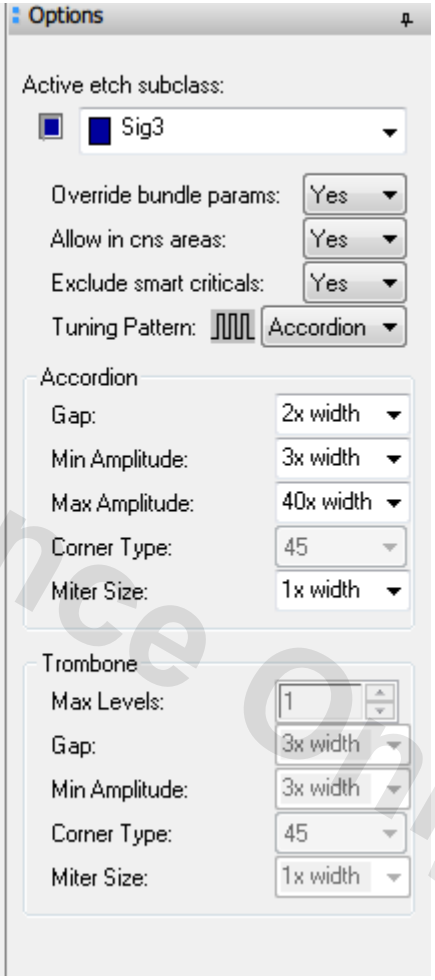
3rd ADDR CMD & CTRL (Channel A & B)
- Timing vision (High-Speed option)



Plan (Design Planning Option)

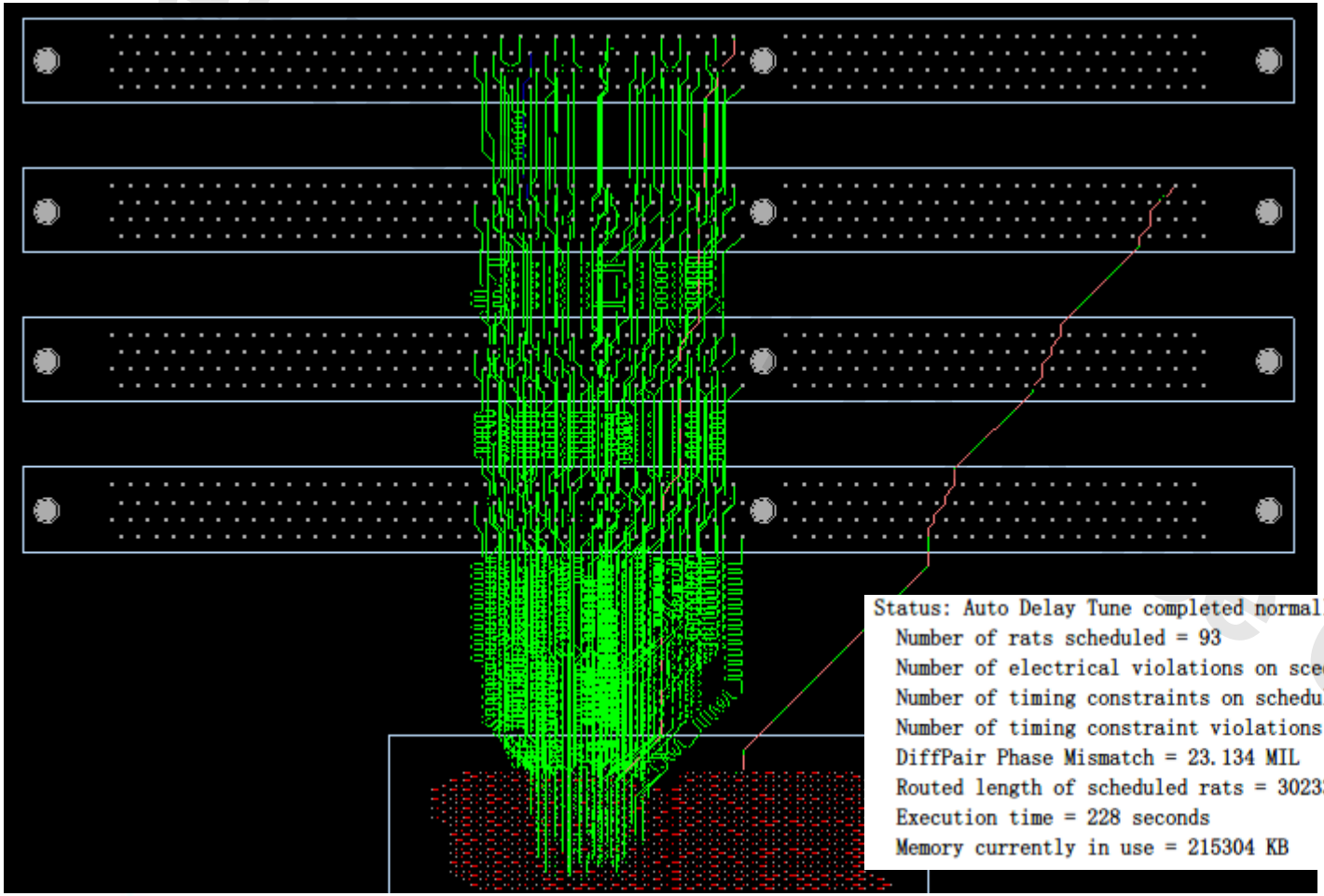
3rd ADDR CMD & CTRL (Channel A & B)
- AiDT(High-Speed option)





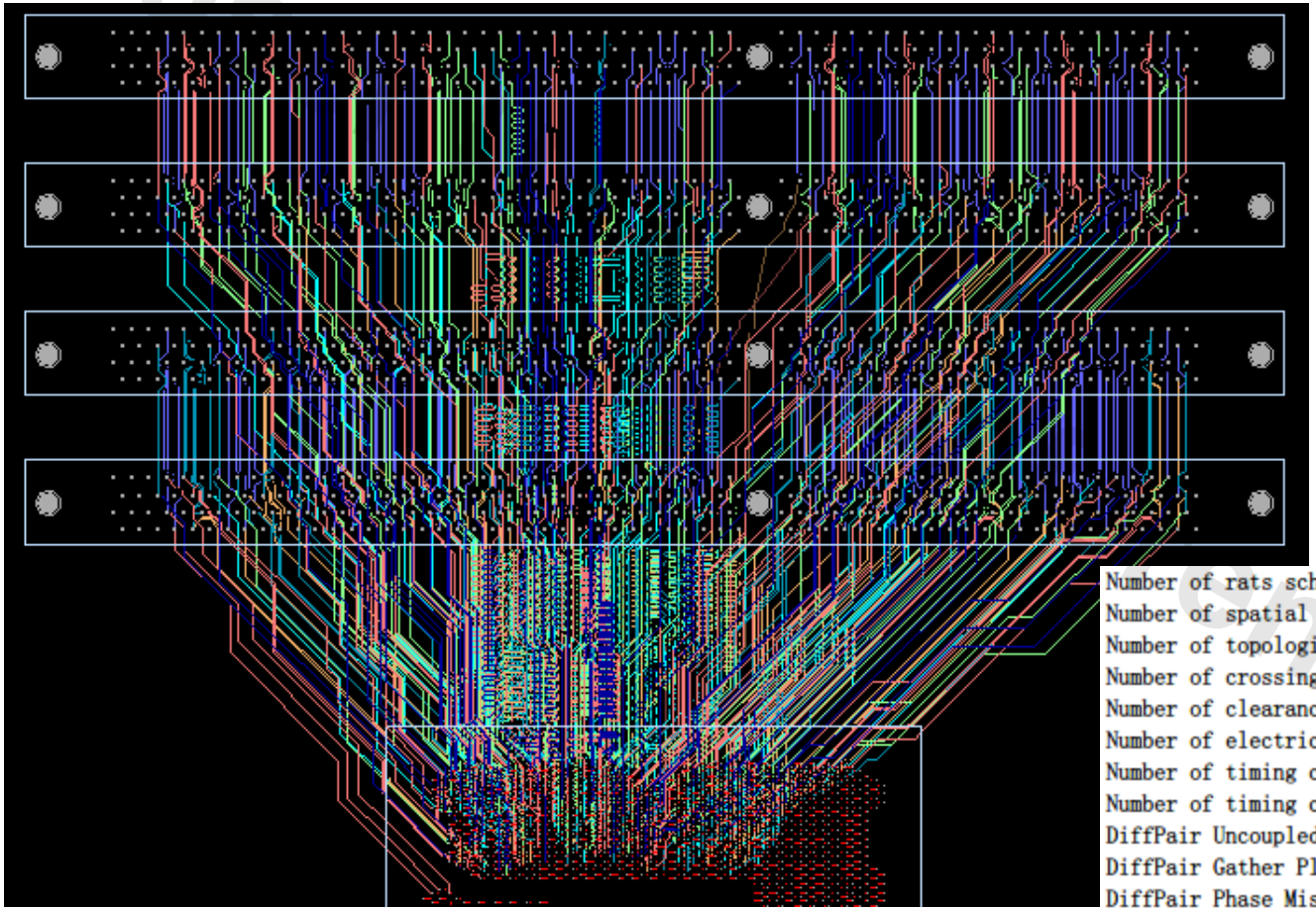
Plan (Design Planning Option)

3rd ADDR CMD & CTRL (Channel A & B)
- AiDT(High-Speed option)



Plan (Design Planning Option)

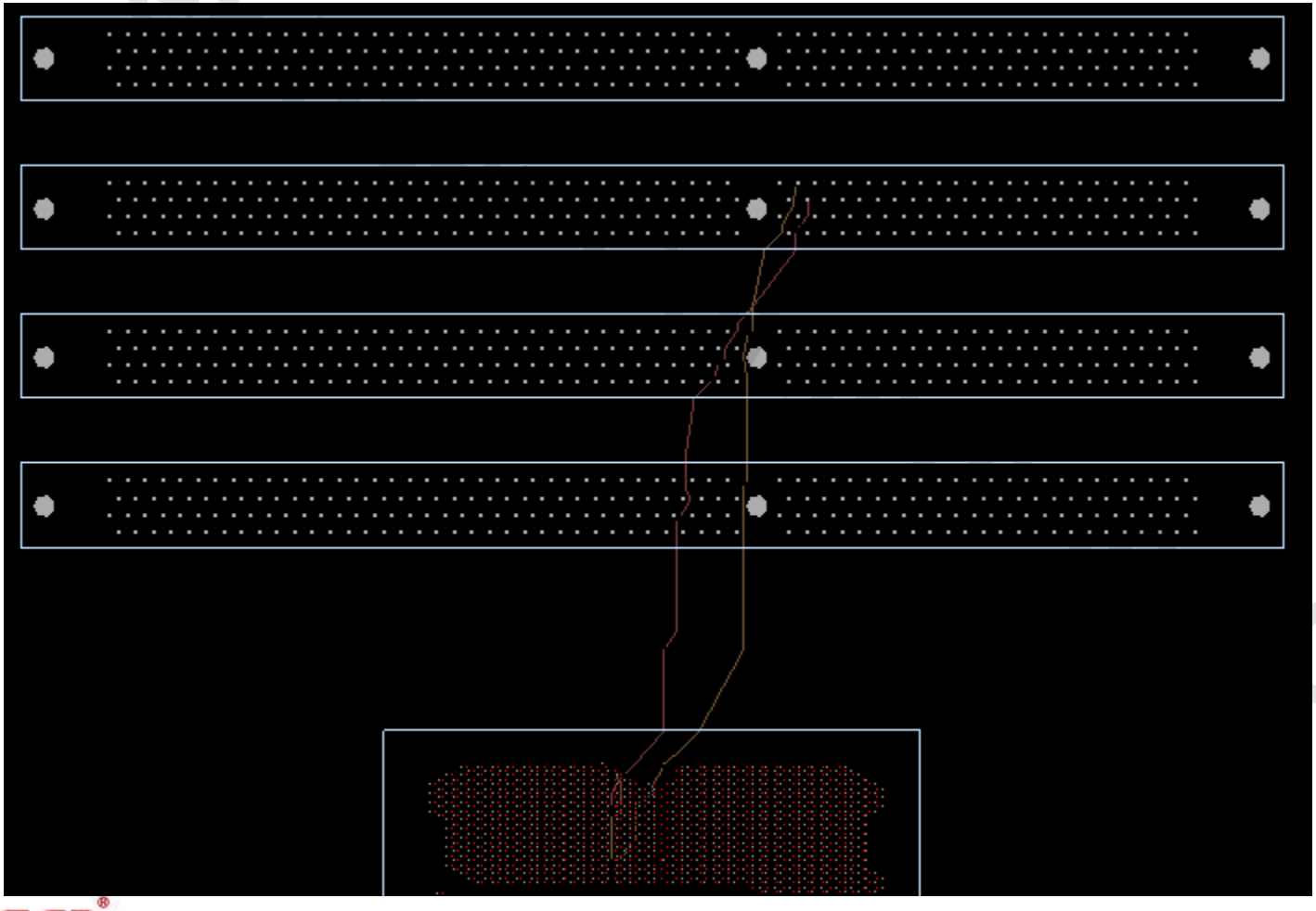
4th DATA (Channel A & B)



```
Number of rats scheduled = 432
Number of spatial unroutes for scheduled rats = 0
Number of topological unroutes for scheduled rats = 2
Number of crossings on scheduled rats = 0
Number of clearance on scheduled rats = 0
Number of electrical violations on sceduled rats = 336
Number of timing constraints on scheduled rats = 864
Number of timing constraint violations on scheduled rats = 277
DiffPair Uncoupled Plan Length = 16723.220 MIL
DiffPair Gather Plan Length = 15385.325 MIL
DiffPair Phase Mismatch = 1231.296 MIL
Number of DiffPair Unroutes = 0
Number of vias on scheduled rats = 216
Routed length of scheduled rats = 722961.758 MIL
Percent complete on scheduled rats =  99.54%
Execution time = 676 seconds
Memory currently in use = 217572 KB
```

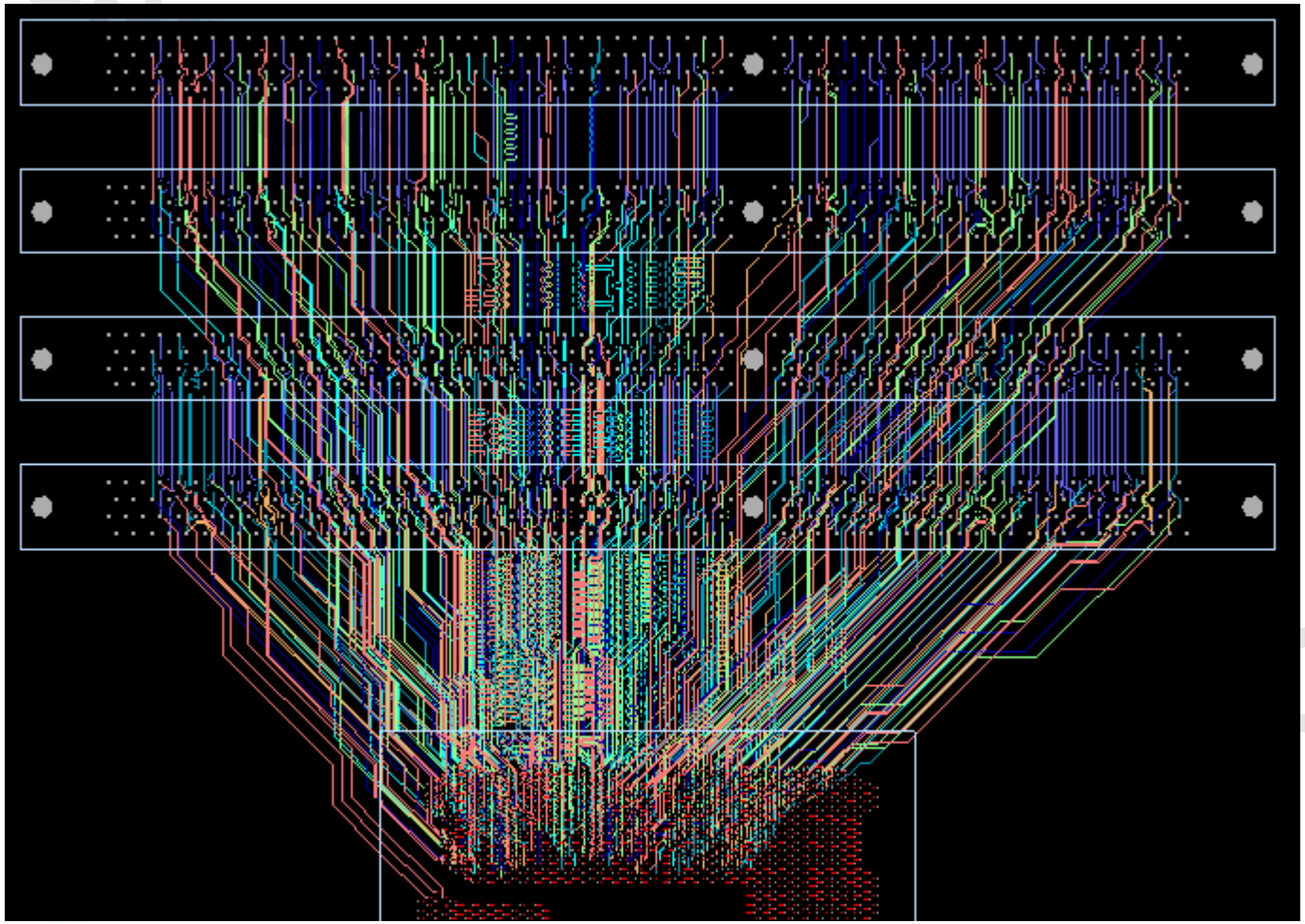
Plan (Design Planning Option)

4th DATA (Channel A & B)
- Unplanning



Plan (Design Planning Option)

4th DATA (Channel A & B)
- Manual add connection

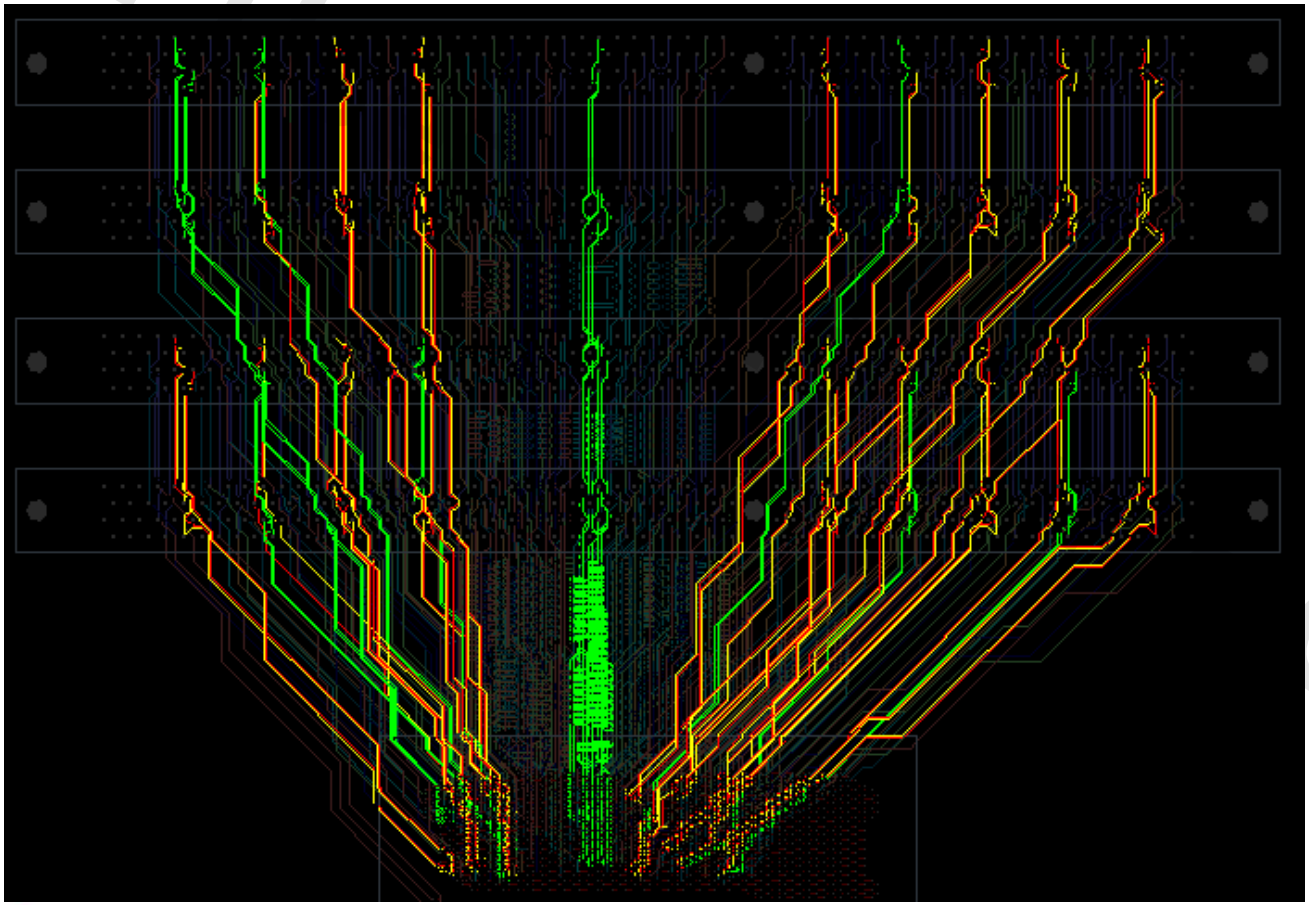


Plan (Design Planning Option)

4th DATA (Channel A & B)

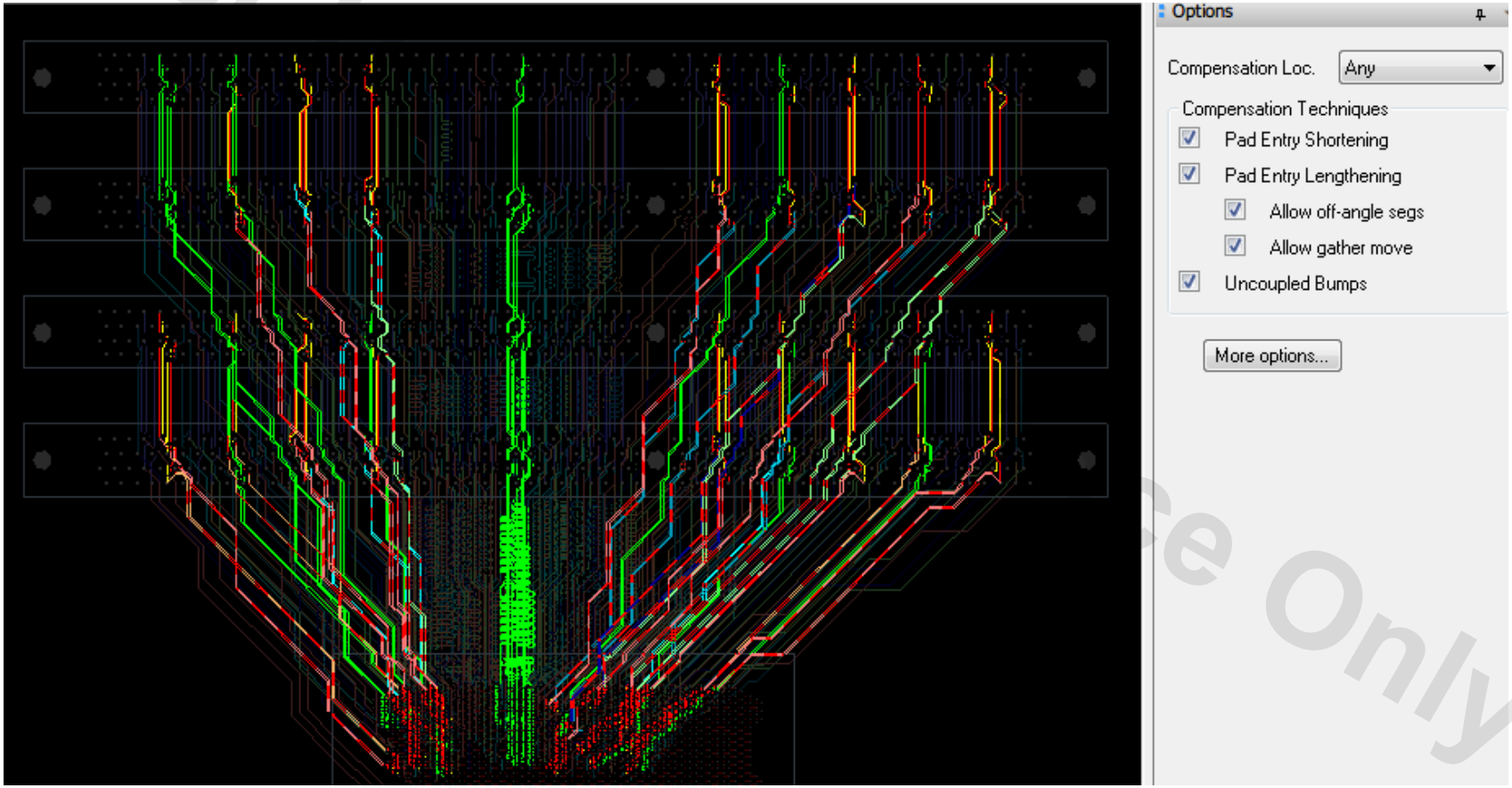
- Timing vision (High-Speed option)

- DRC Phase view



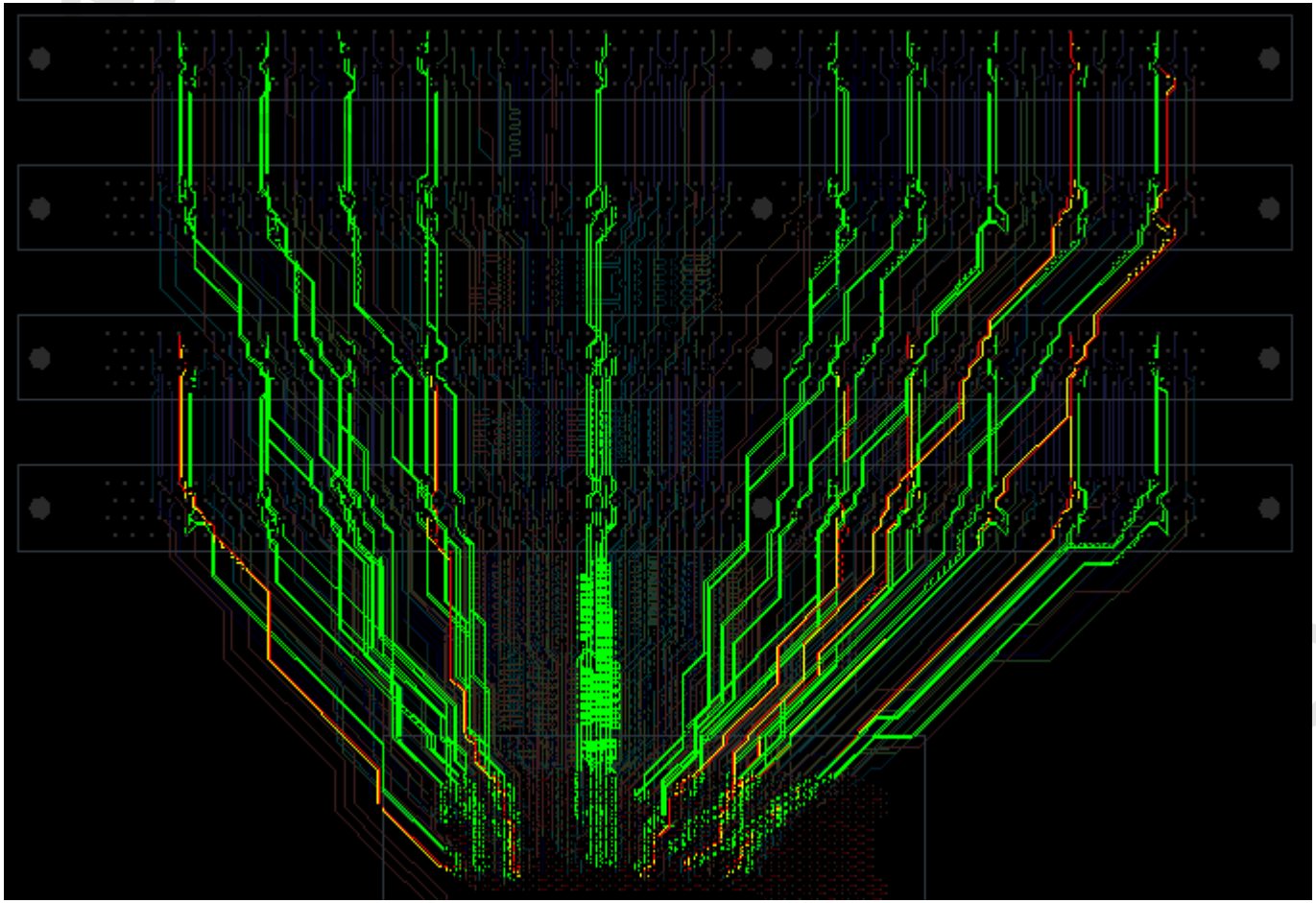
Plan (Design Planning Option)

4th DATA (Channel A & B)
- AiPT(High-Speed option)



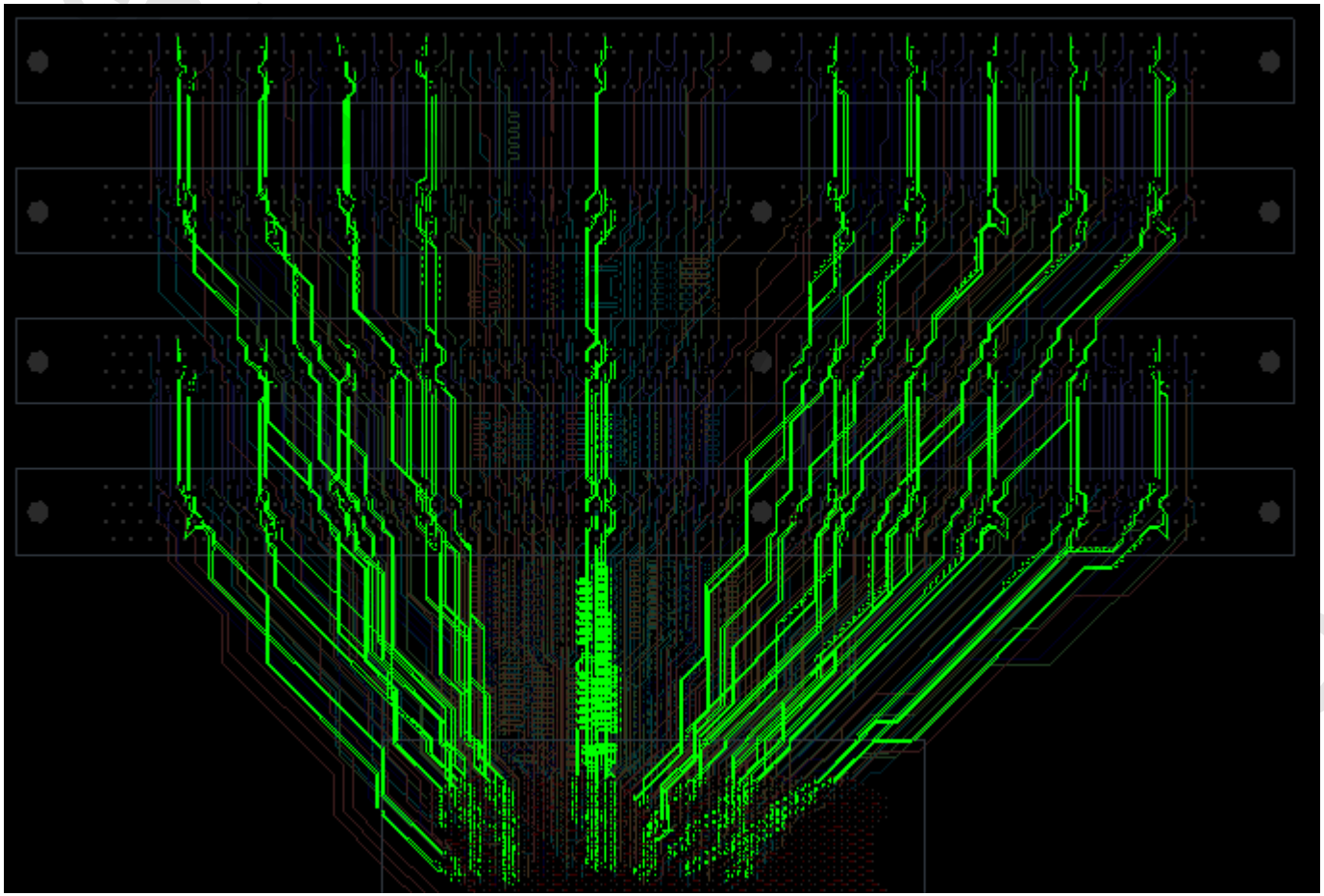
Plan (Design Planning Option)

4th DATA (Channel A & B)
- AiPT(High-Speed option)



Plan (Design Planning Option)

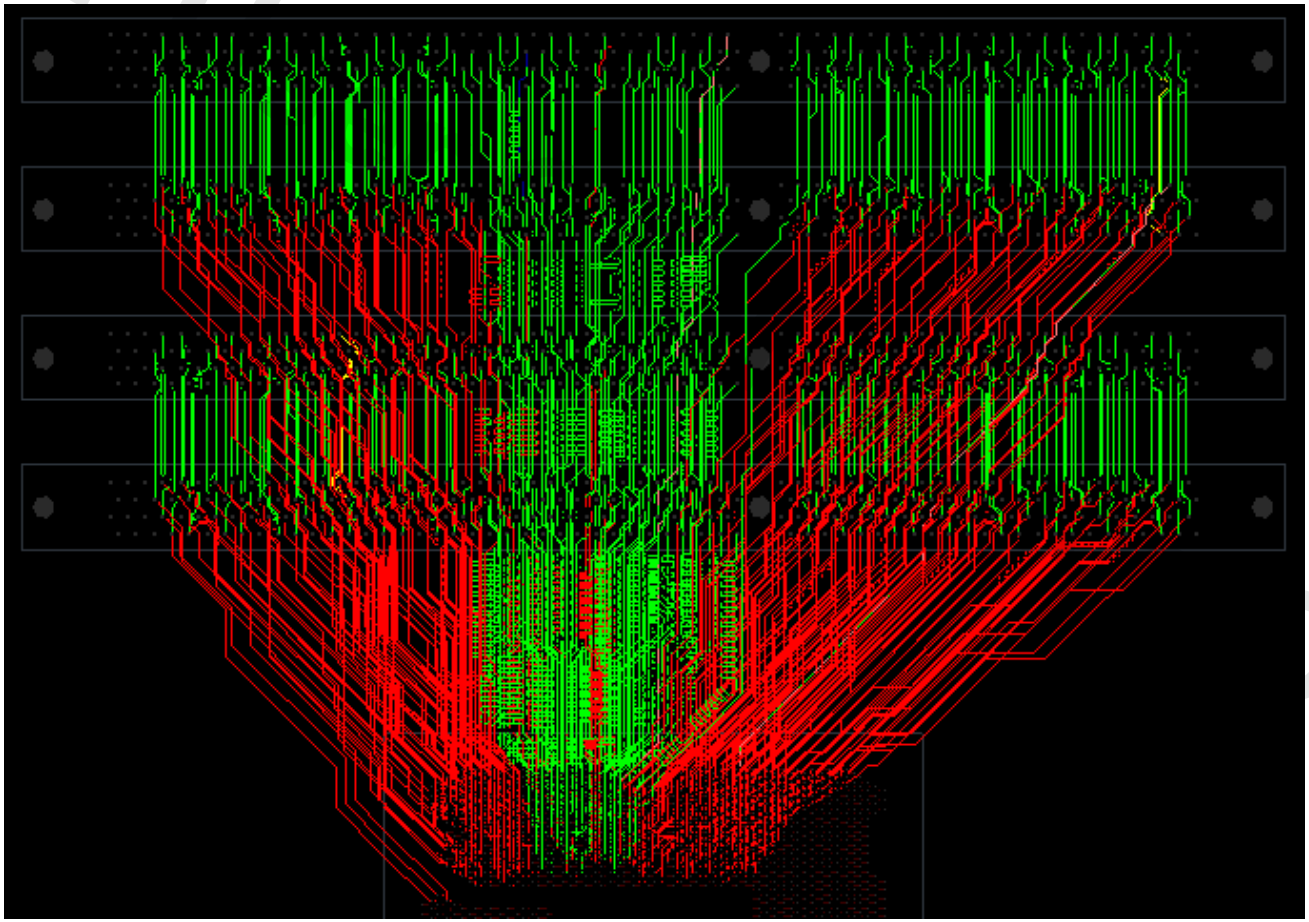
4th DATA (Channel A & B)
- Manual Phase Tuning



Plan (Design Planning Option)

4th DATA (Channel A & B)

- Timing vision (High-Speed option)
- DRC Timing view

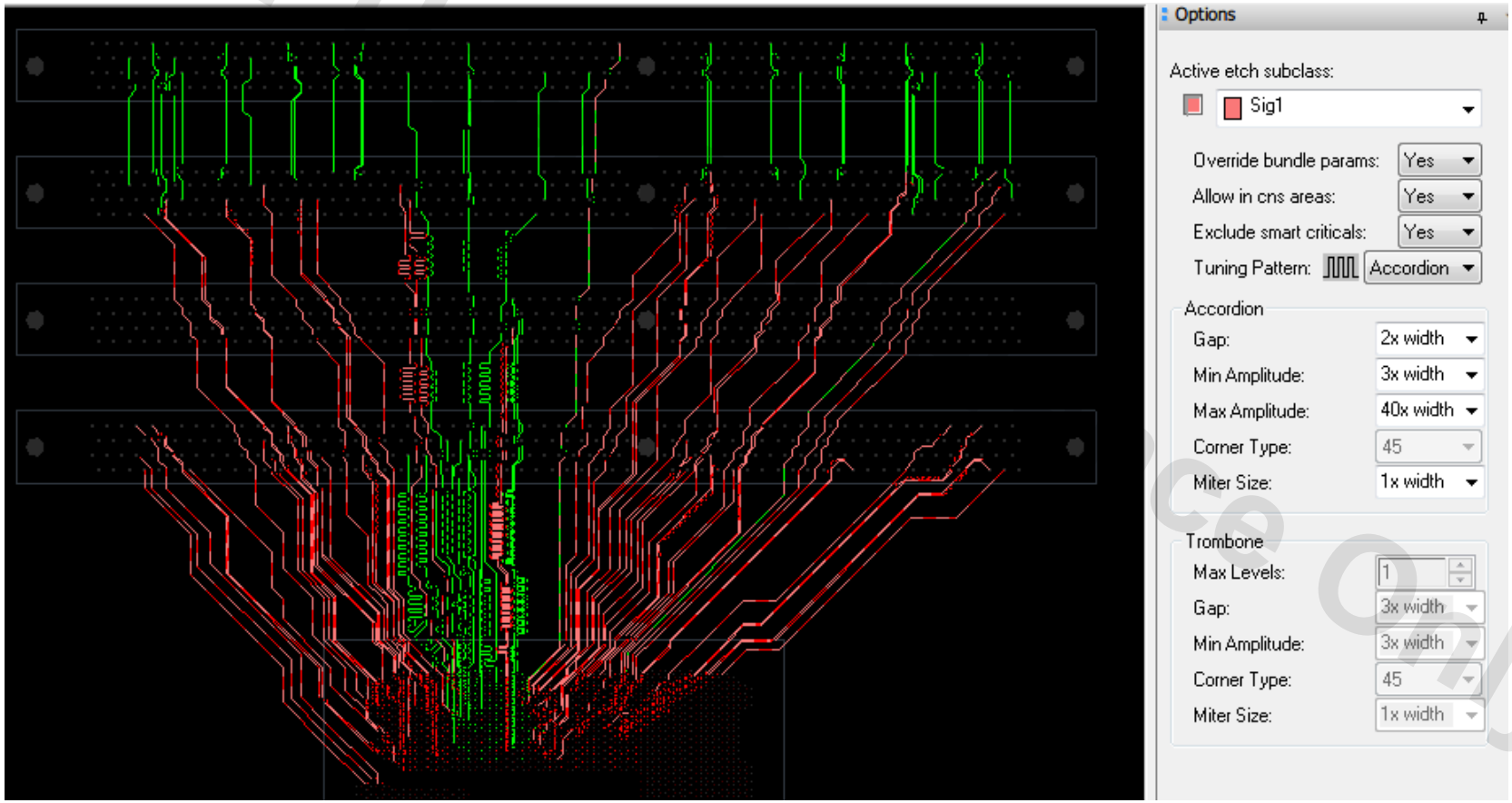


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig1 layer

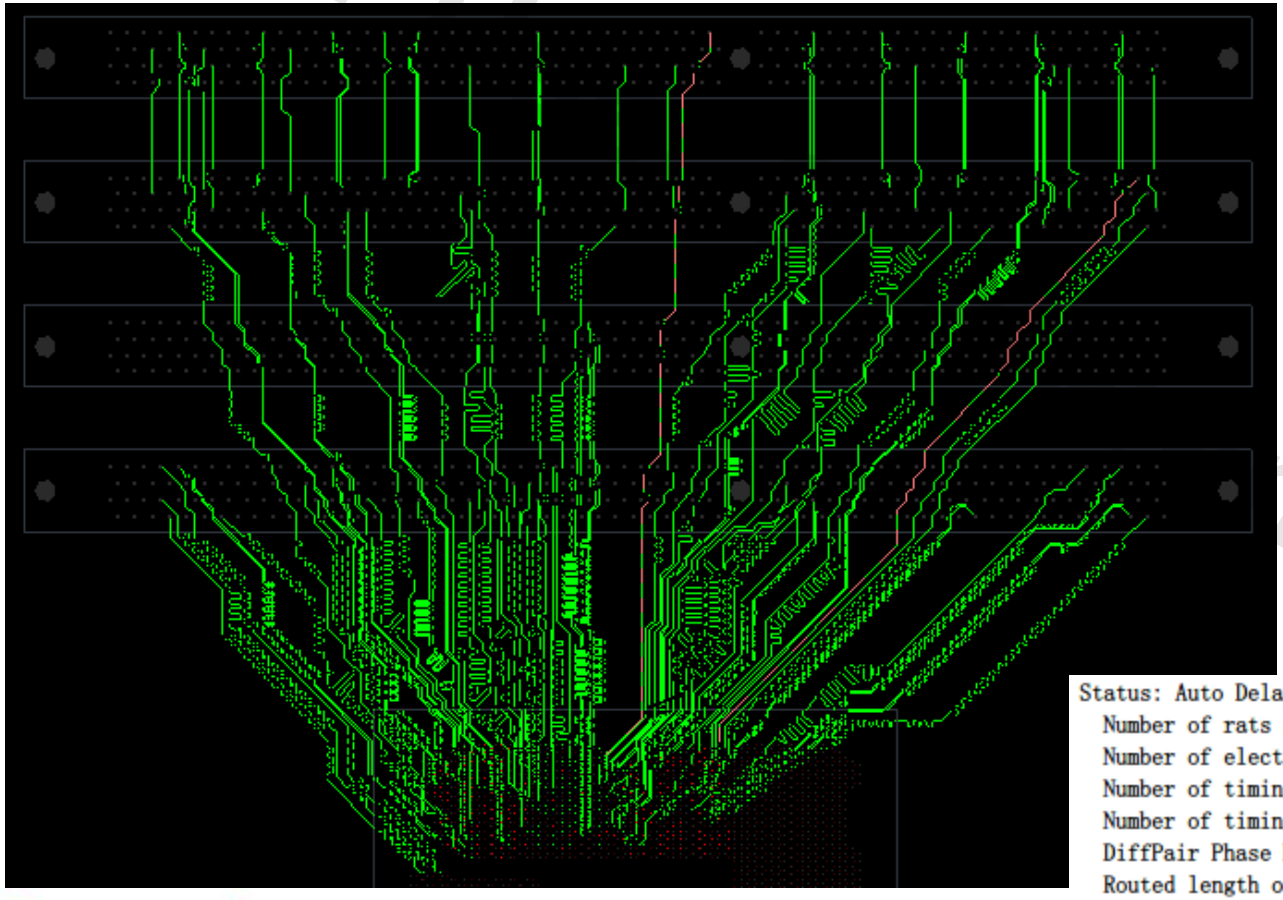


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig1 layer



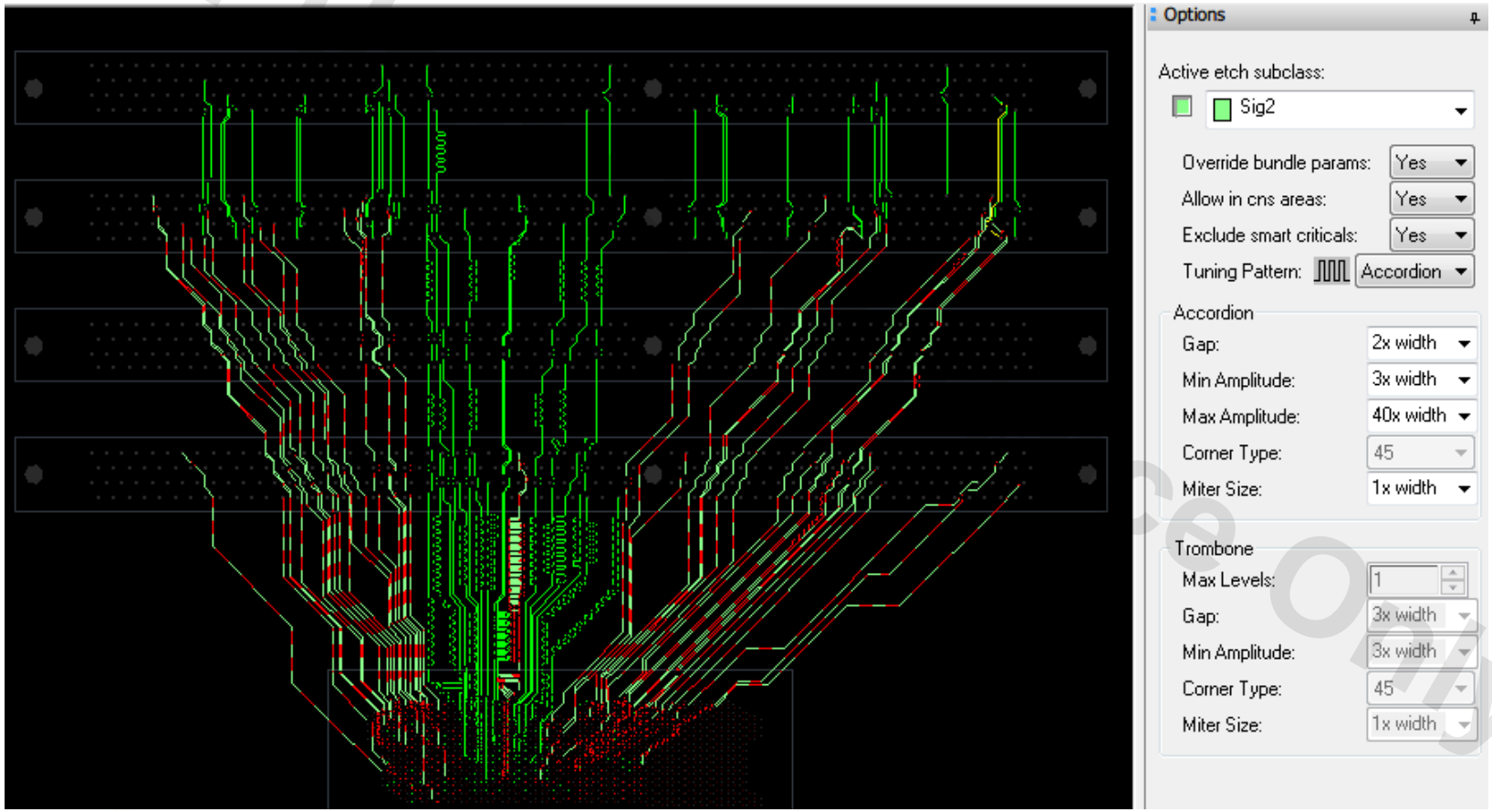
```
Status: Auto Delay Tune completed normally
  Number of rats scheduled = 54
  Number of electrical violations on sceduled rats = 26
  Number of timing constraints on scheduled rats = 108
  Number of timing constraint violations on scheduled rats = 0
  DiffPair Phase Mismatch = 384.141 MIL
  Routed length of scheduled rats = 190206.853 MIL
  Execution time = 493 seconds
  Memory currently in use = 279991 KB
```

Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig2 layer

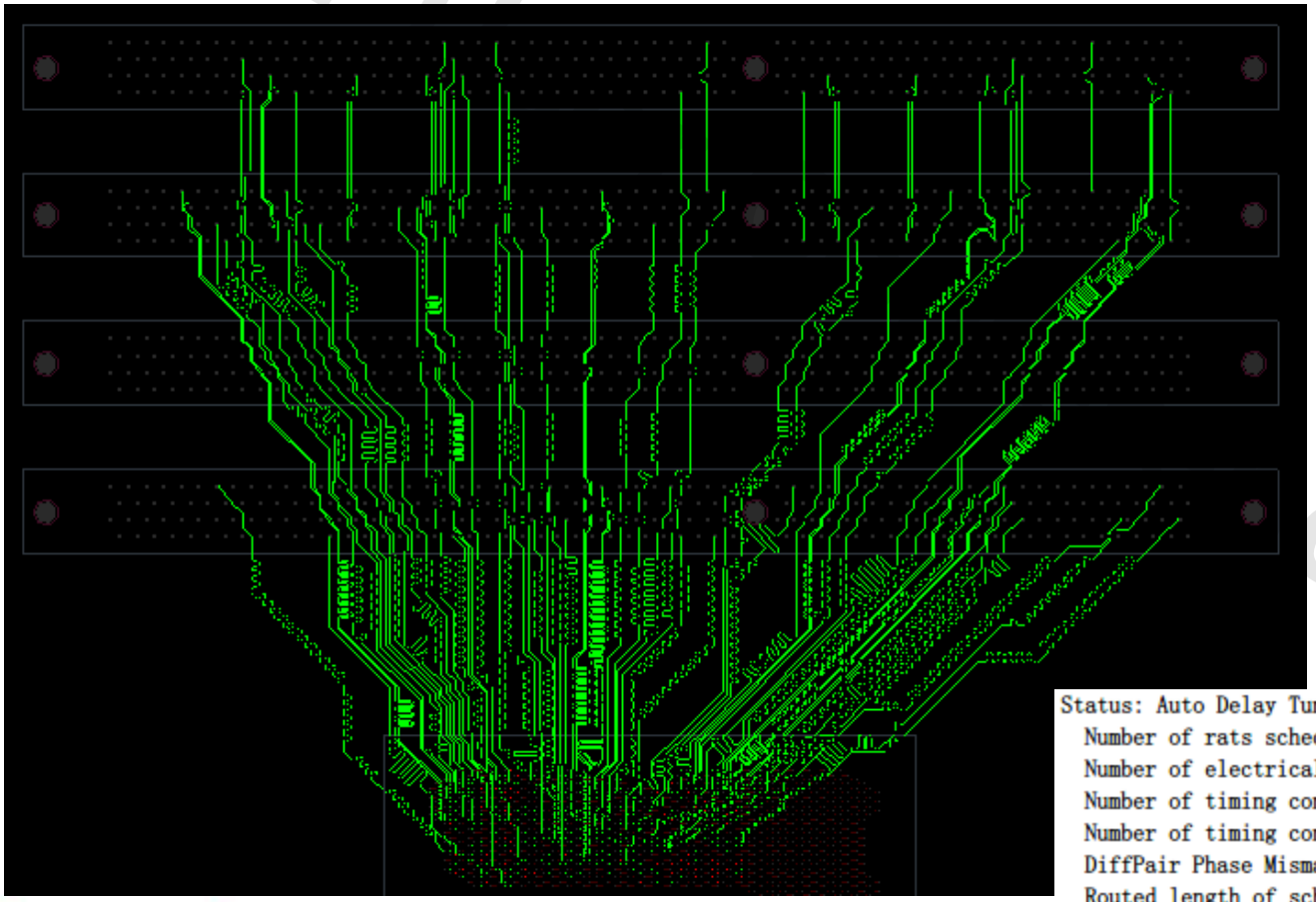


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig2 layer



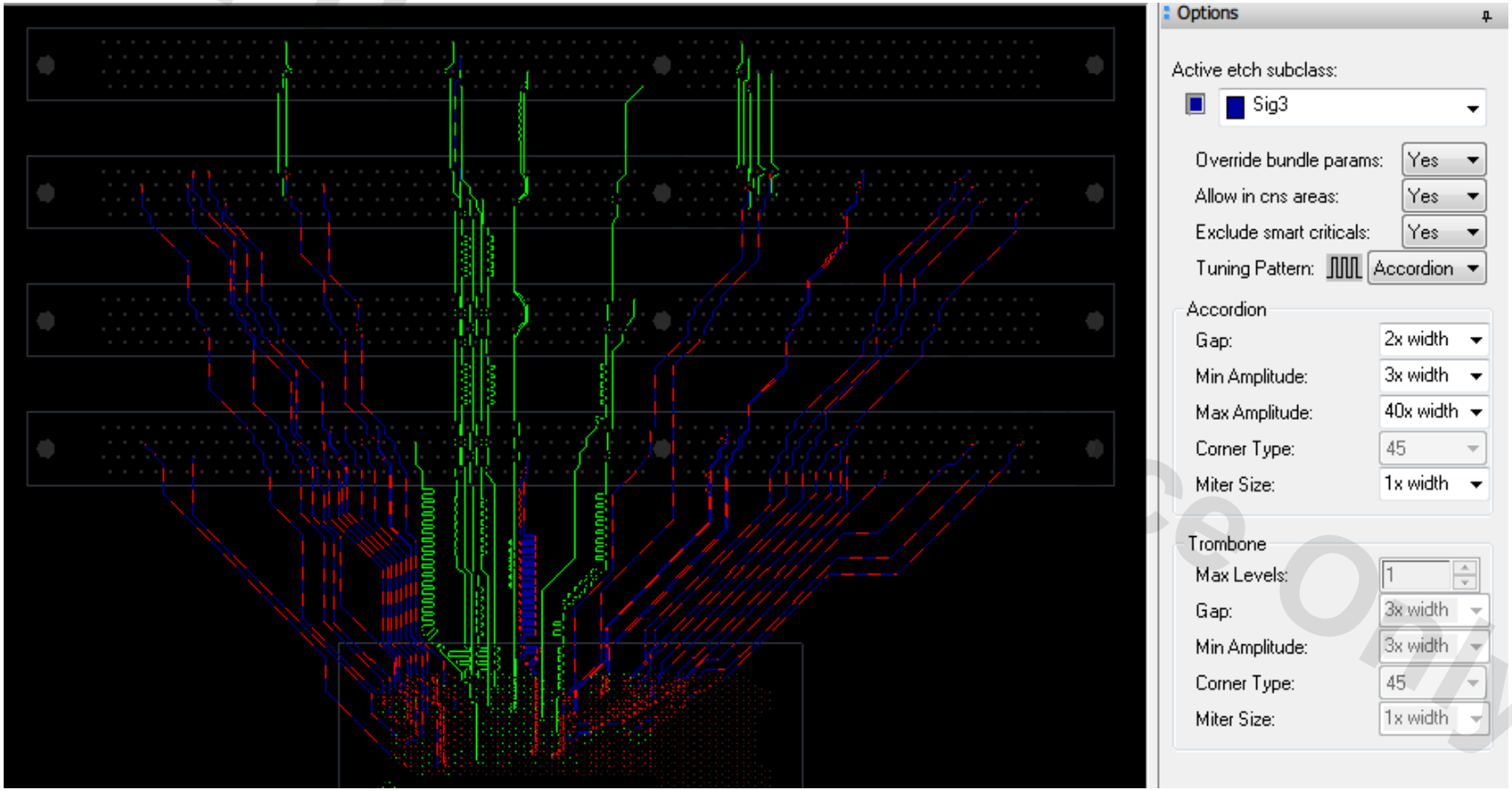
```
Status: Auto Delay Tune completed normally
  Number of rats scheduled = 42
  Number of electrical violations on sceduled rats = 12
  Number of timing constraints on scheduled rats = 84
  Number of timing constraint violations on scheduled rats = 0
  DiffPair Phase Mismatch = 270.318 MIL
  Routed length of scheduled rats = 154392.988 MIL
  Execution time = 191 seconds
  Memory currently in use = 280637 KB
```

Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig3 layer

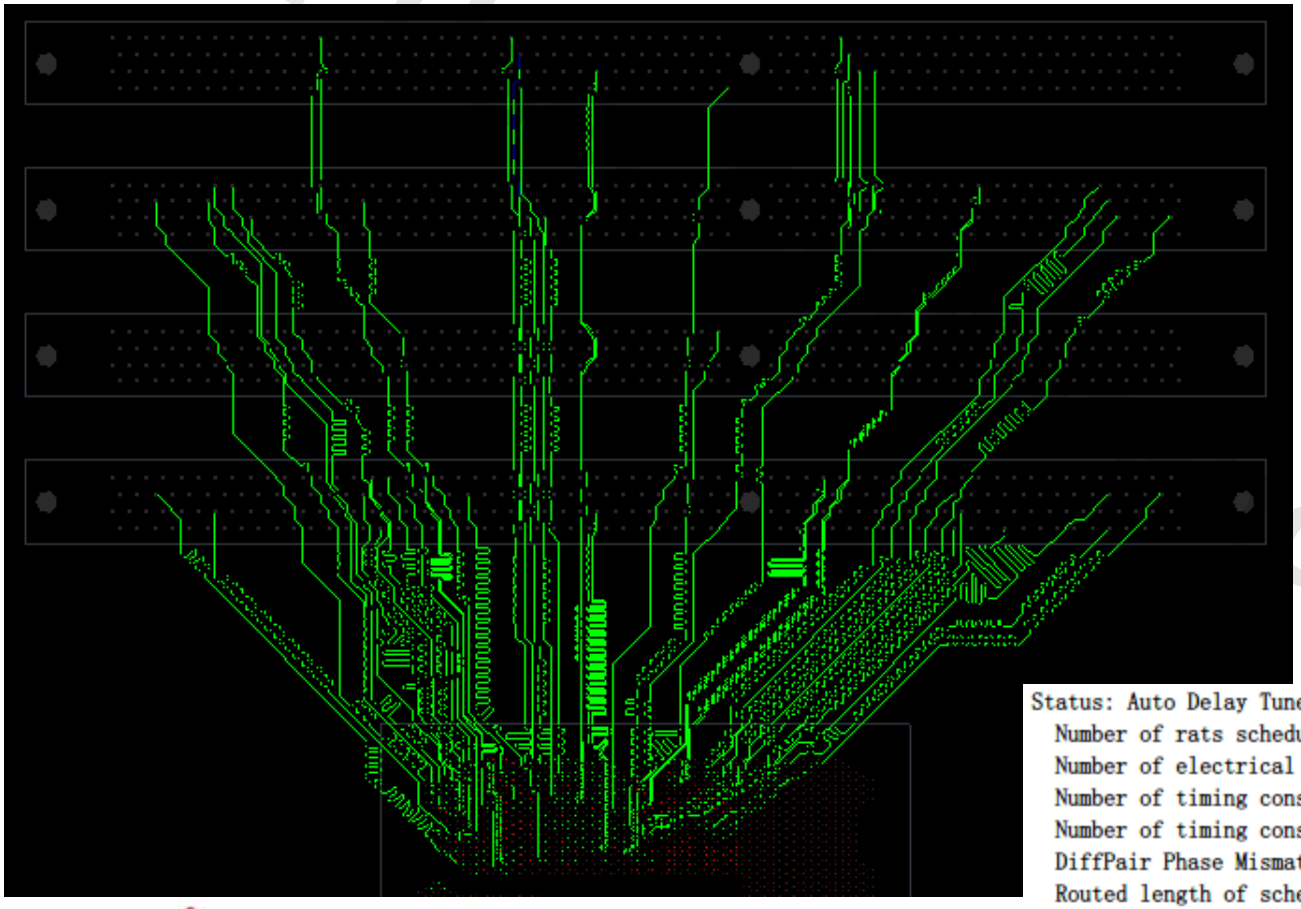


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig3 layer



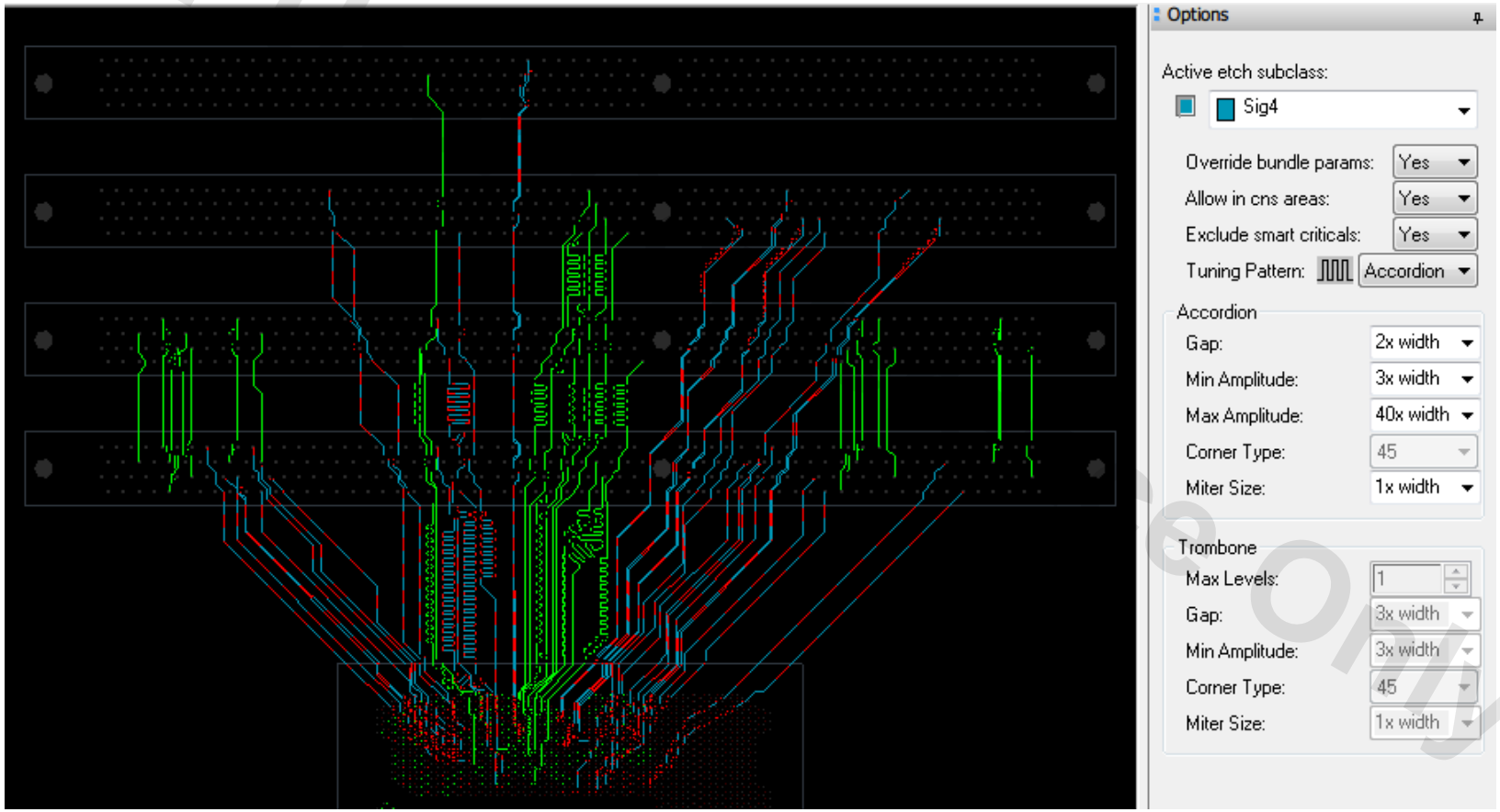
```
Status: Auto Delay Tune completed normally
  Number of rats scheduled = 34
  Number of electrical violations on sceduled rats = 6
  Number of timing constraints on scheduled rats = 68
  Number of timing constraint violations on scheduled rats = 0
  DiffPair Phase Mismatch = 18.444 MIL
  Routed length of scheduled rats = 122215.163 MIL
  Execution time = 106 seconds
  Memory currently in use = 280823 KB
```

Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig4 layer

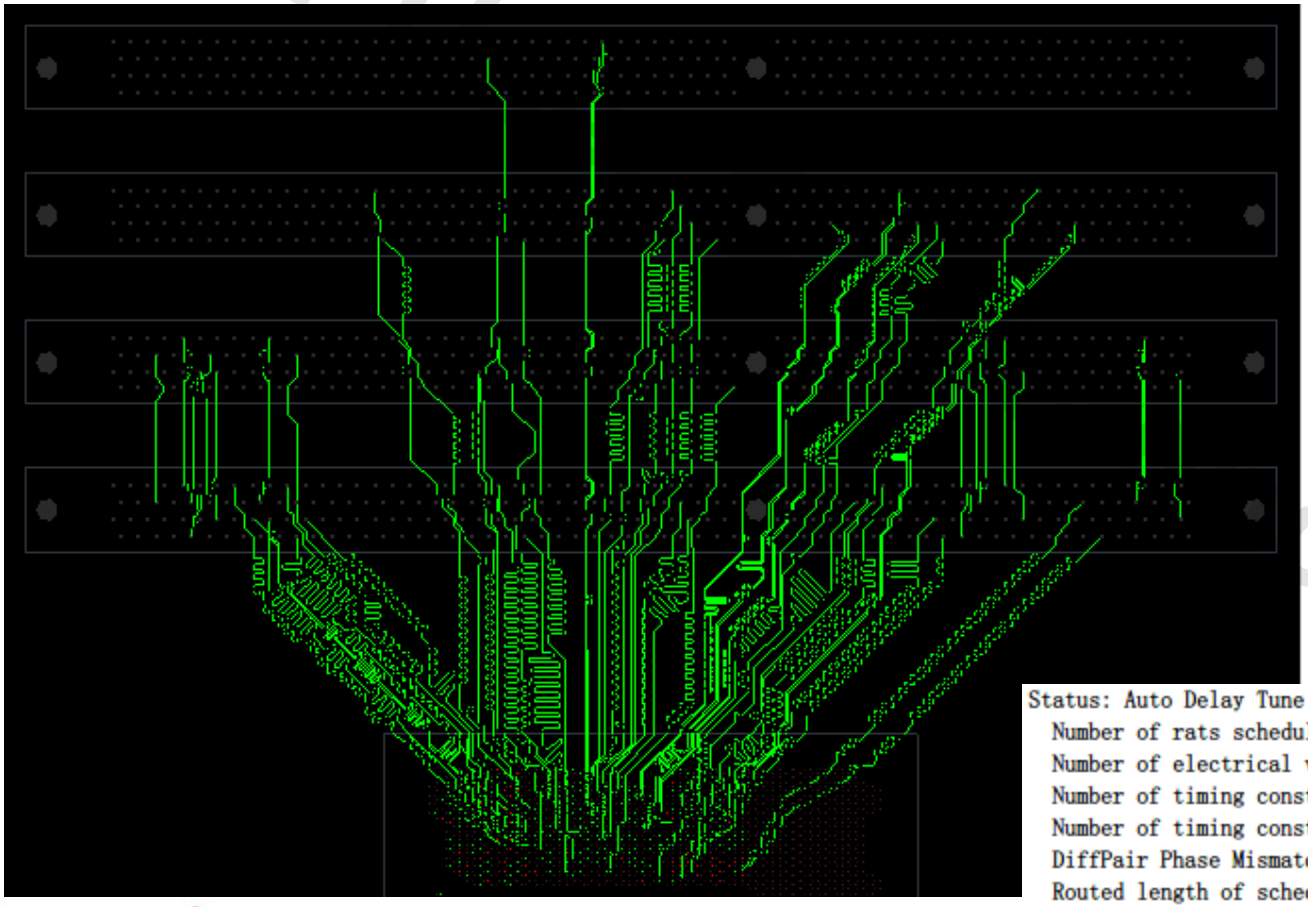


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig4 layer



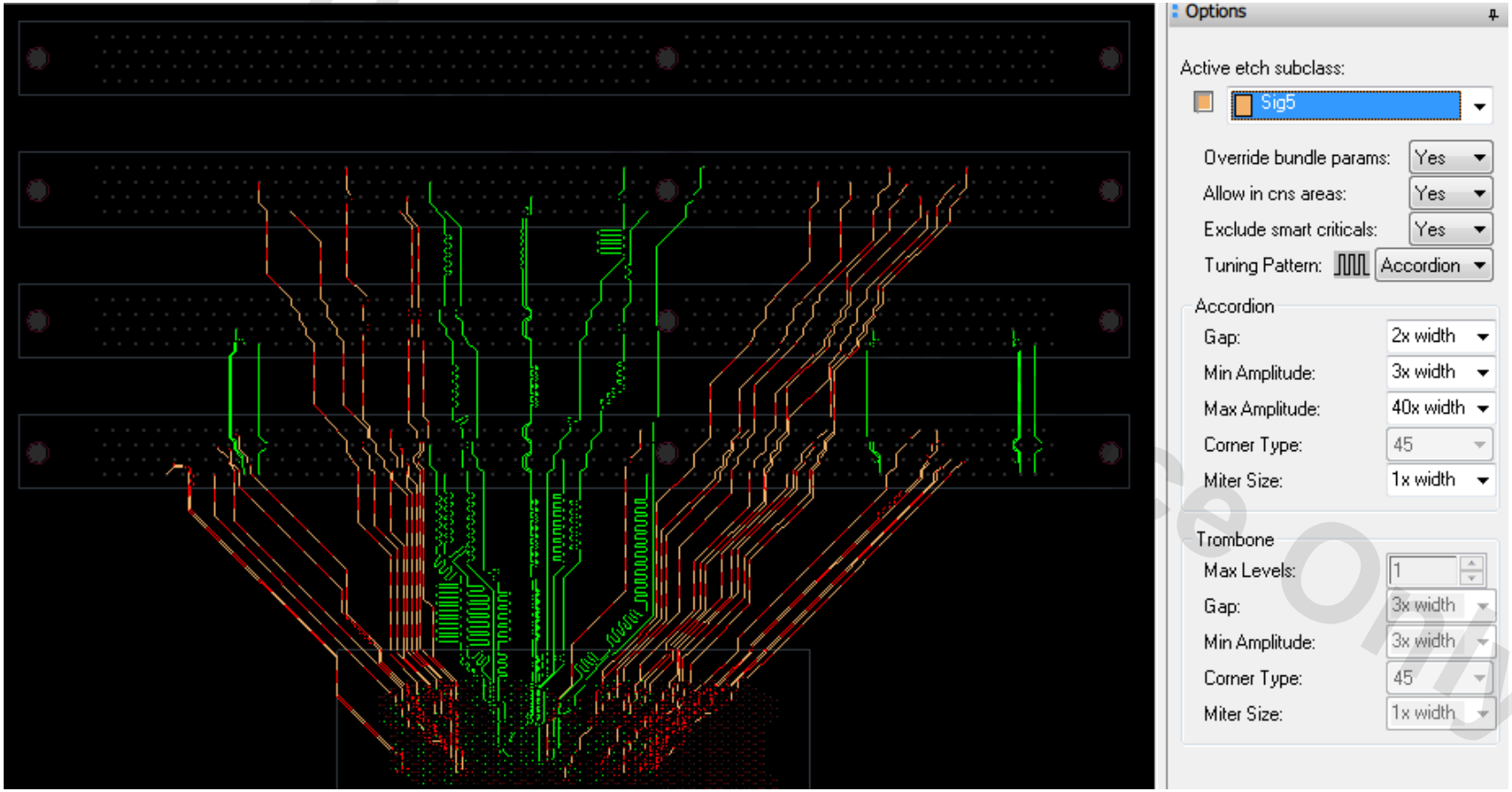
```
Status: Auto Delay Tune completed normally
  Number of rats scheduled = 34
  Number of electrical violations on sceduled rats = 10
  Number of timing constraints on scheduled rats = 68
  Number of timing constraint violations on scheduled rats = 0
  DiffPair Phase Mismatch = 68.032 MIL
  Routed length of scheduled rats = 123287.731 MIL
  Execution time = 115 seconds
  Memory currently in use = 281217 KB
```

Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig5 layer

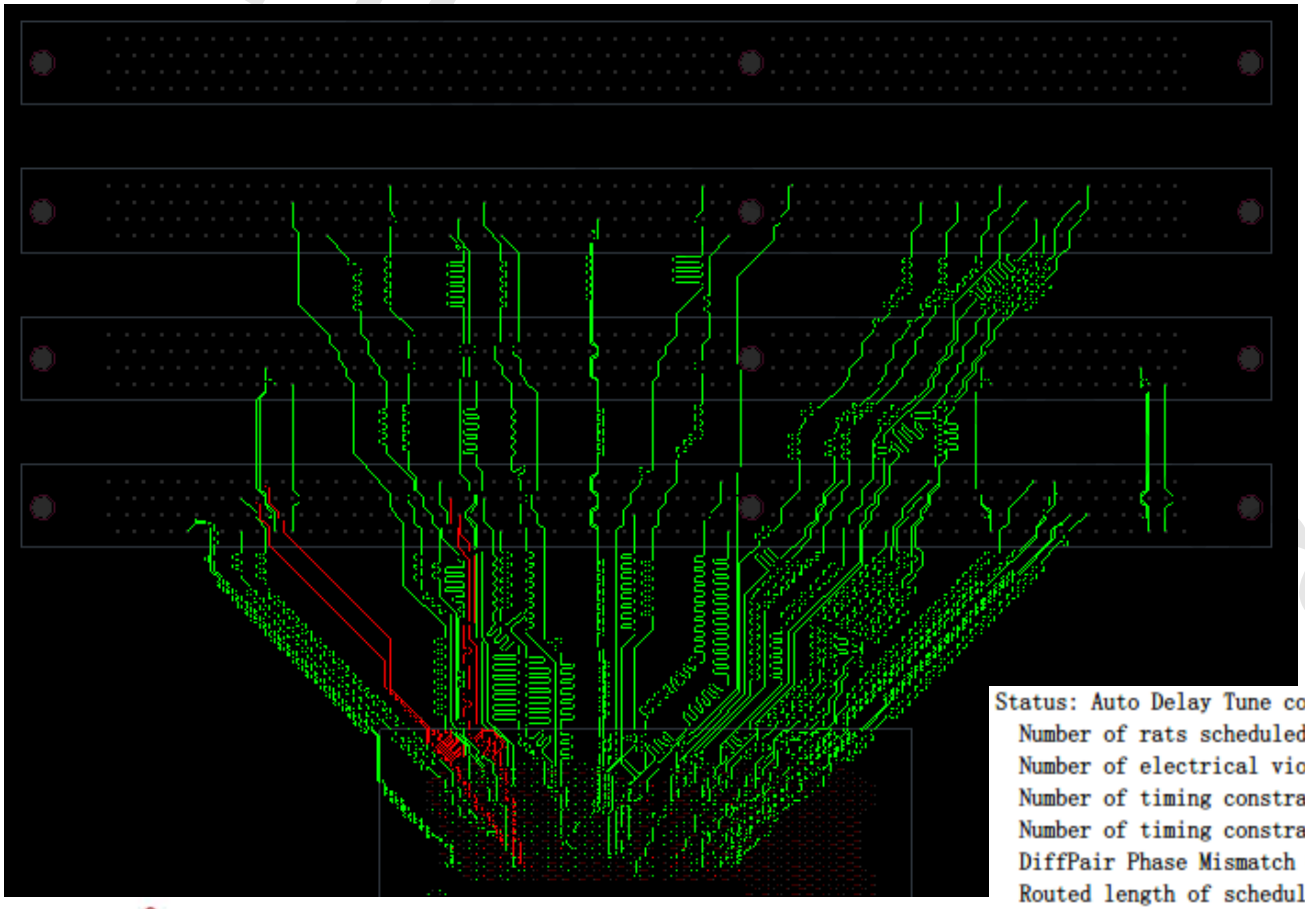


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig5 layer



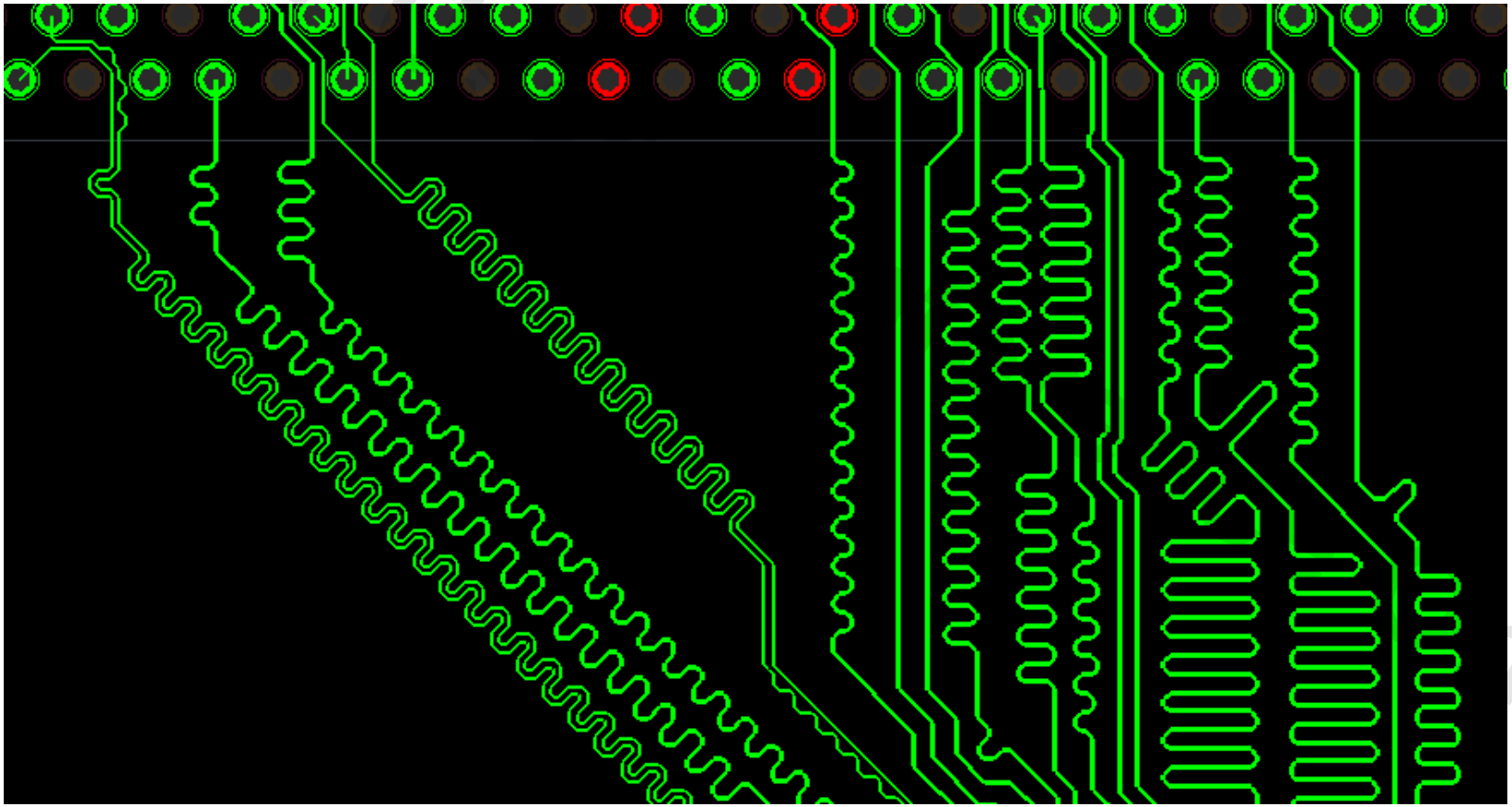
```
Status: Auto Delay Tune completed normally
  Number of rats scheduled = 33
  Number of electrical violations on sceduled rats = 12
  Number of timing constraints on scheduled rats = 66
  Number of timing constraint violations on scheduled rats = 4
  DiffPair Phase Mismatch = 71.585 MIL
  Routed length of scheduled rats = 115874.077 MIL
  Execution time = 189 seconds
  Memory currently in use = 284152 KB
```

Plan (Design Planning Option)

4th DATA (Channel A & B)

- Manual fine tuning + AiDT

- Sig5 layer

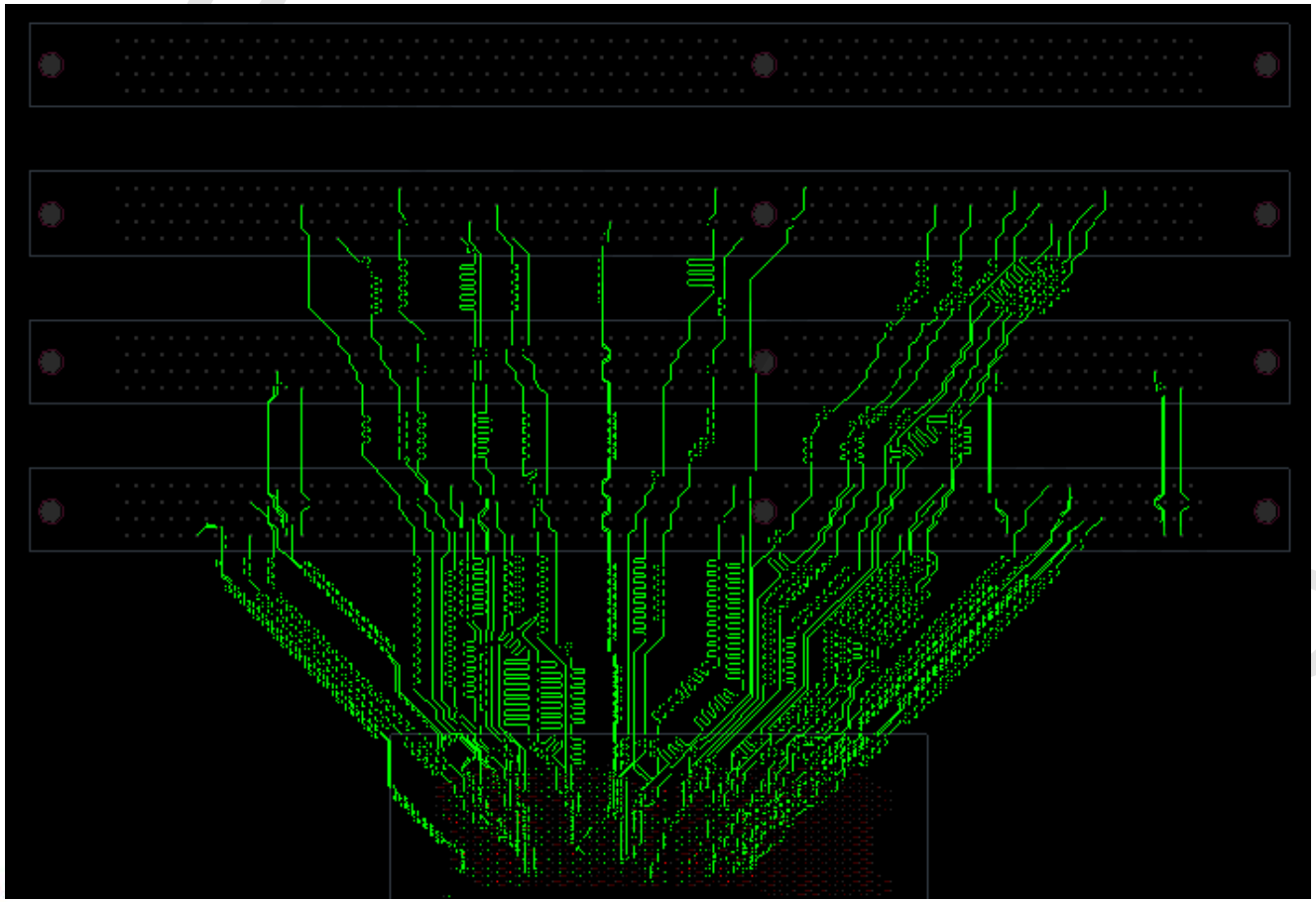


Plan (Design Planning Option)

4th DATA (Channel A & B)

- Manual fine tuning + AiDT

- Sig5 layer

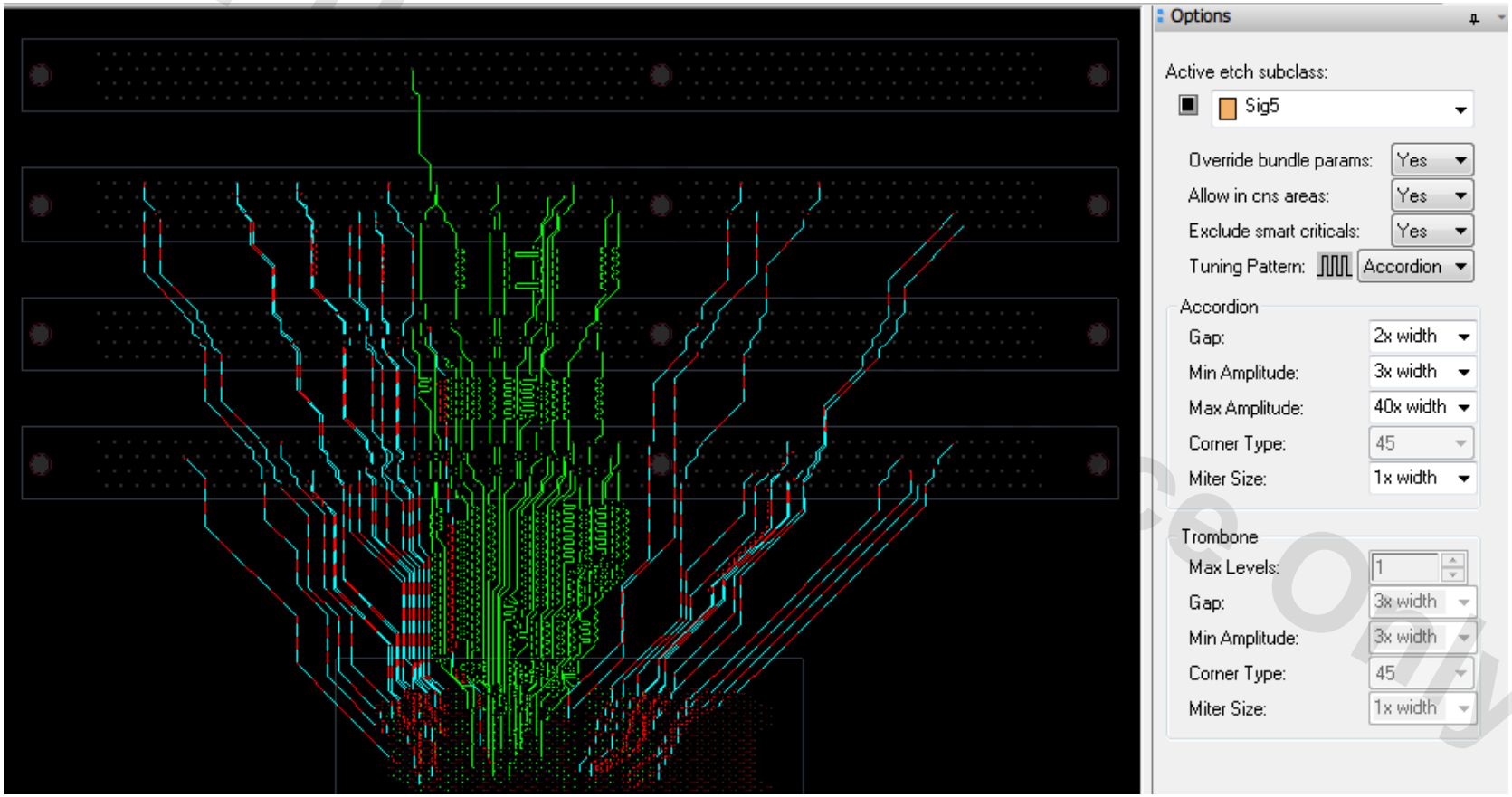


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

- Sig6 layer

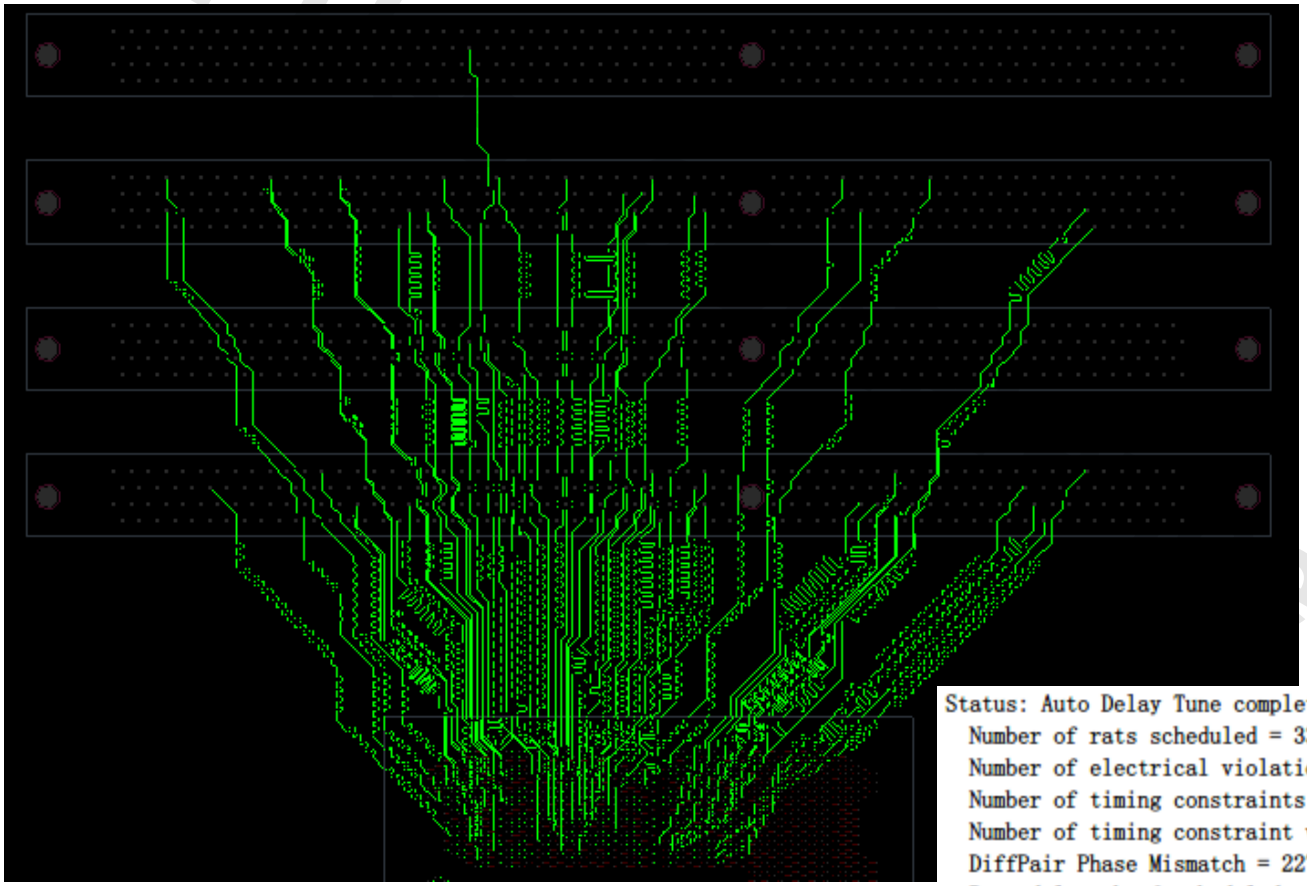


Plan (Design Planning Option)

4th DATA (Channel A & B)

- AiDT (High-Speed option)

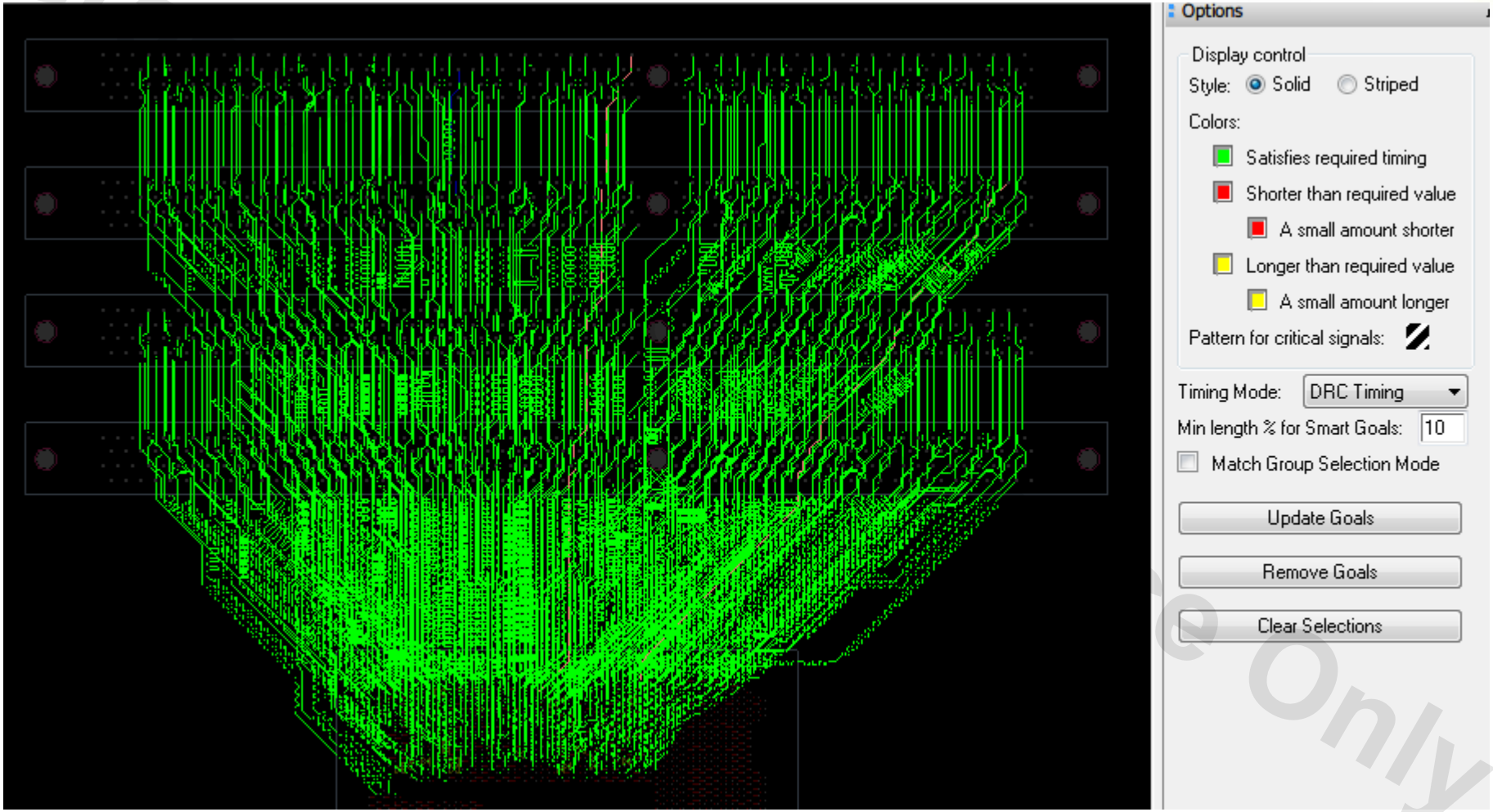
- Sig6 layer



```
Status: Auto Delay Tune completed normally
  Number of rats scheduled = 33
  Number of electrical violations on sceduled rats = 14
  Number of timing constraints on scheduled rats = 66
  Number of timing constraint violations on scheduled rats = 0
  DiffPair Phase Mismatch = 227.202 MIL
  Routed length of scheduled rats = 113486.195 MIL
  Execution time = 195 seconds
  Memory currently in use = 304297 KB
```

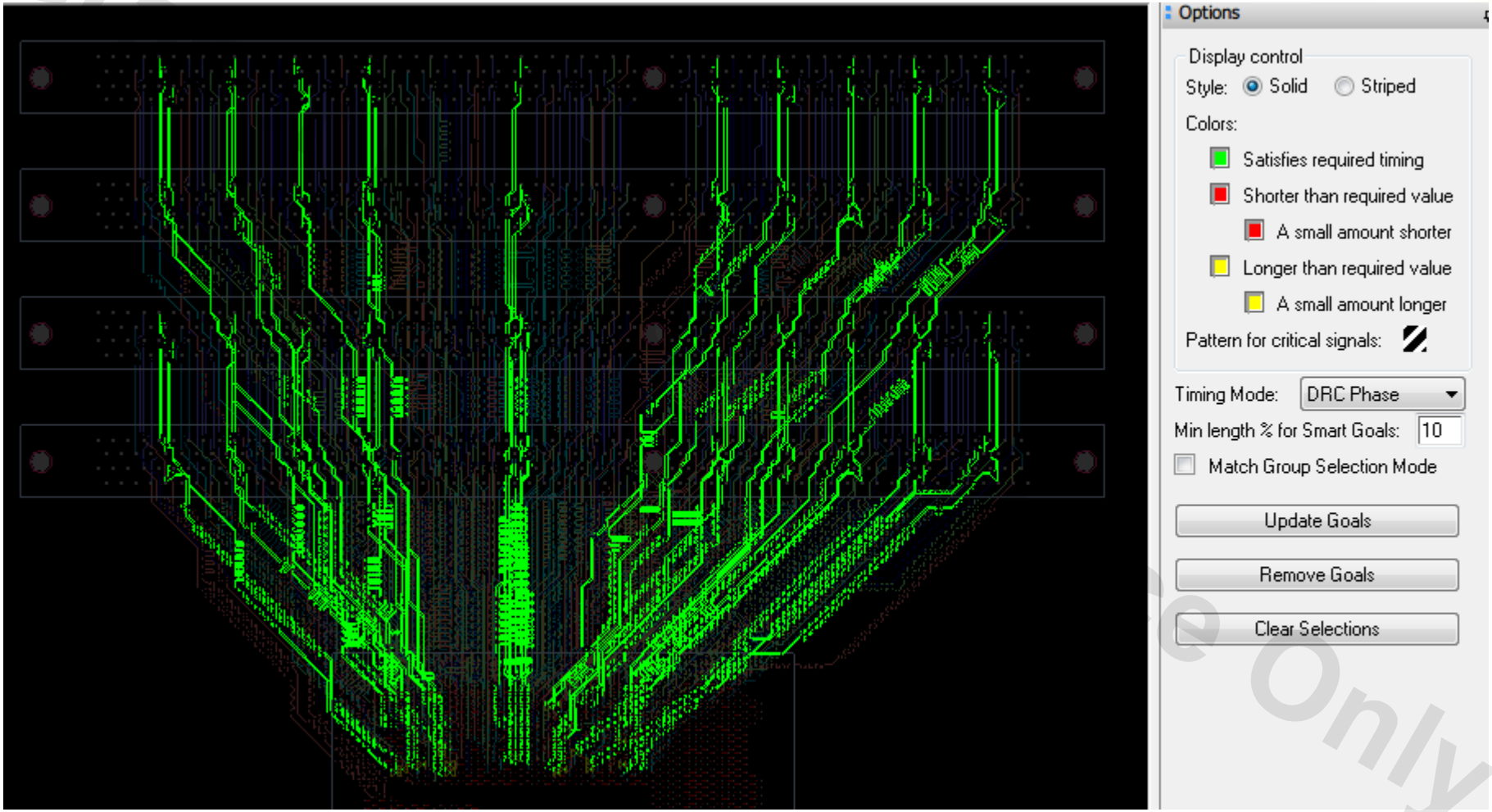
Routing Result

Timing view



Routing Result

Phase view



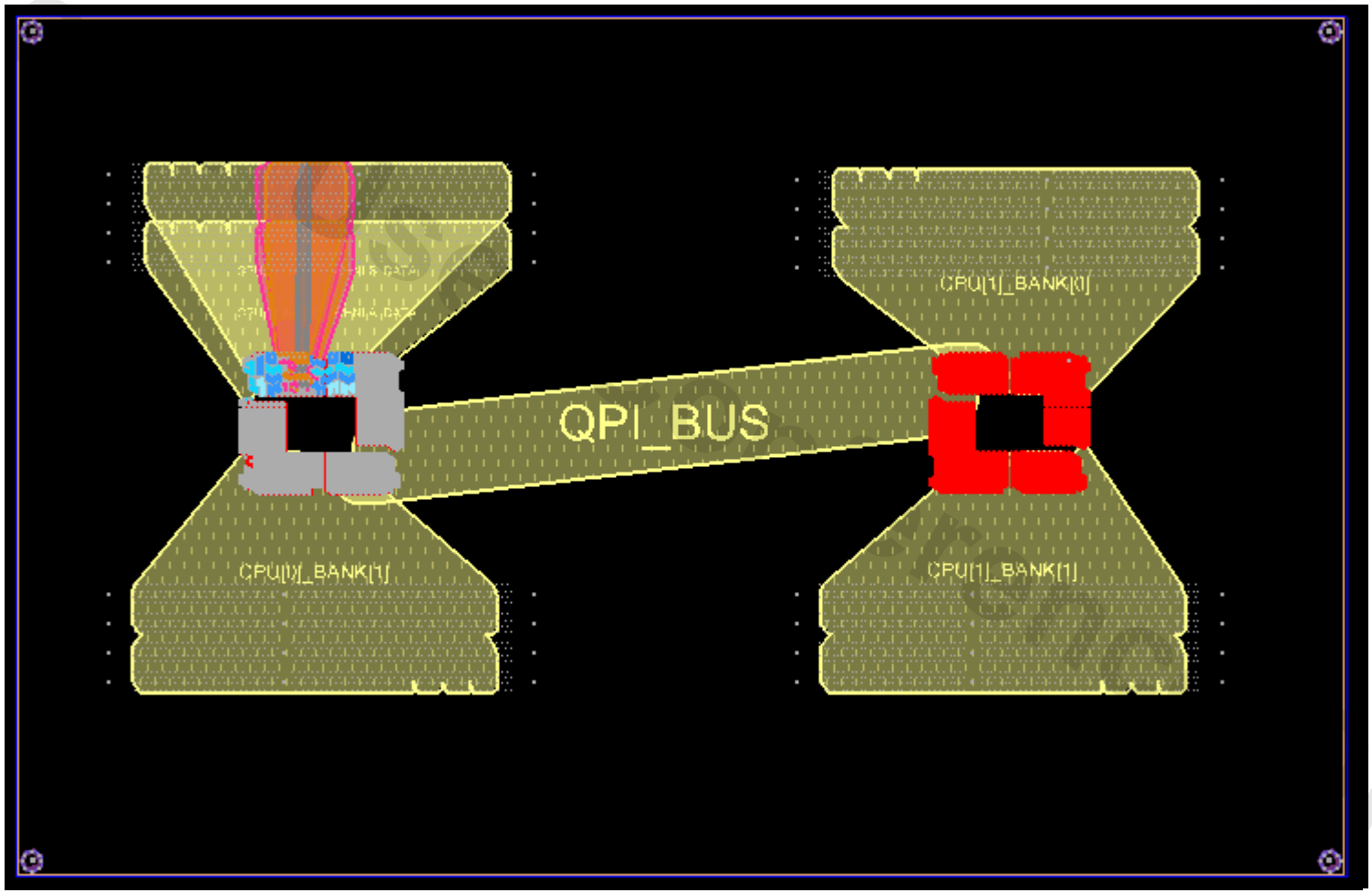
Conclusion

DDR (276 Nets)

- Setting Time: About 30 ~ 120 mins
- Automation Time : About 40 ~ 60 mins
- Manual Time: About 2 ~ 6 hrs

This case : Took 5 hrs

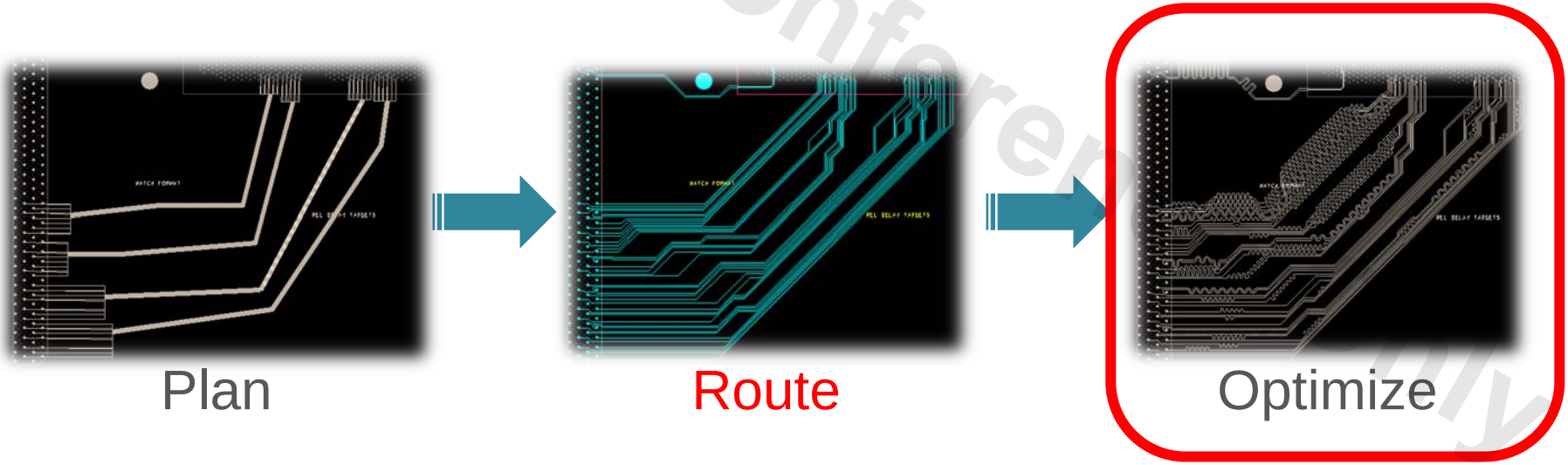
What else



Chapter Three

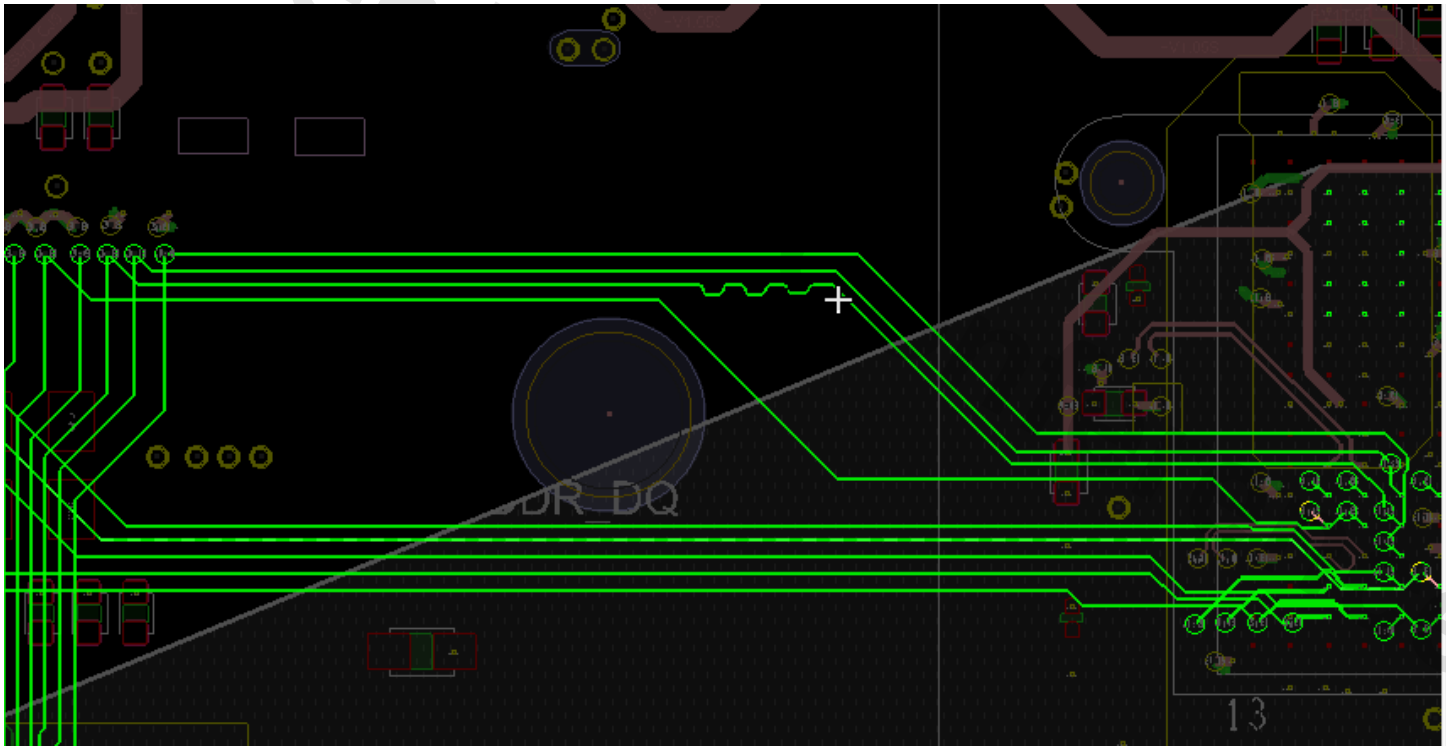
Routing Flow

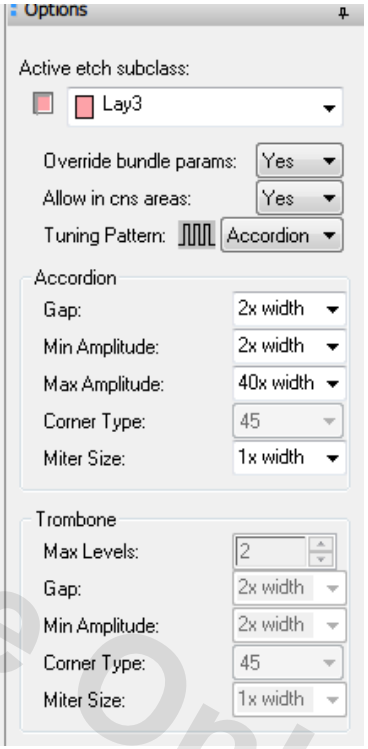
- Fan out
- Break out
- Route



Optimize

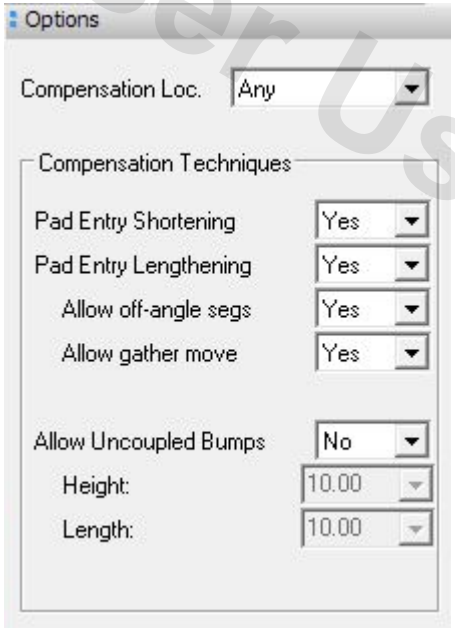
Auto-interactive Delay Tune (AiDT – High Speed Option)
(Enhanced by QIR#4)

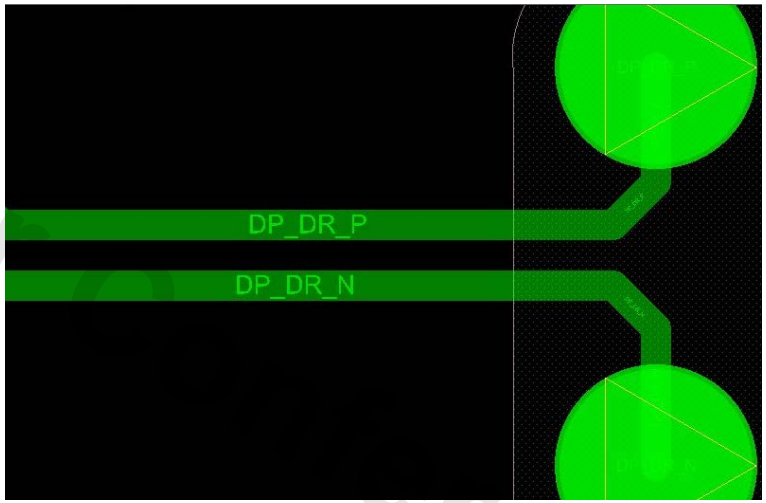


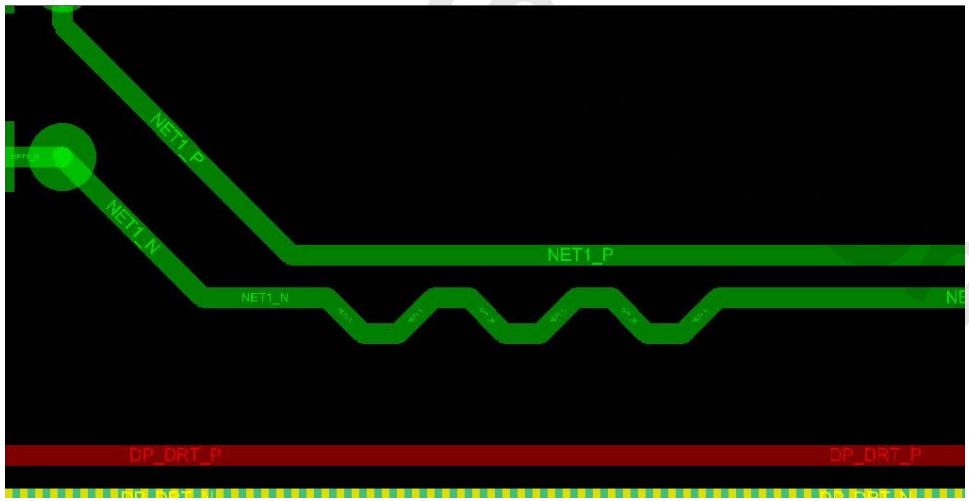


Optimize

Auto-interactive Phase Tune (AiPT – High Speed Option)
(Enhanced by QIR#4)



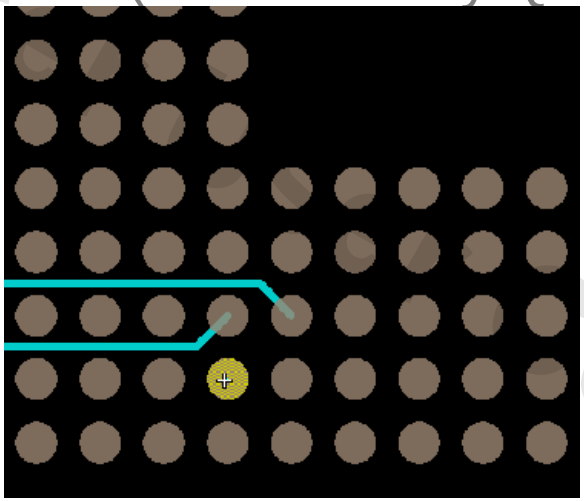


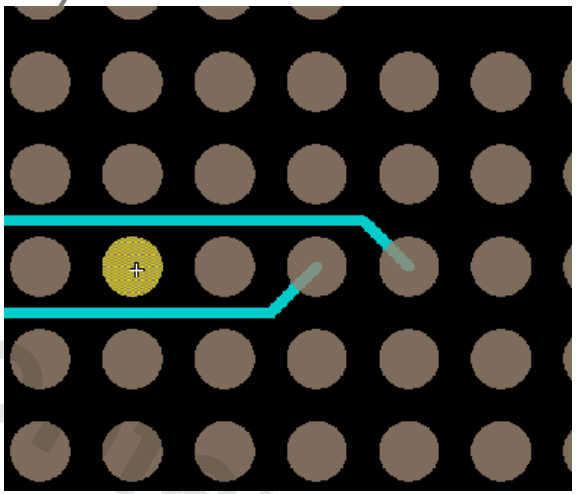


Optimize

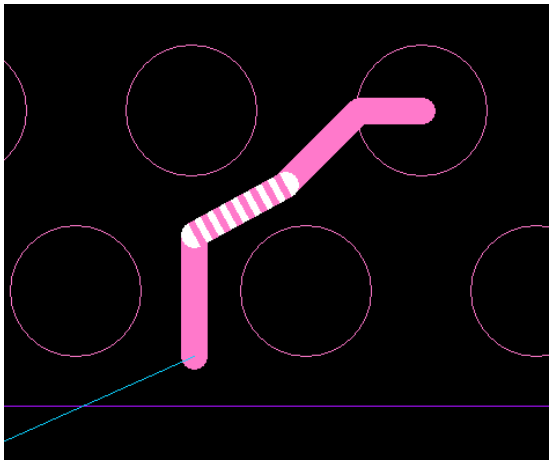
Auto-interactive Add Connect (AiAC – PCB Designer)

Scribble Mode (Enhanced by QIR#7)

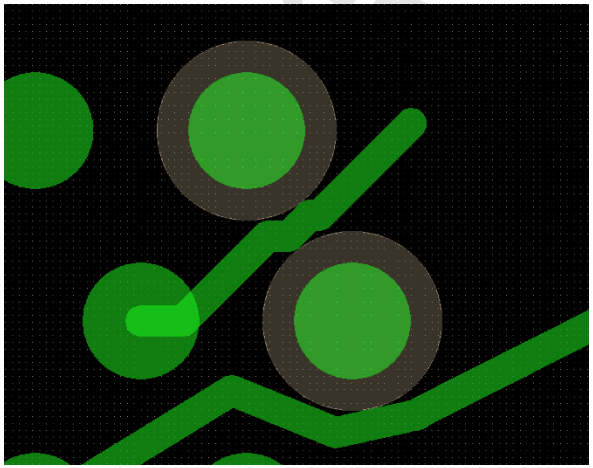




Off angle fit



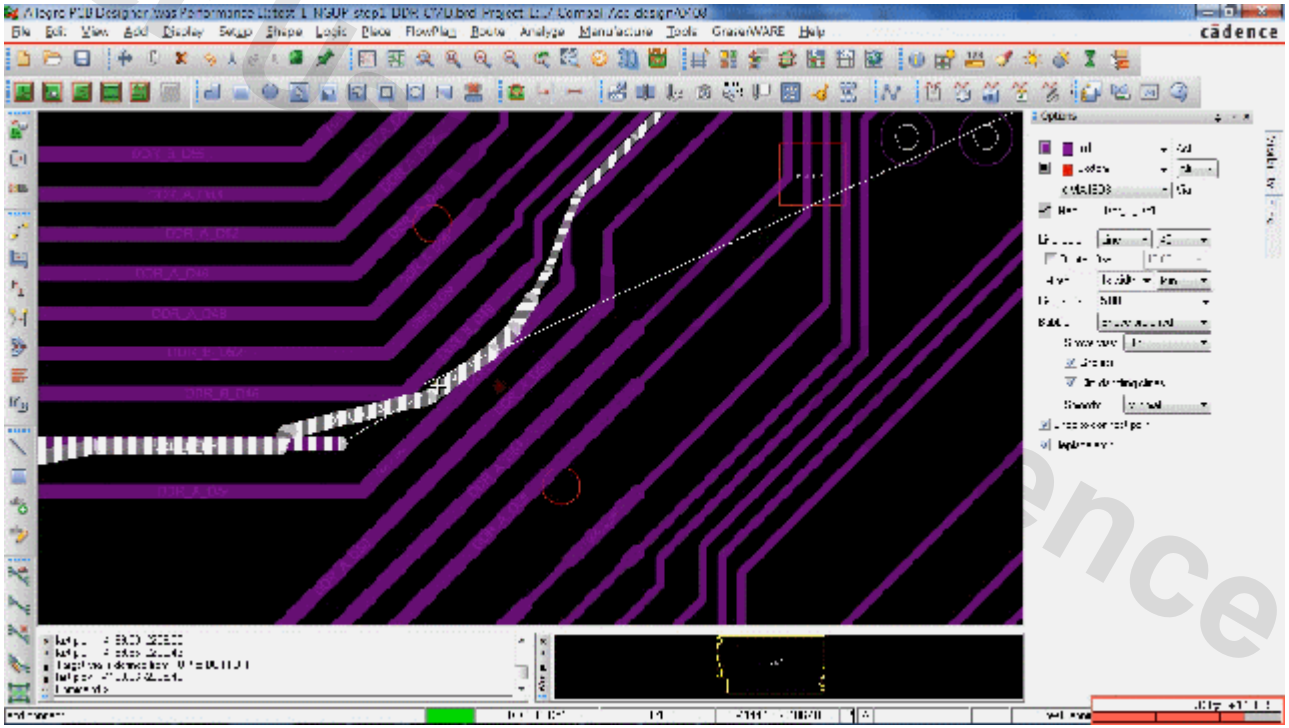
Exact fit



Optimize

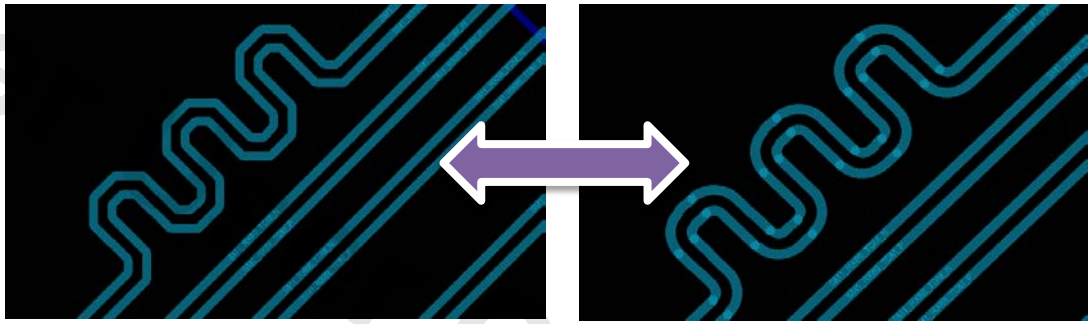
Auto-interactive Add Connect (AiAC – PCB Designer)

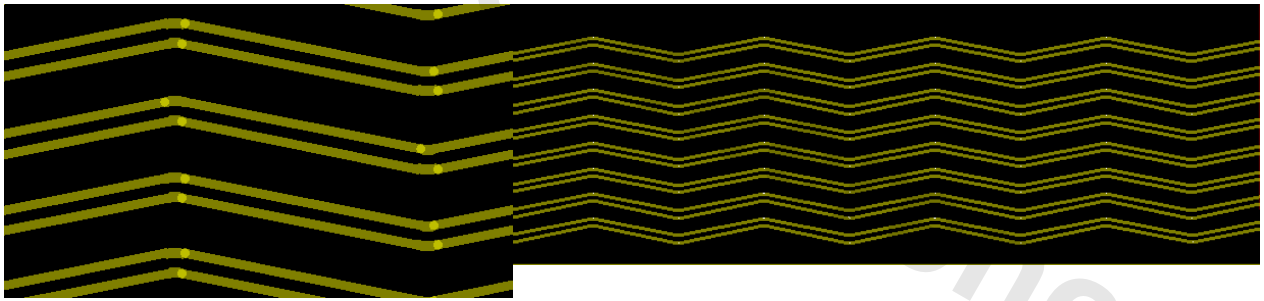
Scribble Mode (Enhanced by QIR#7)

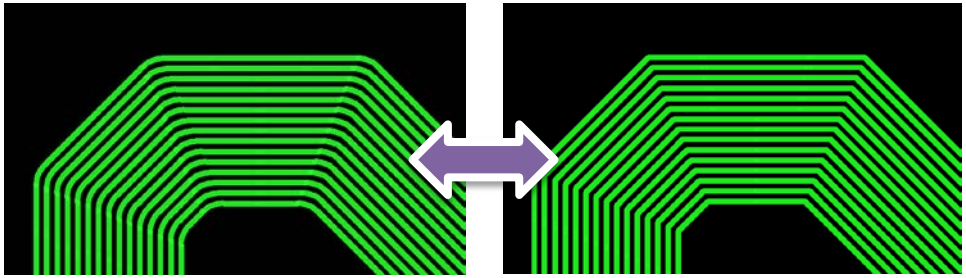


Optimize

Auto-interactive Convert Corner (AiCC – PCB Designer)







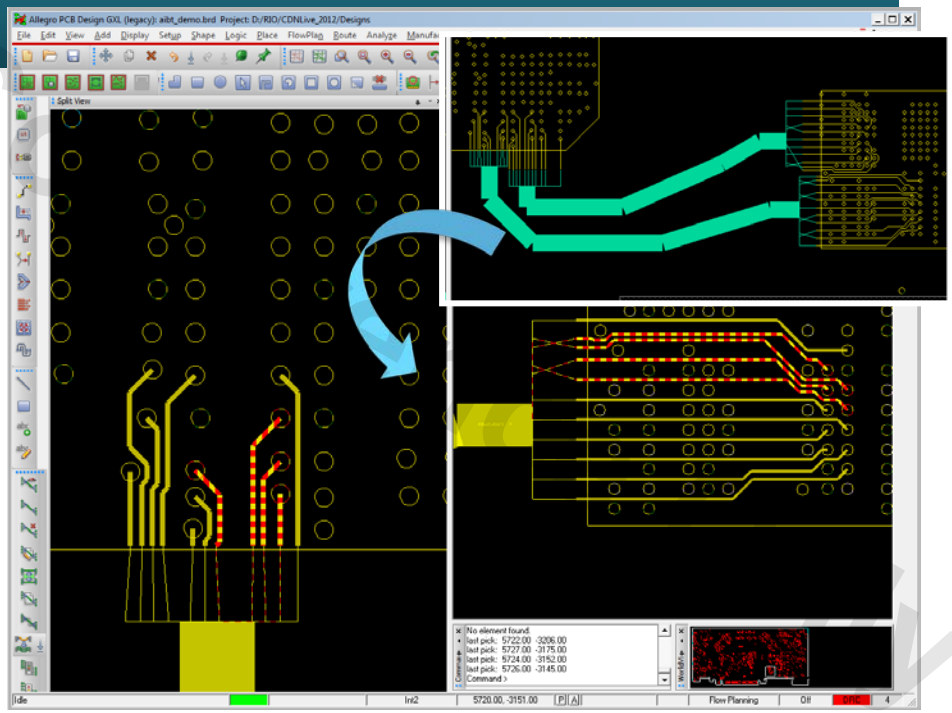
Optimize

Auto-interactive Breakout (AiBT – Design Planning Option)
(Enhanced by QIR#6)

For enterprise customers who design PCBs with high-speed interfaces such as DDR3, PCI Express 3.0, SATA, HDMI, USB 3, XAUI, SFP+

Helps you plan breakout of both components tied to an interface
Reduce routing steps and improve efficiency

- Interface breakout (both ends) analysis
- Canvas-driven inputs for direction, distance, sequence
- Rat ordering and layering



Split Views allows working on
both ends of an interface zoomed-in

Optimize

Auto-interactive Trunk Routing (AiTR – Design Planning Option)

(Enhanced by QIR#7)

- New Auto-Interactive function designed to route the ‘trunk’ or main section of an interface
- Works with Auto-interactive Breakout Tuning
  - Flow the Bundle
  - Run Auto-Interactive Breakout on both ends
  - Trunk Route follows bundle path (approximately)
- Accelerates time to breakout and route an interface