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2014 Oct³¹
Taipei

Designing Power Electronics

Mark Wu / Graser

31/Oct/2014

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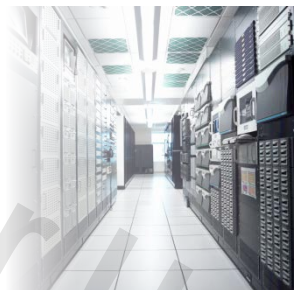
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Power Electronic Designing Vision

Miniaturization

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2014 Oct
Tappi

2010s



Nano
Technology

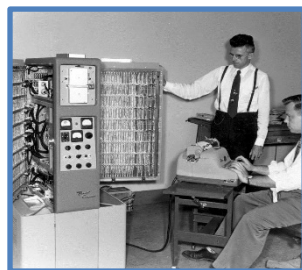
2000s

1990s



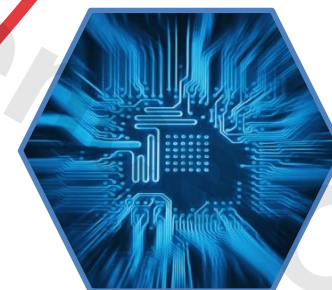
1980s

1970s



1960s

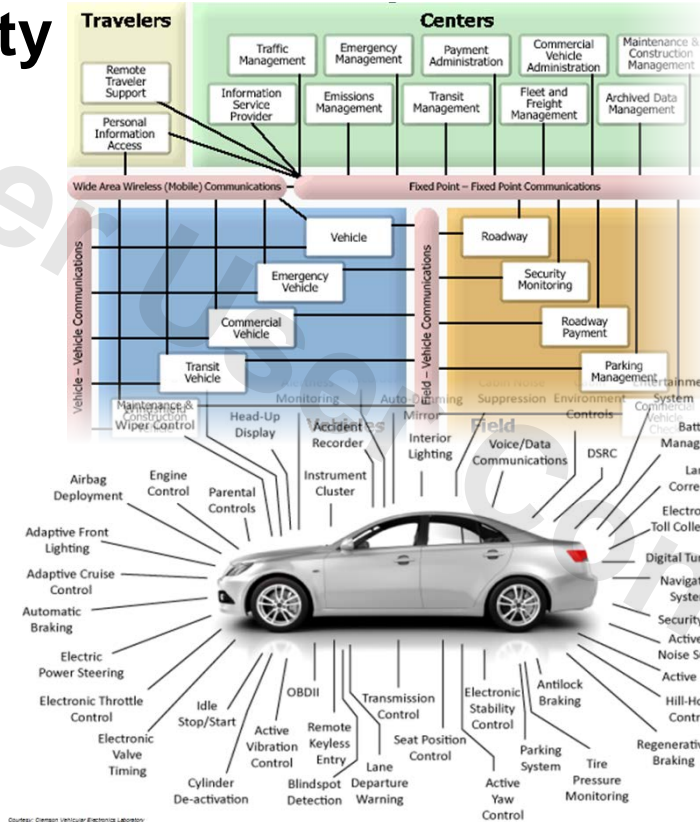
SILICON
CAPACITY



Technology

Miniaturization

Complexity

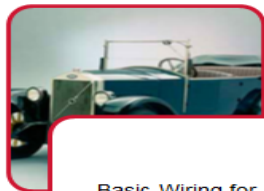


Motor Control



Michelin Active Wheel combines an electric motor, suspension and brakes within the hub of a wheel.

- Systems Modeling
- ECU Logic Authoring
- Power Electronics
- Multi-Domain Mixed Signal Control Systems
- Sensors
- Network Enabled
- Embedded Software



Basic Wiring for Headlights and Ignition



Radio & Electronic Ignition



Integration of ECUs
ABS, Air bags, LED,
Electronic Gear Box,
Navigation



Interaction with Environment
Proliferation of ECUs
Telematics, Bluetooth,
Internet,
Drive-by-Wire,
Hybrid Drives

Medical Electronics

Complexity

Trending in Portable Imaging Monitoring

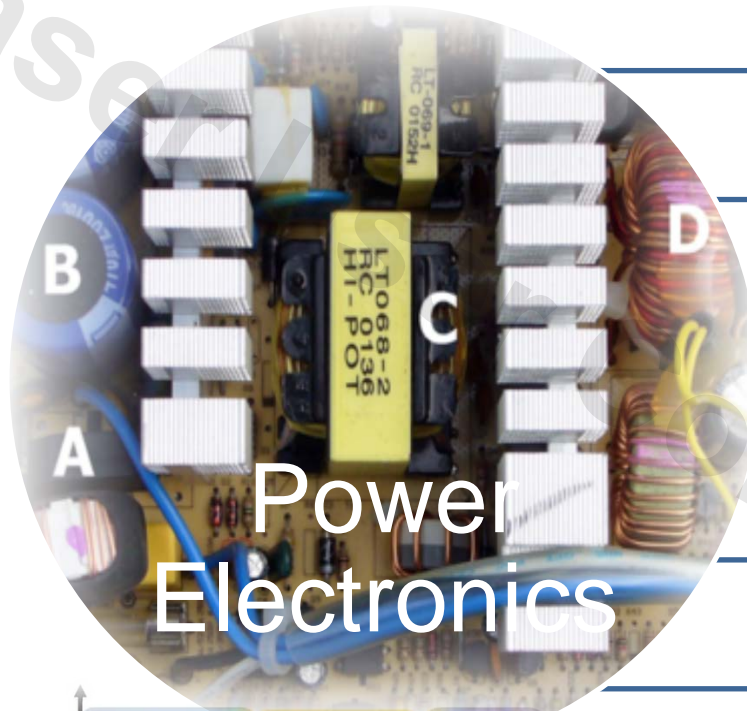


Growth Factors:
Elderly Population & Emerging Markets

Power Electronics

A Common Denominator

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2014 Oct
10pp



Computing



Automotive



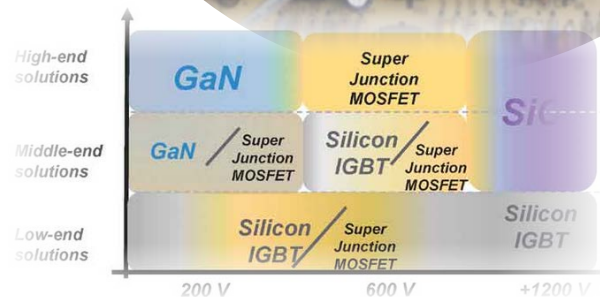
Medical



IoT



Consumer Electronics



New Device Technology

Source :UK Power Electronics report and Electronic Design

Design Challenges

1. Green Power Design
2. Energy storage issue
3. Energy conversion efficiency
4. Power Management
5. Analog Device Interface

PSpice Enhancement

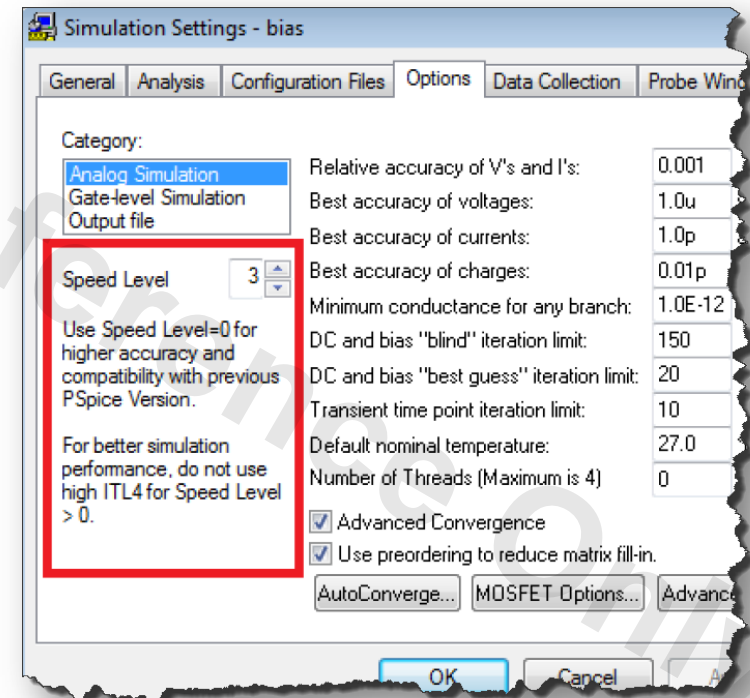
- Power Electronic Designing Vision
- Performance Upgrade
- Model Support Enhancement
- Features Enhancement
- IBIS model support to V5.0



Performance Improvements

Speed Upgrades

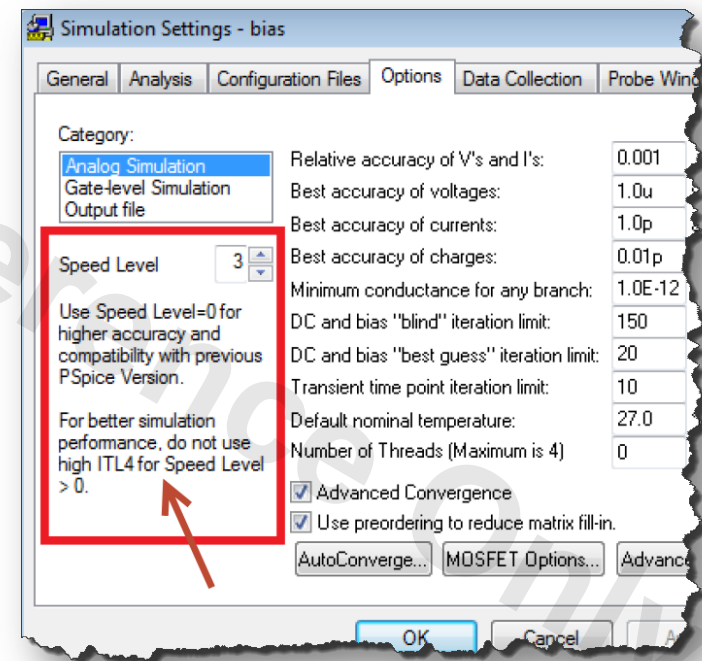
- 5 levels of speed upgrades
 - Default speed level is 3
 - Speed level 0 should be set for compatibility with previous releases
- Removed multi-core usage limit and default multi-thread usage
 - Previous releases used 50% of the available threads up to 4 cores
- Speed level allows faster switching of devices and shows substantial improvement
 - In test cases with switches, more than a 5x performance improvement has been measured at level 3



Performance Improvements

Convergence Improvements

- Previous release required a high ITL4 values when using Switches circuits to achieve convergence
 - At low ITL4 values, convergence errors were observed
 - At high ITL4 values, performance and mathematic errors were frequently observed
- With QIR7 improvements, it is recommended to use lower values of ITL4 to achieve convergence and performance
 - Note: using SPEED_LEVEL=0 will require high ITL4 values to converge



Performance Improvements

New Convergence Options

16.6

Advanced Analog Options

Total Transient iteration limit (0=infinity):	0	(ITL5)
Relative magnitude for matrix pivot:	1.0E-3	(PIVREL)
Absolute magnitude for matrix pivot:	1.0E-13	(PIVTOL)
Simulation algorithm:	default	(SOLVER)
Relative factor for minimum delta	1	(DMFACTOR)
No GMIN across current sources	<input type="checkbox"/>	(NOGMINI)
Worst Case Deviation	0	(WCDEVIATION)
Absolute Data Value Limit	0	(LIMIT)
Enable Breakpoints for Dependent Sources	<input type="checkbox"/>	(BRKDEPSRC)
Bias Point		
Use Gmin Stepping	<input type="checkbox"/>	(STEPGMIN)
Gmin Steps	0	(GMINSTEPS)
Skip Source-Stepping	<input type="checkbox"/>	(NOSTEPSRC)
ITL6	0	(ITL6)
Do not Step dependent sources during Source-Stepping	<input type="checkbox"/>	(NOSTEPDEP)
Step GMIN inside Source-Stepping	<input type="checkbox"/>	(GMINSRC)
Use Pseudo-Transient	<input type="checkbox"/>	(PSEUDOTRAN)
Pseudo Tran Steps	0	(PTRANSTEP)
Transient		
Integration Method	Default	(METHOD)
Relative Time step Tolerance	7	(TRTOL)

OK Cancel Reset

16.6 with QIR Update 3

Advanced Analog Options

Total Transient iteration limit (0=infinity):	0	(ITL5)	Bias Point		
Relative magnitude for matrix pivot:	1.0E-3	(PIVREL)	Use Gmin Stepping	<input type="checkbox"/>	(STEPGMIN)
Absolute magnitude for matrix pivot:	1.0E-13	(PIVTOL)	Gmin Steps	0	(GMINSTEPS)
Simulation algorithm:	default	(SOLVER)	Skip Source-Stepping	<input type="checkbox"/>	(NOSTEPSRC)
Relative factor for minimum delta	1	(DMFACTOR)	Source-Stepping Iteration Limit	0	(ITL6)
No GMIN across current sources	<input type="checkbox"/>	(NOGMINI)	Do not Step dependent sources during Source-Stepping	<input type="checkbox"/>	(NOSTEPDEP)
Worst Case Deviation	0	(WCDEVIATION)	Step GMIN inside Source-Stepping	<input type="checkbox"/>	(GMINSRC)
Absolute Data Value Limit	1.0E12	(LIMIT)	Use Pseudo-Transient	<input type="checkbox"/>	(PSEUDOTRAN)
Enable Breakpoints for Dependent Sources	<input type="checkbox"/>	(BRKDEPSRC)	Pseudo Tran Steps	0	(PTRANSTEP)
Minimum Diode Rs value	<input checked="" type="checkbox"/> 1.0E-4	(DIODERS)	Transient		
Minimum Diode Cig value	<input checked="" type="checkbox"/> 2.0E-12	(DIODECJO)	Integration Method	Default	(METHOD)
Minimum BJT Cje and Cjc value	<input checked="" type="checkbox"/> 1.0E-11	(BJTCJ)	Relative Time step Tolerance	7	(TRTOL)
Generate 1op files for convergence failure	<input type="checkbox"/>	(CONVAID)	Use CSHUNT	<input type="checkbox"/>	(CSHUNT)
			Enable continuation methods	<input type="checkbox"/>	(TRANCONV)

OK Cancel Reset

Features Enhancement

New Model Search

New Part Search Window

The screenshot displays the OrCAD Capture Marketplace interface. At the top, a navigation bar includes links for Home, Component Search, Models (highlighted), Multimedia, PCB Services, OrCAD Apps, EDA360, and Contact. The main content area is titled "PSpice & IBIS Models" and features a banner with the text "Find the right simulation or signal integrity model to help achieve first-pass success". Below this, a section titled "Models" provides information about PSpice and IBIS models. To the right, a "Search" section includes a search bar and instructions on how to search. Below the search section, "Popular Models" are listed, including STMicroelectronics Thyristors & AC Switches Smart Power Devices SPICE models and National Semiconductor SPICE Macromodels for Op Amps. At the bottom, a "Featured Vendor" section is visible. A red arrow points from the "Search" button in the top right corner of the OrCAD window to the "Search" button in the new model search window. The new model search window is titled "PSpice Part Search" and includes a "Search" button, a "Categories" tab, and a list of categories such as "1_shot" (10Parts), "7400" (150Parts), "74ac" (750Parts), "74act" (74Parts), and "74als" (183Parts).

Place SI Analysis Macro PSpice Acc

Pin... Pin Array... Part... PSpice Component... Parameterized Part... Wire W

PSpice Part Search

Hide Categories View

Categories Library

"1_shot" (10Parts)
"7400" (150Parts)
"74ac" (750Parts)
"74act" (74Parts)
"74als" (183Parts)

Search

OrCAD Capture Marketplace

Home Component Search Models Multimedia PCB Services OrCAD Apps EDA360 Contact

PSpice & IBIS Models

Find the right simulation or signal integrity model to help achieve first-pass success

Models

PSpice and IBIS models are used in simulating analog circuits and signal integrity analysis. Significant numbers of publicly available PSpice / IBIS simulation models and library parts are from semiconductor and supplier sources, but are traditionally difficult to locate or know the location of them all. Engineers now have a conduit to help locate needed models and library parts to use in design simulation and analysis.

Featured Vendor

Search

Search Our Site ...

Search by Location, keyword, language, content type, etc.

Popular Models

- STMicroelectronics Thyristors & AC Switches Smart Power Devices SPICE models (OrCAD .lib & .olb format)
- National Semiconductor SPICE Macromodels for Op Amps

Play a role in the OrCAD Capture Marketplace

Select the library to add Add

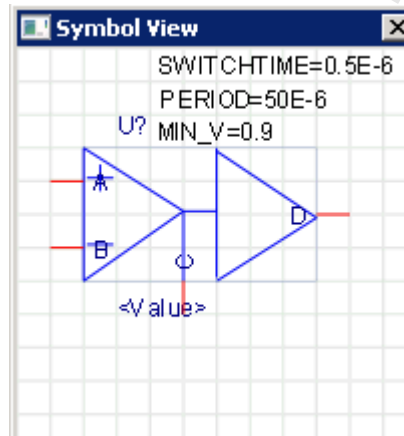
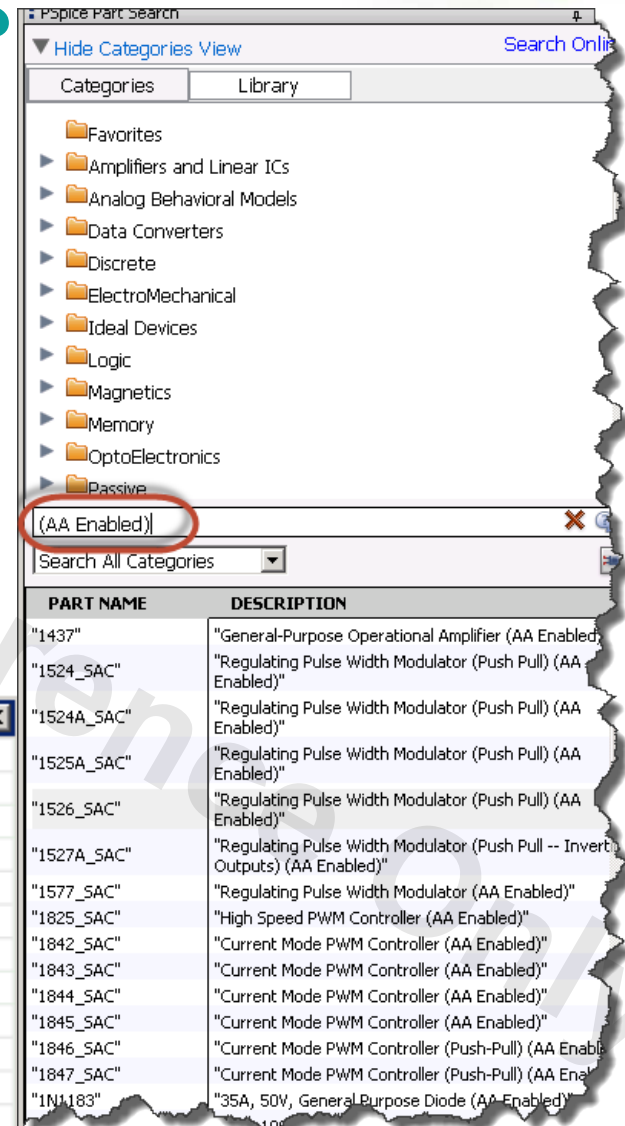
INV INV Gate

"IPULSE" "Pulsed Current Source"

SYMBOL LIBRARY:

PSpice Search – Advanced Analysis Parts

- Advanced Analysis Parts are now available through PSpice Searcher
 - Use search string 'A/A Enabled' to find all A/A parts
- Searcher symbol viewer updated



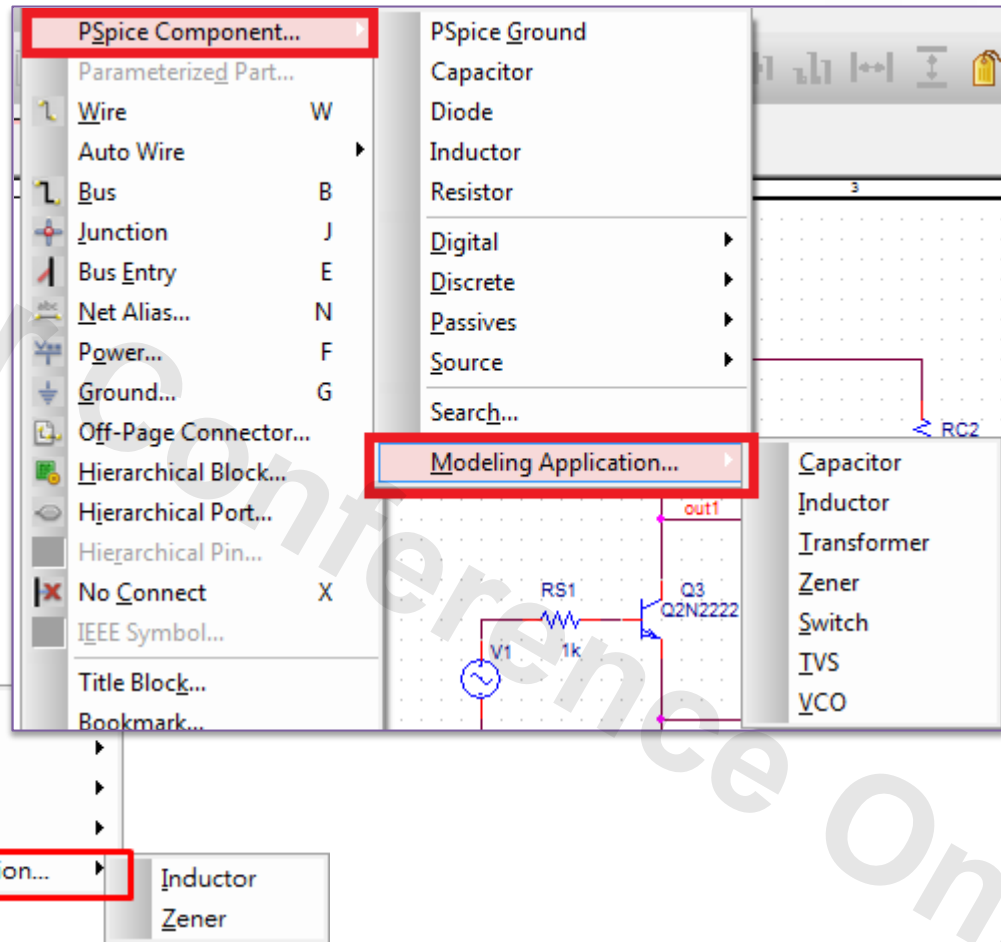
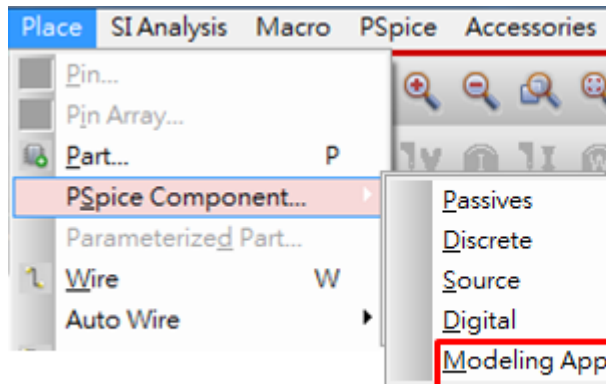
Model Support Enhancement

PSpice Modeling APPs

V16.6 QIR#

PSpiceModeling V2.0 APPs

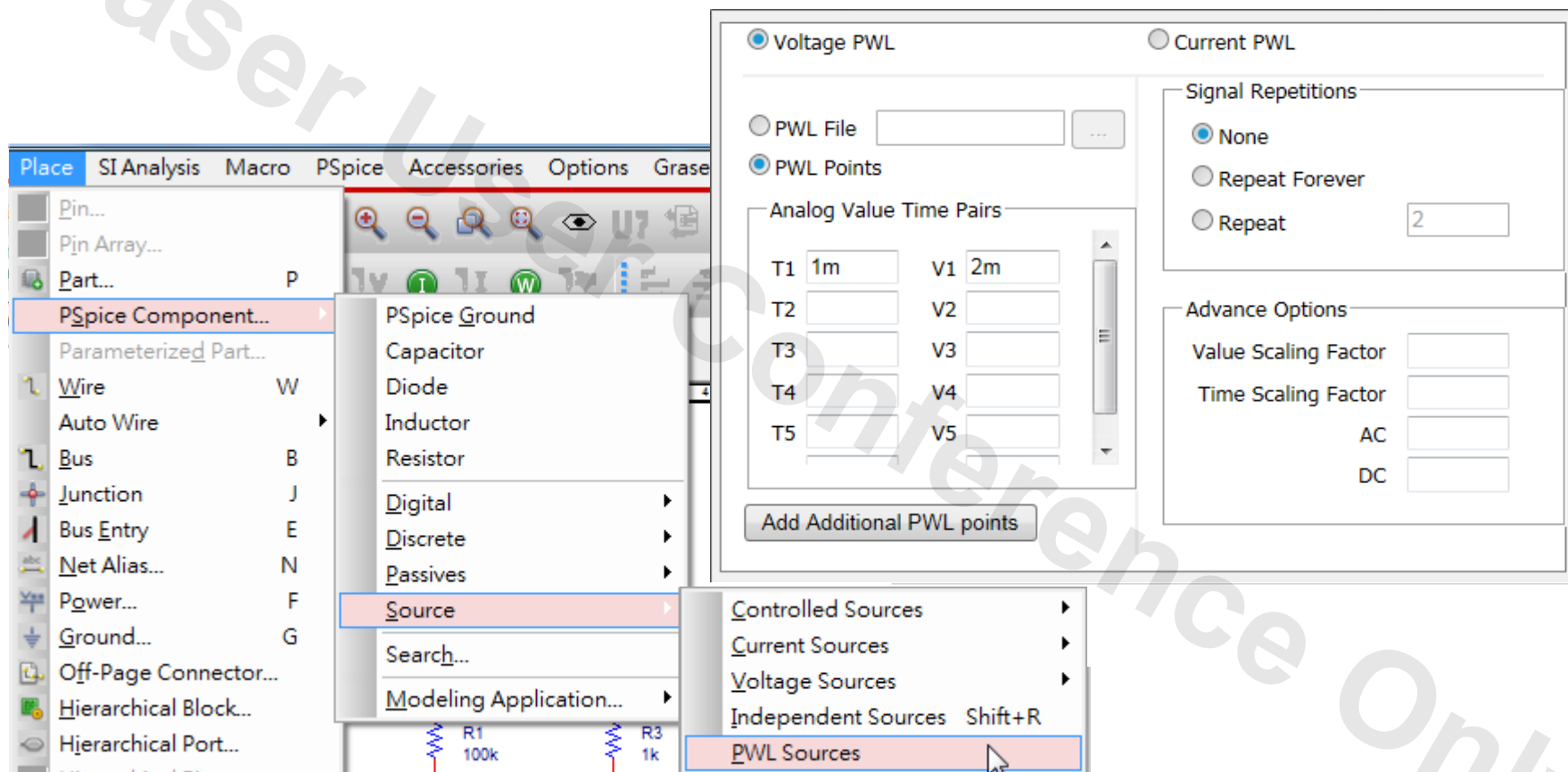
V16.6 Basic



PSpiceModeling V1.0 APPs

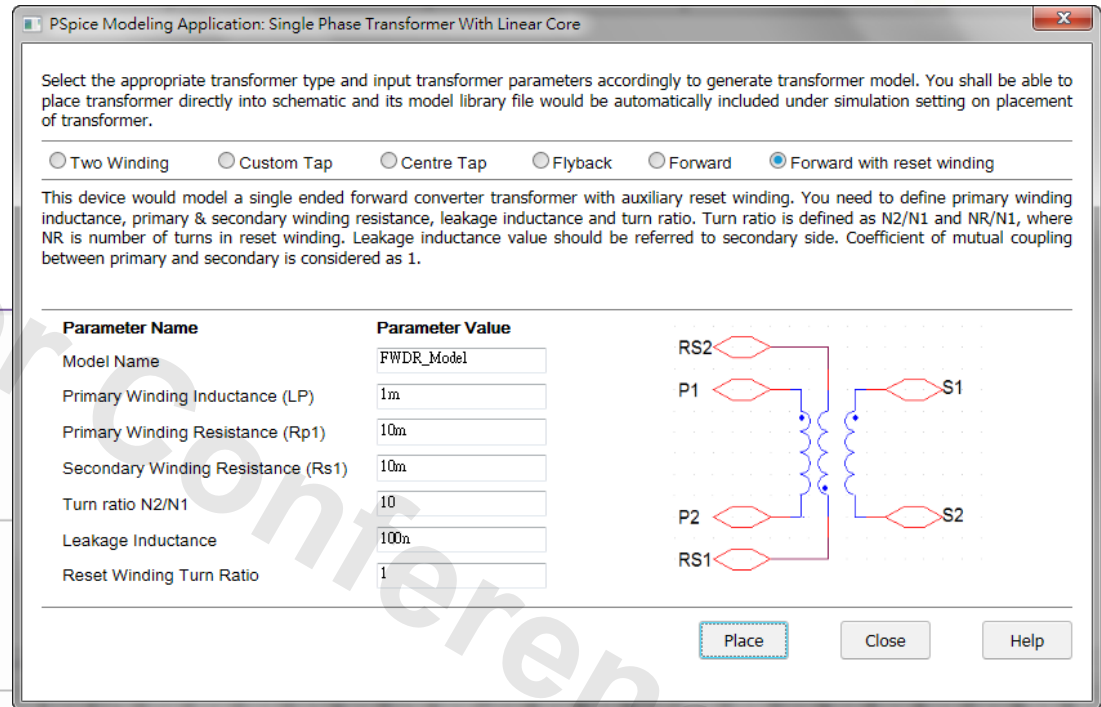
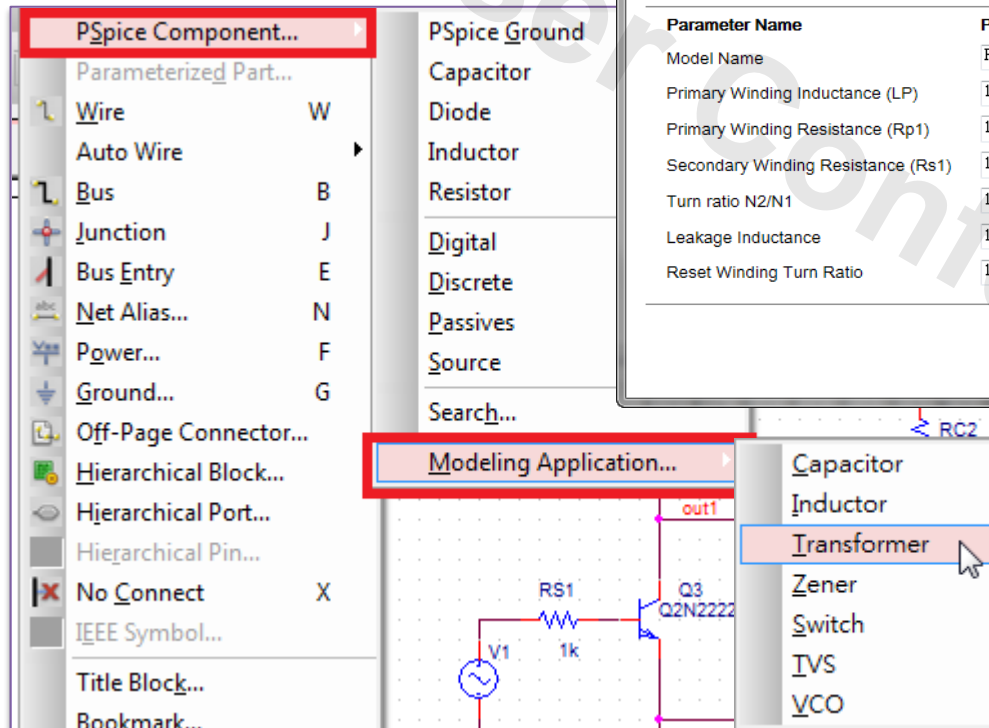
Model Support Enhancement

PSpiceModeling Apps V2.0



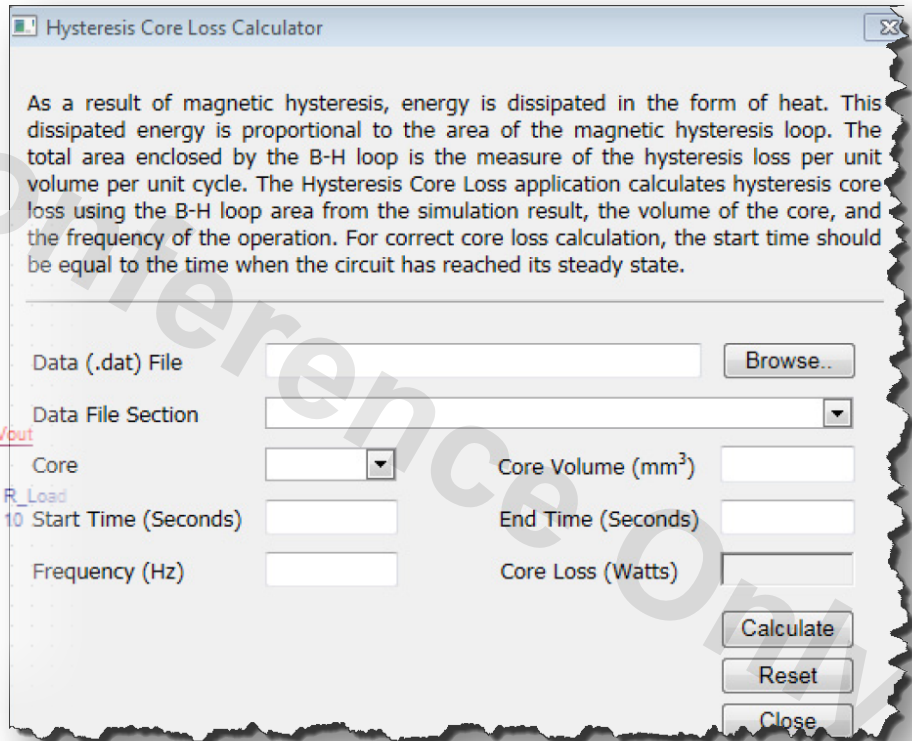
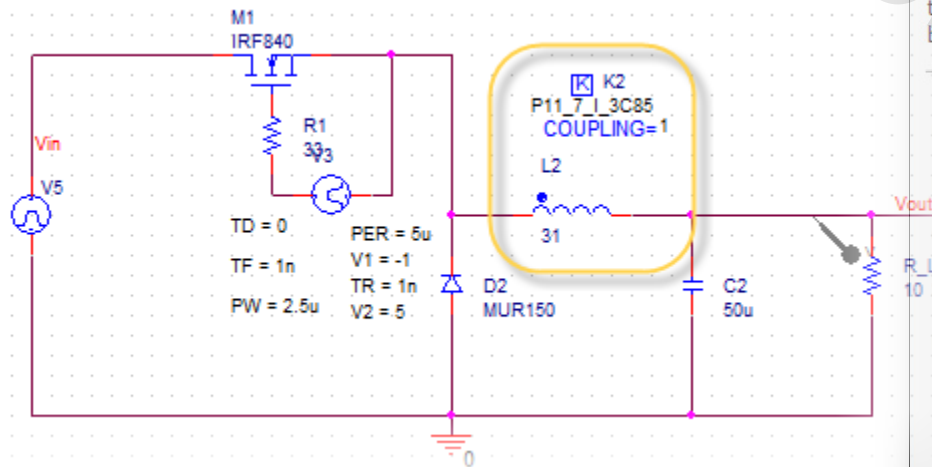
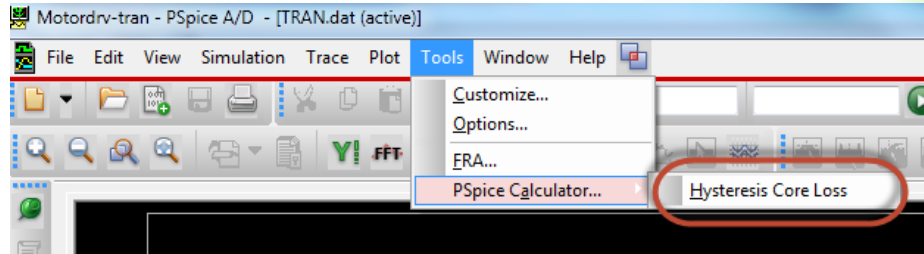
Model Support Enhancement

Simply Transfer Models

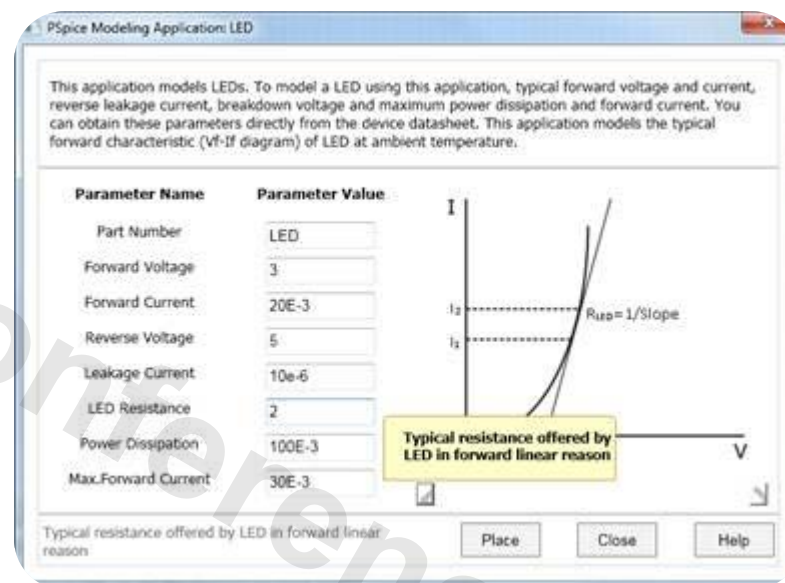
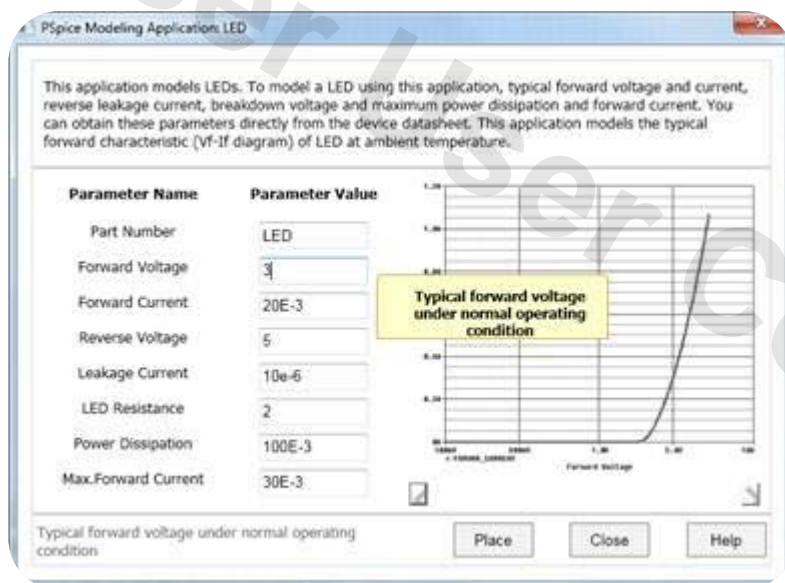


Hysteresis Core Loss Calculator

- App to measure Steady State loss of energy in a magnetic core for power supplies



New PSpice Modeling App for LED Coming in QIR#8



16.6



Quarterly
Incremental
Releases



QIR#8

Model Assignment

The screenshot shows a circuit simulation software interface. In the background, a circuit diagram is visible with components R1 (1K), R2 (50K), C15 (10uF), C11 (10uF), and a central component U3 (NE555). A context menu is open over U3, with the 'Associate' option highlighted. In the foreground, the 'Model Import Wizard : Define Pin Mapping' dialog box is displayed. It contains a table for mapping model terminals to symbol pins.

Model: TLC555 Part: U3

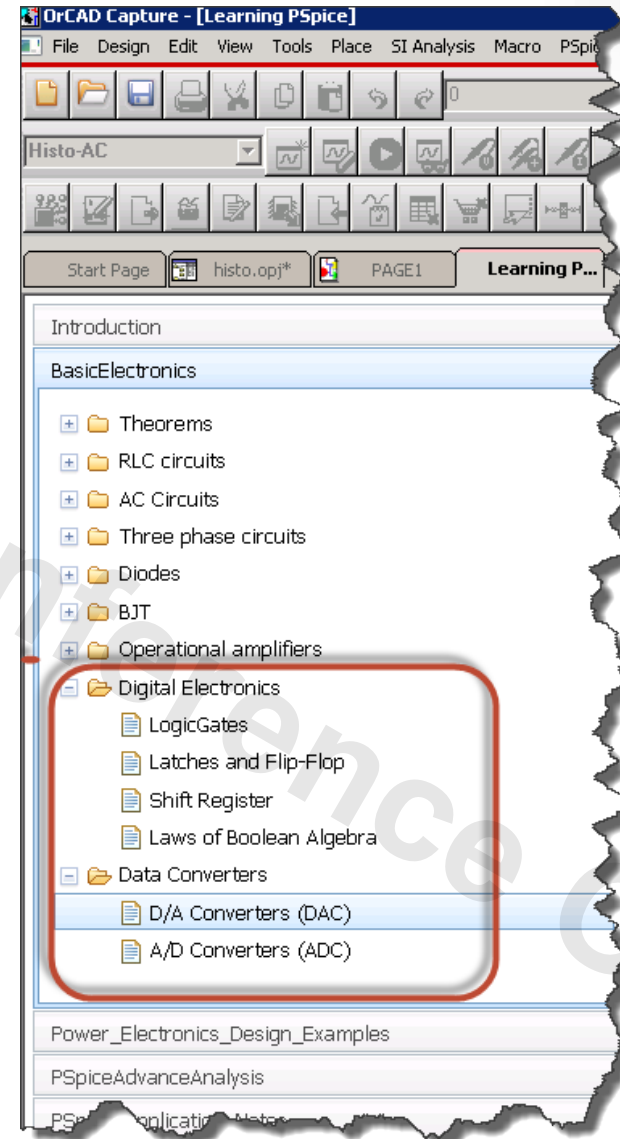
☒ Show Invisible Symbol Power Pins

Model Terminal	Symbol Pin
THRES	THR
CONT	CV
TRIG	
RESET	
OUT	
DISC	DIS
VCC	VCC
GND	GND

Buttons: View Model, < 上一步(B), 完成, 取消, 說明

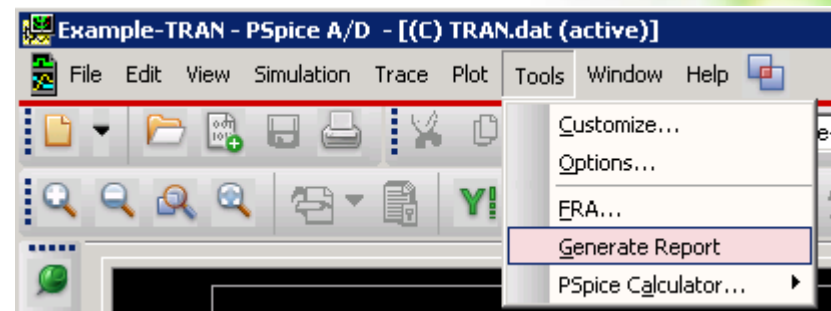
Learning with PSpice

- Instructional / introductory material on
 - Logic Gates
 - Latches
 - Flip-flops
 - Shift Registers
- PSpice Mixed-signal simulator chapters
 - Data converters
 - Analog-to-Digital (ADC)
 - Digital-to-Analog (DAC)



New Simulation Report Capability

- HTML report generated for Analog Transient simulation
 - Average, RMS, and Peak values of Current, Voltage and Power can be reported
- User customizable
 - Tcl source available in installation hierarchy
 - <installation>\tools\pspice\tclscripts\orPspReport
- .TCLPOSTRUN command can be used to configure auto-generation of HTML reports



Bias Value	Max Current	Min Current	Average	RMS	Max di/dt
-6.724173n	112.818u	-107.338u	2.0684u	79.711u	3.27156k
7.738638u	8.34771u	7.46526u	7.69682u	8.17574u	371.011

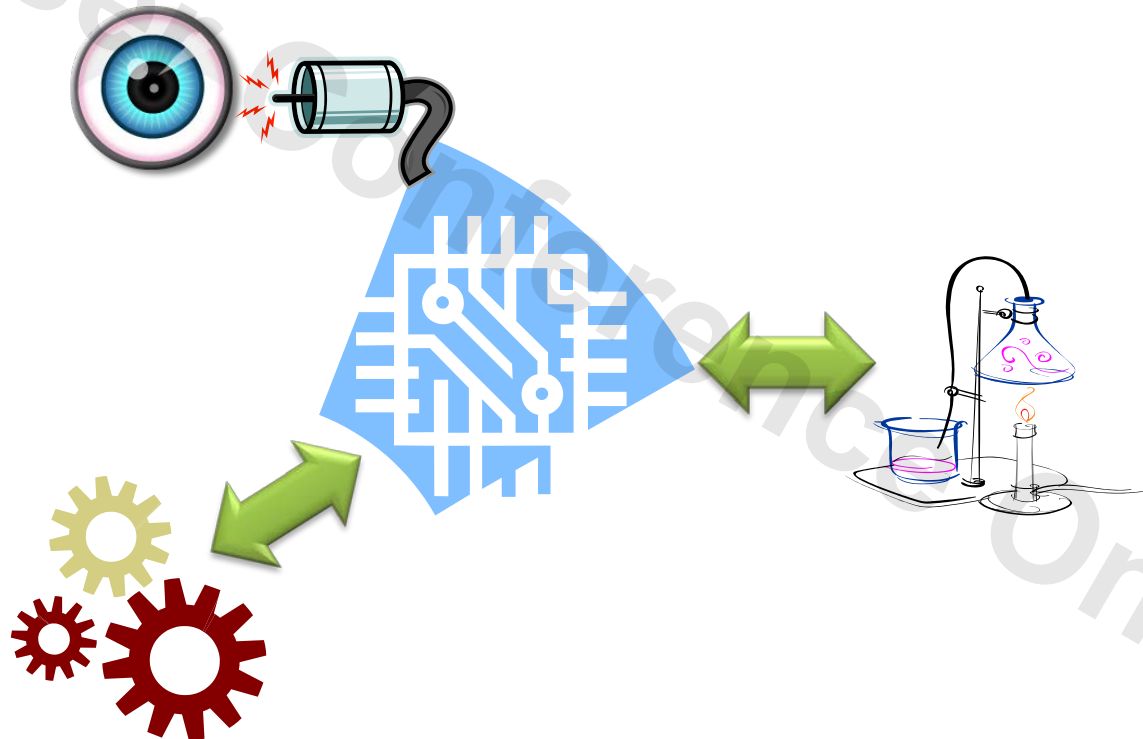
Bias value	Max Voltage	Min Voltage	Average	RMS	Max dV/dt
0.0	0.0	0.0	0.0	0.0	0.0
-4.294311m	52.1454m	-58.4785m	-3.52959m	40.1367m	1.66552Meg
-11.35038	-11.3503	-11.3505	-11.3504	11.3504	11.0859k
-4.302968m	37.276m	-47.5725m	-4.99191m	31.1941m	1.28267Meg
628.3144u	99.6763m	-99.6767m	30.7959u	75.9248m	3.14157Meg

Bias value	Max Power	Min Power	Average	RMS
1.809f	90.1598u	-85.9044u	1.05507u	41.5584u
753.4941u	756.526u	750.162u	753.428u	753.431u
14.9968m	15.1489m	14.8349m	14.9908m	14.9912m
3.990363m	4.59948m	3.31221m	3.95436m	3.98071m
3.989889m	4.77772m	3.2639m	4.00463m	4.03999m
27.26201m	27.2623m	27.2618m	27.262m	27.262m

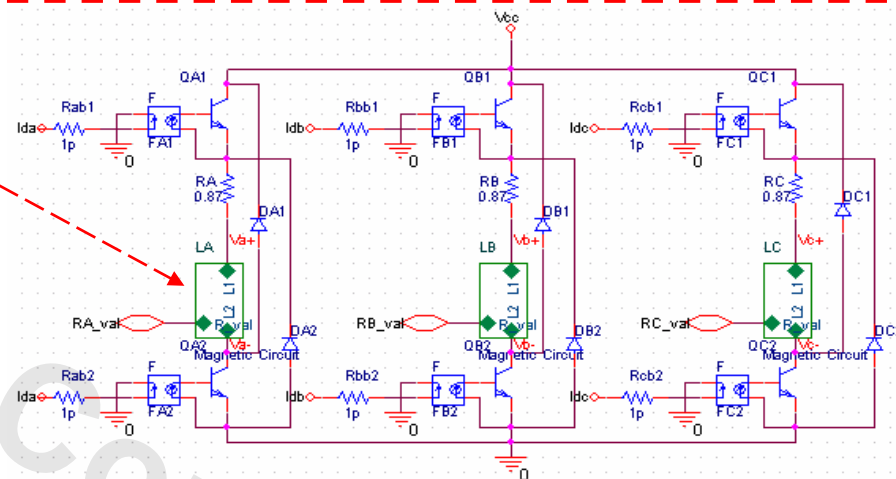
Miscellaneous

Mechatronics integration Design

- Example : Automotive Safety System
- Passive mode : ABS 、 Airbag 、 Reversing radar
- Active mode : DSTC , ROPS , EBD , CWFAB , PDFAB , DAC , LDW

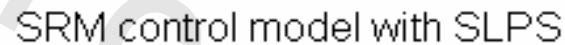


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1991

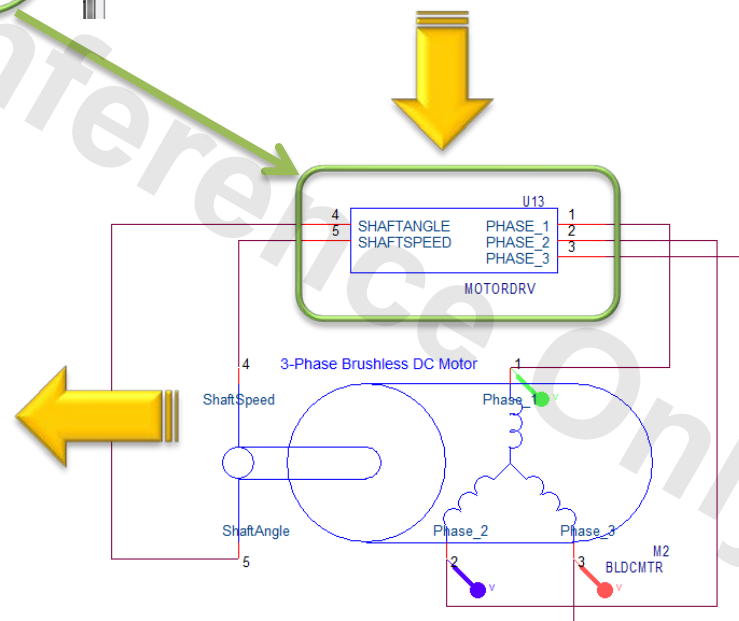
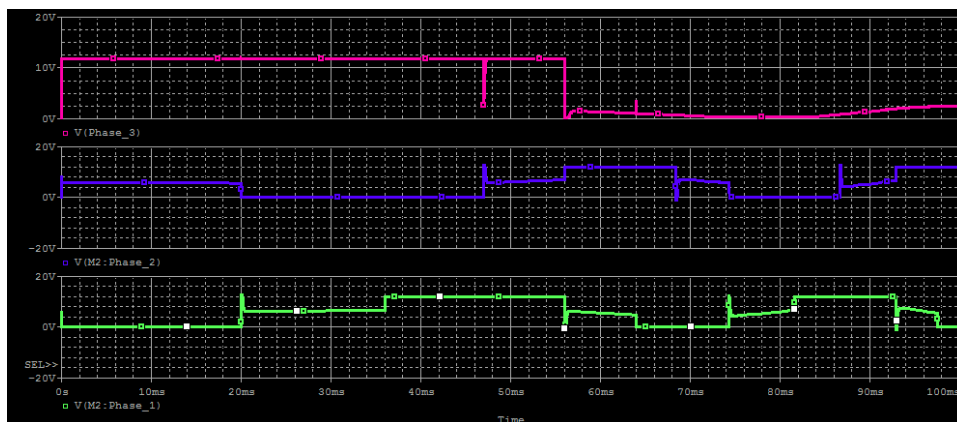
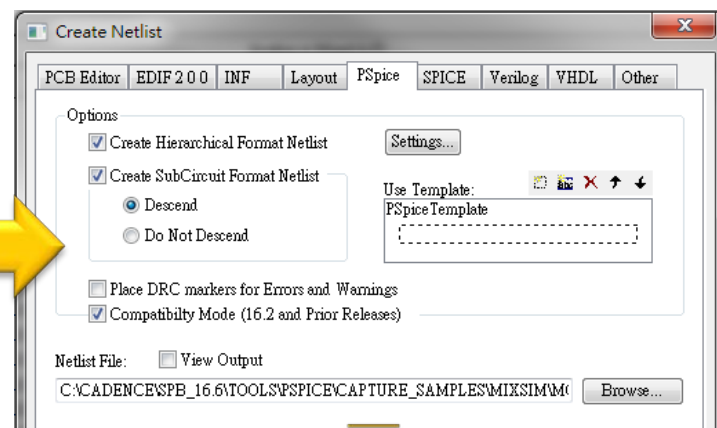
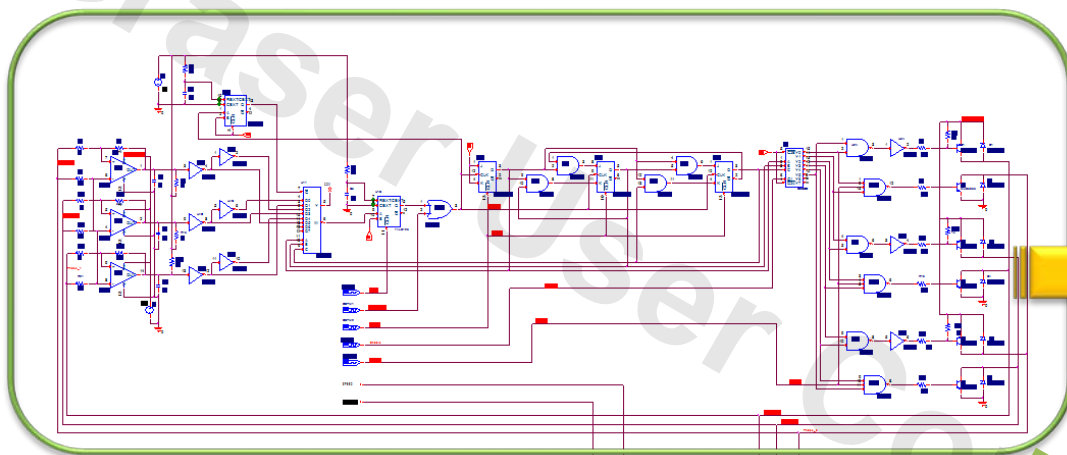


The diagram illustrates the control system architecture. It starts with two reference inputs: I_d (labeled 1) and L_value (labeled 2). These inputs are processed by a block labeled **SLPS** (Sliding Mode Control with a $\frac{1}{s}$ integrator). The output of the SLPS block is fed into a multi-channel processing block. This block contains three parallel paths, each consisting of a summing junction (+), a gain block ($\frac{1}{s}$), and a saturation block (\tanh). The outputs of these paths are then fed into a block labeled **Ex_CuA**, which produces the output current I_j (labeled 1). The output current I_j is then fed into a block labeled V_a , which produces the output voltage V_j (labeled 2). The diagram also shows the internal signals Ex_CuB and Ex_CuC and the output current I_j and output voltage V_j .

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Modularized Design and Simulation



Modularized Design and Simulation

