OrCAD Sigrity ERC

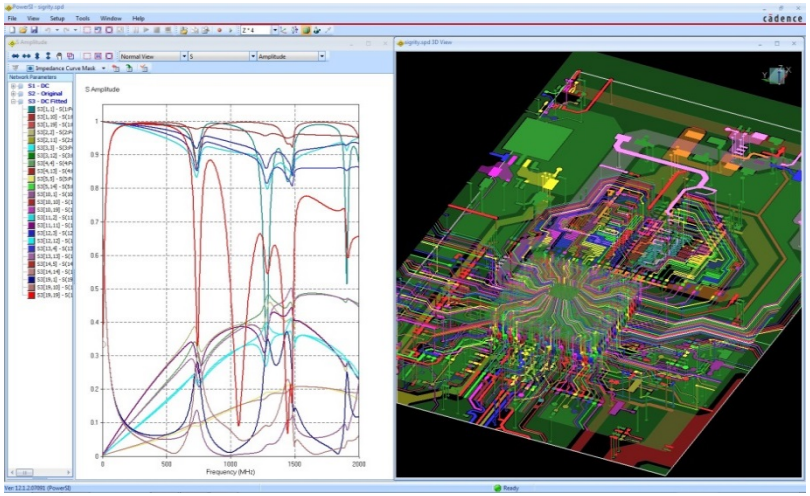
Josh Moore – Product Management Director
Cadence OrCAD Solutions

Graser User Conference Only

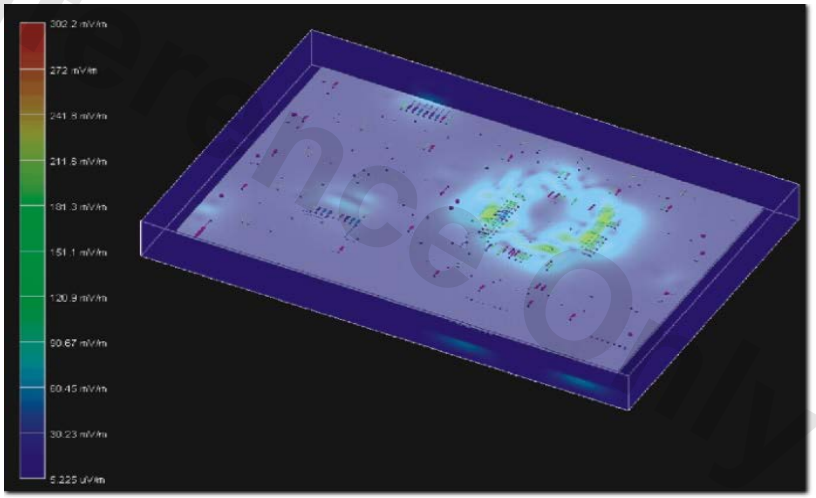
OrCAD
CADENCE PCB SOLUTIONS

Cadence Sigrity – Industry-leading SI / PI Solution

- Product of choice for power and signal integrity analysis
  - Integration with full wave 3D EM solver
- Layout-based frequency-domain SI / PI simulation
  - Highly accurate modeling of PCB structures
- Single-ended and mixed-mode results and post-processing
- Unique capability for ensuring accuracy down to DC
- Targeted workflows to streamline setup operations



Frequency domain SI, PI and EMC



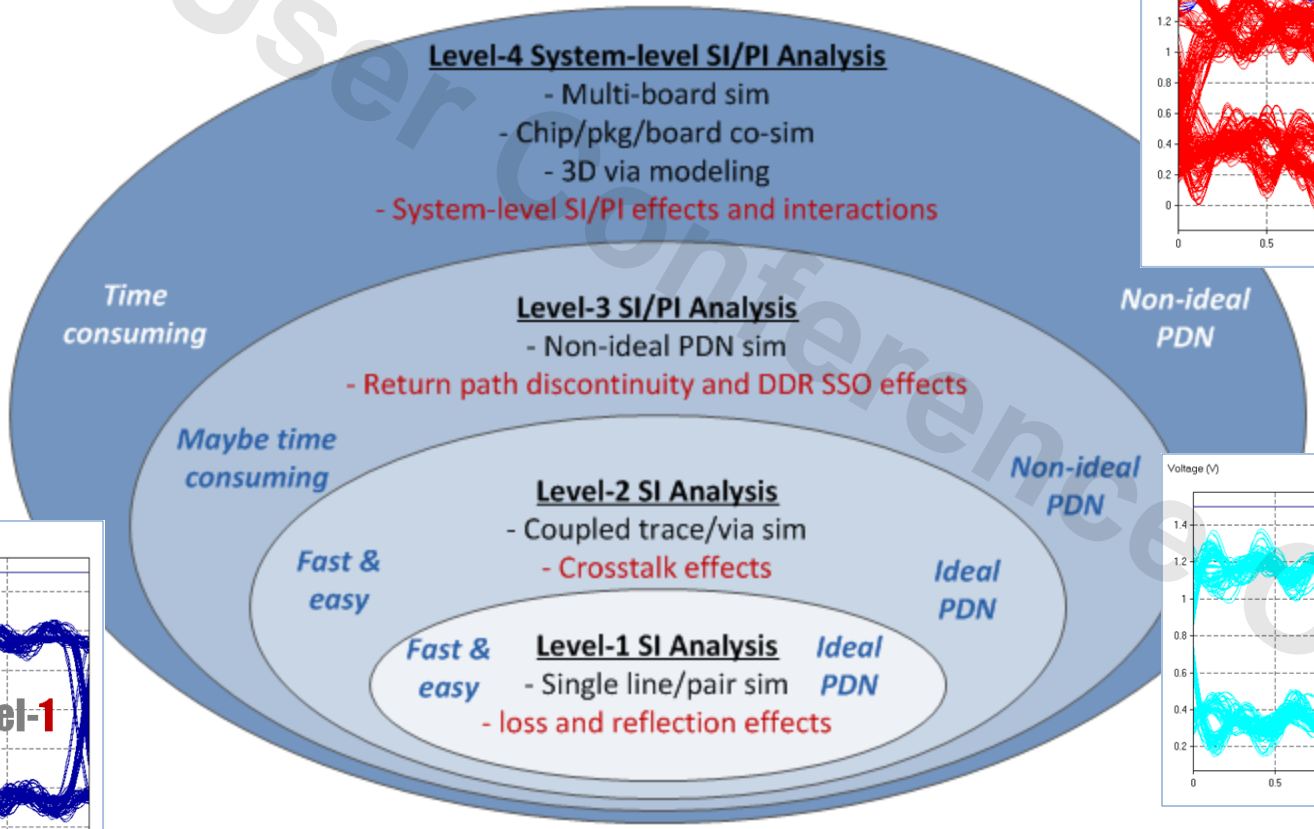
Cadence User Conference

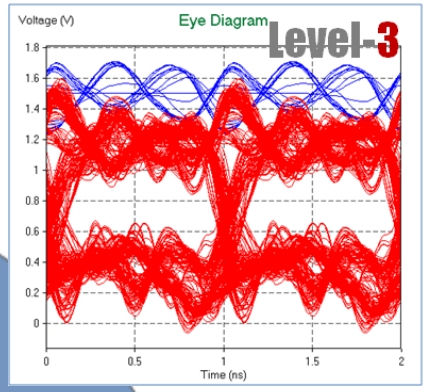
© 2014 Cadence Design Systems, Inc..

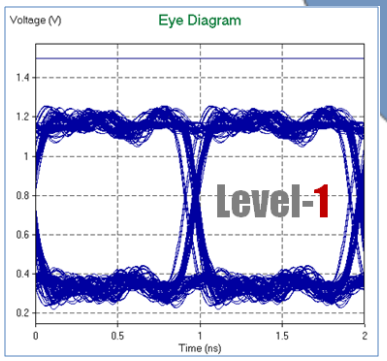
OrCAD™
CADENCE PCB SOLUTIONS

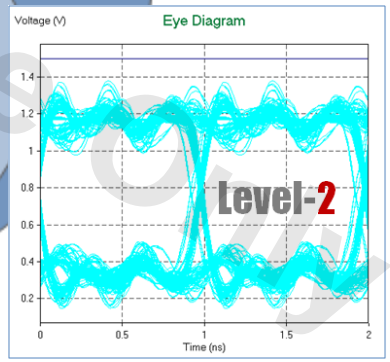
Different SI / PI / EMI Levels for Different Needs

- Simulations and analysis can be done at four levels
  - Based on considerations of trace / via couplings, non-ideal PDN, etc.
- Both layout-based and model-based analysis









Cadence User Conference

© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS

Layout-based, Time-domain SI / PI Simulation

- SPEED2000™ is industry's only layout-based, time-domain SI / PI solution
- Five workflows for SI / PI analysis from level 1 to 3

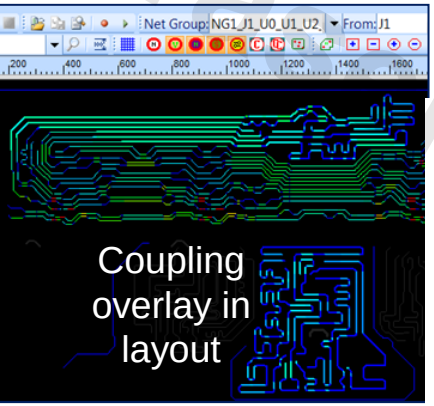
Workflow 1 General SI Simulation	Workflow 2 Trace Impedance/ Coupling Check	Workflow 3 SI Performance Metrics Check	Workflow 4 DDR Simulation	Workflow 5 Time-domain PDN Simulation
Mainstream SI *L1/L2 for fast sim* Easy to setup; Sim runs fast Waveforms & measurements	Geometry based Trace impedance, coupling & reference check for entire board or net groups Results tables; Results plots; Layout overlay; Layout x-probing	Simulation based *L1/L2 for fast sim* *L3 for non-ideal PDN* Loss, reflection, xtalk check, typically by net groups Waveforms; Xtalk v_max & v_min	Layout-based DDR simulation *L1/L2 for fast sim* *L3 for SSO* No s-parameter model needed for on-board DRAMs Waveforms & measurements	Layout-based TD PDN sim PDN chip-pkg-board co-sim with *-Voltus die mode* *- XcitePI IO model with die grid* Voltage / current distributions; dynamic noise propagation

Cadence User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD™ CADENCE PCB SOLUTIONS

Geometry- and Simulation-based Layout Checks

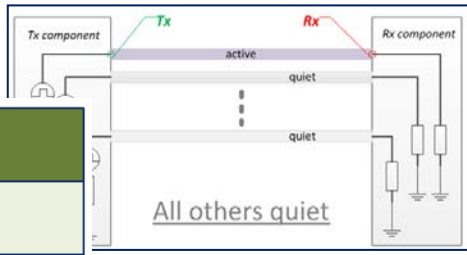


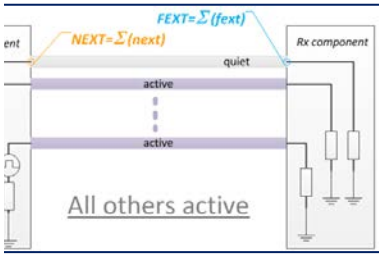
Coupling plot

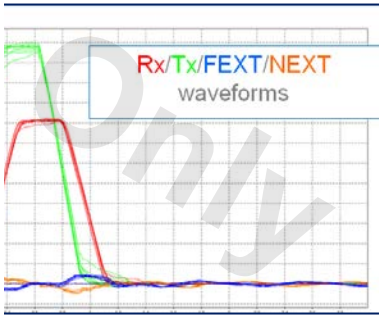
Coupling table

Electrical Rules Checks

Trace Impedance/Coupling Check	SI Metrics Check
Geometry-based	Simulation-based
Micro, individual, segment-level view (coupling %, Ω & mm)	Macro, combined net-level, view (mv & ps)
Options Check all nets Check selected nets Check nets in net groups	**Options** Level-1 simulation Level-2 simulation Level-3 simulation
Results Coupling coefficient Impedance Trace reference Summary & detailed tables Expanded & collapsed plots Layout overlay Layout cross probing HTML report	**Results** Waveforms: Tx / Rx / NEXT / FEXT v_min & v_max SI performance metrics HTML report







OrCAD™
CADENCE PCB SOLUTIONS

Cadence User Conference Only

© 2014 Cadence Design Systems, Inc..

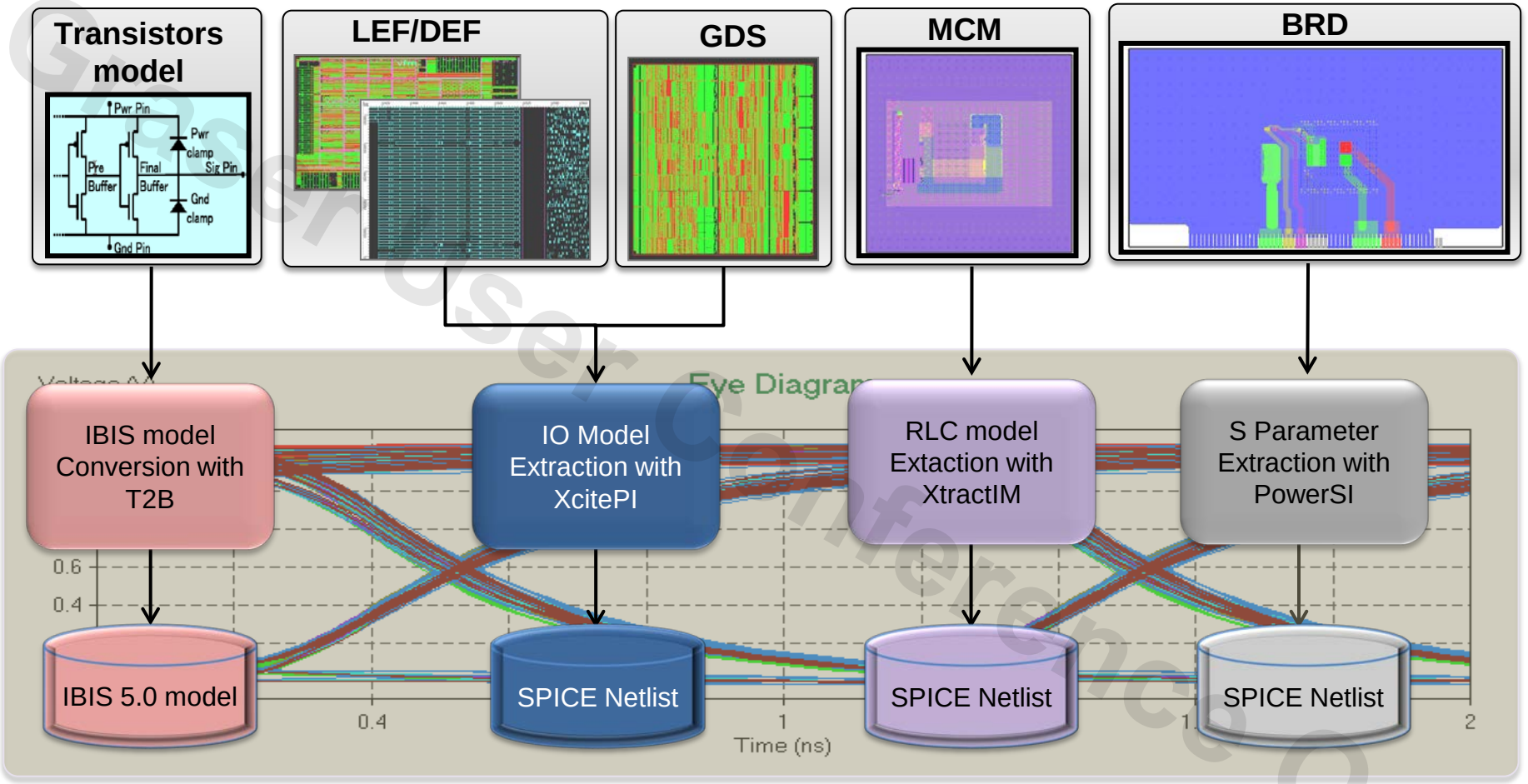
SI Barriers for PCB Designers

Graser User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS

Complex Flow for Simulation and Verification



- Comprehensive SI / PI simulation and analysis relies on experienced, well trained engineers with sophisticated tools

Cadence User Conference Only

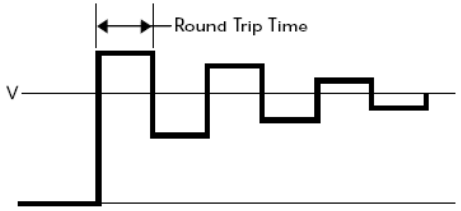
© 2014 Cadence Design Systems, Inc..

OrCAD™ CADENCE PCB SOLUTIONS

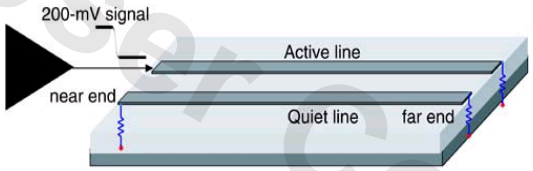
Common SI Analysis Needs to be Simple

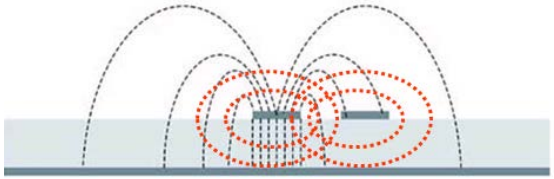
Grasser User Conference Only

- Reflections (ringing)
  - Impedance mismatch

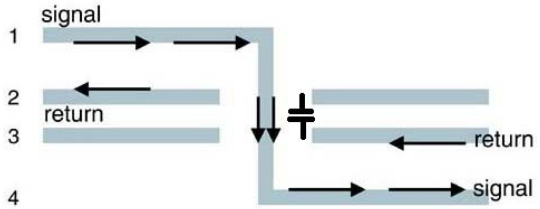


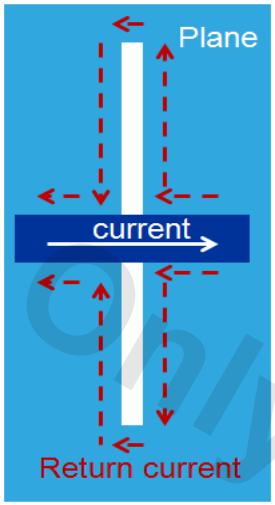
- Crosstalk
  - Electromagnetic coupling between adjacent signal lines





- Return path discontinuity
  - Layer transitions or plane split crosses



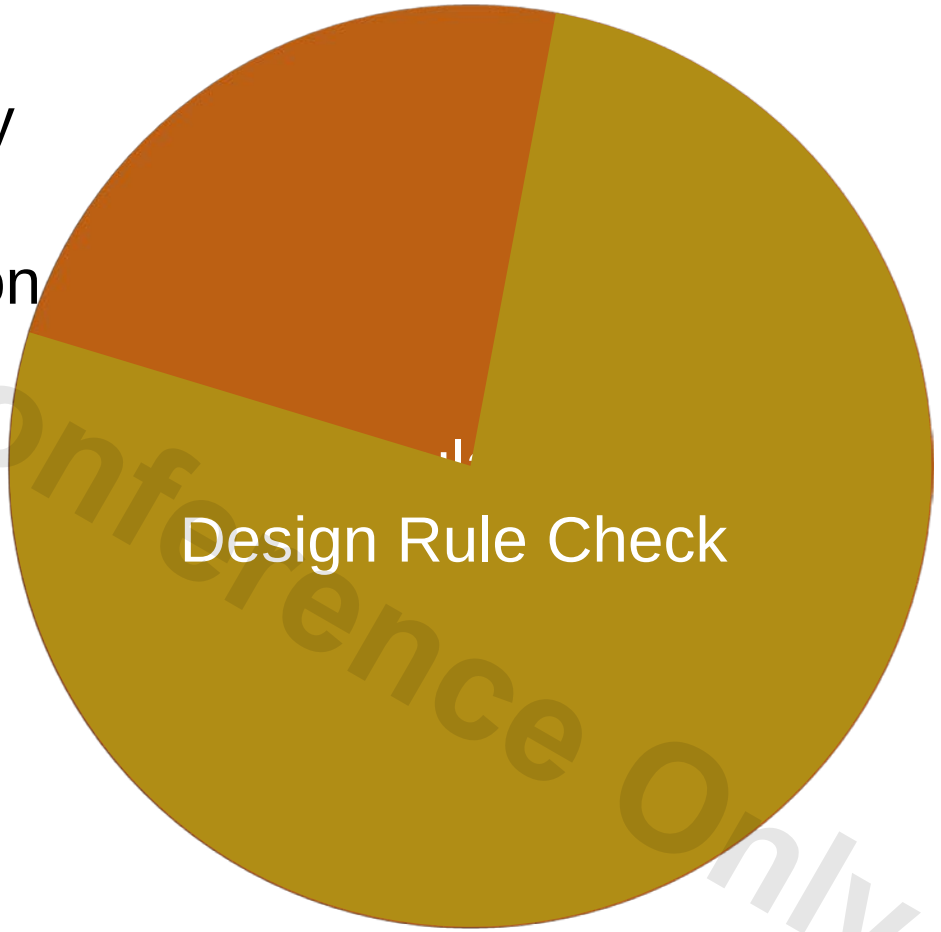


© 2014 Cadence Design Systems, Inc..

OrCAD
CADENCE PCB SOLUTIONS

Simulation and Design Rule Check

- Ideally, designs should be 100% driven and validated by simulation
- Typically, pre-layout simulation results drive design rules
- Only small portion covered by simulation
- PCB DRCs usually contain only dimension information such as length, width, distance, spacing, etc.
- What do constraints / DRCs forget to tell you?



Graser User Conference Only

© 2014 Cadence Design Systems, Inc..

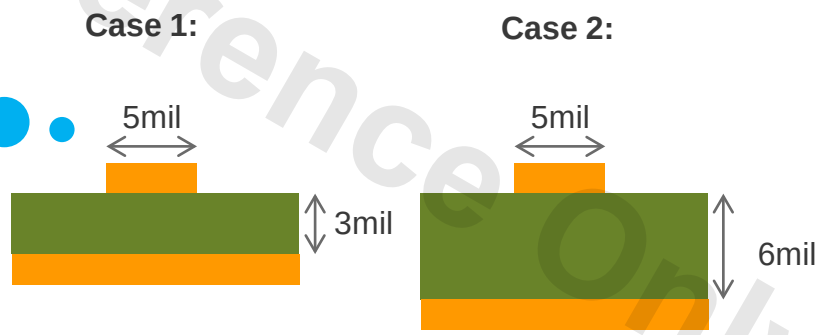
OrCAD™
CADENCE PCB SOLUTIONS

DRC Correct or Electrically Correct?

Grace User Conference Only

- Simple design rule checks for dimension will not validate electrical characteristics

Question:
1. Are the DRC results of these 2 structures the same or different? **Same**
2. Do these 2 structures have the same or different electrical properties? **Different**
3. Do these 2 structures have the same impedance or not?



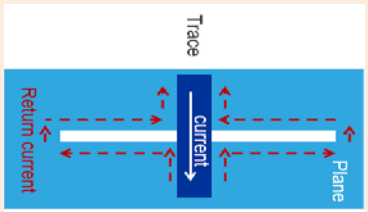
© 2014 Cadence Design Systems, Inc..

OrCAD
CADENCE PCB SOLUTIONS

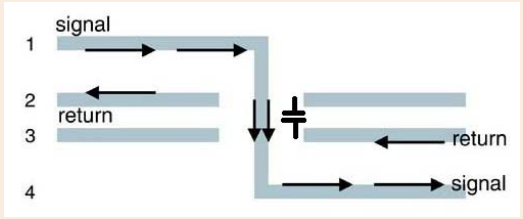
DRC Correct or Electrically Correct?

Grace User Conference Only

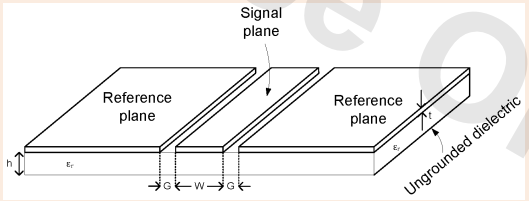
- Pre-layout simulation, defines a trace width to be 5 mils for a target impedance
  - The following routed trace results in **no DRC** violation



1. Reference change
2. Cross plane split



1. Layer Transition

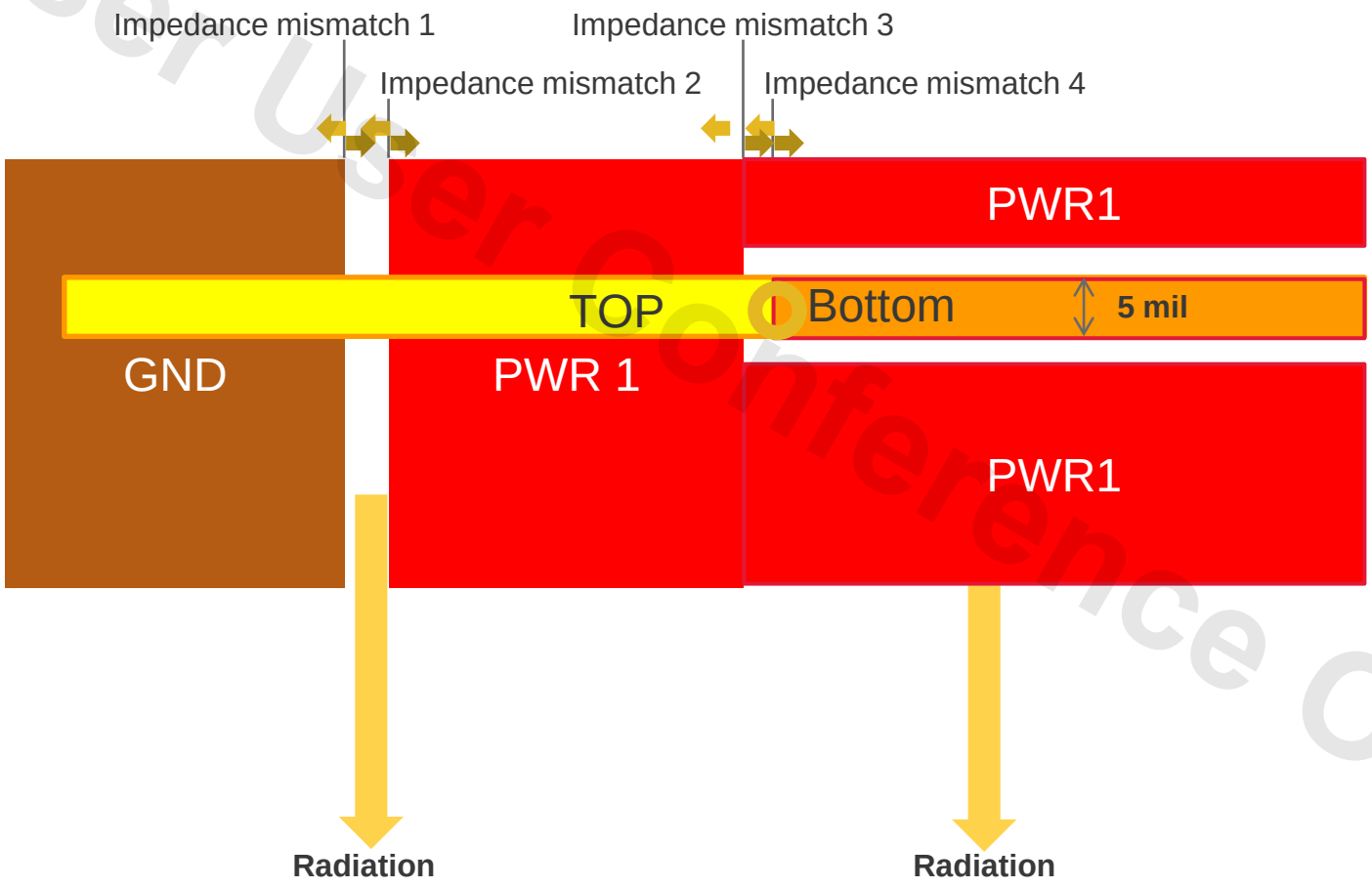


1. Coplanar reference

© 2014 Cadence Design Systems, Inc..

OrCAD
CADENCE PCB SOLUTIONS

DRC Correct or Electrically Correct?



Graser User Conference Only

© 2014 Cadence Design Systems, Inc..

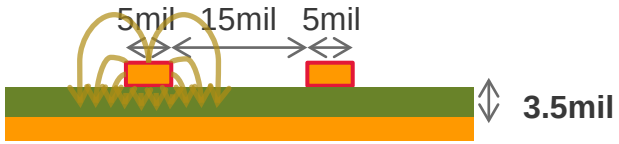
OrCAD™
CADENCE PCB SOLUTIONS

DRC Correct or Electrically Correct?

Grace User Conference Only

- To minimize crosstalk, many follow the ‘3W’ rule – set the spacing between critical adjacent traces to 3 times the width of the trace
  - The following routed trace results in **no DRC** violation

‘3W’ rule works for the following structure



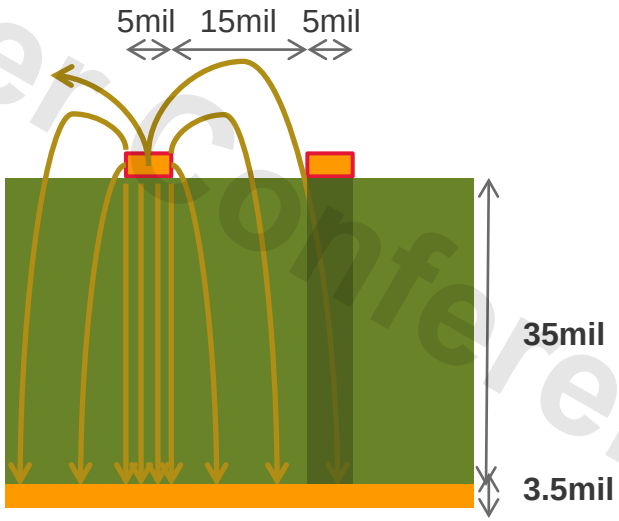
No DRC violation ➡ No Xtalk issue

© 2014 Cadence Design Systems, Inc..

OrCAD™ CADENCE PCB SOLUTIONS

DRC Correct or Electrically Correct?

- What if the stack-up looks like the following, will ‘3W’ rule still work?



No DRC violation ➡ Still no Xtalk issue?

How do you know?

Grasper User Conference Only

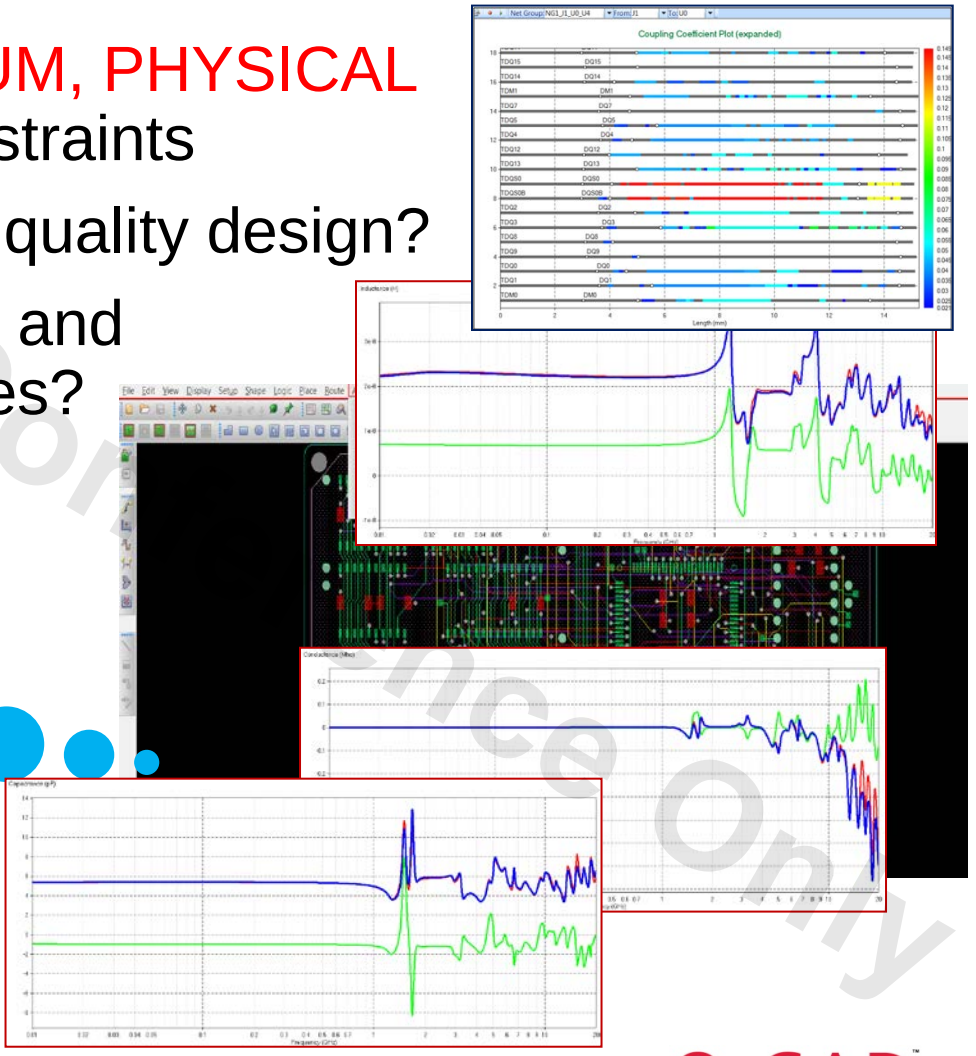
© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS

DRC Correct or Electrically Correct?

- DRCs only validate MINIMUM, PHYSICAL requirements of design constraints
- Do no DRCs mean a good, quality design?
- Can PCB designers identify and address signal quality issues?

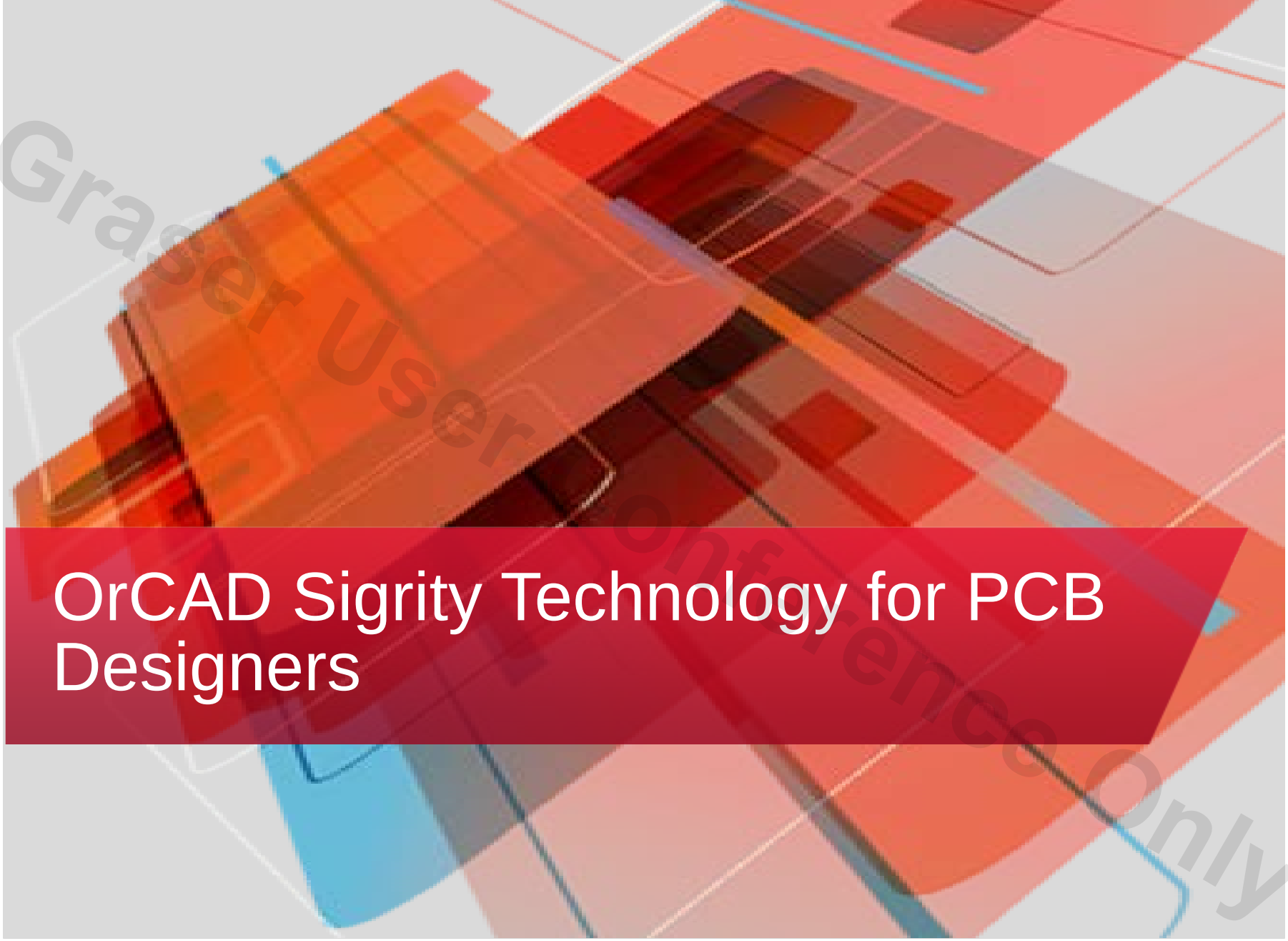
How difficult is it to setup?
Is it easy to use?
Do I have to be an SI expert?
Is it expensive?



Grass Lee Confidence Only

© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS



OrCAD Sigrity Technology for PCB Designers

Graser User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS

Electrical Rule Checks with OrCAD Sigrity ERC

- ERCs are better than DRCs for signal quality validation
  - Go beyond MINIMUM, GEOMETRY-BASED constraint validation
- Easy to use, minimal setup
- PCB designers can identify and address signal quality issues

Grasser User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD
CADENCE PCB SOLUTIONS

OrCAD Sigrity ERC (coming 2015 / 17.0 & QIRs)

Graser User Conference Only

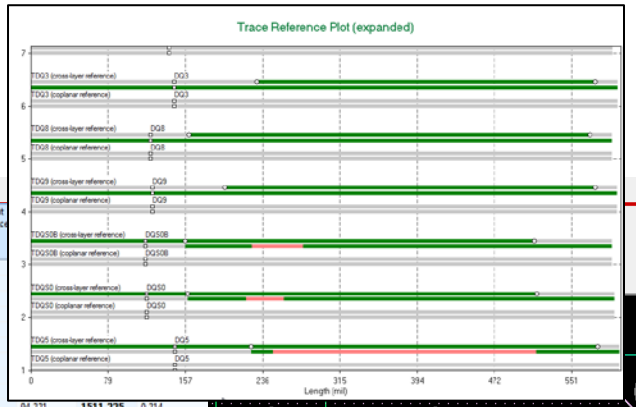
- No complex modeling / setup required
- Electrical checks include
  - SI Metrics (Level 1 & Level 2)
    - Differential Pair Serial Link Screening
  - Trace impedance check
  - Trace return path check
  - Via return path check
  - Trace coupling check
  - Net coupling check
  - Additional future checks

- OrCAD FloorPlanner
  - Place and route edits only
  - Cross-probe (pan / highlight / zoom) between analysis & layout

© 2014 Cadence Design Systems, Inc..

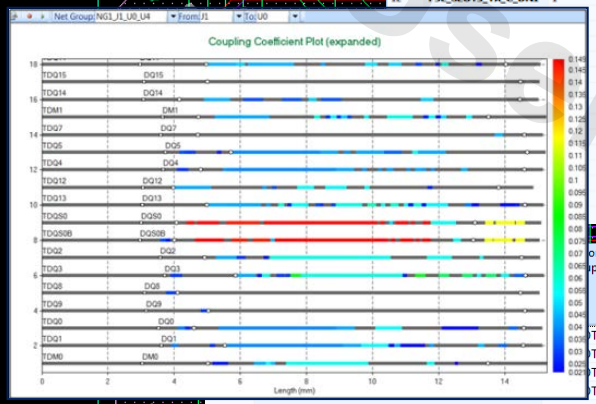
OrCAD™
CADENCE PCB SOLUTIONS

OrCAD Sigrity ERC Flow



File Edit View Display Setup Shape Logic Place Route Analyze Tools Help

Net count	Net name	No. of segments without reference	No. of trace reference discontinuities	No. of vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)	Dominant Impedance (Ohm)
1	P3E_SLOT2_TX_C_DN0	1	3	2	144.946	56.449	56.449
2	P3E_SLOT2_TX_C_DN1	1	3	2	144.946	56.449	56.449
3	P3E_SLOT2_TX_C_DN2	1	3	2	144.946	56.449	56.449
4	P3E_SLOT2_TX_C_DN3	1	3	2	153.005	63.836	63.836
5	P3E_SLOT2_TX_C_DN4	1	1	2	63.836	63.836	63.836
6	P3E_SLOT2_TX_C_DP0	1	3	2	144.946	56.449	56.449
7	P3E_SLOT2_TX_C_DP1	1	3	2	144.946	56.449	56.449
8	P3E_SLOT2_TX_C_DP2	1	3	2	144.946	56.449	56.449
9	P3E_SLOT2_TX_C_DP3	1	3	2	153.005	63.836	63.836
10	P3E_SLOT2_TX_C_DP4	1	1	2	63.836	63.836	63.836
11	P3E_SLOT3_TX_C_DN0	1	1	1	56.449	56.449	56.449
12	P3E_SLOT3_TX_C_DN1	1	1	1	56.449	56.449	56.449



			Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
		T2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
		T2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
		T2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
		T2_TX_C_DN2	0.125%	36.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.125%	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

Trace Impedance / return path

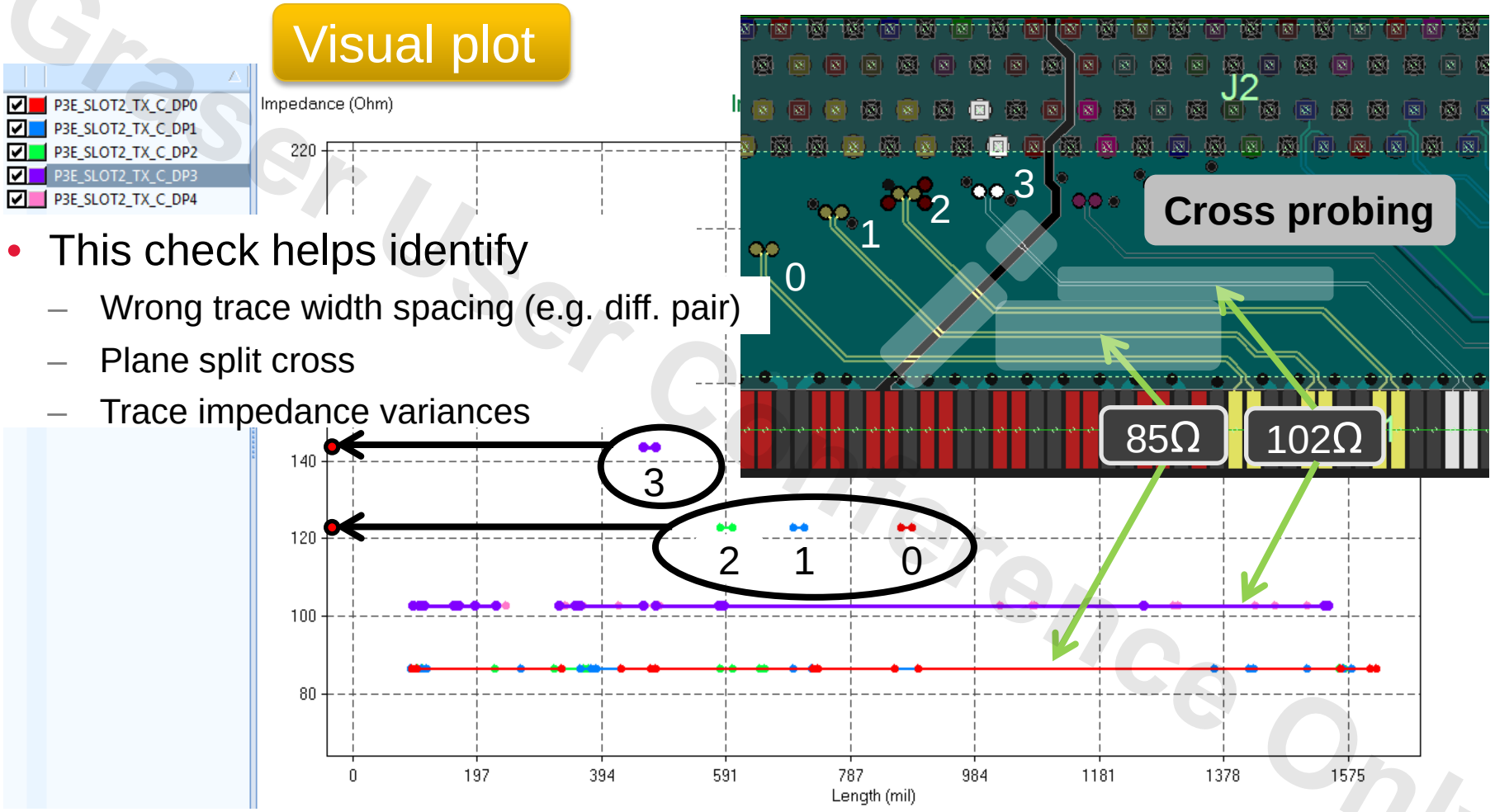
Coupling / metrics

Design modification

© 2014 Cadence Design Systems, Inc.

OrCAD CADENCE PCB SOLUTIONS

Trace Impedance Check



- This check helps identify
  - Wrong trace width spacing (e.g. diff. pair)
  - Plane split cross
  - Trace impedance variances
- Visually or tabular results for trace impedance check shows trace segment(s) mismatch vs. target impedance

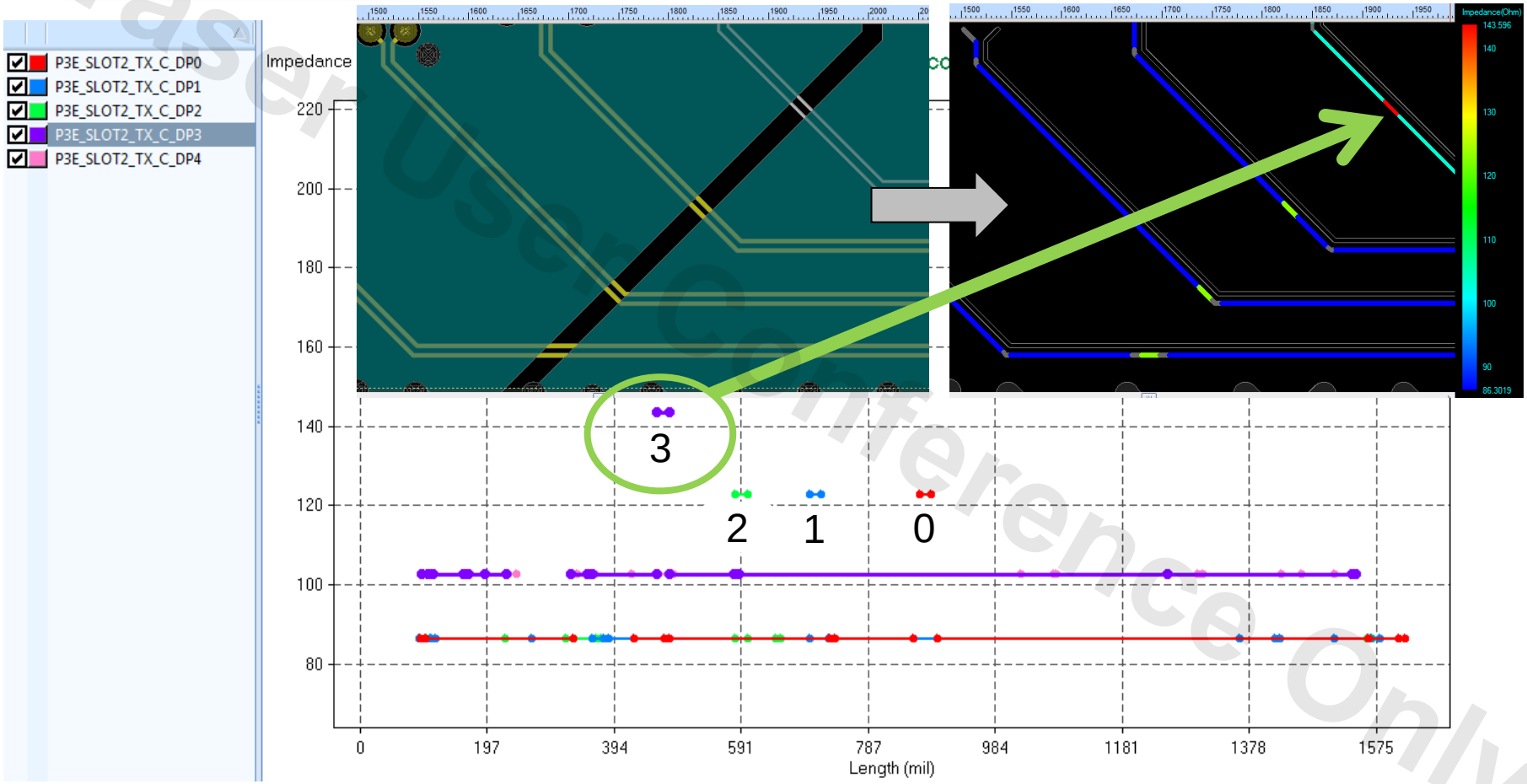
Cadence User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD CADENCE PCB SOLUTIONS

Trace Impedance Check

Cross Probing



- Cross probing allows issues to be quickly identified

Cadence User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS

Trace Impedance Check

Tabular Results

Net count	Net name	No. of segments without reference	No. of trace reference discontinuities	No. of vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)	Dominant Impedance (Ohm)	Dominant Imp Length (%)	Trace total length (mil)	Trace delay(ns)
1	P3E_SLOT2_TX_C_DN0	1	3	2	144.946	56.449	56.449	92.921	1633.158	0.233
2	P3E_SLOT2_TX_C_DN1	1	3	2	144.946	56.449	56.449	93.168	1583.722	0.225
3	P3E_SLOT2_TX_C_DN2	1	3	2	144.946	56.449	56.449	93.186	1575.168	0.224
4	P3E_SLOT2_TX_C_DN3	1	3	2	153.005	63.836	63.836	93.074	1549.678	0.220
5	P3E_SLOT2_TX_C_DN4	1	1	2	63.836	63.836	63.836	94.228	1513.121	0.214
6	P3E_SLOT2_TX_C_DP0	1	3	2	144.946	56.449	56.449	92.923	1633.643	0.233
7	P3E_SLOT2_TX_C_DP1	1	3	2	144.946	56.449	56.449	93.221	1583.404	0.225
8	P3E_SLOT2_TX_C_DP2	1	3	2	144.946	56.449	56.449	93.184	1574.865	0.224
9	P3E_SLOT2_TX_C_DP3	1	3	2	153.005	63.836	63.836	93.059	1546.528	0.219
10	P3E_SLOT2_TX_C_DP4	1	1	2	63.836	63.836	63.836	94.221	1511.225	0.214
11	P3E_SLOT3_TX_C_DN0	1	1	1	56.449	56.449	56.449	94.142	1490.958	0.211
										0.208
										0.217
										0.209
										0.225
										0.214
										0.203
										0.212
										0.212
										0.209
										0.217
										0.210
										0.225
										0.214
										0.203
										0.212

- Cross plane split?
- Any trace segment mismatch? Cross plane split?
- Too much breakout neck length?
- Too much MS/SL routing difference in a group?
- The same trace length means the same trace delay?
- Routing on MS/SL has different trace delay.

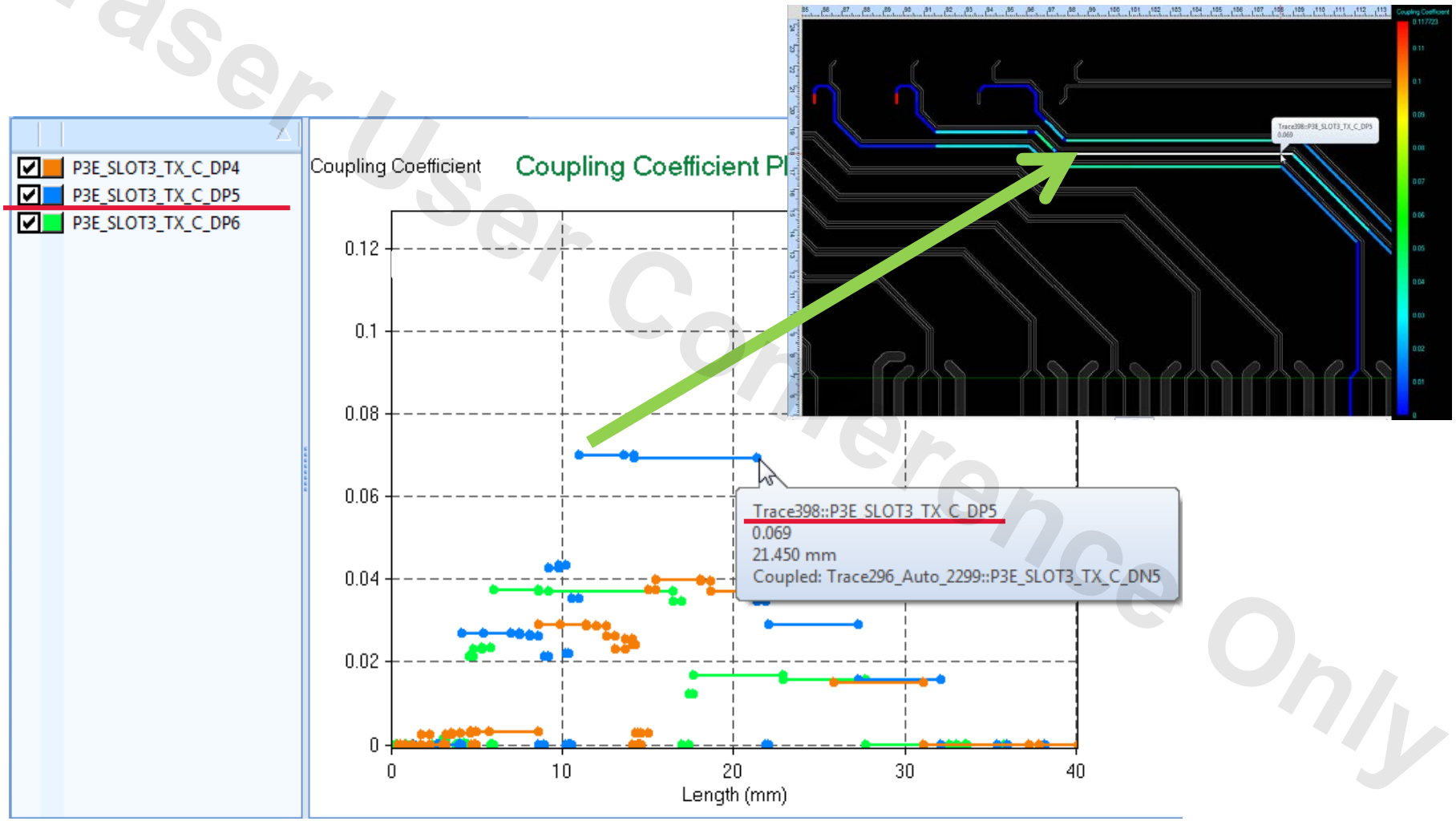
Cadence User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD CADENCE PCB SOLUTIONS

Trace Coupling Check

Cross probing helps to easily resolve issues



Cadence User Conference Only

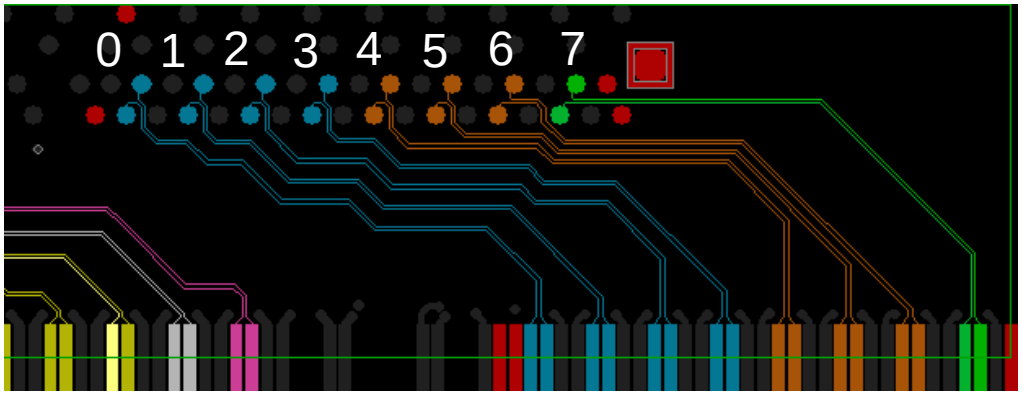
© 2014 Cadence Design Systems, Inc..

OrCAD
CADENCE PCB SOLUTIONS

Trace Coupling Check

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef >0.05	% length with coupling coef 0.001~0.05	Total coupling index (mm-%)
1	P3E_SLOT2_TX_C_DP0-P3E_SLOT2_TX_C_DN0	P3E_SLOT2_TX_C_DP1	0.163%	40.183	----	40.183	2.605
2	P3E_SLOT2_TX_C_DP1-P3E_SLOT2_TX_C_DN1	P3E_SLOT2_TX_C_DP2	0.573%	1.132	----	43.513	2.941
3	P3E_SLOT2_TX_C_DP2-P3E_SLOT2_TX_C_DN2	P3E_SLOT2_TX_C_DN1	0.573%	1.138	----	34.387	2.668
4	P3E_SLOT2_TX_C_DP3-P3E_SLOT2_TX_C_DN3	P3E_SLOT2_TX_C_DN2	0.125%	6.798	----	15.328	2.177
5	P3E_SLOT2_TX_C_DP4-P3E_SLOT2_TX_C_DN4	P3E_SLOT2_TX_C_DN3	0.125%	15.686	----	15.686	0.754
6	P3E_SLOT3_TX_C_DP0-P3E_SLOT3_TX_C_DN0	P3E_SLOT3_TX_C_DP1	0.156%	45.886	----	45.886	2.881
7	P3E_SLOT3_TX_C_DP1-P3E_SLOT3_TX_C_DN1	P3E_SLOT3_TX_C_DN0	0.147%	46.545	----	56.715	3.440
8	P3E_SLOT3_TX_C_DP2-P3E_SLOT3_TX_C_DN2	P3E_SLOT3_TX_C_DN1	0.156%	42.769	----	71.100	4.302
9	P3E_SLOT3_TX_C_DP3-P3E_SLOT3_TX_C_DN3	P3E_SLOT3_TX_C_DN2	0.156%	55.397	----	60.345	3.541
10	P3E_SLOT3_TX_C_DP4-P3E_SLOT3_TX_C_DN4	P3E_SLOT3_TX_C_DP5	2.808%	26.979	----	68.281	47.643
11	P3E_SLOT3_TX_C_DP5-P3E_SLOT3_TX_C_DN5	P3E_SLOT3_TX_C_DN4	2.810%	28.293	----	71.503	54.733
12	P3E_SLOT3_TX_C_DP6-P3E_SLOT3_TX_C_DN6	P3E_SLOT3_TX_C_DN5	2.810%	30.093	----	62.280	45.025
13	P3E_SLOT3_TX_C_DP7-P3E_SLOT3_TX_C_DN7	----	----	----	----	----	----

18X



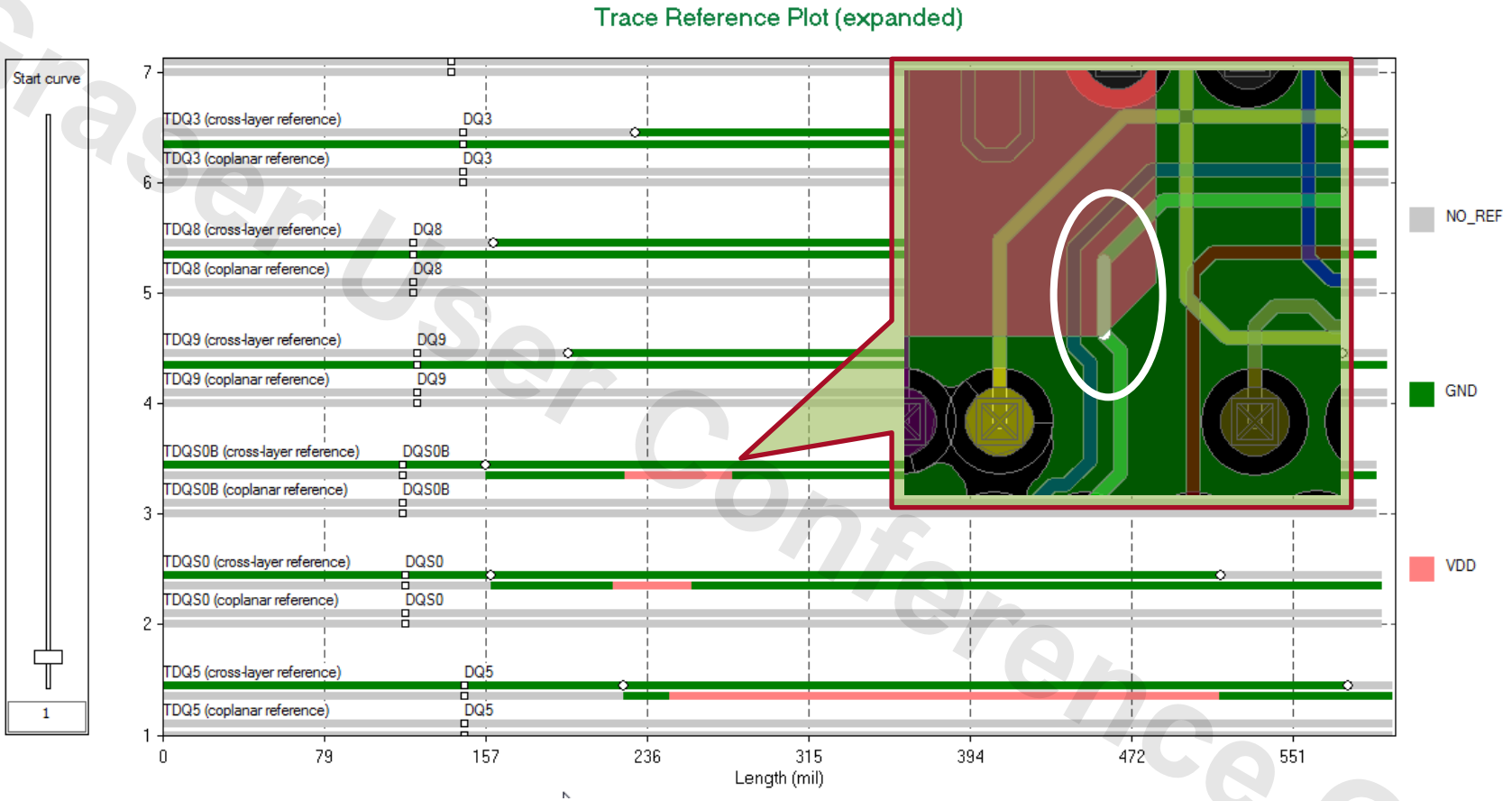
- Tight coupling pairs
- Max coupling aggressor
- Dangerous vs. safe coupling
  → **18X** (= 2.81% / 0.156%)

Cadence Confidential Only

© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS

Trace Reference Check



- Trace cross layer reference shows the net names for the reference plane shapes directly above and below the corresponding trace segment
- Trace coplanar reference shows the net names for the reference plane shapes next to the corresponding trace segment on the same layer

Grasser User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD™ CADENCE PCB SOLUTIONS

Summary / Benefits

- ERCs are better than DRCs for signal quality validation
  - Identify issues geometry-based DRCs miss
- OrCAD Sigrity ERC specifically designed for PCB designers leveraging industry-leading Cadence Sigrity technology
  - Easy to use, minimal setup
  - Cross-probing
- Actionable results to identify and quickly address signal quality issues

Grasper User Conference Only

© 2014 Cadence Design Systems, Inc..

OrCAD™
CADENCE PCB SOLUTIONS

Graser User Conference Only

OrCAD™

CADENCE PCB SOLUTIONS

©2014 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, Sigrity, and OrCAD are registered trademarks and the OrCAD logo is a trademark of Cadence Design Systems, Inc. in the United States and other countries. All other trademarks are the property of their respective owners.