

USER
CONFERENCE
Graser®

2014 Oct³¹
Taipei

OrCAD New Option Feature

Addi Lin / Graser

31/Oct/2014

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Topics

- OrCAD Library Builder
- Engineering Data Management
- OrCAD Documentation Editor

OrCAD Library Builder

Questions and Concerns

- Describe your part building process
 - Librarian, engineering
- Are your engineers / designers responsible for creating their own new parts?
- Have your librarian resources kept up with your engineering and designer resources?
- How easy is it for your librarians or engineers / designers to build parts? Adhere to corporate or industry standards?
- Have you ever encountered a project or schedule delay because of a part error? What was the cost?
- Bandwidth issues for peak demand?

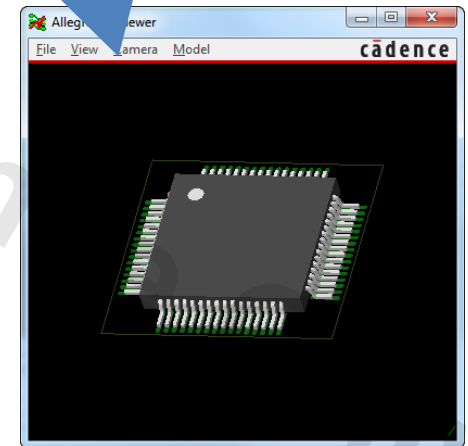
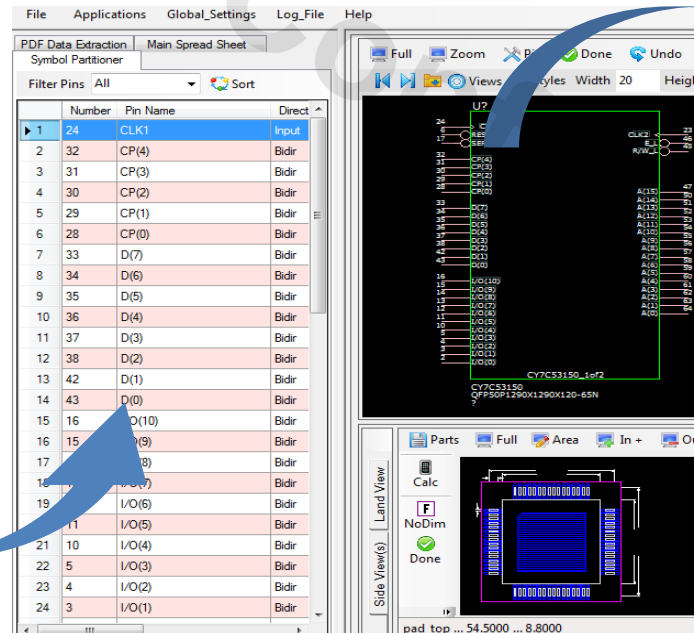
OrCAD Library Builder

- OrCAD® Library Builder is an advanced, automated part generation solution for schematic symbols and PCB footprints. It provides intelligent and highly automated capabilities for quickly creating part symbols and footprints for OrCAD PCB schematics and layouts. It substantially reduces the time needed and virtually eliminates errors associated with traditional manual processes; creating accurate component libraries in a fraction of the time.

Part Datasheet

Pin Descriptions

| Pin Name | I/O | Pin Function | CYT63150 TQFP-64 Pin No. | CYT63120xx SOIC-32 Pin No. | CYT63120xx TQFP-44 Pin No. |
|------------|-------------------------------------|--|-----------------------------|-------------------------------|-------------------------------|
| CLK1 | Input | Oscillator connection or external clock input. | 24 | 15 | 15 |
| CLK2 | Output | Oscillator connection. Leave open when external clock is input to CLK1. Maximum of one external load. | 23 | 14 | 14 |
| RESET | I/O (Built-In Pull up) | Reset pin (active LOW). Note The allowable external capacitance connected to the RESET pin is 100-1000 pF. | 6 | 1 | 40 |
| SERVICE | I/O (Built-In Configurable Pull up) | Service pin (active LOW). Alternates between input and output at a 75-Hz rate. | 17 | 8 | 5 |
| I/O0-I/O3 | I/O | Large current-sink capacity (20 mA). General I/O port. The output of timer/counter 1 may be routed to I/O0. The output of Timer/Counter 2 may be routed to I/O1. | 2, 3, 4, 5 | 7, 6, 5, 4 | 4, 3, 2, 43 |
| I/O4-I/O7 | I/O (Built-In Configurable Pull up) | General I/O port. The input to Timer/Counter 1 may be derived from one of I/O4-I/O7. The input to Timer/Counter 2 may be derived from I/O4. | 10, 11, 12, 13 | 3, 30, 29, 28 | 42, 36, 35, 32 |
| I/O8-I/O10 | I/O | General I/O port. May be used for serial communication under firmware control. | 14, 15, 16 | 27, 26, 24 | 31, 30, 27 |
| I/O-D7 | I/O | Bidirectional memory data bus. | 43, 42, 38, 37 | N/A | N/A |



3D-Setup

Symbol / Footprint Builder

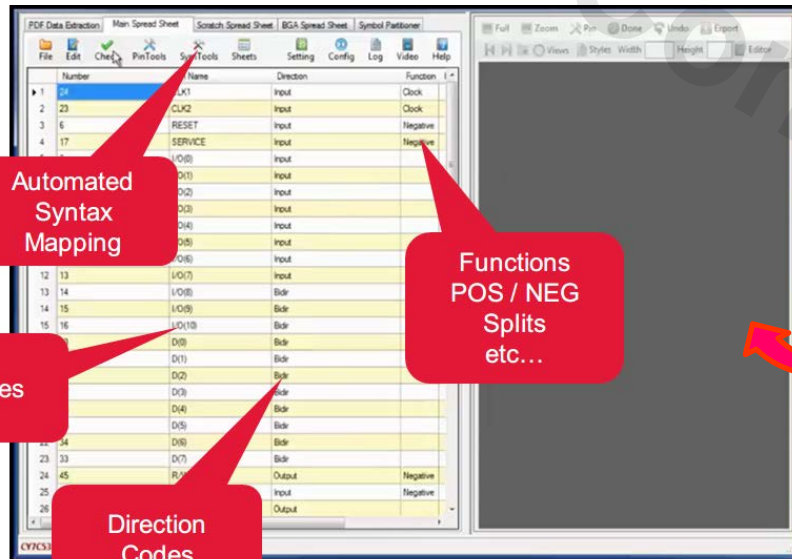
Why is Any of This Important?

- Libraries are the building blocks for every PCB design; everyone needs them and they are never finished.
- Part complexities are increasing, higher pin-count devices are more common, and corporate / industry standards are more critical than ever.
- In many parts of the world, the number of formal Librarians is not keeping pace with the number of electrical engineers and PCB designers.
- Since parts and libraries are the basis for every PCB design, errors can be extremely costly and time consuming.
- Optimizing part and library creation boosts productivity, saves time, and enables reuse opportunities.

PDF Extraction

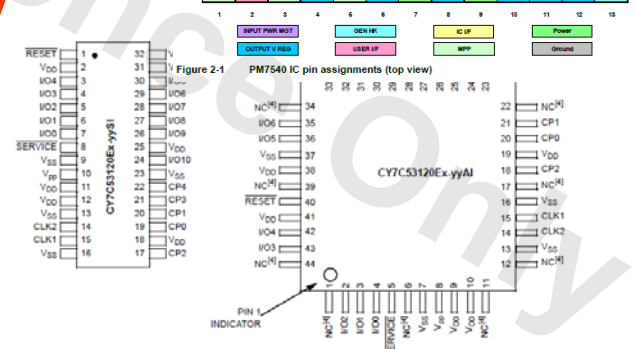
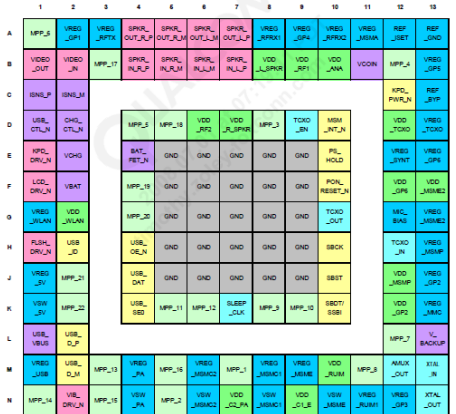
Intelligent PDF datasheets extraction

- Direct datasheet extraction
- Spreadsheet import / manipulation
- Checks and verification



Pin Descriptions

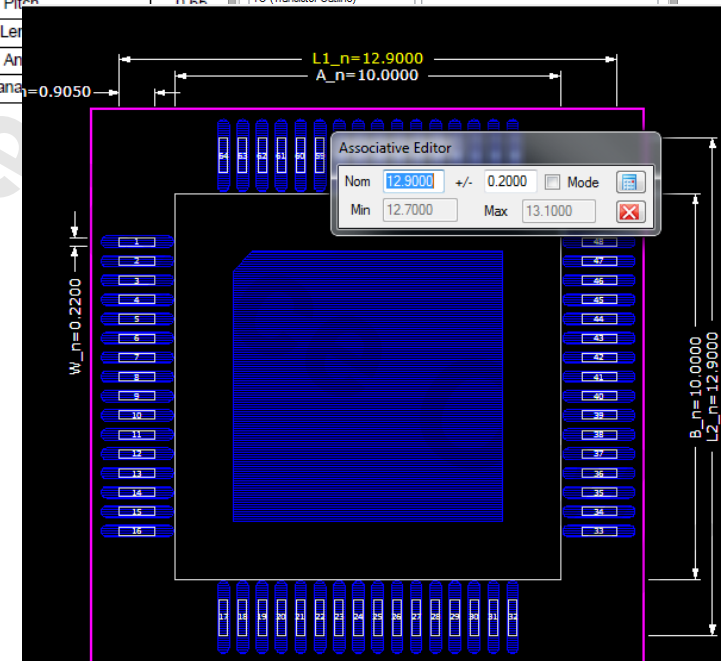
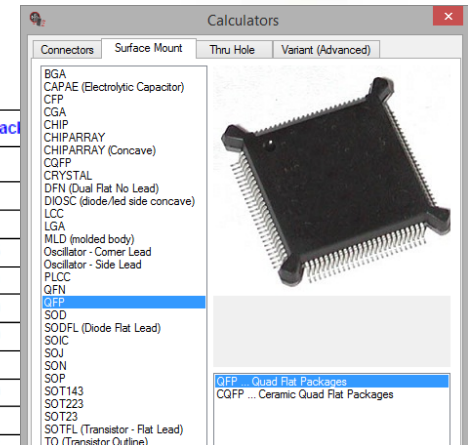
| Pin Name | I/O | Pin Function | CY7C53150 TQFP-44 Pin No. | CY7C53120xx SOIC-32 Pin No. | CY7C53120xx TQFP-44 Pin No. |
|-----------------|--------------------------------------|--|------------------------------|--------------------------------|--------------------------------|
| CLK1 | Input | Oscillator connection or external clock input. | 24 | 15 | 15 |
| CLK2 | Output | Oscillator connection. Leave open when external clock is input to CLK1. Maximum of one external load. | 23 | 14 | 14 |
| RESET | I/O (Built-In Pull up) | Reset pin (active LOW). Note: The allowable external capacitance connected to the RESET pin is 100–1000 pF. | 6 | 1 | 40 |
| SERVICE | I/O (Built-In Configurable Pull up) | Service pin (active LOW). Alternates between input and output at a 76-Hz rate. | 17 | 8 | 5 |
| IO0–IO3 | I/O | Large current-sink capacity (20 mA). General I/O port. The output of timer/counter 1 may be routed to I/O0. The output of Timer/Counter 2 may be routed to I/O1. | 2, 3, 4, 5 | 7, 6, 5, 4 | 4, 3, 2, 43 |
| IO4–IO7 | I/O (Built-In Configurable Pull ups) | General I/O port. The Timer/Counter 1 may be routed to I/O4–IO7. The input may be derived from I/O. | | | |
| IO8–IO10 | I/O | General I/O port. May communicate under I/O. | | | |
| D0–D7 | I/O | Bidirectional memory | | | |
| R/R | Output | Read/write control or memory. | | | |
| E | Output | Enable clock control or memory. | | | |
| A0–A15 | Output | Memory address out | | | |
| V _{DD} | Input | Power input (5 V nom) be connected together. | | | |
| V _{SS} | Input | Power input (0 V GND) be connected together. | | | |
| V _{PP} | Input | In-circuit test mode only when RESET is asserted and data buses become | | | |
| CP0–CP4 | Communication Network Interface | Bidirectional port sup- ports in three mode | | | |
| NC | — | No connect. Must not be user's PC board, since connected internal to | | | |



Accurate Footprints

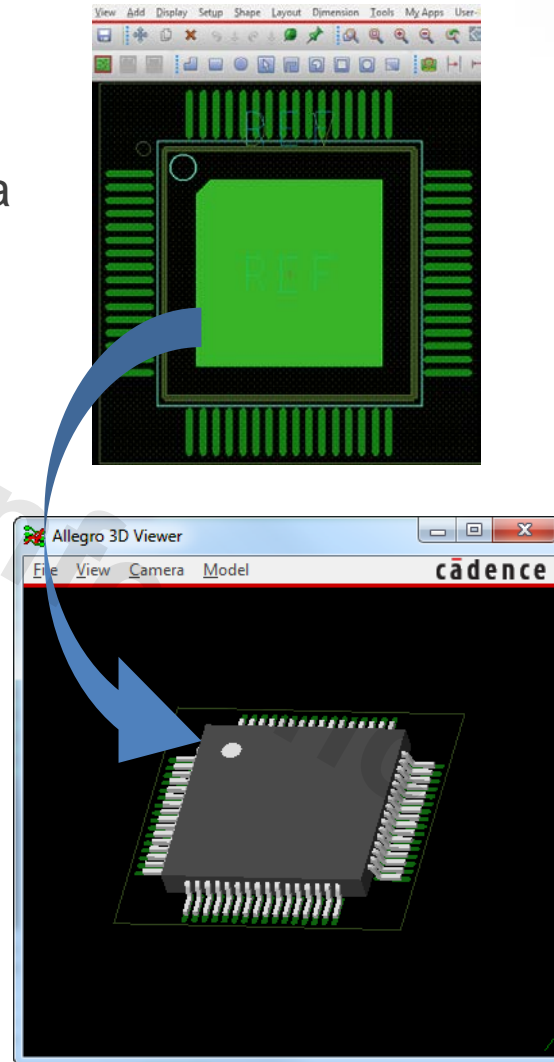
- Calculator-style interface for complex PCB footprint creation
 - Comprehensive library of footprints
 - Simple calculator-based interface
 - Associative editing enables quick on the fly adjustments
 - Extensive pad support

| Quad Flatpack | | |
|----------------|--------------------|------|
| Symbol | Description | Min |
| N | Lead Count | |
| A | Overall Height | |
| A ₁ | Stand Off | 0.05 |
| b | Lead Width | 0.20 |
| c | Lead Thickness | 0.10 |
| D | Terminal Dimension | 12.0 |
| D ₁ | Package Body | |
| E | Terminal Dimension | 12.0 |
| E ₁ | Package Body | |
| e ₁ | Lead Pitch | 0.65 |
| L ₁ | Foot Length | |
| T | Lead Angle | |
| Y | Coplanarity | |



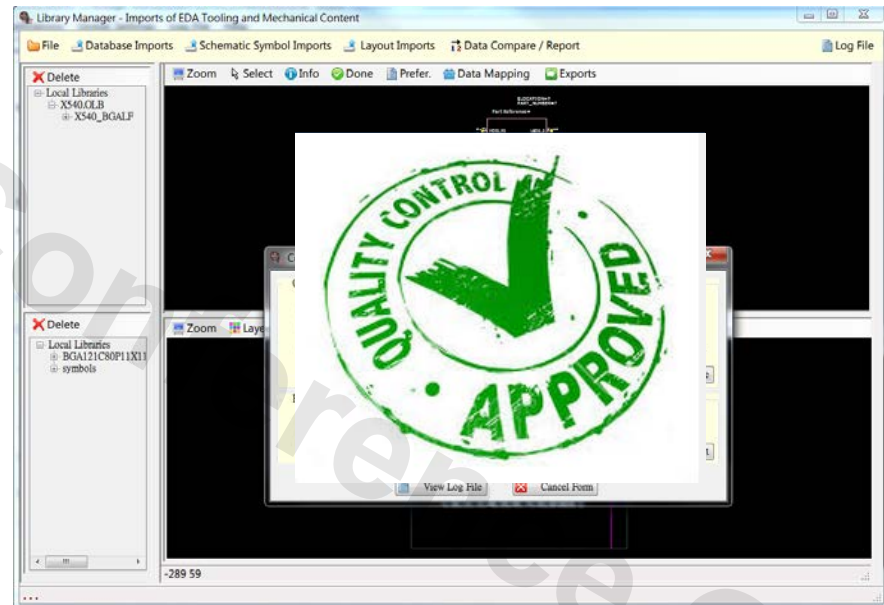
3D Model Creation

- STEP models
 - Accurate 3D STEP models
 - Derived directly from the footprint data
 - Three click process



Automated Error Checking

- Comprehensive checks and
 - Checks done throughout creation process
 - Symbol and footprint DRCs
 - Symbol-footprint validation
- valuable
 - Ensure symbols and footprints are correct
 - Eliminate library part errors
 - Ensure symbol-footprint association



...Symbol: SYM_DS ...Package: BGA_for_DS (BGA)

File Applications Global_Settings Log_File Help

PDF Data Extraction Main Spread Sheet Symbol Partitioner

Filter Pins: [All] Sort [] Sel/Drop [] Done [] Left [] Right [] Top [] Bot [] Tool []

| Number | Pin Name | Direction | Function | Pin Group | Position | Section | Grid | Swap |
|--------|----------|----------------------------------|----------|-----------|----------|---------|------|------|
| 1 | L8 | COM0 | Output | Right | 1 | 2 | | |
| 2 | J9 | LCDCAPI/R33 | Bidr | Left | 1 | 9 | | |
| 3 | C11 | P1.0/TA0/OA0RFB | Bidr | Left | 1 | 11 | | |
| 4 | C12 | P1.1/TA0/MCLK/OA1RFB | Bidr | Left | 1 | 12 | | |
| 5 | D11 | P1.2/TA1/A4_/OA0I3SW0C | Bidr | Left | 1 | 13 | | |
| 6 | D12 | P1.3/TB0UTH/SVSOUT/A4+/OA1I3SW1C | Bidr | Left | 1 | 14 | | |
| 7 | E11 | P1.4/TBCLK/SMCLK/A3-/OA1I0DAC1 | Bidr | Left | 1 | 15 | | |
| 8 | F11 | P1.5/TACLK/ACLK/A3+ | Bidr | Left | 1 | 16 | | |
| 9 | G12 | P1.6/CA0/A2-/OA0I0DAC0 | Bidr | Left | 1 | 17 | | |
| 10 | G11 | P1.7/CA1/A2+ | Bidr | Left | 1 | 18 | | |
| 11 | C3 | P2.0/TA2/S1_2 | Bidr | Left | 1 | 20 | | |
| 12 | C2 | P2.0/TA2/S1_1 | Bidr | Left | 1 | 21 | | |
| 13 | C1 | P2.1/TB0/S0 | Bidr | Left | 1 | 22 | | |
| 14 | L5 | P5.0/S20 | Bidr | Left | 1 | 24 | | |
| 15 | M5 | P5.1/S21 | Bidr | Left | 1 | 25 | | |
| 16 | M8 | P5.2/COM1 | Bidr | Left | 1 | 26 | | |
| 17 | L9 | P5.3/COM2 | Bidr | Left | 1 | 27 | | |
| 18 | M9 | P5.4/COM3 | Bidr | Left | 1 | 28 | | |
| 19 | M10 | P5.5/R23 | Bidr | Left | 1 | 29 | | |
| 20 | L10 | P5.6/LCDREF/R13 | Bidr | Left | 1 | 30 | | |
| 21 | M11 | P5.7/R03 | Bidr | Left | 1 | 31 | | |
| 22 | B8 | P6.0/A0-/OA00 | Bidr | Left | 1 | 32 | | |
| 23 | B9 | P6.1/A0-/OA0FB | Bidr | Left | 1 | 33 | | |
| 24 | A9 | P6.2/OA0I1SW0A | Bidr | Left | 1 | 34 | | |
| 25 | D9 | P6.3/A1-/OA10 | Bidr | Left | 1 | 35 | | |
| 26 | A10 | P6.4/A1-/OA1FB | Bidr | Left | 1 | 36 | | |
| 27 | B10 | P6.5/OA0I2SW0B | Bidr | Left | 1 | 37 | | |
| 28 | A11 | P6.6/OA1I1SW1A | Bidr | Left | 1 | 38 | | |
| 29 | B12 | P6.7/OA1I2/SVSINISW1B | Bidr | Left | 1 | 39 | | |
| 30 | B5 | RST/NMI | Input | Left | 1 | 3 | | |
| 31 | M7 | S25 | Output | Right | 1 | 4 | | |
| 32 | L7 | S24 | Output | Right | 1 | 5 | | |
| 33 | M6 | S23 | Output | Right | 1 | 6 | | |
| 34 | L6 | S22 | Output | Right | 1 | 7 | | |
| 35 | J4 | S19 | Output | Right | 1 | 8 | | |
| 36 | M4 | S18 | Output | Right | 1 | 9 | | |
| 37 | L4 | S17 | Output | Right | 1 | 10 | | |
| 38 | L3 | S16 | Output | Right | 1 | 11 | | |
| 39 | M3 | S15 | Output | Right | 1 | 12 | | |
| 40 | M2 | S14 | Output | Right | 1 | 13 | | |

U?

B7 TDO/TDI
B5 RST/NMI
A5 TCK
A6 TDI/TCLK
B6 TMS
E1 XIN
A7 XT2IN
J9 LCDCAPI/R33

C11 P1.0/TA0/OA0RFB
C12 P1.1/TA0/MCLK/OA1RFB
D11 P1.2/TA1/A4_/OA0I3SW0C
D12 P1.3/TB0UTH/SVSOUT/A4+/OA1I3SW1C
E11 P1.4/TBCLK/SMCLK/A3-/OA1I0DAC1
F11 P1.5/TACLK/ACLK/A3+
G12 P1.6/CA0/A2-/OA0I0DAC0
G11 P1.7/CA1/A2+

C3 P2.0/TA2/S1_2
C2 P2.0/TA2/S1_1
C1 P2.1/TB0/S0

COM0 L8
M7
S25 L7
S24 M6
S23 L6
S22 J4
S19 M4
S18 L4
S17 L3
S16 M3
S15 M2
S14 M1
S13 L1
S12

VREF A12
XOUT F1
XT2OUT A8

Parts Full Area In + Out - Layer Info PinTool PadTool Exports

Calc
NoDim
CompD
LandD
Dimen1
Dimen2
Done
Grid
Pref.

A_n=11.0000
B_n=11.0000
pad_top=-10.7600... 5.6900

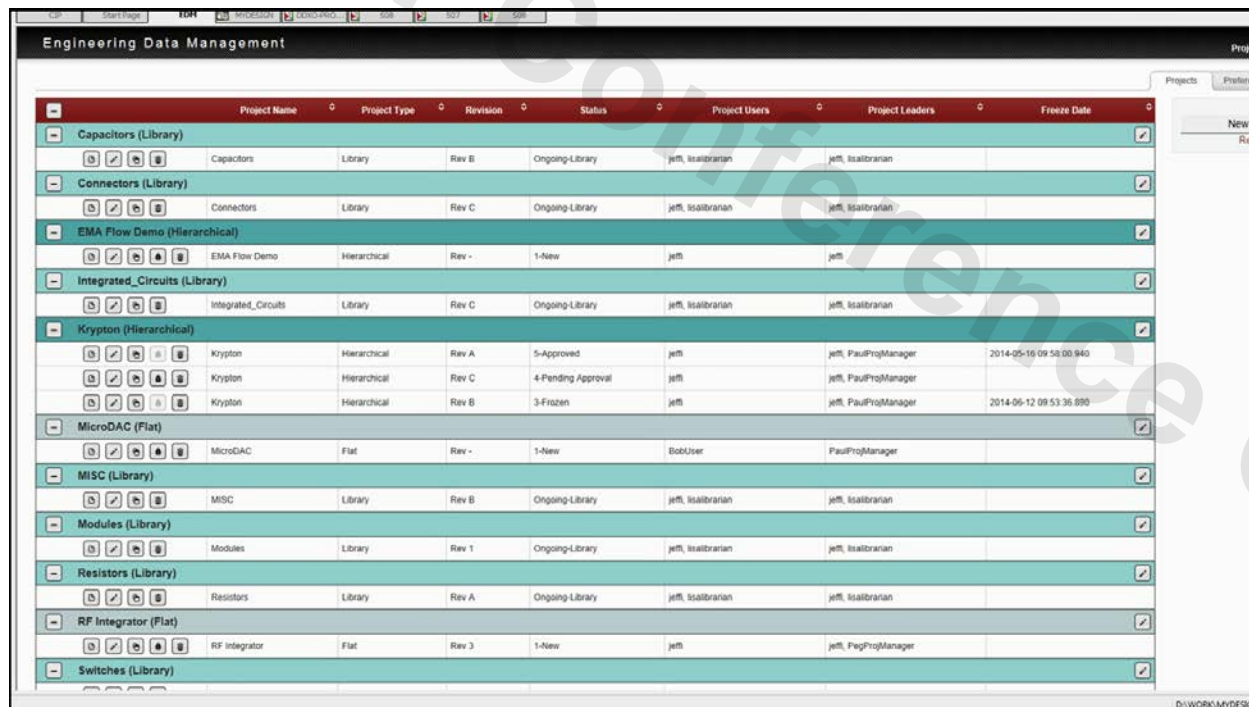
Engineering Data Management

Questions and Concerns

- Lost designers' productivity and/or design process efficiency
- Design team's confusion, miscommunication, and errors
- Project or schedule is delayed due to design mismanagement

Engineering Data Management

- OrCAD® Engineering Data Management (EDM) is a comprehensive collaboration, design and data management environment for the OrCAD Capture PCB schematic solution. It is fully integrated within the OrCAD Capture environment and lets your engineering design team take advantage of benefits gained from effective collaboration and design data management.



The screenshot displays the OrCAD Engineering Data Management (EDM) interface. The main window shows a table with columns for Project Name, Project Type, Revision, Status, Project Users, Project Leaders, and Freeze Date. The table is organized into sections for different project types, such as Capacitors (Library), Connectors (Library), EMA Flow Demo (Hierarchical), Integrated_Circuits (Library), Krypton (Hierarchical), MicroDAC (Flat), MISC (Library), Modules (Library), Resistors (Library), RF Integrator (Flat), and Switches (Library). Each section contains a list of projects with their respective details.

| Project Name | Project Type | Revision | Status | Project Users | Project Leaders | Freeze Date |
|--------------------------------------|--------------|----------|--------------------|------------------|-----------------------|-------------------------|
| Capacitors (Library) | | | | | | |
| Capacitors | Library | Rev B | Ongoing-Library | jeff, tsalbranan | jeff, tsalbranan | |
| Connectors (Library) | | | | | | |
| Connectors | Library | Rev C | Ongoing-Library | jeff, tsalbranan | jeff, tsalbranan | |
| EMA Flow Demo (Hierarchical) | | | | | | |
| EMA Flow Demo | Hierarchical | Rev - | 1-New | jeff | jeff | |
| Integrated_Circuits (Library) | | | | | | |
| Integrated_Circuits | Library | Rev C | Ongoing-Library | jeff, tsalbranan | jeff, tsalbranan | |
| Krypton (Hierarchical) | | | | | | |
| Krypton | Hierarchical | Rev A | 5-Approved | jeff | jeff, PaulProjManager | 2014-05-16 09:56:00 940 |
| Krypton | Hierarchical | Rev C | 4-Pending Approval | jeff | jeff, PaulProjManager | |
| Krypton | Hierarchical | Rev B | 3-Frozen | jeff | jeff, PaulProjManager | 2014-06-12 09:53:36 890 |
| MicroDAC (Flat) | | | | | | |
| MicroDAC | Flat | Rev - | 1-New | BobUser | PaulProjManager | |
| MISC (Library) | | | | | | |
| MISC | Library | Rev B | Ongoing-Library | jeff, tsalbranan | jeff, tsalbranan | |
| Modules (Library) | | | | | | |
| Modules | Library | Rev 1 | Ongoing-Library | jeff, tsalbranan | jeff, tsalbranan | |
| Resistors (Library) | | | | | | |
| Resistors | Library | Rev A | Ongoing-Library | jeff, tsalbranan | jeff, tsalbranan | |
| RF Integrator (Flat) | | | | | | |
| RF Integrator | Flat | Rev 3 | 1-New | jeff | jeff, PaulProjManager | |
| Switches (Library) | | | | | | |

Project-level/Library Management

Projects

Status

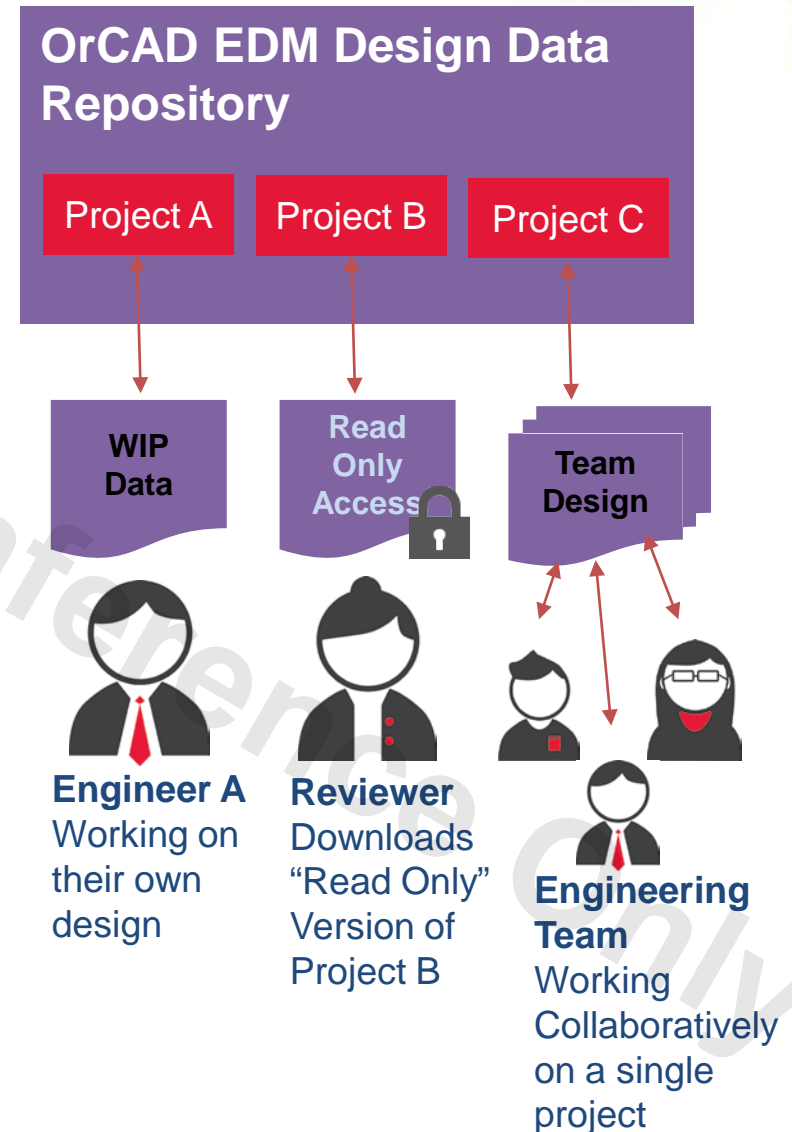
Engineering Data Management

| Project Name | Revision | Status |
|-------------------------------|----------|--------------------|
| Capacitors (Library) | Rev B | Ongoing-Library |
| Connectors (Library) | Rev C | Ongoing-Library |
| EMA Flow Demo (Hierarchical) | Rev - | 1-New |
| Integrated_Circuits (Library) | Rev C | Ongoing-Library |
| Krypton (Hierarchical) | Rev C | 4-Pending Approval |
| MISC (Library) | Rev B | Ongoing-Library |
| Modules (Library) | Rev 1 | Ongoing-Library |
| Resistors (Library) | Rev A | Ongoing-Library |
| RF Integrator (Flat) | Rev 3 | 1-New |
| Switches (Library) | Rev 2 | Ongoing-Library |
| Transistors (Library) | Rev C | Ongoing-Library |
| XTALS (Library) | Rev A | Ongoing-Library |

Revision

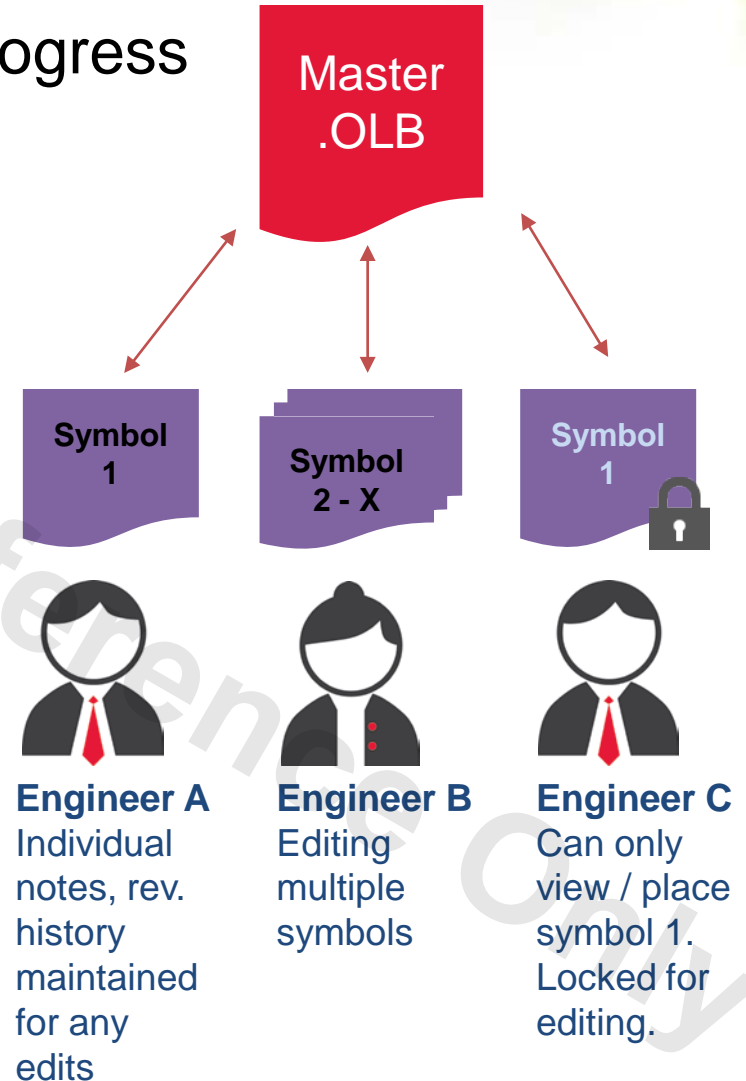
Project-level Management

- The ability to manage and track
 - Dashboard with real-time updates
 - Full revision history
 - Quick project access inside Capture



Library Management

- The ability to manage and track progress
 - Create, edit, review, promote
 - Dashboard with real-time updates
 - Full revision history
 - Quick part(s) access inside Capture



Page-level Management

USER
CONFERENCE
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Tappi

Pages

Users

History

Being Edited
and By Whom

Check-in /
Check-out

Status

| Page Name | Status | Assigned Users | Locked | Date Locked | Lock for Edit | Download | History |
|-------------------------------|----------|------------------------|--------|-------------------------|--------------------------|--------------------------|---------|
| DXO-PROxx_Top_Blk_Diagram | | | | | | | |
| DXO-PROxx_Top_Blk_Diagram | Working | jeffl, PaulProjManager | jeffl | 2014-07-22 20:24:15.497 | <input type="checkbox"/> | <input type="checkbox"/> | |
| P430F5529_TOP_Block | | | | | | | |
| MSP430F5529_TOP_Block | Approved | jeffl, PaulProjManager | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P05/MSP430F5529_GPIO_Ports1-4 | | | | | | | |
| MSP430F5529_GPIO_Ports1-4 | Working | BobUser | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P04/MSP430F5529_GPIO_Ports5-8 | | | | | | | |
| MSP430F5529_GPIO_Ports5-8 | Approved | BobUser | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P05/MSP430F5529_USB/Test | | | | | | | |
| MSP430F5529_USB/Test | 1-New | JohnUser | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P06/MSP430F5529_Power | | | | | | | |
| MSP430F5529_Power | Approved | JohnUser | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P07/Clock_Pre-Scalar_1 | | | | | | | |
| Clock_Pre-scalar_1 | Working | jeffl | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P08/Clock_Pre-Scalar_2 | | | | | | | |
| Clock_Pre-Scalar_2 | Working | jeffl | jeffl | 2014-07-22 20:24:15.500 | <input type="checkbox"/> | <input type="checkbox"/> | |
| P09/Clock_Pre-Scalar_3 | | | | | | | |
| Clock_Pre-Scalar_3 | Approved | jeffl | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P10/Clock_Pre-Scalar_4 | | | | | | | |
| Clock_Pre-Scalar_4 | Approved | jeffl | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P11/TSic-716_Temp_Sensor | | | | | | | |
| TSic-716_Temp_Sensor | Approved | BobUser | | | <input type="checkbox"/> | <input type="checkbox"/> | |
| P12/FPGA_Controller_Block | | | | | | | |
| FPGA_Block_Diagram | Approved | BobUser | | | <input type="checkbox"/> | <input type="checkbox"/> | |

Actions

- ☒ Download
- ☐ Upload
- ☐ Remove Lock

Download

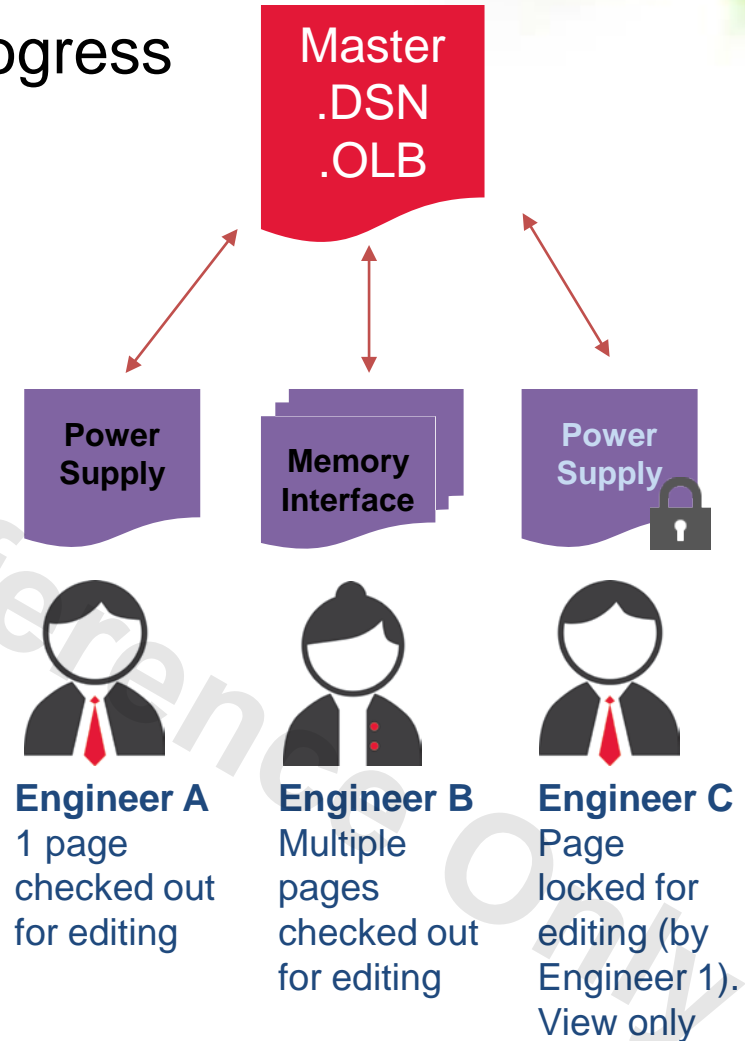
Refresh

Project Hierarchy

Page-level/Library Management

- The ability to manage and track progress
 - Dashboard with real-time updates
 - Full revision history
 - Quick page(s) access inside Capture

| Page Name | Status | Assigned Users | Locked | Date Locked | Lock for Edit | Download | History |
|---------------------------|----------|---------------------|--------|-------------------------|---------------|----------|---------|
| DXO-PROxx_Tap_Blk_Diagram | Working | jff, PaulHighmanger | jff | 2014-07-22 20:24:15:487 | | | |
| SP430F5529_TOP_Block | Approved | jff, PaulHighmanger | | | | | |
| SP430F5529_TOP_Block | Working | BalChen | | | | | |
| SP430F5529_GPIO_Ports1-4 | Working | BalChen | | | | | |
| SP430F5529_GPIO_Ports5-8 | Approved | BalChen | | | | | |
| SP430F5529_GPIO_Ports8 | Approved | BalChen | | | | | |
| P05MSP430F5529_USD/Test | 1-New | jff | | | | | |
| SP430F5529_USD/Test | Approved | jff | | | | | |
| P06MSP430F5529_Power | Approved | jff | | | | | |
| SP430F5529_Power | Approved | jff | | | | | |
| P07Clock_Pre-Scalar_1 | Working | jff | | | | | |
| Clock_Pre-Scalar_1 | Working | jff | | | | | |
| P08Clock_Pre-Scalar_2 | Working | jff | | | | | |
| Clock_Pre-Scalar_2 | Working | jff | | 2014-07-22 20:24:15:500 | | | |
| P09Clock_Pre-Scalar_3 | Approved | jff | | | | | |
| Clock_Pre-Scalar_3 | Approved | jff | | | | | |
| P10Clock_Pre-Scalar_4 | Approved | jff | | | | | |
| Clock_Pre-Scalar_4 | Approved | jff | | | | | |
| P11TStc-716_Temp_Sensor | Approved | BalChen | | | | | |
| TStc-716_Temp_Sensor | Approved | BalChen | | | | | |
| P12PPGA_Controller_Block | Approved | BalChen | | | | | |
| PPGA_Controller_Block | Approved | BalChen | | | | | |



Administrative Control

- The ability to manage projects and project access for design teams
 - Provides ability to control project access and users roles
 - Create, edit, manage projects
 - Easily assign pages to users
 - Specific pages
 - Set of page numbers
 - Control user rights
 - What they can edit
 - What they can view

The screenshot shows a 'New Page' dialog box with the following fields and options:

- Page Name:** A text input field containing 'Micro Section' with an asterisk indicating it is required.
- Schematic:** A dropdown menu showing 'P01/DDXO-PROxx_Top_Blkg_Diagram'.
- Status:** A dropdown menu showing 'In Work' with an asterisk.
- Assigned Users:** A list of users: 'NatasiaR', 'BruceB', and 'PeterP', each with a close button (X).
- Buttons:** 'Create' and 'Cancel' buttons at the bottom right.

Administrative Control

Project
Management

Edit, Copy,
Freeze, etc.

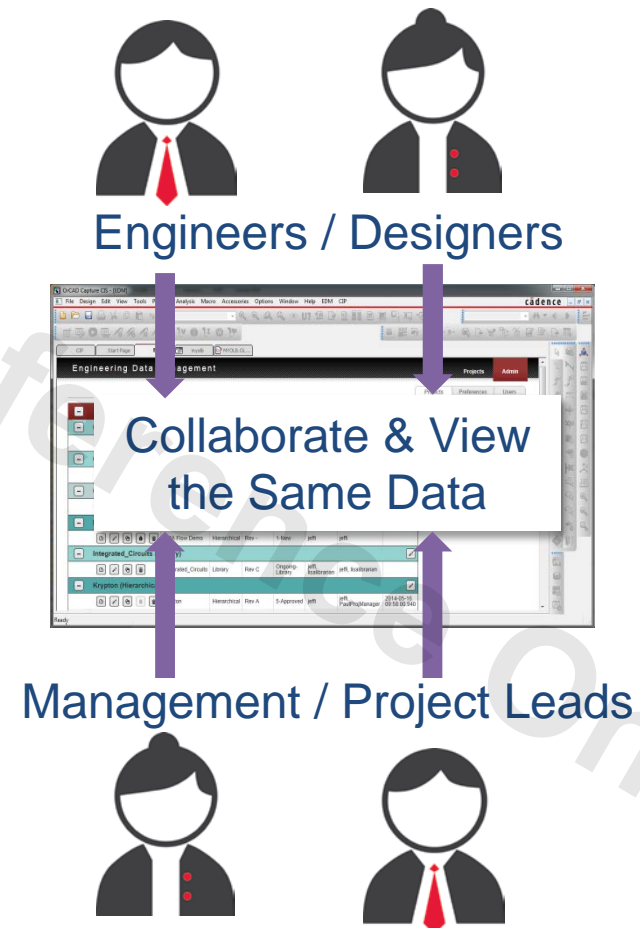
Assign Leads

Add / Delete
Users

| Project Name | Project Type | Revision | Status | Project Users |
|-------------------------------|---------------------|----------|--------------------|-----------------------|
| Capacitors (Library) | Capacitors | | | jeff, lisalibrarian |
| Connectors (Library) | Connectors | | | jeff, lisalibrarian |
| EMA Flow Demo (Hierarchical) | EMA Flow Demo | | | jeff |
| Integrated_Circuits (Library) | Integrated_Circuits | Rev C | Ongoing-Library | jeff, lisalibrarian |
| Krypton (Hierarchical) | Krypton | Rev A | 5-Approved | jeff, PaulProjManager |
| | Krypton | Rev C | 4-Pending Approval | jeff, PaulProjManager |
| | Krypton | Rev B | 3-Frozen | jeff, PaulProjManager |
| MicroDAC (Flat) | MicroDAC | Rev - | 1-New | BobUser |
| MISC (Library) | MISC | Rev B | Ongoing | jeff, lisalibrarian |
| Modules (Library) | Modules | Rev 1 | | jeff, lisalibrarian |
| Resistors (Library) | Resistors | | | jeff, lisalibrarian |
| RF Integrator (Flat) | RF Integrator | | | jeff, PegProjManager |
| Switches (Library) | | | | |

Change Tracking / Reporting

- The ability to input and track change through a design management cockpit
 - Full audit trail is maintained
 - Why/What
 - Who
 - When
 - Real-time status
 - Individual project status
 - All project progress
 - User tasks / progress



Change Tracking / Reporting

Project

What & Why

Versions

Projects > Krypton1_Rev0 > DDXO-PROxx_Top_Blk_Diagram - History

| Date | Action | Comments | Status | Copy |
|-------------------------|-----------------------------------|-----------------|--------|------|
| 2013-09-24 16:59:21.697 | Jeffi upload and unlock | Change Res | New | |
| 2013-09-24 16:55:22.117 | Jeffi download with lock for edit | Page downloaded | New | |
| 2013-09-24 14:22:00.383 | Jeffi unlock | Page unlocked | New | |
| 2013-09-24 14:20:28.017 | Jeffi download with lock for edit | Page downloaded | New | |
| 2013-09-24 12:21:18.410 | Jeffi upload and unlock | Deleted R23 | New | |

When

Who

OrCAD Capture CIS - [EDM]

File Design Edit View Tools Place SI Analysis Macro Accessories Options Window Help EDM CIP

cadence

CIP Start Page **EDM** myolb MYOLB.OL...

Engineering Data Management

Projects Admin

Projects Preferences Users

New Project
Refresh

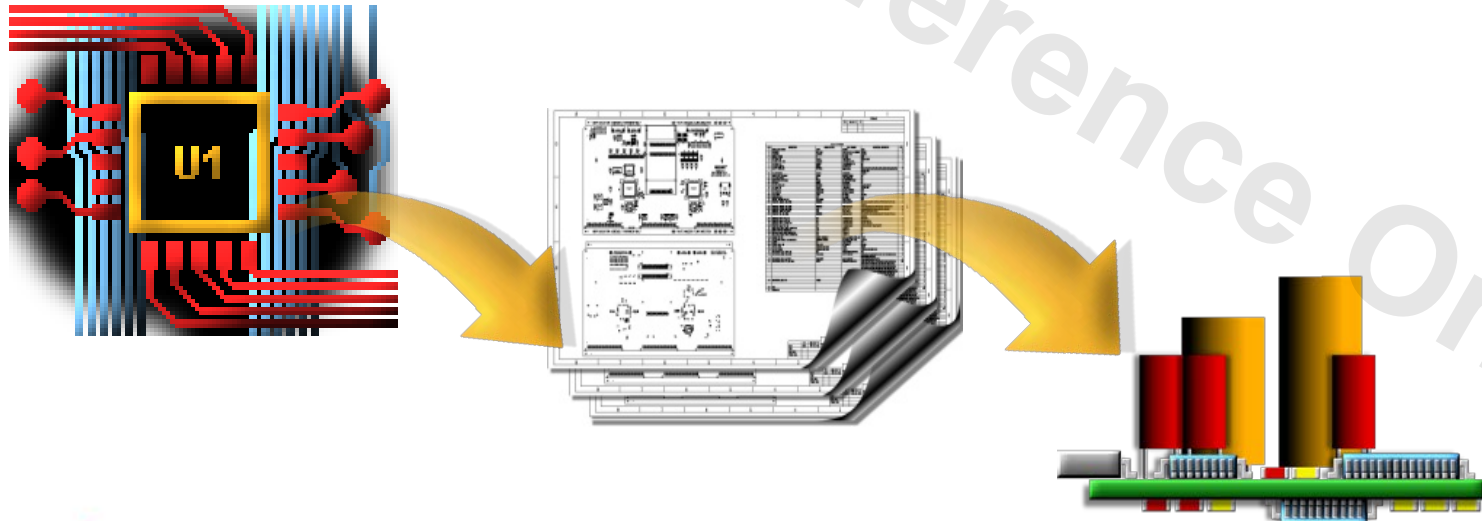
| | Project Name | Project Type | Revision | Status | Project Users | Project Leaders | Freeze Date |
|--------------------------------------|---------------------|--------------|----------|-----------------|---------------------|-----------------------|-------------------------|
| Capacitors (Library) | Capacitors | Library | Rev B | Ongoing-Library | jeff, lisalibrarian | jeff, lisalibrarian | |
| Connectors (Library) | Connectors | Library | Rev C | Ongoing-Library | jeff, lisalibrarian | jeff, lisalibrarian | |
| Controller (Flat) | Controller | Flat | Rev 1 | 1-New | jeff | jeff, PaulProjManager | |
| EMA Flow Demo (Hierarchical) | EMA Flow Demo | Hierarchical | Rev - | 1-New | jeff | jeff | |
| Integrated_Circuits (Library) | Integrated_Circuits | Library | Rev C | Ongoing-Library | jeff, lisalibrarian | jeff, lisalibrarian | |
| Krypton (Hierarchical) | Krypton | Hierarchical | Rev A | 5-Approved | jeff | jeff, PaulProjManager | 2014-05-16 09:58:00.940 |

Ready

OrCAD Documentation Editor

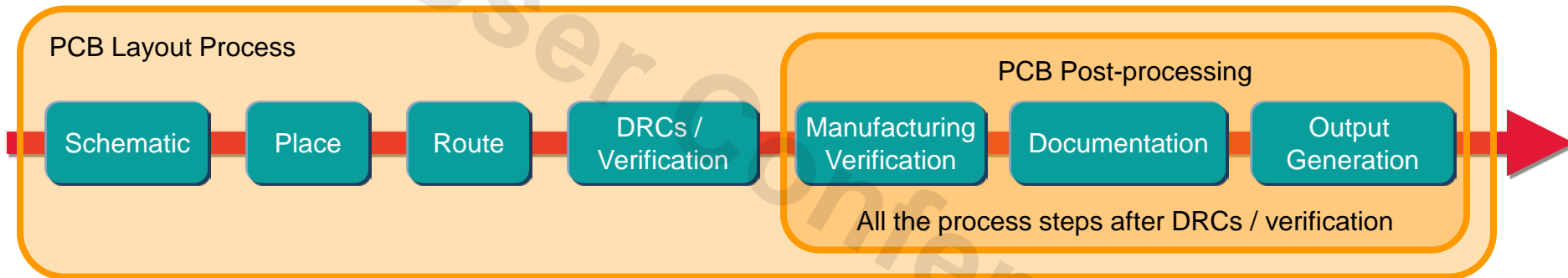
Questions and Concerns

- To go from design to an end product, it must be able to be fabricated and assembled with high-quality, at a profit, and in volume.
- Delays and re-spins can result in project impacts and missed schedule targets.
- Manufacturing issues can drive up project costs and impact profit.



PCB Post-processing

- Preparation of a PCB design for manufacturing along with all the data and documents for use by fabricators, assemblers, testers / inspectors, service technicians, etc.

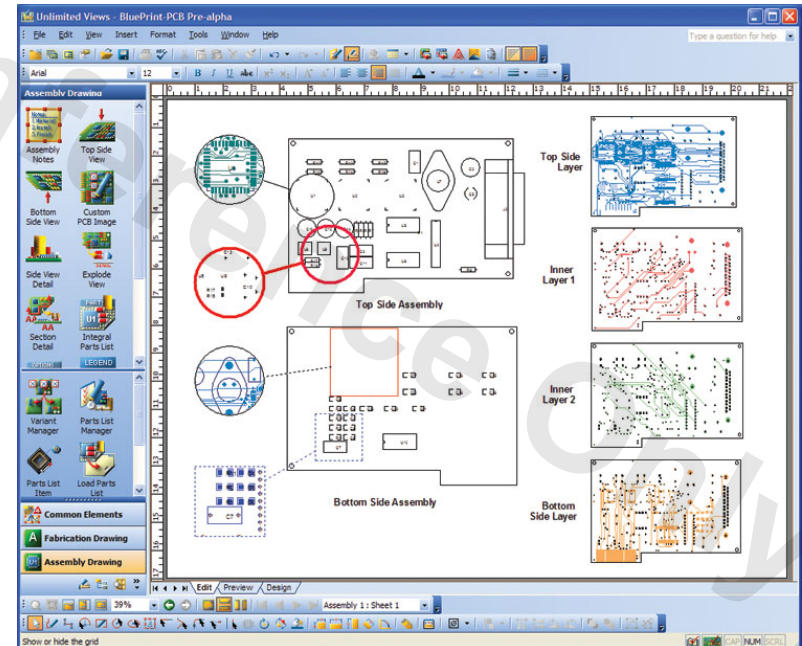
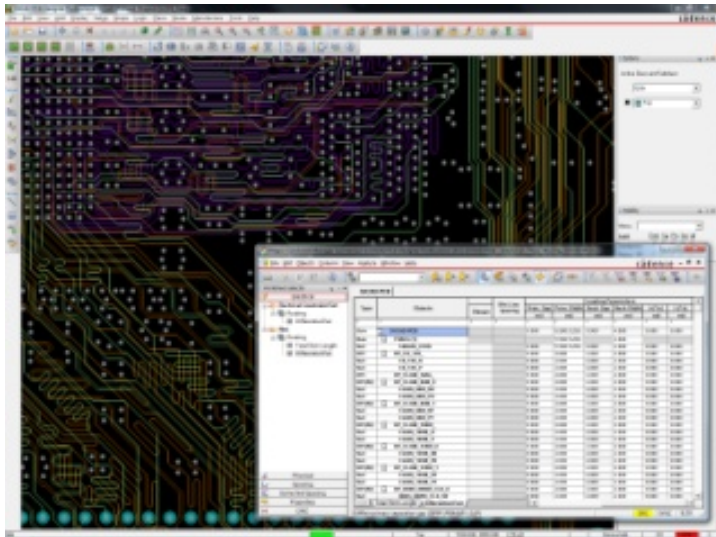


PCB Post-processing

- Gerber / netlist verification and drill optimization
- Panel creation
- Assembly and test verification
- Documentation (fabrication, assembly, etc.)
- Output generation (Gerber / 2581, drill, mill, pick and place, BOM, etc.)

OrCAD Documentation Editor

- OrCAD® Documentation Editor is an intelligent, interactive PCB documentation environment that enhances and significantly simplifies the PCB documentation process. It does this by automating the creation of documentation elements and utilizing advanced technology that directly leverages PCB design data, synchronizes engineering change orders (ECOs), and enables dynamic content. OrCAD Documentation Editor streamlines the entire PCB design.

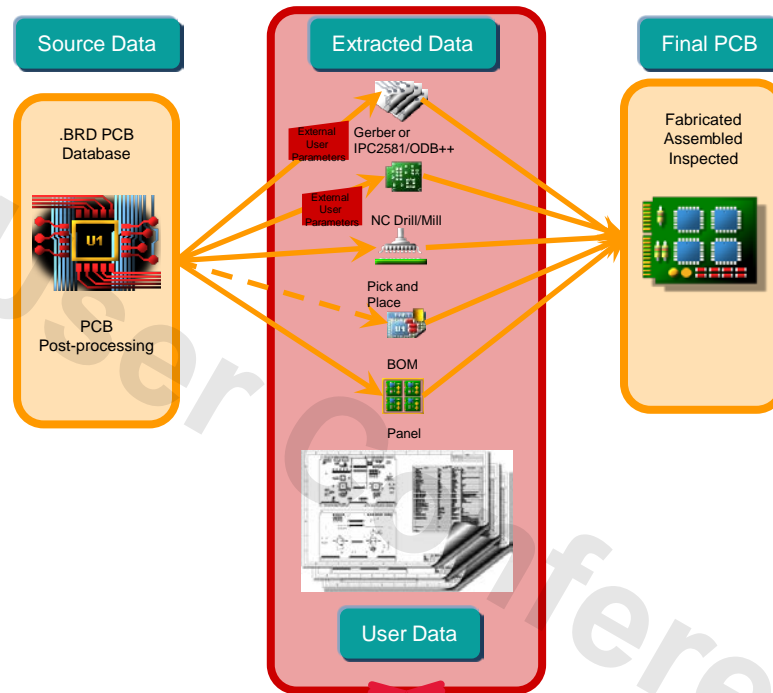


Why is Any of This Important?

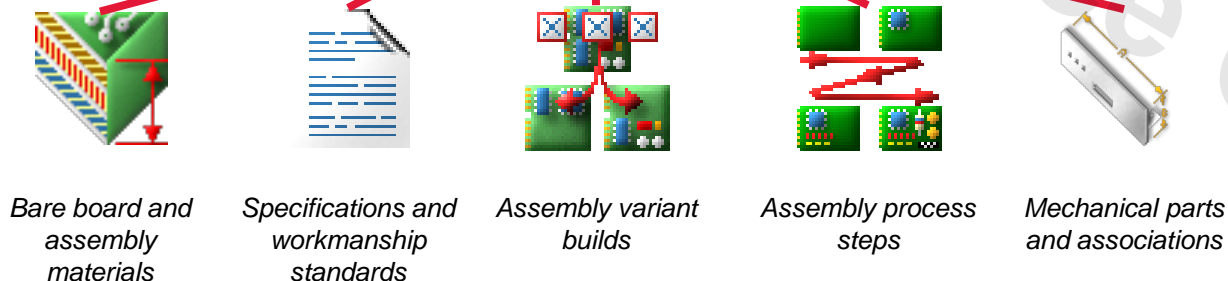
- Every PCB design must be documented(a little or a lot)
- CAD tools were not designed for drafting / documentation
- Even though documentation adds no value to the end product, it can impact a project just as a short on a board will scrap a batch of boards
- PCB designers and design teams face two, undesirable, choices when it comes to producing PCB documentation
 - An average the PCB design to produce adequate documentation for assembly and manufacturing that utilizes highly skilled, highly compensated PCB designers who could be off to the next project
 - Attempt to reduce the design cycle time by producing very cursory documentation that potentially increases the risk of project delays due to incomplete or inaccurate fabrication or assembly instructions and/or intent

Document Authoring

PCB documentation controls how all the various outputs are used together to create the final PCB, then used to verify that the final PCB was put together correctly

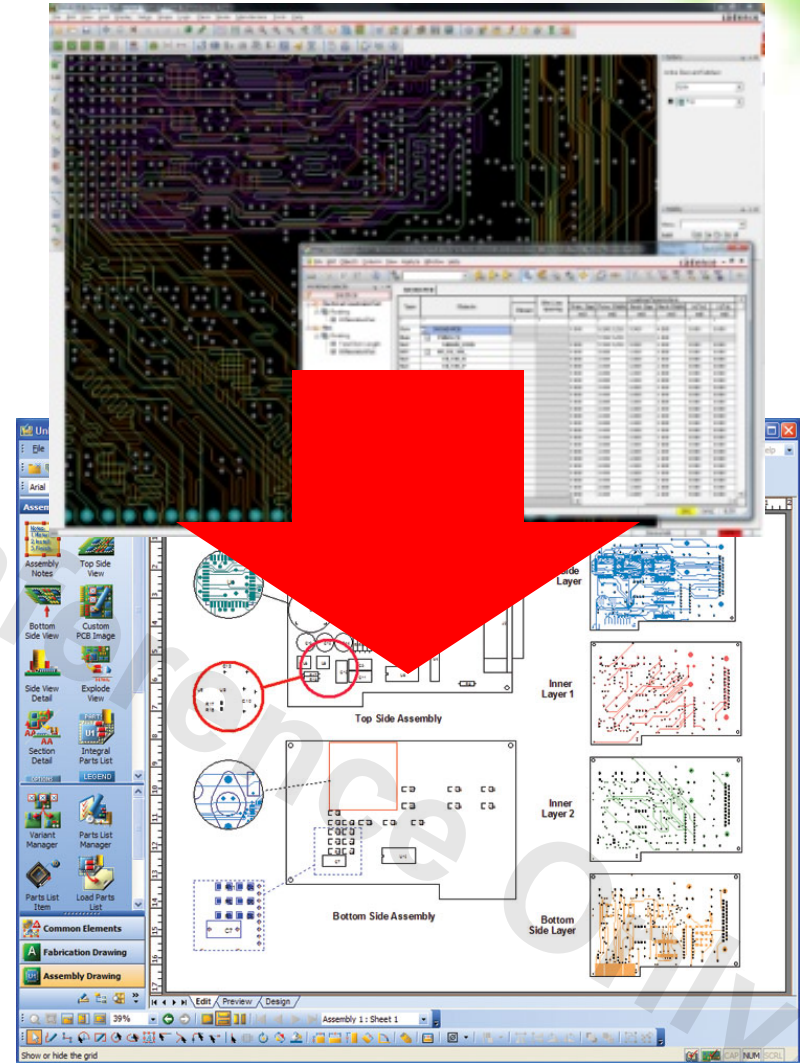


PCB documentation also specifies how external requirements are to be merged with outputs to create the final PCB



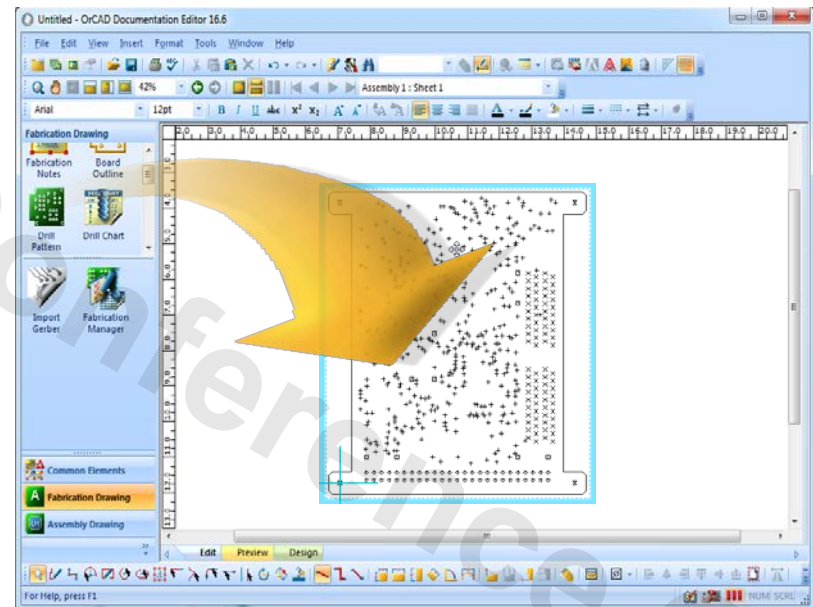
Design-driven Intelligence

- Entire PCB Editor database is imported and used to create documentation / elements
 - CAD database import
 - Templates
 - Elements



Drag...Drop...Draw

- Automatically creates fabrication and assembly elements intelligently and accurately
 - Views, details, and tables
 - Templates
 - Elements



Instant Documentation ECOs

- Automatic element update based on CAD data revisions / ECOs
 - Views, details, and tables
 - Templates
 - Elements

