

2013
AUG 13
TAIPEI

Graser
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Conference






Chip, Package , Board Co- Simulation For 3D/2.5D IC Design

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Trends and Challenges

- Quest for higher data rate

- Clock speed 
- Feature size 
- Power supply voltage 
- Noise margin 
- Packaging density 



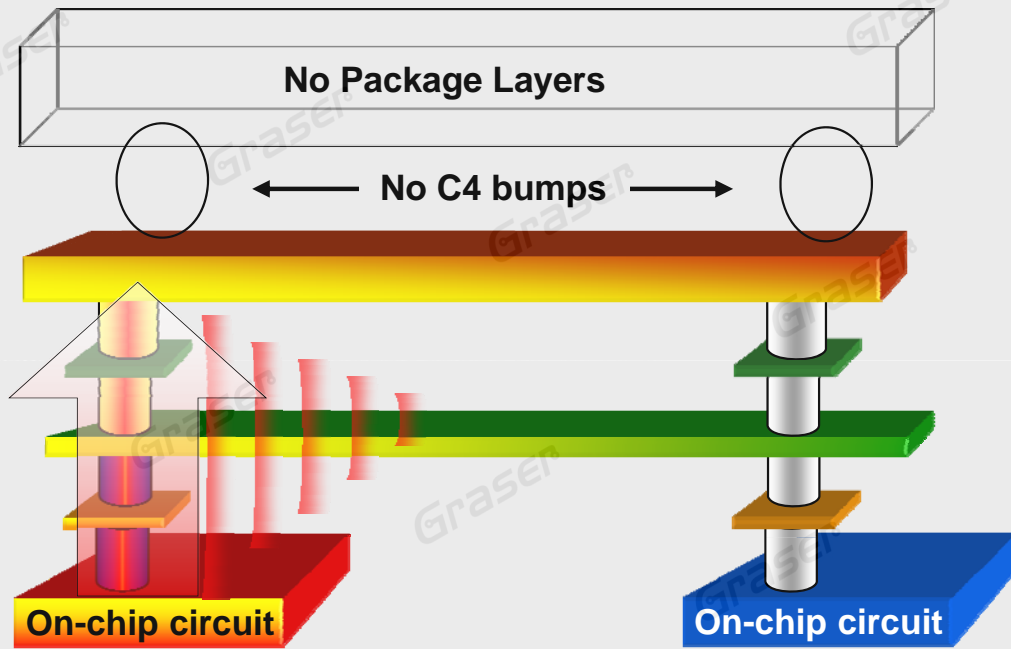
- Designer's Challenges

- PI (On-chip PDN, SSO noise, ...)
- SI (3D crosstalk, return current path, ...)
- EMC (In-system EMI, noise immunity, ...)
- Package design (MCP, SiP, PoP, SoC, ...)
- Modeling / simulation
- Cost down, short time-to-market, ...

Why to Do Chip-Package-Board Co-Simulation

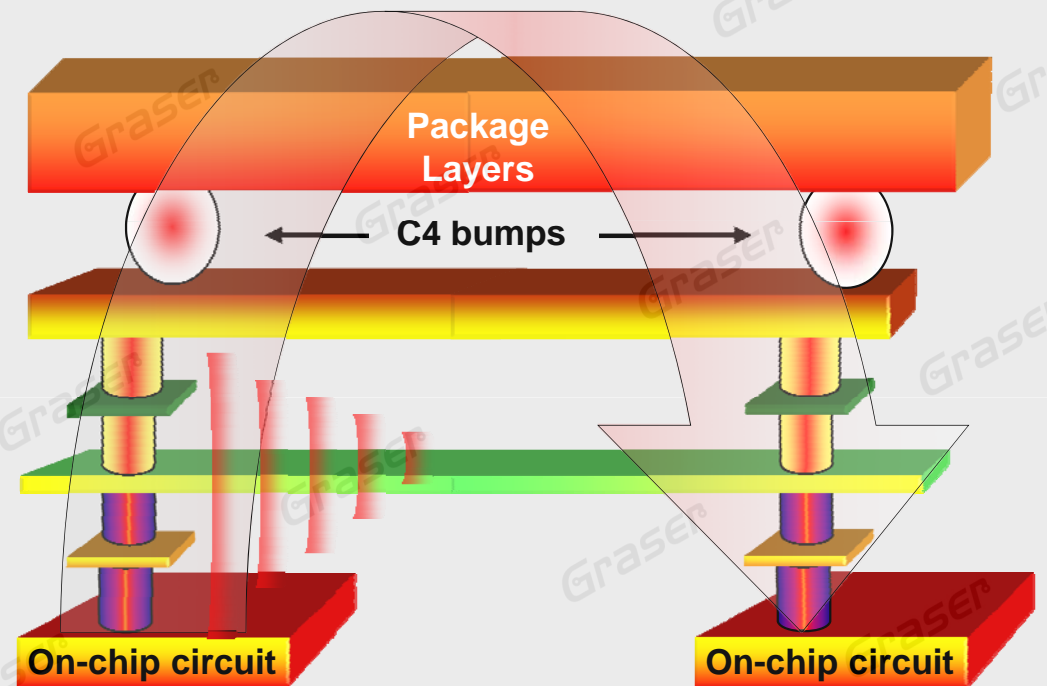
- Quite often the power and ground noise on the chip are computed under the condition that the voltage sources are connected directly at chip bumps.
- Sometimes simplistic per-pin RLC models are used that do not accurately represent the actual package and board effect.
- The power and ground noise, especially the dynamic voltage fluctuation, on the chip is dramatically different from that with voltage sources connected directly at chip bumps, and heavily depends on the package and board model used.
- Adequate modeling of package and board effect is crucial to obtain reliable solution of dynamic voltage fluctuation on the chip.

Why does Chip-System Co-Design?



Chip

Highly resistive / High-loss system
Results in localized voltage noise effects



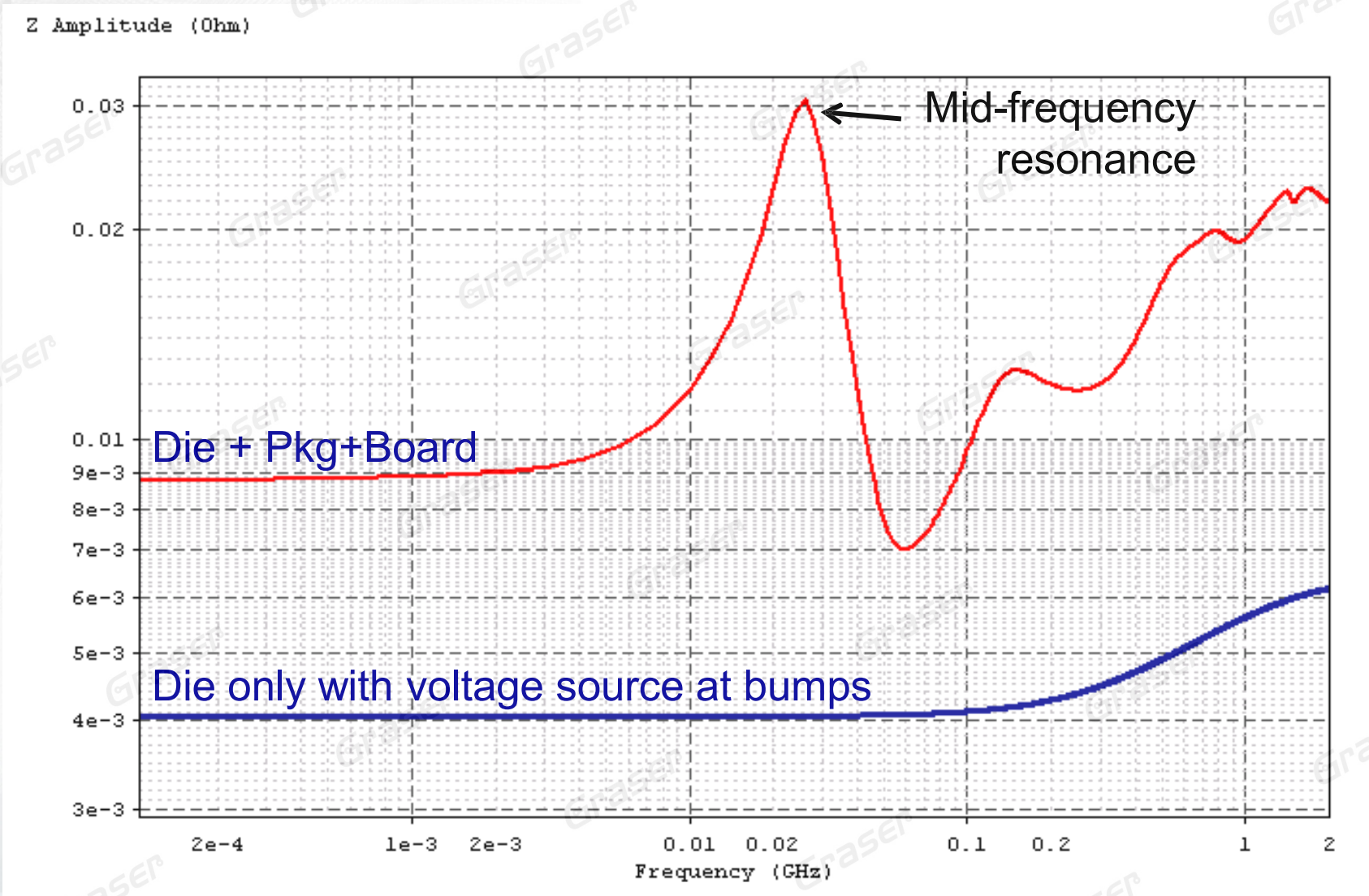
Package

Low impedance / Low-loss system
Results in global voltage noise effects to other IC circuits

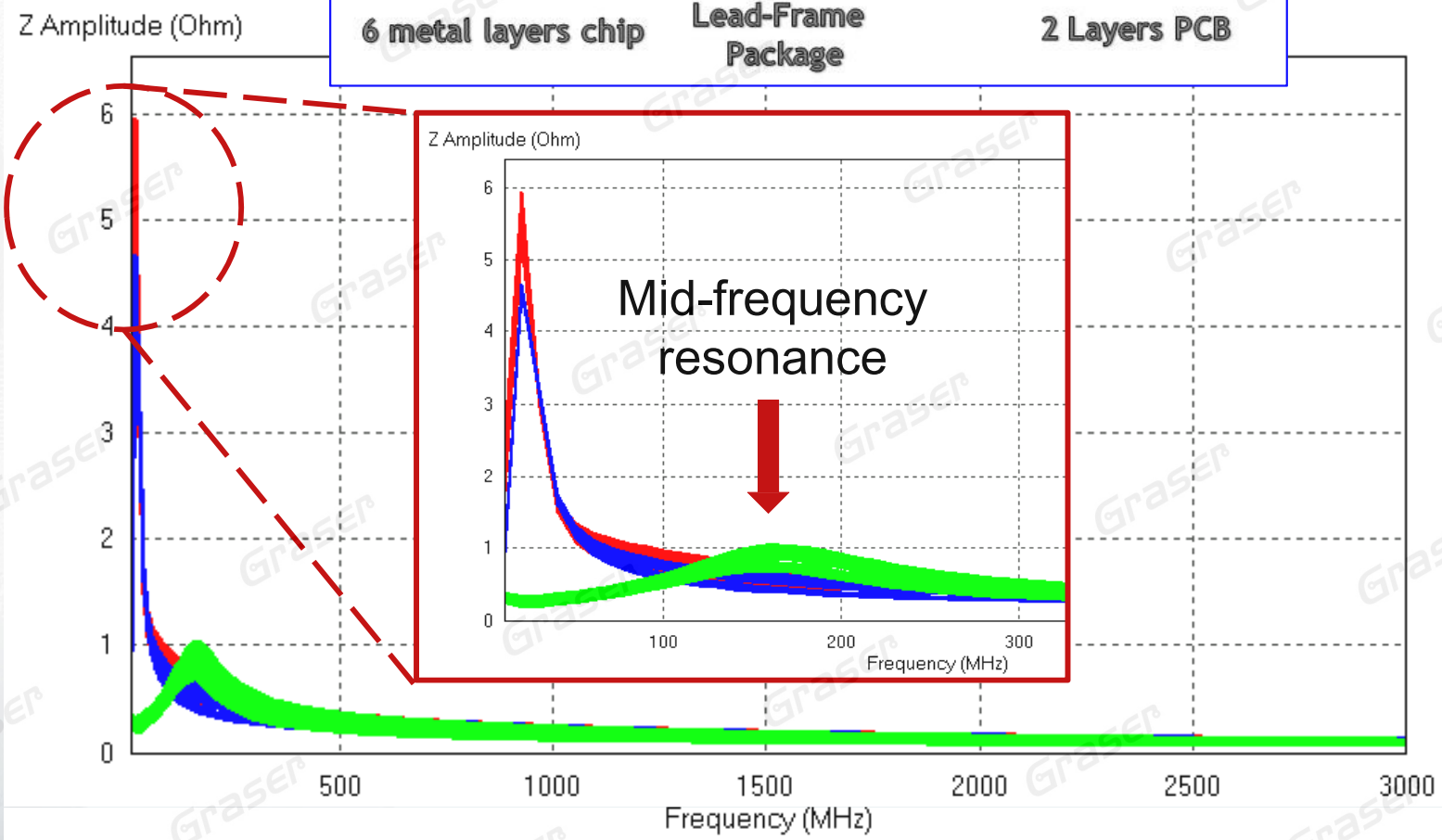
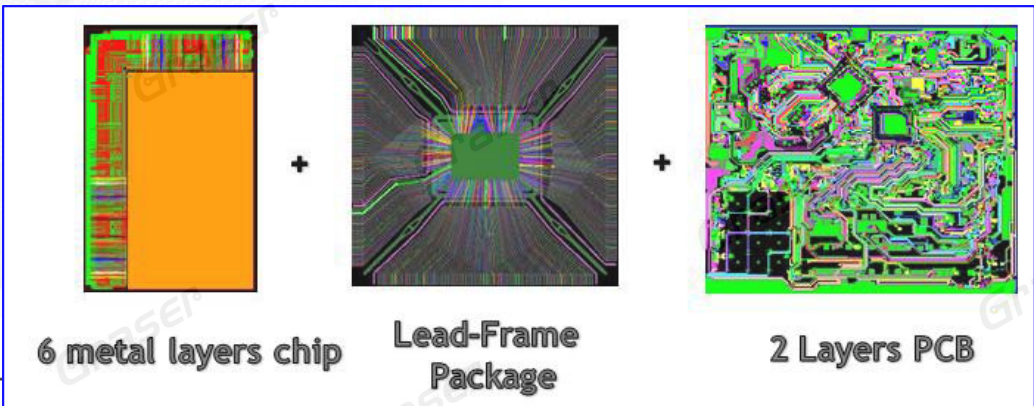
The low-loss power distribution system of the package easily transfers voltage noise effects to other on-chip circuits

PDN Impedance Analysis

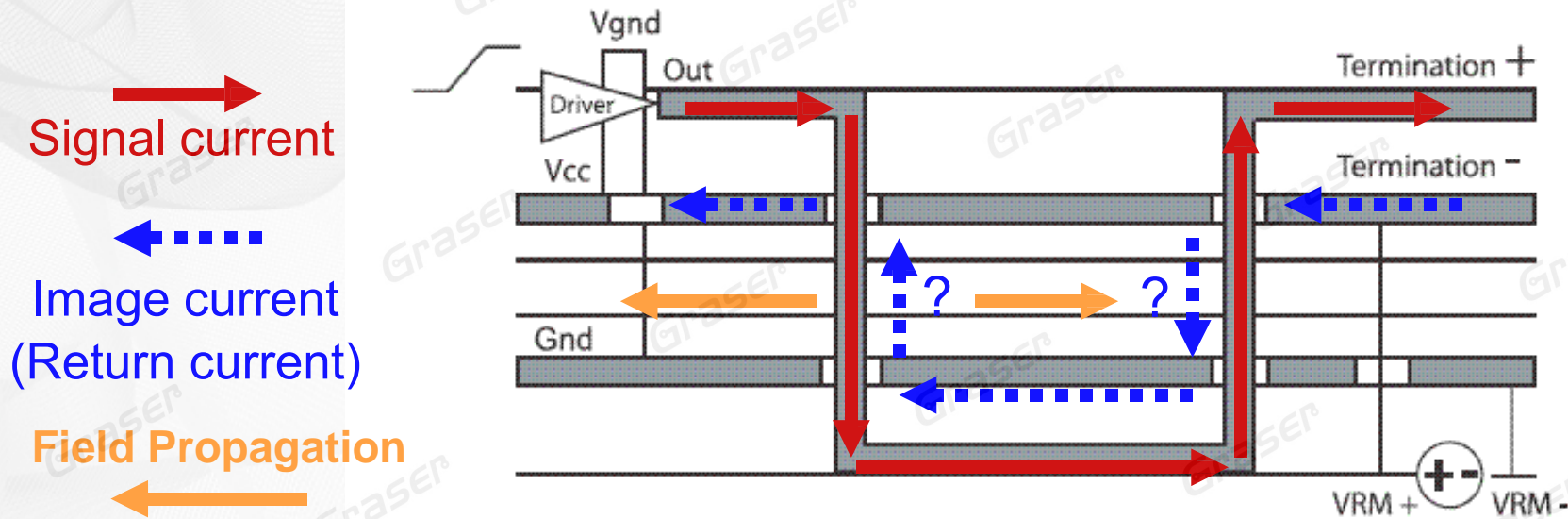
(At one observation port on metal1 layer)



PDN Impedance Analysis

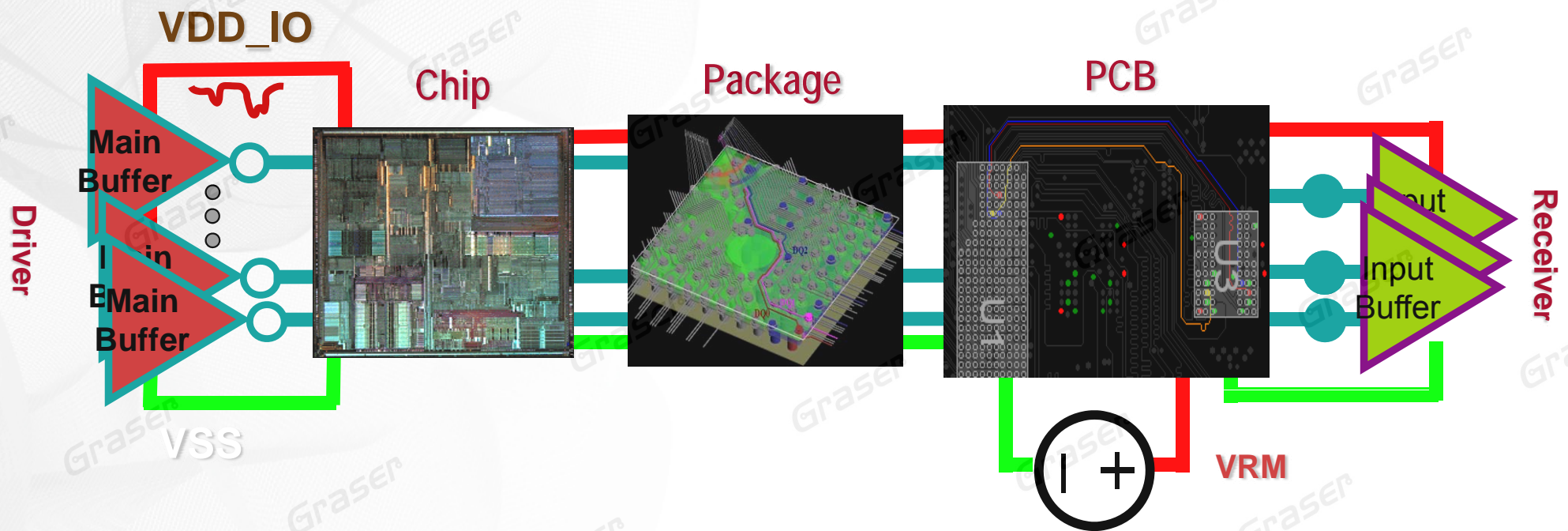


Coupling Mechanism Among Signal/Power/Ground



- Vias coupling in free space is decreased and proportional to $1/r^2$
- Via coupling between field domain (waveguide like) may be enhanced and attenuated slowly.
- Field coupled is strong when field components are in parallel
- For TM/TE like field propagate between power/ground domain, signal via is strongly coupled with field between power and ground due to field components are in parallel.
- Chip level P/G grids are formed as domain and interact with signal (RDL)
- From system level perspective, current loops formed by signal to ground and power to ground will interfere with others

Challenges for System Level SSO Simulation

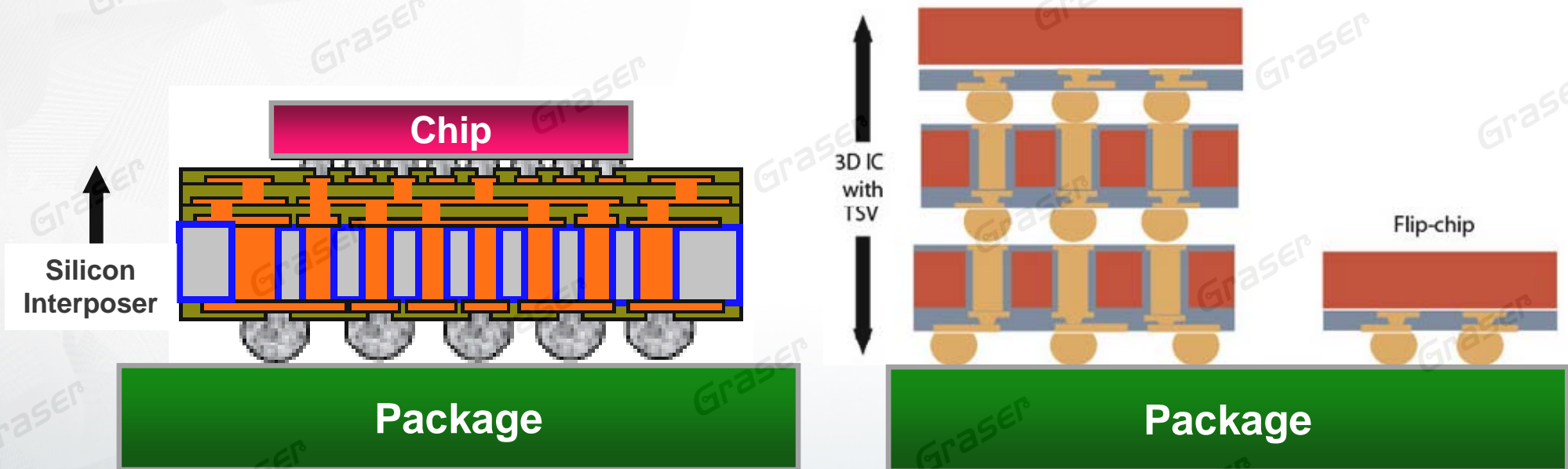


- The complex manual task for nodes linkages between circuits.
- No guaranteed for passivity and causality on each circuit block.
- Non-linearity of the whole system circuit network which include transistor models of drivers and receivers
- Lost DC accuracy without low frequency data from EM solver, especially for SI analysis with power aware
- Long run time and non-convergence result are commonly happened.

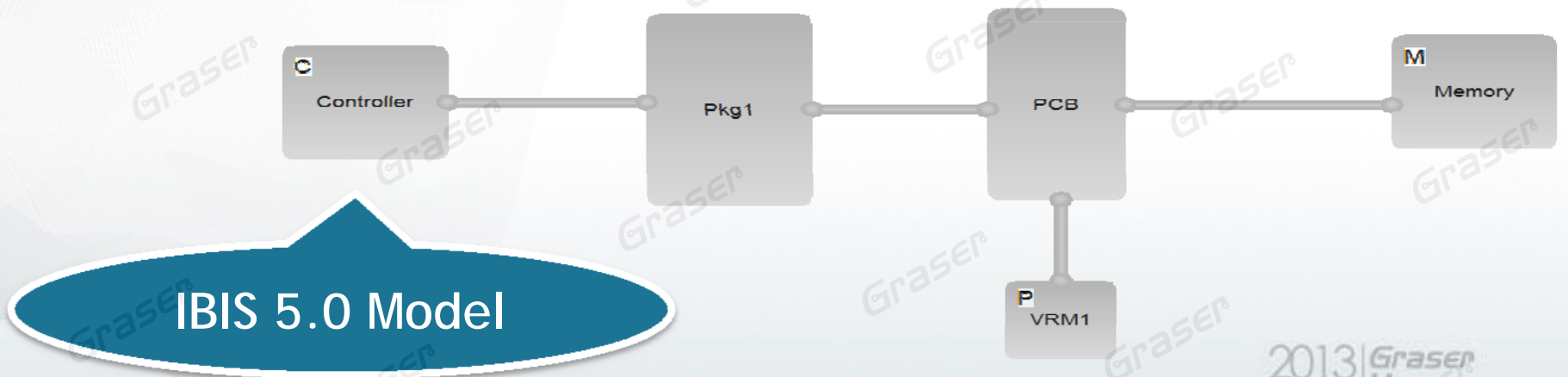
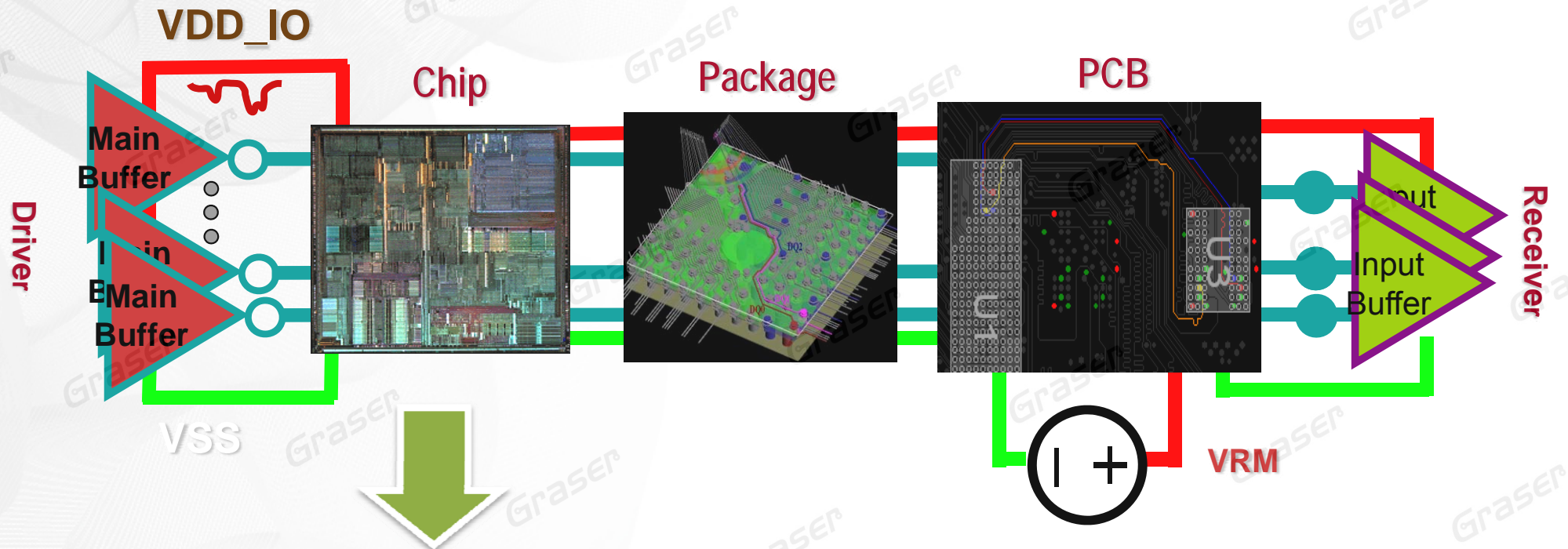
Cadence solutions are adopted to overcome problems listed as above

Additional Chip-to-Chip Interconnect

- Flip-chips and routable package substrates
 - C4 bumps, RDL routing, and package routing (including vias)
- Through silicon via interconnect
 - TSVs, micro bumps, and silicon interposers

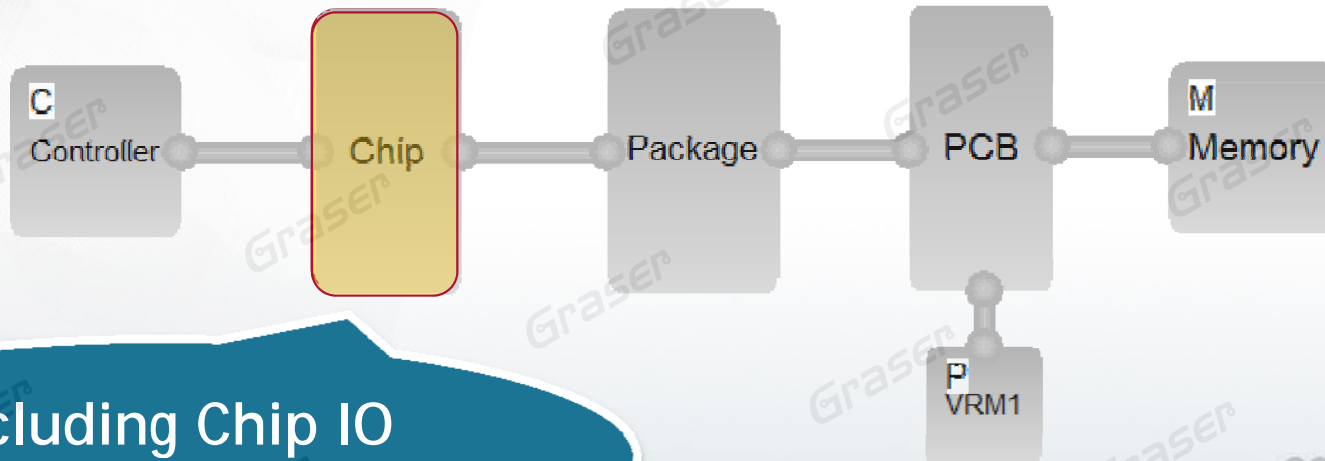
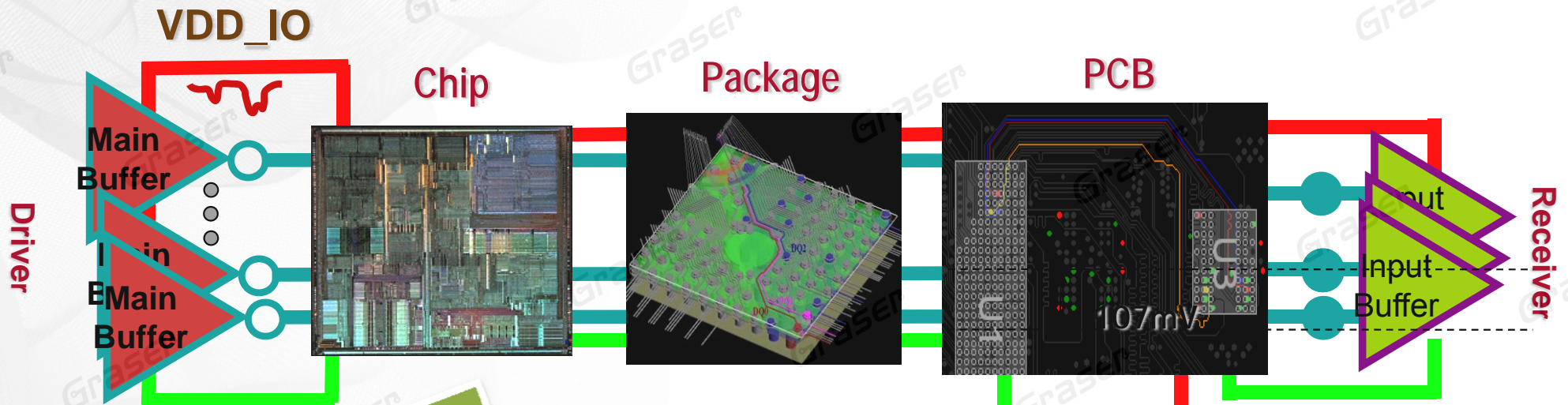


High-Speed IO System-Level SSN Simulation



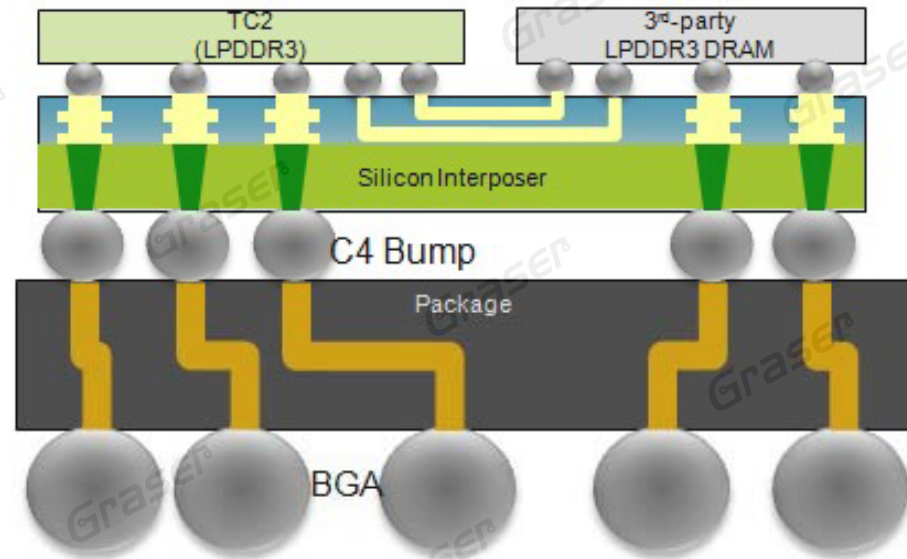
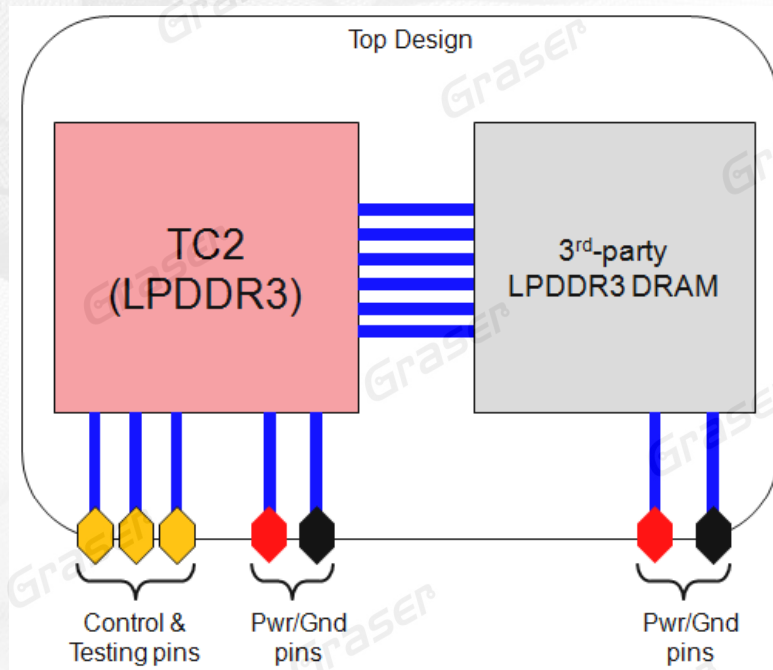
IBIS 5.0 Model

High-Speed IO System-Level SSN Simulation

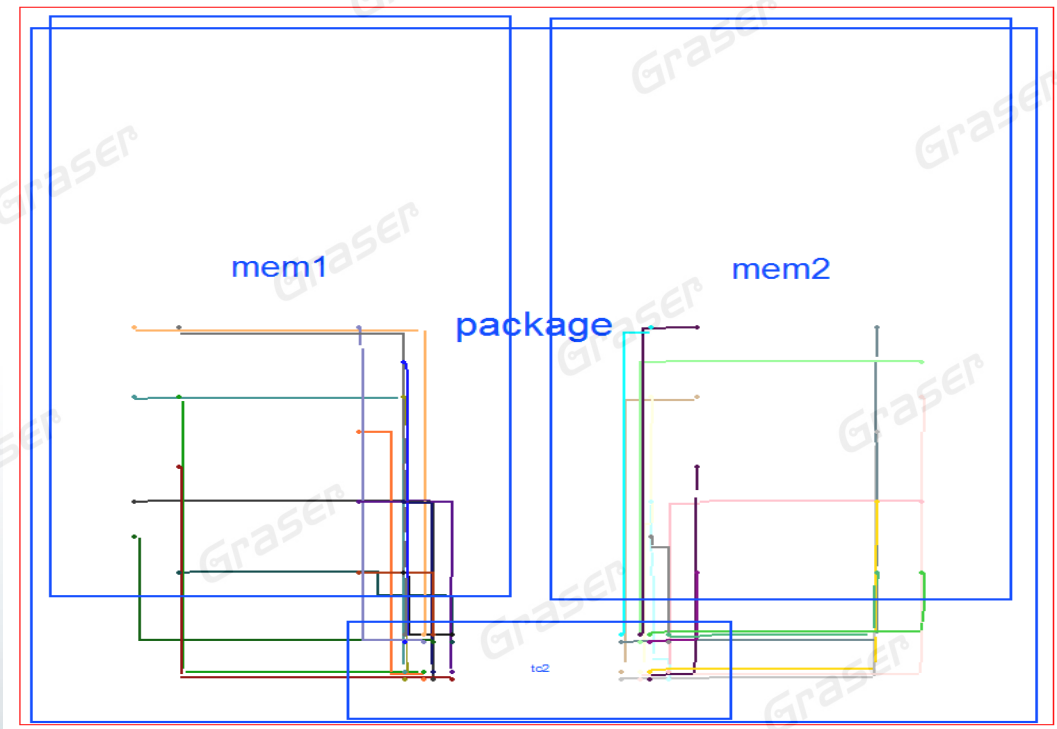


Including Chip IO Interconnect Model

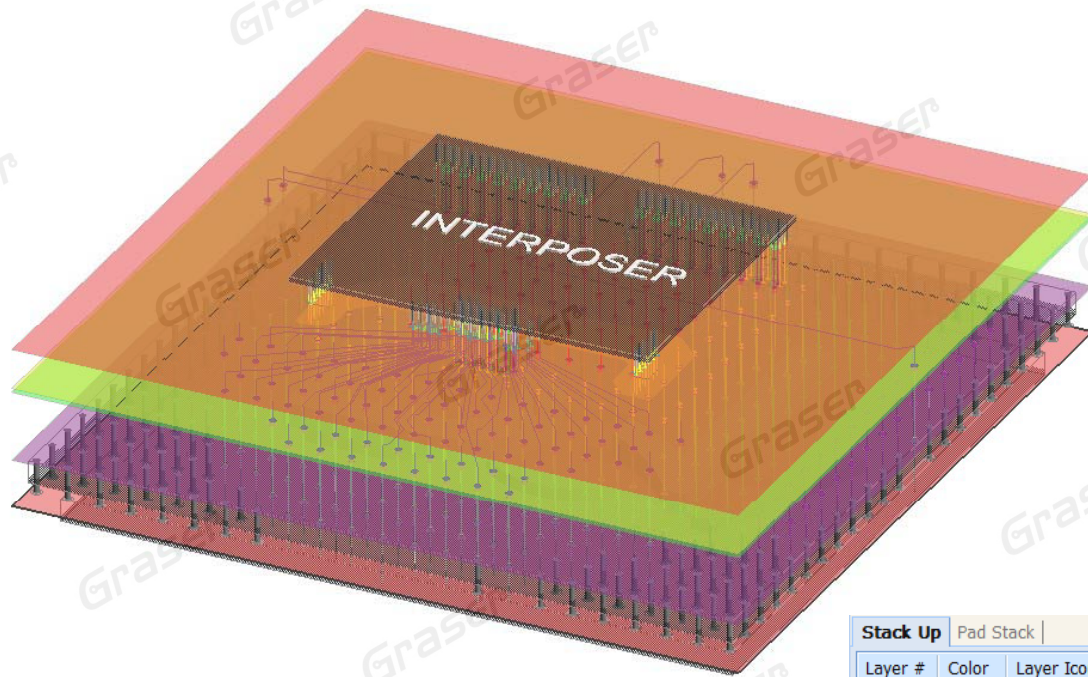
System Architecture-2.5D IC



- There are 3 daughter dies placed on interposer, TC2 and 2 memory dies.
- Only TC2 and Interposer GDS layout are considered during the analysis.
- 3rd party LPDDR3 DRAM is used and physical gds layout is not available. We just consider DDR I/Os on interposer directly.



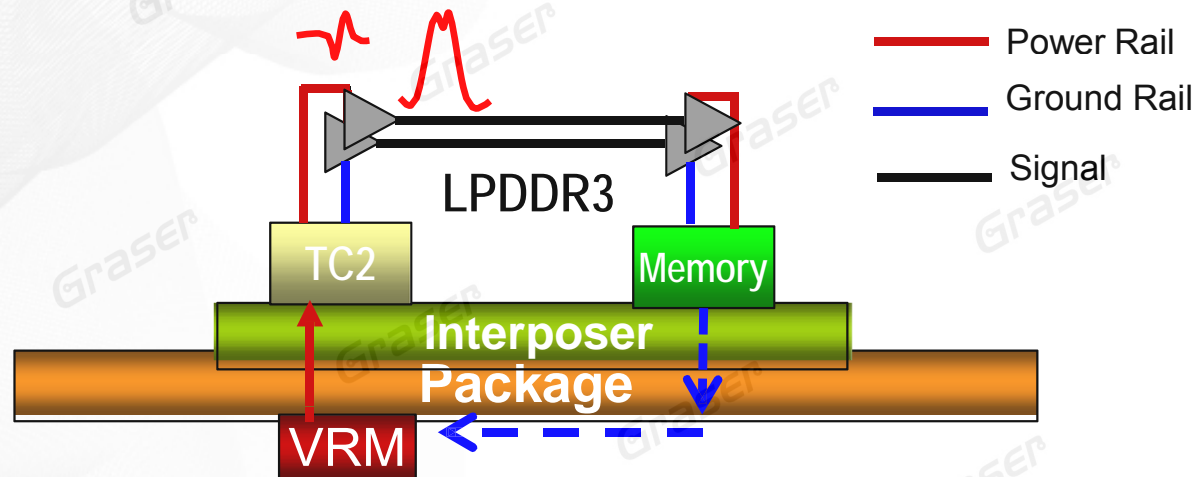
System Architecture-Package



- LPDDR3 interface is implemented on interposer. Package design here is to play a role for power delivery for TC2 and memory dies.

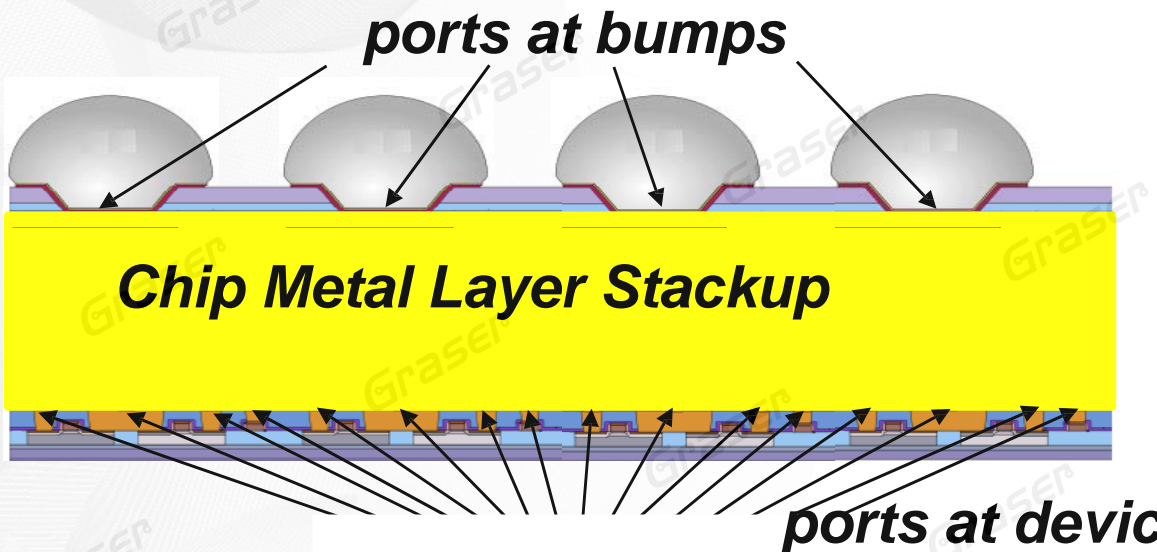
Layer #	Color	Layer Icon	Layer Name	Thickness...	Material	Conductivity...	Fill-in Dielectric	Permittivity	Loss Tangent
			Medium03	0.005				4	0
1	Yellow	Signal	Signal\$TOP	0.00145		4.3e+007		[4.15]	[0.001]
			Medium\$SIIA23	0.000775				4.3	0.002
2	Blue	Signal	Signal\$SILM2	0.000900001		5.959e+007		[4.3]	[0.0011]
			Medium\$SIIA12	0.000619999				4.3	0.0002
3	Red	Signal	Signal\$SILM1	0.000900001		5.959e+007		[8.1]	[0.0011]
			Medium\$TSV_VIA	0.1008				11.9	0.002
4	Yellow	Signal	Signal\$SILMB	0.002		4.3e+007		[8.2]	[0.001]
			Medium\$C4_VIA	0.06				4.5	0
5	Blue	Signal	Signal\$PKG_M1	0.015		5.959e+007		[4.5]	[0.0175]
			Medium\$49	0.2032				4.5	0.035
6	Red	Signal	Signal\$PKG_M2	0.03048		5.959e+007		[4.5]	[0.035]
			Medium\$51	0.2032				4.5	0.035
7	Yellow	Signal	Signal\$PKG_M3	0.03048		5.959e+007		[4.5]	[0.0235]
			Medium\$53	0.03				4.5	0.012
8	Blue	Signal	Signal\$PKG_M4	0.018		5.959e+007		[4.5]	[0.0155]
			Medium\$55	0.8				4.5	0.019
9	Red	Signal	Signal\$PKG_M5	0.018		5.959e+007		[4.5]	[0.0155]
			Medium\$57	0.03				4.5	0.012
10	Yellow	Signal	Signal\$BOTTOM	0.015		5.959e+007		[4.25]	[0.006]
			Medium01	0.35				4	0
11	Blue	Signal	Signal01	0.03556		5.8e+007		[4]	[0]
			Medium02	0.1				4	0
12	Green	Plane	Plane01	0.03556		5.8e+007		[1]	[0]

Power-Aware SI Analysis with Chip-Package Co-Simulation

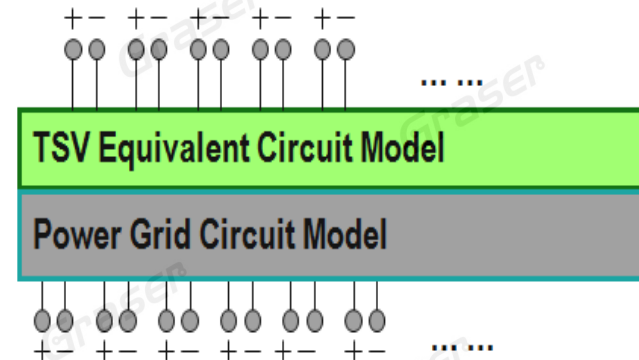
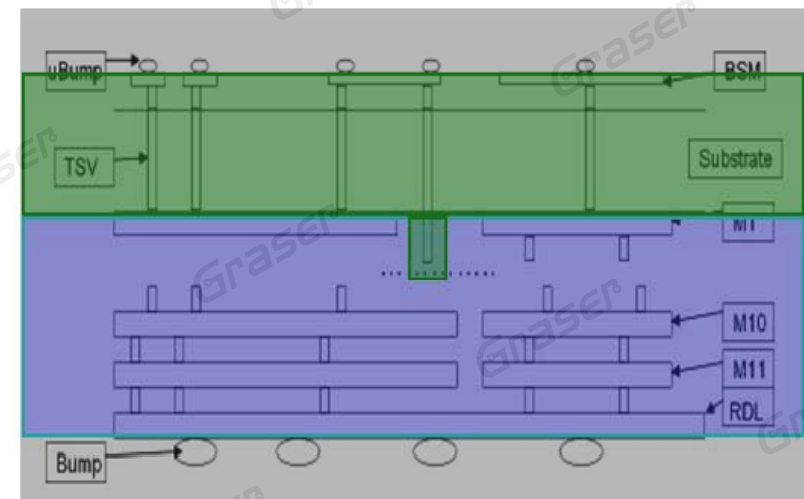


- The power is supplied by voltage regulation module (VRM) on package
- Input impedance observed by TC2 or Memory that cause voltage droop at driver end and leads to signal quality and timing degradation.
- Traditional chips only analyze that powers the chip at interposer or driver end that will obtain over optimistic result and lead to wrong judgment on design problem.
- To overcome the long run time and non-convergence result in TD analysis, power-aware IBIS behavior model and passivity guaranteed chip and package models are required.

I/O Model Extraction with XcitePI-IOME

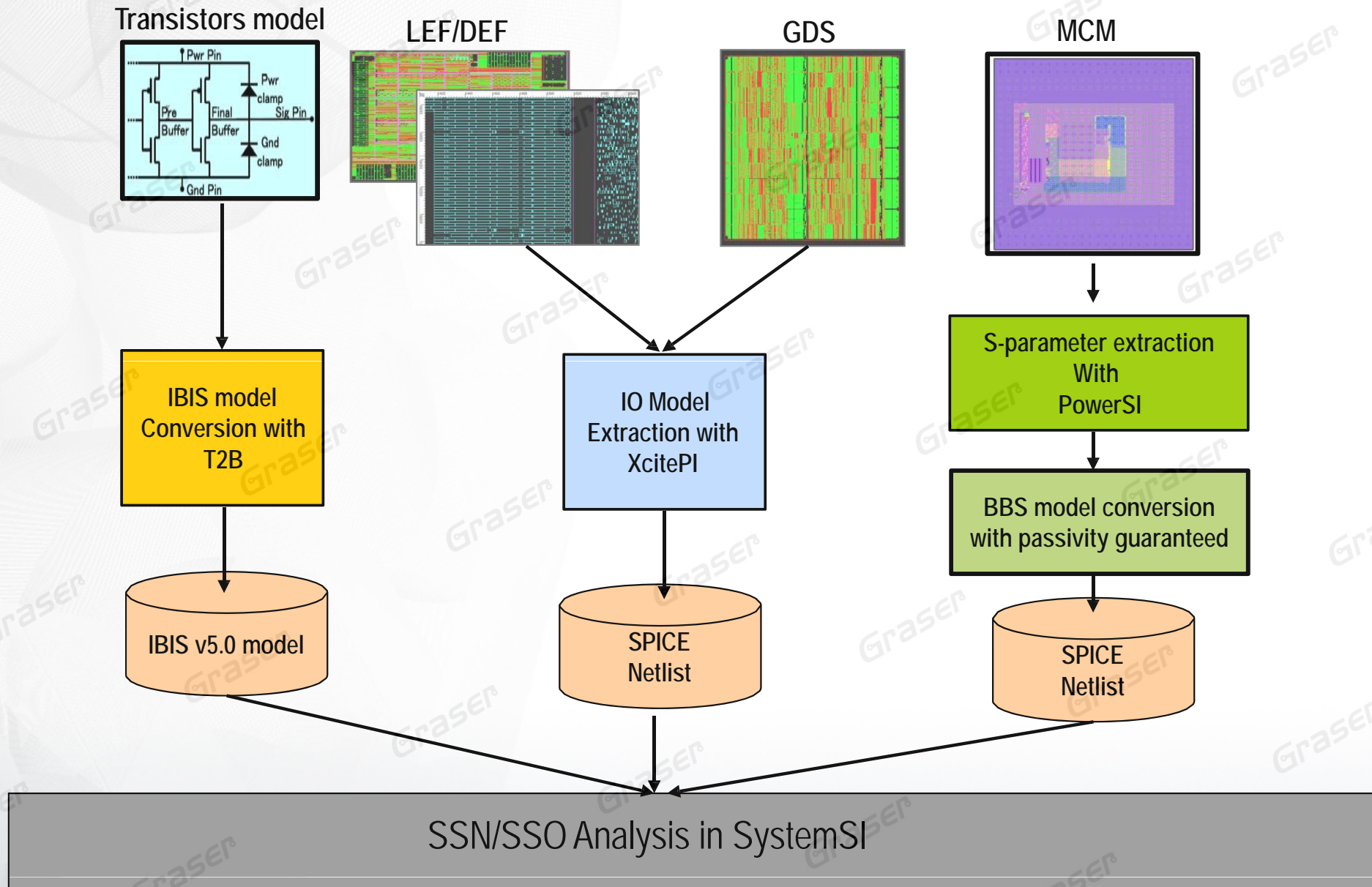


Connect to I/O cells through these ports



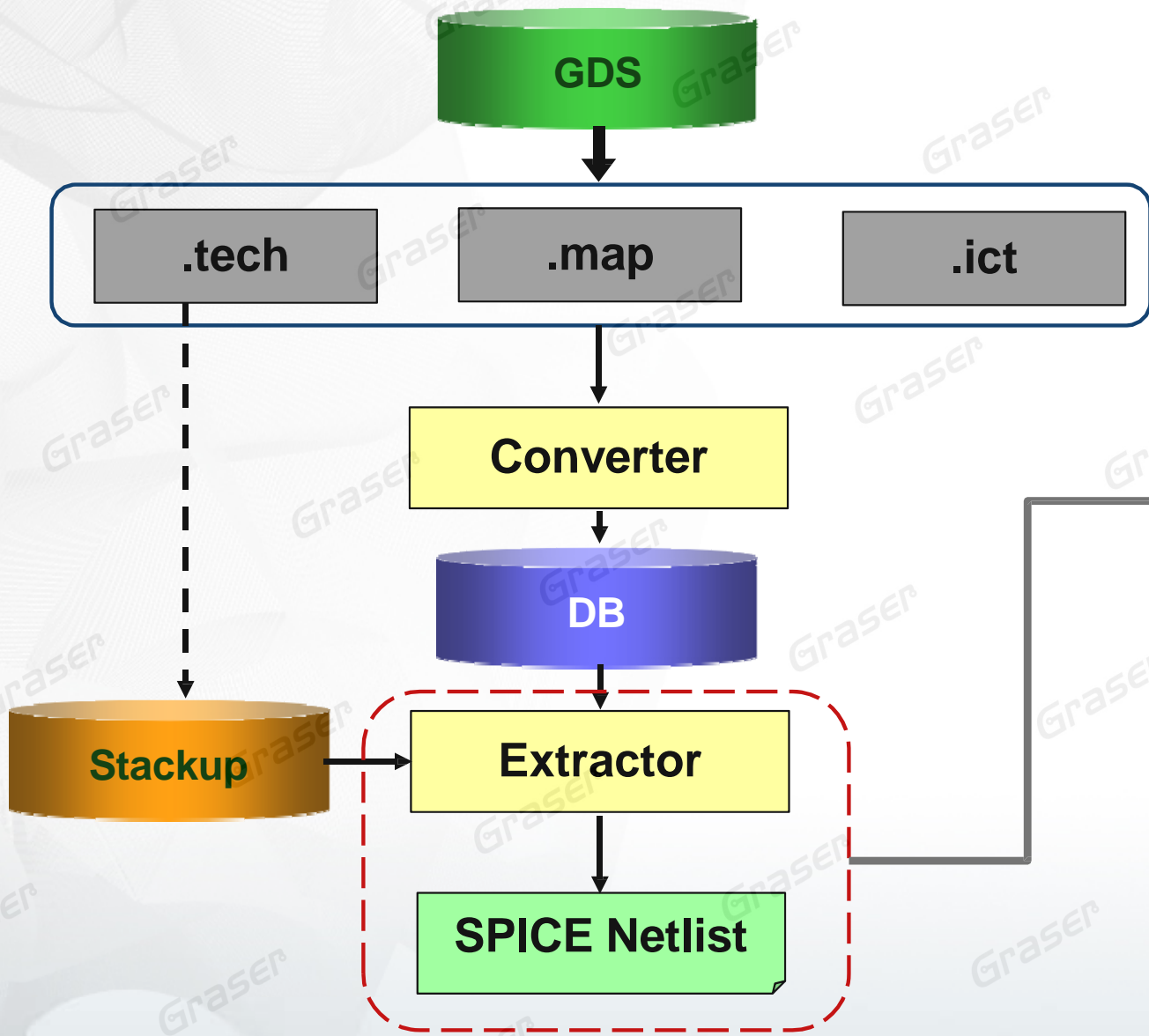
- All ports for I/O signal/power/ground at devices and bump side are set automatically.
- TSVs model and I/O P/G/S are extracted independently and then combined into one SPICE netlist for interposer model generation.
- TC2 extracted I/O model will cascade with interposer part later in SystemSI

SSO/SSN Analysis with Cadence Solutions



XcitePI – IO Model Extraction IOME

I/O Model Extraction with XcitePI-IOME



IO Model Extraction
Manage Design
New Design
Open Design
Save
Technology Setup
Package Type
Bump Parameter
Stackup
Via Resistance
Chip Setup
Chip Size
Net
Bump
Via
Core Area
Circuit Setup
Definition
Placement
Decap
External Component
Output Setup
Spice Netlist
Port
Probe
Performance Assessment
Checklist
View/Export Result

Work flow to guide you how to generate I/O model

XcitePI - IOME

The screenshot displays the XcitePI software interface for IO Model Extraction Setup. The main window shows a layout view with components labeled 'ram1', 'ram2', and 'package'. The 'External Component' table provides detailed information for each component.

Name	Layer	ltx (um)	lty (um)	urx (um)	ury (um)
ram1	bump	849.339130	3031.543478	8125.043478	15871.021739
ram2	bump	10086.630435	3102.873913	17255.339130	15871.021739
tc2	bump	6341.782609	0.000000	12048.217391	2246.908696
package	TSVBump	171.700000	0.000000	18360.960870	16370.334783

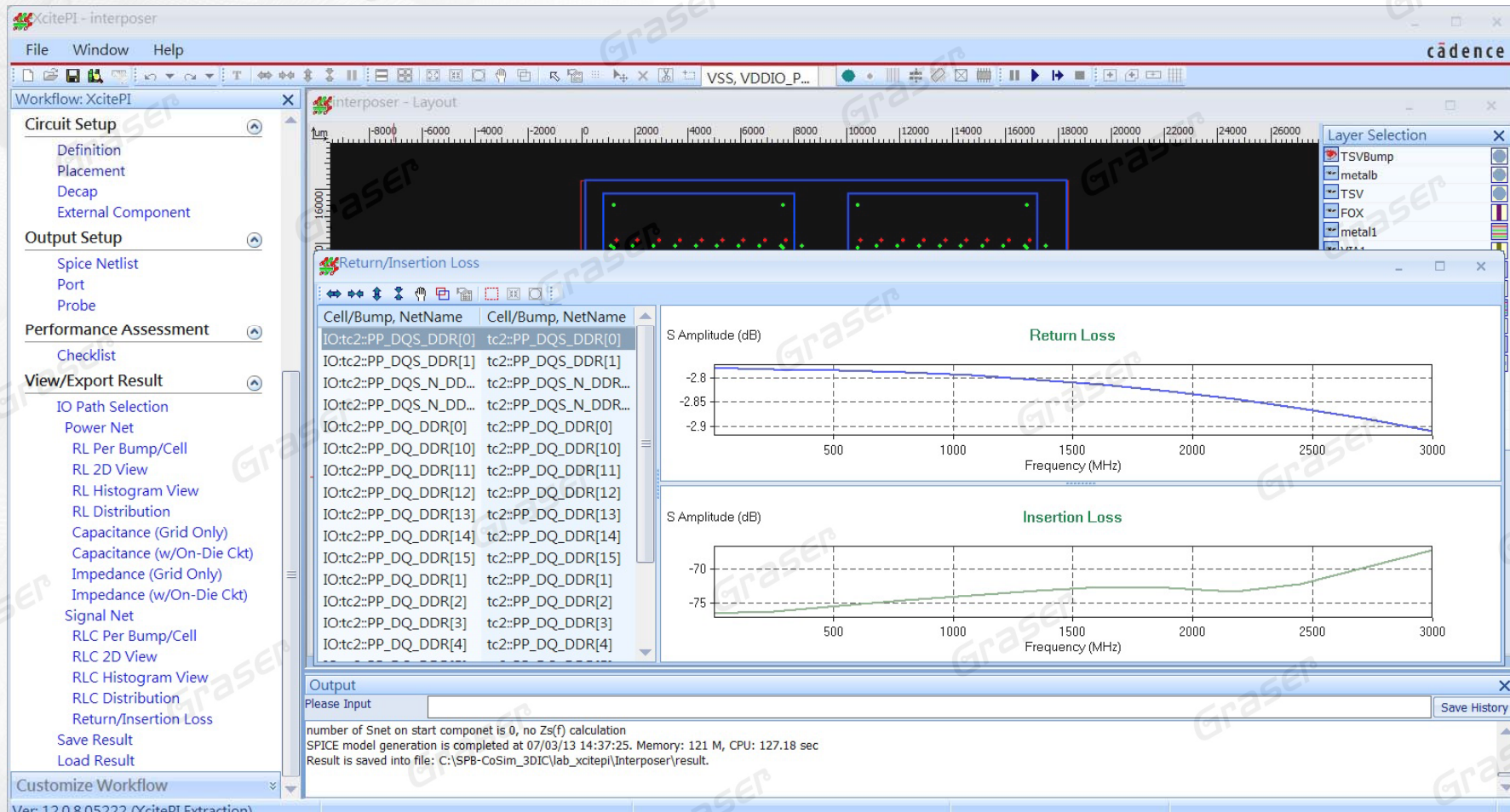
XcitePI – IOME

EPA

The screenshot displays the Cadence XcitePI software interface. The main window shows a 3D bar chart representing the RL Distribution for the VSS and VDDIO_PHASE nets. The chart has a vertical axis ranging from 0 to 160,000. A legend on the left lists the nets: VSS and VDDIO_PHASE. Below the chart, a 2D layout view shows the physical placement of components, with a red box highlighting a specific area. The interface includes a menu bar (File, Window, Help), a toolbar, and a sidebar with various analysis options. The bottom status bar shows the following text:

number of Snet on start componet is 0, no Zs(f) calculation
SPICE model generation is completed at 07/03/13 14:37:25. Memory: 121 M, CPU: 127.18 sec
Result is saved into file: C:\SPB-CoSim_3DIC\lab_xcitepi\Interposer\result.

XcitePI – IOME



XcitePI – IOME

Model extraction

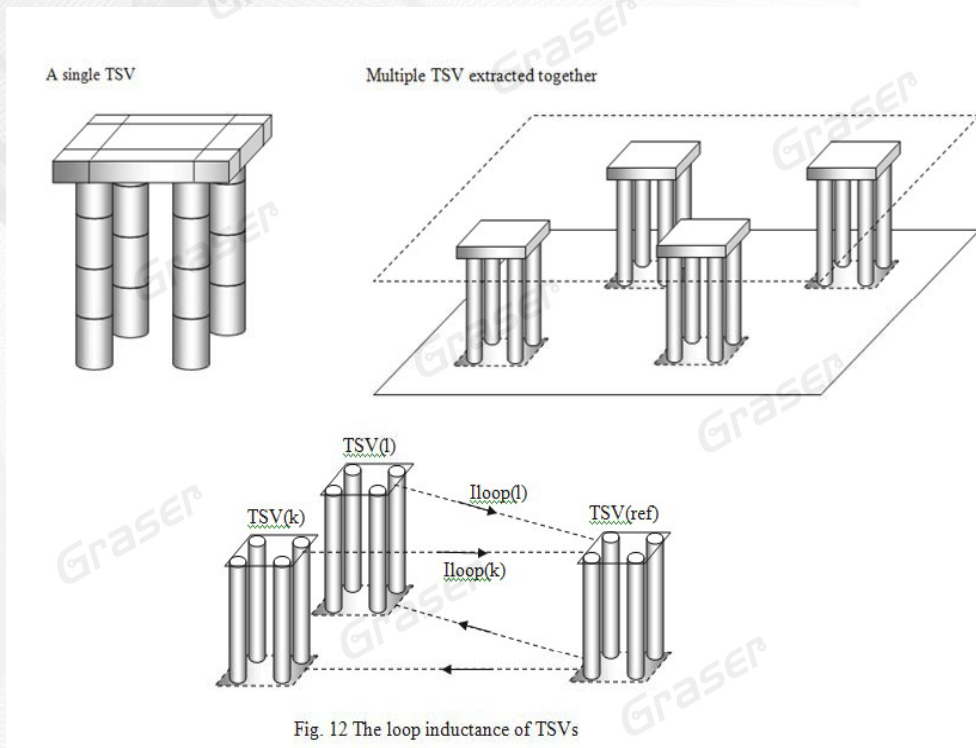
The screenshot displays the XcitePI software interface, which is part of the Cadence ecosystem. The main window shows a circuit layout with two rectangular regions highlighted in blue, containing various colored dots representing components or nodes. The interface includes a menu bar (File, Edit, View, Feature, Window, Help) and a toolbar. On the left, there is a 'Workflow: XcitePI' panel with sections for 'Circuit Setup', 'Output Setup', and 'Performance Assessment'. The 'Output Setup' section is currently active, showing options like 'Spice Netlist', 'Port', and 'Probe'. Below this, the 'View/Export Result' section is visible, listing various analysis options such as 'IO Path Selection', 'Power Net', 'RL Per Bump/Cell', 'RL 2D View', 'RL Histogram View', 'RL Distribution', 'Capacitance (Grid Only)', 'Capacitance (w/On-Die)', 'Impedance (Grid Only)', 'Impedance (w/On-Die)', 'Signal Net', 'RLC Per Bump/Cell', 'RLC 2D View', 'RLC Histogram View', 'RLC Distribution', 'Return/Insertion Loss', 'Save Result', and 'Load Result'. A 'Customize Workflow' button is at the bottom of this panel. In the foreground, two UltraEdit-32 windows are open, displaying the extracted model files. The left window shows the file 'interposer.sp' with the following content:

```
1 * Compact double mesh (CDM) chip model -- generated by XcitePI (V12.0.8)
2 * Created time is at 07/03/13 14:35:18.
3 * Design Name is interposer.
4
5 .SUBCKT interposer
6 + bump68_VSS bump81_VSS bump99_VSS
7 + bump110_VSS bump122_VSS bump132_VSS bump154_VSS
8 + bump162_VSS bump175_VSS bump187_VSS bump217_VSS
9 + bump38_VSS bump75_VSS bump93_VSS bump103_VSS
10 + bump117_VSS bump129_VSS bump153_VSS bump155_VSS
11 + bump169_VSS bump177_VSS bump202_VSS bump225_VSS
12 + bump230_VSS bump43_VSS bump69_VSS bump82_VSS
13 + bump100_VSS bump111_VSS bump123_VSS bump133_VSS
14 + bump137_VSS bump163_VSS bump176_VSS bump196_VSS
15 + bump44_VDDIO_PHASE bump46_VSS bump48_VDDIO_PHASE
16 + bump53_VSS bump57_VDDIO_PHASE bump64_VSS
```

```
1 * Compact double mesh (CDM) chip model (RLCK, IO cell terminals) -- gen
2 * Created time is at 07/03/13 14:35:18.
3 * Design Name is interposer.
4
5 .SUBCKT interposer
6 + bump68_VSS bump81_VSS bump99_VSS
7 + bump110_VSS bump122_VSS bump132_VSS bump154_VSS
8 + bump162_VSS bump175_VSS bump187_VSS bump217_VSS
9 + bump38_VSS bump75_VSS bump93_VSS bump103_VSS
10 + bump117_VSS bump129_VSS bump153_VSS bump155_VSS
11 + bump169_VSS bump177_VSS bump202_VSS bump225_VSS
12 + bump230_VSS bump43_VSS bump69_VSS bump82_VSS
13 + bump100_VSS bump111_VSS bump123_VSS bump133_VSS
14 + bump137_VSS bump163_VSS bump176_VSS bump196_VSS
15 + bump44_VDDIO_PHASE bump46_VSS bump48_VDDIO_PHASE
16 + bump53_VSS bump57_VDDIO_PHASE bump64_VSS
```

The right window shows the file 'interposer_RLCK.sp' with similar content. The status bar at the bottom of the UltraEdit windows indicates '列 1, 行 1, CO', 'DOS', and '修改: 2013/7/3 02:35; 大小: 4423888 插入'.

Published TSV Circuit Modeling

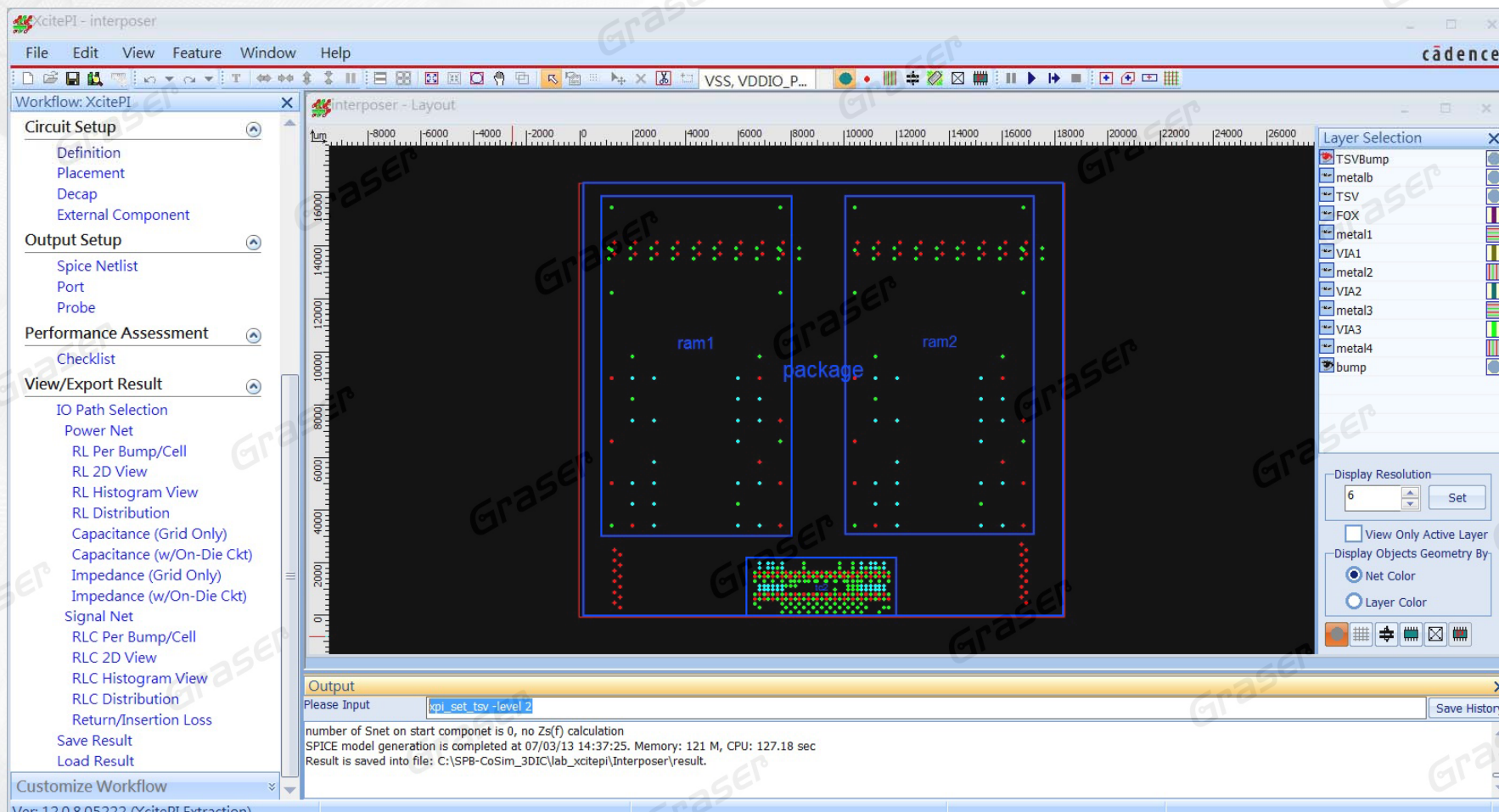


Level 0: DC circuit, only contained R_{via} , used for IR drop analysis or connection testing.	
Level 1: Simple RLC model Have PG loop inductance, capacitance to the substrate, no via-via coupling	
Level 2: Pin based circuit model. Have the L matrix and C matrix based on each TSV branches.	
Level 5: user defined TSV model	

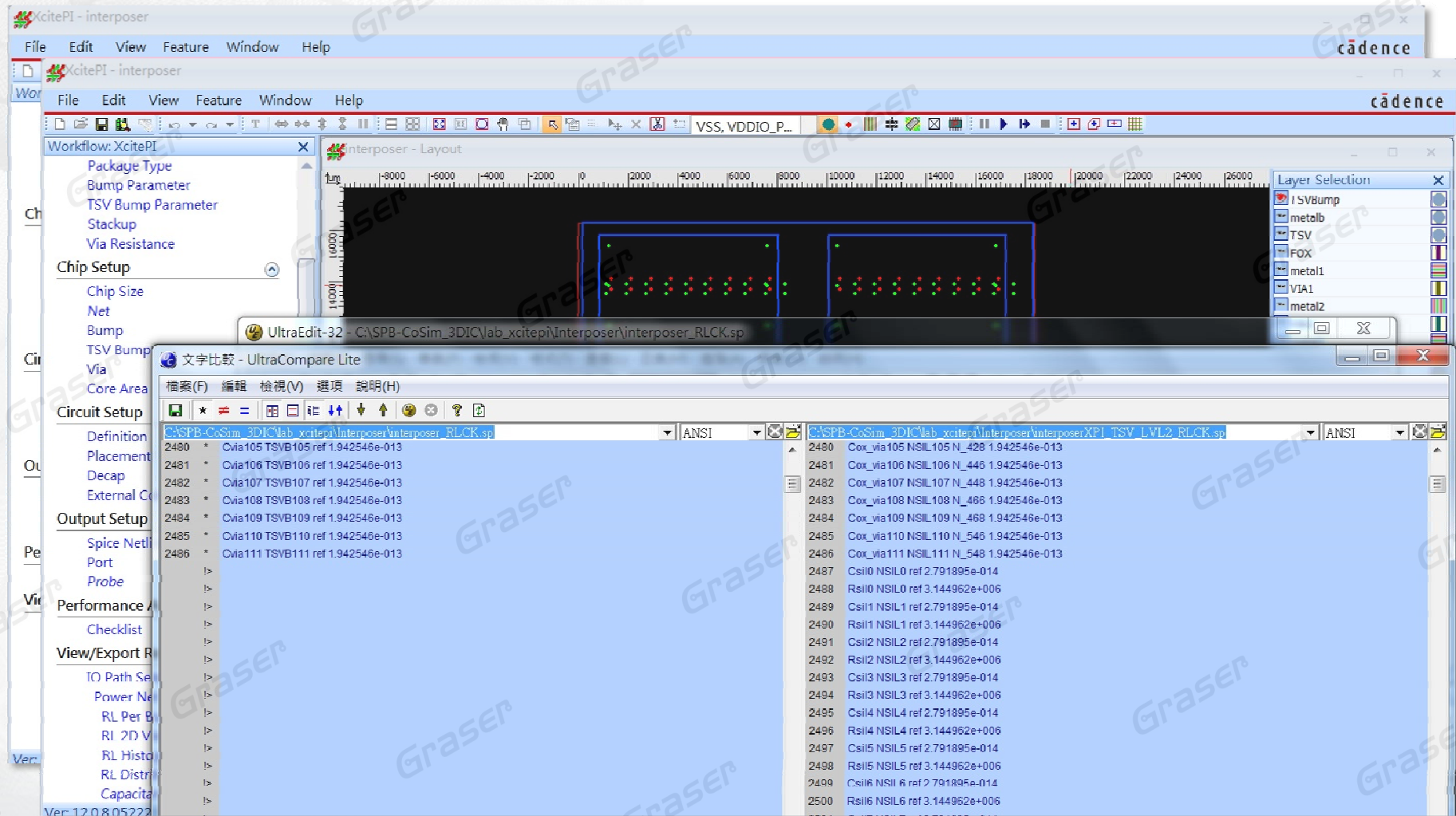
About TSV modeling:

- We didn't calculate each via's partial inductance and mutual inductance. If we do so, that will form a huge circuit matrix that can't be simulated in HSPICE
- We adopt loop calculation. For example, we have n vias, then we have $(n-1)$ loop, then we calculate $(n-1)$ loop and consider coupling between loops. But loop coupling will decay very fast, then final circuit matrix will be small.

Published TSV Circuit Modeling

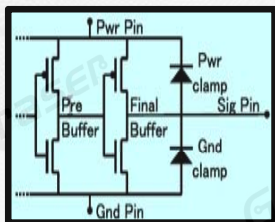


XcitePI - IOME

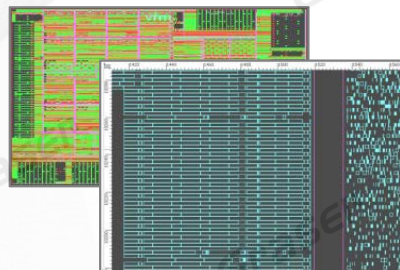


SSO/SSN Analysis with Cadence Solutions

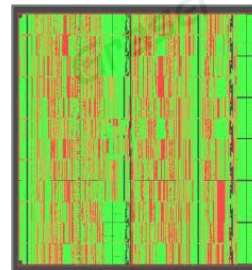
Transistors model



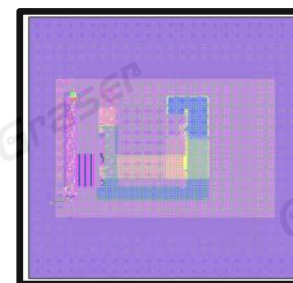
LEF/DEF



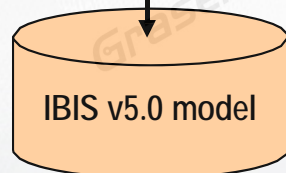
GDS



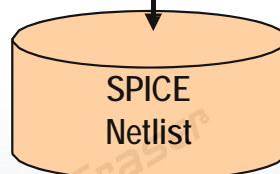
MCM



IBIS model
Conversion with
T2B



IO Model
Extraction with
XcitePI



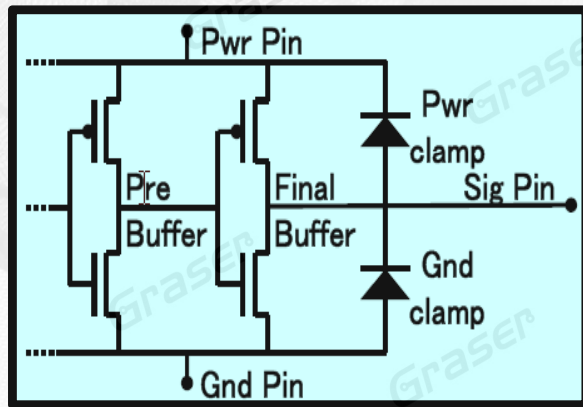
S-parameter extraction
With
PowerSI

BBS model conversion
with passivity guaranteed

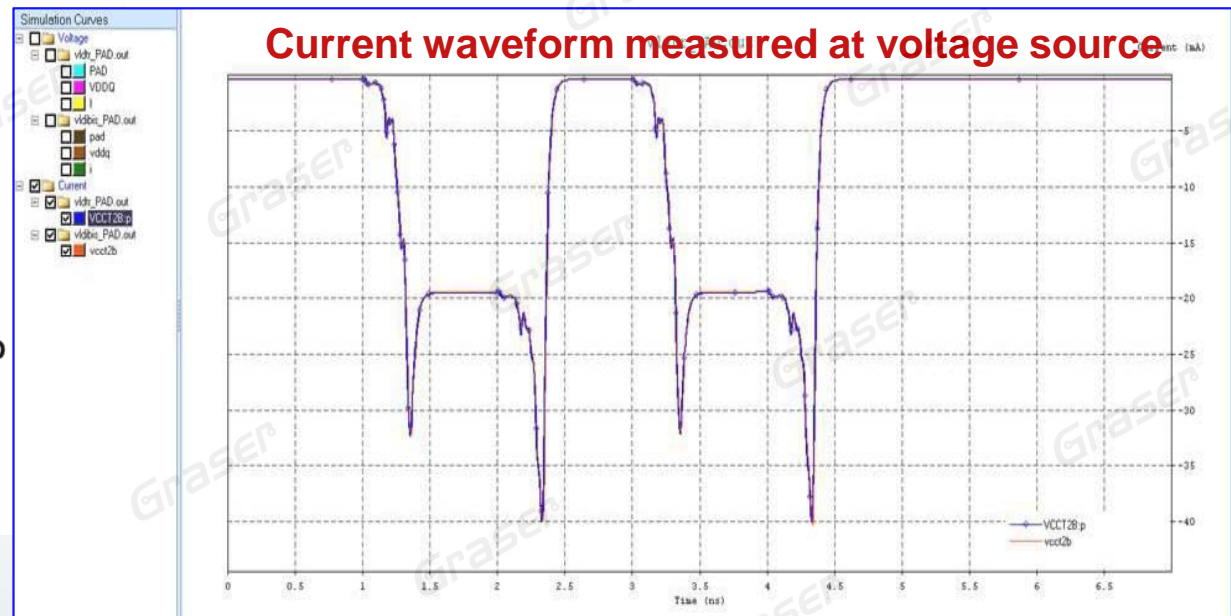
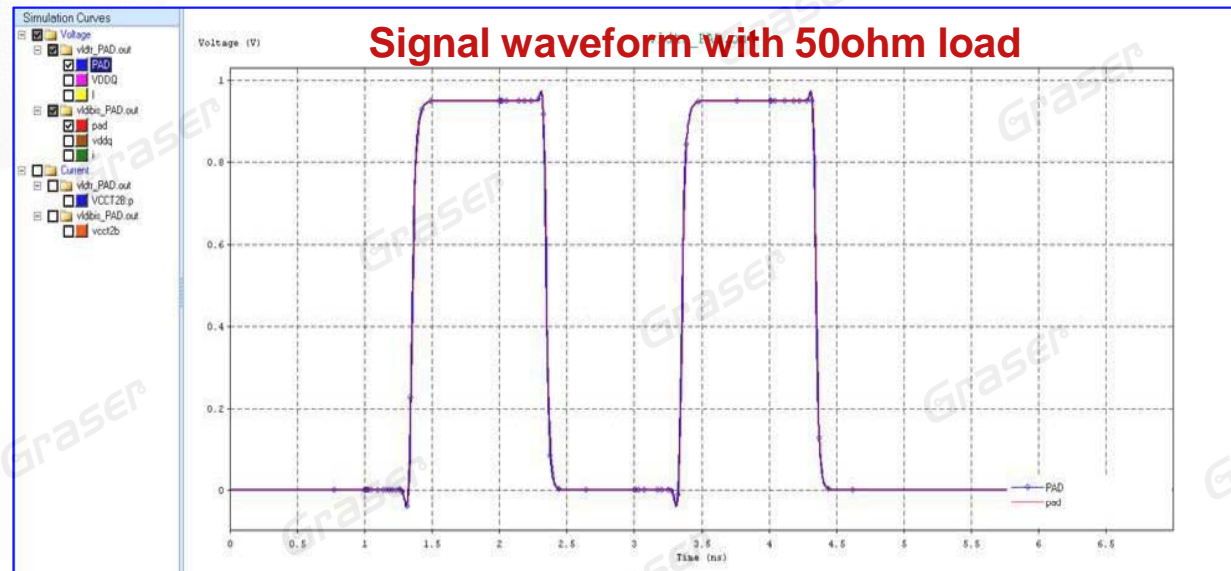
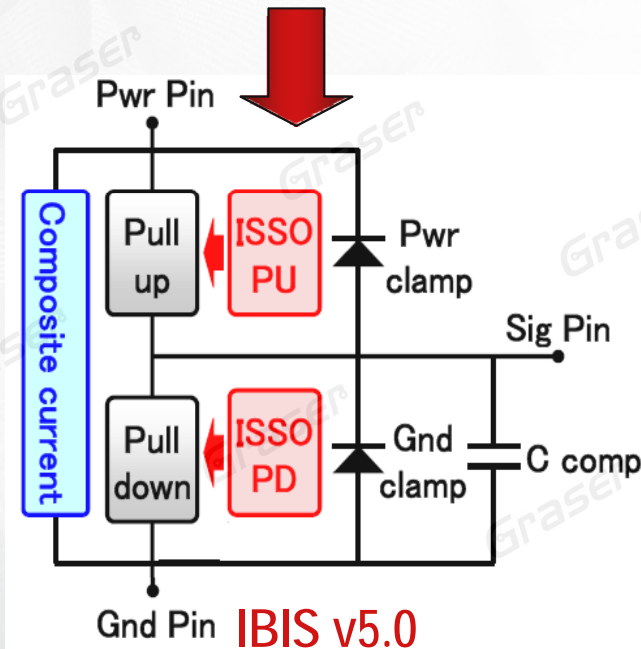


SSN/SSO Analysis in SystemSI

Transistor to IBIS v5.0 Conversion with T2B

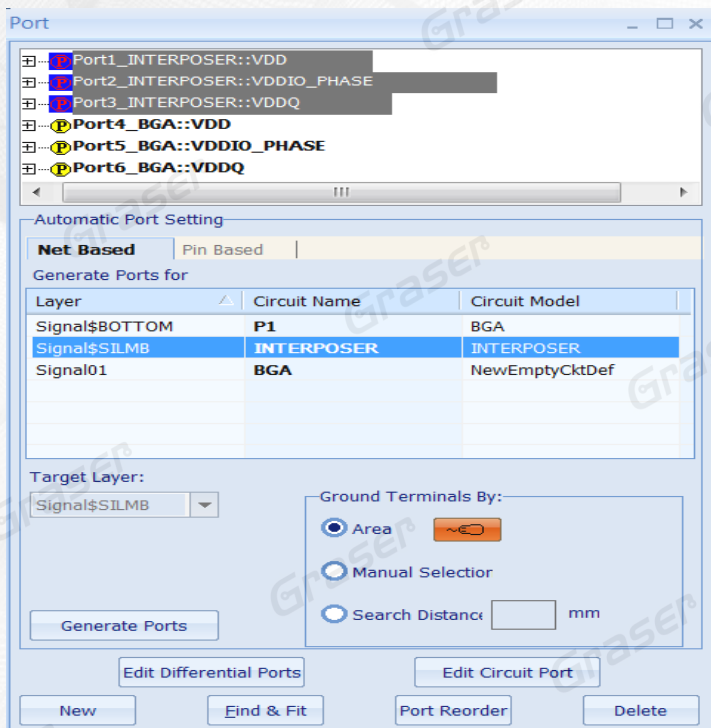


Transistors Model

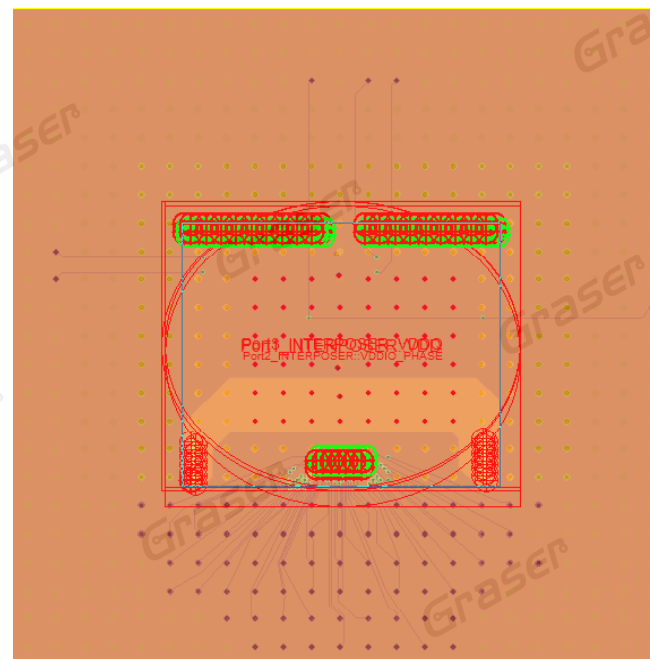


- Voltage and current are good correlated between IBIS and HSPICE

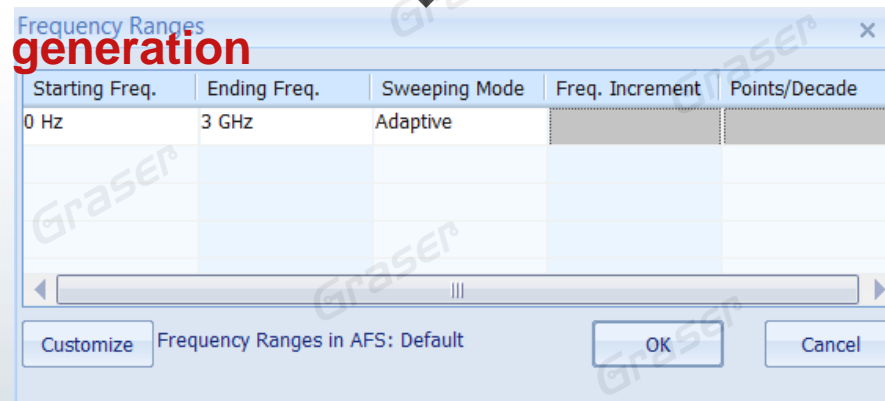
Package S-Parameter Extraction with PowerSI



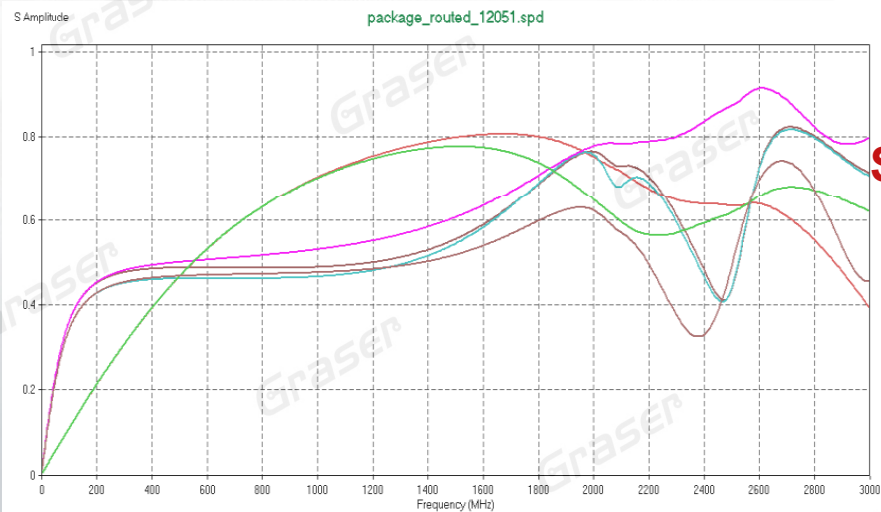
Auto-ports generation



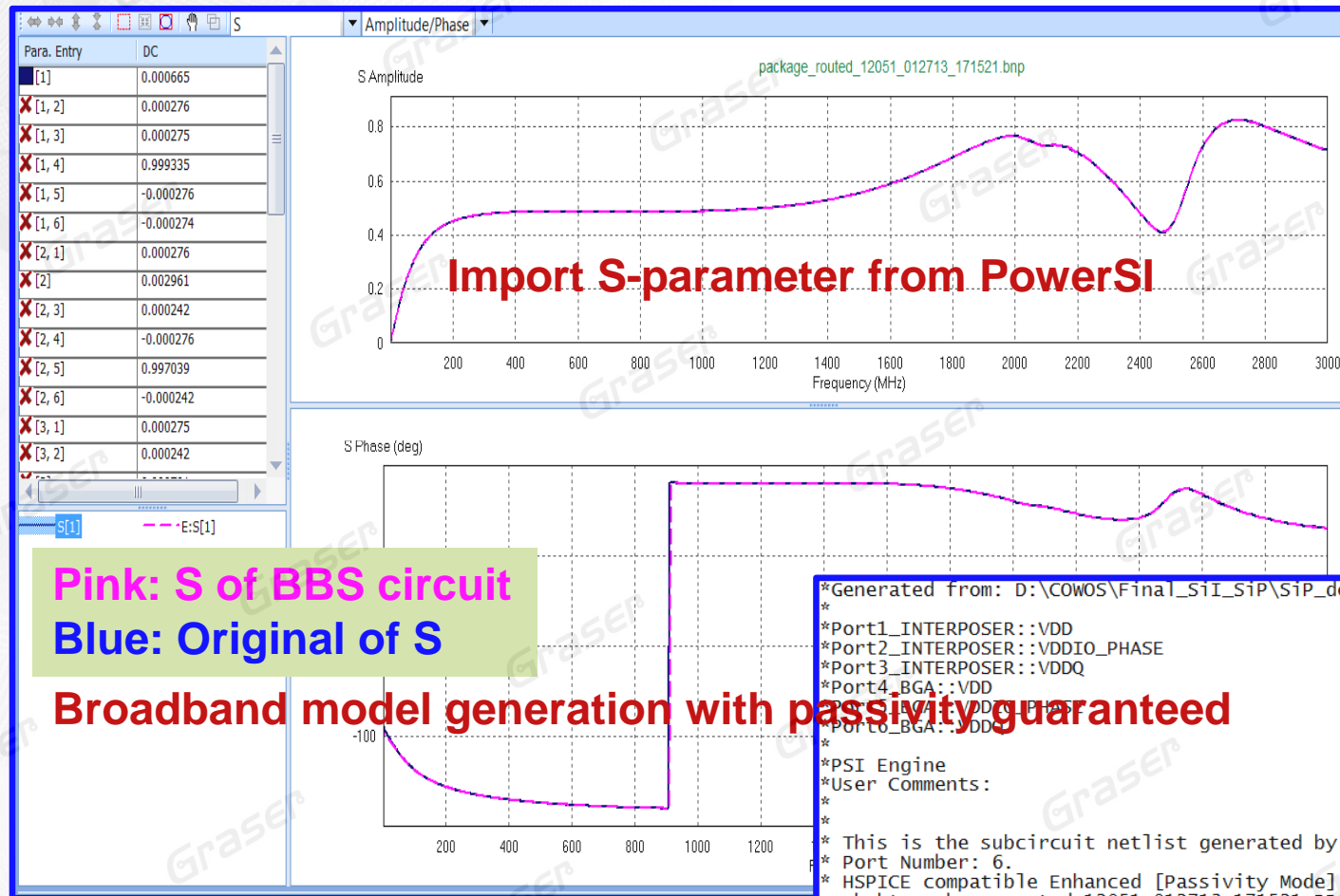
Frequency sweep



S-parameter generation



Broadband Model Conversion with BBS

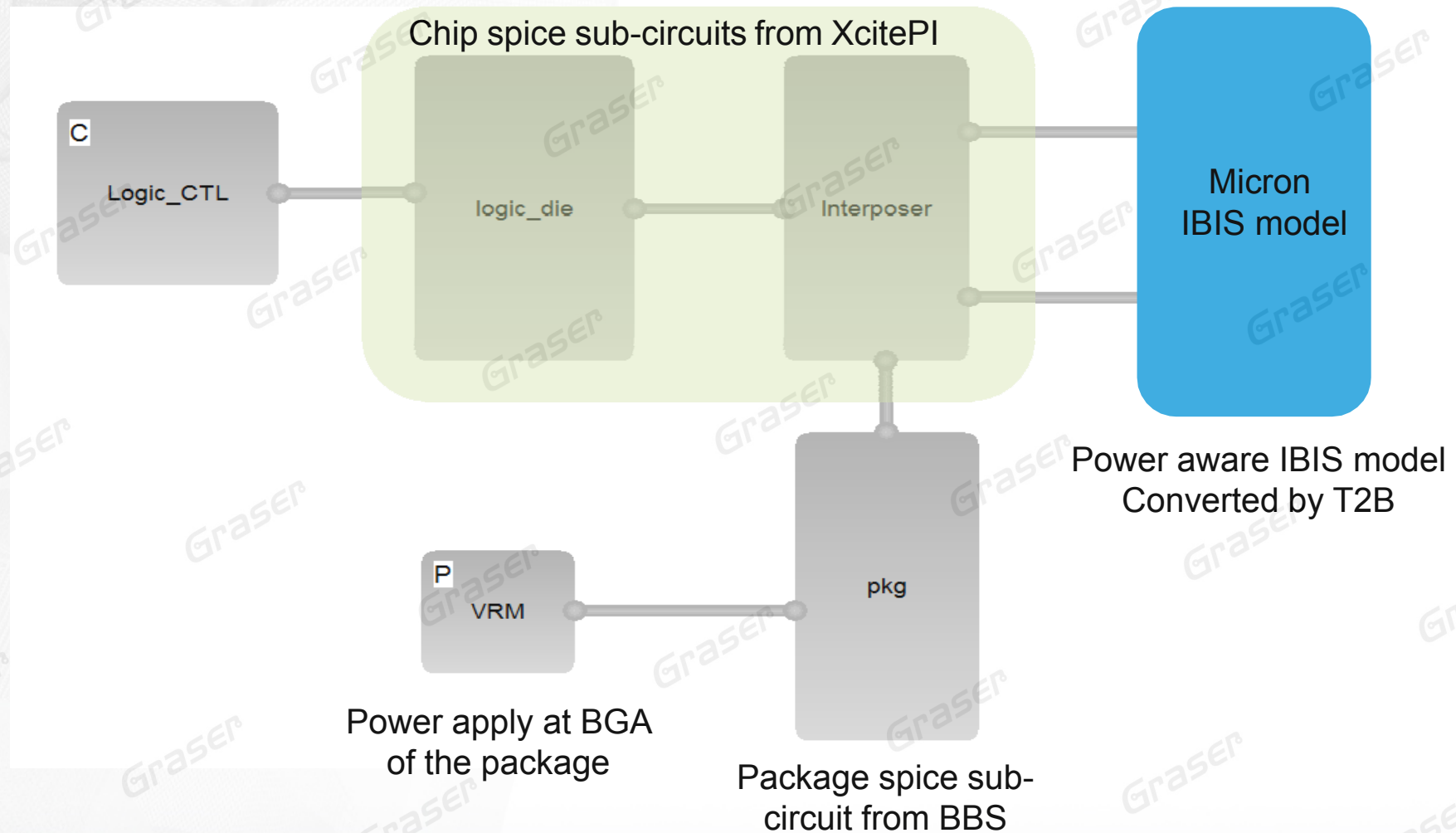


- S-parameter (amplitude and phase) of BBS circuit is almost the same as original S- parameter

```

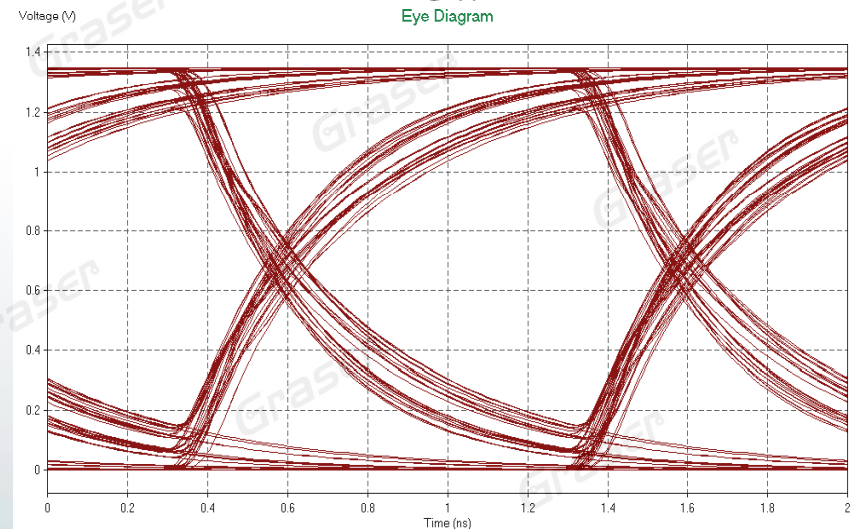
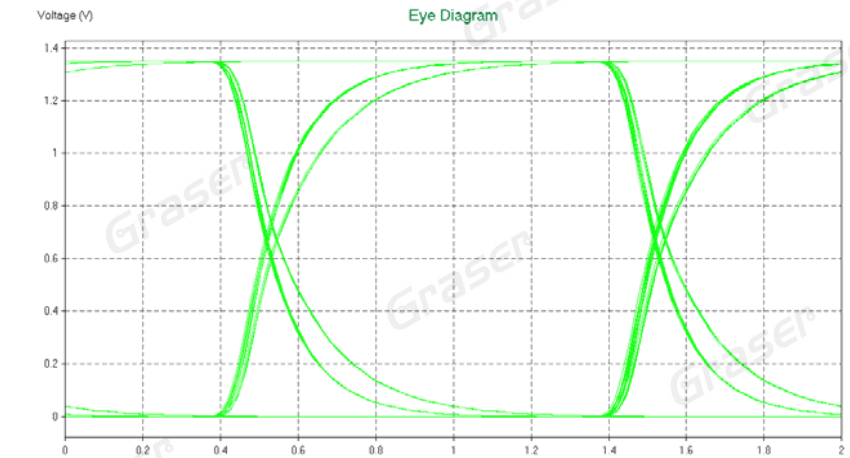
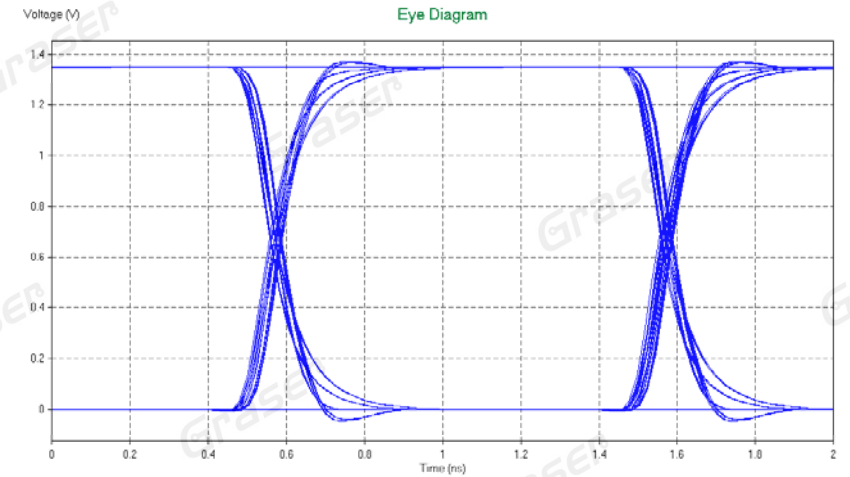
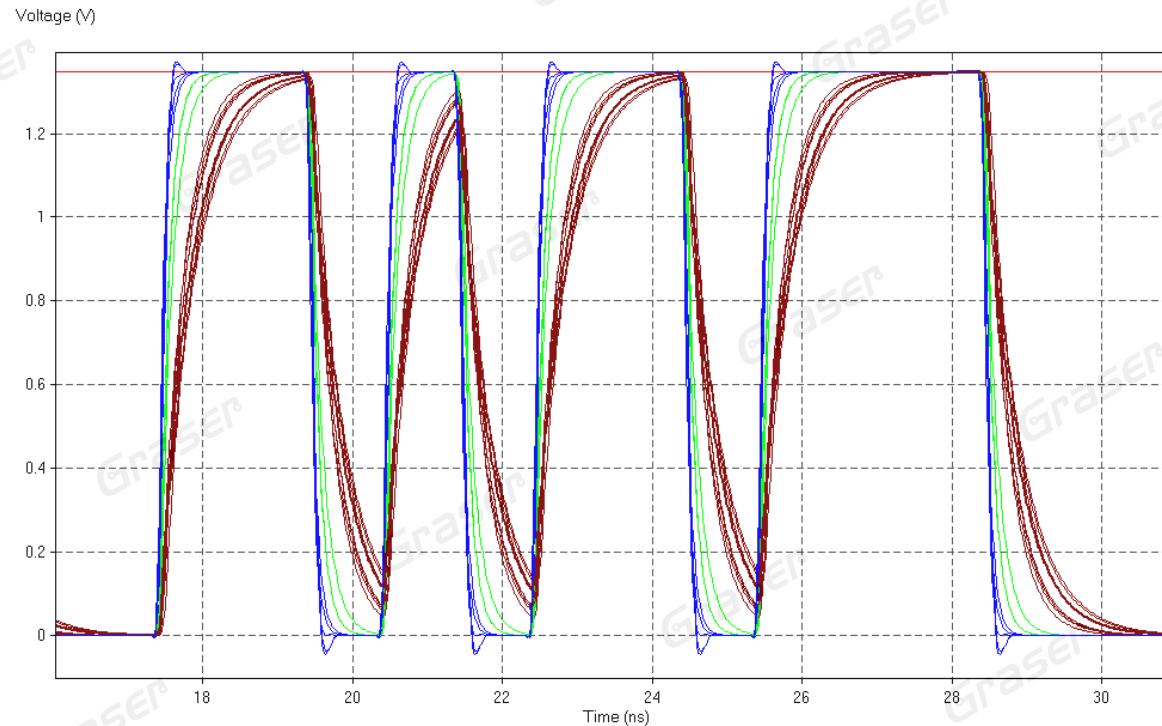
*Generated from: D:\COWOS\Final_SiI_SiP\SiP_design_final\package_routed_12051.spd
*
*Port1_INTERPOSER::VDD
*Port2_INTERPOSER::VDDIO_PHASE
*Port3_INTERPOSER::VDDQ
*Port4_BGA::VDD
*Port5_VDDIO_PHASE
*Port6_BGA::VDDQ
*
*PSI Engine
*User Comments:
*
* This is the subcircuit netlist generated by Sigrity Broadband SPICE v12.0.7.11261
* Port Number: 6.
* HSPICE compatible Enhanced [Passivity Mode]
.subckt package_routed_12051_012713_171521_BBSckt 1 2 3 4 5 6 ref
Rd1_1 7 ref 1.000000
Rd1_2 8 ref 0.500000
Vd1 1 7 0
F1 ref 8 vd1 1.0 1
G1 ref 8 1 ref
Rd2_1 9 ref 1.000000
Rd2_2 10 ref 0.500000
Vd2 2 9 0
F2 ref 10 vd2 1.0 1
G2 ref 10 2 ref
Rd3_1 11 ref 1.000000
Rd3_2 12 ref 0.500000
Vd3 3 11 0
F3 ref 12 vd3 1.0 1
G3 ref 12 3 ref
Rd4_1 13 ref 1.000000
Rd4_2 14 ref 0.500000
    
```

SSO/SSN Analysis with SystemSI



- Blocked based topology editor with SPICE sub-circuits modeling approach
- I/O modeling flexibility for power-aware IBIS and transistor level circuits

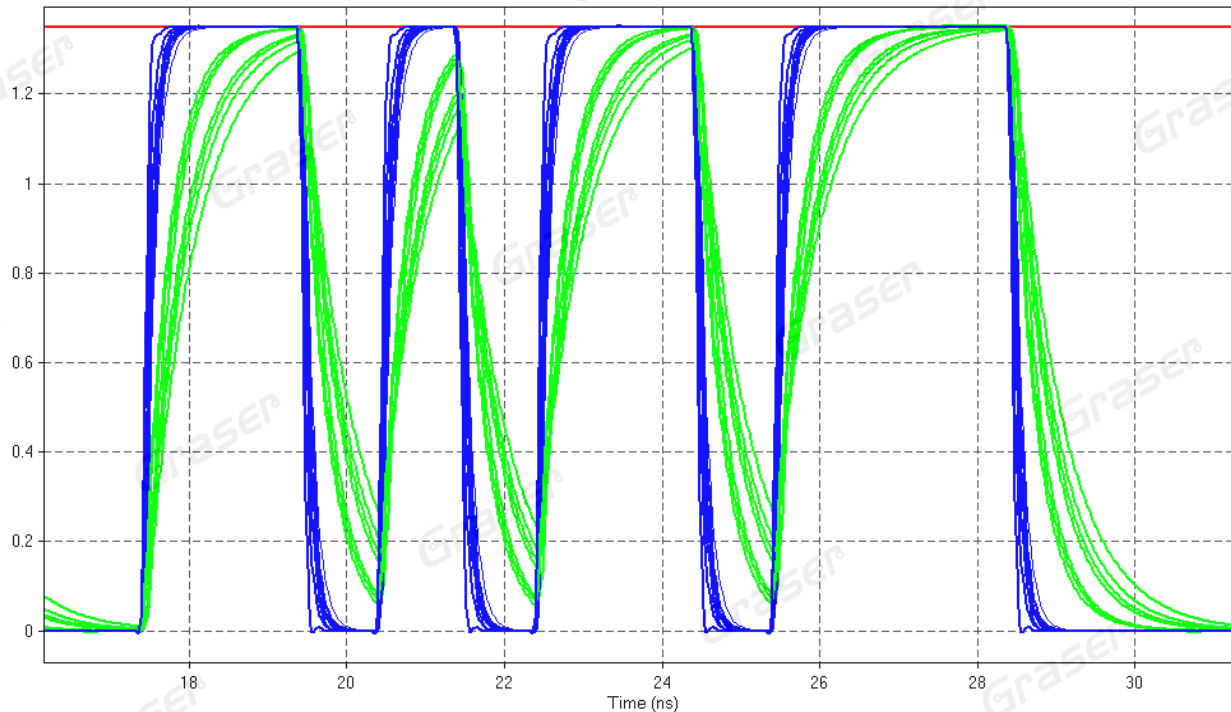
Simulation Result-Ideal PDN for DQ[0:15]



- It is obviously that rise/fall slew rate categorizes to 3 groups.
- Slower charge and dis-charge on load that make signal can't reach to full high and low state.
- Will large RC of signals impact jitter and eye opening a lots?

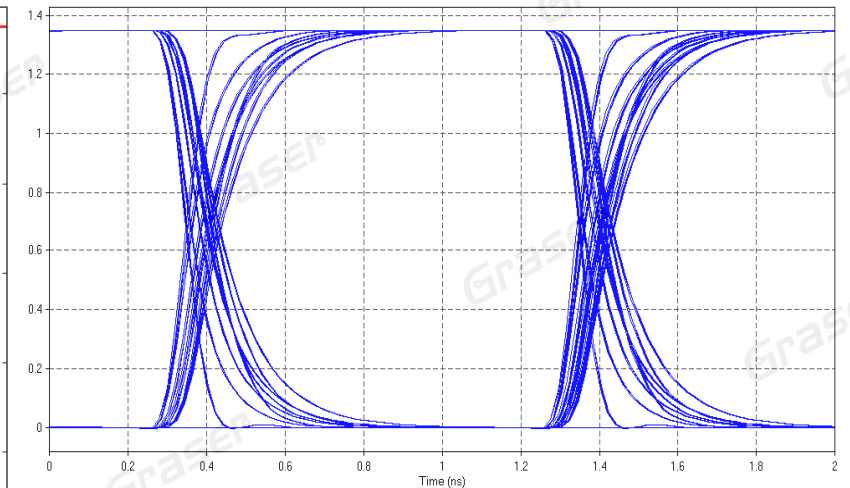
Simulation Result-Ideal PDN for DQ[16:30]

Voltage (V)



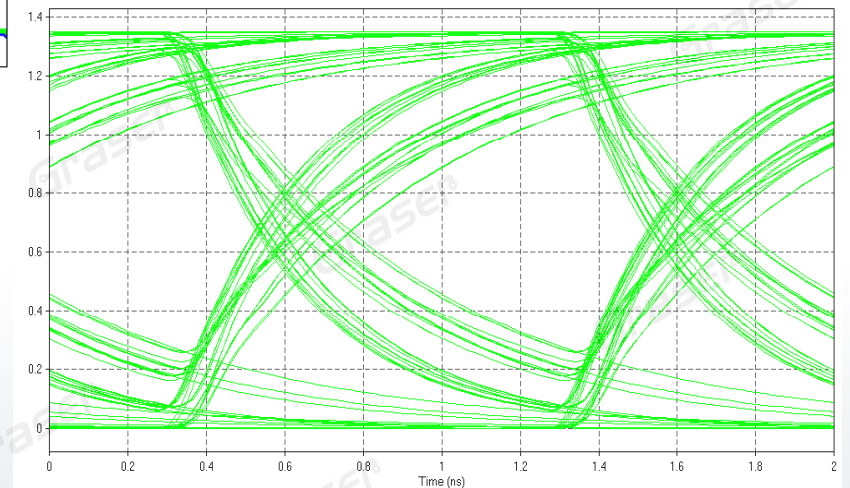
Voltage (V)

Eye Diagram



Voltage (V)

Eye Diagram



- The signal route from TC2 to mem2 has more worse signal quality than TC2 to mem1

Simulation Result-RLC Extraction For DQ[0:15]

Bump name	Net	R(Ohm)	L(nH)	C(pF)
bump293_PP_DQ_DDR[6]	PP_DQ_DDR[6]	48.4694	3.2797	0.561401
bump281_PP_DQ_DDR[2]	PP_DQ_DDR[2]	49.959	3.31472	0.589096
bump241_PP_DQ_DDR[11]	PP_DQ_DDR[11]	55.7621	2.30635	0.373289
bump245_PP_DQ_DDR[13]	PP_DQ_DDR[13]	57.4191	1.29754	0.186612
bump249_PP_DQ_DDR[15]	PP_DQ_DDR[15]	83.3328	1.63575	0.185425
bump236_PP_DQ_DDR[0]	PP_DQ_DDR[0]	105.21	3.66265	0.558155
bump289_PP_DQ_DDR[4]	PP_DQ_DDR[4]	116.763	4.43087	0.684715
bump299_PP_DQ_DDR[9]	PP_DQ_DDR[9]	124.84	3.16693	0.500917
bump295_PP_DQ_DDR[7]	PP_DQ_DDR[7]	279.983	6.35549	0.917687
bump259_PP_DQ_DDR[1]	PP_DQ_DDR[1]	293.068	6.12851	0.775298
bump297_PP_DQ_DDR[8]	PP_DQ_DDR[8]	307.619	5.75101	0.685041
bump243_PP_DQ_DDR[12]	PP_DQ_DDR[12]	315.273	4.19995	0.418102
bump247_PP_DQ_DDR[14]	PP_DQ_DDR[14]	315.385	4.81455	0.572413
bump287_PP_DQ_DDR[3]	PP_DQ_DDR[3]	317.473	6.46446	0.821224
bump239_PP_DQ_DDR[10]	PP_DQ_DDR[10]	328.795	5.68991	0.651809
bump291_PP_DQ_DDR[5]	PP_DQ_DDR[5]	346.292	7.07552	0.878386

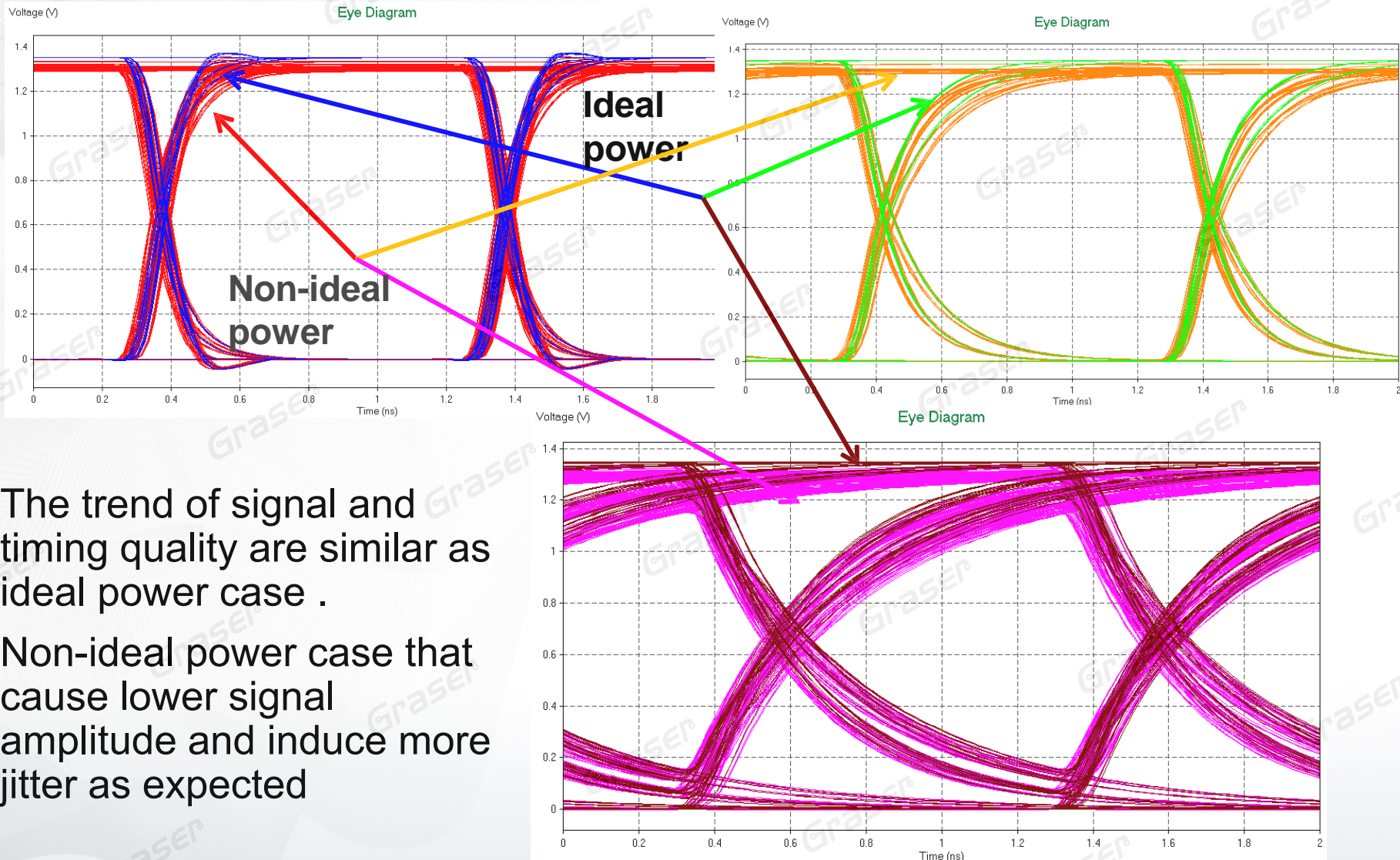
- During the SPICE model extraction by XcitePI, RLC values are generated as well.
- Resistance of each net reflects the length and width of RDL route.
- Improper placement of TC2 and mem dies that cause RDL length discrepancy significantly and lead to large discrepancy in RL value.
- Large RC values that maps to worse signal quality and timing margin.

Simulation Result-RLC Extraction For DQ[16:30]

Bump name	Net	R(Ohm)	L(nH)	C(pF)
bump283_PP_DQ_DDR[30]	PP_DQ_DDR[30]	34.3671	1.42753	0.247769
bump277_PP_DQ_DDR[28]	PP_DQ_DDR[28]	58.0473	1.36851	0.196704
bump273_PP_DQ_DDR[26]	PP_DQ_DDR[26]	70.1409	2.32963	0.396866
bump263_PP_DQ_DDR[21]	PP_DQ_DDR[21]	79.503	3.91352	0.827598
bump269_PP_DQ_DDR[24]	PP_DQ_DDR[24]	80.3488	3.00485	0.495025
bump257_PP_DQ_DDR[19]	PP_DQ_DDR[19]	80.6993	3.36821	0.599283
bump267_PP_DQ_DDR[23]	PP_DQ_DDR[23]	106.942	4.24413	0.678631
bump253_PP_DQ_DDR[17]	PP_DQ_DDR[17]	122.531	4.07635	0.61541
bump285_PP_DQ_DDR[31]	PP_DQ_DDR[31]	221.814	3.28349	0.438711
bump271_PP_DQ_DDR[25]	PP_DQ_DDR[25]	253.277	4.68389	0.50802
bump279_PP_DQ_DDR[29]	PP_DQ_DDR[29]	282.102	4.01578	0.343756
bump251_PP_DQ_DDR[16]	PP_DQ_DDR[16]	296.592	5.92323	0.80677
bump255_PP_DQ_DDR[18]	PP_DQ_DDR[18]	330.227	6.67474	0.857893
bump265_PP_DQ_DDR[22]	PP_DQ_DDR[22]	333.358	6.71043	0.831939
bump261_PP_DQ_DDR[20]	PP_DQ_DDR[20]	366.846	6.87882	0.975814
bump275_PP_DQ_DDR[27]	PP_DQ_DDR[27]	469.645	5.39636	0.44823

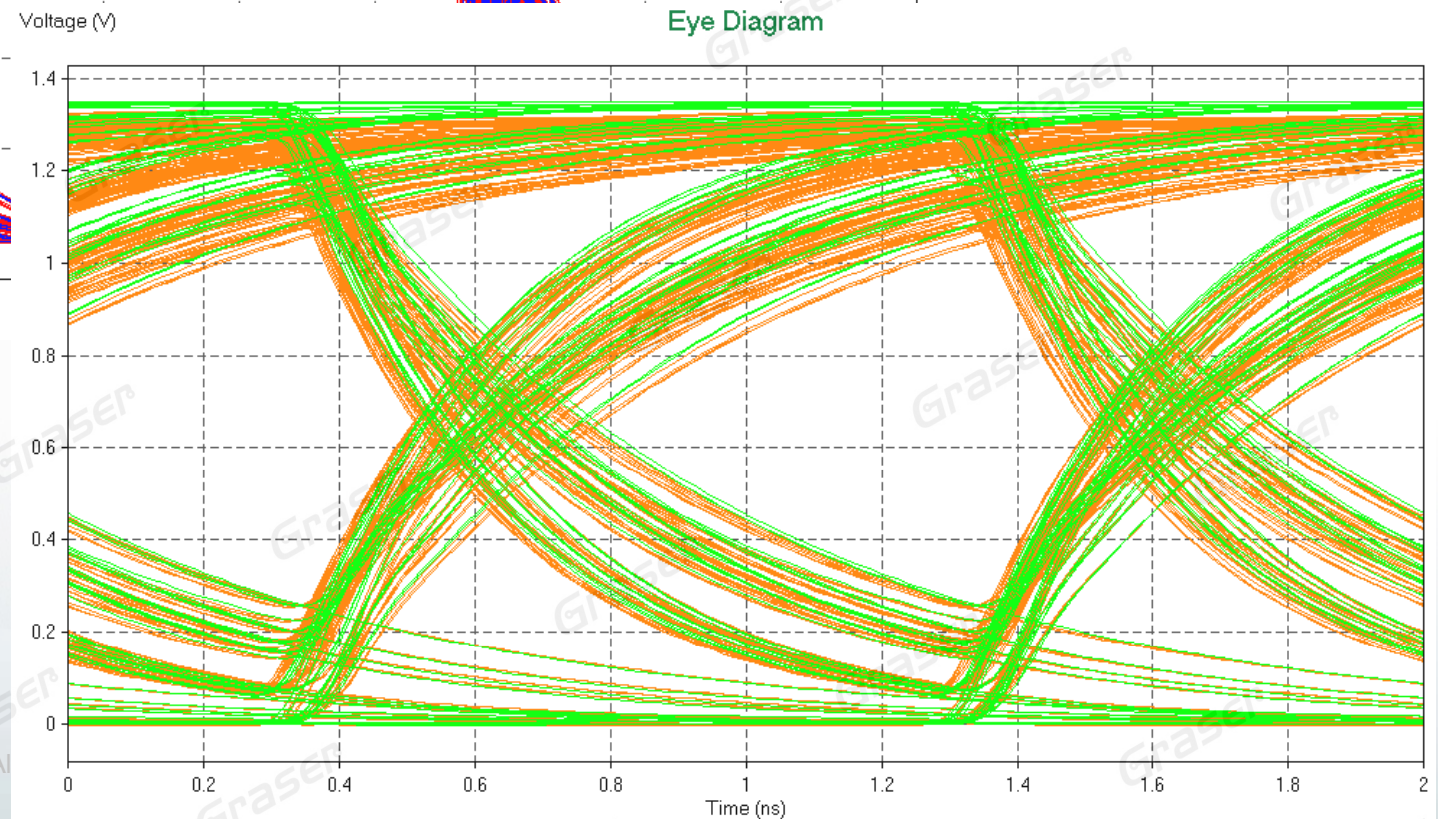
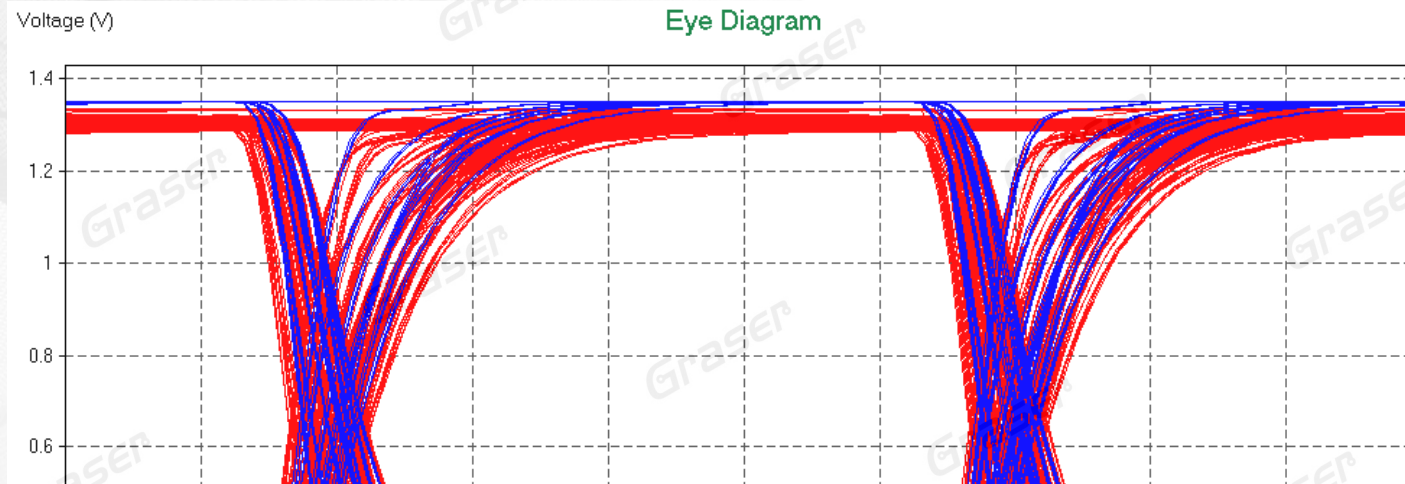
- Comparing with TC2 to mem1 route, TC2 to mem2 is more worse in RLC
- This also leads to more worse signal and timing quality than TC2 to mem1 data group.

Simulation Result-Non-Ideal Power Comparison DQ[0:15]



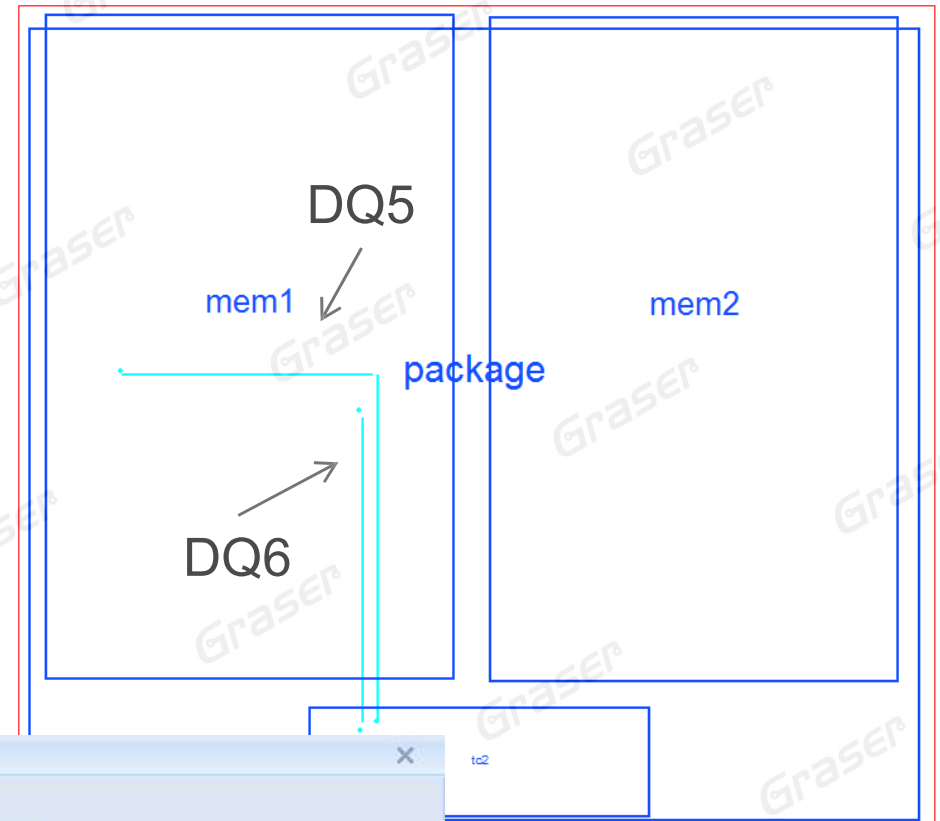
- The trend of signal and timing quality are similar as ideal power case .
- Non-ideal power case that cause lower signal amplitude and induce more jitter as expected

Simulation Result--Non-Ideal Power Comparison DQ[0:15]



What If Analysis

- DQ5 has longer RDL length than DQ6.
- On metal4, both signals have the same metal width.
- The width of DQ5 on metal3 is just 1/10 of DQ5/DQ6 on metal4
- Change width of DQ5 to get lower resistance
- Capacitance of DQ5 is higher than original



BBox Property

Net: PP_DQ_DDR[5] Unit: nm

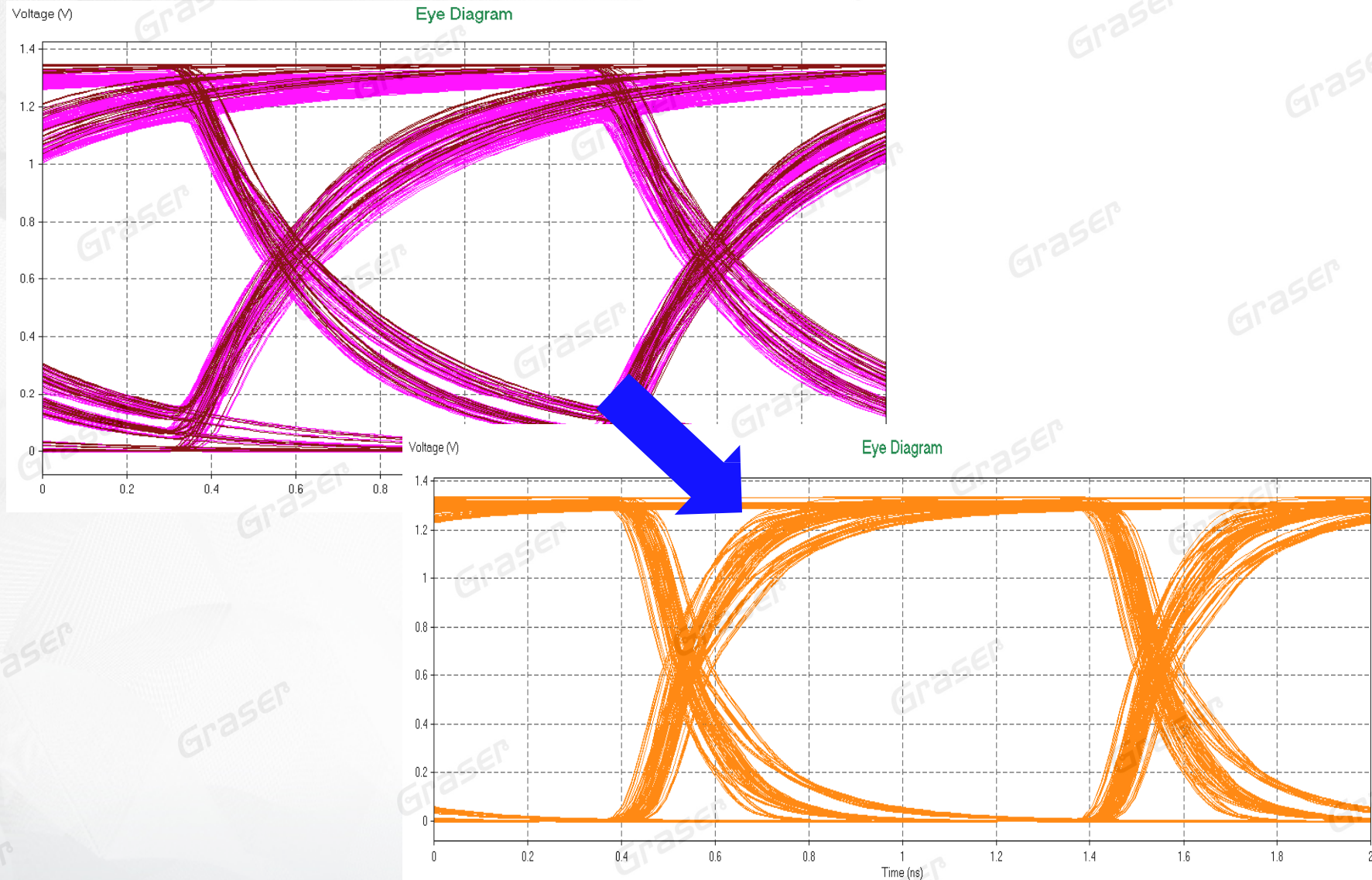
Left: 2059200 Top: 9013800

Right: 7099600 Bottom: 9010800

OK Cancel

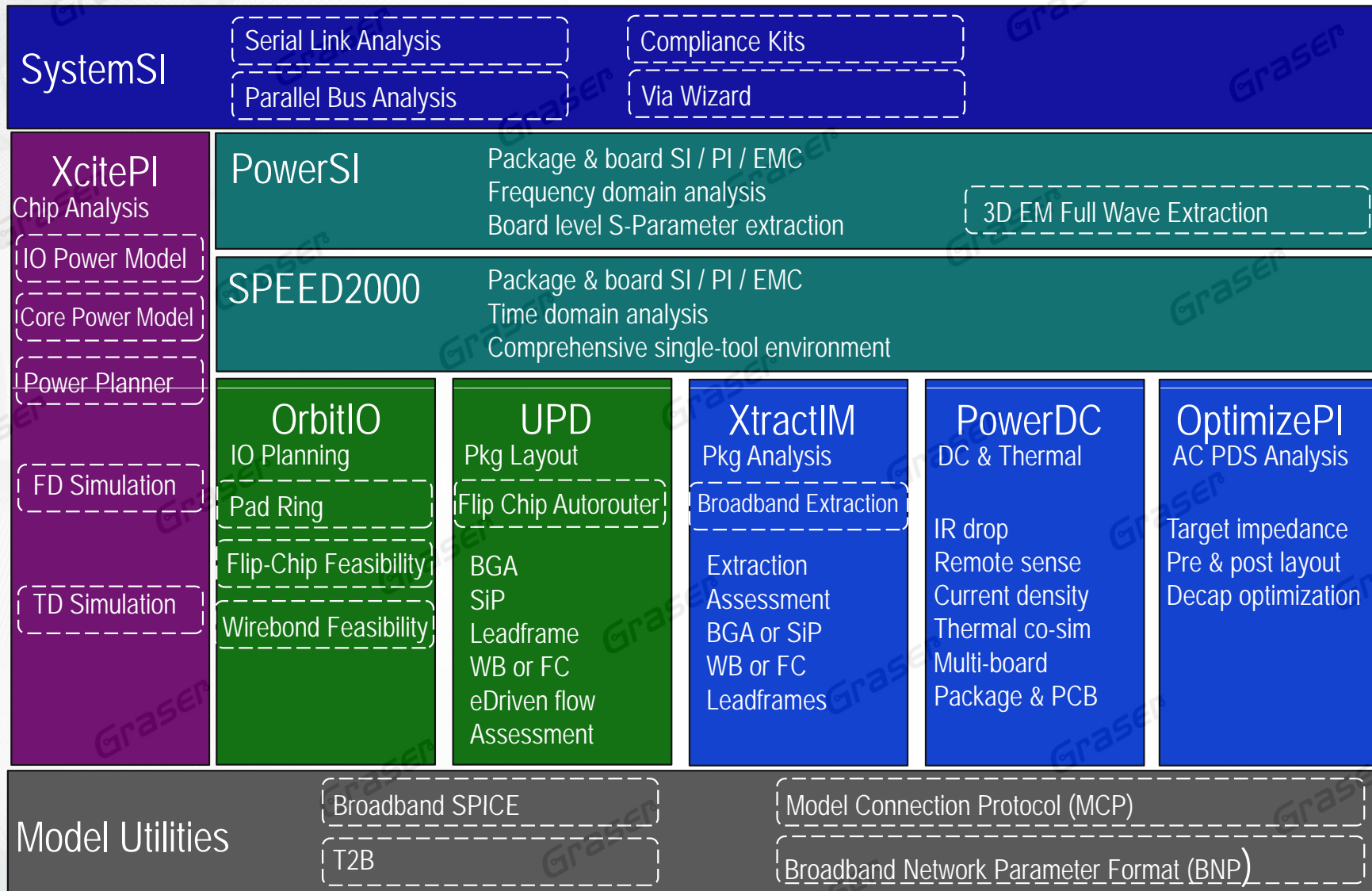
Bump name	Net	R(Ohm)	L(nH)	C(pF)
bump291_PP_DQ_DDR[5]	PP_DQ_DDR[5]	99.808	5.97765	1.16981
bump293_PP_DQ_DDR[6]	PP_DQ_DDR[6]	48.4694	3.2797	0.735876

What If Analysis



- After changing width for DQ[1,3,5,7,8,12,14,10], we can see that the eye opening has great improved.

Cadence Sigrity Products



■ System Level Die-to-Die
 ■ General PCB & Package Analysis
 ■ Customized PCB & Package Analysis
 ■ Package Physical Design
 ■ Chip Analysis
 ■ Model Utilities