

# Simple Transistor to Behavior Model Conversion

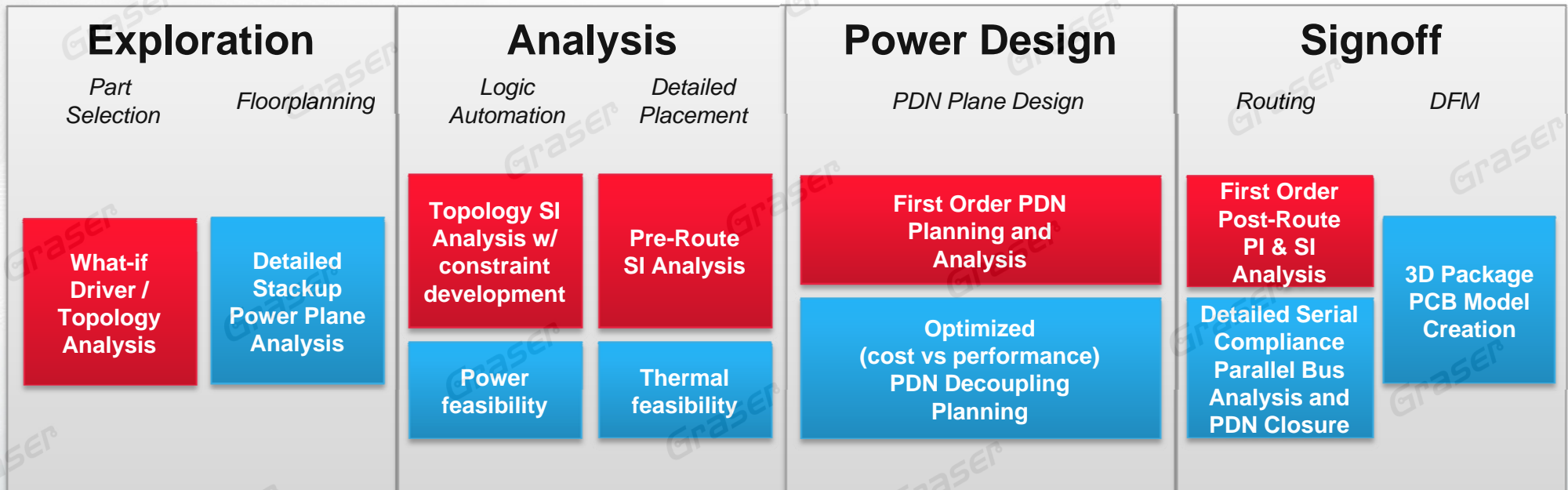
Eric Chen

13/Aug/2013

# Allegro / Virtuoso / EPS with Sigrity

- Comprehensive Front-to-Back Solution
- Better Together

Single vendor Front-to-Back flow: design, verification, analysis, and compliance closure  
For emerging gigabit design challenges  
Focus on High-end Consumer and Data-center Infrastructure verticals  
Integrated 3D solvers for chip, package and board



+



> 2

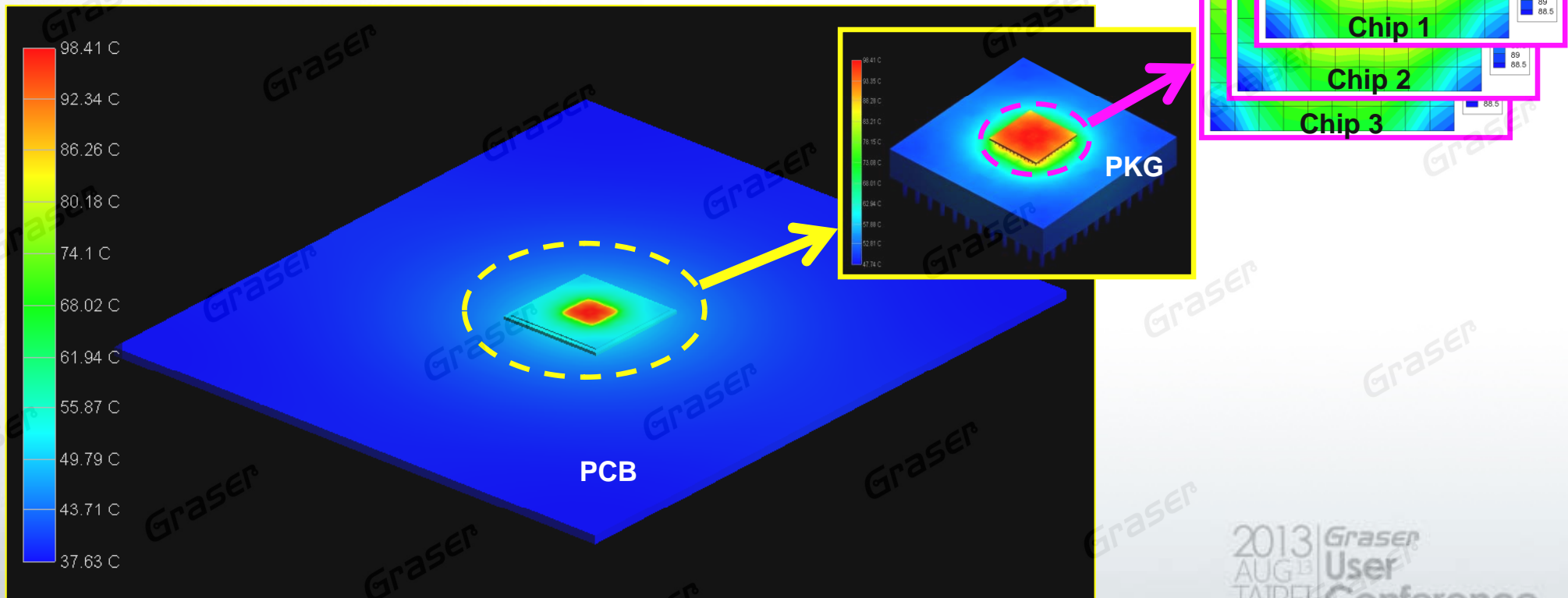
2013 AUG 13  
TAIPEI Graser User Conference

# Digital IC - Sigrity EPS + PowerDC



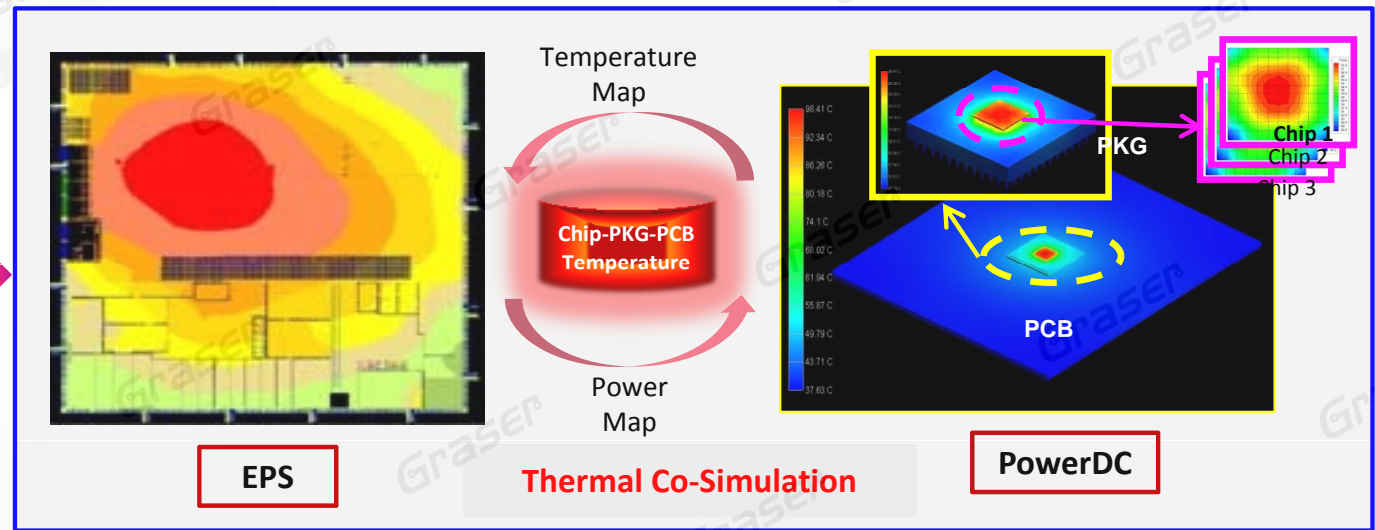
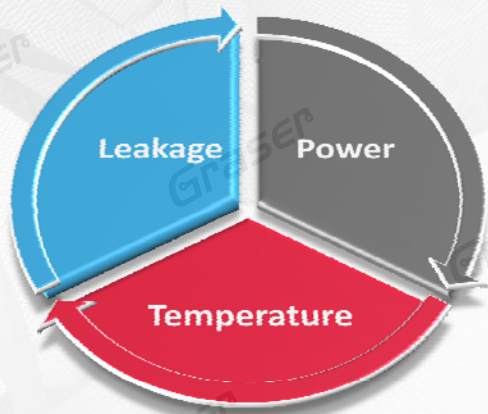
# Overview

- EPS + PowerDC → Electrical/Thermal Co-Simulation of 3D IC
  - EPS generates temperature and location dependent power maps
  - PowerDC computes detailed temperature distribution of dies, interposer, package, and board
- Physics Based 3D Thermal Simulation
  - Each and every vias, wires, balls, and bump are modeled explicitly
  - Considers both Joule heating and component heating





# Electrical-Thermal Co-Simulation



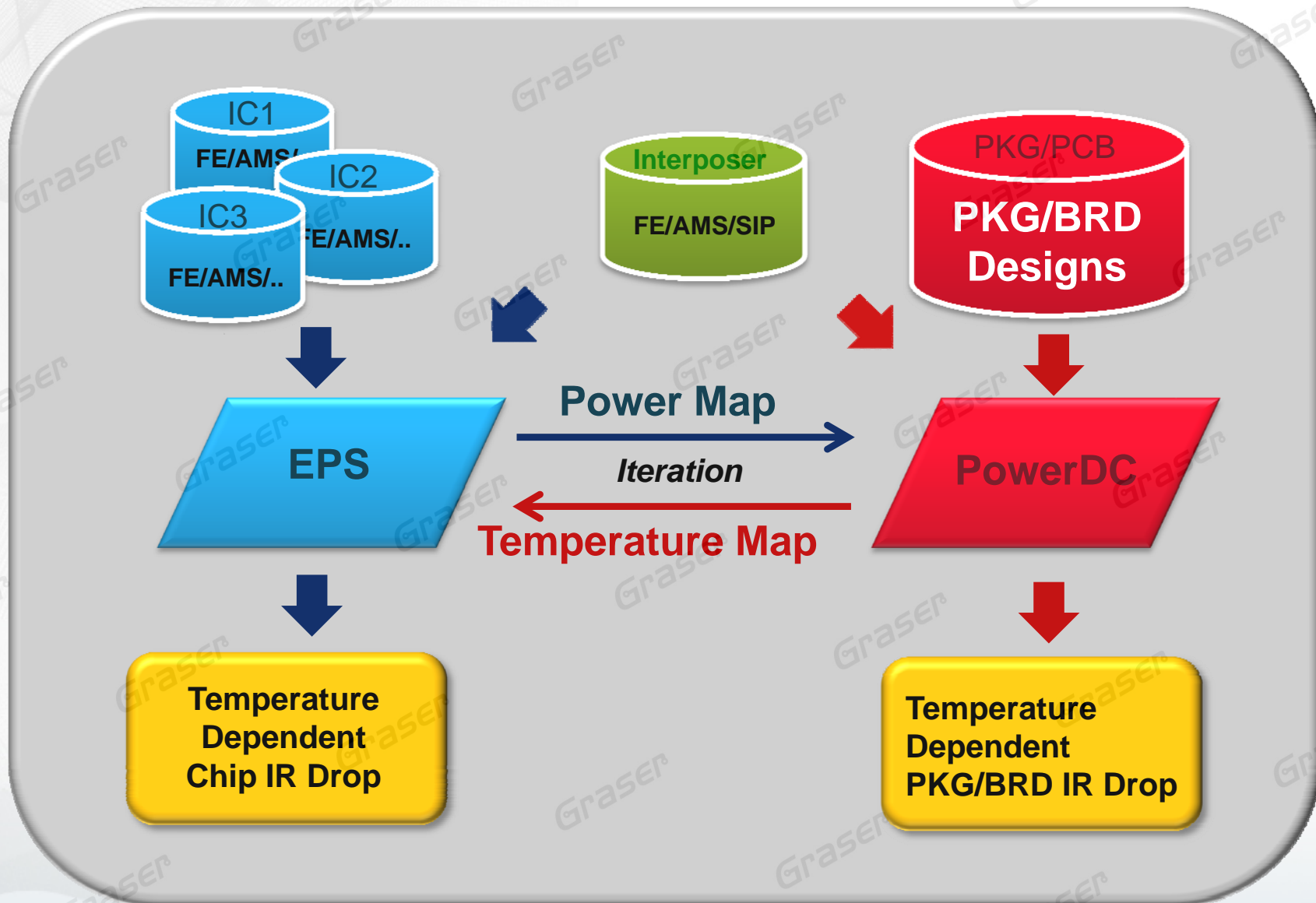
- **Thermal Runaway**

- Positive feedback and interaction among chip's temperature, leakage and power dissipation
- Temperature-dependent EMIR failures

- **Physics Based 3D Thermal Simulation in “EPS + Sigrity PowerDC”**

- EPS generates temperature and location dependent “Power Map” file
- PowerDC computes detailed temperature distribution for Chip-PKG-PCB and sends back “Temperature Map” file to EPS for more iteration and convergence
- Thermal view is available in 2D/3D for interposer and full 3DIC systems.

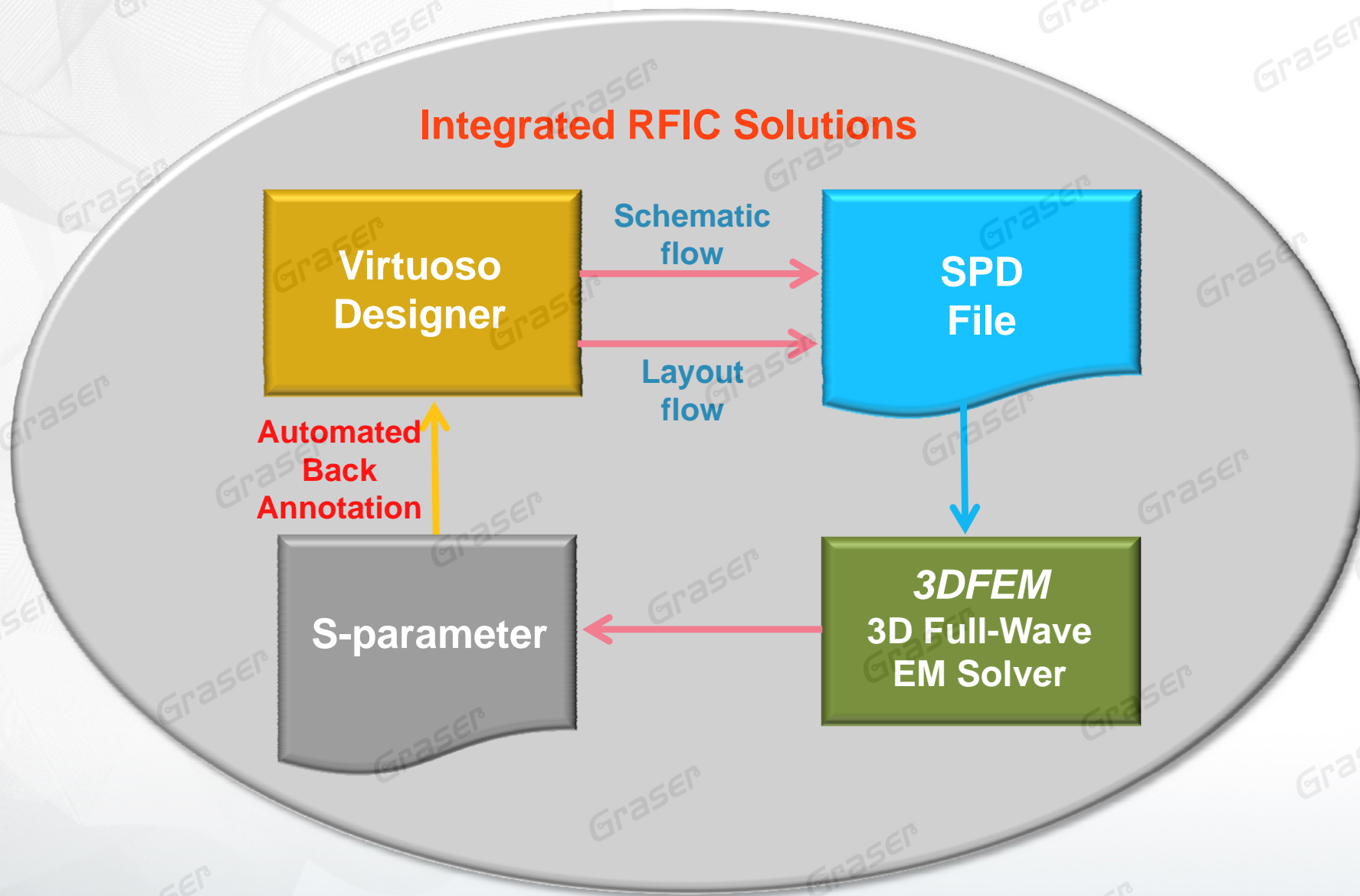
# CoWoS Thermal Simulation Flow



# Custom IC - Sigrity Virtuoso + PowerDC



# Seamless Integration



# Schematic Flow

The screenshot displays the RF Designer software interface. The main window shows a schematic diagram of a circuit with two ports, P1 and P2, and various components like inductors, capacitors, and a central component labeled 'Cout'. A red box highlights the text: "Access solver directly from the schematic. select nets and components off the schematic". Another red box highlights the "Solver" menu, which is open, showing options: "Setup", "Net Constraints...", "Solver", and "About...". The "Solver" sub-menu is also open, showing options: "Setup Extraction Groups...", "Setup Process...", "Setup Ports...", "Show Extraction...", and "Manage States...". The text "Solver menu" is written next to the Solver menu. The status bar at the bottom shows mouse coordinates and object properties.

Tools Design Window Edit Add Check Sheet Options Migrate RF Designer Help

Setup  
Net Constraints...  
Solver  
About...

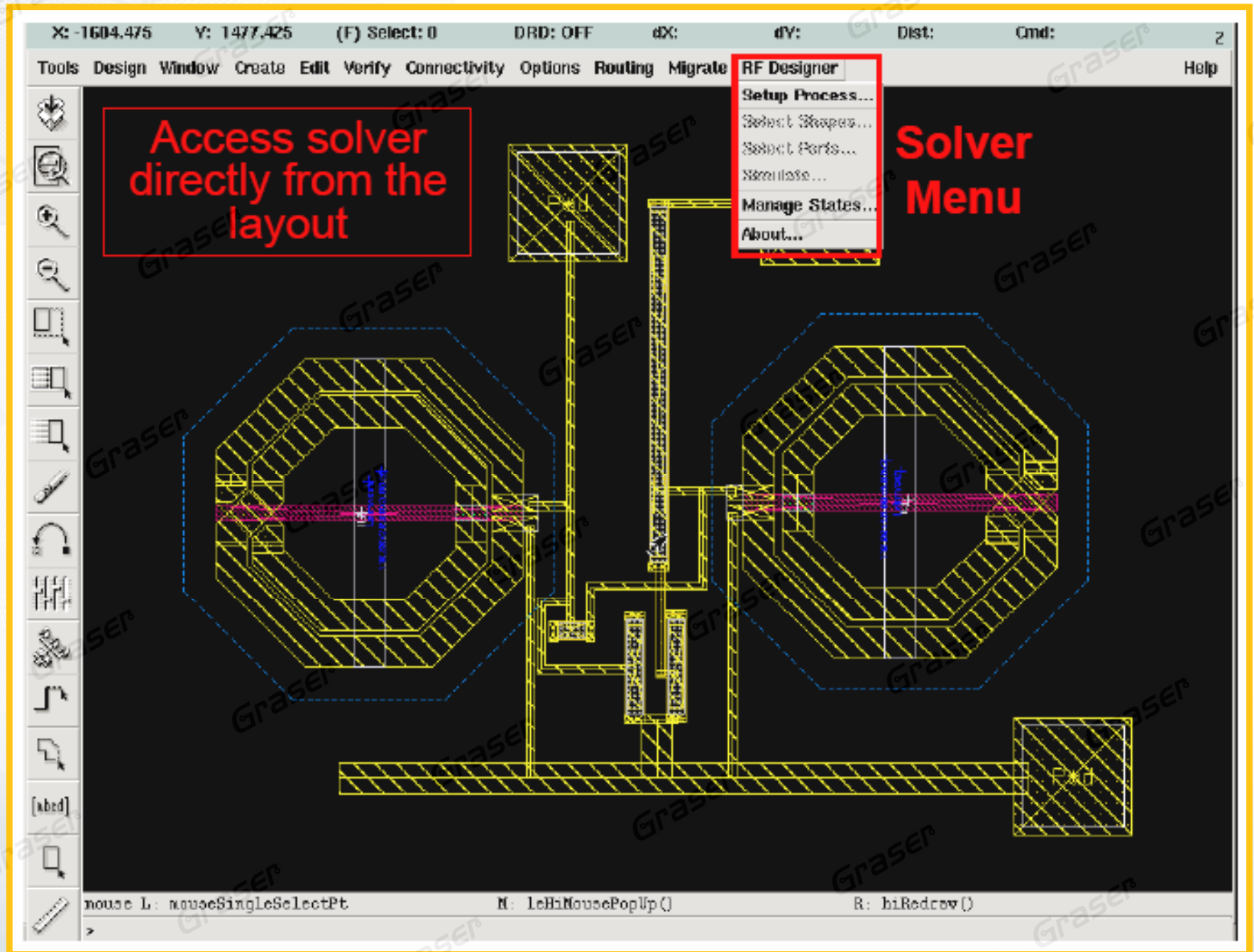
Setup Extraction Groups...  
Setup Process...  
Setup Ports...  
Show Extraction...  
Manage States...

Access solver directly from the schematic. select nets and components off the schematic

Solver menu

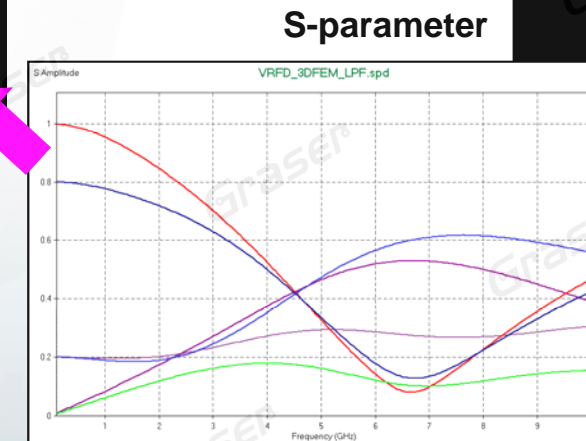
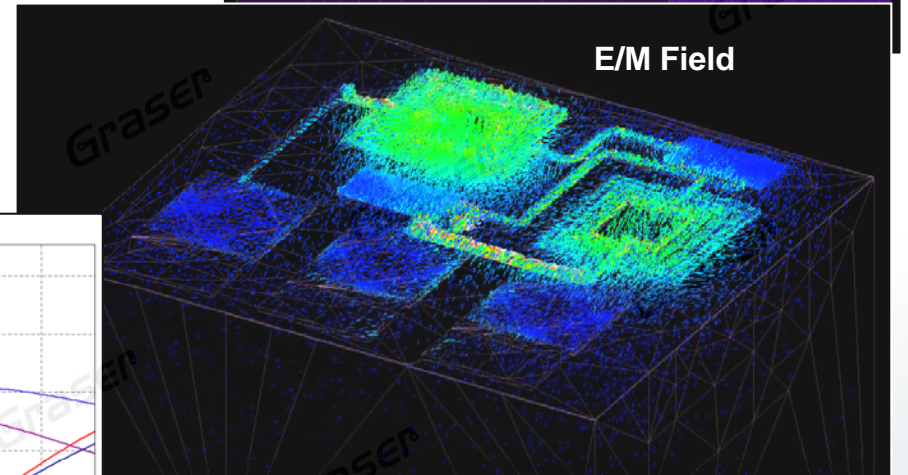
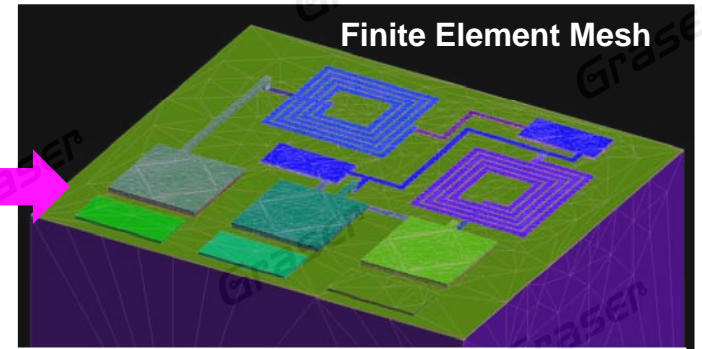
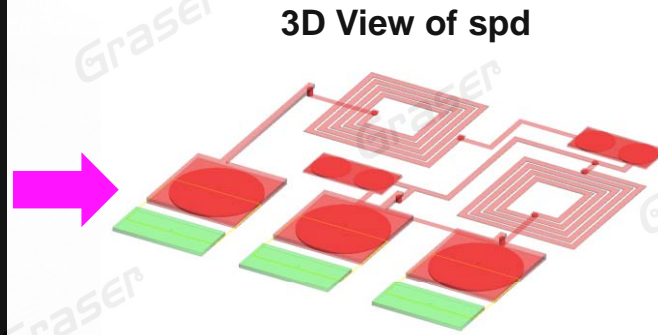
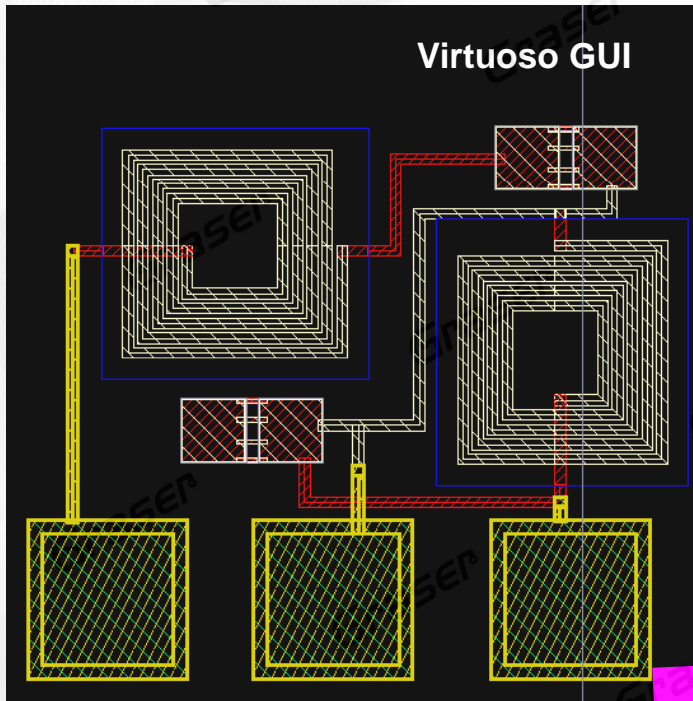
mouse L: (neo2Catch schSingleSelectPt() neoC M: schHiMousePopUp() R: schHiObjectProperty()

# Layout Flow



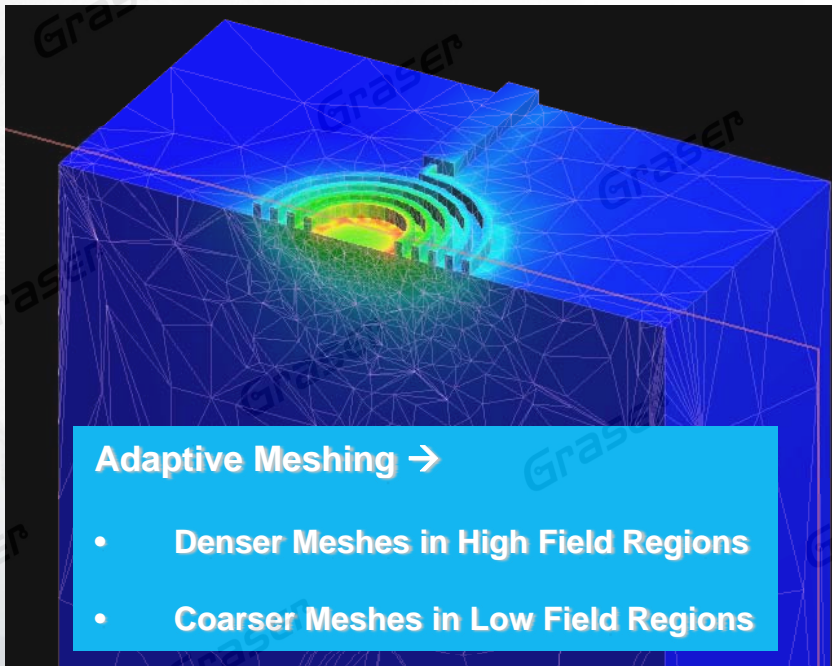
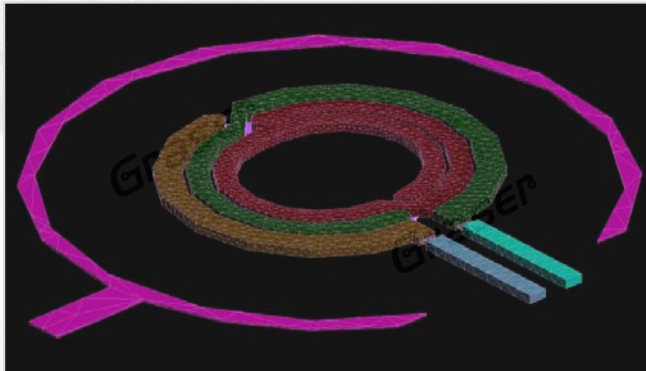


# Simulation Data Flow



# Accuracy and Performance Benchmark

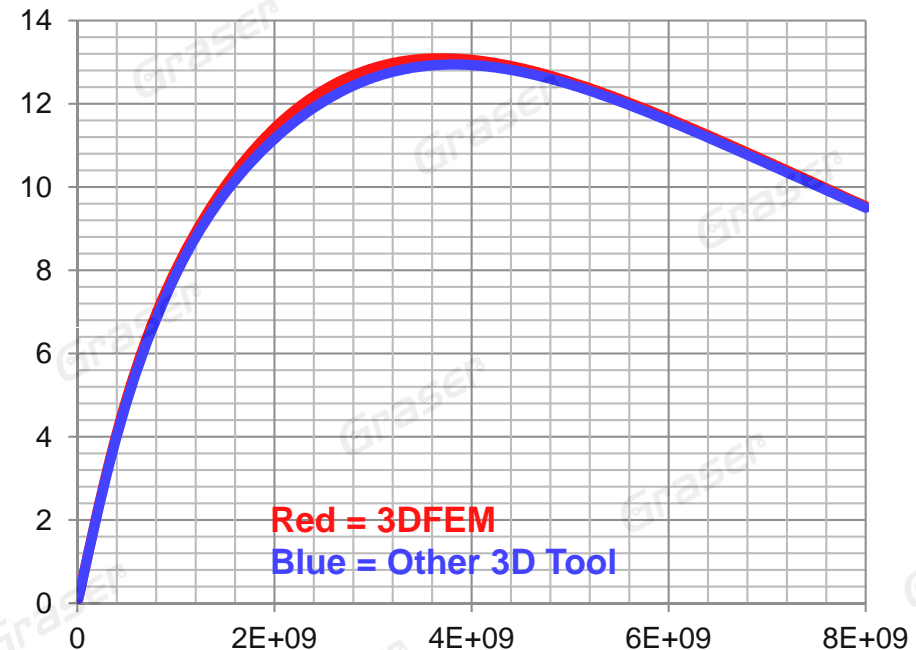
## RFIC Spiral Inductor



Adaptive Meshing →

- Denser Meshes in High Field Regions
- Coarser Meshes in Low Field Regions

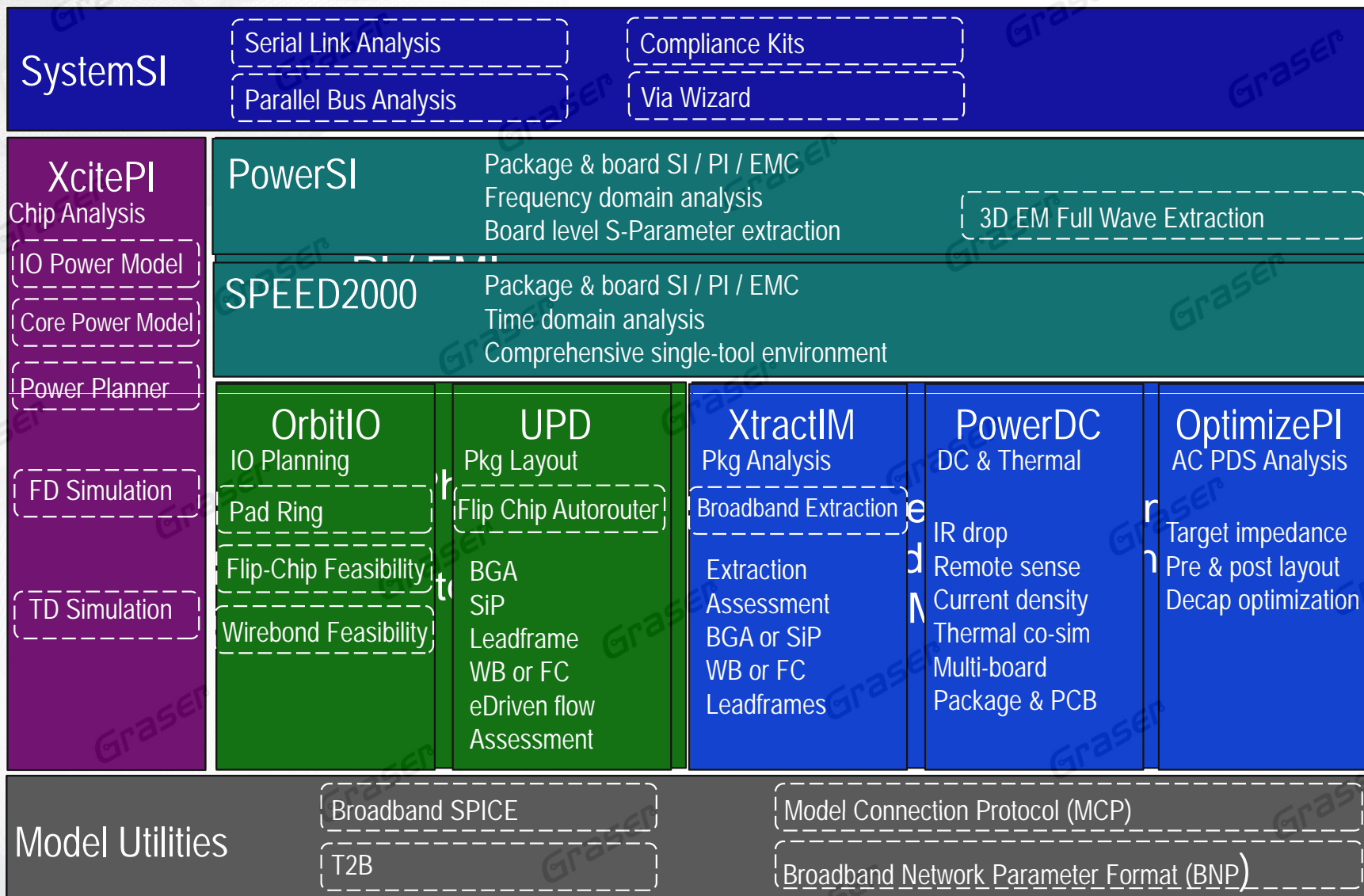
Q Factor



Red = 3DFEM  
Blue = Other 3D Tool

- Even with a slower computer, 3DFEM's speed is still >4X of the other 3D tool
  - ✓ 3DFEM : i5-2520, 2-core
  - ✓ Other Tool: Xenon-5620, 8-core

# Cadence Sigrity Products



- System Level Die-to-Die
- General PCB & Package Analysis
- Customized PCB & Package Analysis
- Package Physical Design
- Chip Analysis
- Model Utilities



# Simple Transistor to Behavior Model Conversion

# T2B Overview

- T2B converts SPICE transistor-level buffer models to IBIS behavioral models.
- Implementation based on S2IBIS from NC State Univ.
- **T2B Features**
  - code translated from Java
  - GUI added for both front-end and back-end processing
    - spreadsheet setup
    - graphical results
    - applies golden parser
  - applies either HSPICE, SPDSIM or Spectre
  - BIRD 95/98 support added for full support of IBIS 5.0
    - “power-aware” capabilities
  - IBIS Plus model
    - Greater accuracy than standard IBIS, including: on-die capacitance extraction as well as bias-dependent/frequency-dependent C\_comp.
  - applications support and software support/enhancements from Cadence/Sigrity

# SSO Simulation Enablement

- High-speed parallel buses experience issues when all signals are switched simultaneously
  - this is dominantly due to power delivery effects
    - proximity coupling of signals plays a secondary role
    - SSO simulation with ideal power delivery will rarely, if ever, be successful
- Transistor-level IO models properly power current
  - **simulations take days** to run for only a few lanes in a bus modeled
  - capacity/accuracy are limited, simple board/package models are applied
    - W-elements for boards, a few RLC elements for packages
- IBIS 5.0 buffer models properly consider power currents
  - IBIS 5.0 added support for power-aware effects with BIRD 95/98
    - requires full IBIS 5.0 circuit simulator support (e.g. Sigroty SPEED2000/SystemSI and Synopsys HSPICE)
    - S2IBIS lacks support beyond IBIS 3.2, specifically for BIRD 95/98
- SSO simulation with power-aware IBIS 5.0 models is fast and accurate
  - **hours become minutes**, where including even one transistor-level model implies days
  - IBIS 5.0 power-aware models enable system-level SSO simulation



# SSO Simulation Flow

## Extract IBIS power-aware model

### 1. Setup for Conversion

- start with transistor-level netlist
- configure the conversion
  - select the IOs to convert, select output type, etc.
- test circuit simulation with the netlist

### 2. Convert

- launch the conversion, observe progress bar

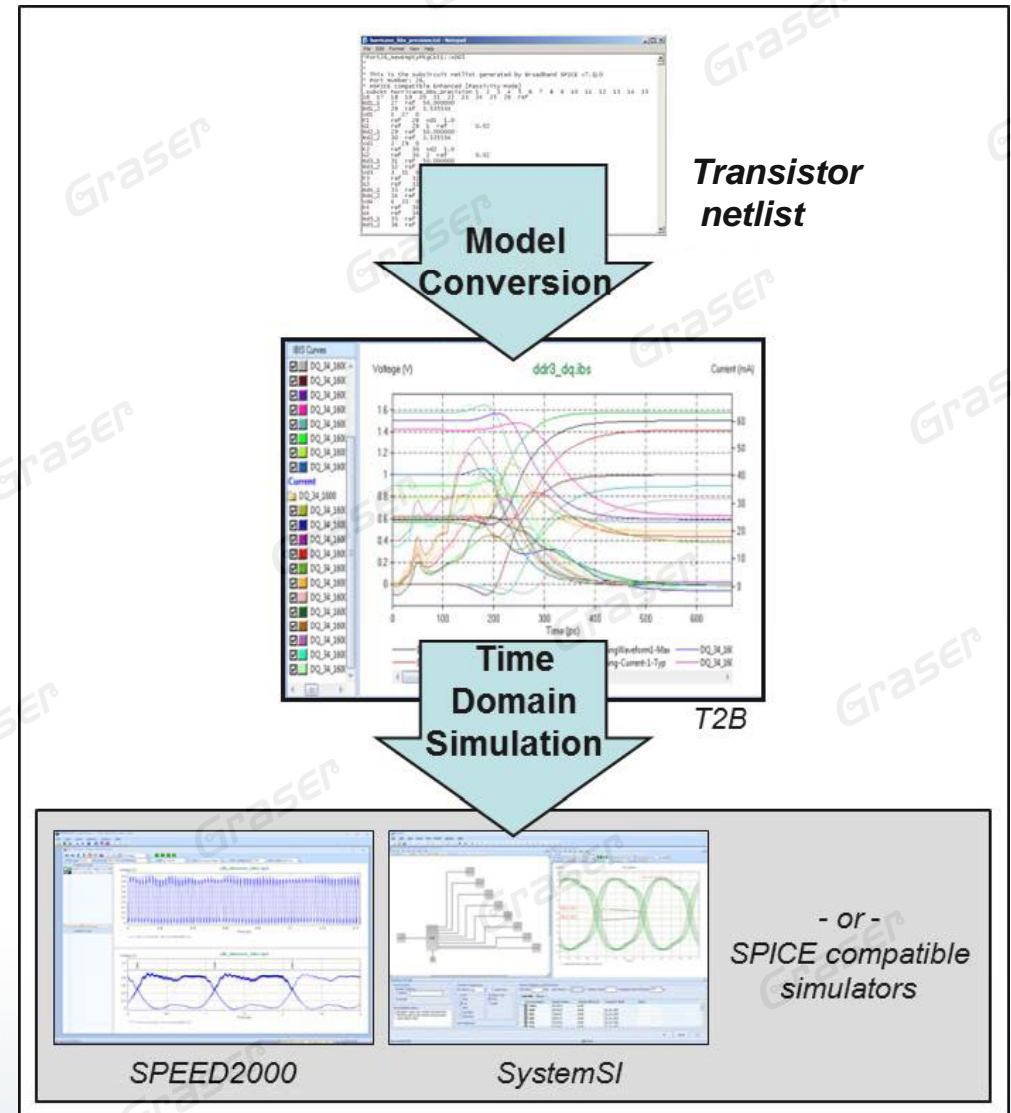
### 3. Validate Model

- check with IBIS golden parser
- view voltage/current for rising/falling edges
- compare transistor vs. behavioral power currents
- verify circuit behavior for various loads

## Apply model for SSO simulation

### 4. Transient circuit/system simulation

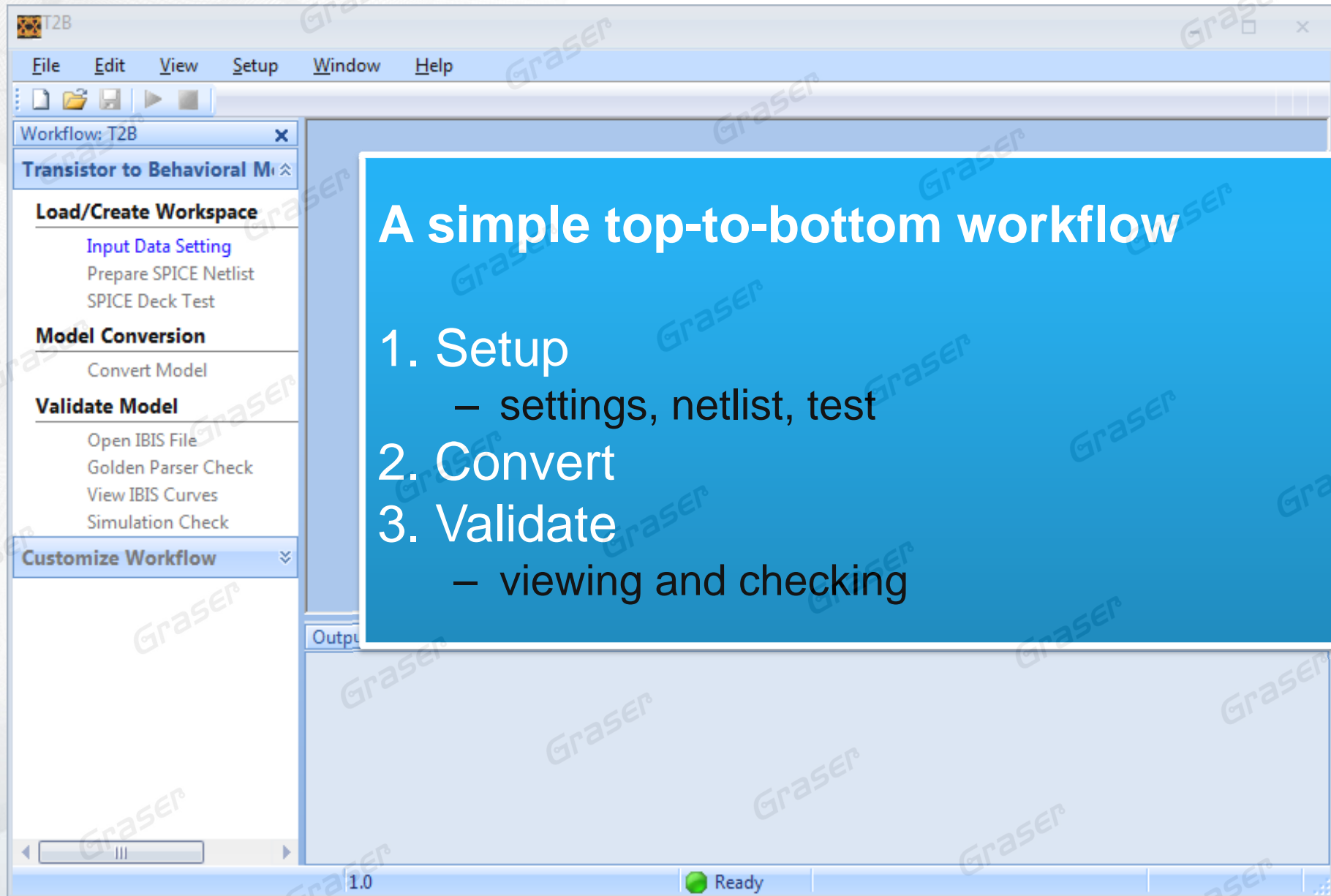
- Cadence/Sigrity SPEED2000/SystemSI and
- HSPICE each provide IBIS 5.0 power-aware support



# System Requirements

- **Circuit simulation engine**
  - HSPICE E-2010.12 or later
  - SPDSIM 11.0 or later
  - Spectre (conversion only, no IBIS 5.0 support yet)
- **Environment variables setting**
  - HSPICE licensing environment variable
  - Path to HSPICE executable

# T2B Workflow



The screenshot shows the T2B software interface. The menu bar includes File, Edit, View, Setup, Window, and Help. The main menu is titled 'Workflow: T2B' and contains the following sections:

- Load/Create Workspace**
  - Input Data Setting
  - Prepare SPICE Netlist
  - SPICE Deck Test
- Model Conversion**
  - Convert Model
- Validate Model**
  - Open IBIS File
  - Golden Parser Check
  - View IBIS Curves
  - Simulation Check
- Customize Workflow**

A red arrow points to the 'Validate Model' section. A blue text box on the right contains the following workflow steps:

**A simple top-to-bottom workflow**

1. Setup
  - settings, netlist, test
2. Convert
3. Validate
  - viewing and checking

The status bar at the bottom shows '1.0' and 'Ready'.



# Setup - Intelligent Spreadsheet Setup GUI

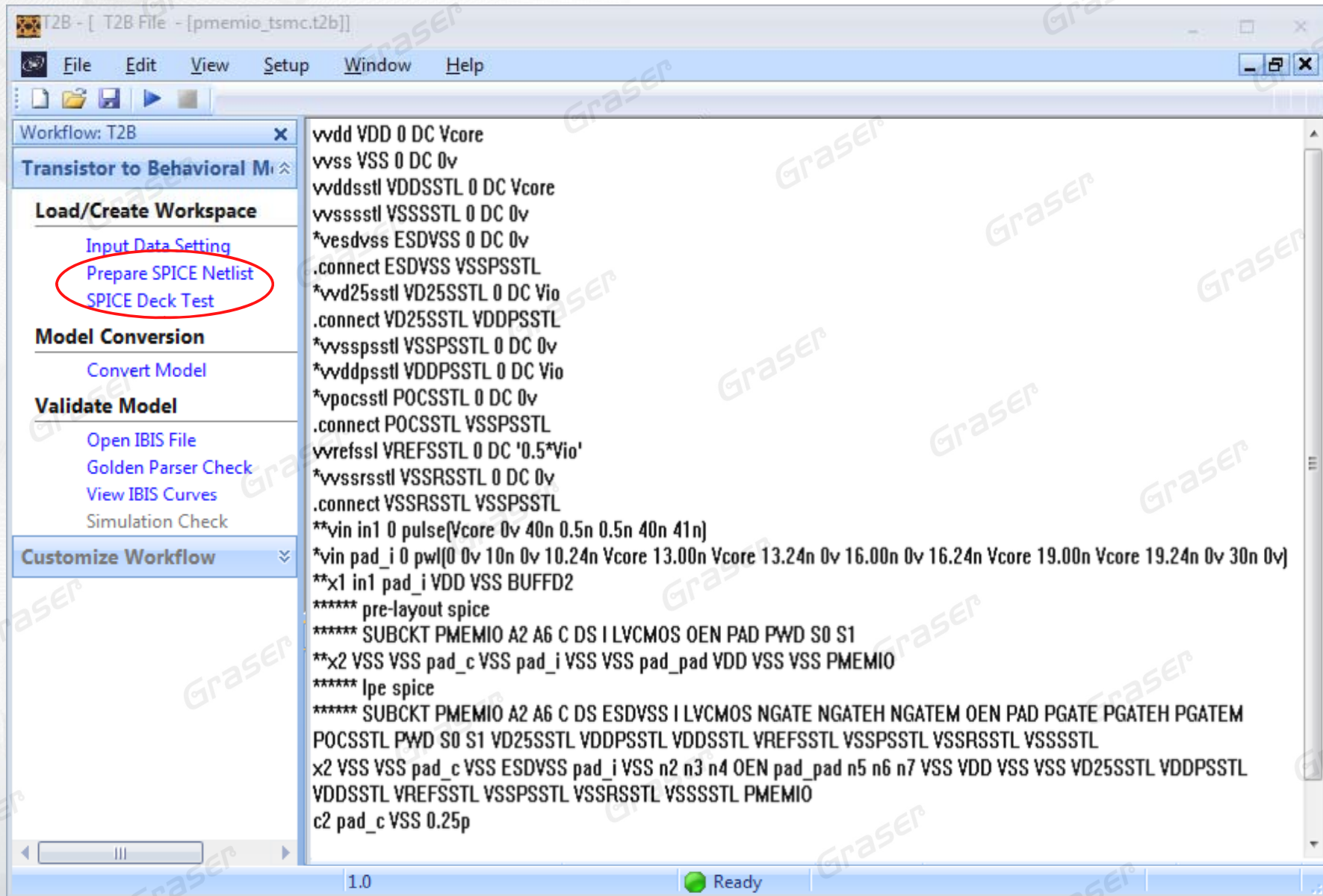
Pin-Name	spice_node	signal_name	model_name	R_pin
[IBIS Ver]	5.0			
[File name]	pmemio_tsmc.ibs			
[Date]	June 16, 2011			
[Source]	Sigrity, Inc.			
[Notes]	Use this section for any special not...			
[Disclaimer]	This is for demo only			
[Copyright]	Sigrity, Inc			
[Temperature range]	27C	125C	0C	
[Voltage range]	1.8	1.7	1.9	
[Sim time]	3ns			
[Vil]	0	0	0	
[Vih]	1.2	1.08	1.32	
[File rev]	1.0			
[Component]	tpdn90lpgv3			
[Spice file]	empty.sp			
[Pin]				
[PAD]	pad_pad	PAD	pmemio	
[IN]	pad_i	IN	dummy	
[OEN]	OEN	OEN	dummy	
[VDDP]	VDDPSSTL	VDDP	POWER	
[VSSP]	VSSPSSTL	VSSP	GND	
[Model]	pmemio			
[Model type]	I/O			
[Enable]	Active-Low			
[Rising waveform]	50	1.8	1.7	
[Falling waveform]	50	0	0	
[Model file]	pmemio_tsmc_typ.sp	pmemio_tsmc_min.sp	pmemio_tsmc_max.sp	
[Rising waveform]	50	1.8	1.7	
[Falling waveform]	50	0	0	
[Model]	dummy			

```

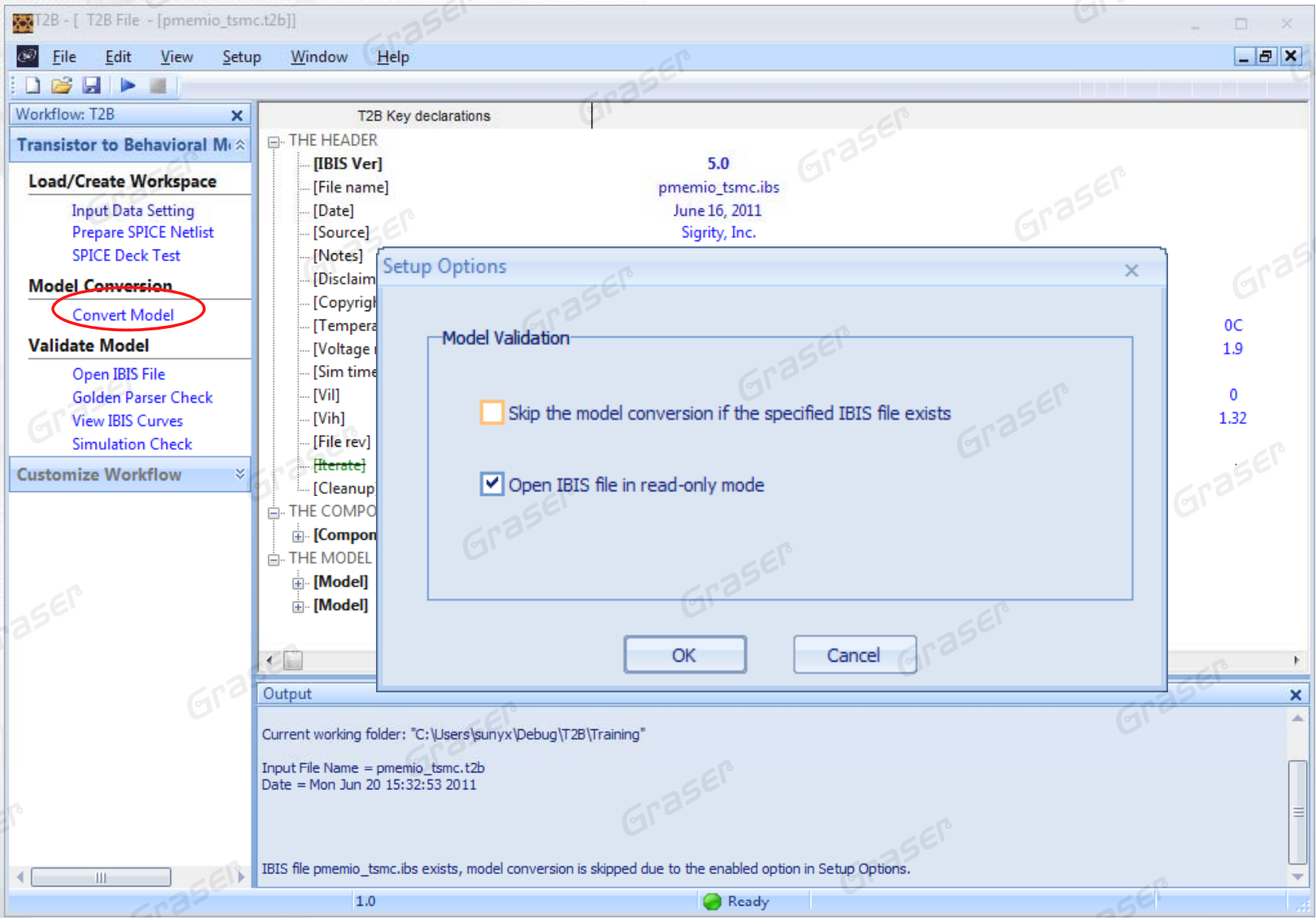
pmemio_tsmc12b - Notepad
File Edit Format View Help
[IBIS Ver] 5.0
[File name] pmemio_tsmc.ibs
[Date] June 16, 2011
[Source] Sigrity, Inc.
[Notes] Use this section for any special notes related to the file
[Disclaimer] This is for demo only
[Copyright] Sigrity, Inc
[Temperature range] 27C 125C 0C
[Voltage range] 1.8 1.7 1.9
[Sim time] 3ns
[Vil] 0 0
[Vih] 1.2 1.08 1.32
[File rev] 1.0
[Iterate]
[Cleanup]
[Component] tpdn90lpgv3
[Spice file] pmemio_top.sp
[Pin]
PAD pad_pad PAD pmemio
-> IN OEN
IN pad_i IN dummy
OEN OEN OEN dummy
VDDP VDDPSSTL VDDP POWER
VSSP VSSPSSTL VSSP GND
[Model] pmemio
[Model type] I/O
[Enable] Active-Low
[Rising waveform] 50 1.8 1.7
[Falling waveform] 50 0 0
[Model file] pmemio_tsmc_typ.sp pme
[Rising waveform] 50 1.8 1.7
[Falling waveform] 50 0 0
[Model] dummy
[NoModel]
  
```

ASCII text file

# Setup - Prepare and Test the Netlist Call



# Launch the Conversion





# Progress Messages are Displayed

The screenshot shows a software window titled "T2B - [ T2B File - [pmemio\_tsmc.t2b]]". The interface includes a menu bar (File, Edit, View, Setup, Window, Help) and a toolbar. On the left, a "Workflow: T2B" sidebar is open, showing a tree view with categories: "Load/Create Workspace", "Model Conversion" (with "Convert Model" circled in red), "Validate Model", and "Customize Workflow". The main workspace displays "T2B Key declarations" with a tree view containing sections like "THE HEADER", "THE COMPONENT DESCRIPTION", and "THE MODEL SPECIFICATION". The "THE MODEL SPECIFICATION" section shows two model entries: "[Model] pmemio" and "[Model] dummy". Below the workspace is an "Output" window with text: "modelName for above pin pmemio", "THIS\_PIN\_NEEDS\_ANALYSIS", "start analyzing pin .. PAD", "This Model Needs Pullup Data ..", "CurrentPin is .. PAD", "Do the typ run in GenerateVITable", "Starting HSpice job with input putPAD.spi", "Do the min run in GenerateVITable", "Starting HSpice job with input punPAD.spi". At the bottom, a status bar shows "1.0", a yellow circle icon, "Conversion" with a green progress bar at 37%, and "Extracting Model Pullup Data..."

# Validation - View the IBIS File

The screenshot shows the T2B software interface with the file [pmemio\_tsmc.ibs] open in Read Only Mode. The left sidebar contains a 'Validate Model' section with 'Open IBIS File' circled in red. The main window displays the following text:

```
*****  
IBIS file pmemio_tsmc.ibs created by T2B Version 1.0  
Sigrity, Inc. 2011  
Simulator: ***** HSPICE – E-2010.12 32-BIT (Nov 20 2010) winnt *****  
*****  
[IBIS ver] 5.0  
[File name] pmemio_tsmc.ibs  
[File Rev] 1.0  
[Date] June 16, 2011  
[Source] Sigrity, Inc.  
[Notes] Use this section for any special notes related to the file  
[Disclaimer] This is for demo only  
[Copyright] Sigrity, Inc  
*****  
  
Component tpdn90lpgv3  
*****  
[Component] tpdn90lpgv3  
[Manufacturer] Manufacturer name  
[Package]  
| variable   typ      min      max  
R_pkg  0.0      0.0      0.0  
L_pkg  0.0H      0.0H      0.0H  
C_pkg  0.0F      0.0F      0.0F  
|  
[Pin] signal_name  model_name  R_pin  L_pin  C_pin  
VSSP VSSP      GND  
VDDP VDDP      POWER  
IOEN IOEN      dummy  
IIN  IN       dummy  
PAD  PAD      pmemio
```

# Validation - Warnings from the Golden Parser

The screenshot shows the T2B software interface. The left sidebar contains a 'Validate Model' section with the following options: 'Open IBIS File', 'Golden Parser Check' (highlighted with a red circle), 'View IBIS Curves', and 'Simulation Check'. The main window displays the output of the Golden Parser Check, which includes the following text:

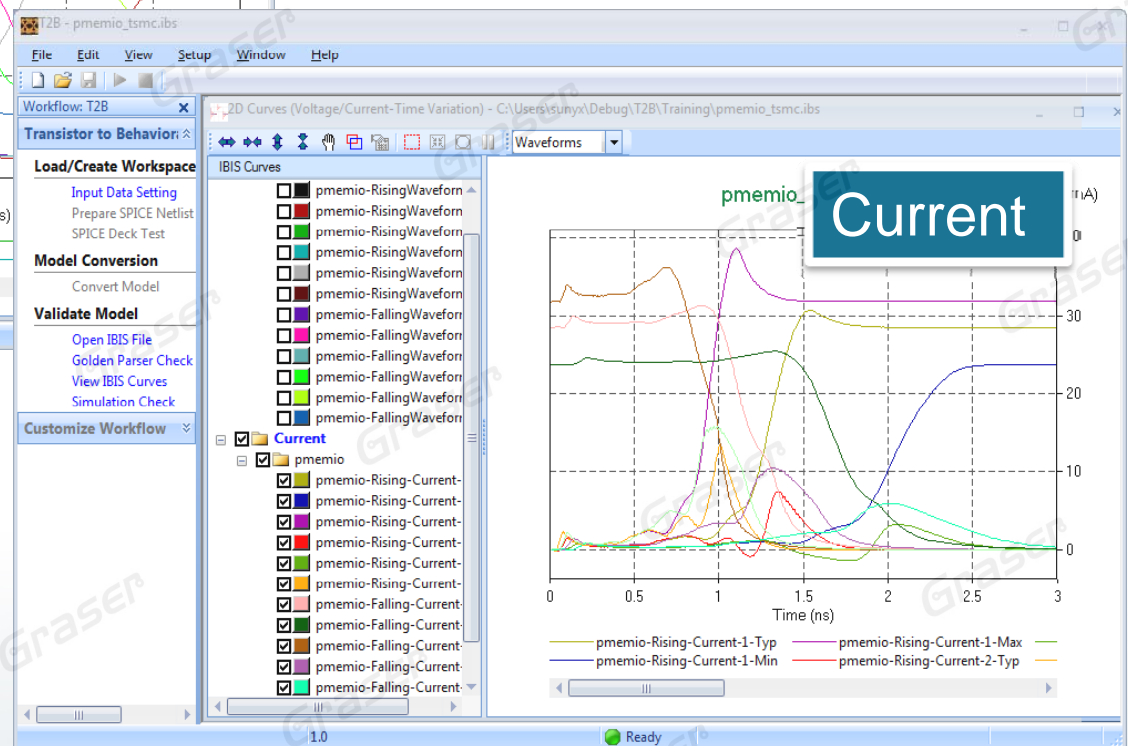
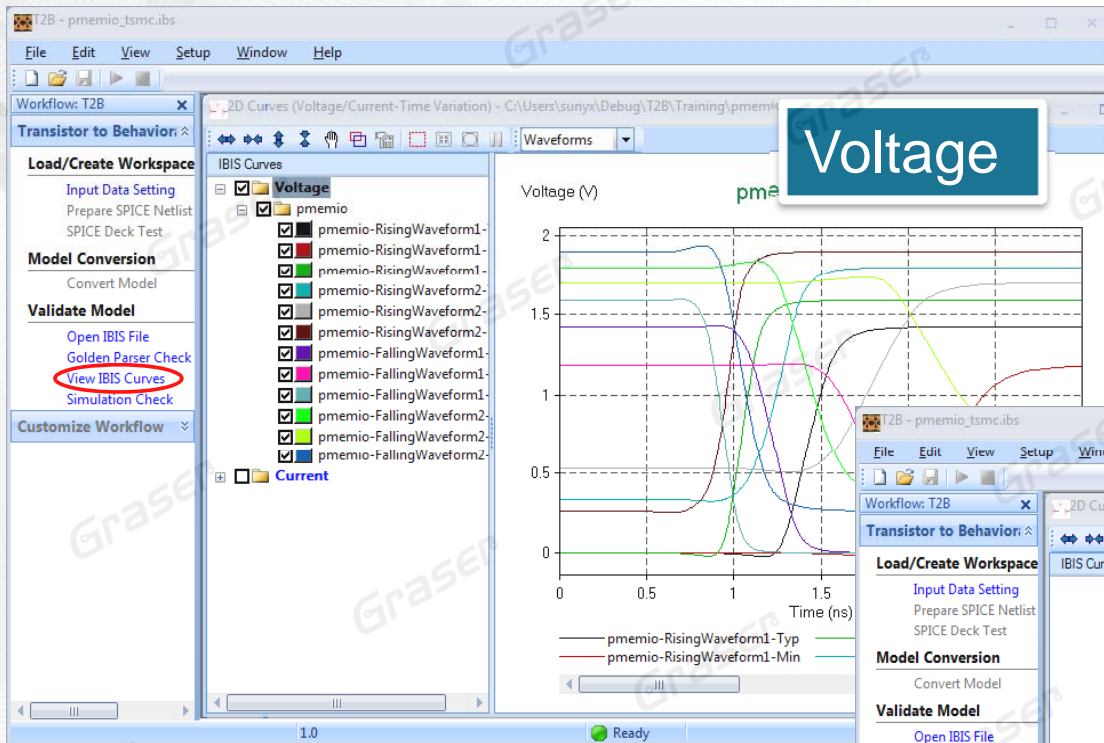
```
*****
| IBIS file pmemio_tsmc.ibs created by T2B Version 1.0
| Sigrity, Inc. 2011
| Simulator: ***** HSPICE – E-2010.12 32-BIT [Nov 20 2010] winnt *****
*****

[IBIS ver] 5.0
[File name] pmemio_tsmc.ibs
[File Rev] 1.0
[Date] June 16, 2011
[Source] Sigrity, Inc.
[Notes] Use this section for any special notes related to the file
[Disclaimer] This is for demo only
[Copyright] Sigrity, Inc

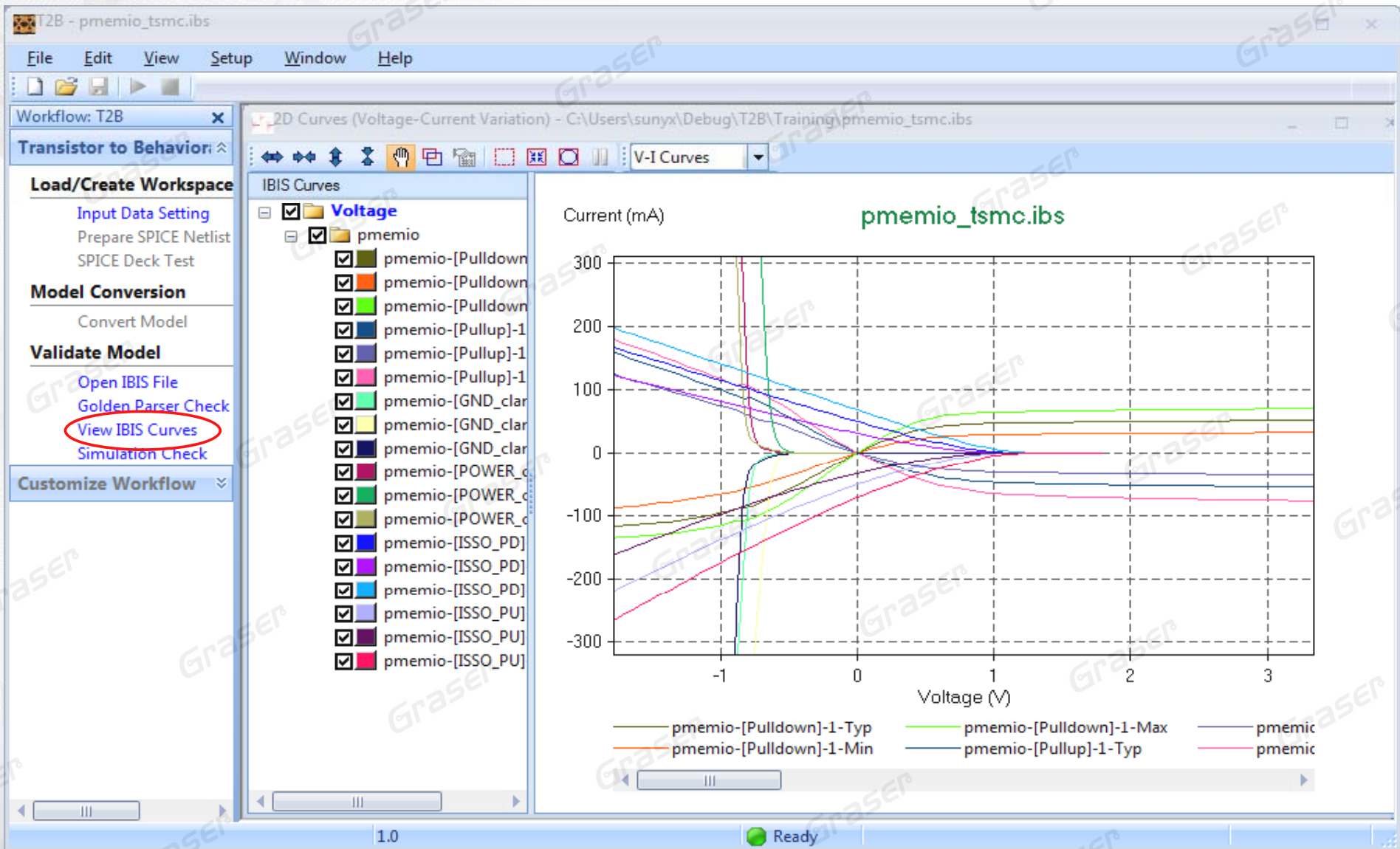
Output
WARNING (line 42) -
  Model pmemio: C_comp min value is not the smallest value listed
WARNING (line 42) -
  Model pmemio: C_comp max value is not the largest value listed
WARNING (line 43) -
  Model pmemio: C_comp_pullup min value is not the smallest value listed
WARNING (line 43) -
  Model pmemio: C_comp_pullup max value is not the largest value listed
WARNING (line 44) -
  Model pmemio: C_comp_pulldown min value is not the smallest value listed
WARNING (line 44) -
  Model pmemio: C_comp_pulldown max value is not the largest value listed
NOTE (line 163) - Pullup Maximum data is non-monotonic
NOTE (line 164) - Pullup Typical data is non-monotonic
NOTE (line 521) - ISSO_PD Minimum data is non-monotonic
WARNING - Model 'pmemio': Model_type 'I/O' must have Vinl set
WARNING - Model 'pmemio': Model_type 'I/O' must have Vinh set
WARNING - Model 'pmemio': Vmeas timing test load parameter should be specified
WARNING - Model pmemio: The [Falling Waveform]
  with [R_fixture]=50 Ohms and [V_fixture_min]=1.7V
  has MIN column DC endpoints of 0.56V and 1.70v, but
  an equivalent load applied to the model's I-V tables yields
  different voltages (0.53V and 1.70V),
  a difference of 2.51% and 0.00%, respectively.
WARNING - Model pmemio: Minimum ISSO_PU current (-0.033A) at 0V does not match Pullup current (-0.033A) at reference (0.000V)
WARNING - Model pmemio: Minimum ISSO_PD current (0.030A) at 0V does not match Pulldown current (0.030A) at reference (1.700V)
WARNING - Model pmemio: Maximum ISSO_PU current (-0.072A) at 0V does not match Pullup current (-0.072A) at reference (0.000V)
WARNING - Model pmemio: Maximum ISSO_PD current (0.067A) at 0V does not match Pulldown current (0.067A) at reference (1.900V)
Errors : 0
Warnings: 14
File Passed
```



# Validation - View Transient Waveforms



# Validation - View the IBIS V-I Curve



# Validation - Power-Aware IO Modeling

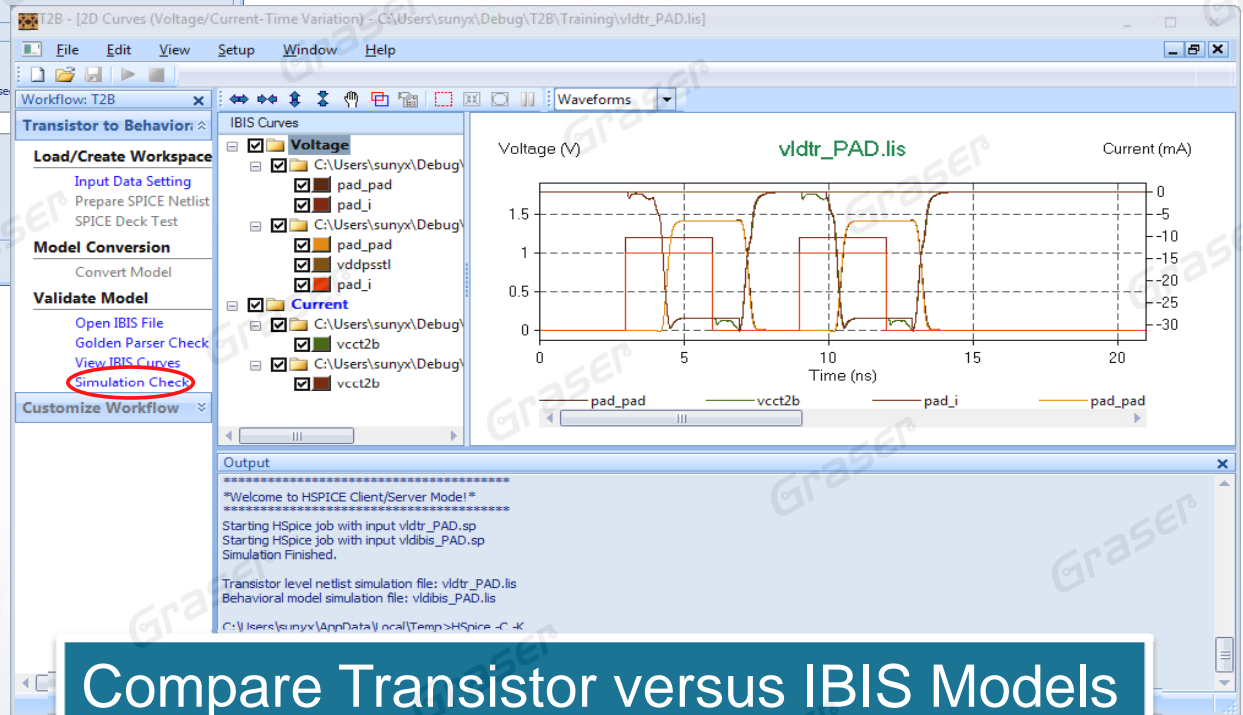
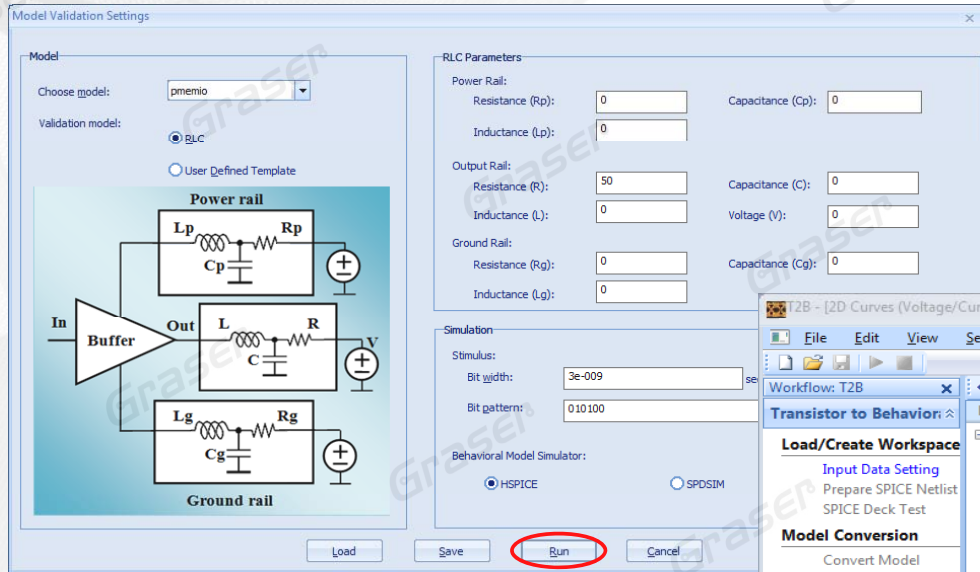
- Power-aware IO modeling
  - SSO is typically dominated by power delivery effects
  - IBIS 5.0 power-aware models are produced by T2B
  - Sigrity IBIS Plus model provides even better power currents





# Validation - Setup and View Circuit Simulation

*With Supply Parasitics and Signal Load*



Compare Transistor versus IBIS Models

# Summary

- Converts SPICE transistor-level IO models to power-aware behavioral models
- Enables SSO and other power delivery dominated simulations
- Provides
  - Complete automation of IBIS 5.0 power-aware models
    - from internal or vendor supplied SPICE models
  - Simply calls HSPICE or SPDSIM engines
  - **Front-end and back-end GUI**
    - for easy setup and thorough validation
  - Cadence/Sigrity support
    - for applications and ongoing flow/technology improvements