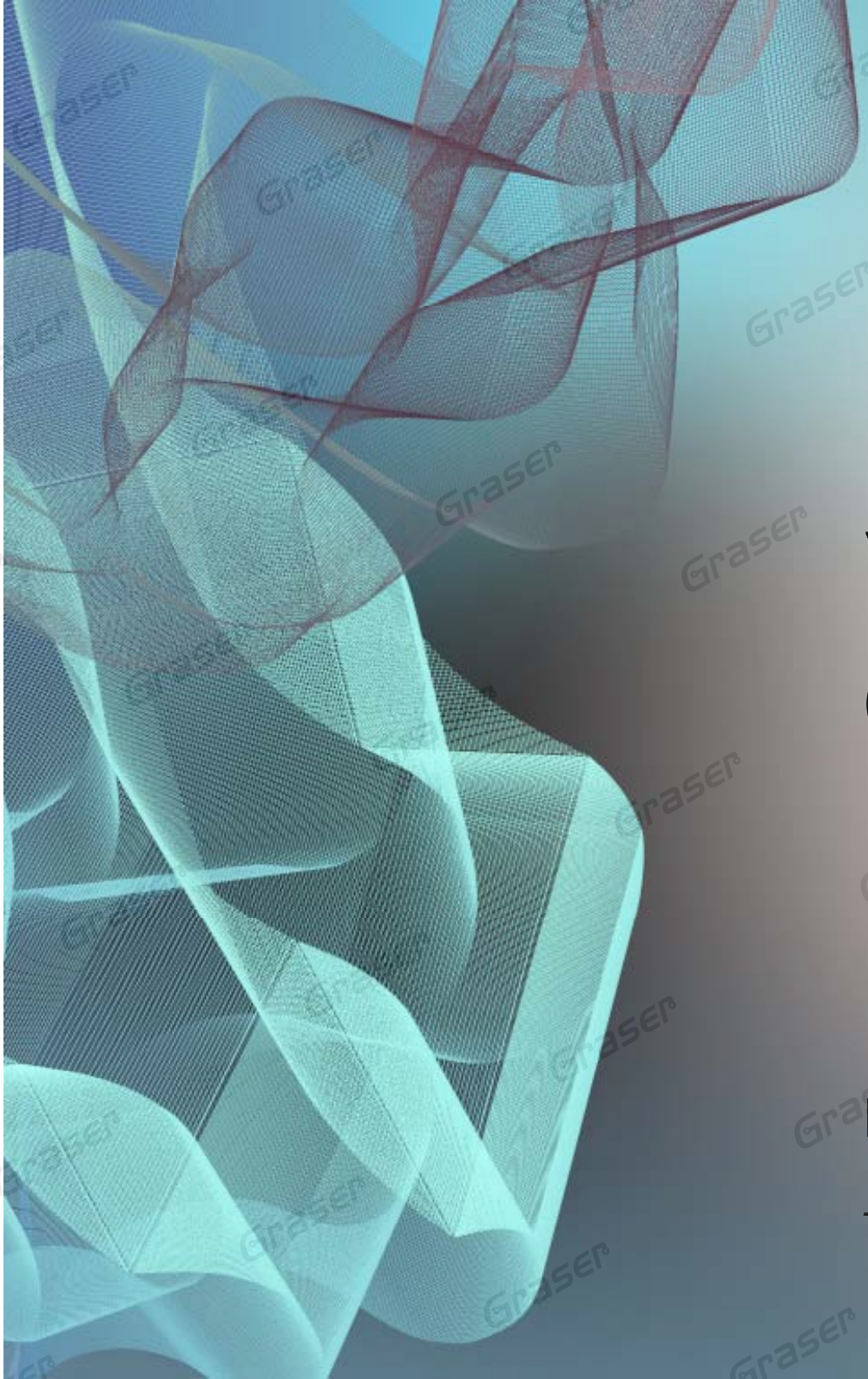

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Simple Transistor to Behavior Model Conversion

Eric Chen

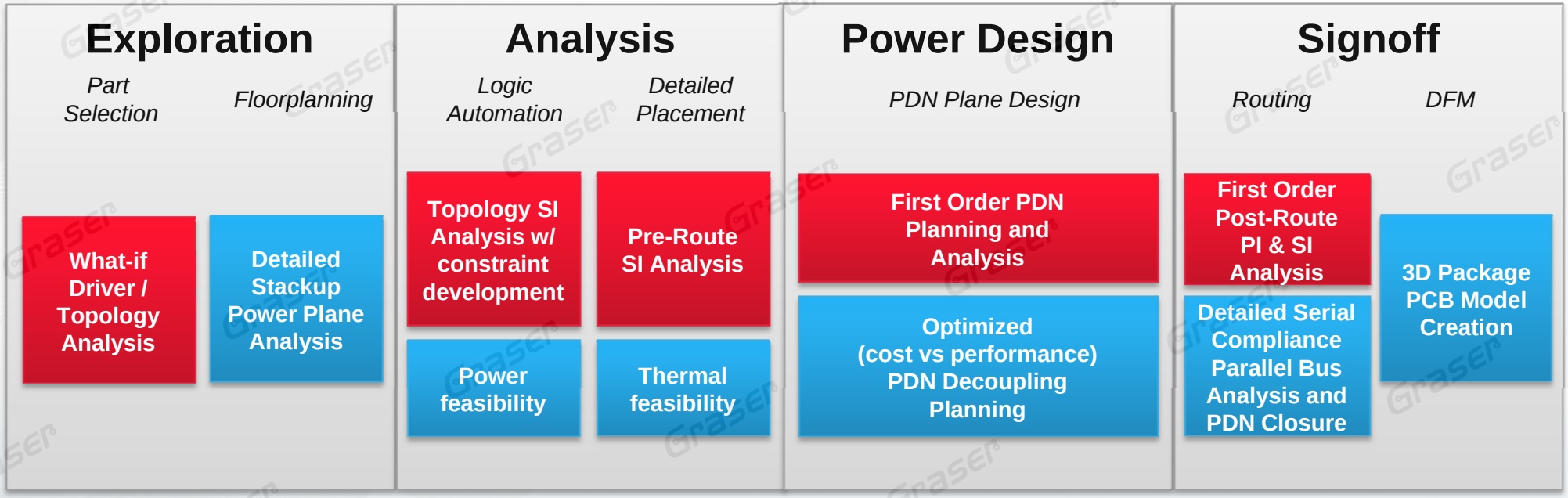
13/Aug/2013

Allegro / Virtuoso / EPS with Sigrity

- Comprehensive Front-to-Back Solution

- Better Together

- Single vendor Front-to-Back flow: design, verification, analysis, and compliance closure
- For emerging gigabit design challenges
- Focus on High-end Consumer and Data-center Infrastructure verticals
- Integrated 3D solvers for chip, package and board



1 cadence + 1 SIGRITY > 2

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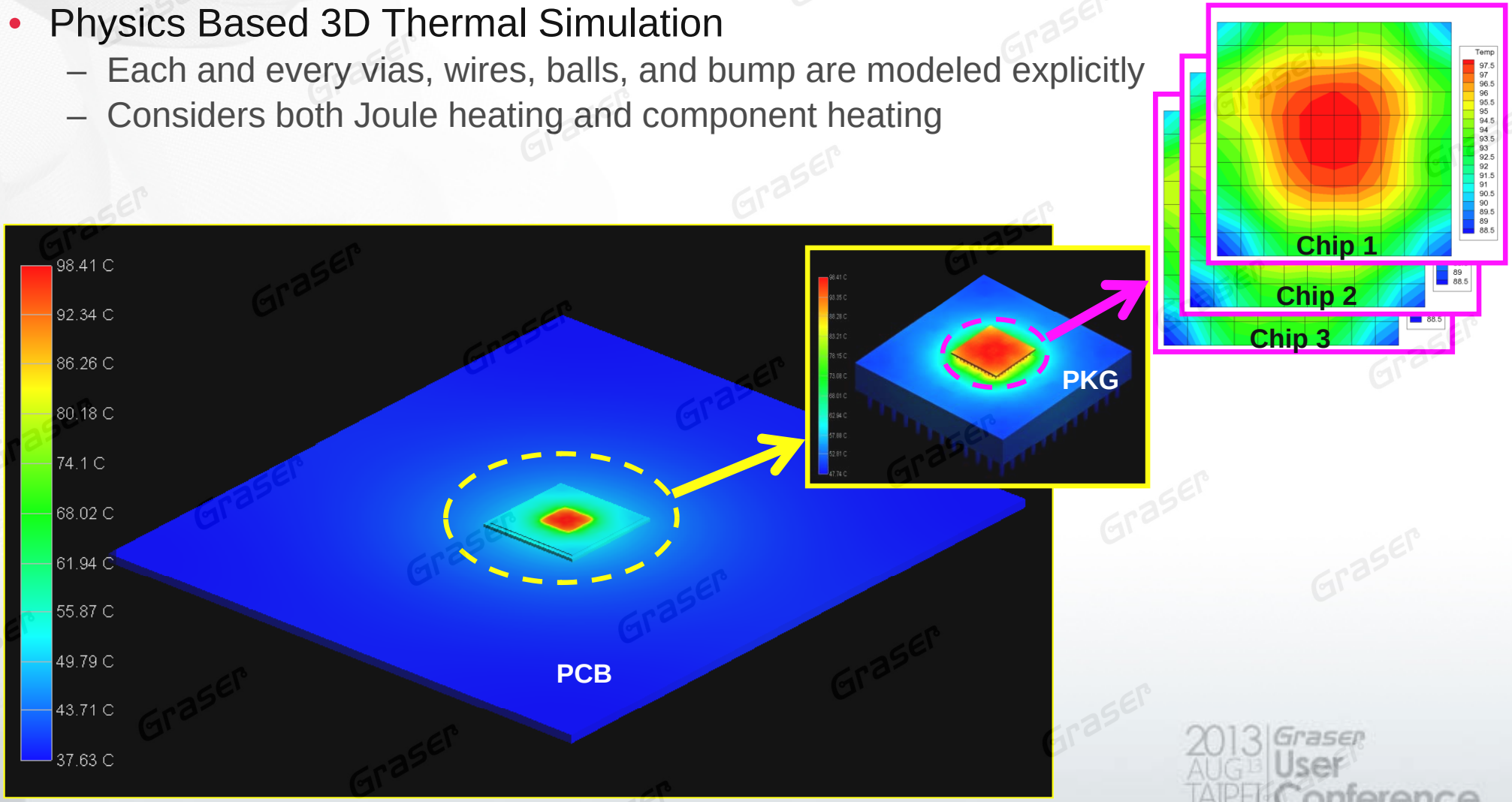
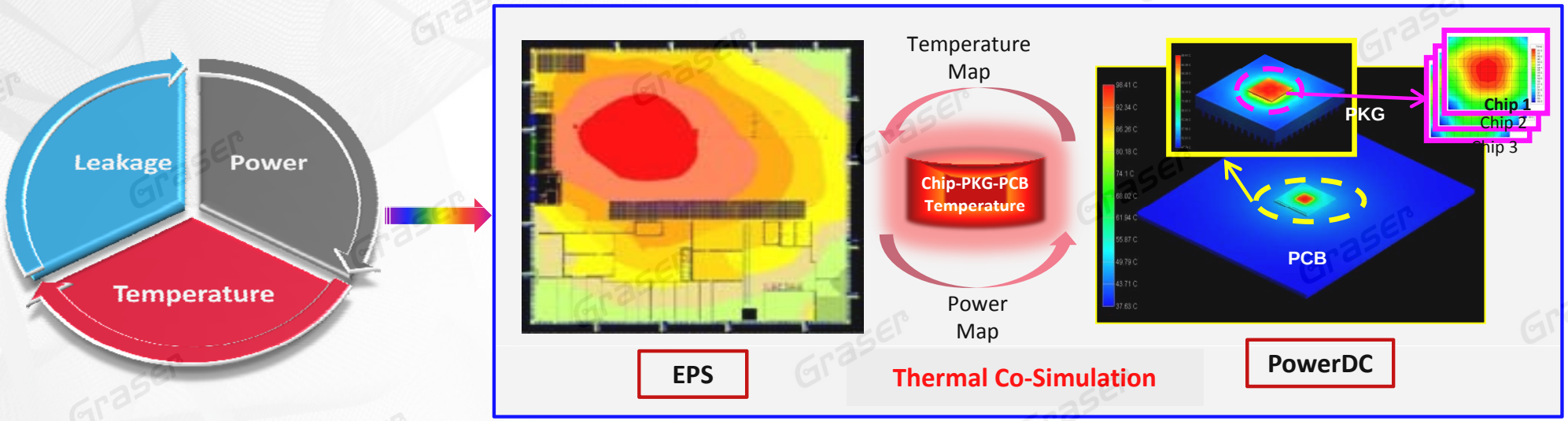
Digital IC - Sigrity EPS + PowerDC

Overview

- EPS + PowerDC → Electrical/Thermal Co-Simulation of 3D IC
  - EPS generates temperature and location dependent power maps
  - PowerDC computes detailed temperature distribution of dies, interposer, package, and board
- Physics Based 3D Thermal Simulation
  - Each and every vias, wires, balls, and bump are modeled explicitly
  - Considers both Joule heating and component heating

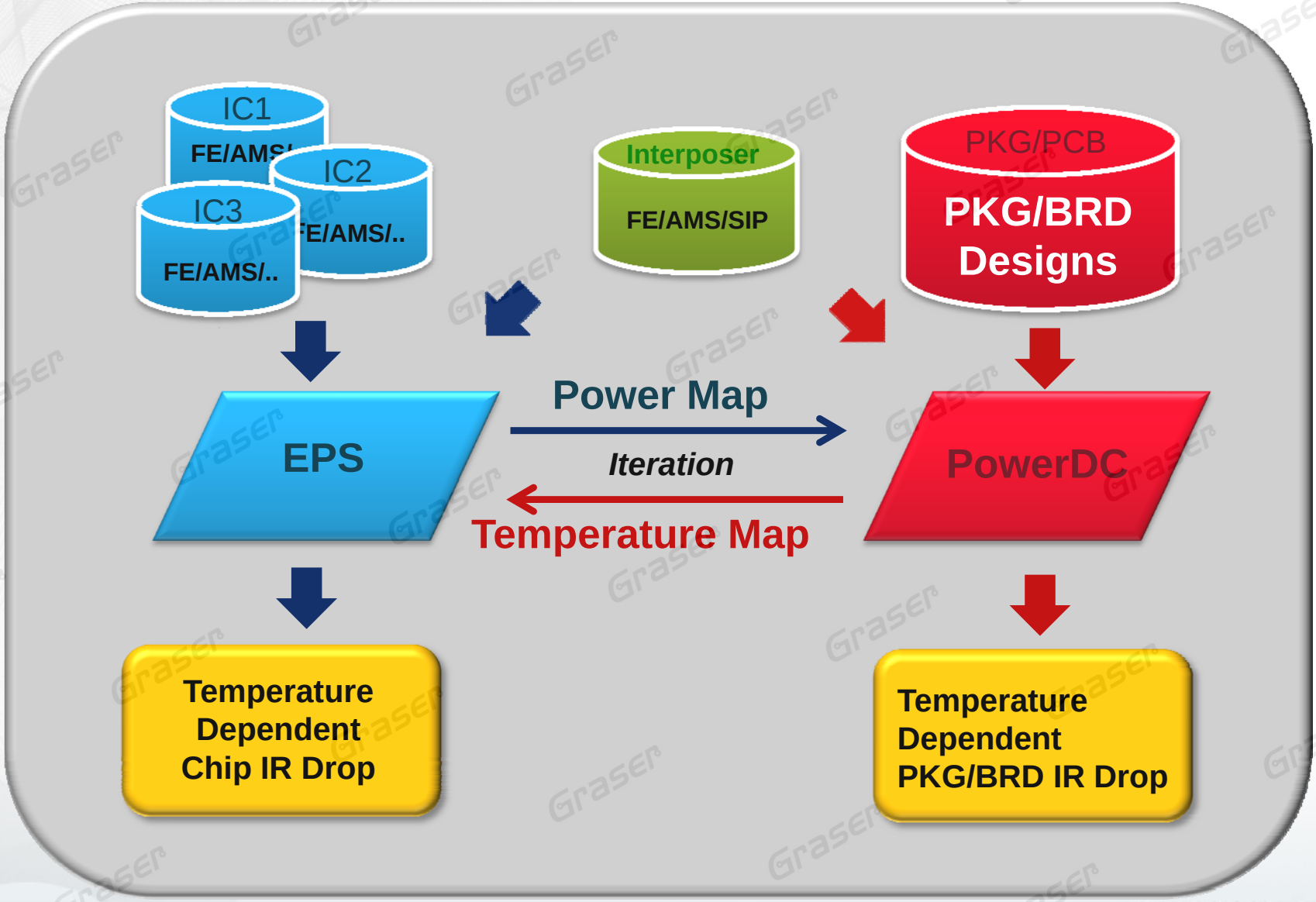


Electrical-Thermal Co-Simulation



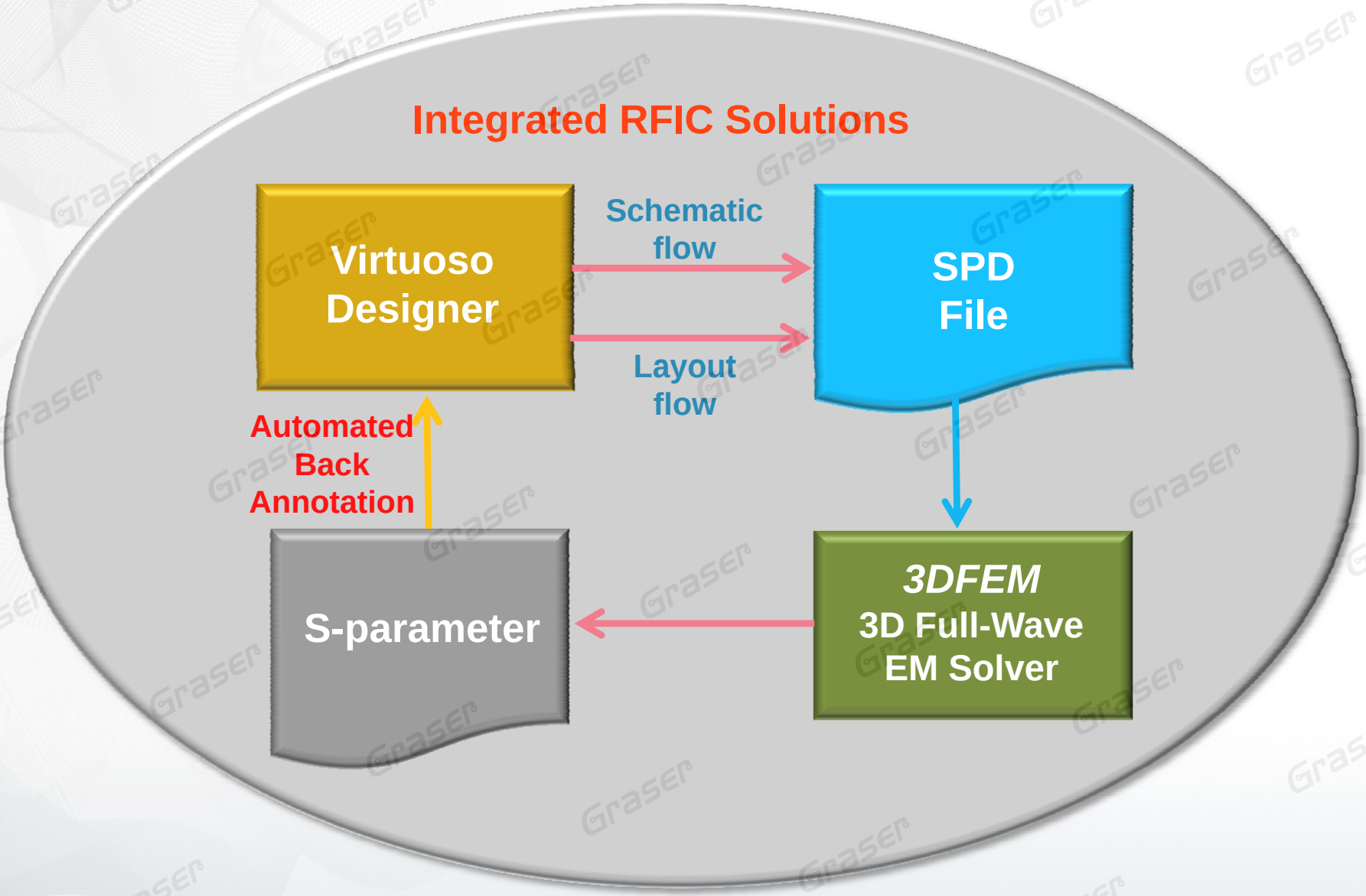
- Thermal Runaway
  - Positive feedback and interaction among chip's temperature, leakage and power dissipation
  - Temperature-dependent EMIR failures
- Physics Based 3D Thermal Simulation in "EPS + Sigrity PowerDC"
  - EPS generates temperature and location dependent "Power Map" file
  - PowerDC computes detailed temperature distribution for Chip-PKG-PCB and sends back "Temperature Map" file to EPS for more iteration and convergence
  - Thermal view is available in 2D/3D for interposer and full 3DIC systems.

CoWoS Thermal Simulation Flow

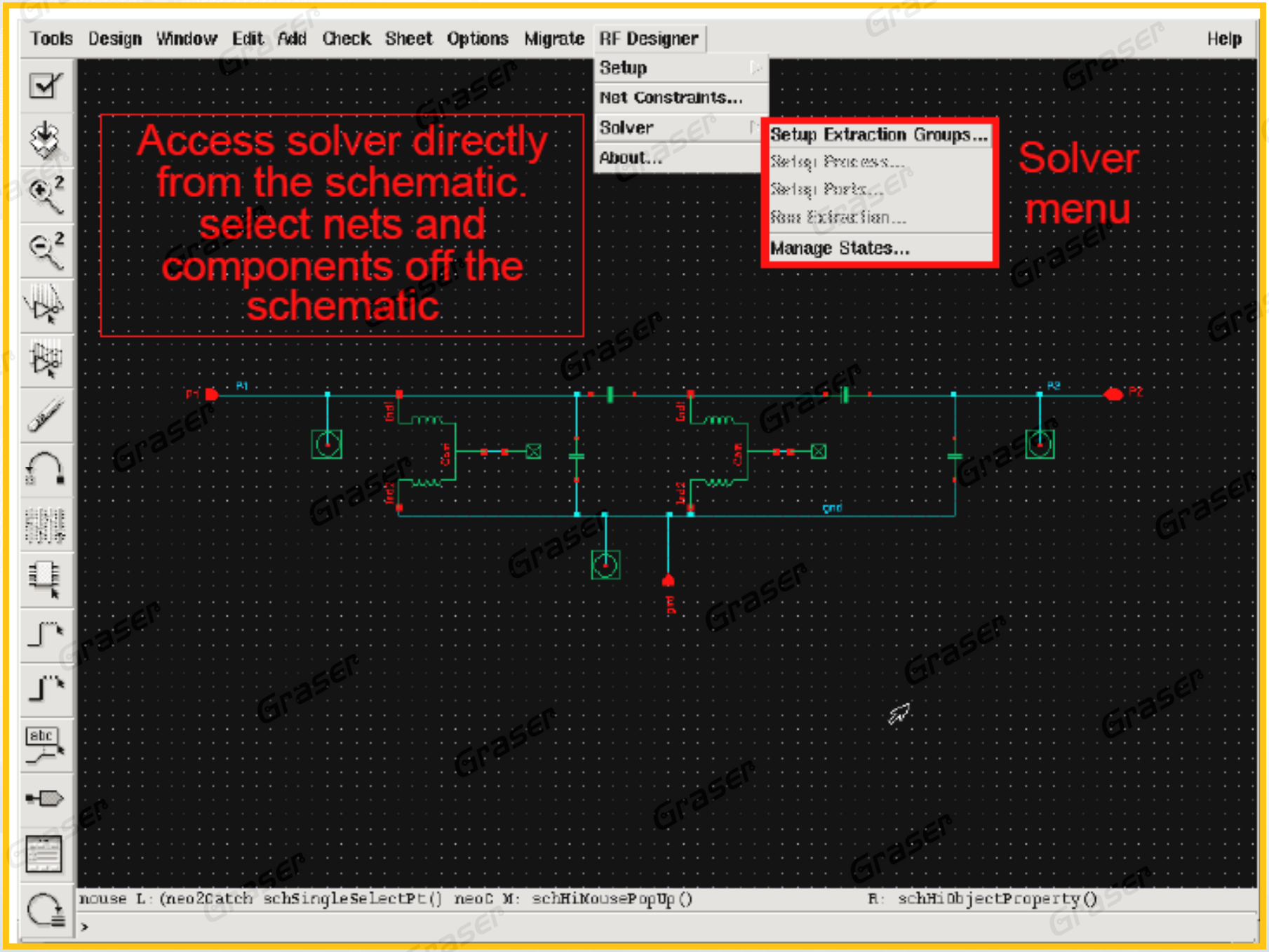


Custom IC - Sigrity Virtuoso + PowerDC

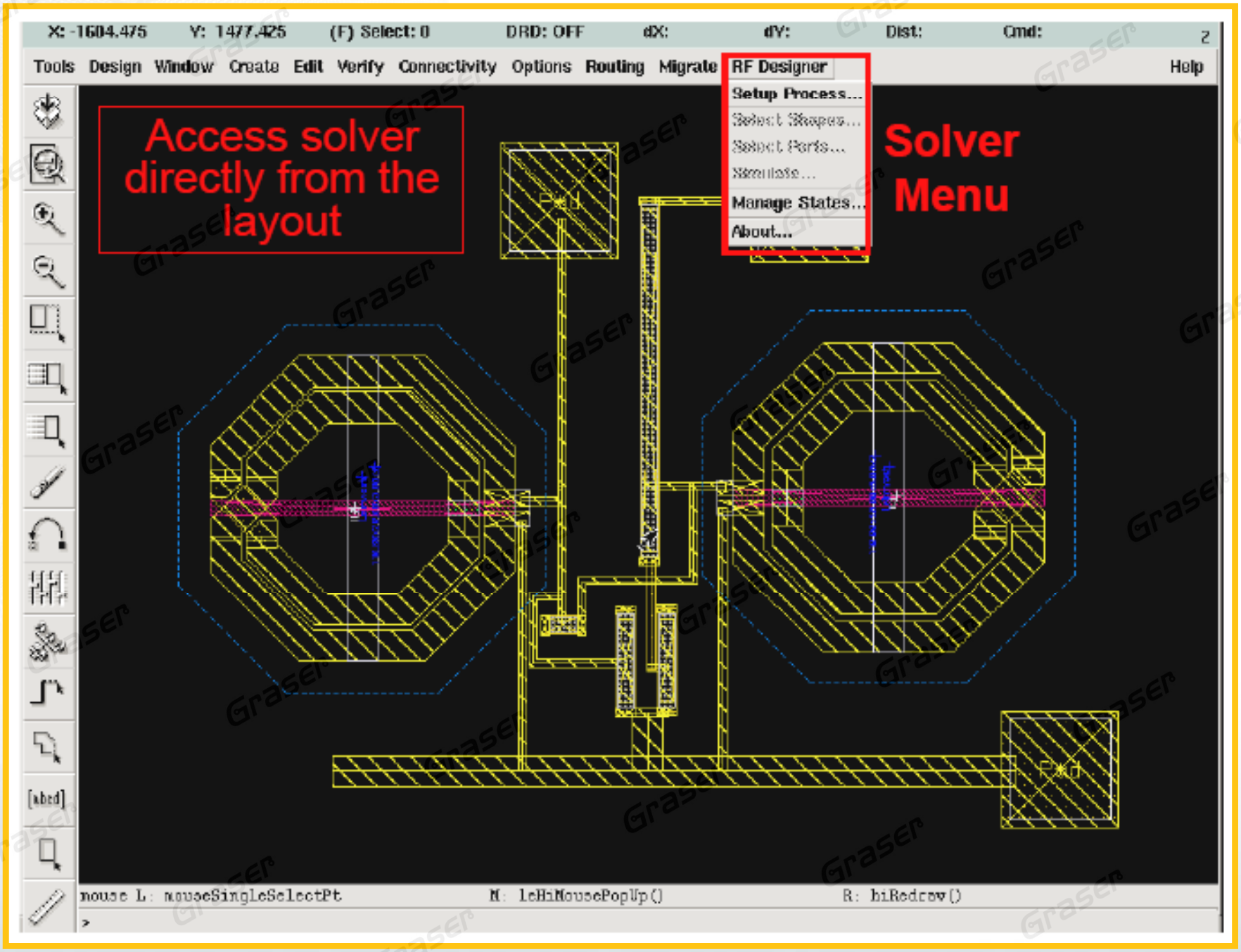
Seamless Integration



Schematic Flow

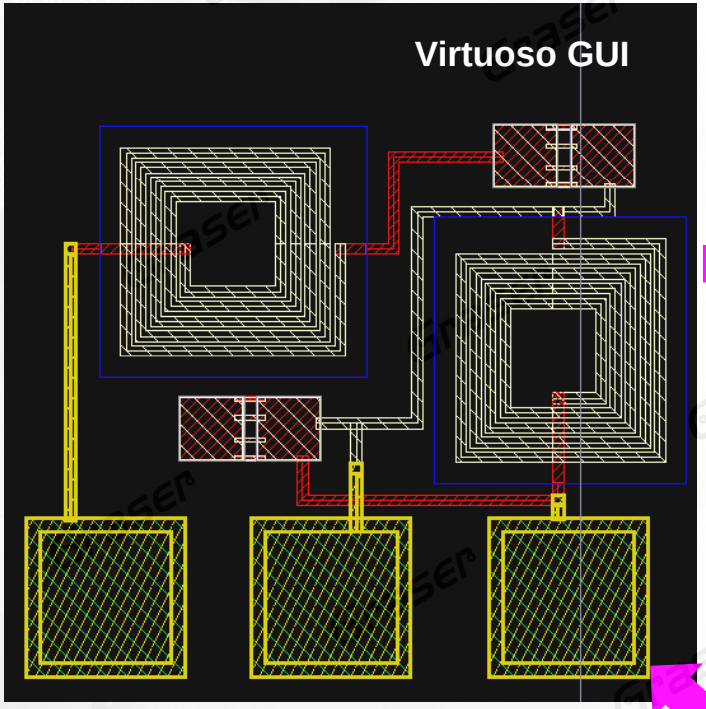


Layout Flow

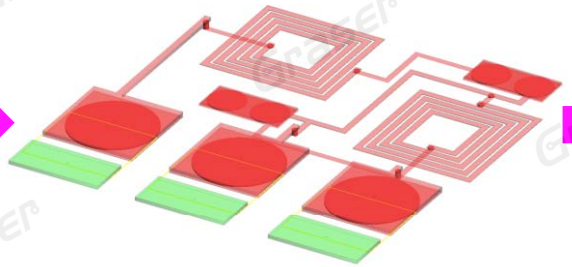

X: -1604.475
Y: 1477.425
(F) Select: 0
DRD: OFF
dX:
dY:
Dist:
Cmd:
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Migrate
RF Designer
Help
Setup Process...
Select Shapes...
Select Ports...
Simulate...
Manage States...
About...
Access solver directly from the layout
Solver Menu
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: hiRedraw()

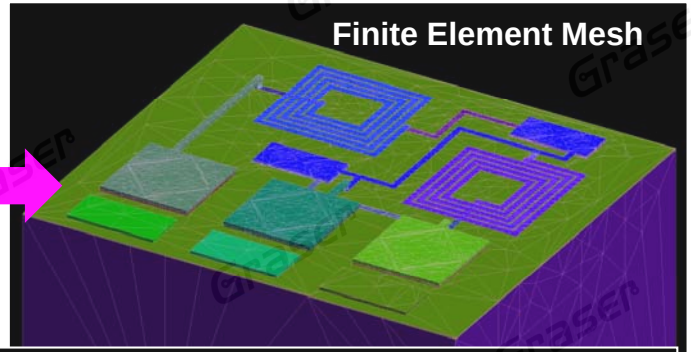
Simulation Data Flow

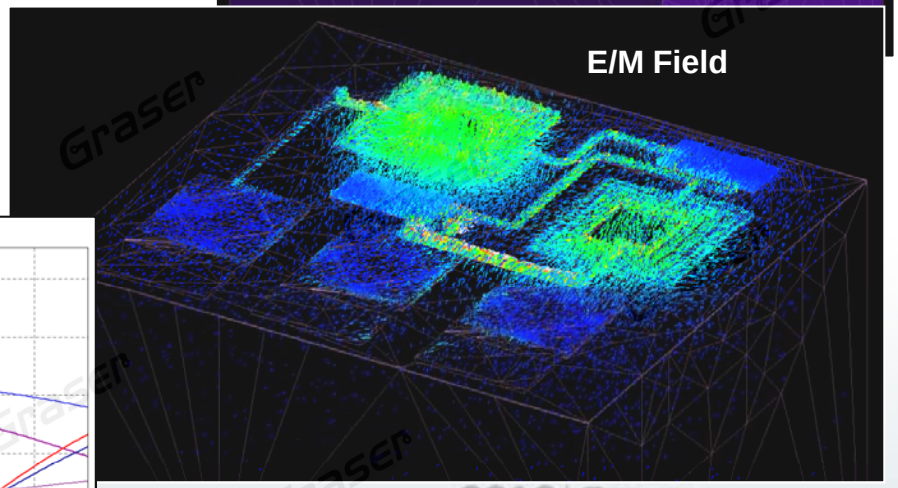
Virtuoso GUI → Virtuoso Data of Selected Components → .spd file → 3DFEM engine



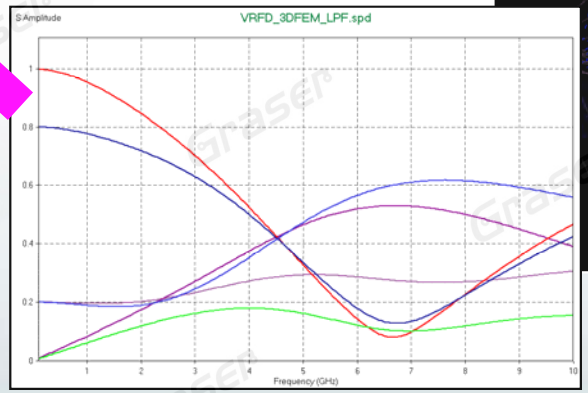
3D View of spd





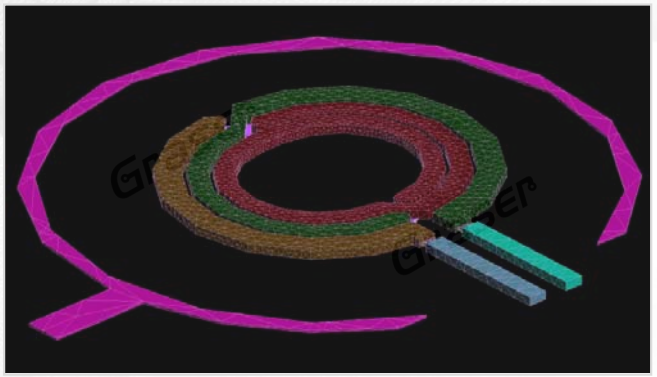


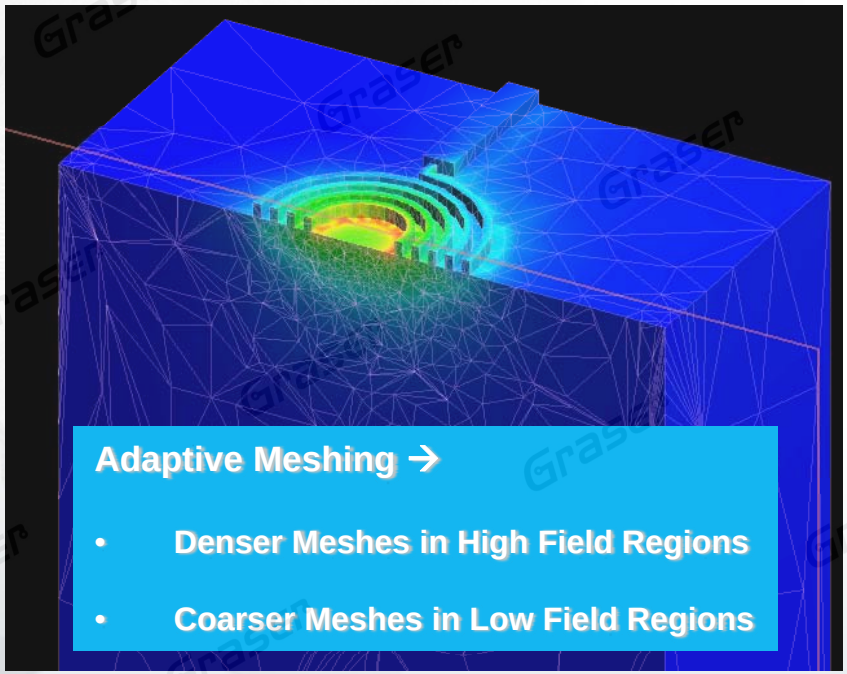
S-parameter

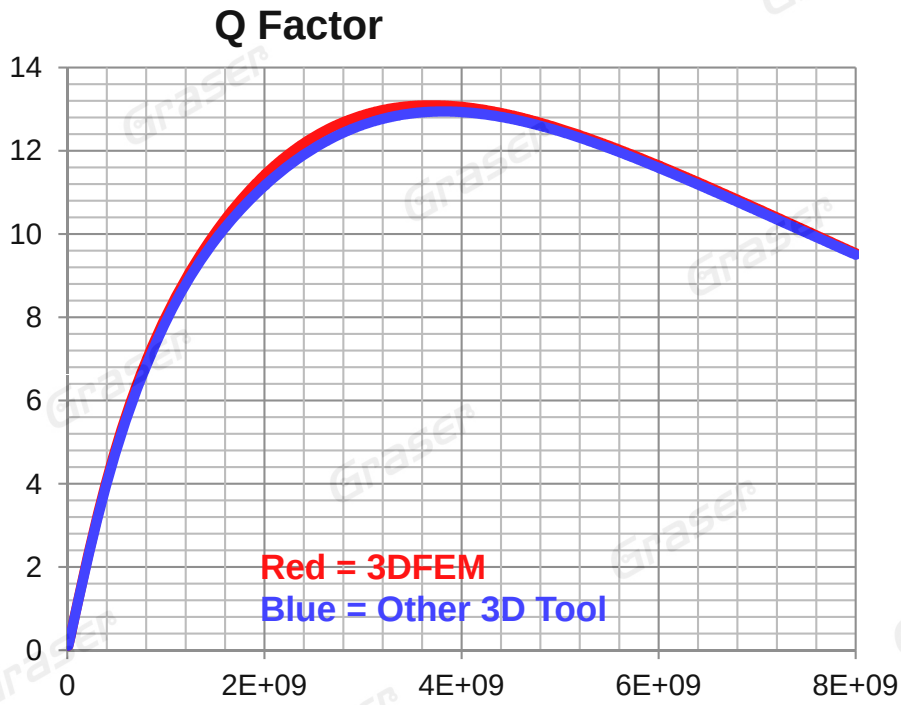


Accuracy and Performance Benchmark

RFIC Spiral Inductor

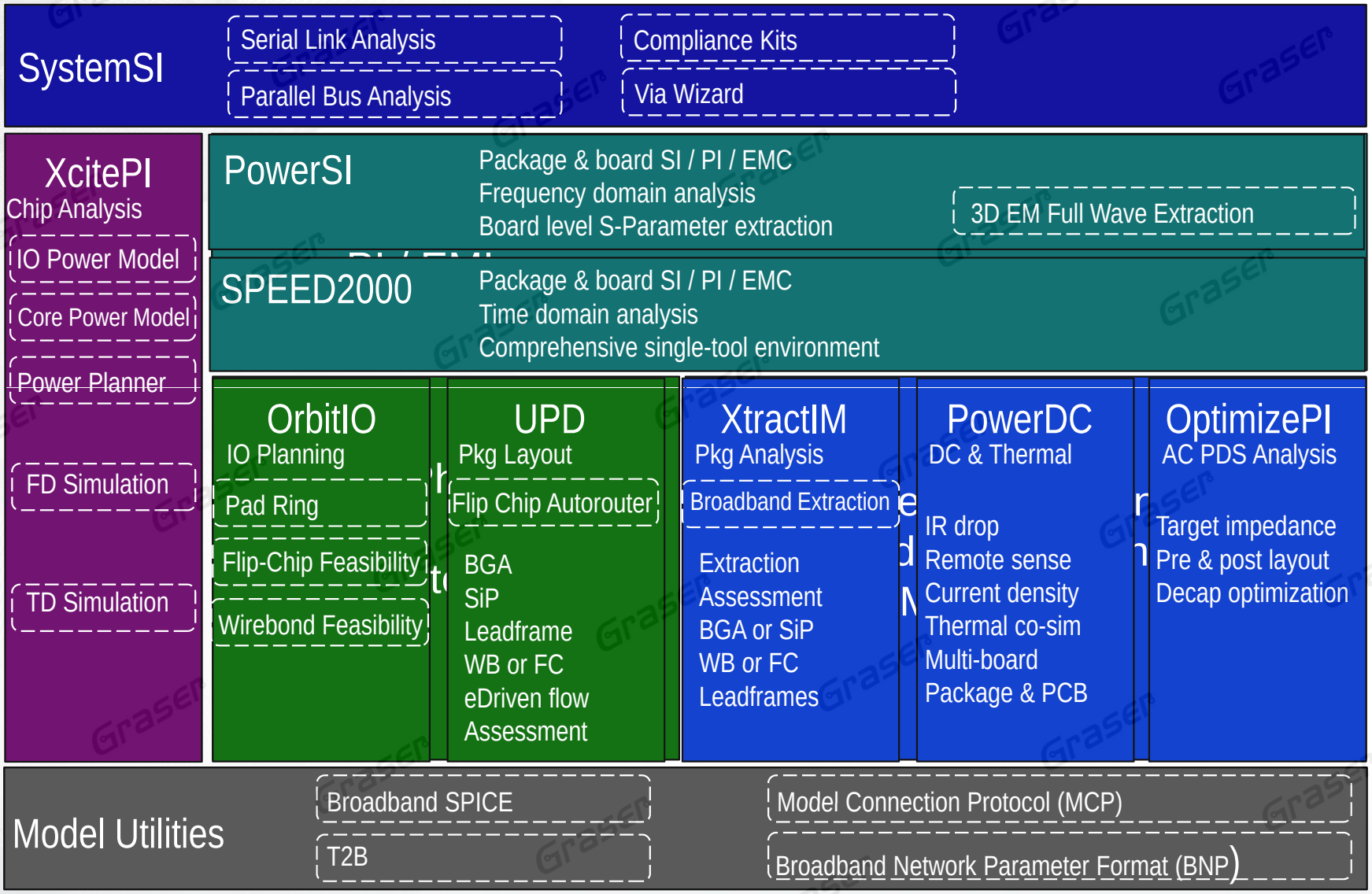






- **Even with a slower computer, 3DFEM's speed is still >4X of the other 3D tool**
  - ✓ 3DFEM : i5-2520, 2-core
  - ✓ Other Tool: Xenon-5620, 8-core

Cadence Sigrity Products



Simple Transistor to Behavior Model Conversion

T2B Overview

- T2B converts SPICE transistor-level buffer models to IBIS behavioral models.
- Implementation based on S2IBIS from NC State Univ.
- T2B Features
  - code translated from Java
  - GUI added for both front-end and back-end processing
    - spreadsheet setup
    - graphical results
    - applies golden parser
  - applies either HSPICE, SPDSIM or Spectre
  - BIRD 95/98 support added for full support of IBIS 5.0
    - “power-aware” capabilities
  - IBIS Plus model
    - Greater accuracy than standard IBIS, including: on-die capacitance extraction as well as bias-dependent/frequency-dependent C_comp.
  - applications support and software support/enhancements from Cadence/Sigrity

SSO Simulation Enablement

- High-speed parallel buses experience issues when all signals are switched simultaneously
  - this is dominantly due to power delivery effects
    - proximity coupling of signals plays a secondary role
  - SSO simulation with ideal power delivery will rarely, if ever, be successful
- Transistor-level IO models properly power current
  - simulations take days to run for only a few lanes in a bus modeled
  - capacity/accuracy are limited, simple board/package models are applied
    - W-elements for boards, a few RLC elements for packages
- IBIS 5.0 buffer models properly consider power currents
  - IBIS 5.0 added support for power-aware effects with BIRD 95/98
    - requires full IBIS 5.0 circuit simulator support (e.g. Sigrity SPEED2000/SystemSI and Synopsys HSPICE)
  - S2IBIS lacks support beyond IBIS 3.2, specifically for BIRD 95/98
- SSO simulation with power-aware IBIS 5.0 models is fast and accurate
  - hours become minutes, where including even one transistor-level model implies days
  - IBIS 5.0 power-aware models enable system-level SSO simulation

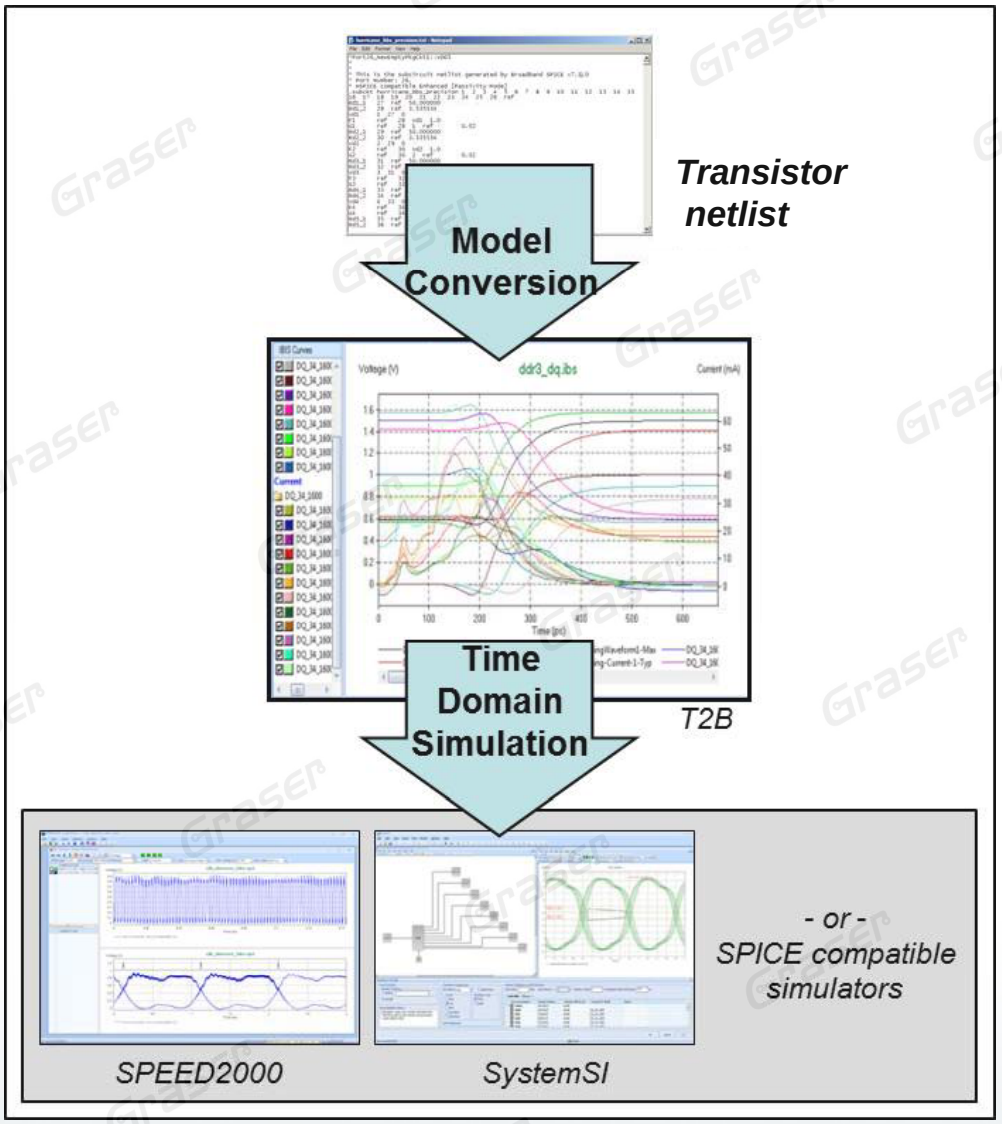
SSO Simulation Flow

Extract IBIS power-aware model

1. Setup for Conversion
   - start with transistor-level netlist
   - configure the conversion
     - select the IOs to convert, select output type, etc.
   - test circuit simulation with the netlist
2. Convert
   - launch the conversion, observe progress bar
3. Validate Model
   - check with IBIS golden parser
   - view voltage/current for rising/falling edges
   - compare transistor vs. behavioral power currents
   - verify circuit behavior for various loads

Apply model for SSO simulation

4. Transient circuit/system simulation
   - Cadence/Sigrity SPEED2000/SystemSI and
   - HSPICE each provide IBIS 5.0 power-aware support

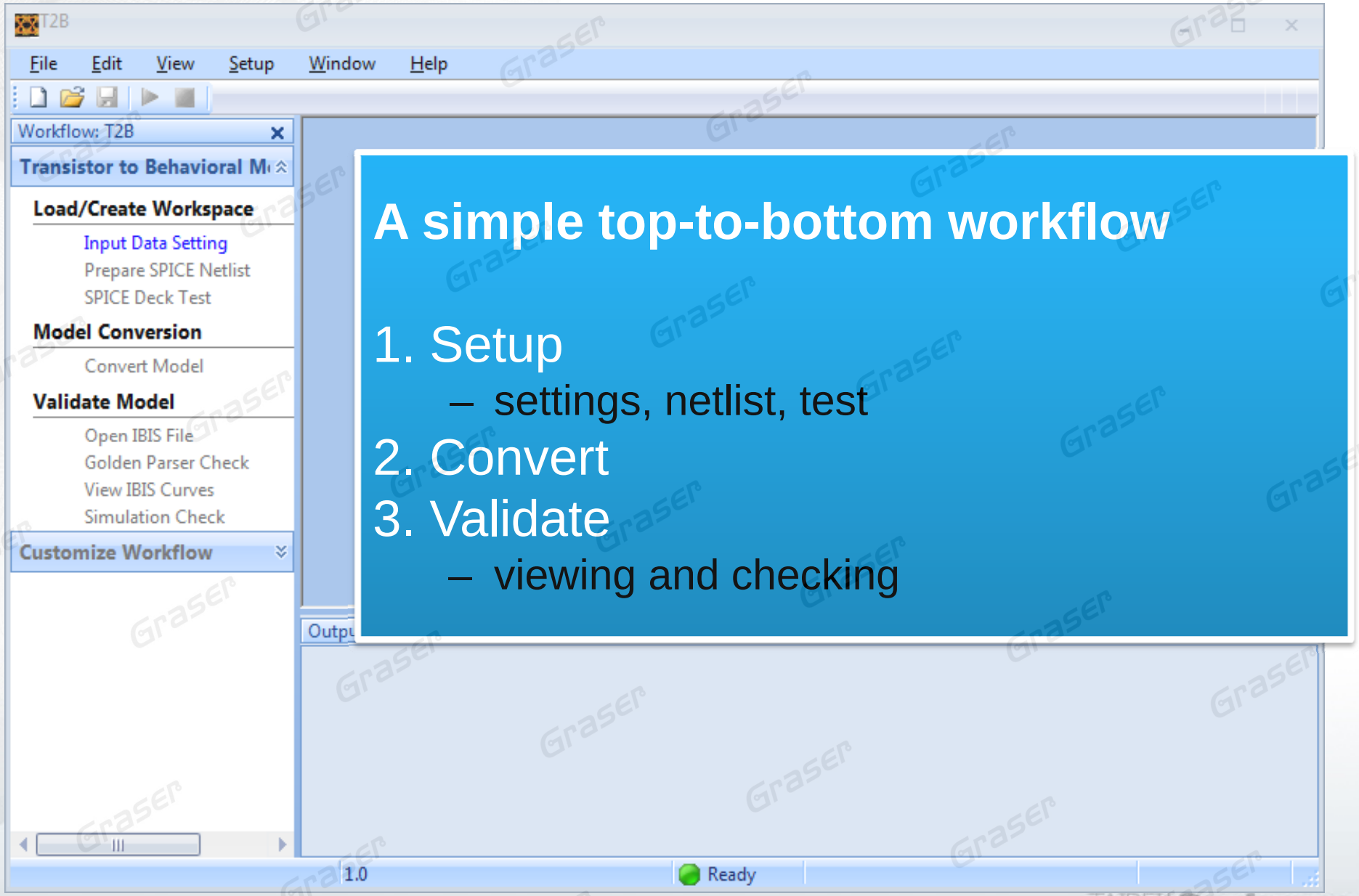


System Requirements

- Circuit simulation engine
  - HSPICE E-2010.12 or later
  - SPDSIM 11.0 or later
  - Spectre (conversion only, no IBIS 5.0 support yet)

- Environment variables setting
  - HSPICE licensing environment variable
  - Path to HSPICE executable

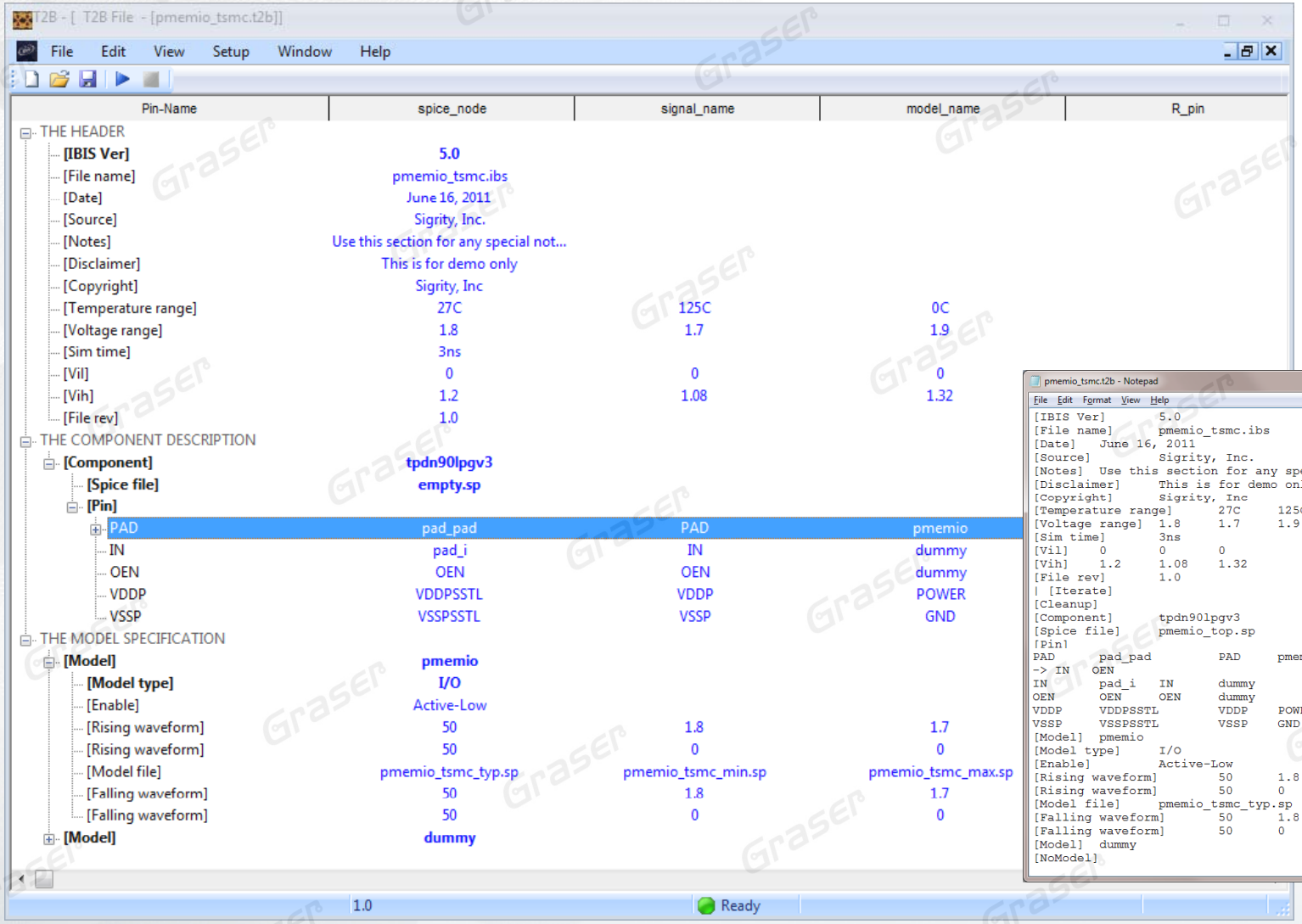
T2B Workflow

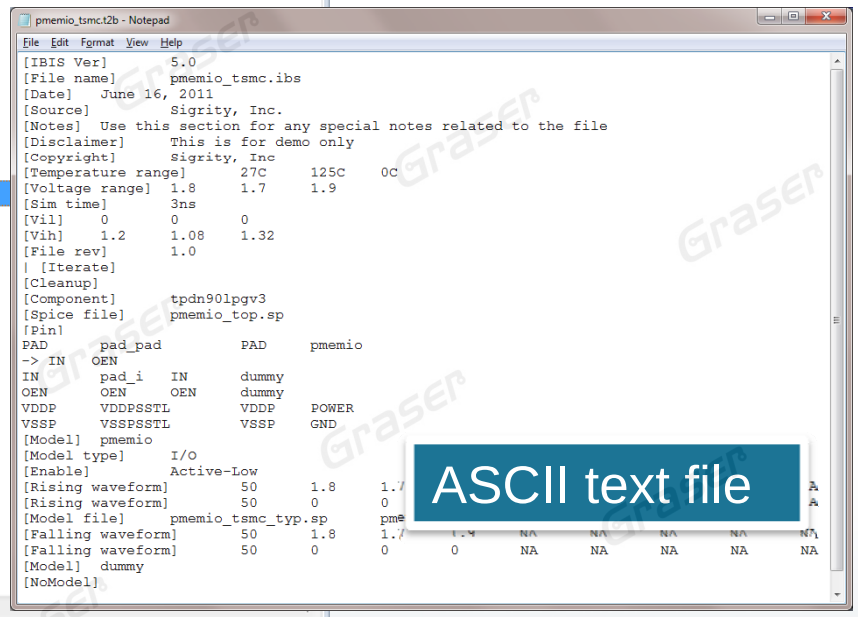


A simple top-to-bottom workflow

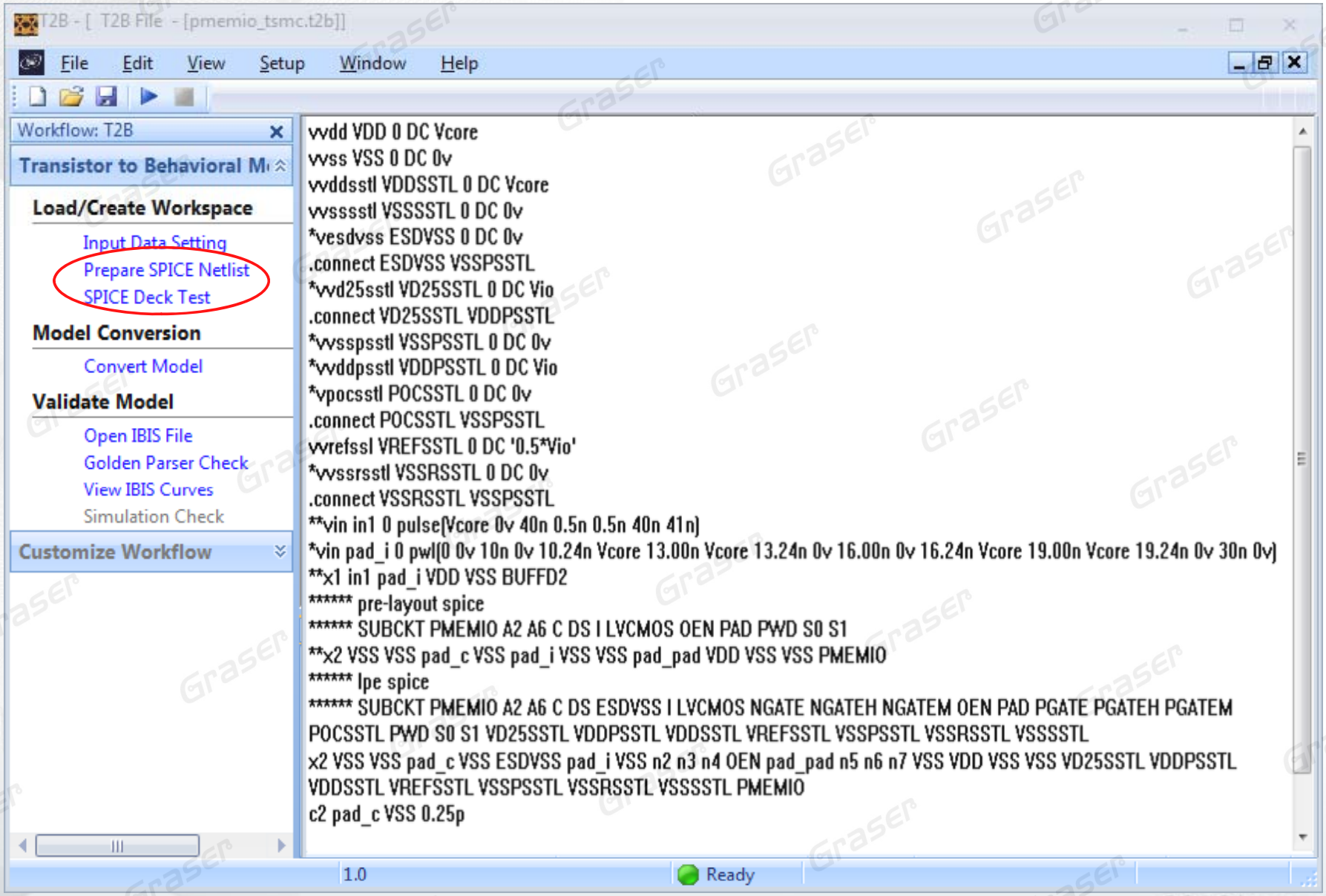
1. Setup
   - settings, netlist, test
2. Convert
3. Validate
   - viewing and checking

Setup - Intelligent Spreadsheet Setup GUI

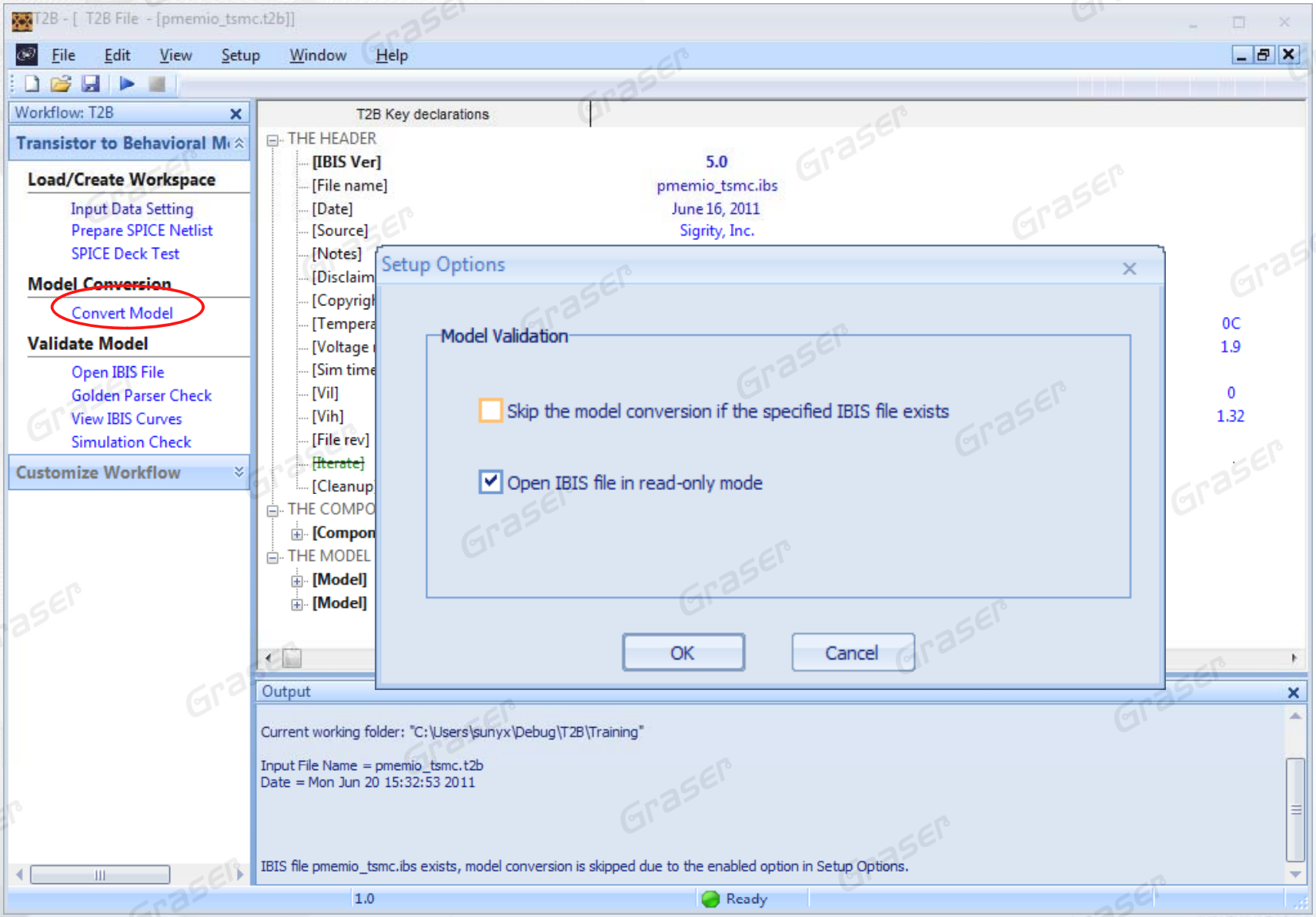




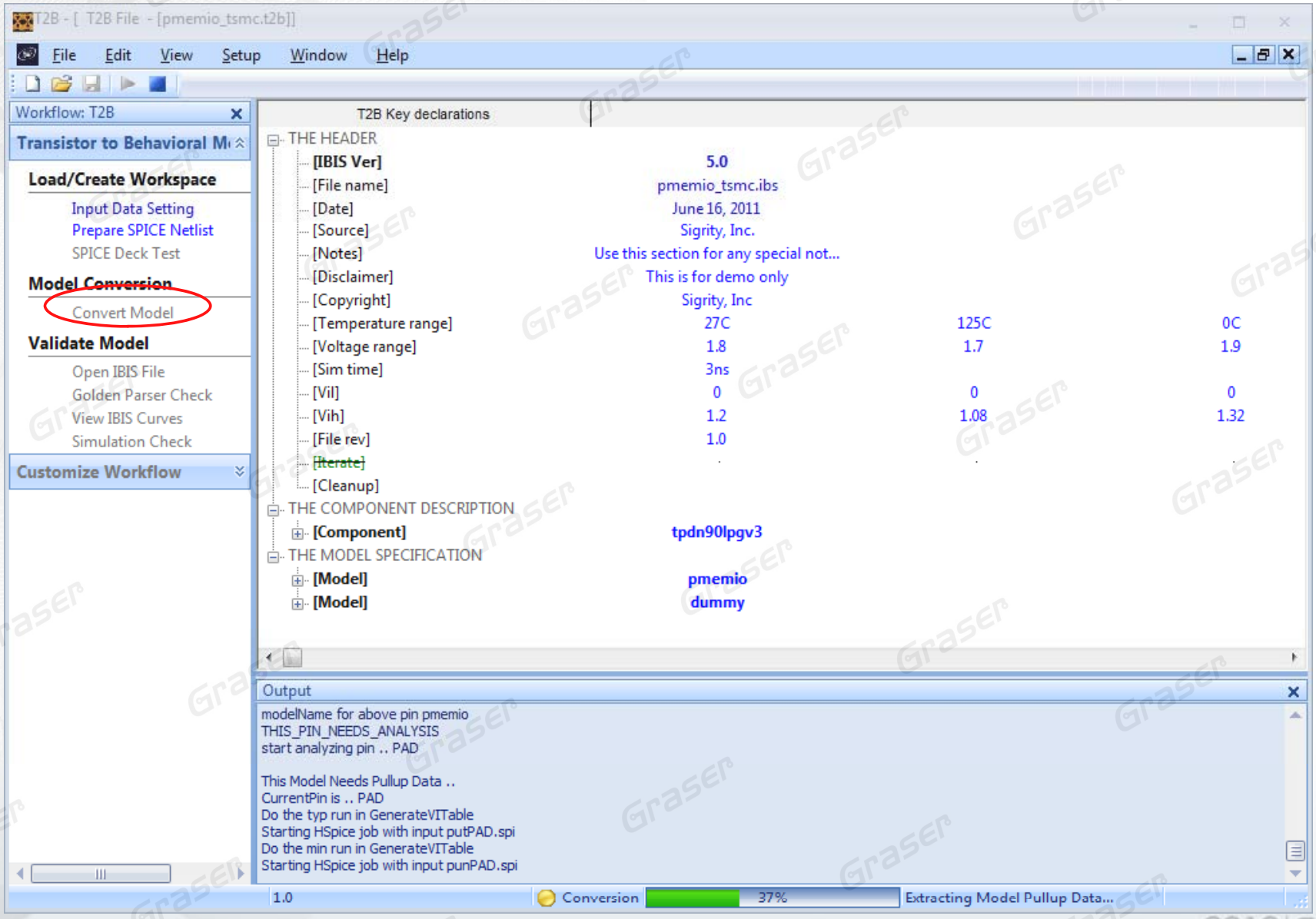
Setup - Prepare and Test the Netlist Call



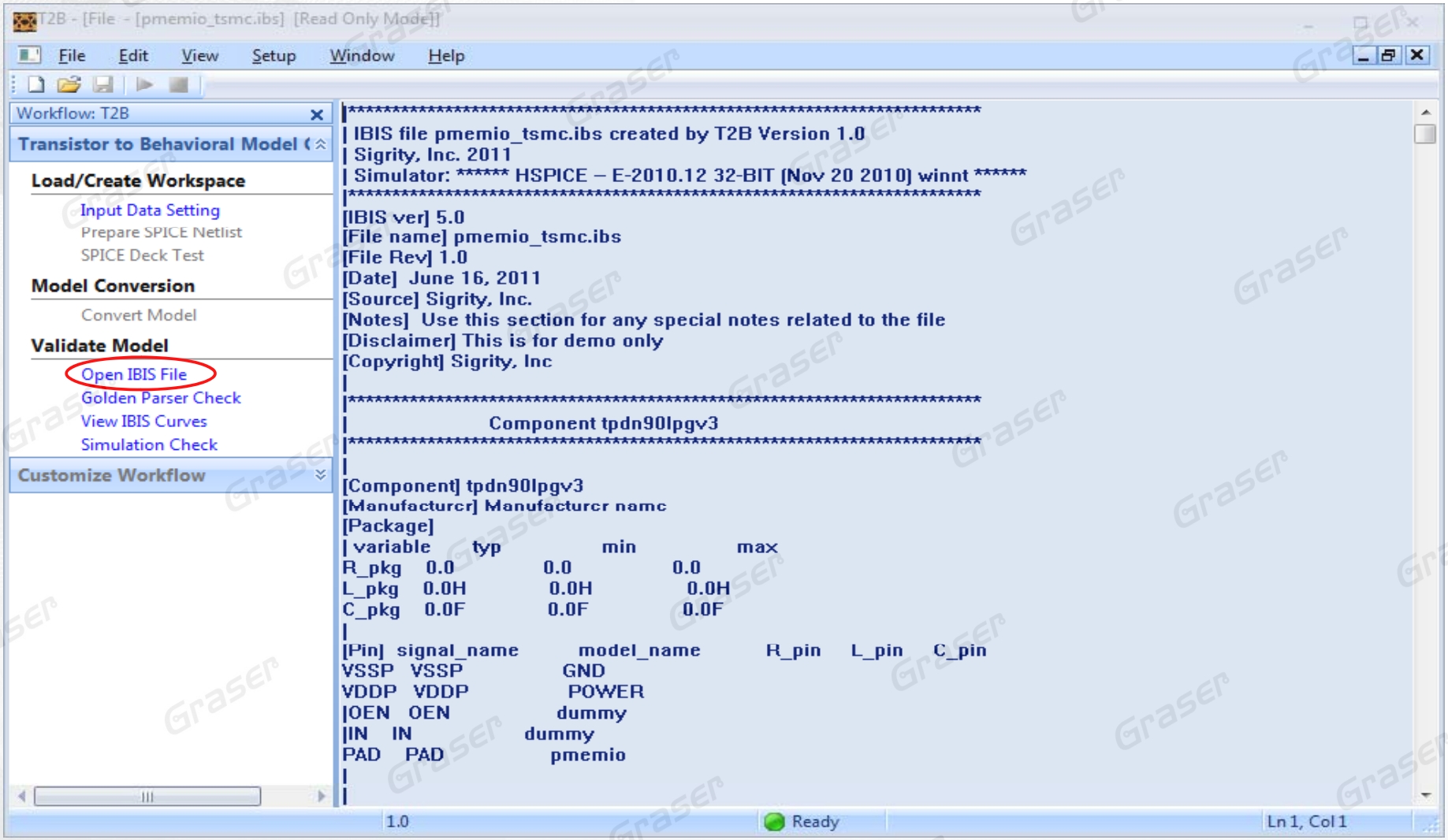
Launch the Conversion



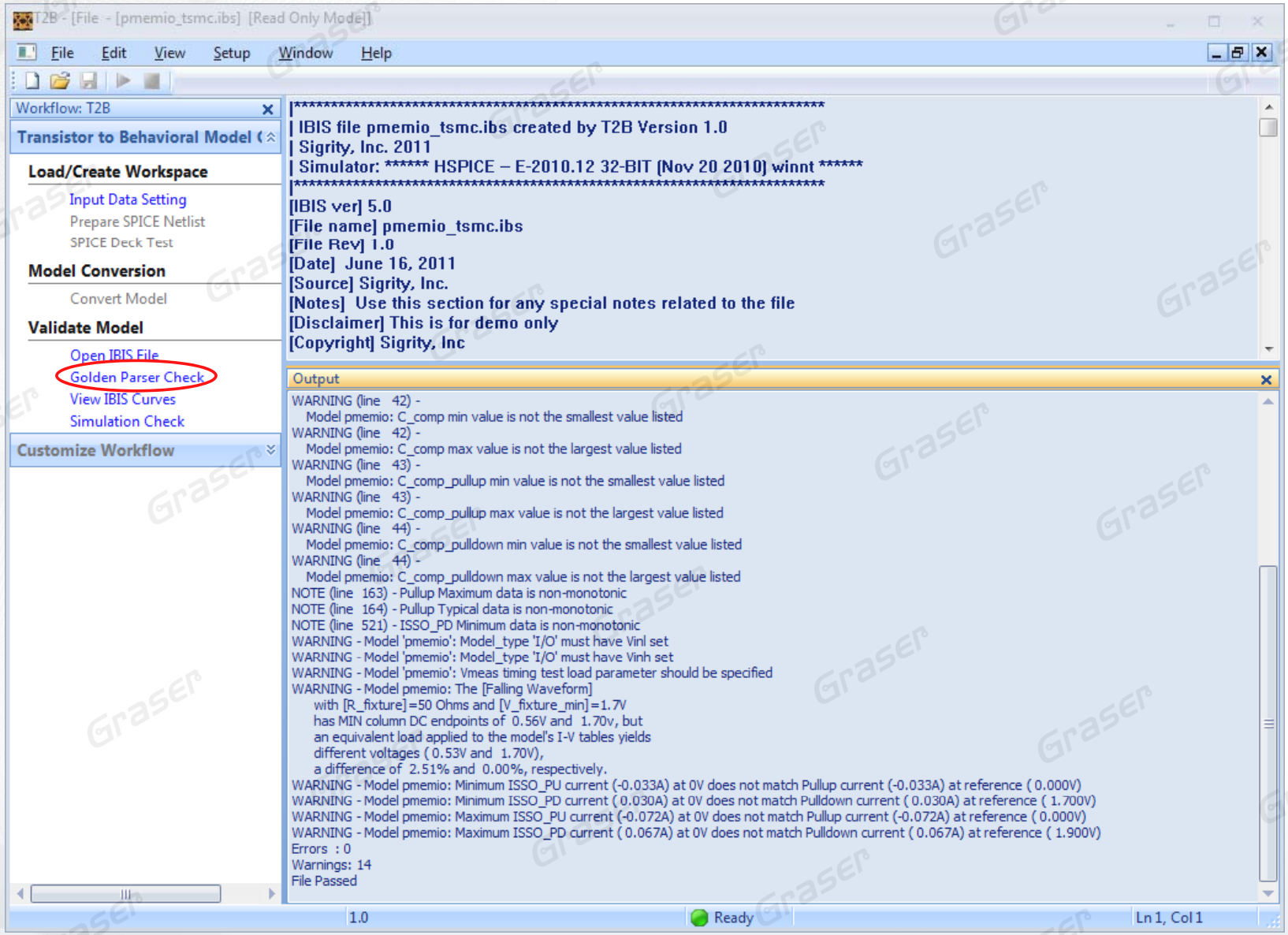
Progress Messages are Displayed



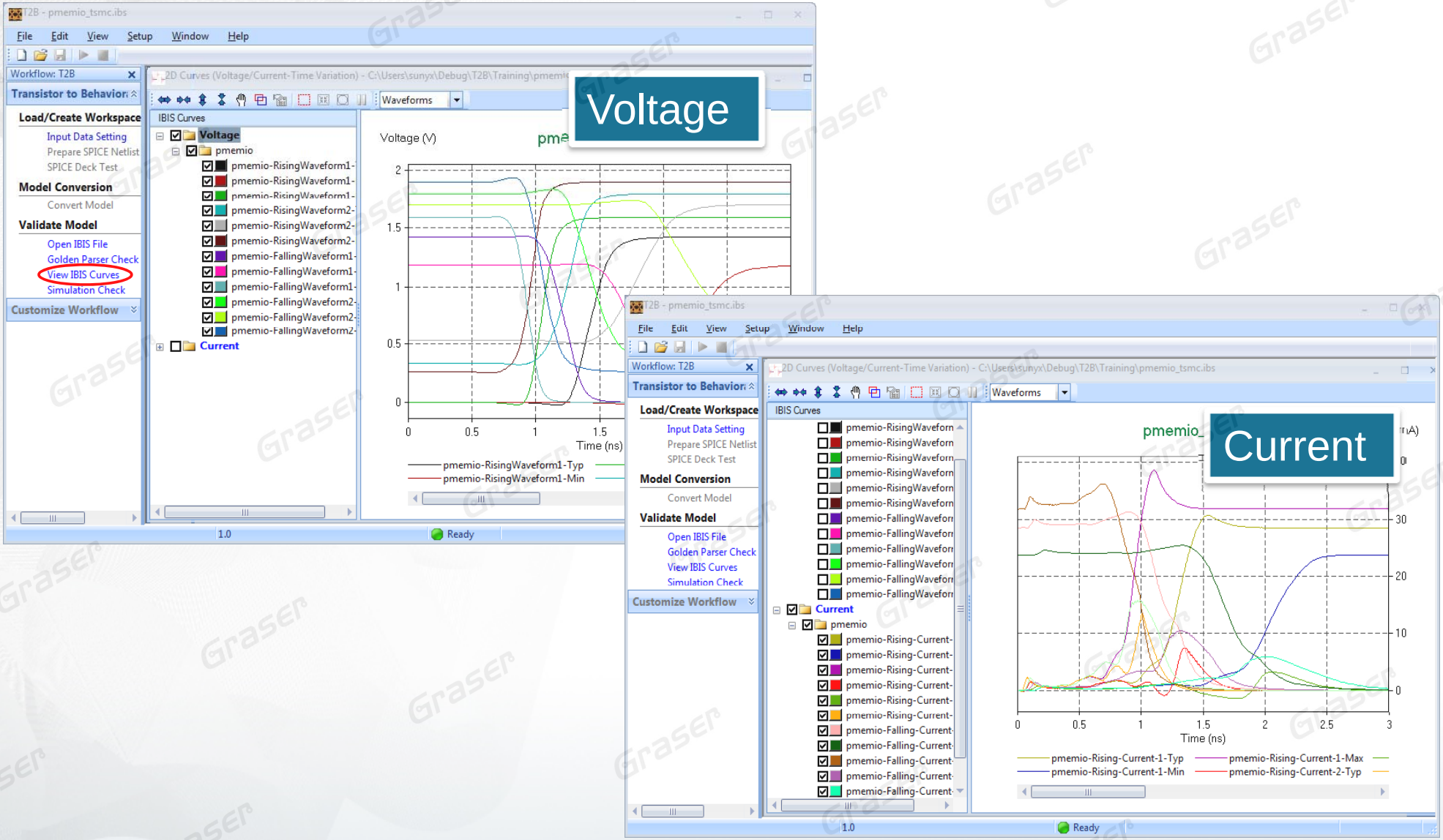
Validation - View the IBIS File



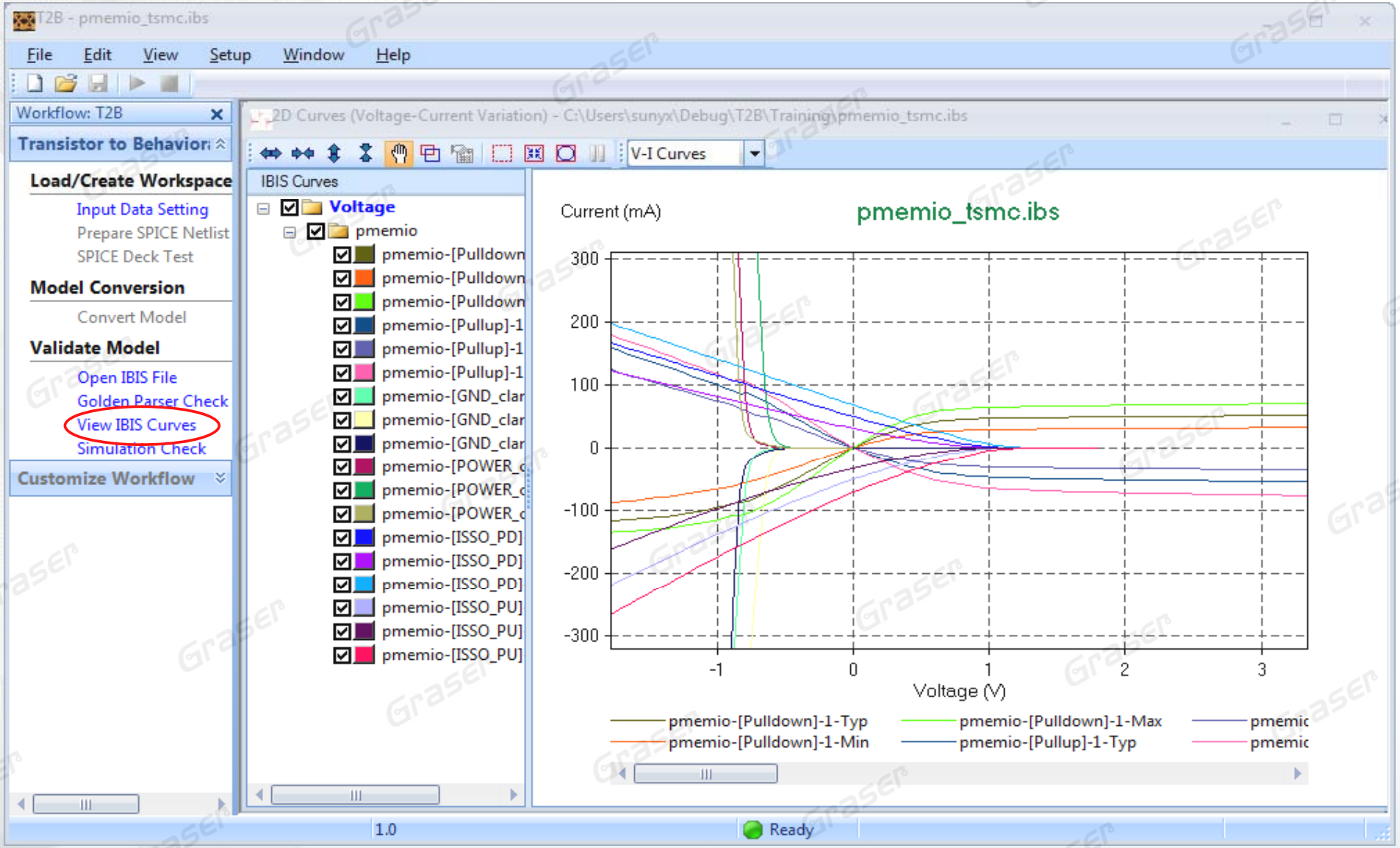
Validation - Warnings from the Golden Parser



Validation - View Transient Waveforms



Validation - View the IBIS V-I Curve

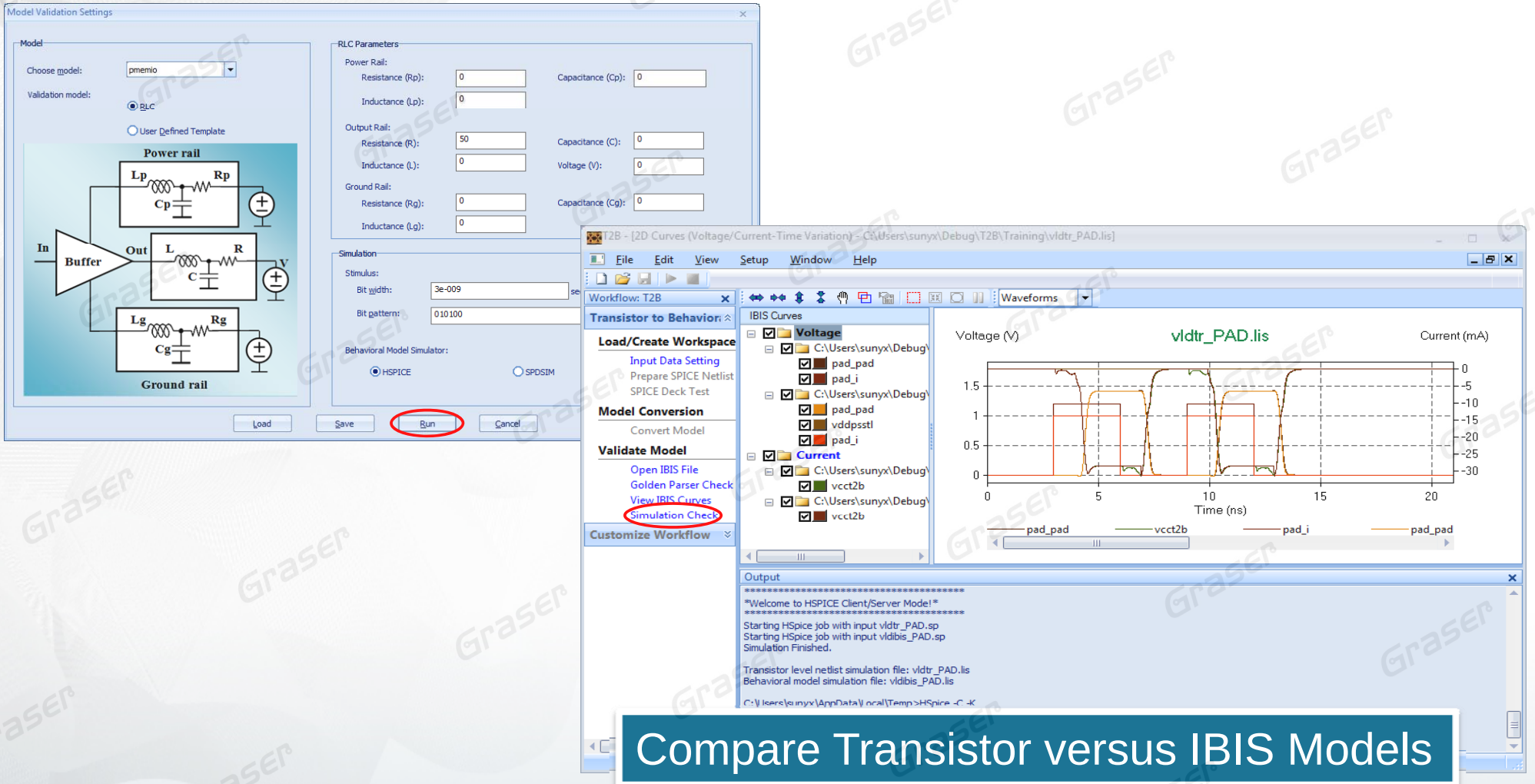


Validation - Power-Aware IO Modeling

- Power-aware IO modeling
  - SSO is typically dominated by power delivery effects
  - IBIS 5.0 power-aware models are produced by T2B
  - Sigrity IBIS Plus model provides even better power currents

Validation - Setup and View Circuit Simulation

With Supply Parasitics and Signal Load



Compare Transistor versus IBIS Models

Summary

- Converts SPICE transistor-level IO models to power-aware behavioral models
- Enables SSO and other power delivery dominated simulations
- Provides
  - Complete automation of IBIS 5.0 power-aware models
    - from internal or vendor supplied SPICE models
  - Simply calls HSPICE or SPDSIM engines
  - **Front-end and back-end** GUI
    - for easy setup and thorough validation
  - Cadence/Sigrity support
    - for applications and ongoing flow/technology improvements