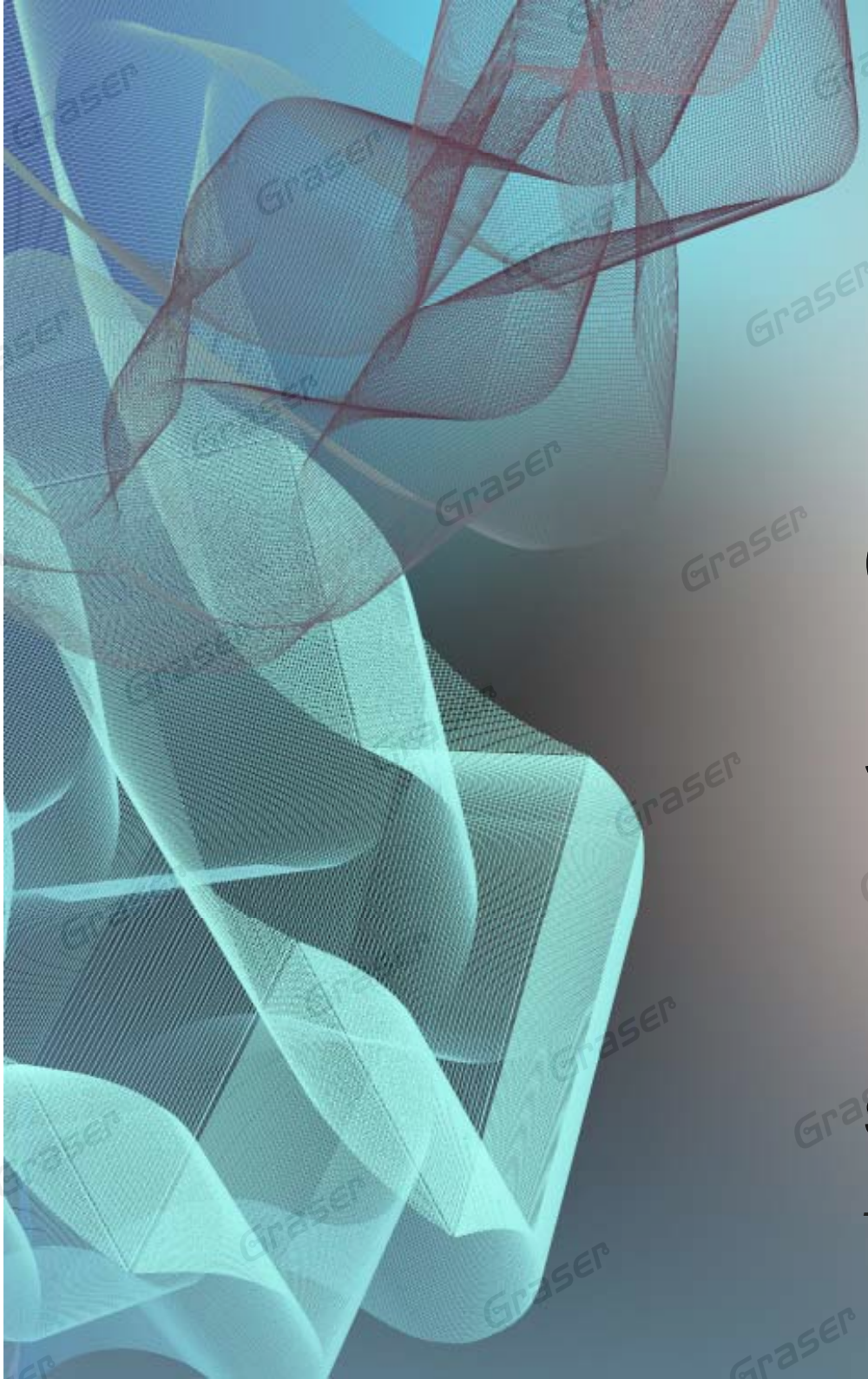


2013 AUG 13 TAIPEI Graser User Conference

New!! Customize IC Design and Simulation Flow

Stacy Chen / Scott Liu

13/Aug/2013

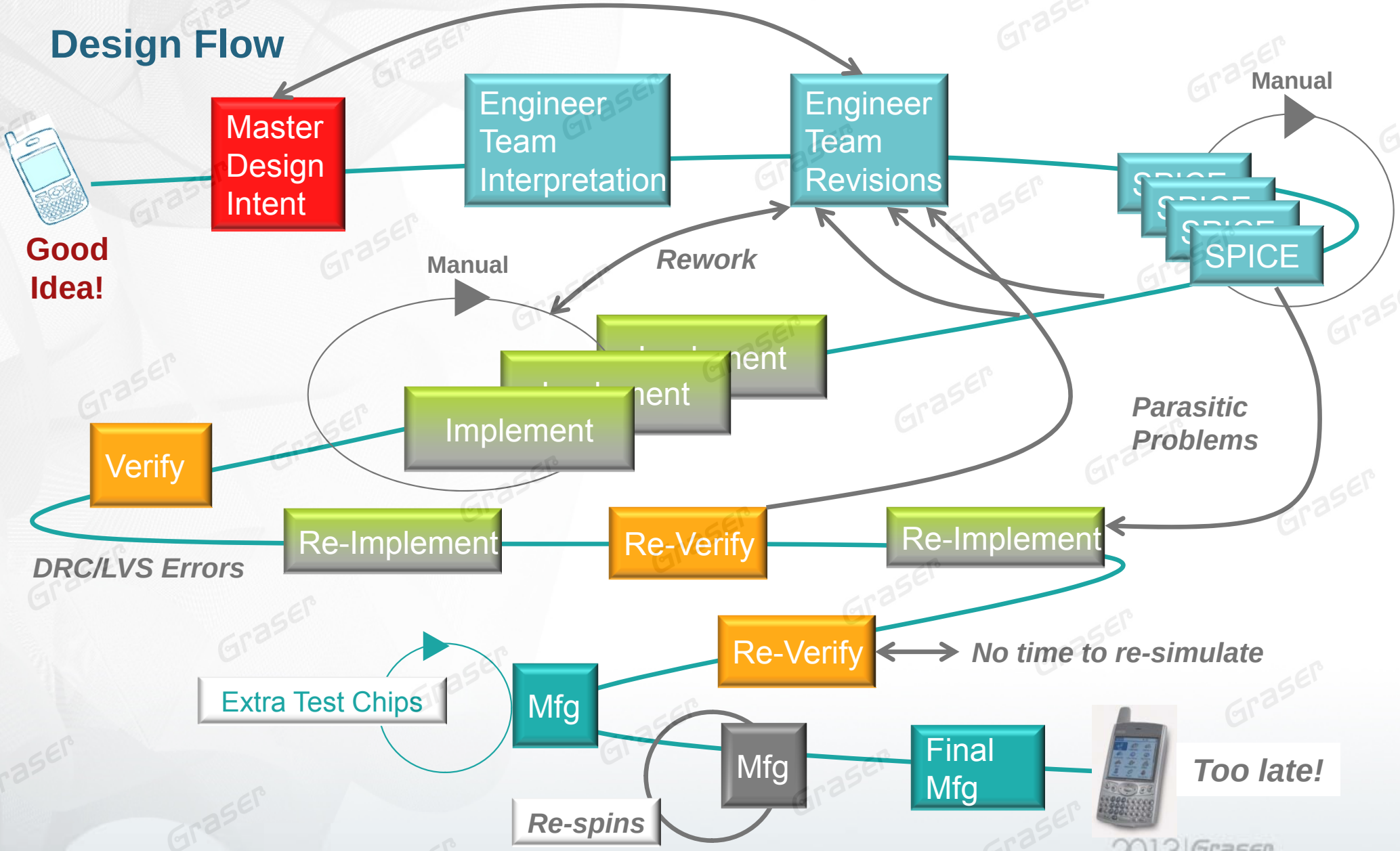
Topic

- Overview
  - Challenges
  - Cadence's Complete Solution
- Virtuoso Custom Design and Verification
  - Ease and Speed to develop the largest and complex schematic
    - **Virtuoso Schematic Editor**
  - Fast and Accurate design verification
    - **Analog Design Environment**
    - **Multi-Mode Simulation**
- Virtuoso Custom Implement
  - Rapid layout implementation
    - **Virtuoso Layout Suite**
- Summary

Overview

Overview

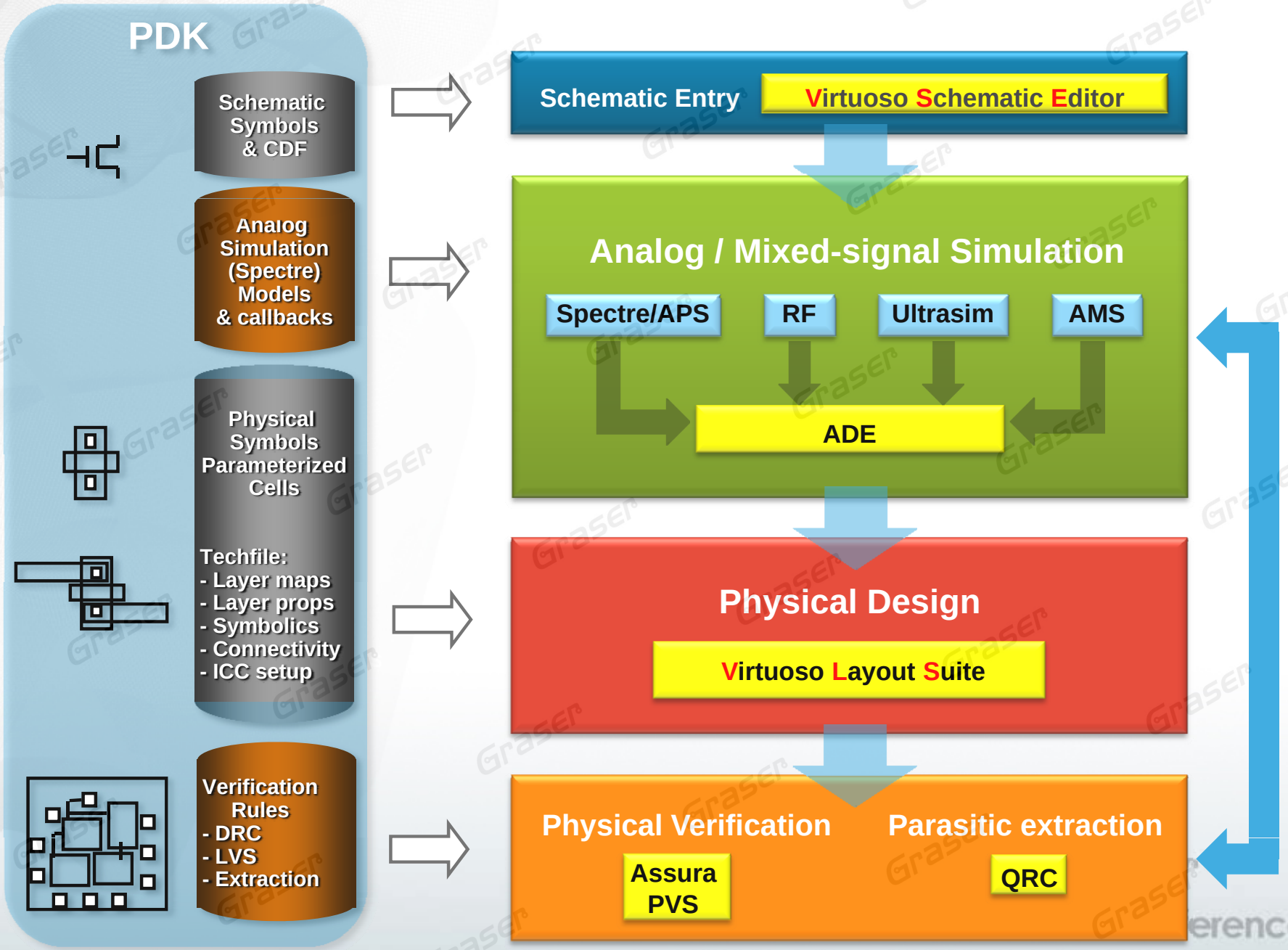
Design Flow



Overview

Latest Version IC6.1.6

Cadence's complete custom design for front to back analog, RF, and mixed-signal



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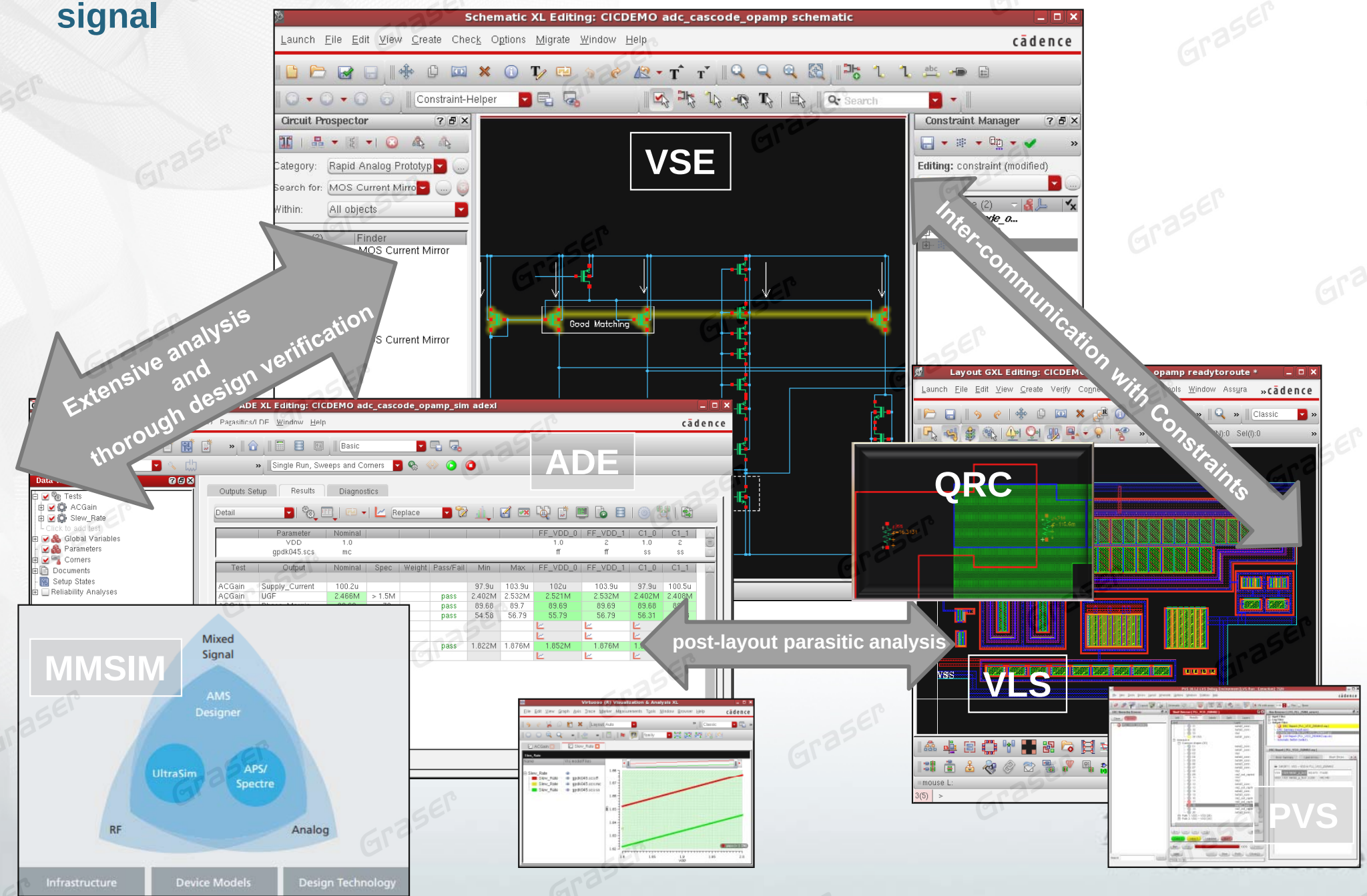
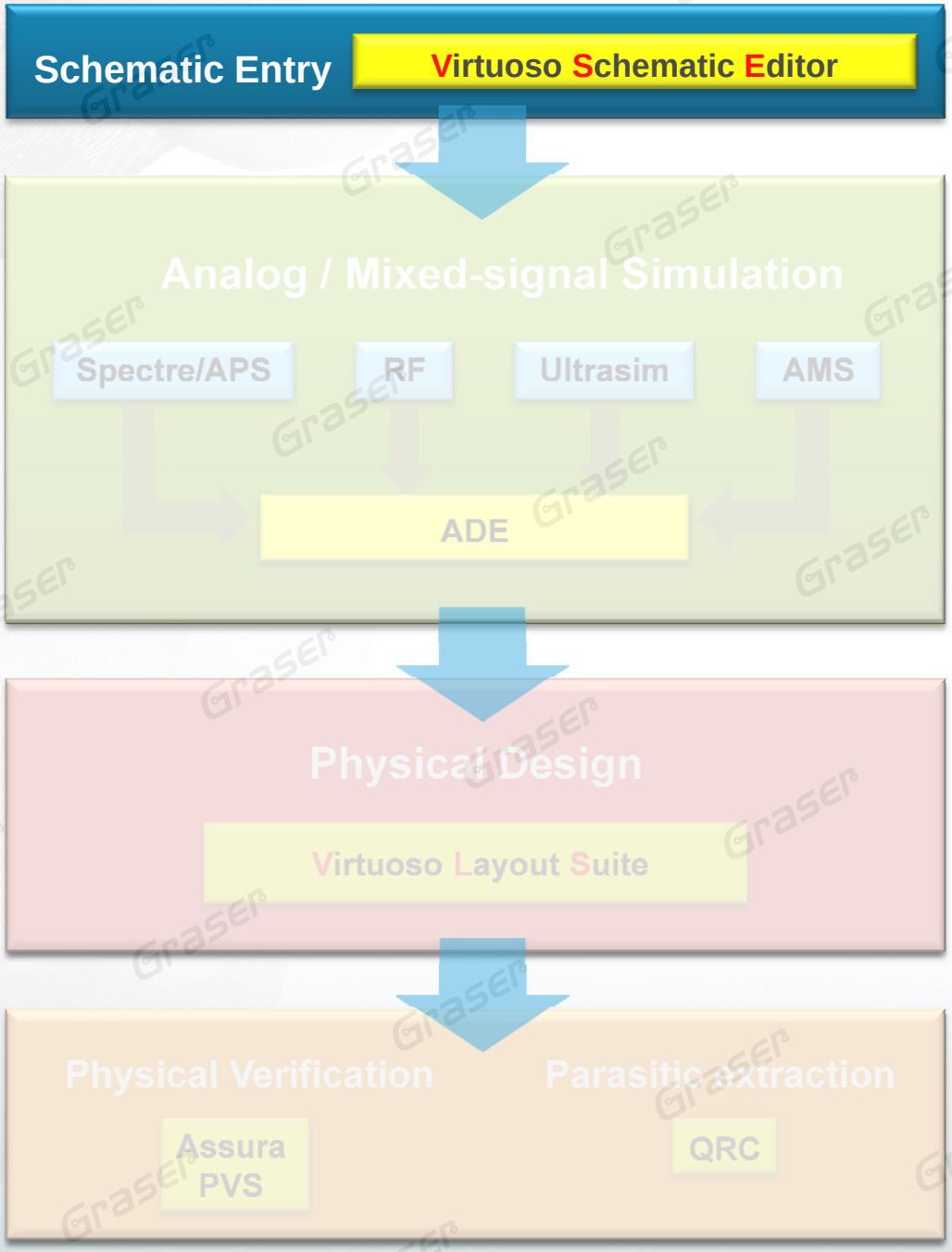


Virtuoso Custom Design and Verification

Ease and Speed to develop the largest and complex schematic
Fast and Accurate design verification

Virtuoso Custom Design and Verification

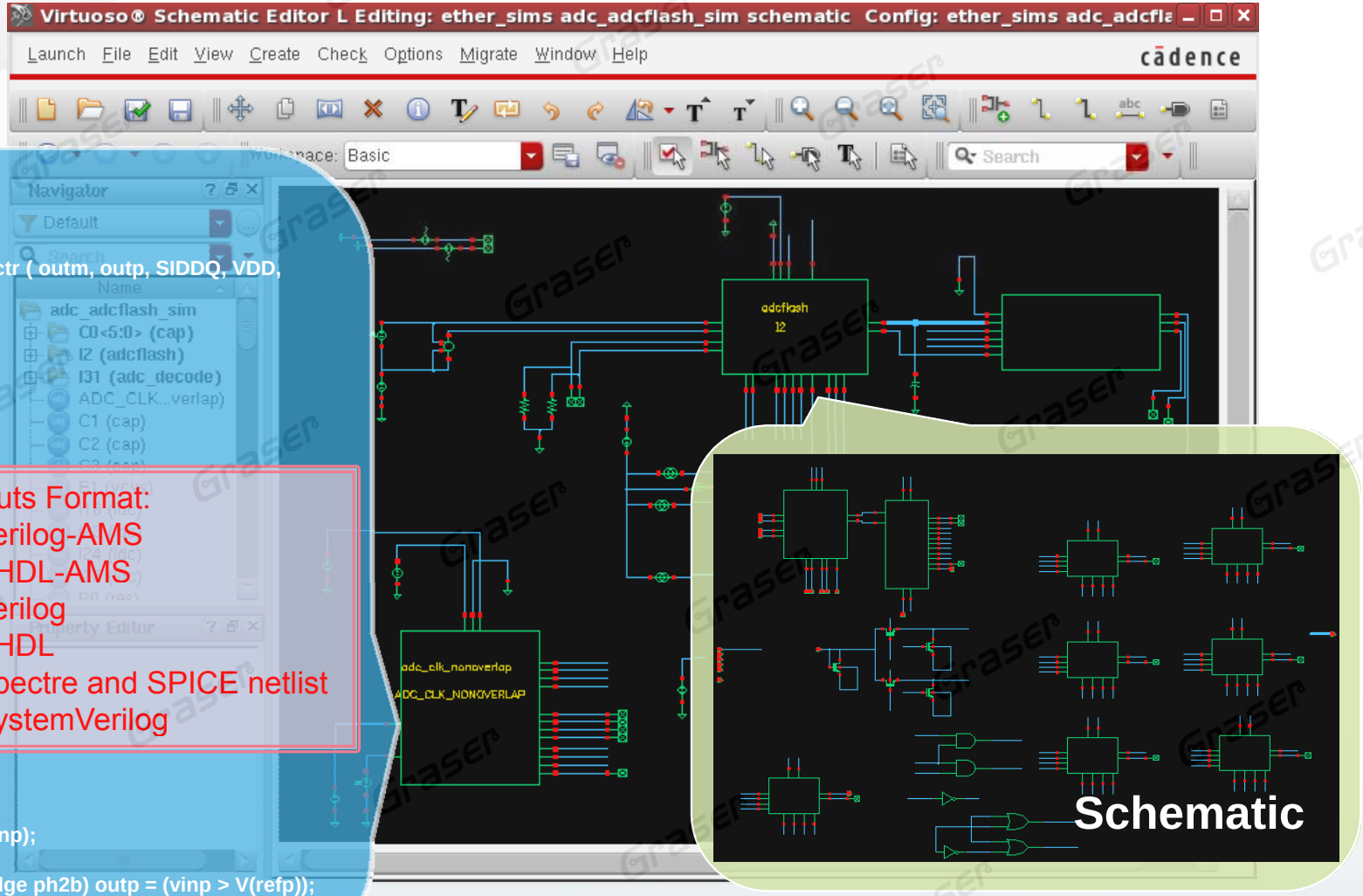


Virtuoso Schematic Editor

- Hierarchical schematic entry and hierarchy editor supports
- Analog, digital, mixed-signal, and RF symbol libraries are supported

```
`include "constants.vams"
`include "disciplines.vams"

module adcflash_comparator_actr ( outm, outp, SIDDQ, VDD,
VSS, inn, inp, ph1,
   ph2b, refn, refp, vbias );

output  outp, outm;
input   inp, inn;
input   ph1, ph2b;
input   refp, refn;
input   VDD, VSS, vbias;
input   SIDDQ;

logic       outp, outm;
logic       ph1, ph2b;
logic       SIDDQ;
electrical    inp, inn;
electrical    refp, refn;
electrical    VDD, VSS;
electrical    vbias;

real vinp, vinm;
reg  outp;
wire outm = ~outp;

analog  vinp = (SIDDQ) ? 0.0: V(inp);
initial outp = 1'b0;
always @(posedge ph1 or posedge ph2b) outp = (vinp > V(refp));

endmodule
```

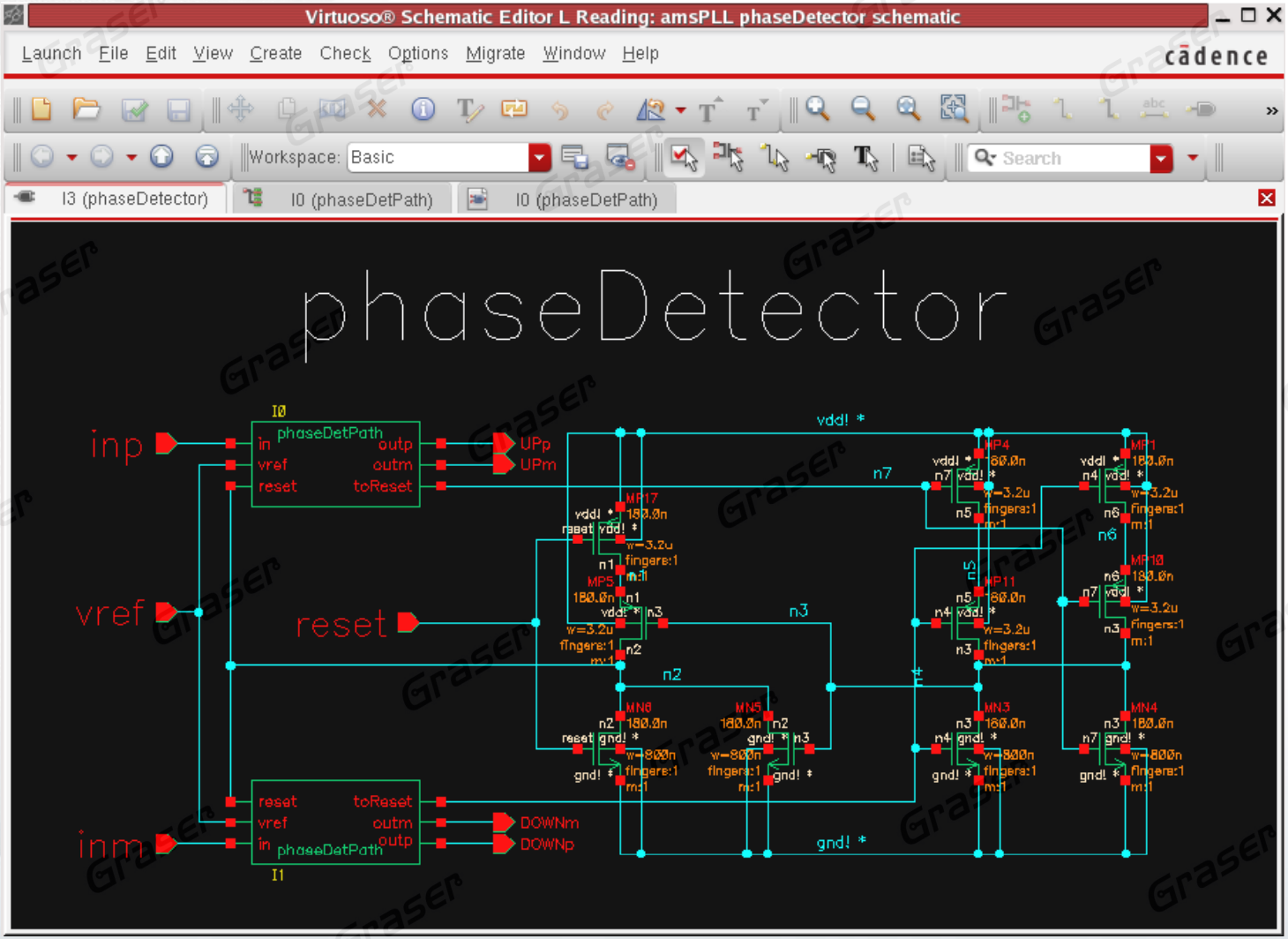
Inputs Format:
- Verilog-AMS
- VHDL-AMS
- Verilog
- VHDL
- Spectre and SPICE netlist
- SystemVerilog



Virtuoso Schematic Editor

Multi-tab / Multi-view canvas

- Open multiple schematics, or different views of the same design



Virtuoso Schematic Editor

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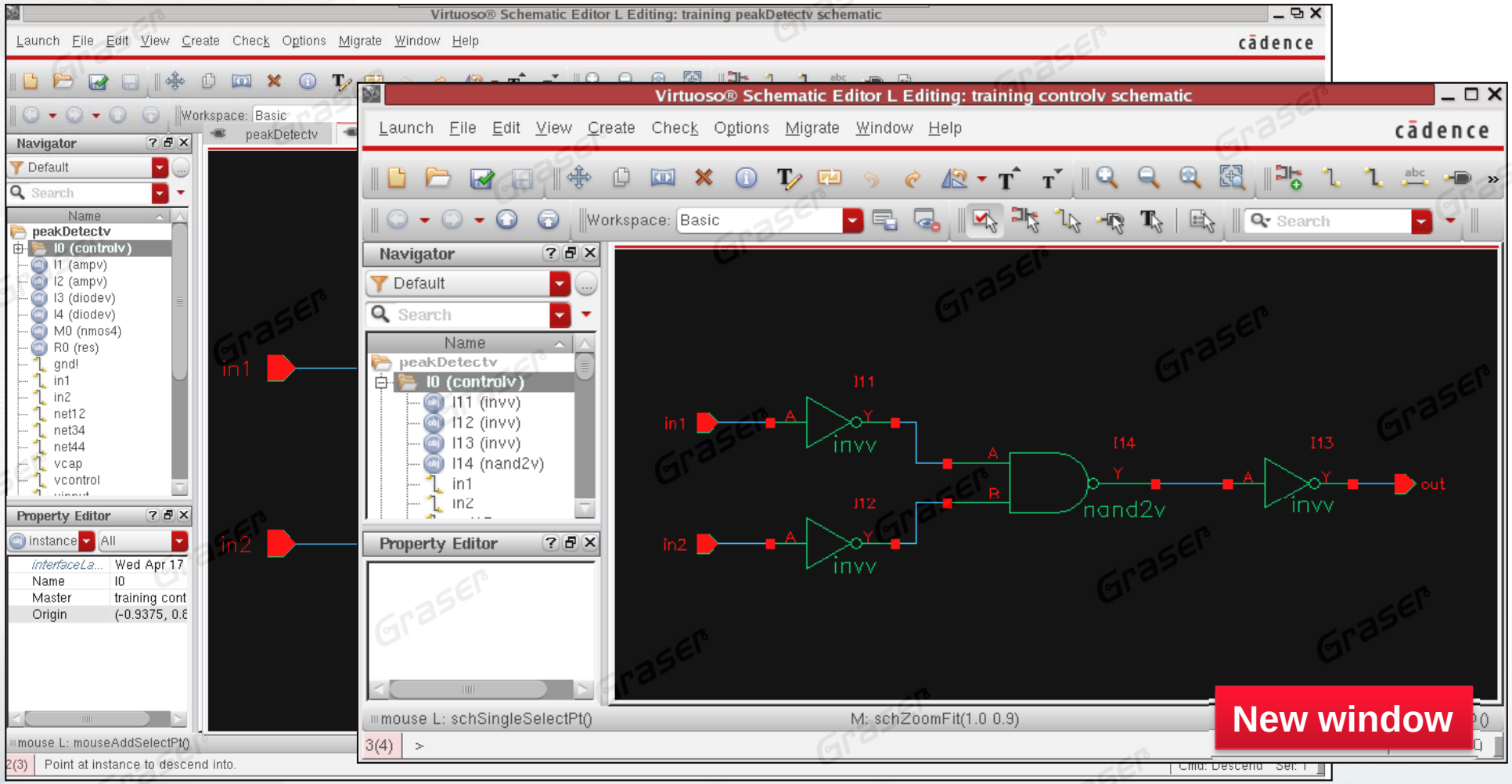
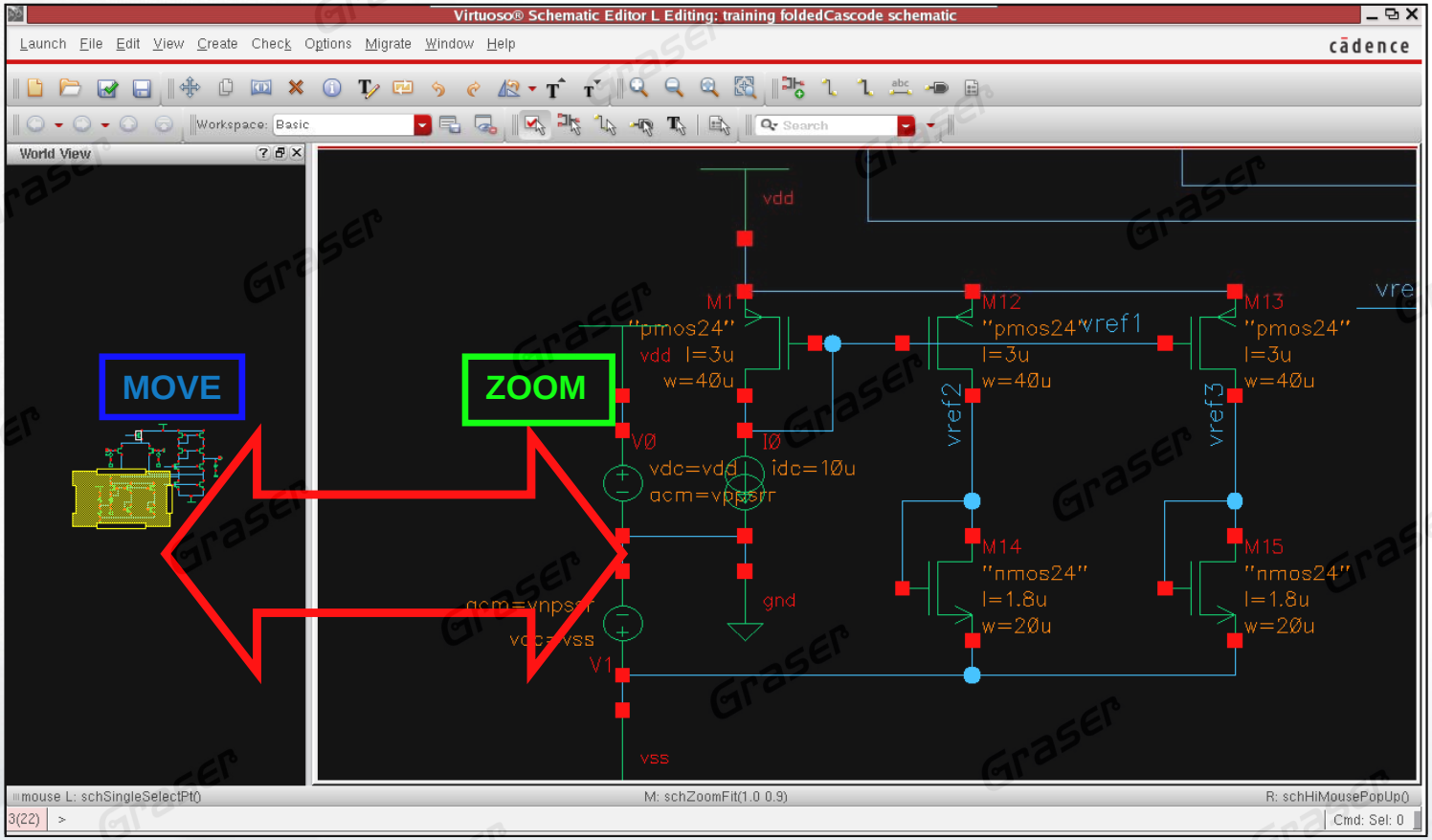


Virtuoso Schematic Editor

Design Task Assistants

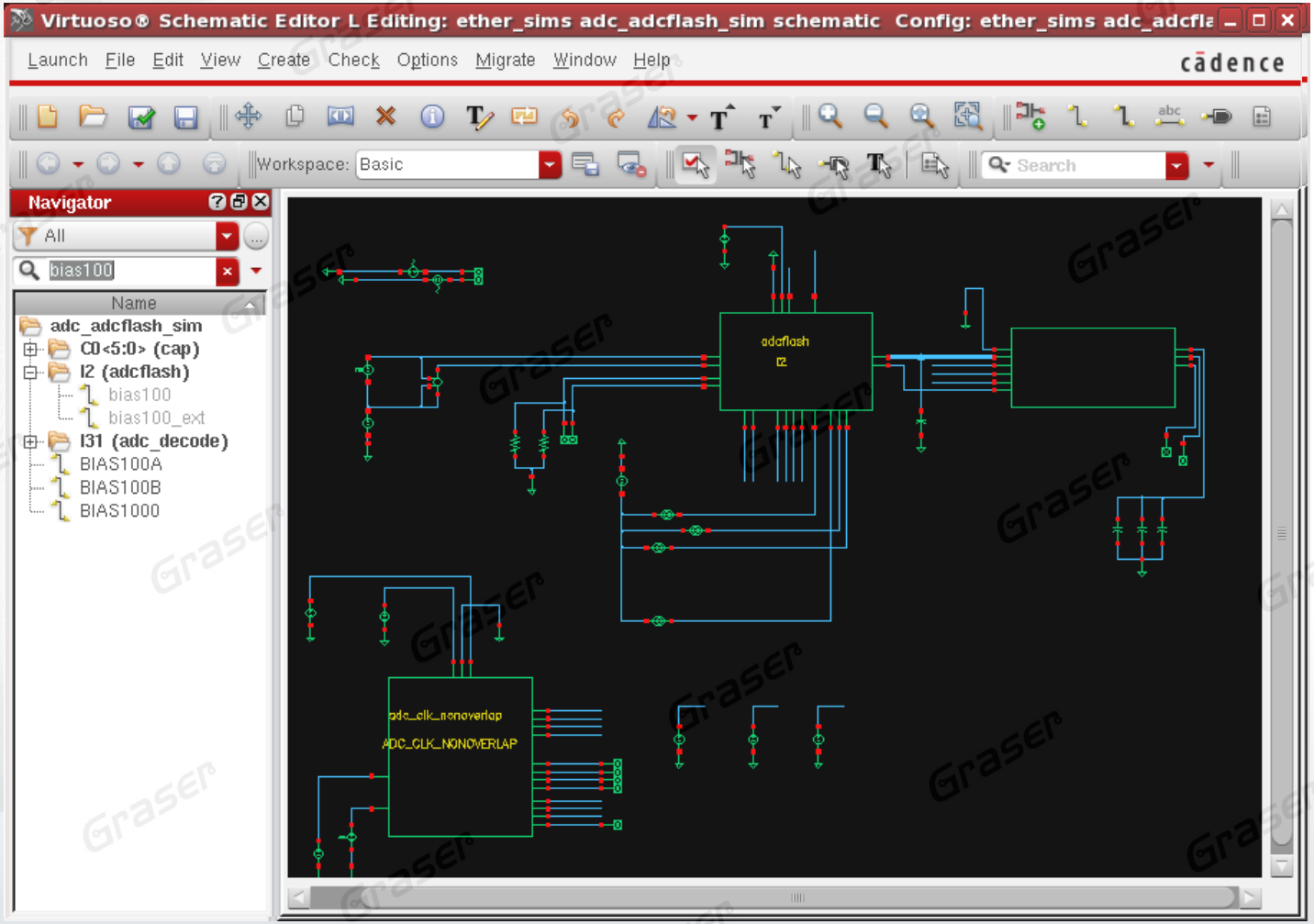
- World View Assistant
  - Panoramic view of an entire schematic
  - Indicating which portion of it is currently visible in the editor window



Virtuoso Schematic Editor

Design Task Assistants

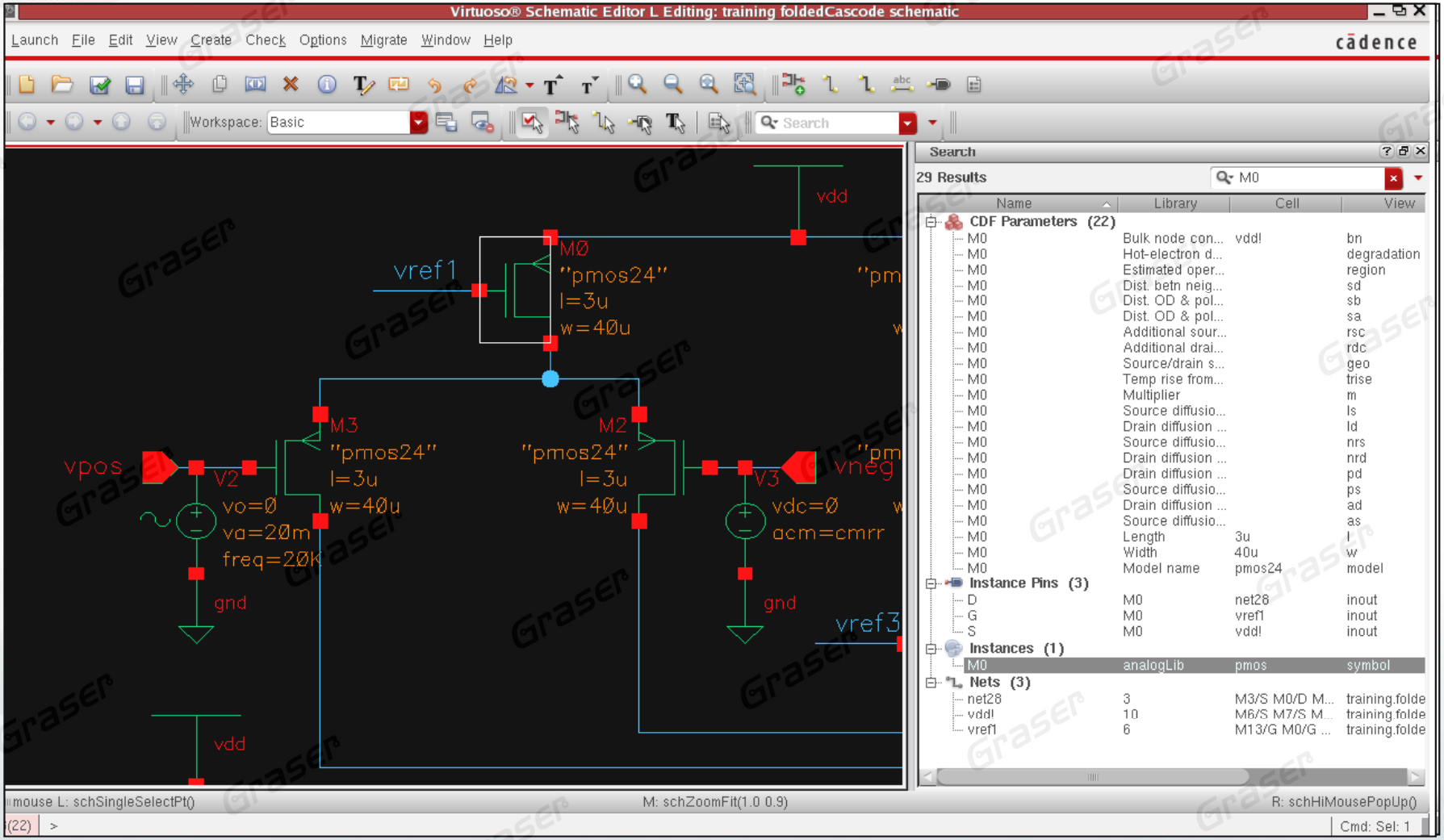
- Navigator Assistant
  - Efficient, intuitive access to the complete design hierarchy



Virtuoso Schematic Editor

Design Task Assistants

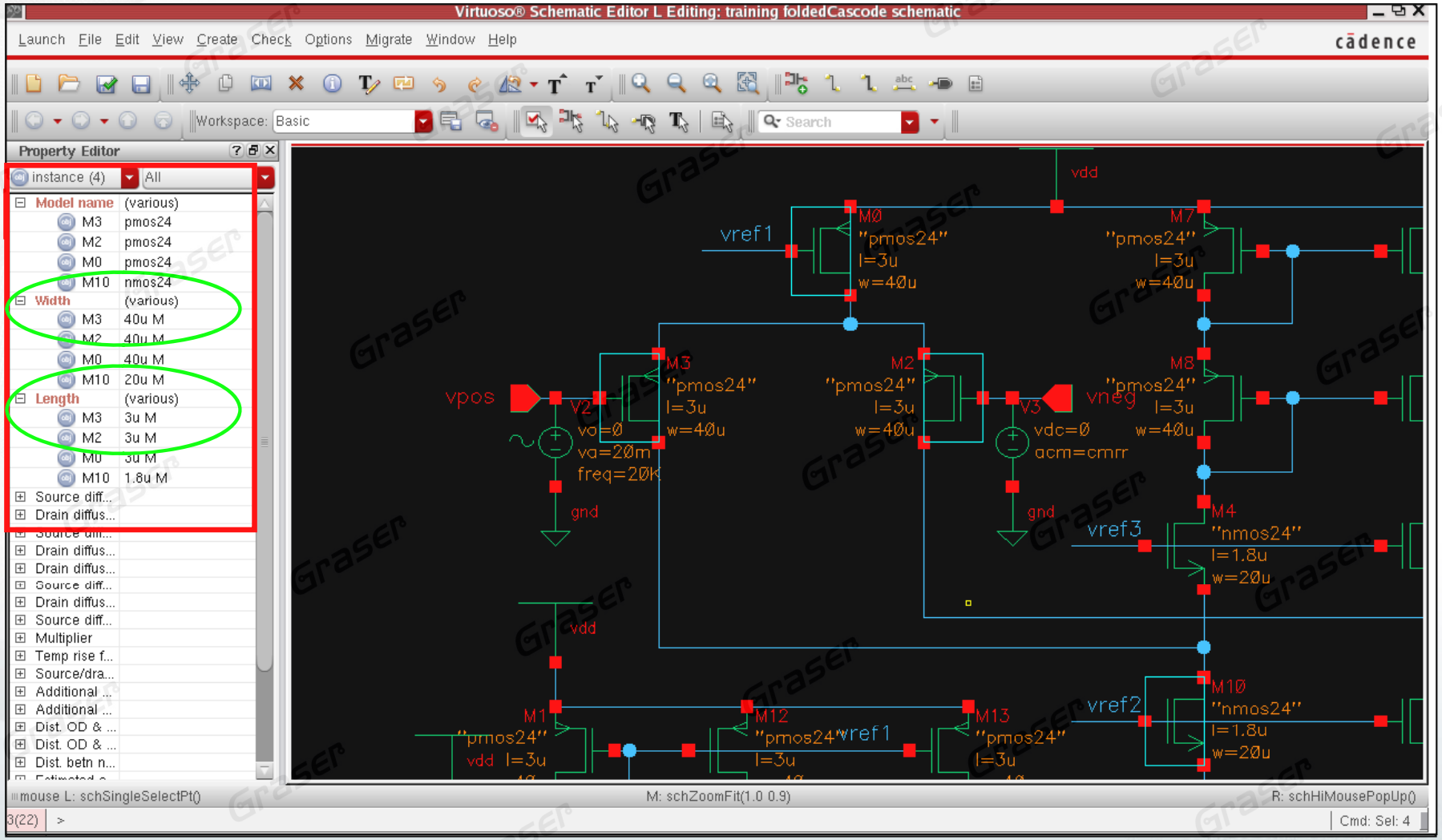
- Search Assistant
  - Quick, comprehensive search engine



Virtuoso Schematic Editor

Design Task Assistants

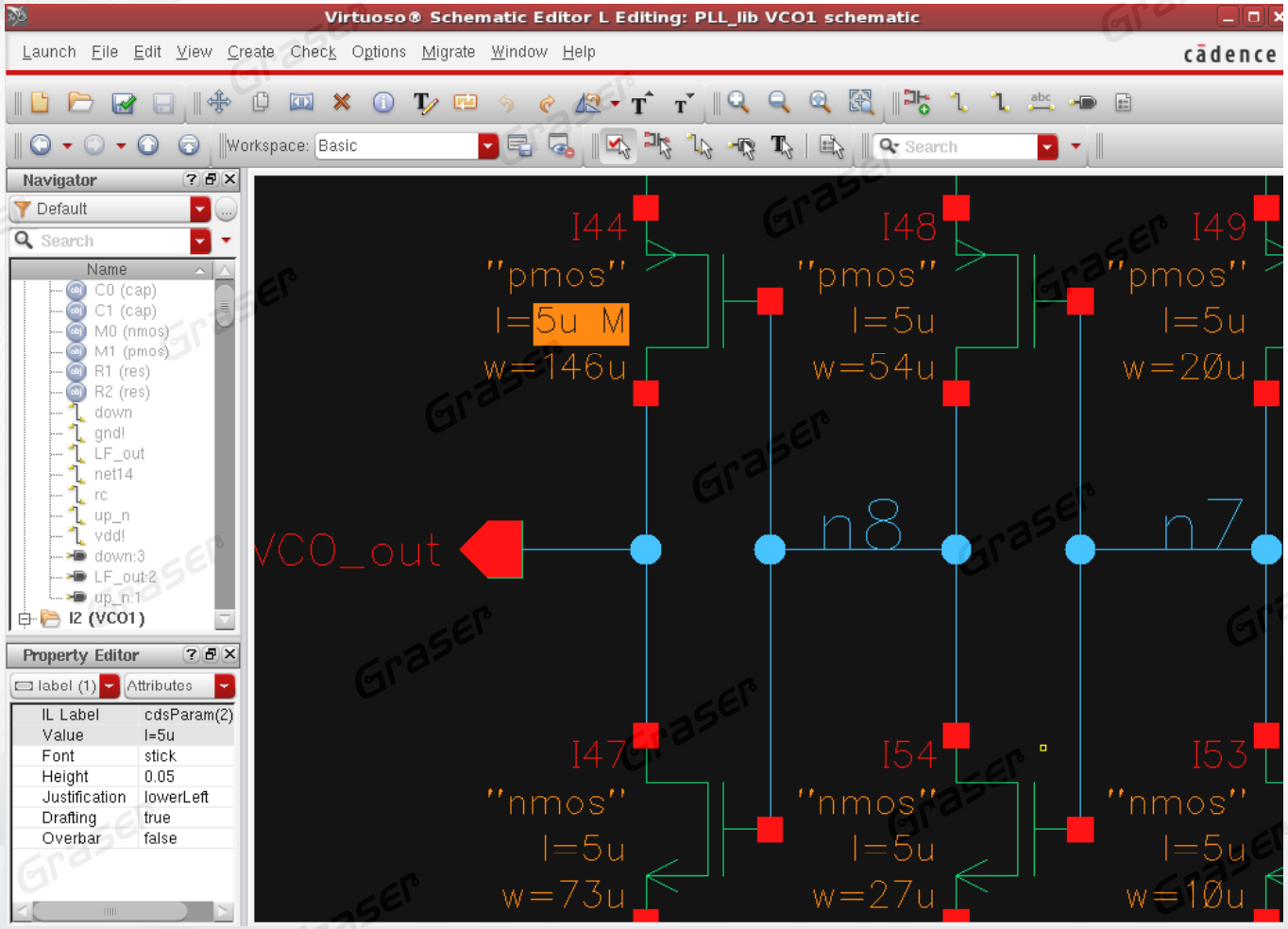
- Property Editor Assistant
  - Intuitive editing of multiple properties on a single object or multiple objects



Virtuoso Schematic Editor

Text Editing

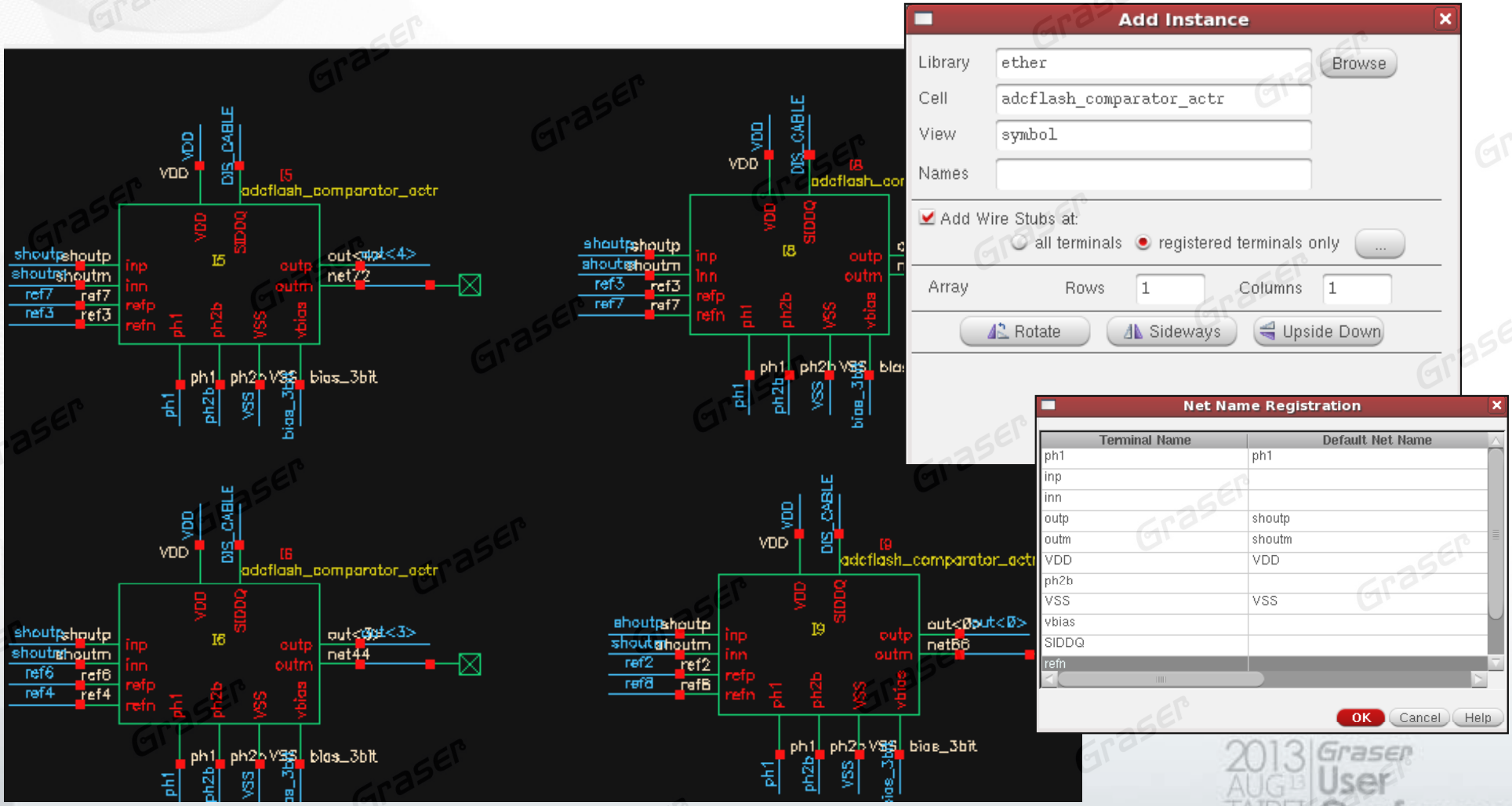
- Direct Text Edit
  - speed to change the values of text



Virtuoso Schematic Editor

Automatic creation wire stubs and labels

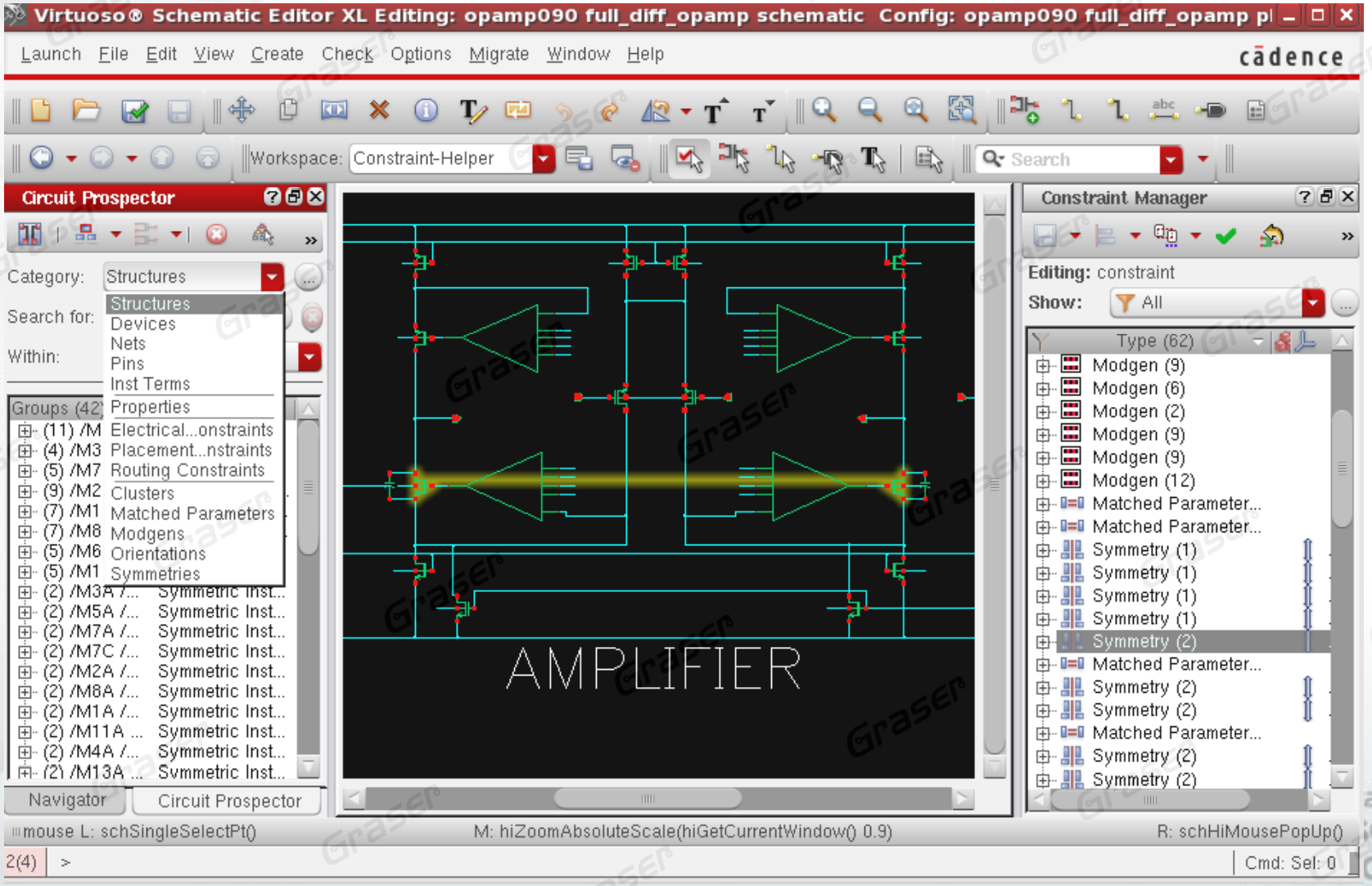
- Wire Stubs and Names
  - It allows automatic creation of such wire stubs and labels.



Virtuoso Schematic Editor

Constraint environment

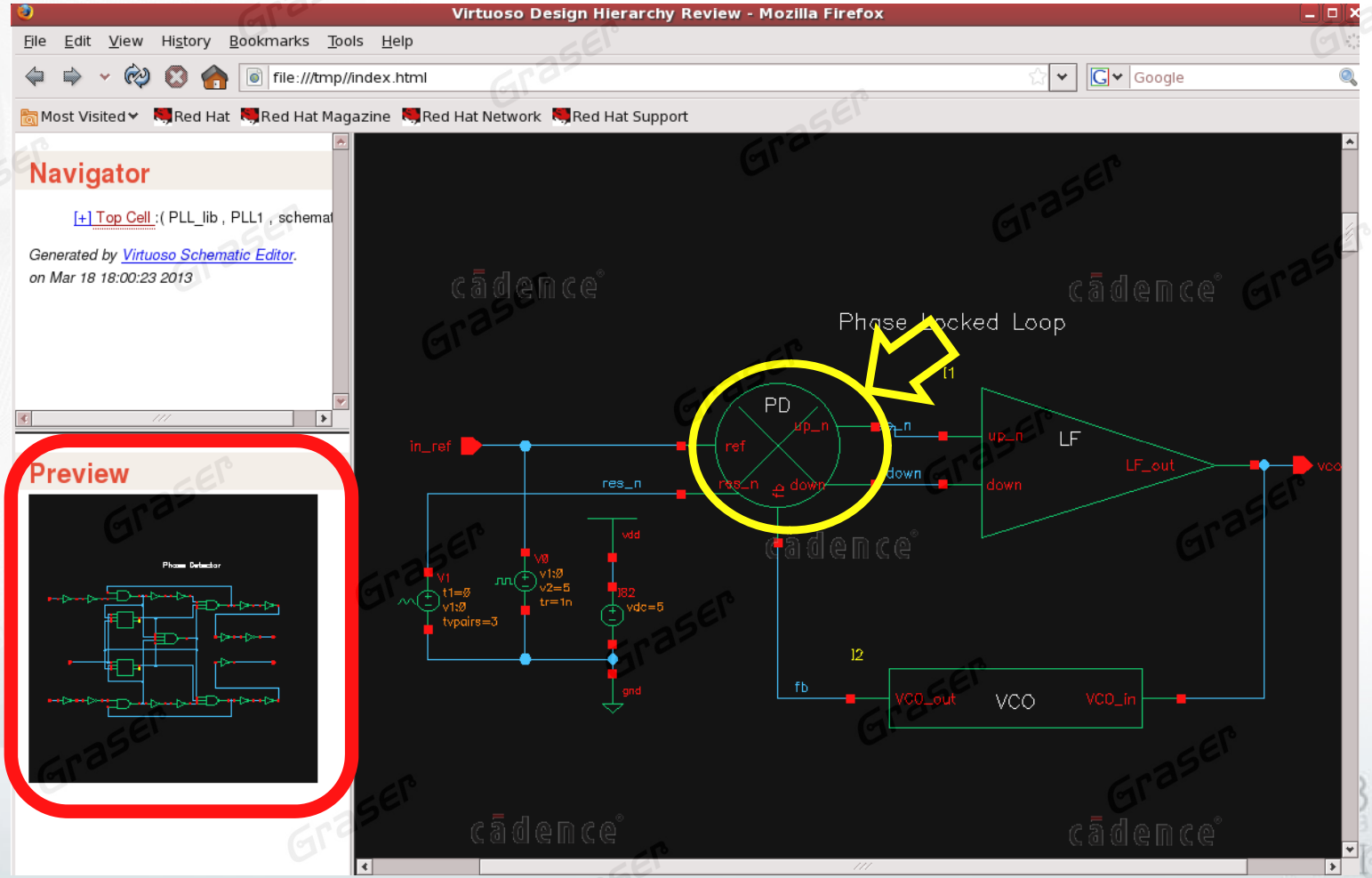
- Easily communicate critical design constraints between multiple users/sites



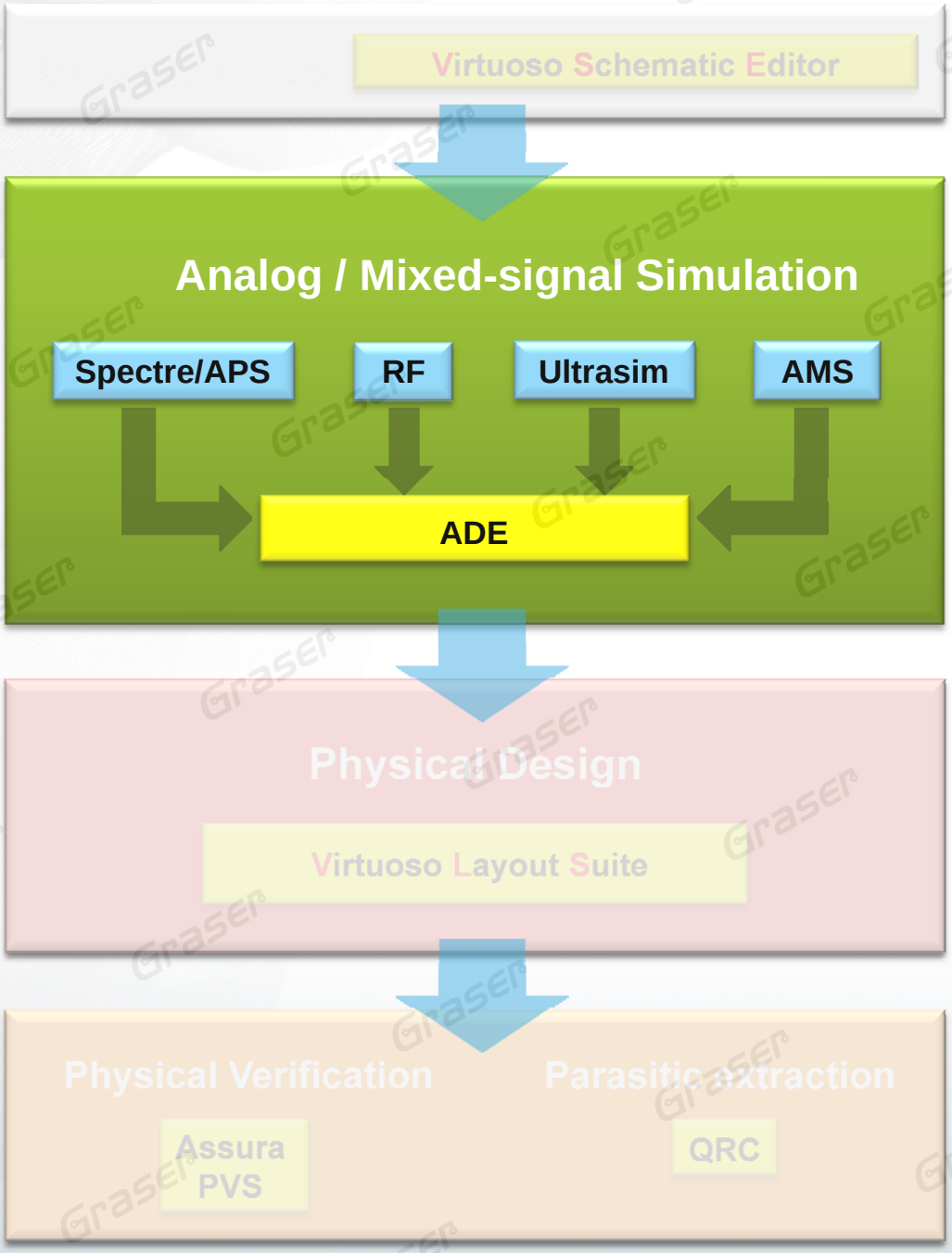
Virtuoso Schematic Editor

Quick schematics graph output

- HTML Publisher
  - Schematic design hierarchy is published that can be displayed in a web browser



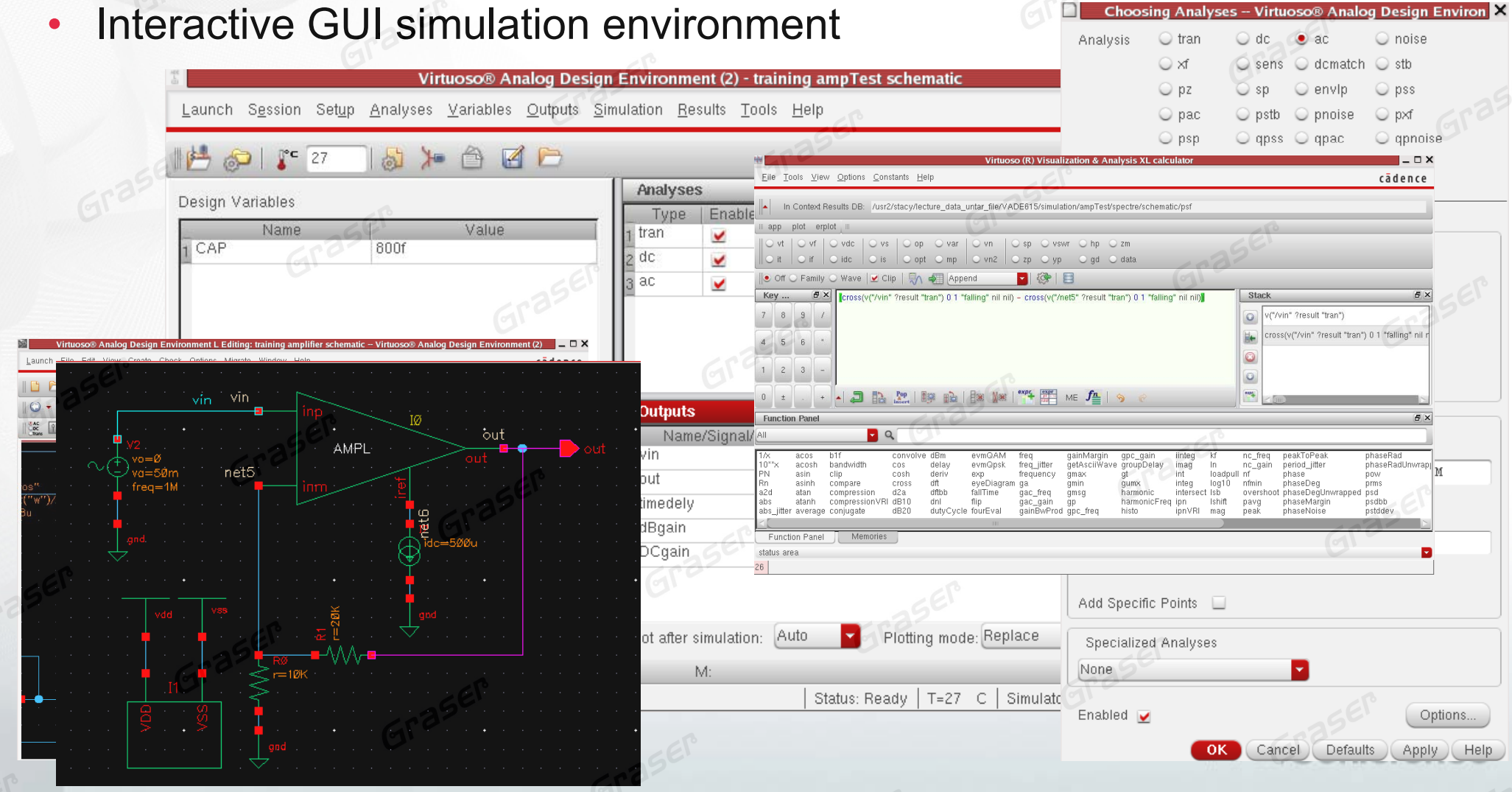
Virtuoso Custom Design and Verification



Analog Design Environment

Simulation GUI Window

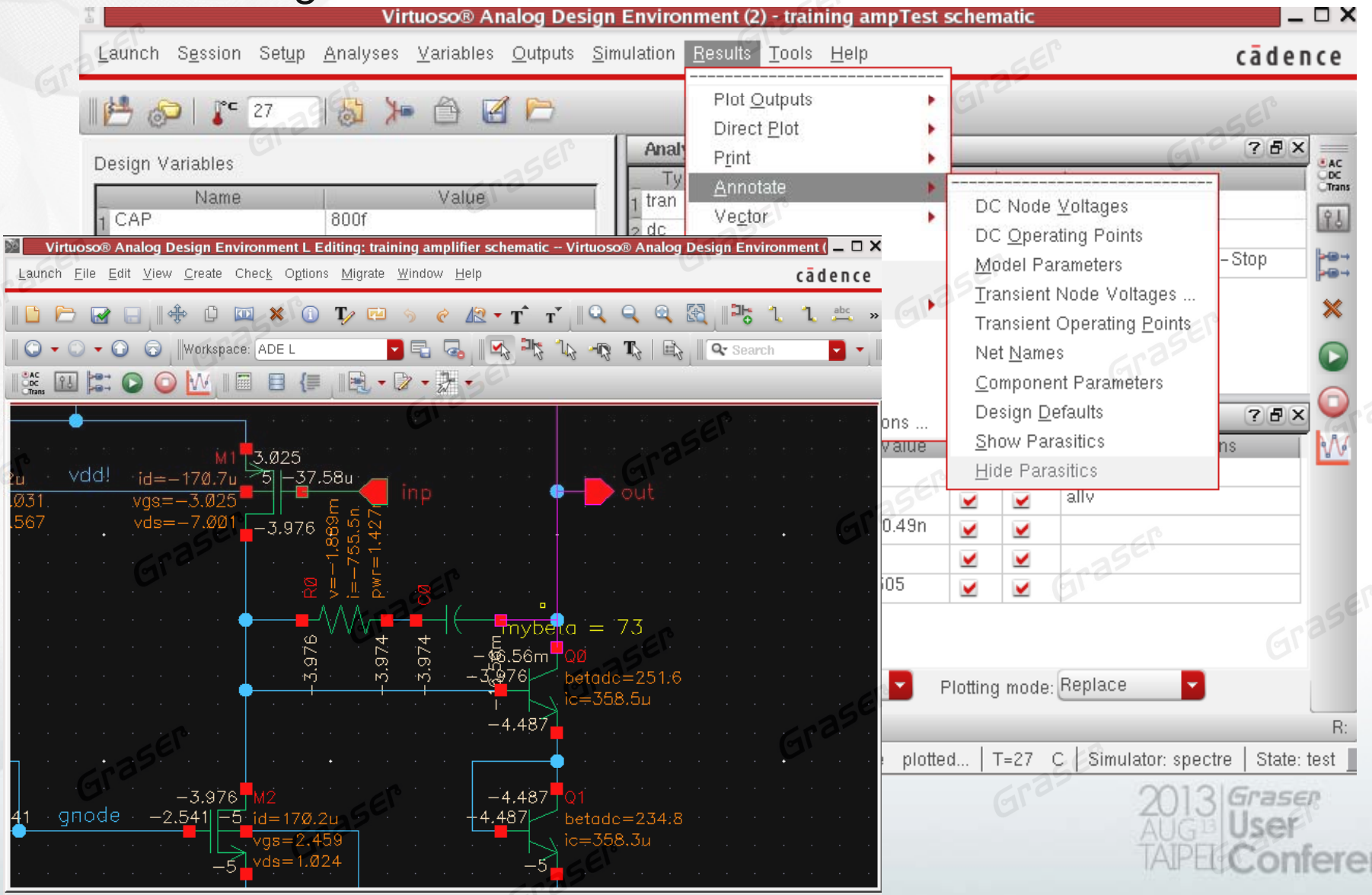
- Not necessary to understand netlist syntax
- Common syntax for different simulators
- Interactive GUI simulation environment



Analog Design Environment

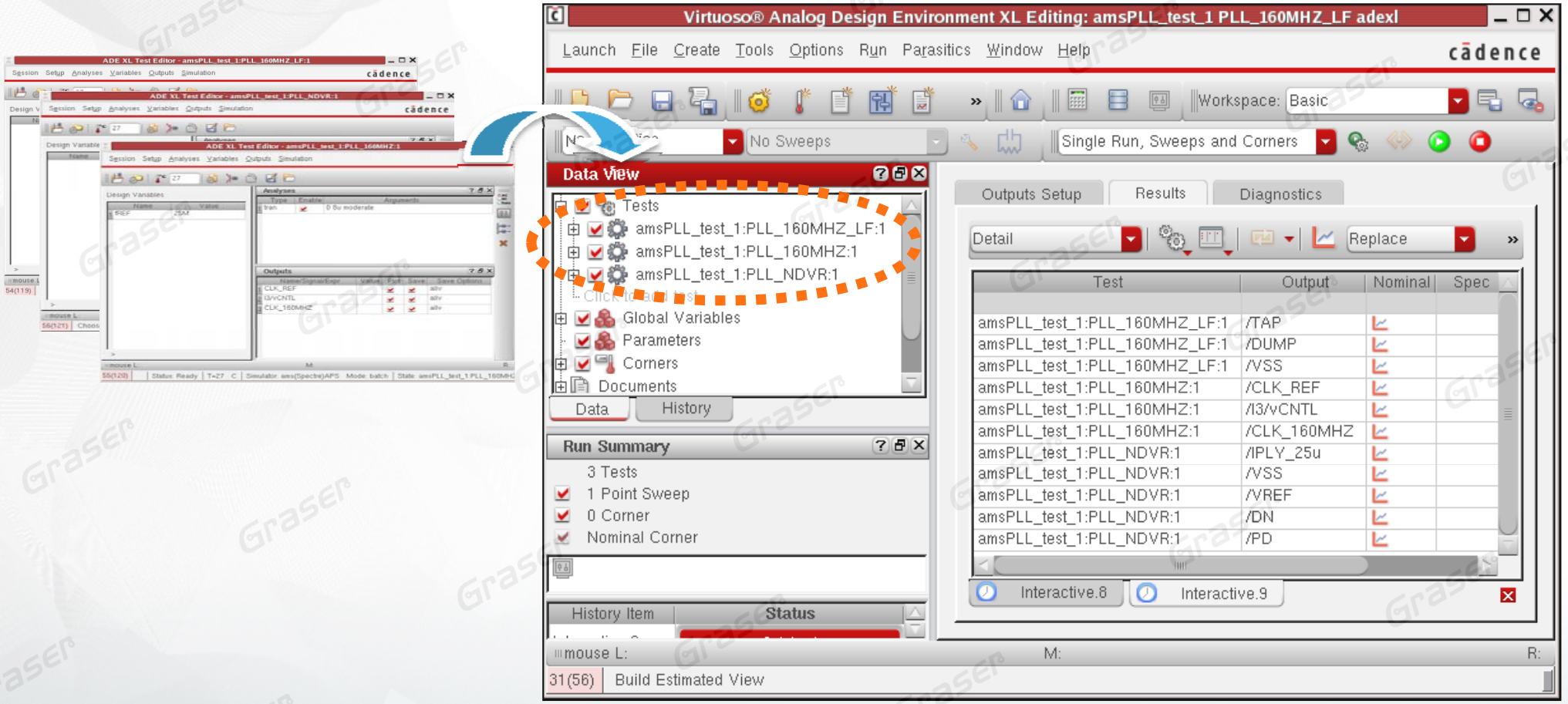
Annotate

- Back-annotating Simulation Information with Schematic



Analog Design Environment

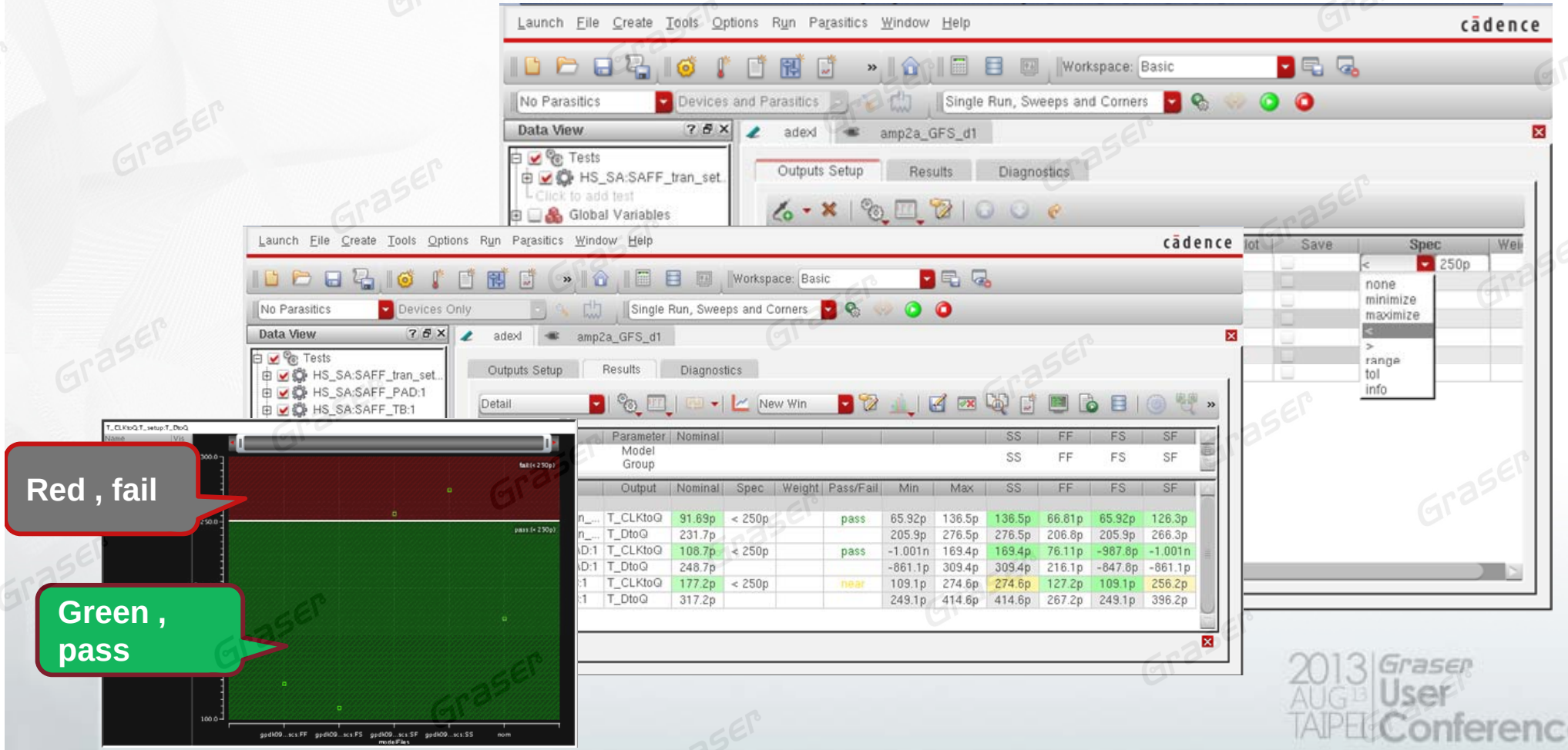
Multi-test Environment



Analog Design Environment

Specification-driven design

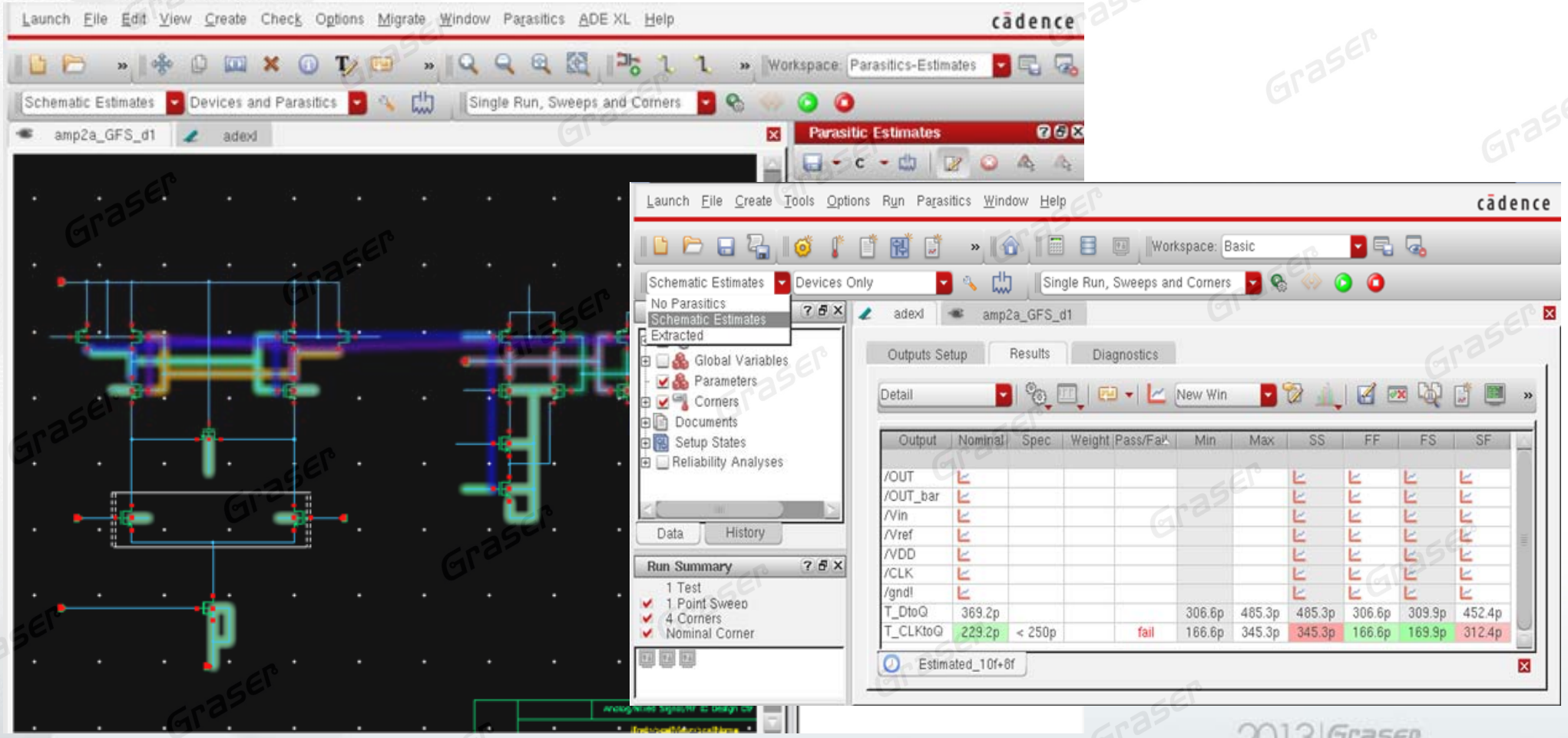
- Quick Spec setup
- color-coded feedback of all results against target specifications
- Intuitive overview color-coded graph with spec



Analog Design Environment

Parasitic Effects

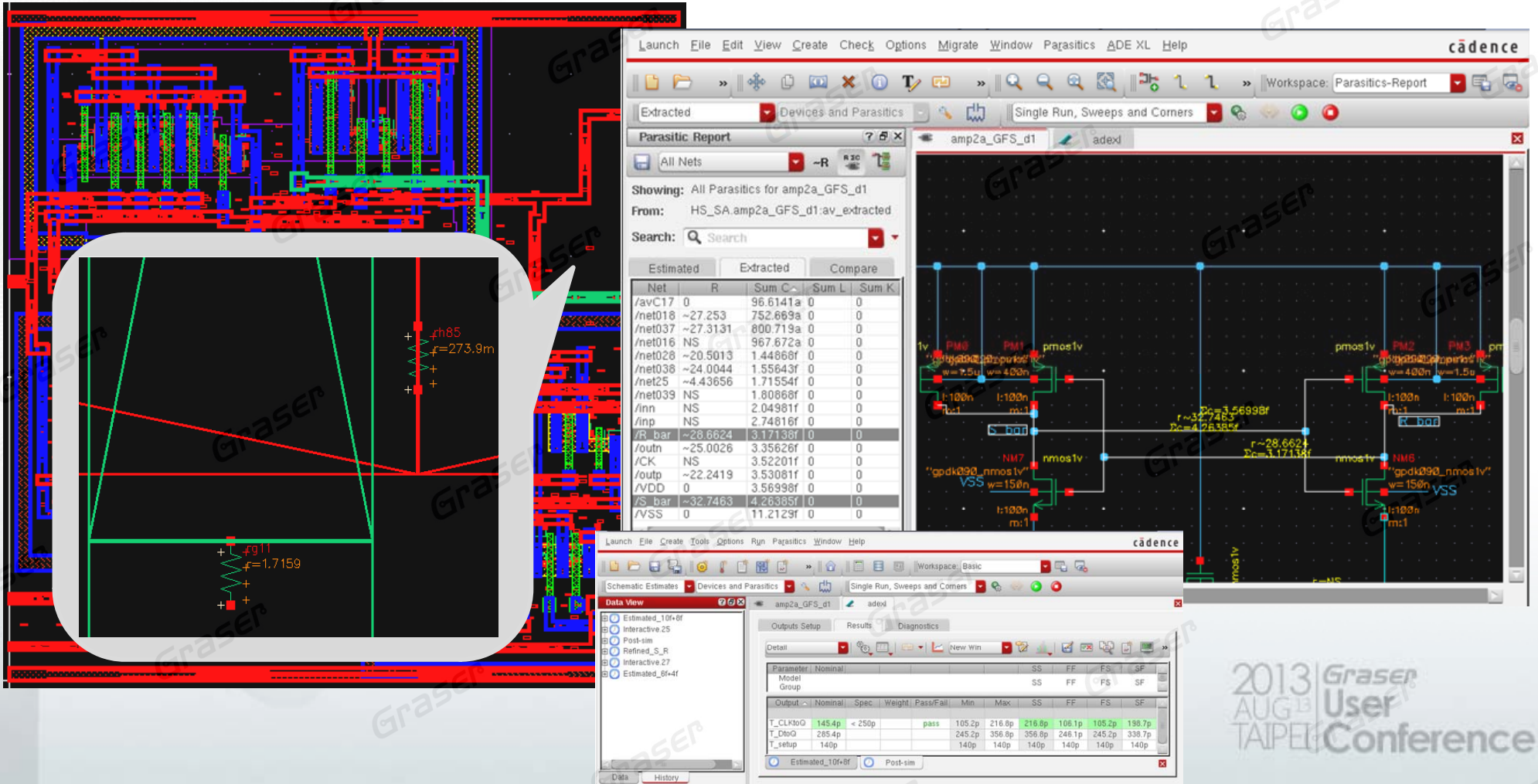
- Parasitic Estimation
  - Helps to quickly identify parasitic sensitivities prior to layout



Analog Design Environment

Parasitic Effects

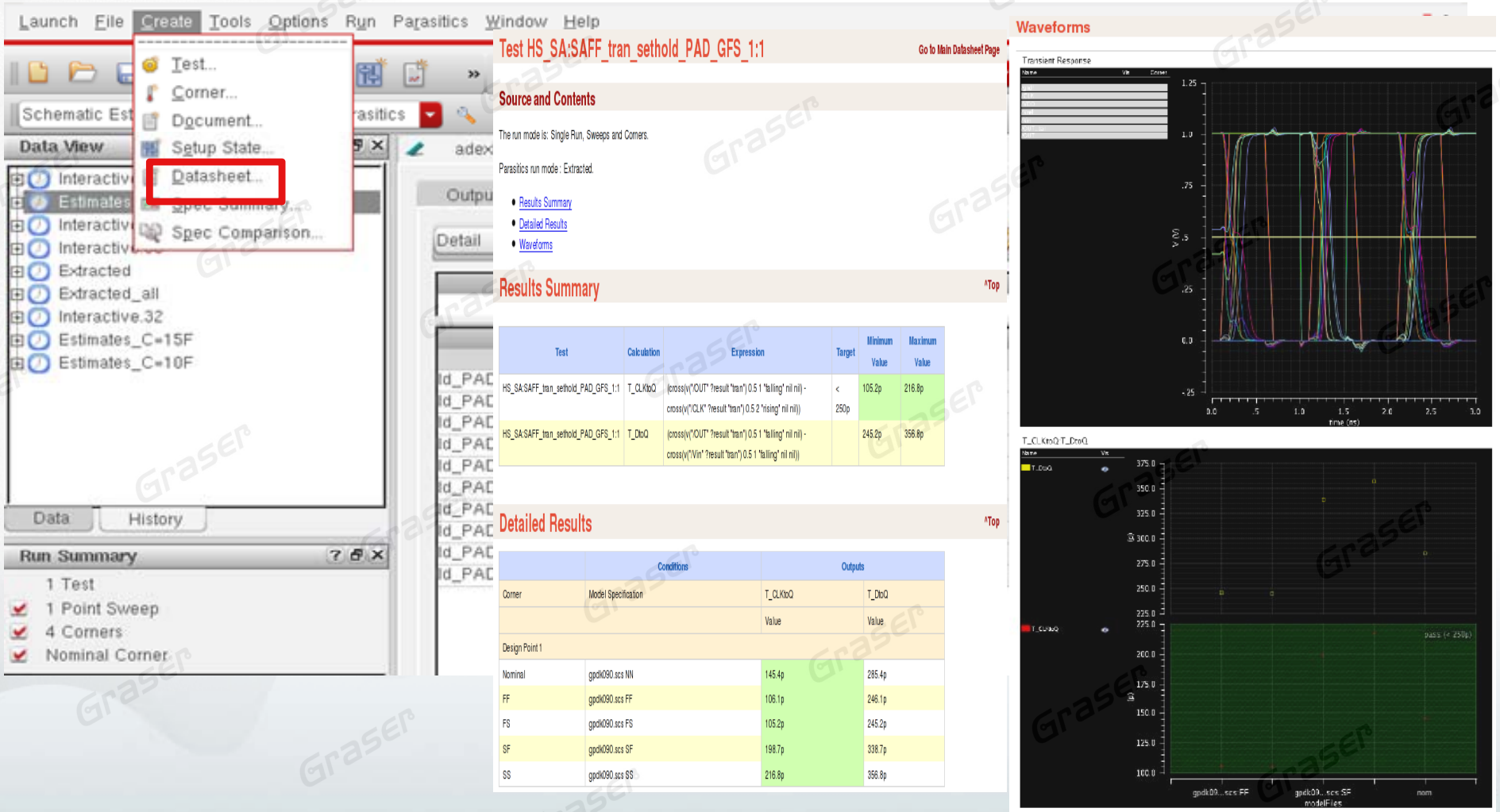
- post-extracted layouts simulation
  - Support av_extracted file
  - Show parasitic sum value on report and schematic view



Analog Design Environment

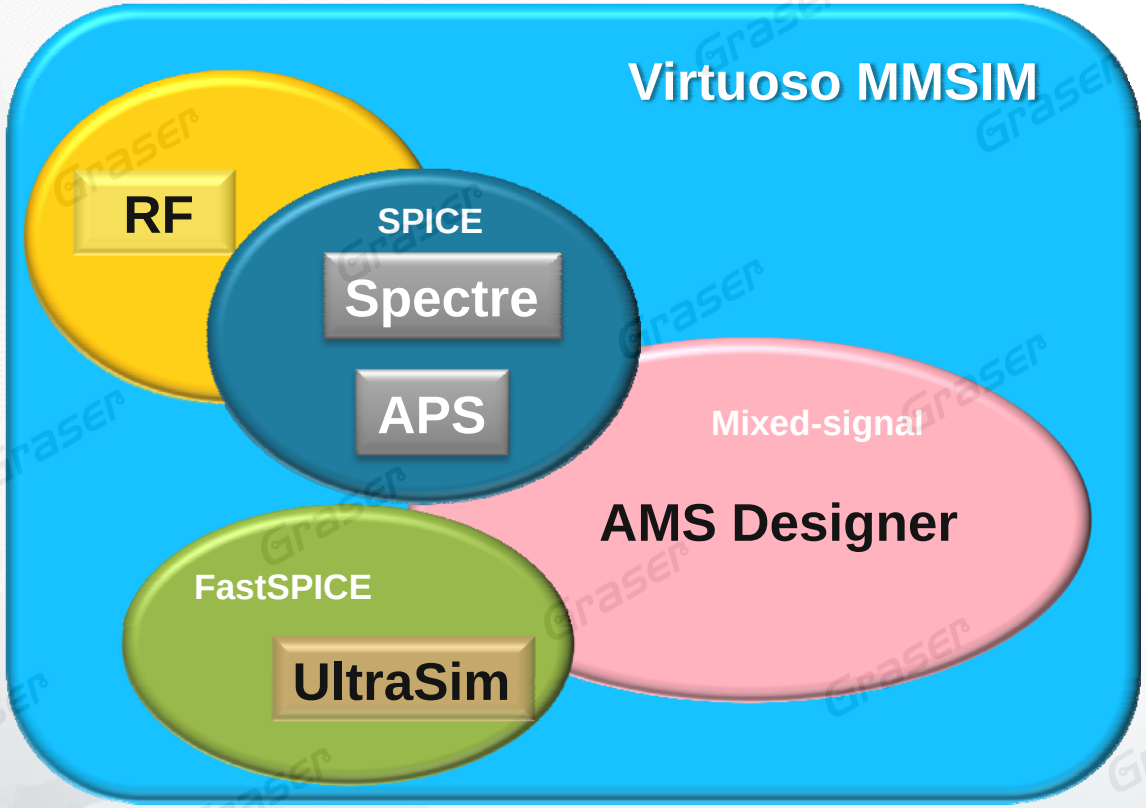
Create Datasheet

- Auto-generate the output of the simulation result and graph to the datasheet



Multi-Mode Simulation

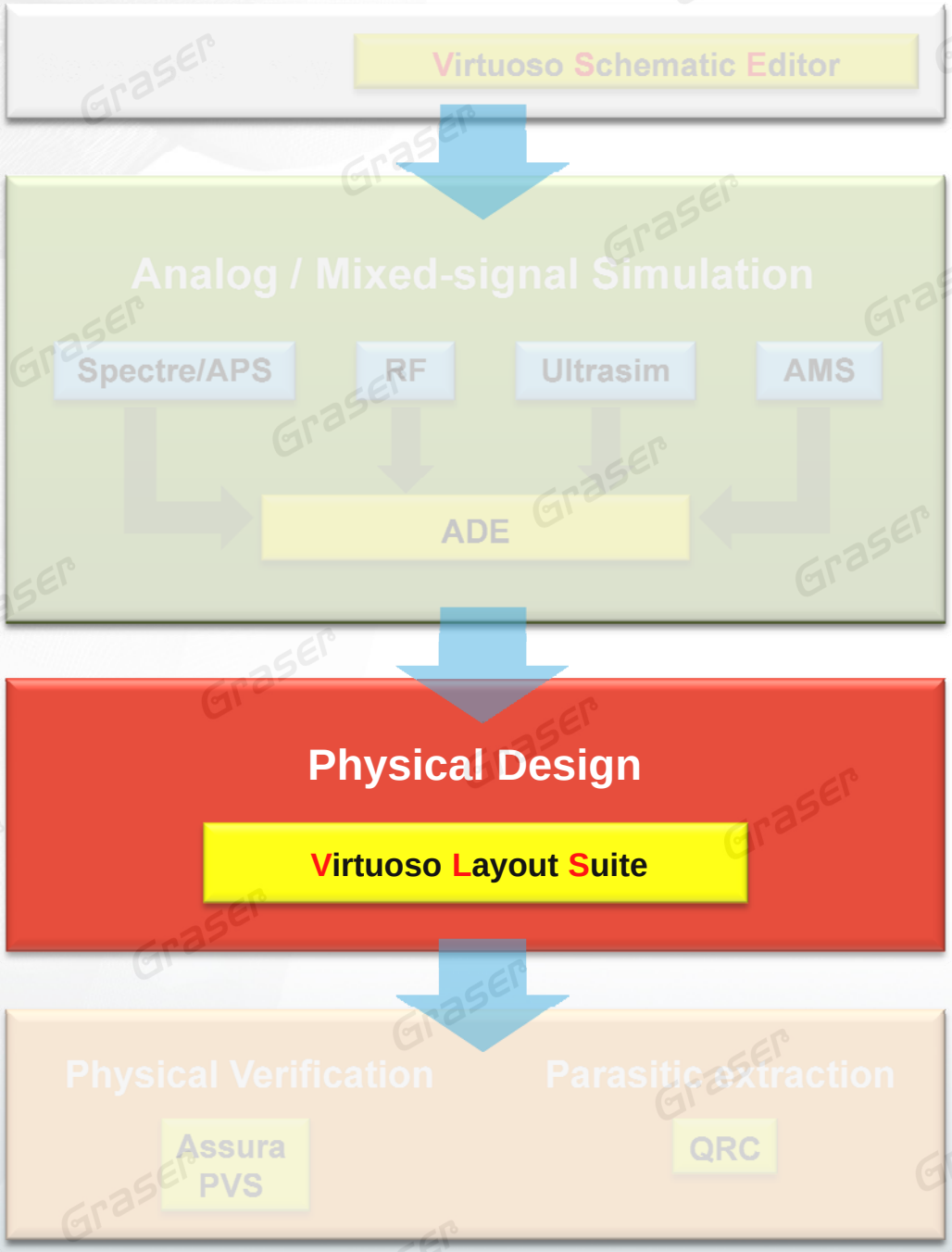
- For Custom Analog and Mixed Signal Design Verification
- MMSIM with multi-core deliver to meet your performance and accuracy



- ✓ Optimized Packaging :
  Scalability and Flexibility
- ✓ RF Analysis
- ✓ High Performance :
  AMS- APS
  Post layout
- ✓ Common model

Virtuoso Custom Implement

Virtuoso Custom Implement



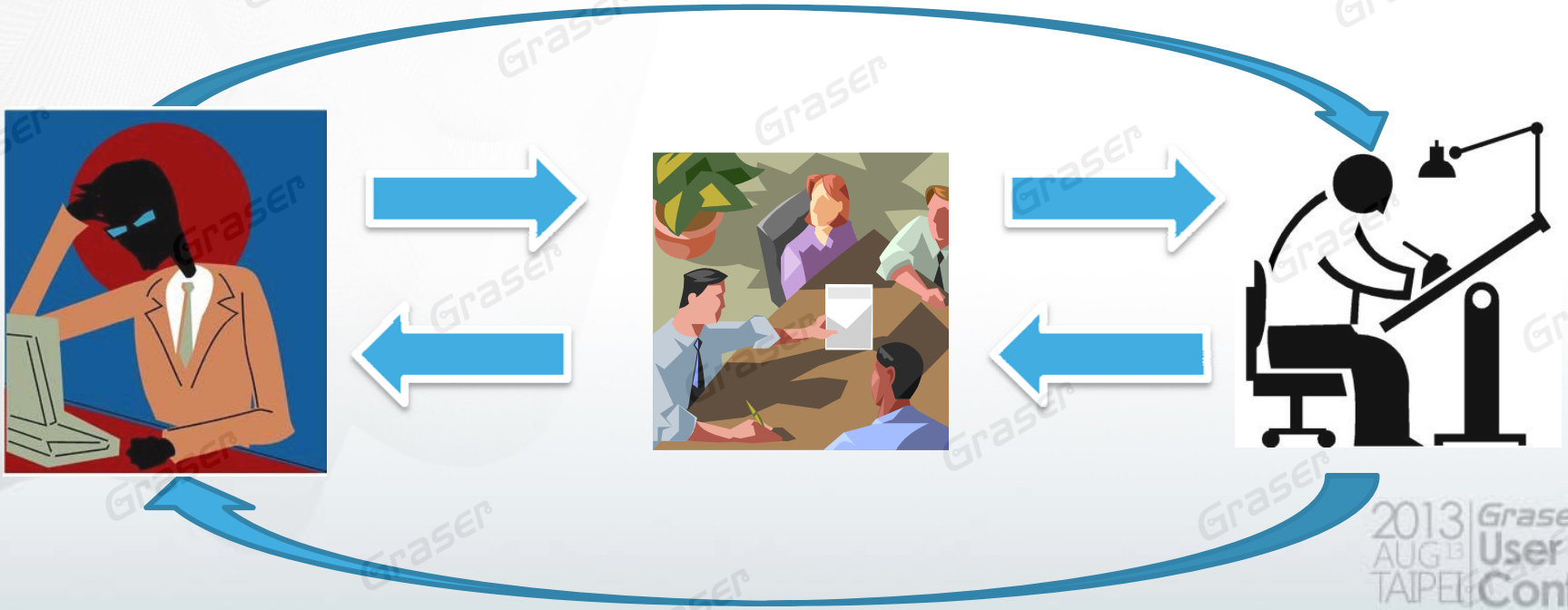
Agenda

- How to increase Team collaboration and productivity ?
- Customize back-end IC design
  - Manually
    - Accelerate Placement & Editing
  - Semi-Auto
    - Interactive Routing
  - Auto
    - Constrain & Generate From Source

How to increase Team collaboration and productivity ?

How to increase Team collaboration and productivity ?

- Capture requirements on How a design is intended to be implemented
- Minimize miscommunication problems with standard design team communications
- Simplify the procedure of Placement & Editing
- Resolve DRC & LVS errors

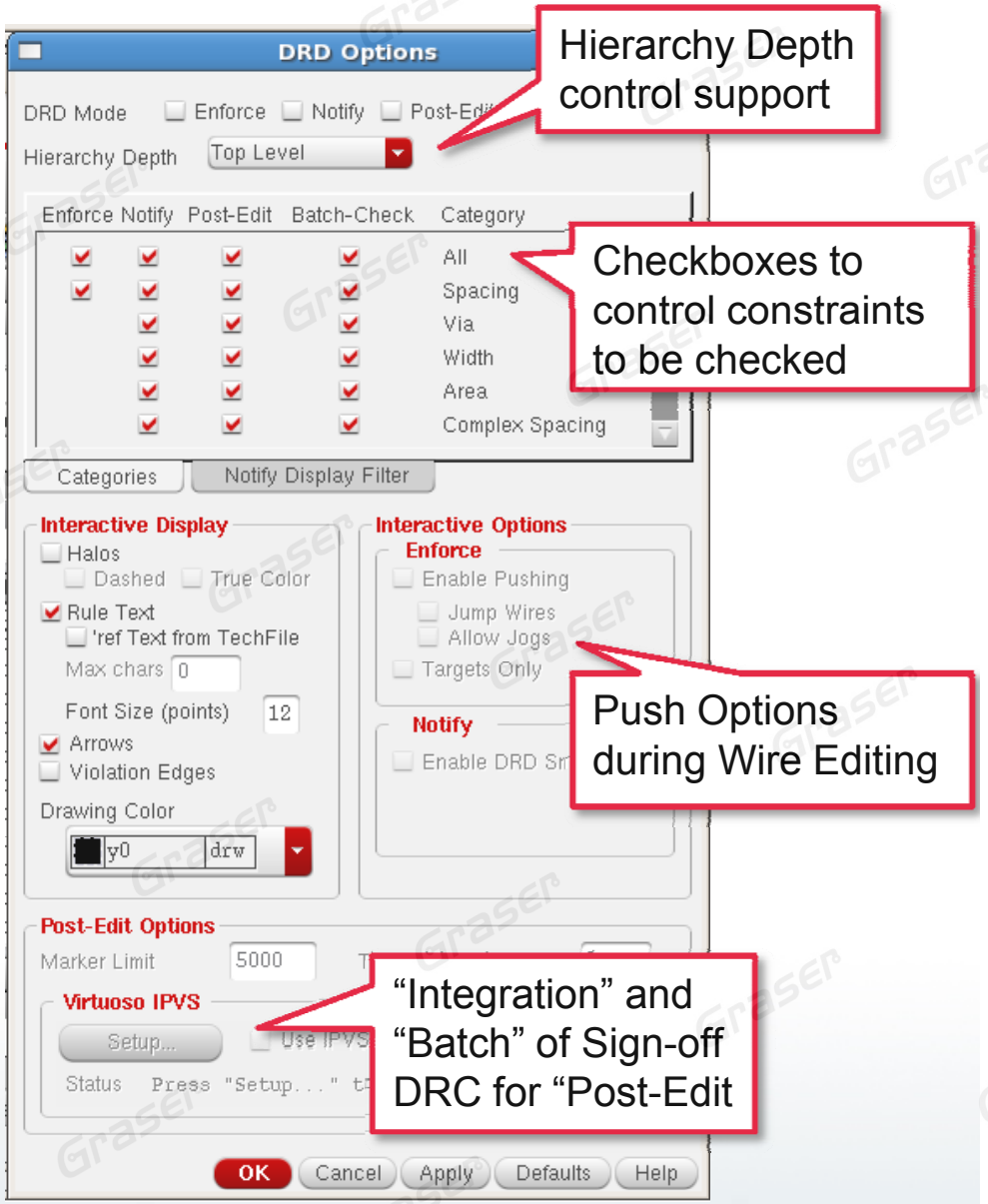


Manually
Accelerate Placement & Editing

Design Rule Driven

Interactive Design Rule Checking

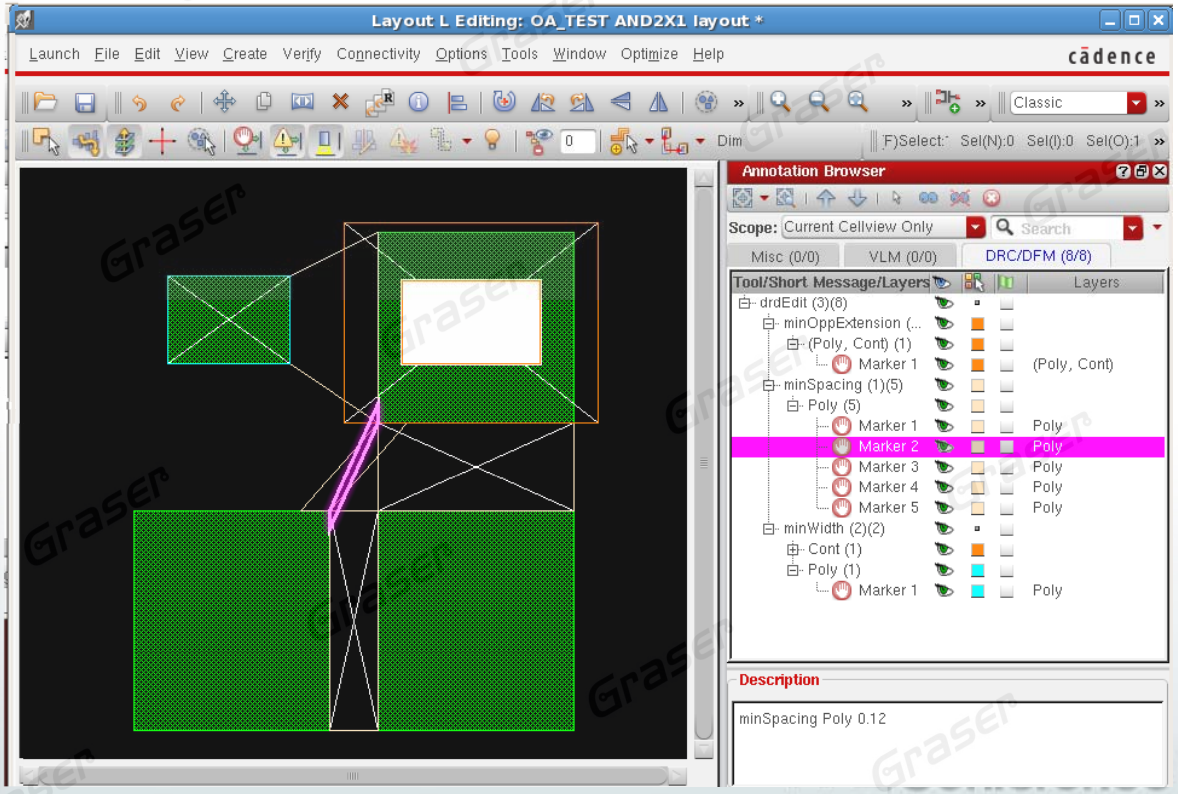
- Real-time DRC Checking
- Automatically enforces design rules
- Eliminate physical verification iterations
- Reduce the number of DRC violations during layout editing



Design Rule Driven

Debugging DRC Violations

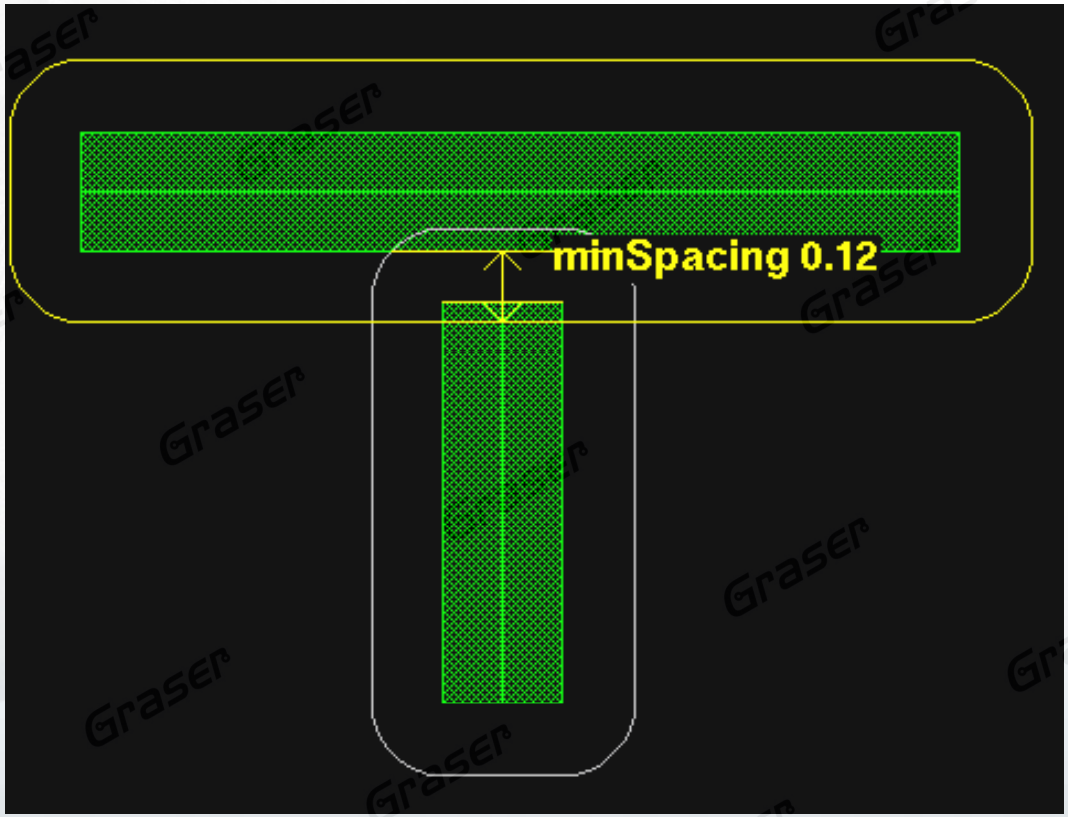
- The post-edit markers can be viewed, analyzed, and filtered in the DRC/DFM tab of Annotation Browser.
- The markers are the persistent objects, which can be saved.



Interactive Wire Editing

Wire Routing

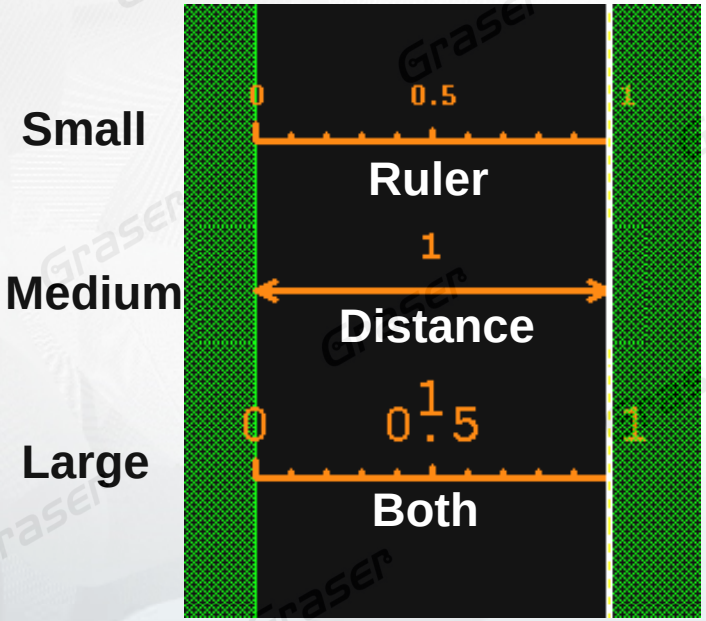
- Smart snapping
- Auto Tap wire
- Easy to change Layers

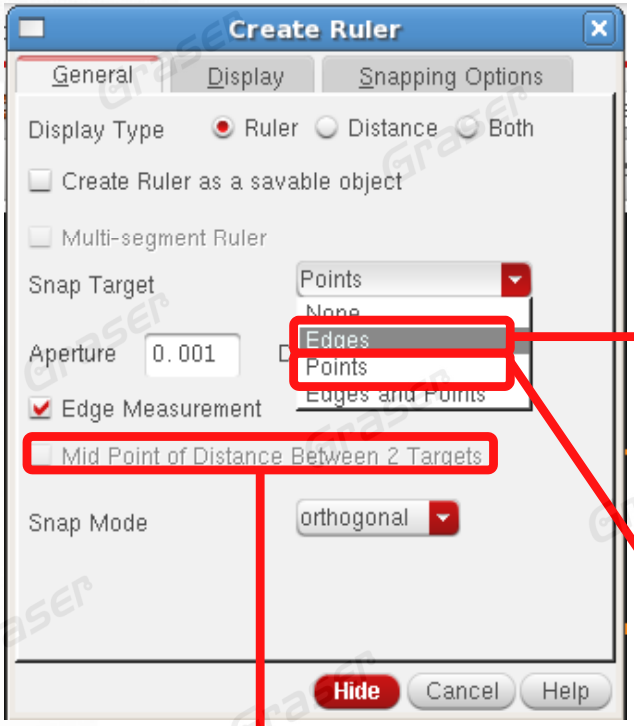


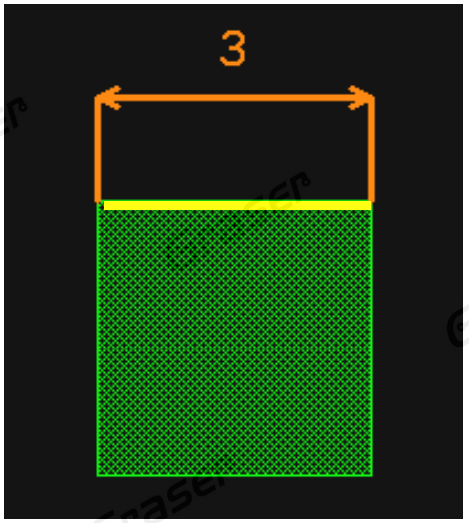
Accelerate Manual-Editing

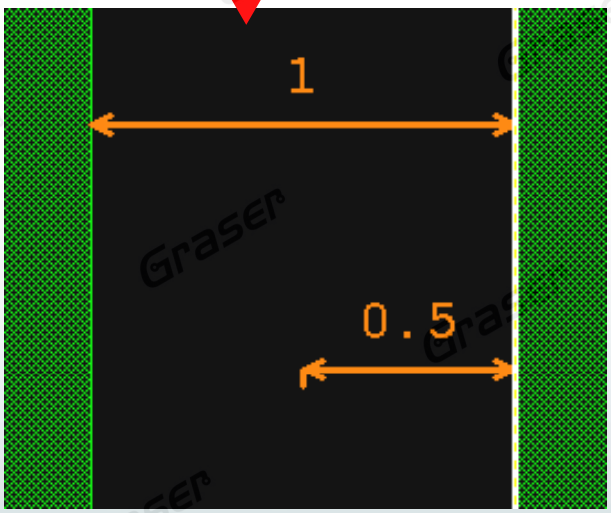
Smart Ruler

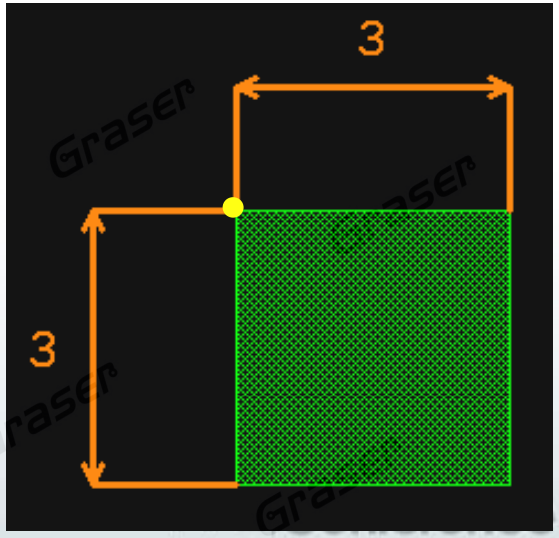
- Smart Snapping
- Multi-segments
- Customize general Ruler measurement and display type







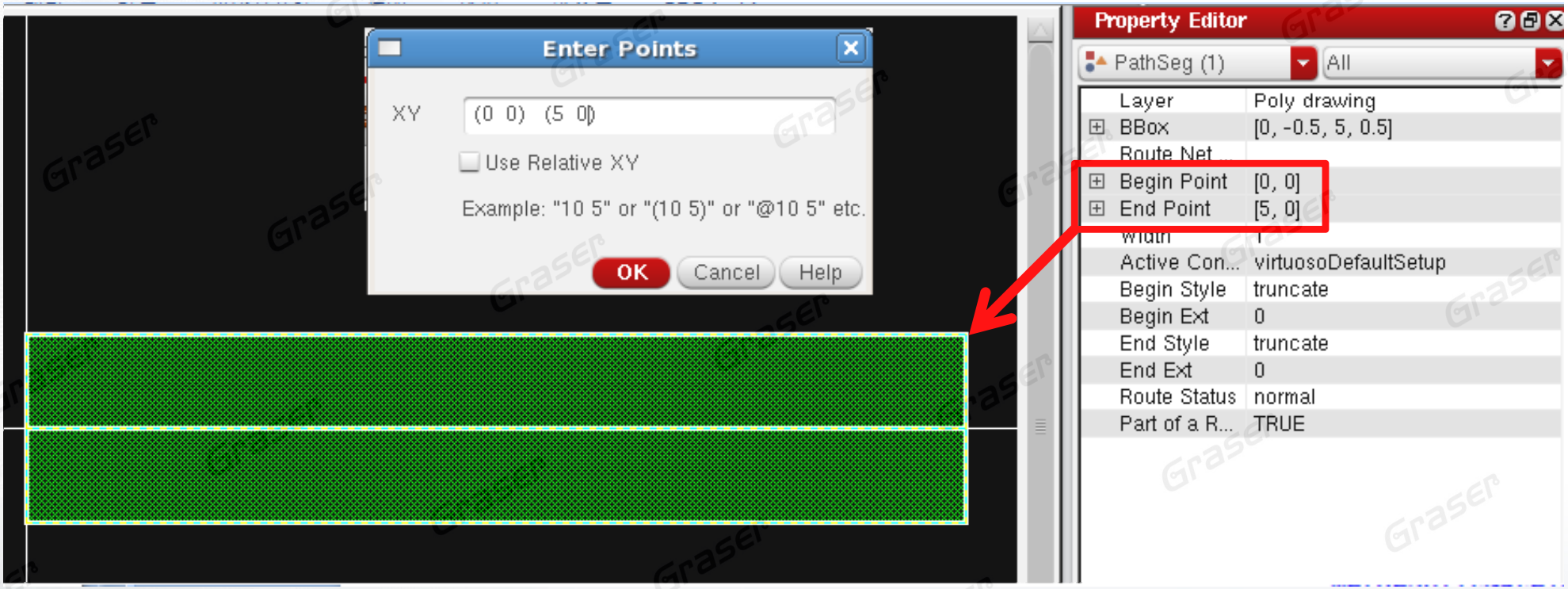




Accelerate Manual-Editing

Enter Points

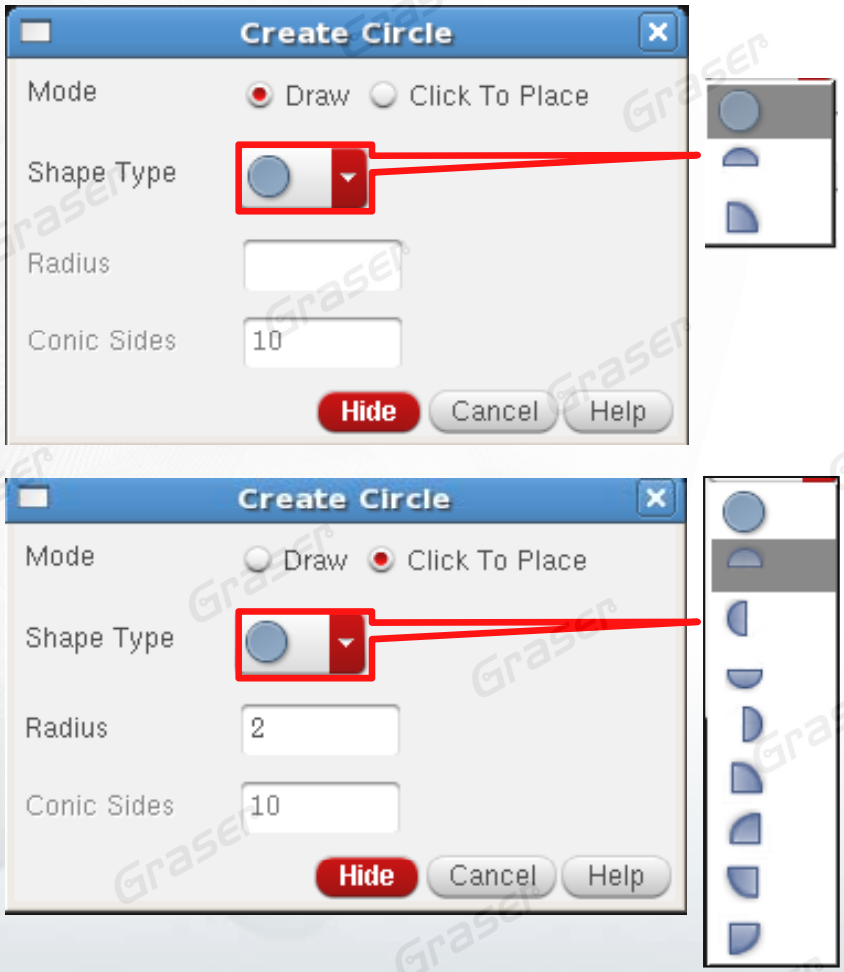
- Easy to specify points for any of the enter function based commands like Create, Move, Stretch, Copy command…

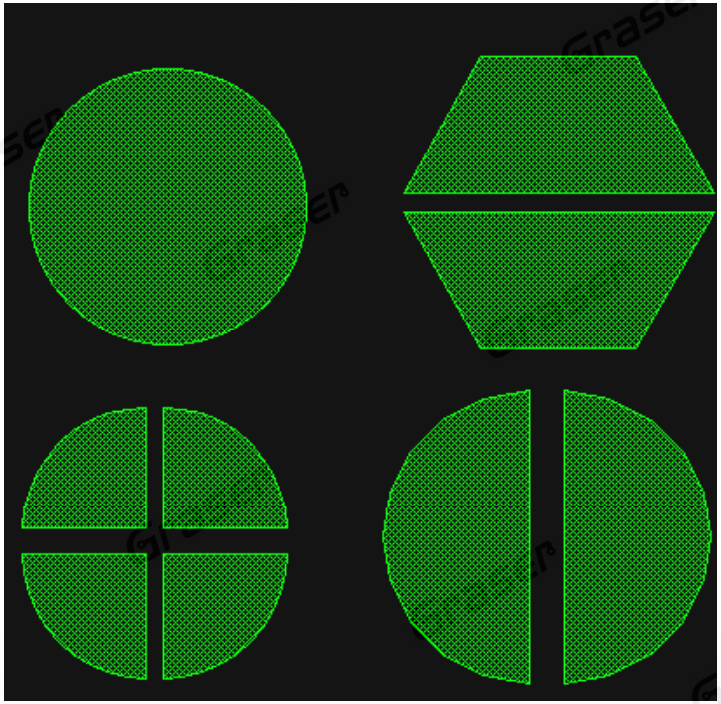


Accelerate Manual-Editing

Create Circle

- Support the Mode of “Draw” and “Click To Place”
- Multiple Shape Type

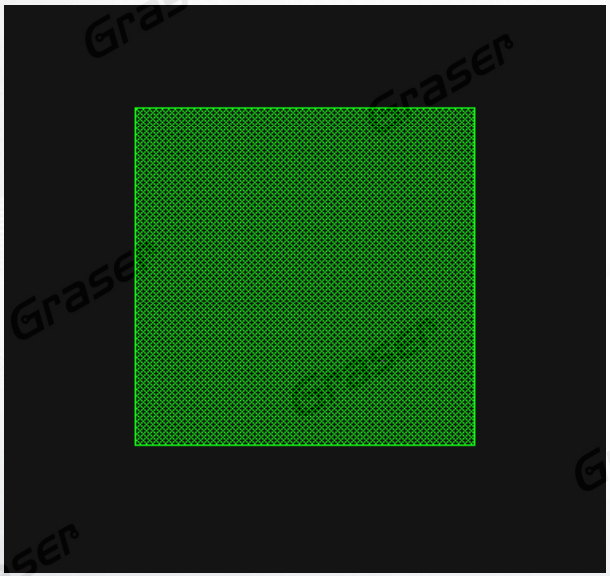


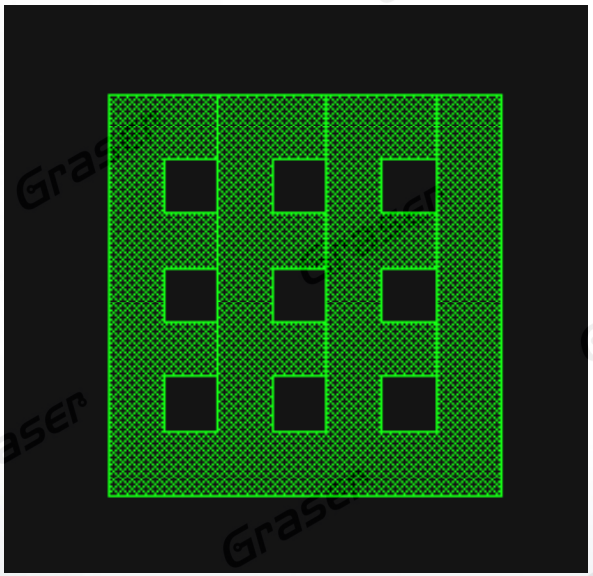


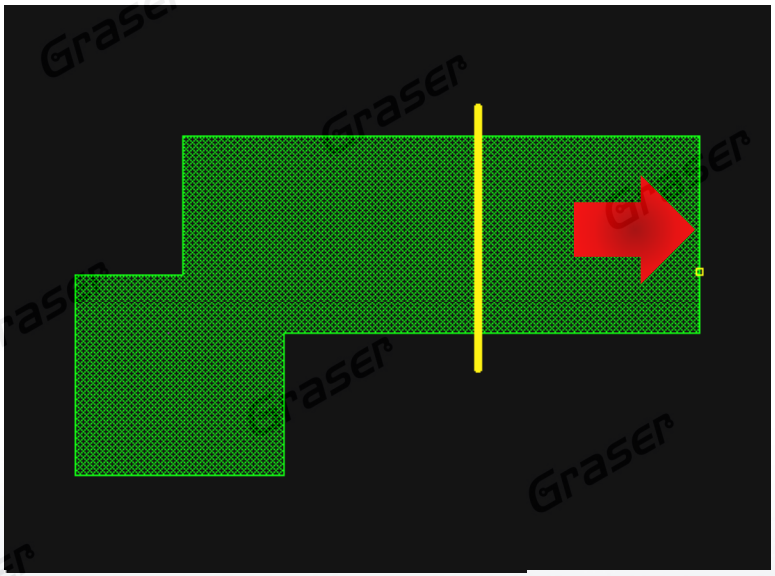
Accelerate Manual-Editing

Create Rectangle

- Draw mode has the Smart Snapping
- Smart to create abutting rectangles to an existing shape
- Snapping can be restricted to Current Active Layer in Layer Palette
- Easy to customize the Dimension, spacing and Edge of Slot



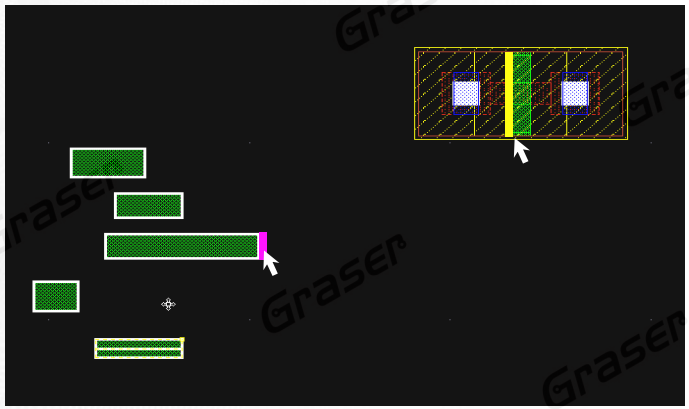


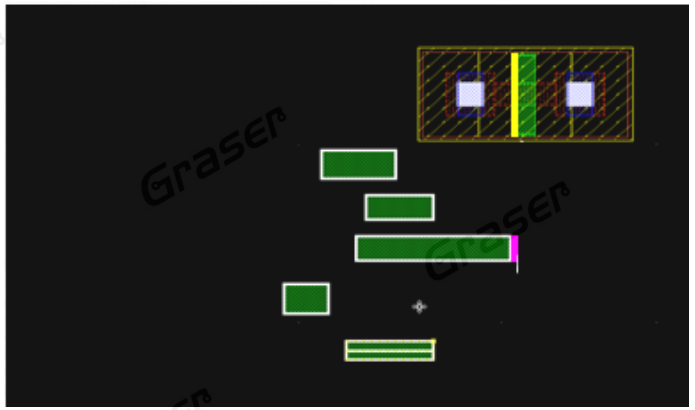


Accelerate Manual-Editing

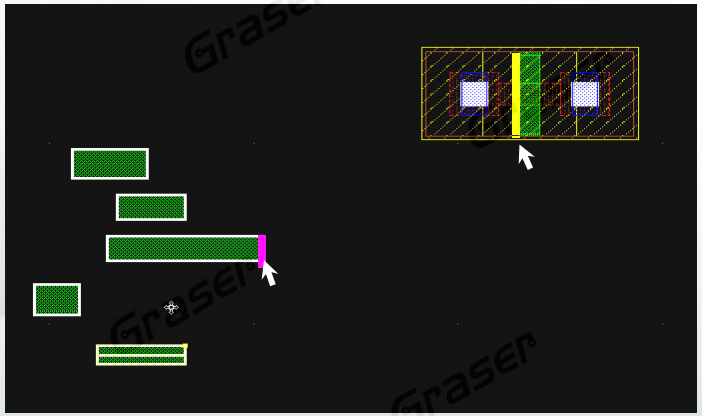
Quick Align

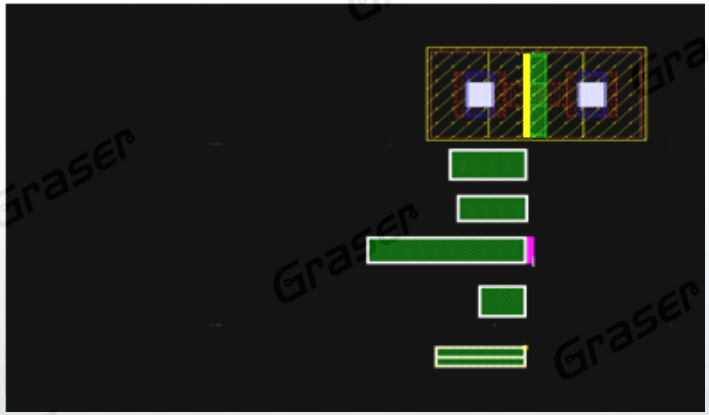
- Quick Align allows users to align objects or instances
  - Full align is done in 1 click and 1 double click





  - Relative align is done in 2 clicks

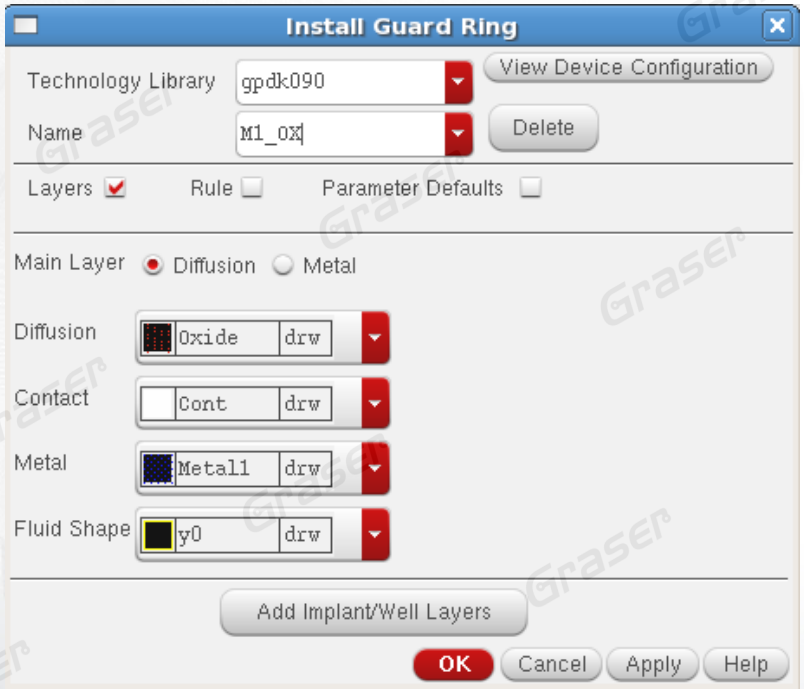


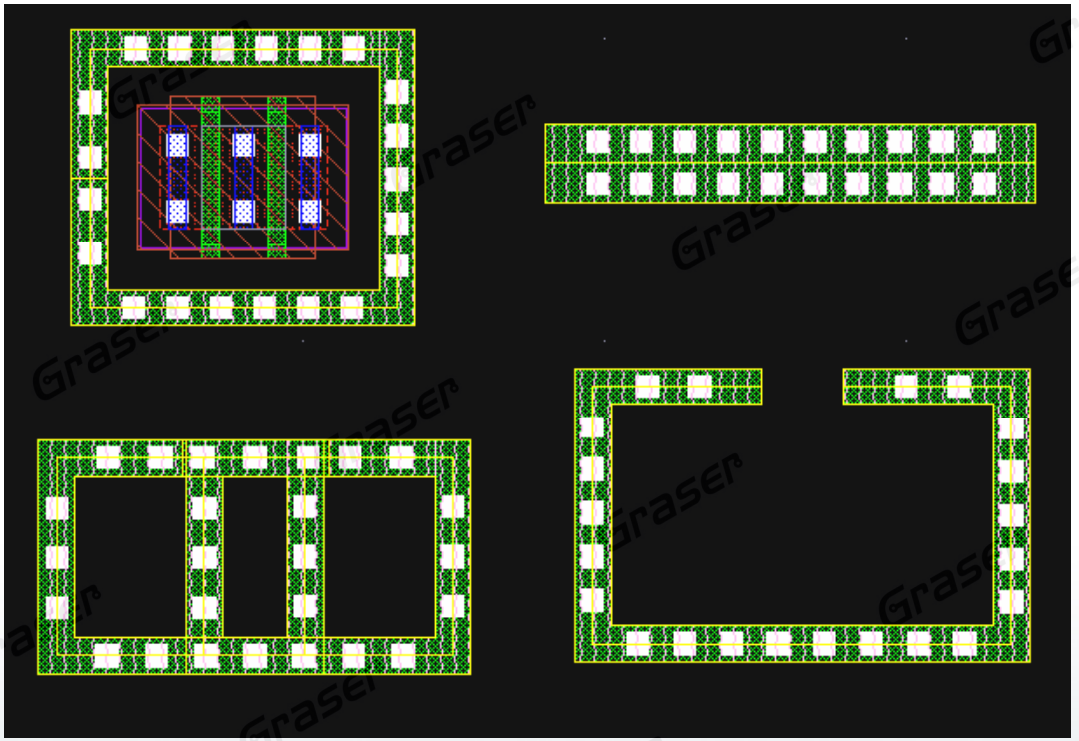


Accelerate Manual-Editing

Create Guard Ring

- Easy to customize the Guard Ring
- It can be created by four different ways: by drawing a path, rectangle, or polygon, or by using the wrap mode

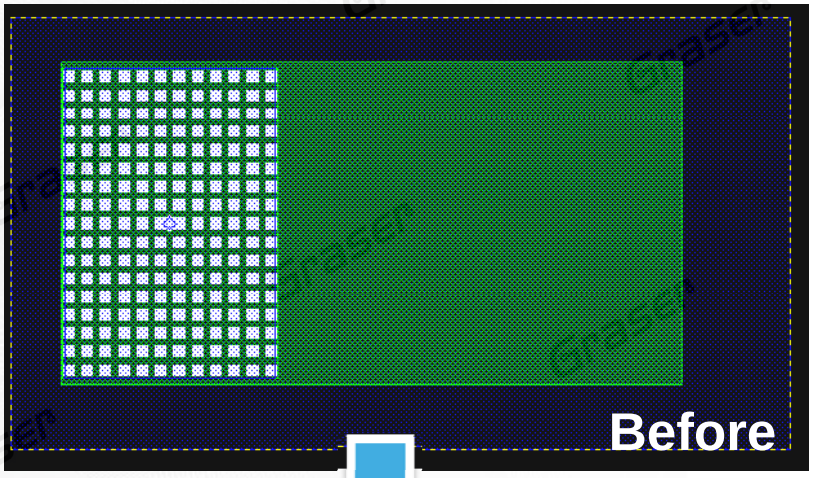


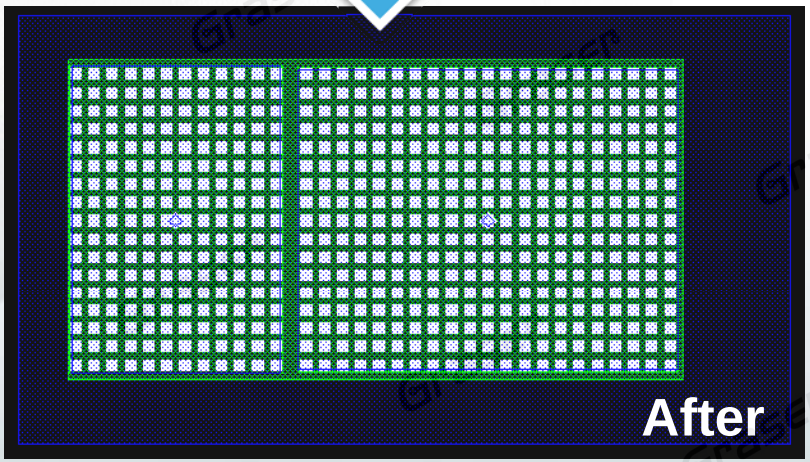


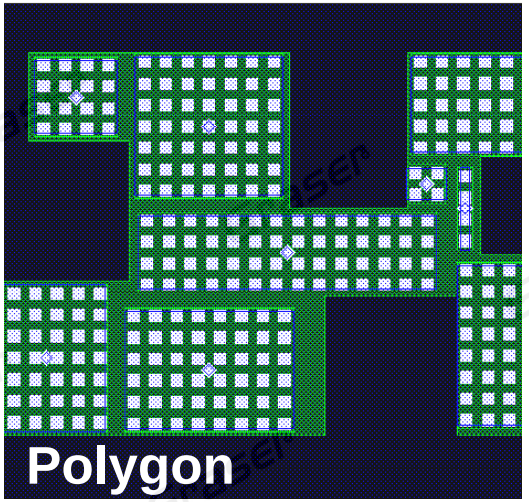
Accelerate Manual-Editing

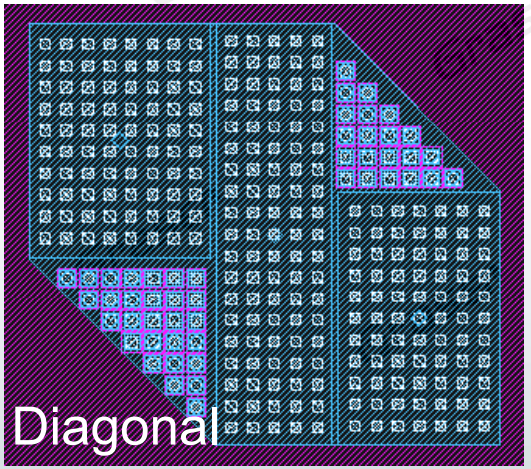
Create Via

- Supports polygonal shapes
- Autovia can fill a shape which already contains vias
- Supports 45 degree/diagonal shapes with below variables







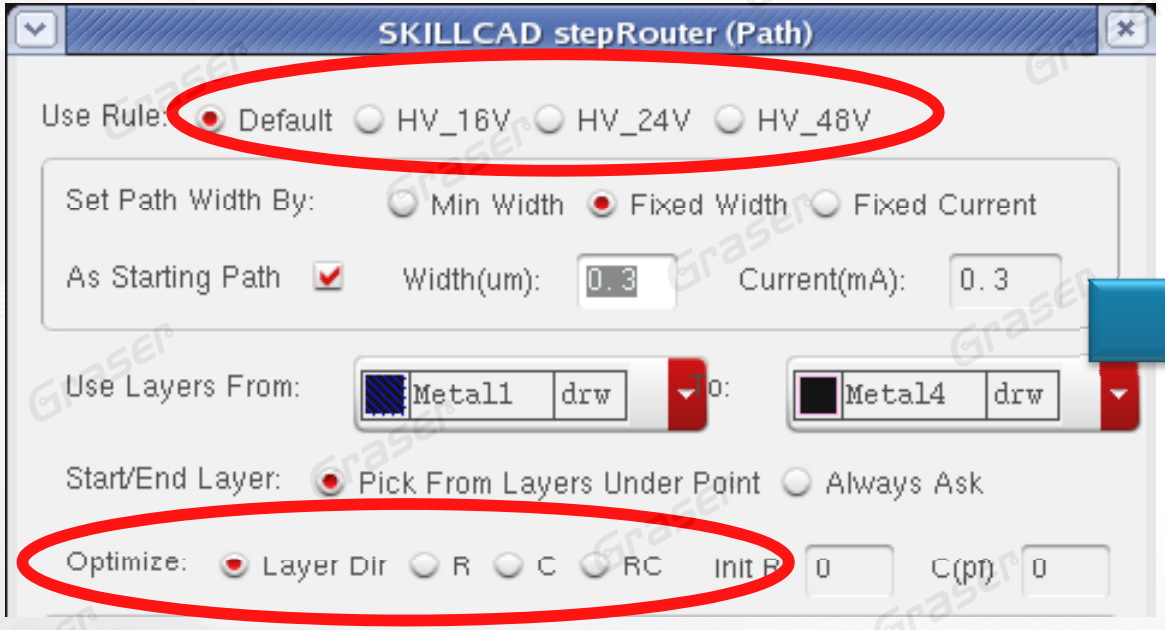


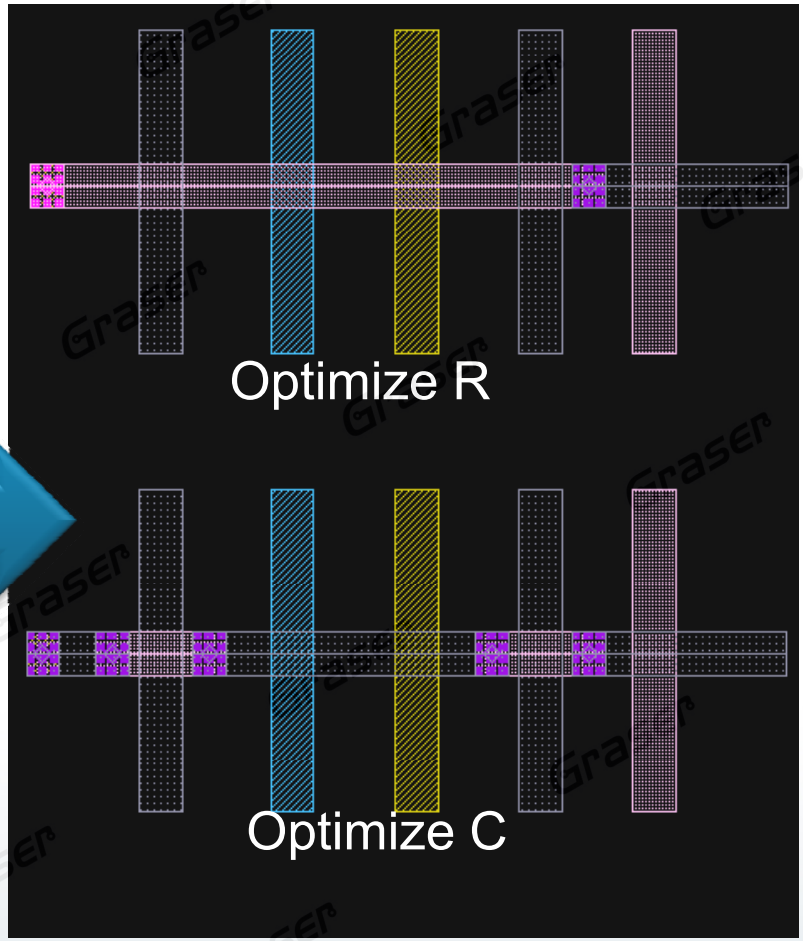
Semi-Auto Interactive Routing

Interactive Wire Editing

Step Router

- Easy to choose rules
- Optimize auto-connections according to
  - Layer direction
  - Optimized RC effect

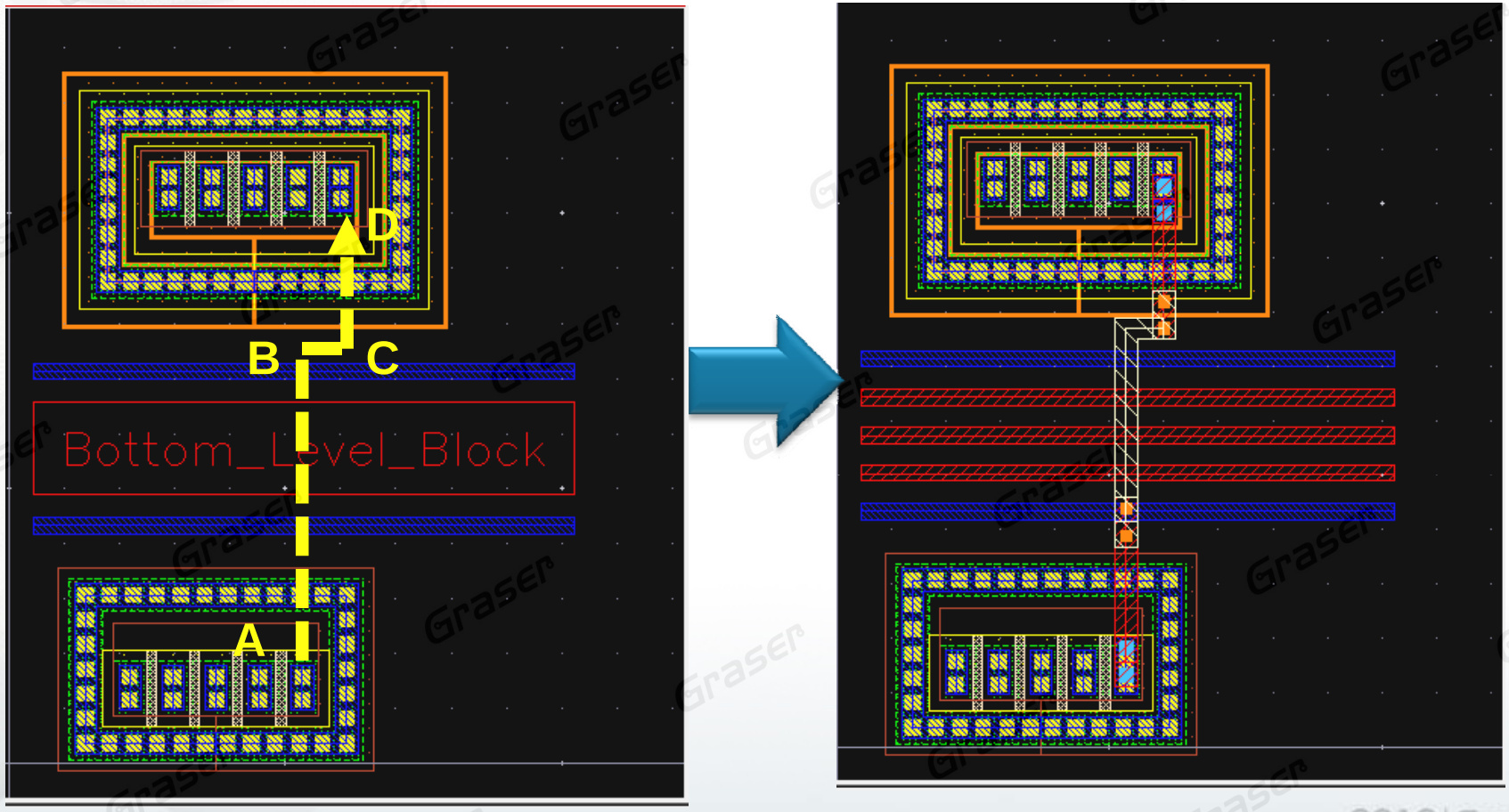




Interactive Wire Editing

Step Router

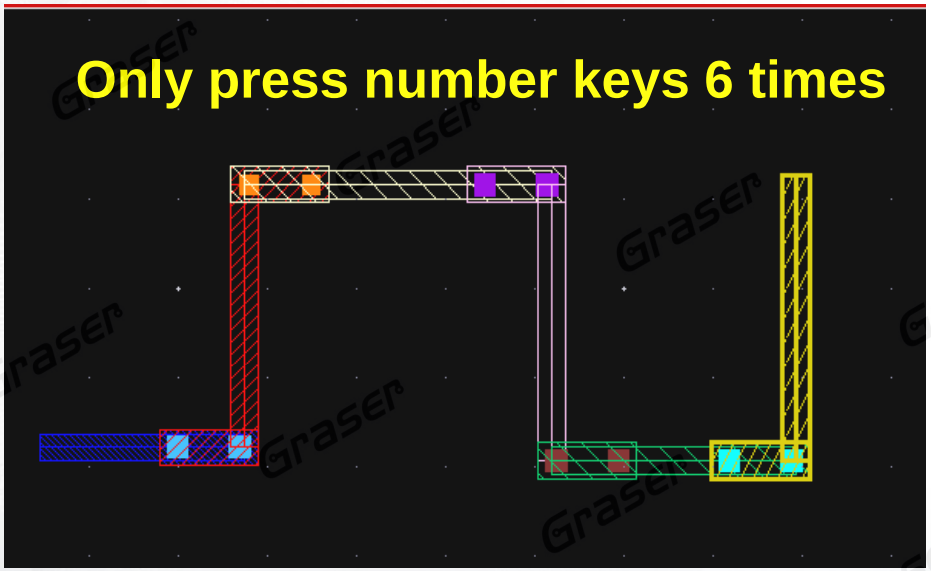
- Auto Tap the Width
- Auto change layer , snap pin & add vias

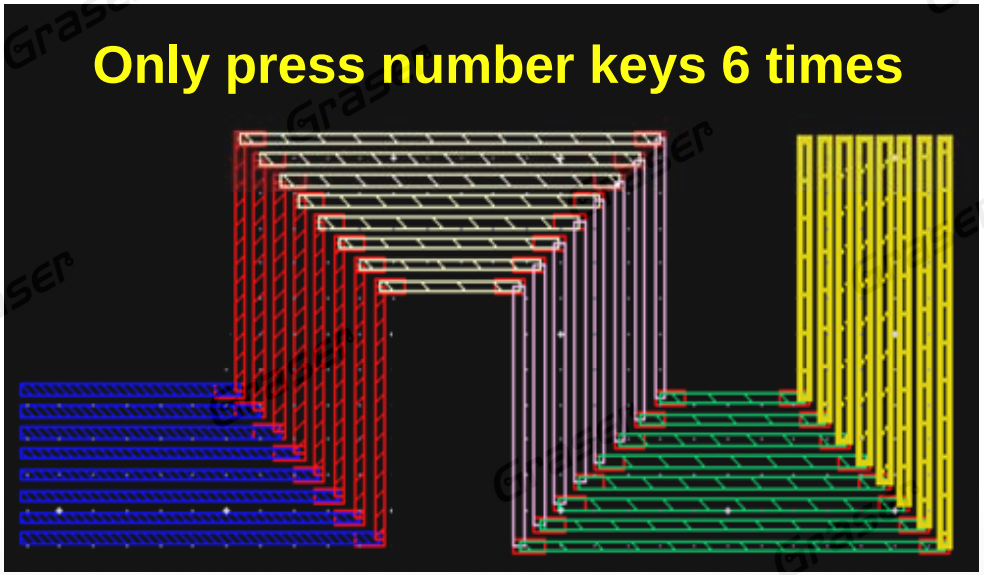


Interactive Wire Editing

Free Jumper

- Use number keys to change the layer what you want to route
- Add double via automatically
- Flexible via corner align style

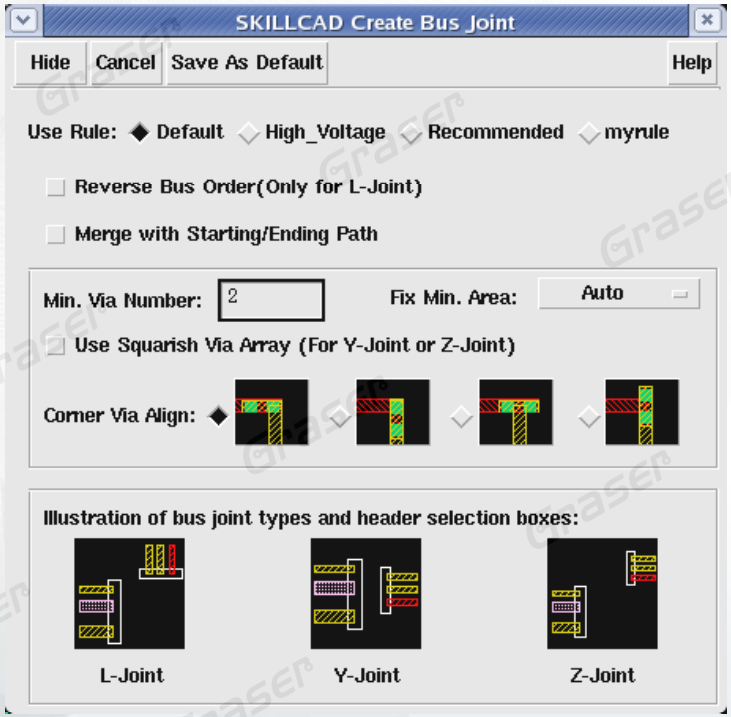


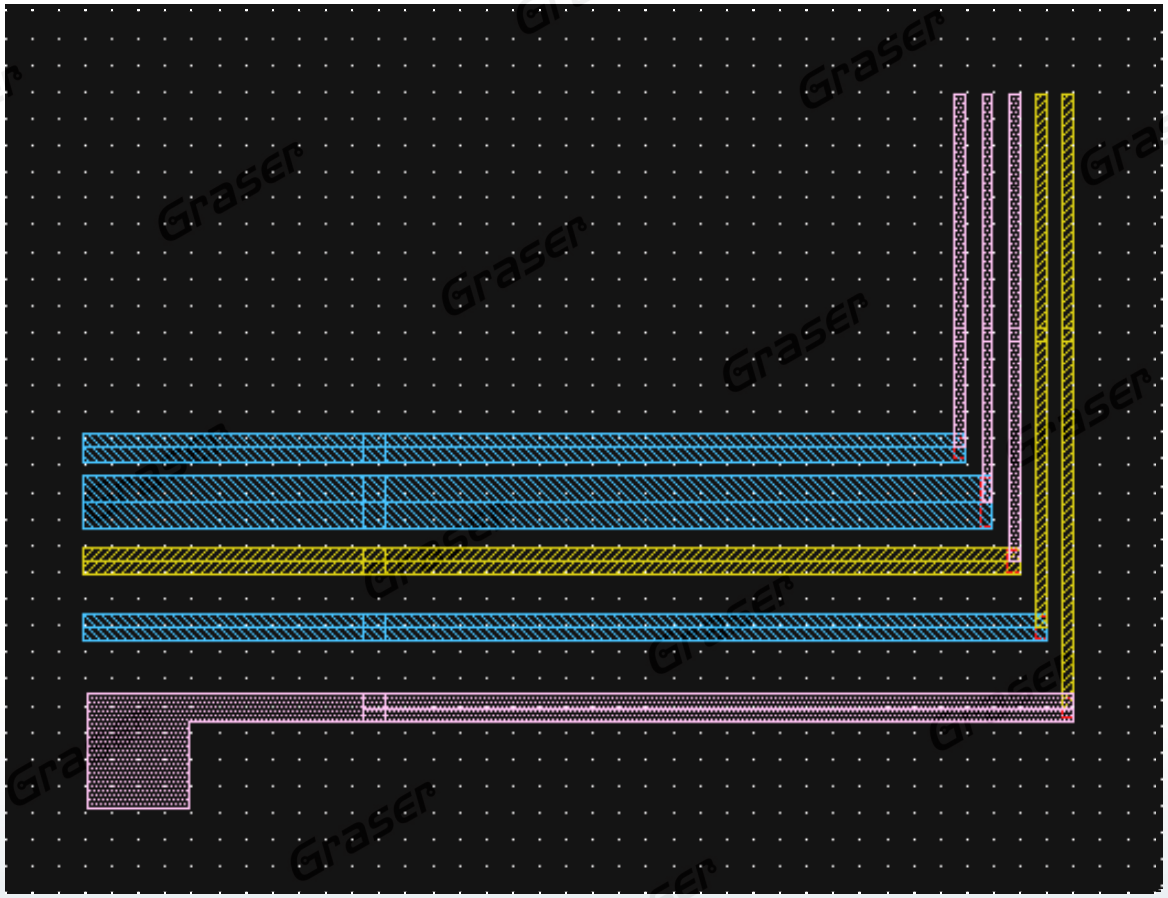


Interactive Wire Editing

Bus Joint

- Connected wire by user selection
- Auto change routing layers and add vias
- Easy to reverse order

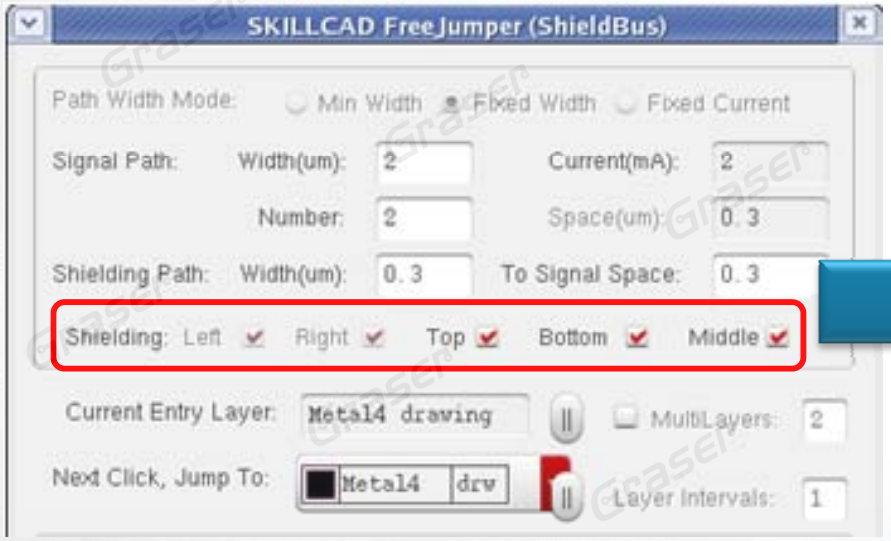


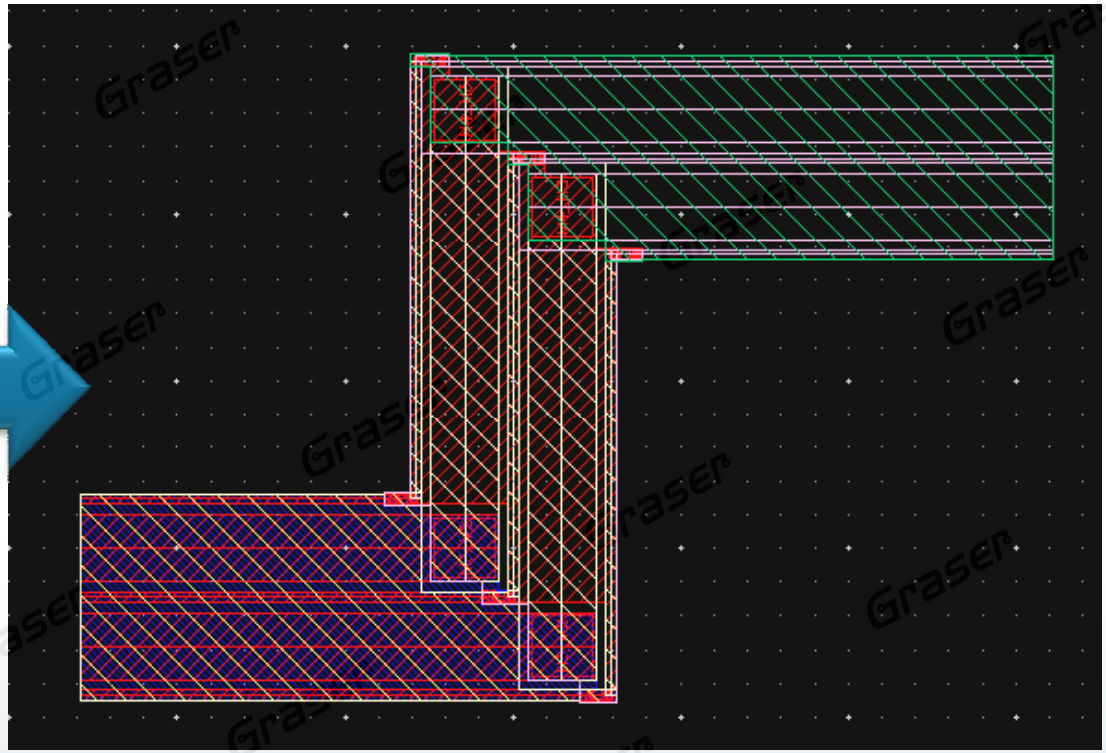


Interactive Wire Editing

Shield Bus

- User-defined width / spacing of shielding path
- Number key to change connecting layers
- Auto-Via





Auto
Constrain & Generate From Source

Constraint Driven & Generate From Source

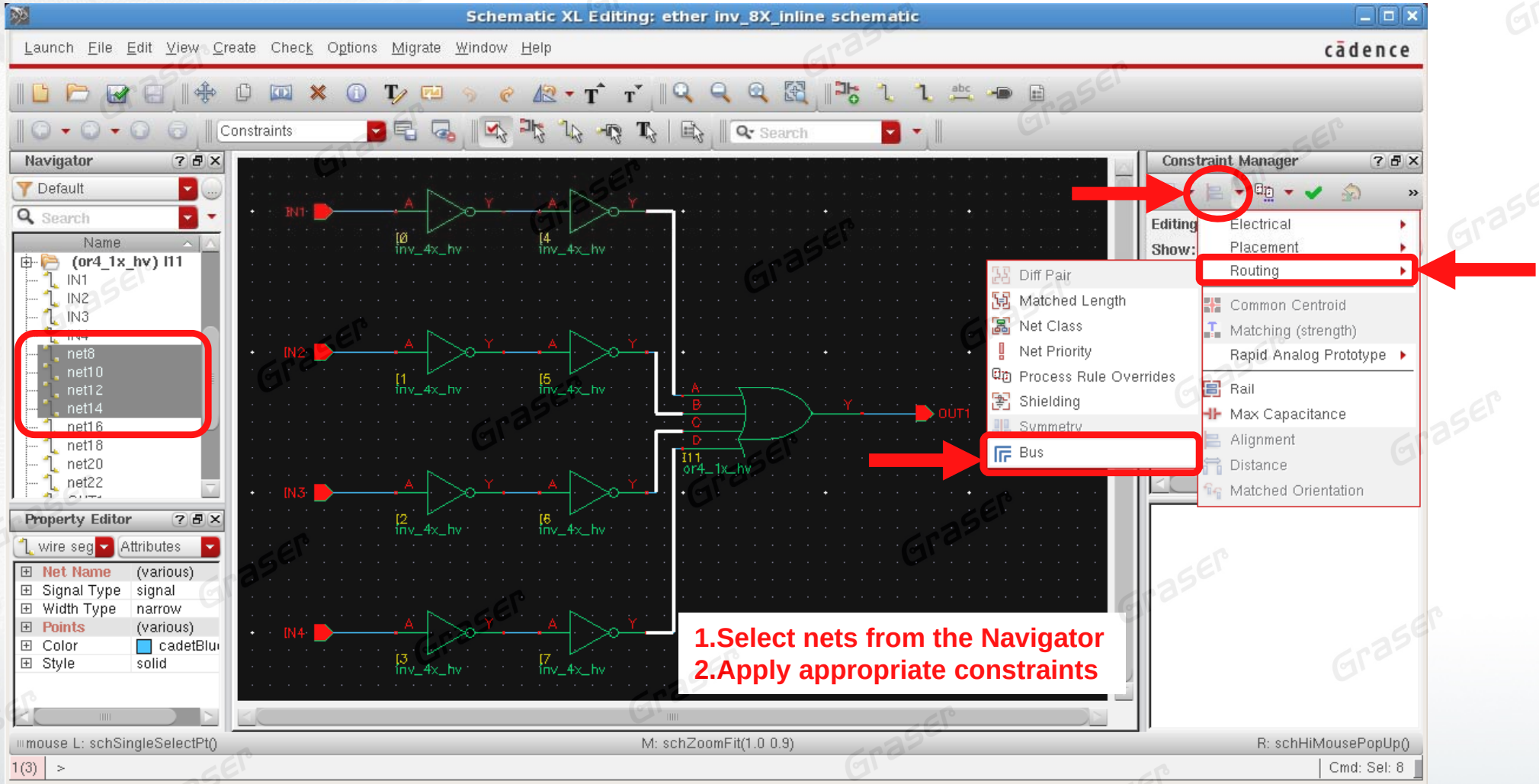
Layout Driven

- Constraint Driven
  - Make Circuit Designers closer to Layout Engineers
  - Common constraint environment to ensure correct-by-construction layout
  - Higher productivity, and fewer physical verification iterations

- Generate From Source (GFS)
  - Quickly generate layout device from schematic
  - Directly get Device type 、Parameter from schematic
  - Connectivity Highlight and Checking

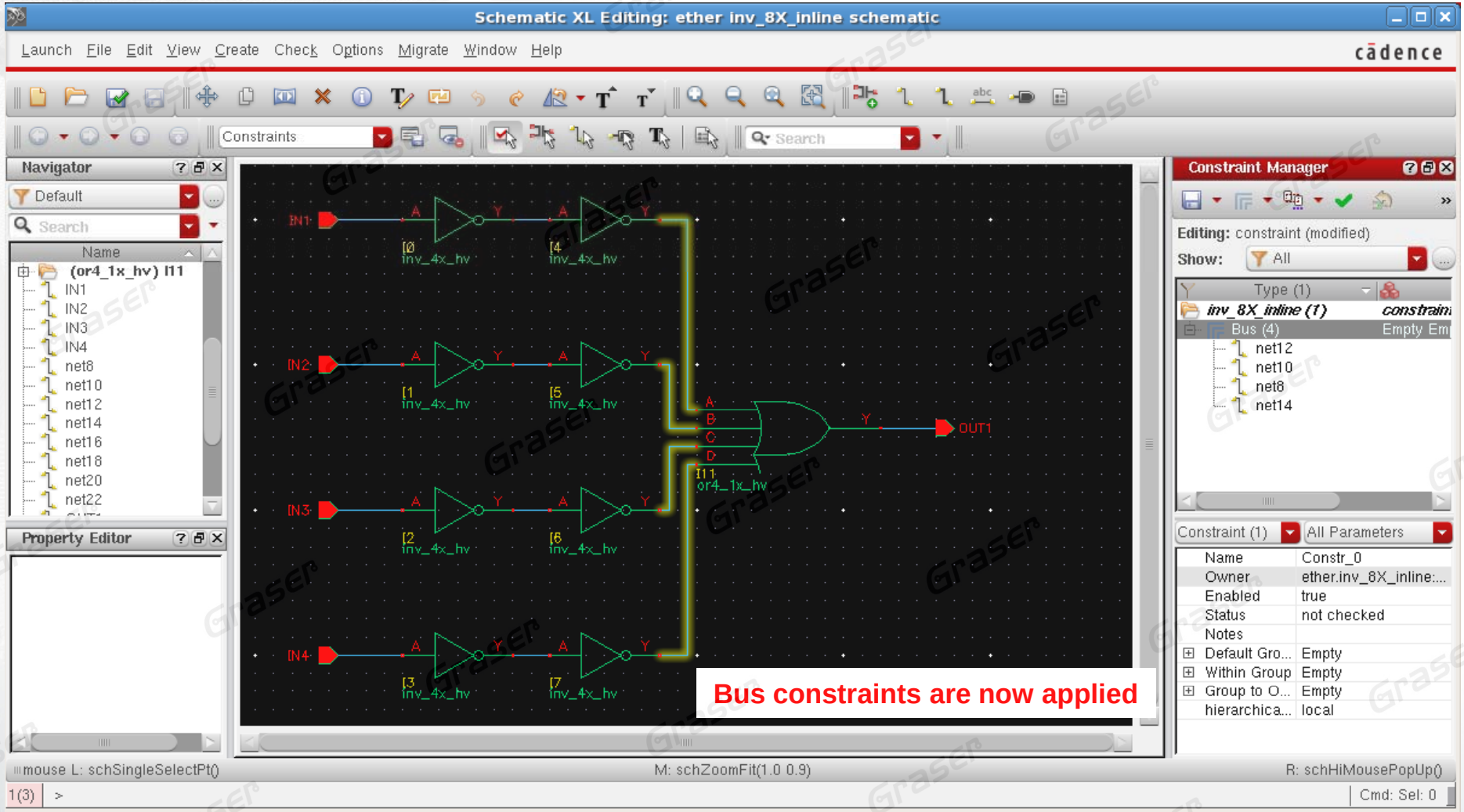
Constraint Driven Layout

Constraints Setting in the Schematic



Constraint Driven Layout

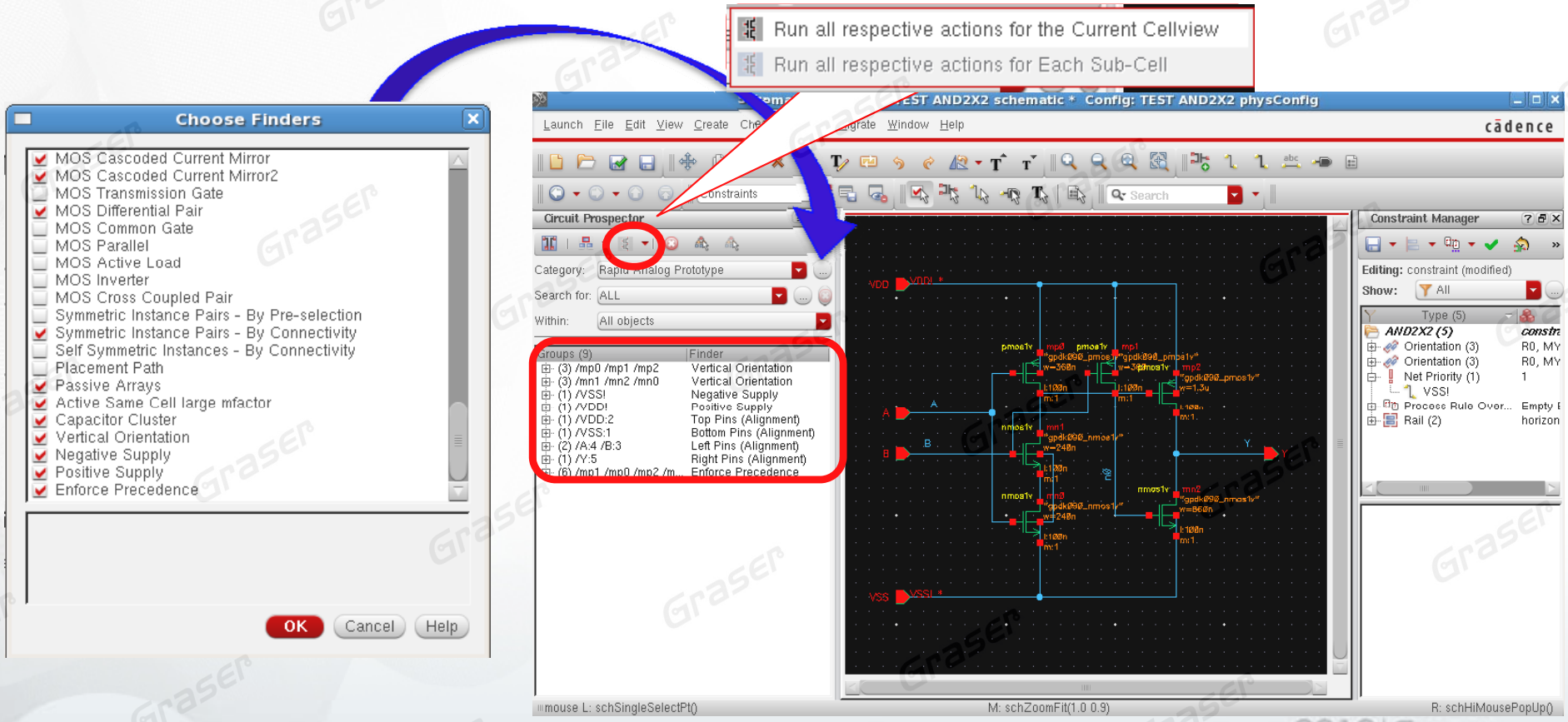
Setting Constraints in the Schematic



Constraint Driven Layout

Automatic Constraint Generators

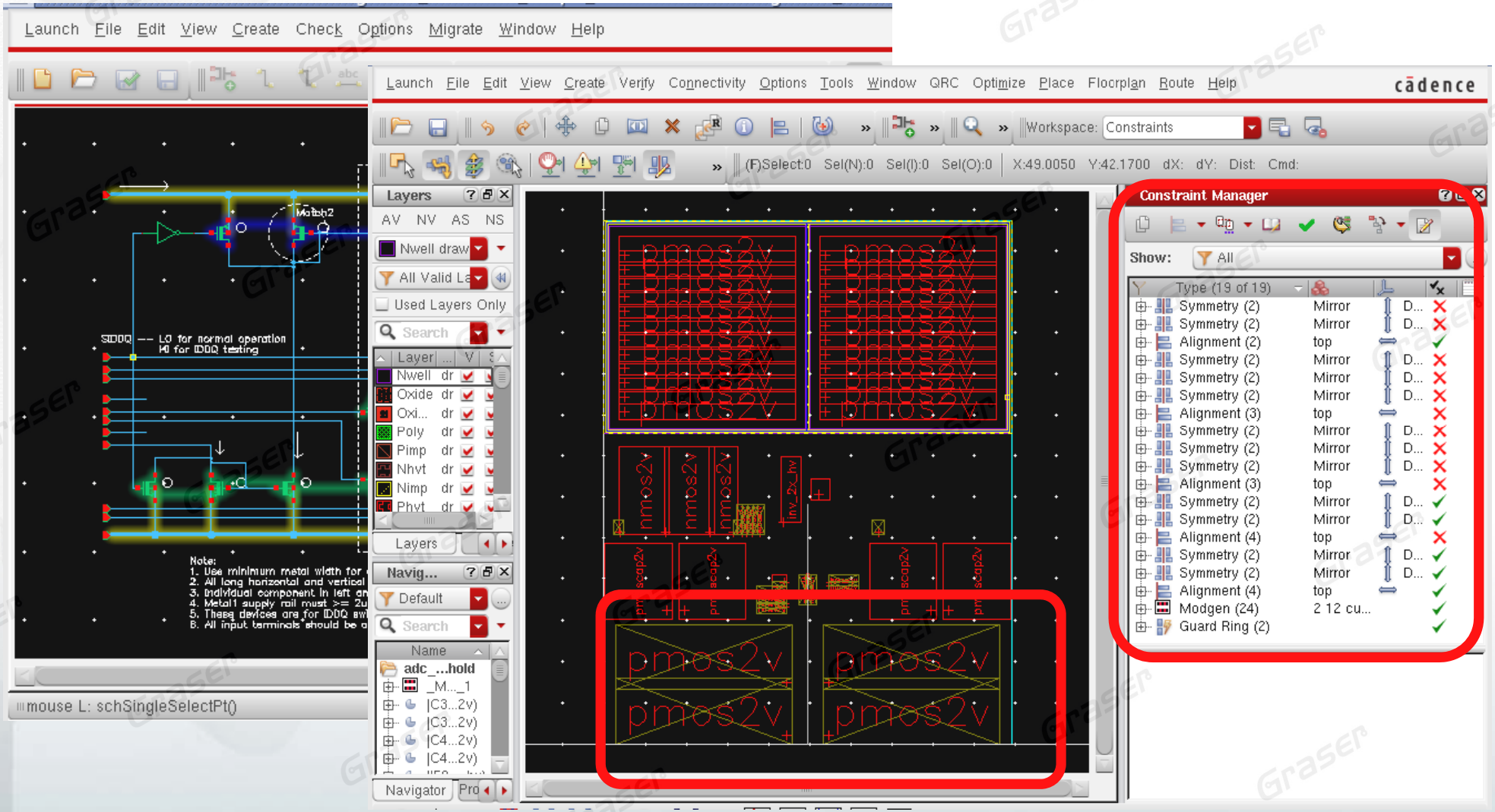
- Single **Rapid Analog Prototype(RAP)** Category in the Circuit Prospector containing all the finders/generators required to automatically constrain a design with just a few mouse clicks



Constraint Driven Layout

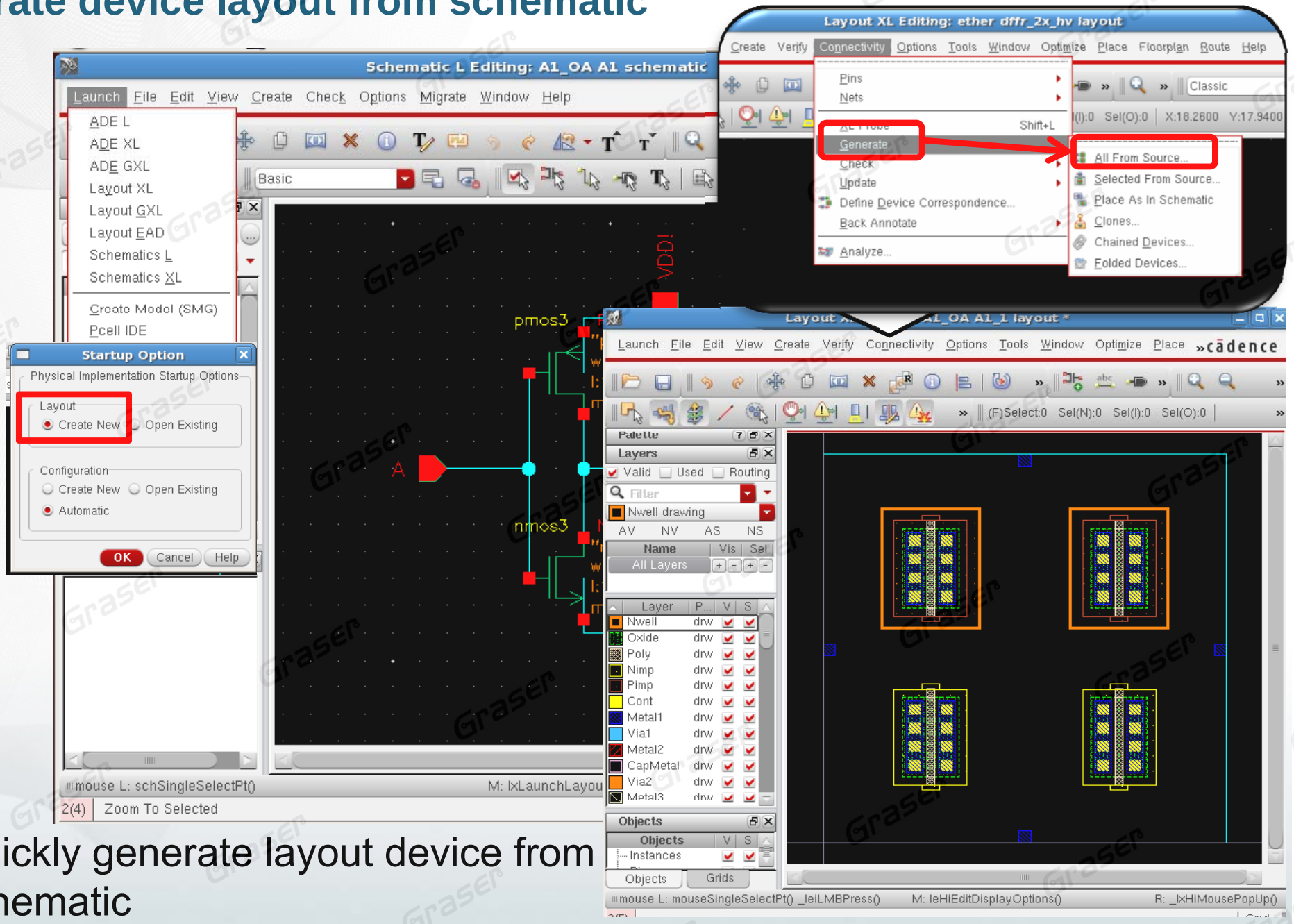
Constraint Manager

- Common constraint environment to ensure correct-by-construction layout



Generate From Source

Generate device layout from schematic

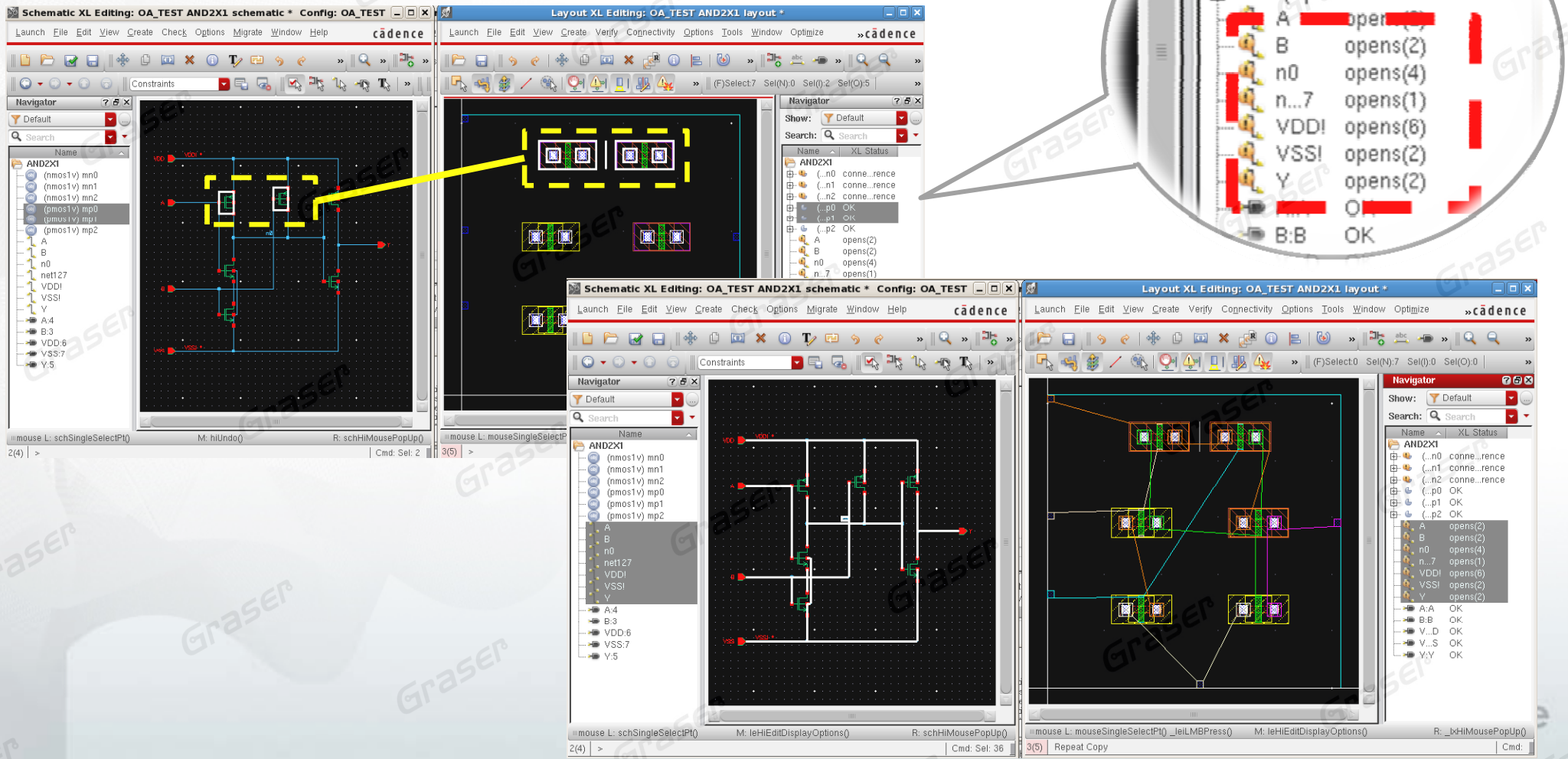


- Quickly generate layout device from schematic

Generate From Source

Generate device layout from schematic

- Cross probing
- Connectivity highlight and checking
- Show incomplete nets and check For Opens/Short



Summary

- Integration with Virtuoso front-to-back custom & analog solution
- Virtuoso is New, fast, easy-to-learn, easy-to-use for design
- Virtuoso Schematic Editor speeds up the largest and most complex custom designs
- Virtuoso ADE is the direct access to MMSIM to realize your silicon
- Virtuoso Layout Suite speeds custom designs to the market
  - Quick placement, routing and editing
  - Reduce DRC and LVS errors
  - Enhance the productivity and efficiency of layout
- Reduces a risk by maintaining design intent between design specification and implementation with unified common constraint environment