

# New!! Customize IC Design and Simulation Flow

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13/Aug/2013

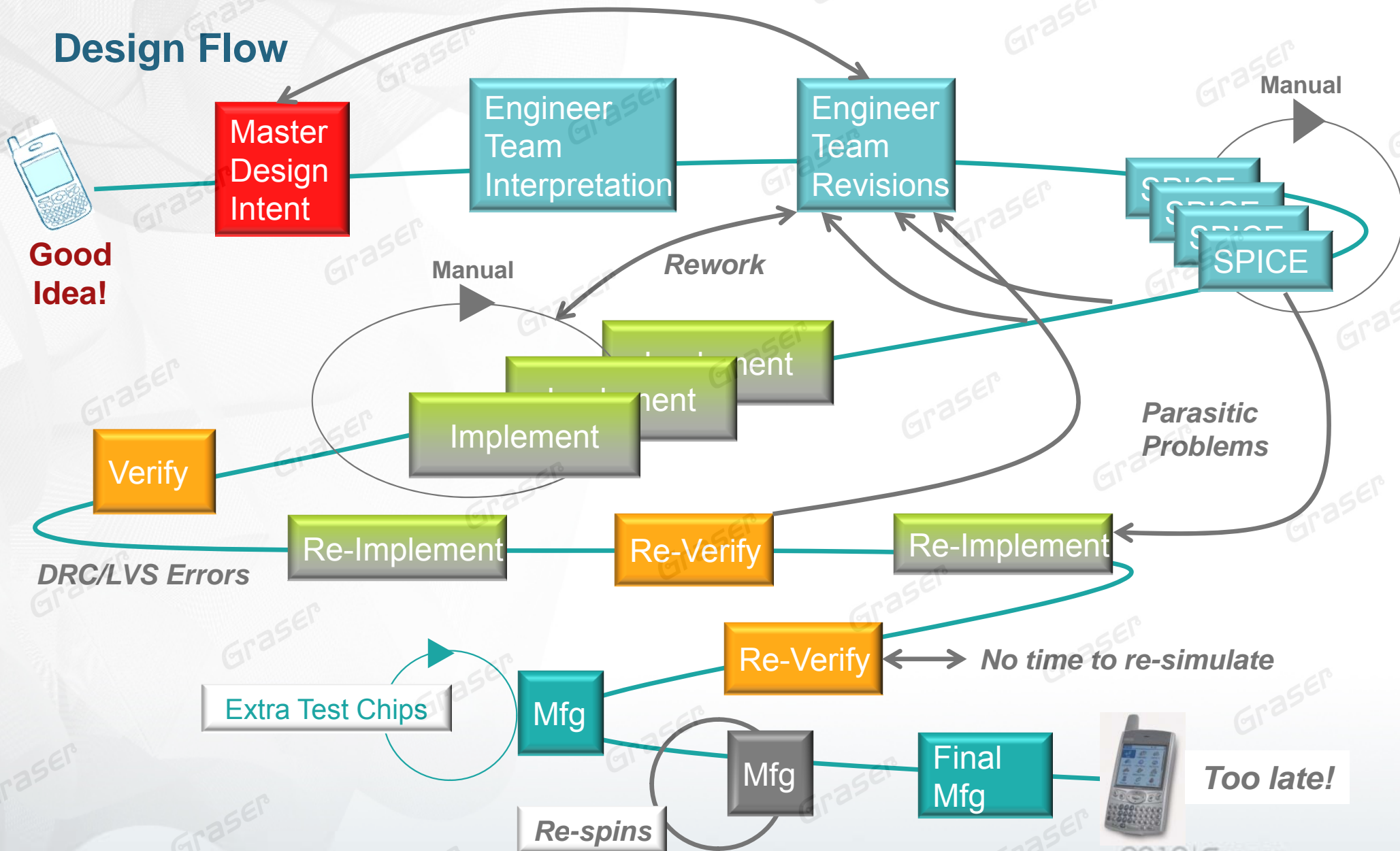
# Topic

- Overview
  - Challenges
  - Cadence's Complete Solution
- Virtuoso Custom Design and Verification
  - Ease and Speed to develop the largest and complex schematic
    - **Virtuoso Schematic Editor**
  - Fast and Accurate design verification
    - **Analog Design Environment**
    - **Multi-Mode Simulation**
- Virtuoso Custom Implement
  - Rapid layout implementation
    - **Virtuoso Layout Suite**
- Summary

# Overview

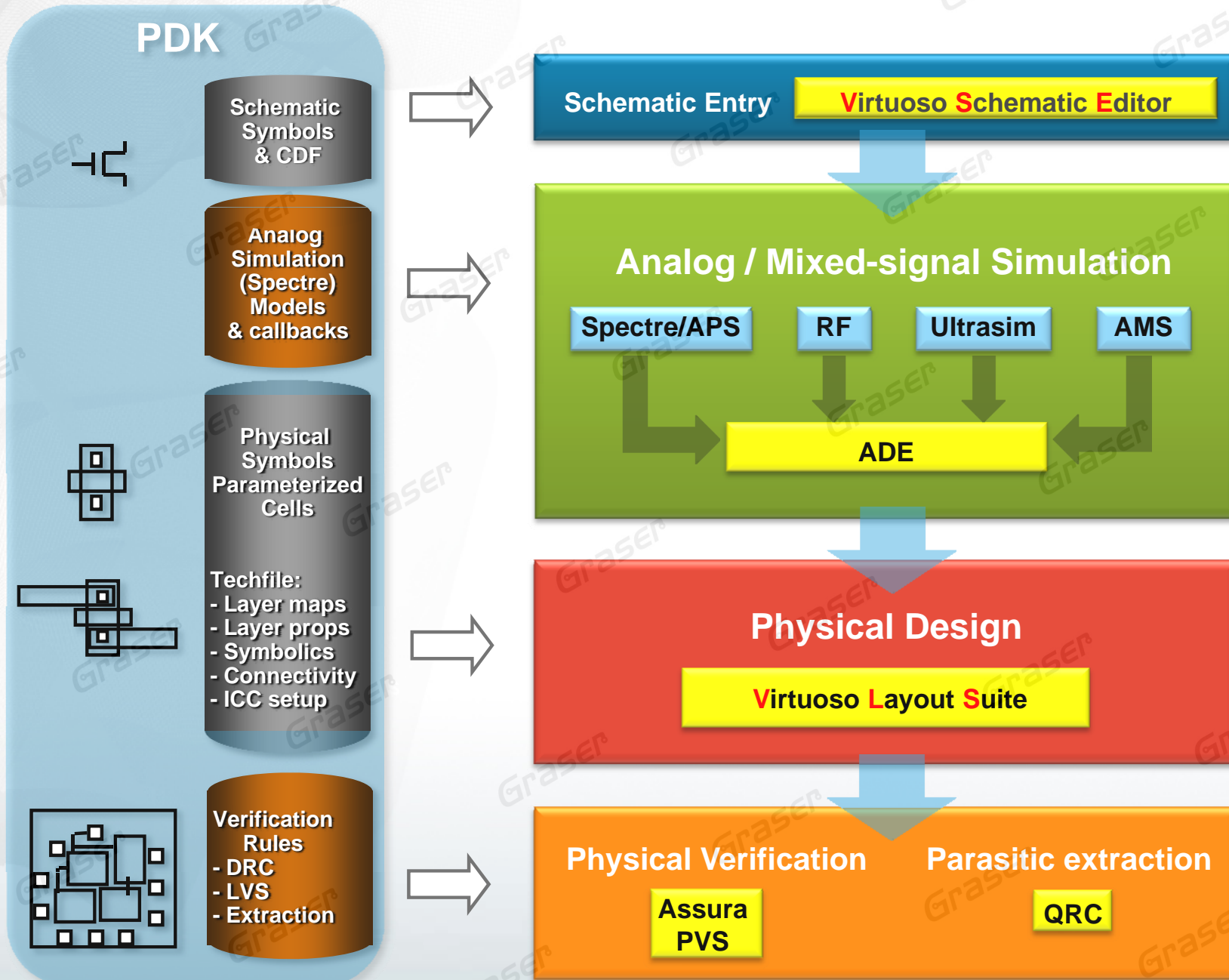
# Overview

## Design Flow



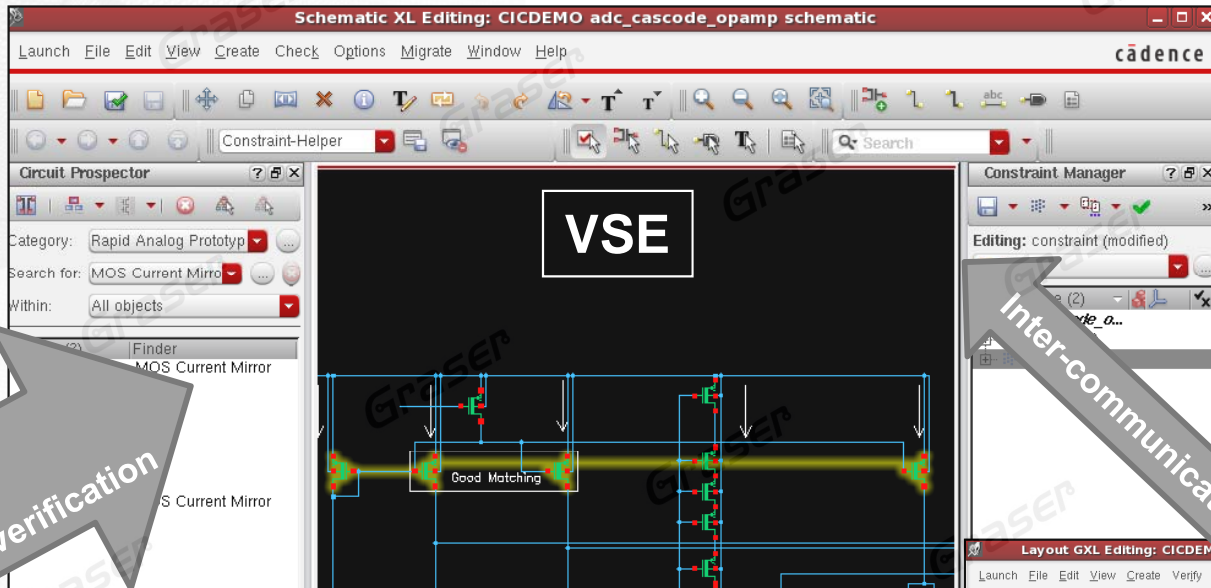
# Overview

Cadence's complete custom design for front to back analog, RF, and mixed-signal



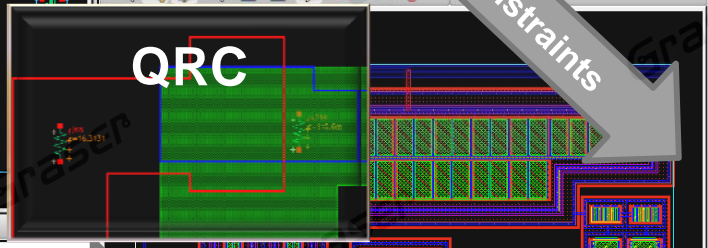
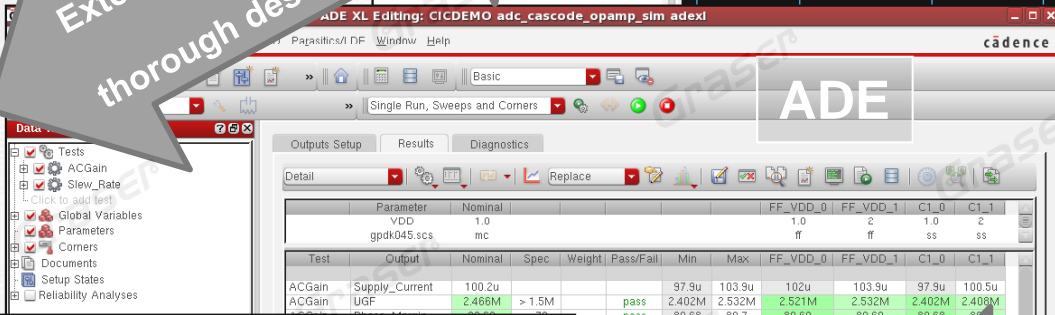
# Overview

Cadence's complete custom design for front to back analog, RF, and mixed-signal

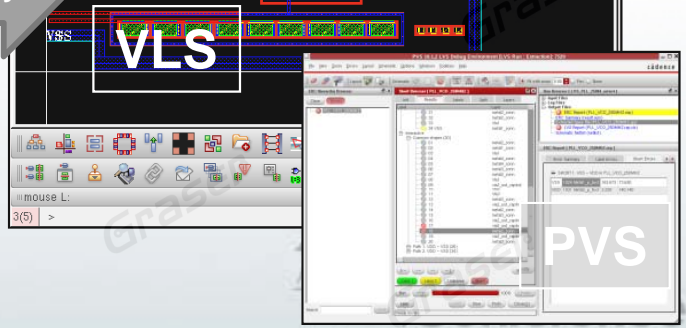
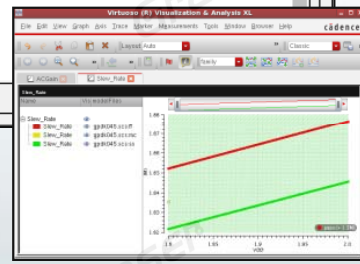
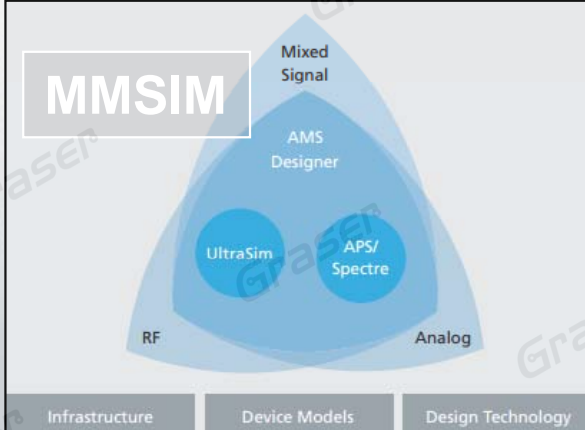


Extensive analysis and thorough design verification

Inter-communication with Constraints



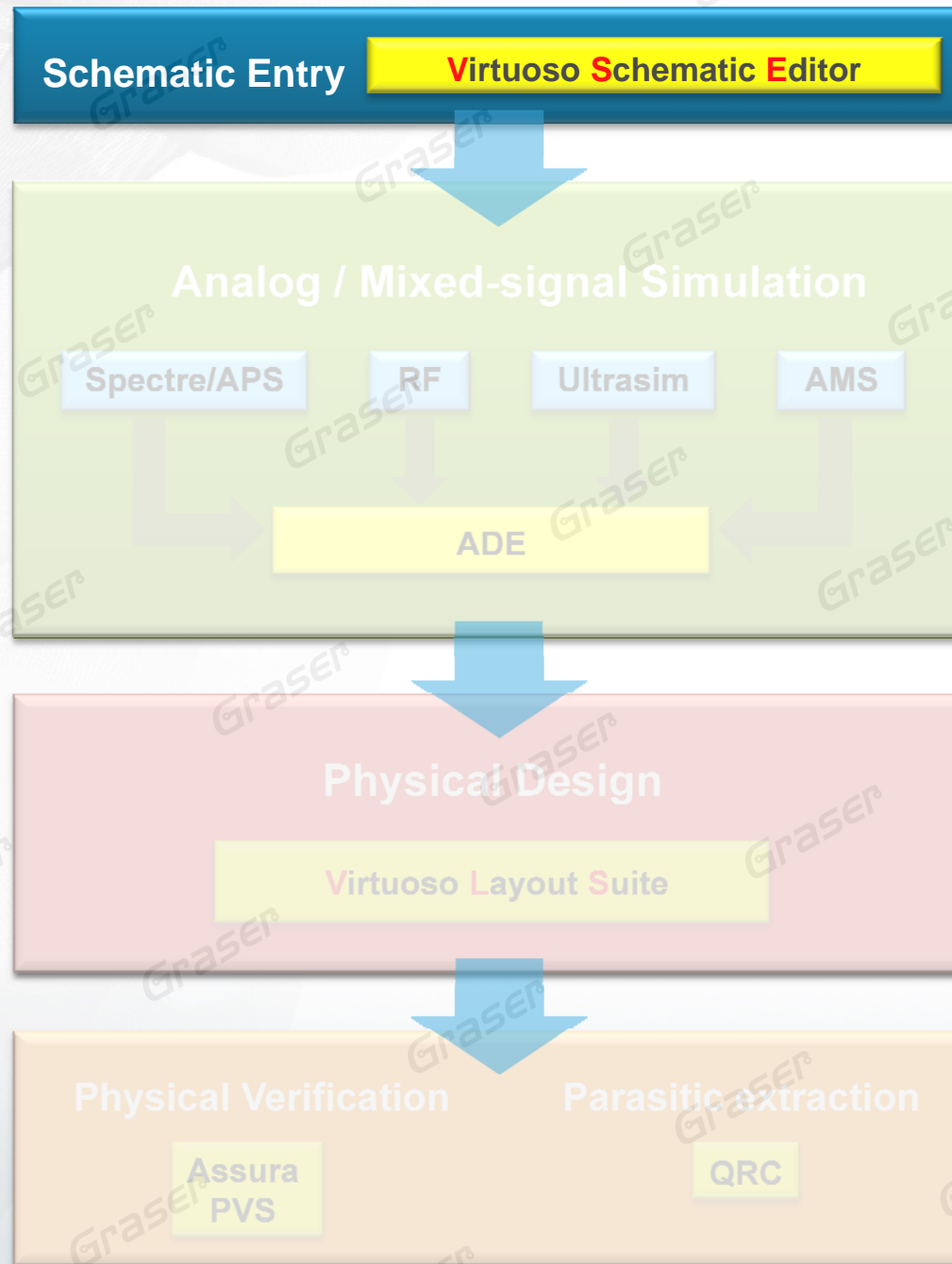
post-layout parasitic analysis



# Virtuoso Custom Design and Verification

*Ease and Speed to develop the largest and complex schematic  
Fast and Accurate design verification*

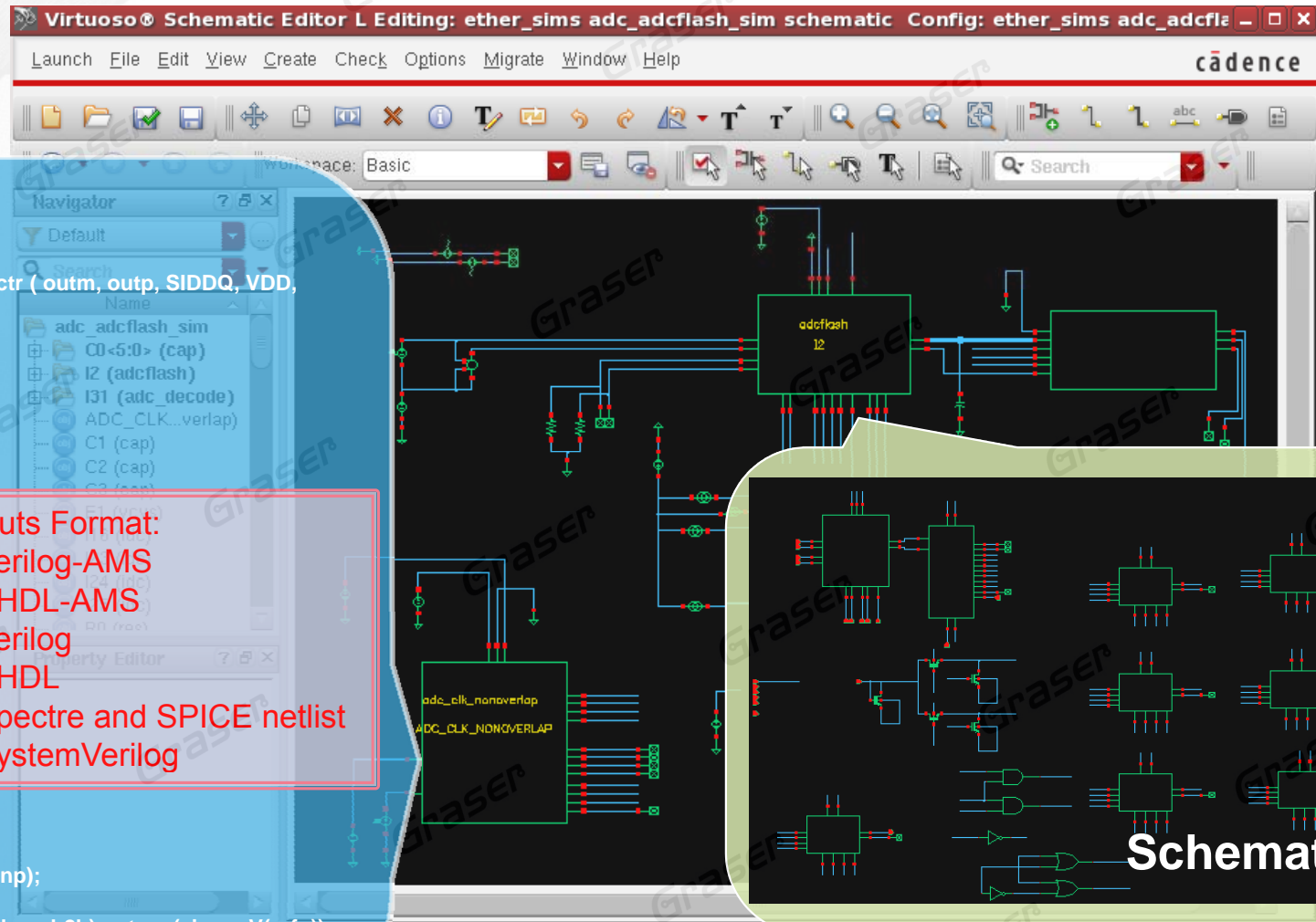
# Virtuoso Custom Design and Verification





# Virtuoso Schematic Editor

- Hierarchical schematic entry and hierarchy editor supports
- Analog, digital, mixed-signal, and RF symbol libraries are supported



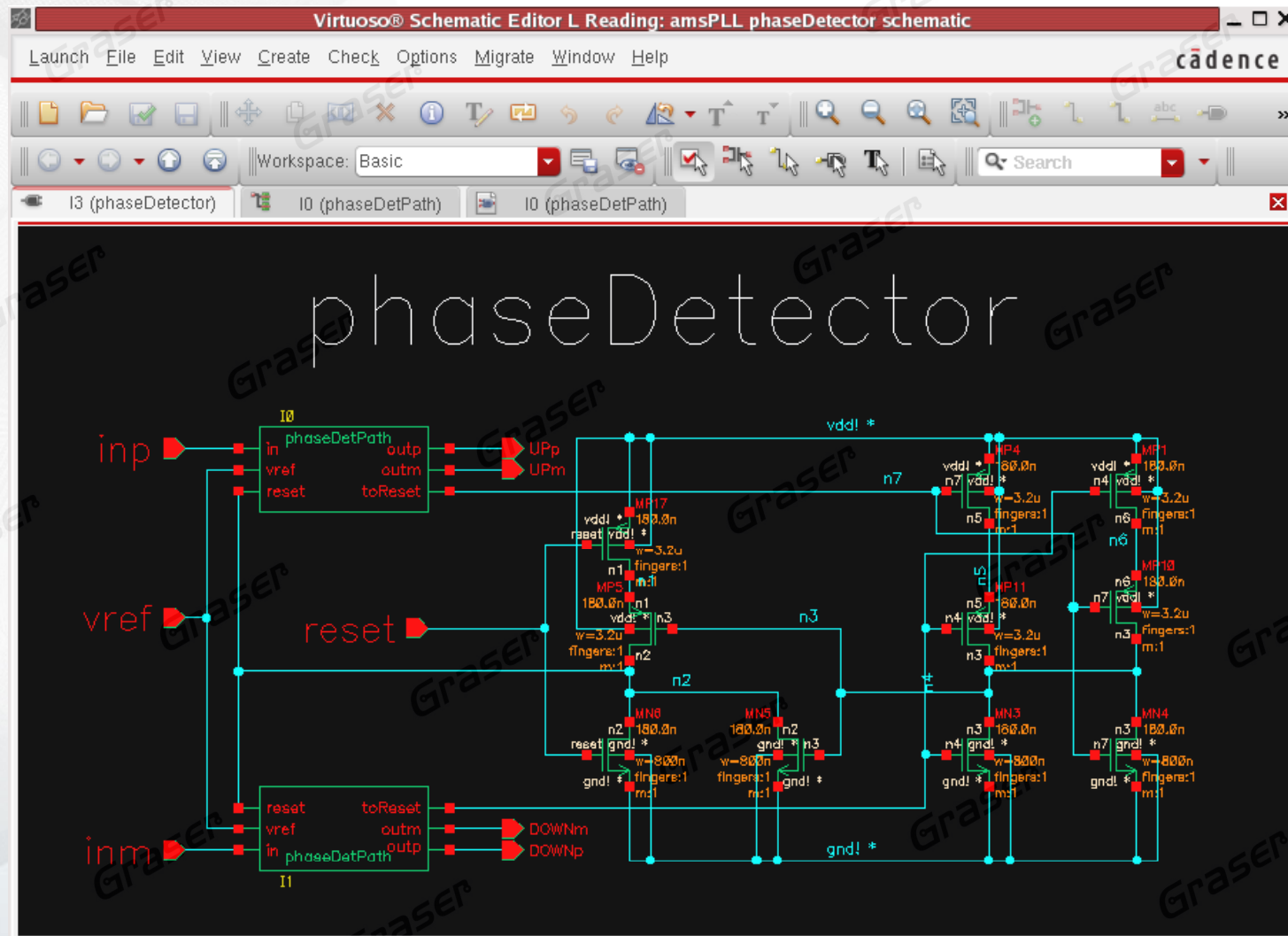
**Inputs Format:**

- Verilog-AMS
- VHDL-AMS
- Verilog
- VHDL
- Spectre and SPICE netlist
- SystemVerilog

# Virtuoso Schematic Editor

## Multi-tab / Multi-view canvas

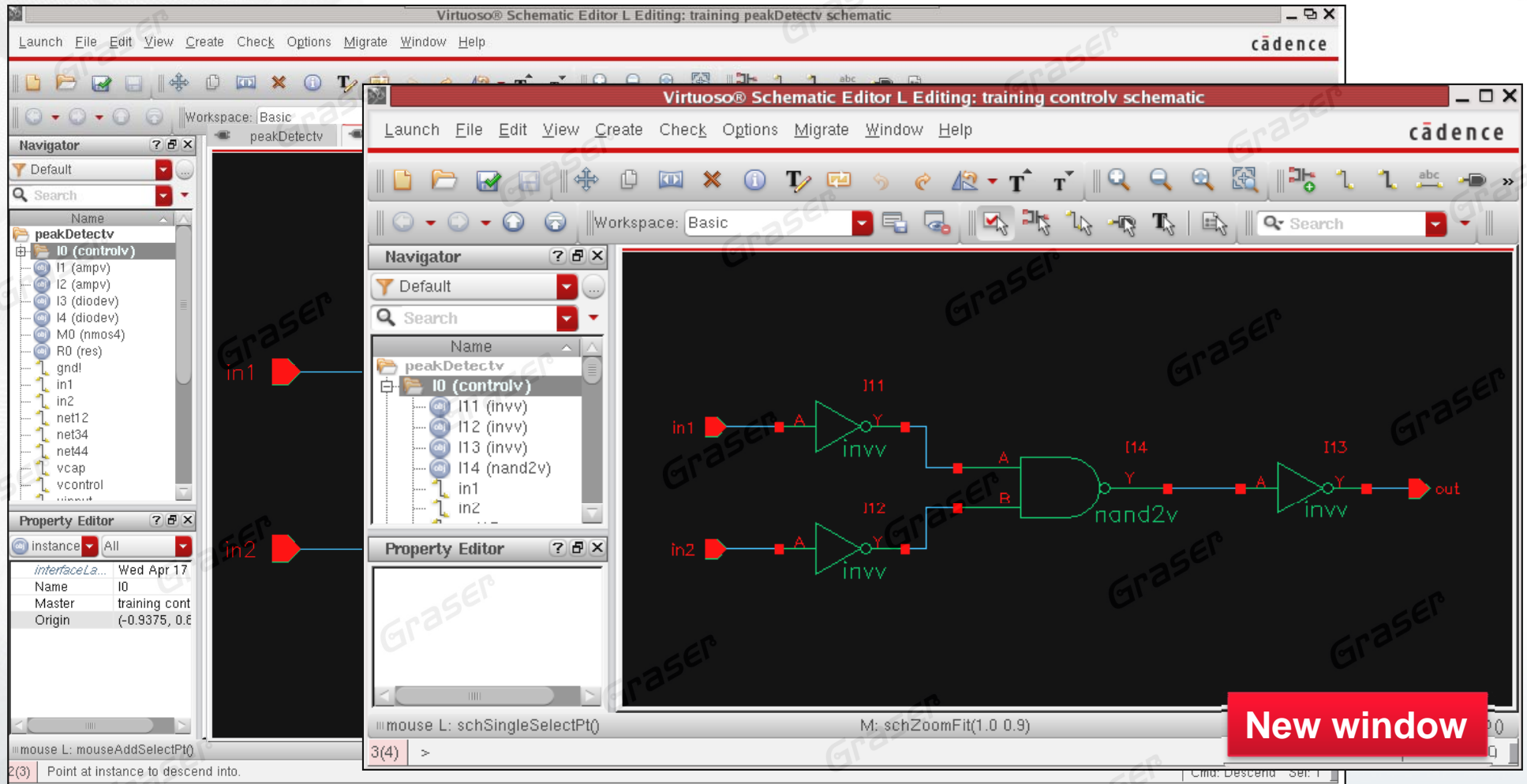
- Open multiple schematics, or different views of the same design



# Virtuoso Schematic Editor

## Multi-tab / Multi-view canvas

- Open multiple schematics, or different views of the same design

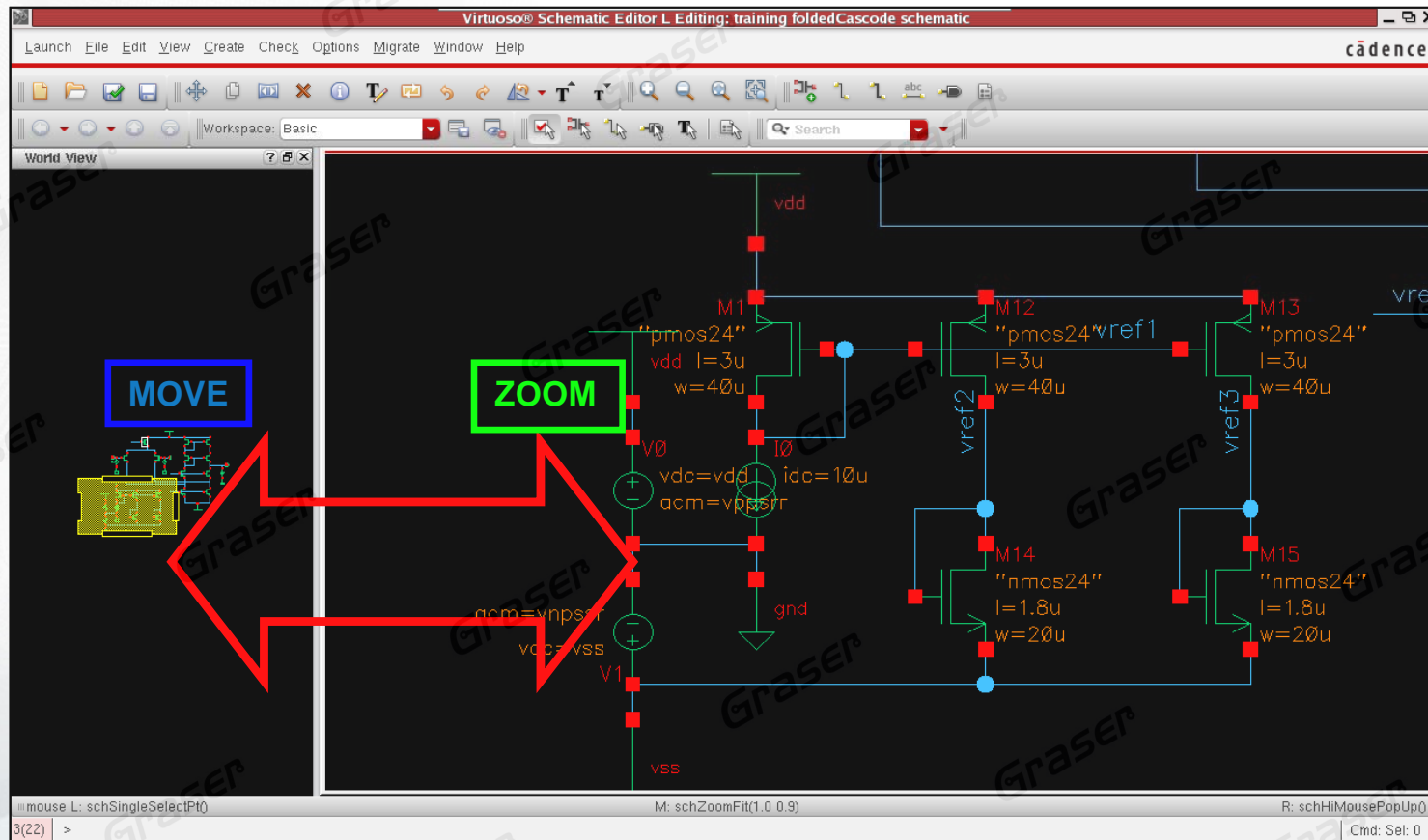


New window

# Virtuoso Schematic Editor

## Design Task Assistants

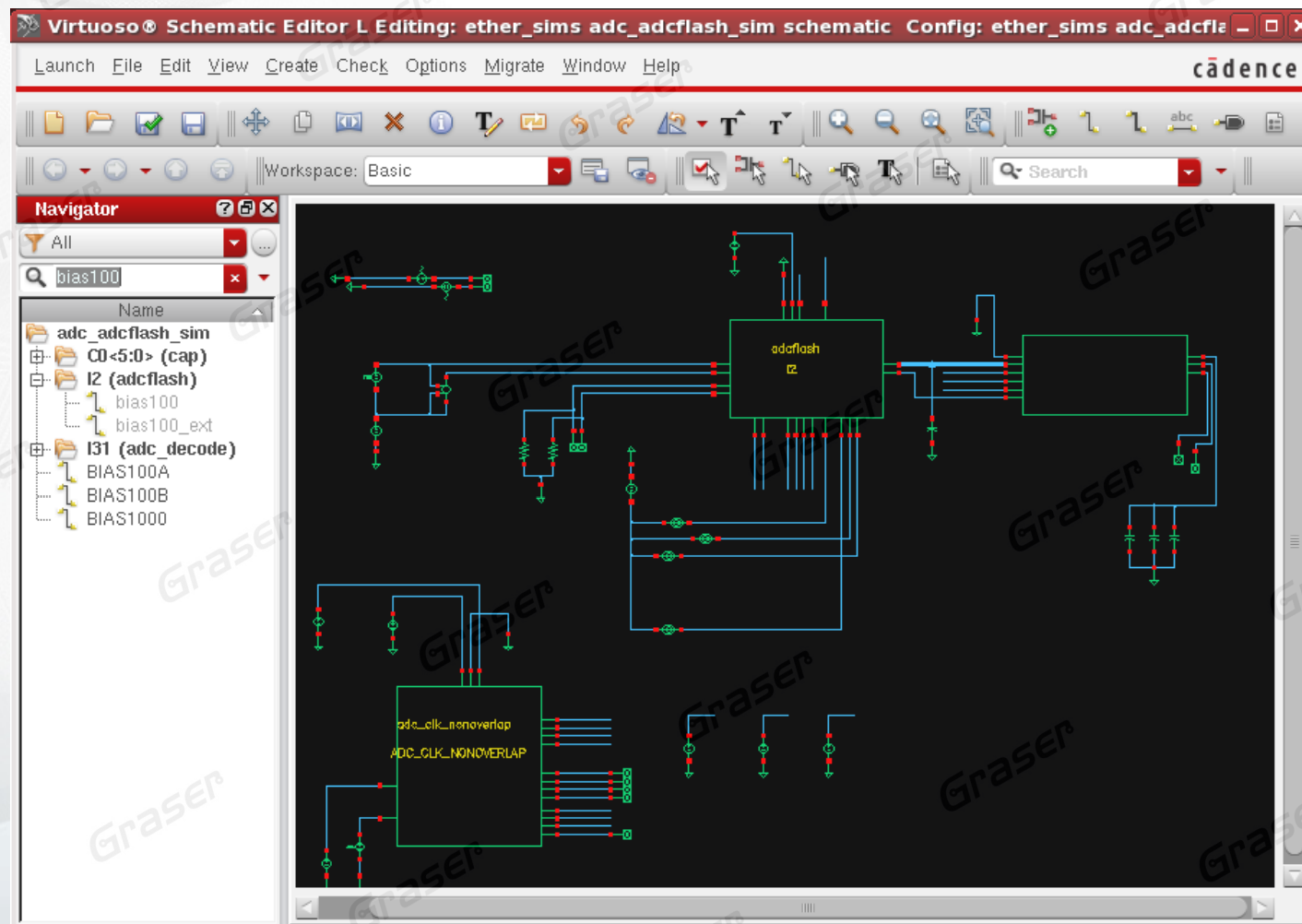
- World View Assistant
  - Panoramic view of an entire schematic
  - Indicating which portion of it is currently visible in the editor window



# Virtuoso Schematic Editor

## Design Task Assistants

- Navigator Assistant
  - Efficient, intuitive access to the complete design hierarchy



# Virtuoso Schematic Editor

## Design Task Assistants

- Search Assistant
  - Quick, comprehensive search engine

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The main window shows a schematic diagram of a folded cascode circuit. The circuit includes several PMOS transistors (M0, M2, M3) and a current source (V2). The schematic is annotated with parameters such as  $l=3\mu$  and  $w=40\mu$  for the PMOS devices. Power supply rails for  $vdd$ ,  $vref1$ ,  $vref3$ , and  $vpos$  are shown, along with ground connections.

On the right side, a search window titled "Search" is open, displaying 29 results for the search term "M0". The results are organized into several categories:

- CDF Parameters (22)**: A list of 22 parameters for the M0 model, including Bulk node con..., Hot-electron d..., Estimated oper..., Dist. beth neig..., Dist. OD & pol..., Dist. OD & pol..., Additional sour..., Additional drai..., Source/drain s..., Temp rise from..., Multiplier, Source diffusio..., Drain diffusion..., Source diffusio..., Drain diffusion..., Drain diffusion..., Source diffusio..., Length, Width, and Model name.
- Instance Pins (3)**: A table showing pins for M0 instances.
- Instances (1)**: A table showing the instance M0.
- Nets (3)**: A table showing nets for M0 instances.

Name	Library	Cell	View
M0	analogLib	pmos	symbol

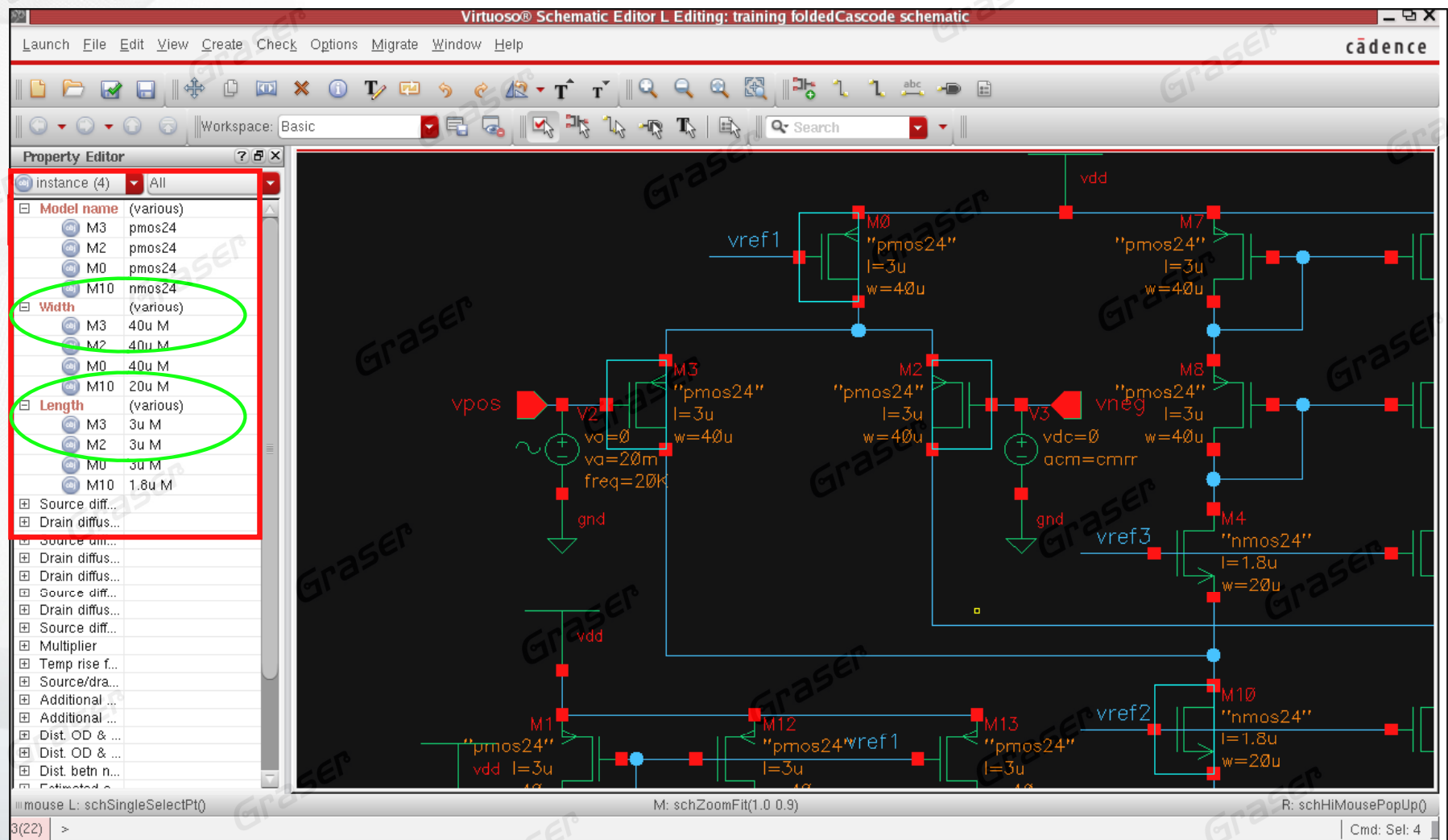
Name	Library	Cell	View
D		net28	inout
G		vref1	inout
S		vdd!	inout

Name	Library	Cell	View
net28	3	M3/S M0/D M...	training.folde
vdd!	10	M6/S M7/S M...	training.folde
vref1	6	M13/G M0/G ...	training.folde

# Virtuoso Schematic Editor

## Design Task Assistants

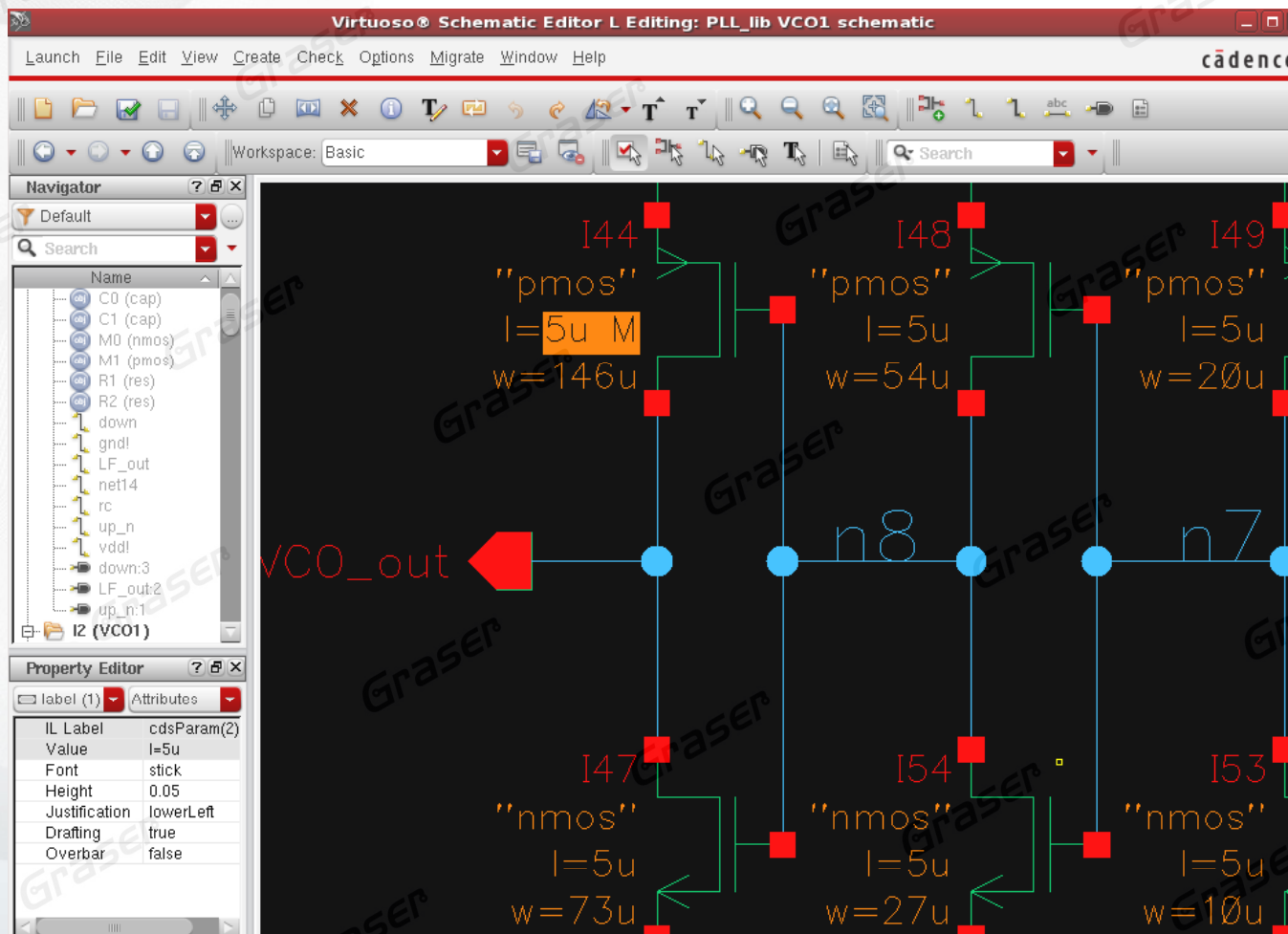
- Property Editor Assistant
  - Intuitive editing of multiple properties on a single object or multiple objects



# Virtuoso Schematic Editor

## Text Editing

- Direct Text Edit
  - speed to change the values of text





# Virtuoso Schematic Editor

## Automatic creation wire stubs and labels

- Wire Stubs and Names
  - It allows automatic creation of such wire stubs and labels.

The screenshot displays a schematic diagram with four instances of the component 'adcflash\_comparator\_actr'. Each instance is connected to a network of terminals and wires. The terminals are labeled with names like 'ph1', 'ph2b', 'VSS', 'bias\_3bit', 'inp', 'inn', 'refp', 'refn', 'shoutp', 'shoutm', 'outp', and 'outm'. The wires are labeled with net names like 'net72', 'net44', 'net56', 'net74', and 'net86'. Two dialog boxes are overlaid on the schematic:

**Add Instance**

Library: ether  
Cell: adcflash\_comparator\_actr  
View: symbol  
Names:   
 Add Wire Stubs at:  
 all terminals  registered terminals only  
Array: Rows: 1, Columns: 1  
Buttons: Rotate, Sideways, Upside Down

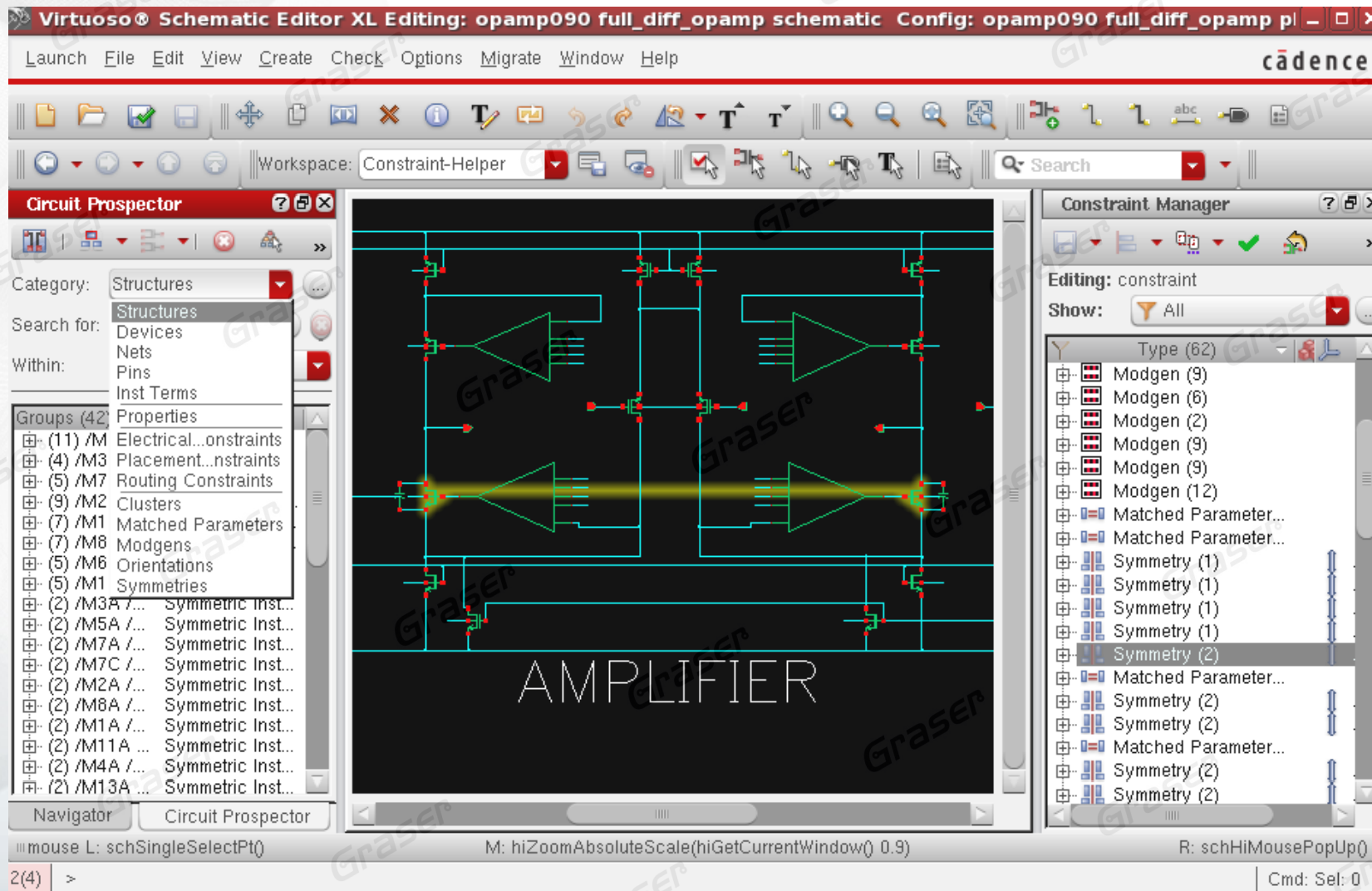
**Net Name Registration**

Terminal Name	Default Net Name
ph1	ph1
inp	
inn	
outp	shoutp
outm	shoutm
VDD	VDD
ph2b	VDD
VSS	VSS
vbias	
SIDDQ	
refn	

# Virtuoso Schematic Editor

## Constraint environment

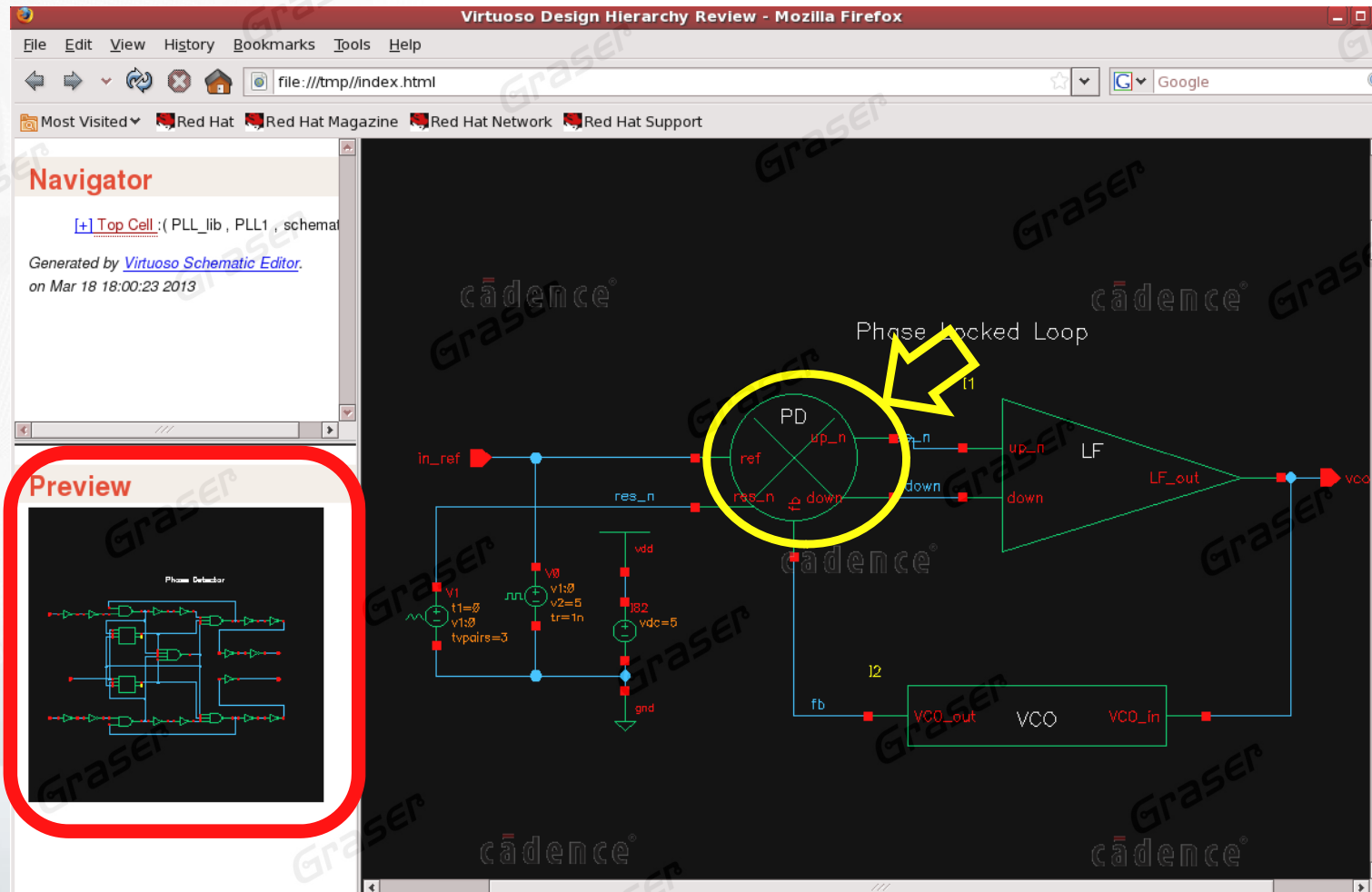
- Easily communicate critical design constraints between multiple users/sites



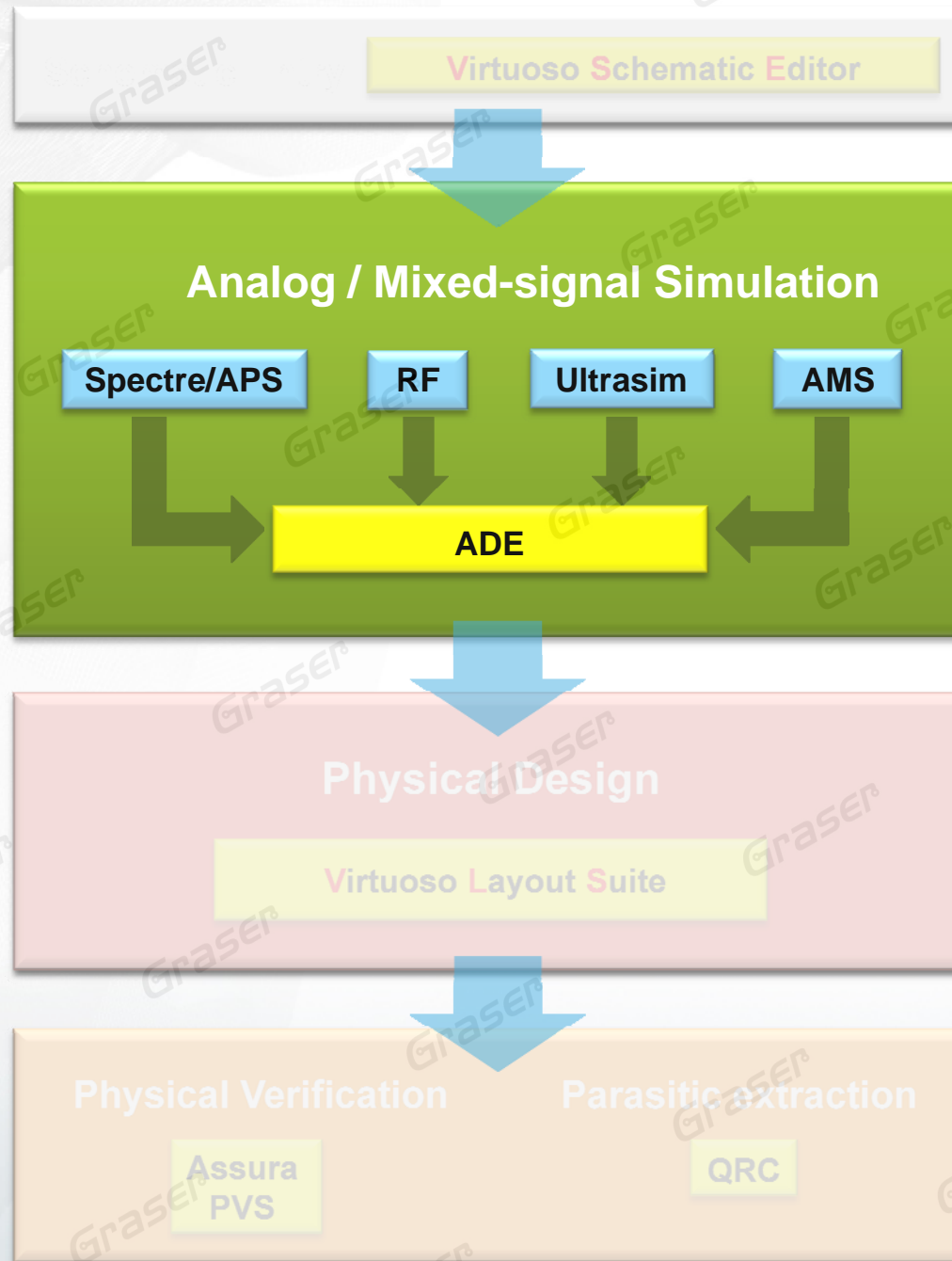
# Virtuoso Schematic Editor

## Quick schematics graph output

- HTML Publisher
  - Schematic design hierarchy is published that can be displayed in a web browser



# Virtuoso Custom Design and Verification



# Analog Design Environment

## Simulation GUI Window

- Not necessary to understand netlist syntax
- Common syntax for different simulators
- Interactive GUI simulation environment

The image displays the Cadence Virtuoso Analog Design Environment GUI. The main window shows a schematic editor with a circuit diagram of an amplifier. The circuit includes an input signal source (v2) with parameters  $v_0=0$ ,  $v_0=50m$ , and  $freq=1M$ . The amplifier is represented by a block labeled 'AMPL' with input nodes 'inp' and 'inm', and output nodes 'out' and 'outm'. The circuit is powered by VDD and VSS rails, with resistors R0 (10K) and R1 (20K) connected to the input and output nodes. The output is connected to a load resistor RL (10K) and a capacitor CL (800f). The circuit is connected to ground (gnd).

Overlaid on the schematic are several windows:

- Design Variables:** A table with columns 'Name' and 'Value'. It contains one entry: CAP with value 800f.
- Analyses:** A table with columns 'Type' and 'Enabled'. It lists three analyses: tran (checked), dc (checked), and ac (checked).
- Choosing Analyses -- Virtuoso® Analog Design Environ:** A dialog box for selecting analysis types. The 'ac' radio button is selected. Other options include tran, dc, noise, xf, sens, dcmatch, stb, pz, sp, envlp, pss, pac, pstb, pnoise, pxf, psp, qpss, qpac, and qpnoise.
- Virtuoso (R) Visualization & Analysis XL calculator:** A window for defining analysis expressions. The expression shown is  $cross(v("vin") ?result "tran") 0.1 "falling" nil nil) - cross(v("net5") ?result "tran") 0.1 "falling" nil nil)$ .
- Outputs:** A window showing a list of available signals and analysis results, including win, out, delay, dBgain, and DCgain.

At the bottom, there is a simulation control panel with buttons for 'Auto', 'Plotting mode: Replace', 'Status: Ready', 'T=27 C', and 'Simulate'. There are also buttons for 'Add Specific Points', 'Specialized Analyses', and 'Options...'. The 'OK', 'Cancel', 'Defaults', 'Apply', and 'Help' buttons are at the bottom right.

# Analog Design Environment

## Annotate

- Back-annotating Simulation Information with Schematic

The screenshot displays the Cadence Virtuoso Analog Design Environment (ADE) interface. The main window shows a schematic diagram of a training amplifier circuit. The circuit includes two MOSFETs (M1 and M2), a resistor (R0), and a current source (Q0). The schematic is annotated with various simulation results, such as node voltages, currents, and power. The 'Results' menu is open, showing the 'Annotate' option selected. A sub-menu is visible, listing various simulation results that can be annotated, including DC Node Voltages, DC Operating Points, Model Parameters, Transient Node Voltages, Transient Operating Points, Net Names, Component Parameters, Design Defaults, Show Parasitics, and Hide Parasitics. The status bar at the bottom indicates the simulator is 'spectre' and the state is 'test'.

**Virtuoso® Analog Design Environment (2) - training ampTest schematic**

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help

Design Variables

Name	Value
CAP	800f

**Virtuoso® Analog Design Environment L Editing: training amplifier schematic -- Virtuoso® Analog Design Environment**

Launch File Edit View Create Check Options Migrate Window Help

Workspace: ADE L

Plotting mode: Replace

plotted... | T=27 C | Simulator: spectre | State: test

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# Analog Design Environment

## Multi-test Environment

The screenshot shows the Cadence Virtuoso Analog Design Environment (ADE) interface. The main window is titled "Virtuoso® Analog Design Environment XL Editing: amsPLL\_test\_1 PLL\_160MHZ\_LF adexl". The interface includes a menu bar (Launch, File, Create, Tools, Options, Run, Parasitics, Window, Help) and a toolbar. The "Data View" panel is active, showing a tree structure of tests and variables. A blue arrow points from the "Data View" panel to the "Run Summary" panel. The "Run Summary" panel displays the following information:

- 3 Tests
- 1 Point Sweep
- 0 Corner
- Nominal Corner

The "Outputs Setup" panel shows a table of test outputs:

Test	Output	Nominal	Spec
amsPLL_test_1:PLL_160MHZ_LF:1	/TAP	⚡	
amsPLL_test_1:PLL_160MHZ_LF:1	/DUMP	⚡	
amsPLL_test_1:PLL_160MHZ_LF:1	/VSS	⚡	
amsPLL_test_1:PLL_160MHZ:1	/CLK_REF	⚡	
amsPLL_test_1:PLL_160MHZ:1	/I3/vCNTL	⚡	
amsPLL_test_1:PLL_160MHZ:1	/CLK_160MHZ	⚡	
amsPLL_test_1:PLL_NDVR:1	/IPLY_25u	⚡	
amsPLL_test_1:PLL_NDVR:1	/VSS	⚡	
amsPLL_test_1:PLL_NDVR:1	/VREF	⚡	
amsPLL_test_1:PLL_NDVR:1	/DN	⚡	
amsPLL_test_1:PLL_NDVR:1	/PD	⚡	

The "Status" panel at the bottom shows "Build Estimated View".

# Analog Design Environment

## Specification-driven design

- Quick Spec setup
- color-coded feedback of all results against target specifications
- Intuitive overview color-coded graph with spec

The screenshot displays the Cadence software interface with a 'Data View' window showing test results for 'amp2a\_GFS\_d1'. The interface includes a menu bar (Launch, File, Create, Tools, Options, Run, Parasitics, Window, Help) and a toolbar. The 'Data View' window has tabs for 'Outputs Setup', 'Results', and 'Diagnostics'. A 'Detail' window is open, showing a table of test results. A graph in the bottom left shows a red area labeled 'Red, fail' and a green area labeled 'Green, pass'.

Parameter Model Group	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF	FS	SF
n... T_CLKtoQ	91.69p	< 250p		pass	65.92p	136.5p	136.5p	66.61p	65.92p	126.3p
n... T_DtoQ	231.7p				205.9p	276.5p	276.5p	206.8p	205.9p	266.3p
ID:1 T_CLKtoQ	108.7p	< 250p		pass	-1.001n	169.4p	169.4p	76.11p	-987.8p	-1.001n
ID:1 T_DtoQ	248.7p				-861.1p	309.4p	309.4p	216.1p	-847.6p	-861.1p
:1 T_CLKtoQ	177.2p	< 250p		near	109.1p	274.6p	274.6p	127.2p	109.1p	256.2p
:1 T_DtoQ	317.2p				249.1p	414.6p	414.6p	267.2p	249.1p	396.2p



# Analog Design Environment

## Parasitic Effects

- Parasitic Estimation
  - Helps to quickly identify parasitic sensitivities prior to layout

The image displays the Cadence ADE XL Parasitic Estimation tool interface. The main window shows a circuit schematic with various components and connections. The 'Parasitic Estimates' window is open, showing the 'Extracted' section with a tree view of extracted parasitics. The 'Run Summary' window is also open, showing the results of the parasitic extraction.

**Run Summary**

- 1 Test
- ✓ 1 Point Sweep
- ✓ 4 Corners
- ✓ Nominal Corner

**Outputs Setup** | **Results** | **Diagnostics**

Detail

Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF	FS	SF
/OUT										
/OUT_bar										
/Vin										
/Vref										
/VDD										
/CLK										
/gnd1										
T_DtoQ	369.2p				306.6p	485.3p	485.3p	306.6p	309.9p	452.4p
T_CLKtoQ	229.2p	< 250p		fail	166.6p	345.3p	345.3p	166.6p	169.9p	312.4p

Estimated\_10f+8f

# Analog Design Environment

## Parasitic Effects

- post-extracted layouts simulation
  - Support av\_extracted file
  - Show parasitic sum value on report and schematic view

The image displays a multi-panel view of the Cadence ADE XL environment. On the left, a layout view shows a complex network of red and blue traces. A callout window provides a magnified view of a specific parasitic element, showing a resistor with a value of  $r=273.9m$  and a capacitor with a value of  $c=1.7159$ . The central panel shows the 'Parasitic Report' window, which displays a table of parasitic values for various nets. The table includes columns for Net, R, Sum C, Sum L, and Sum K. The right panel shows a schematic view of the circuit, with various components like PMOS, NMOS, and resistors, and parasitic values overlaid on the schematic. The bottom panel shows the 'Data View' window, which displays simulation results for various parameters, including T\_CLKtoQ, T\_DtoQ, and T\_setup.

Net	R	Sum C	Sum L	Sum K
/avC17	0	96.6141a	0	0
/net018	~27.253	752.669a	0	0
/net037	~27.3131	800.719a	0	0
/net016	NS	967.672a	0	0
/net028	~20.5013	1.44868f	0	0
/net038	~24.0044	1.55643f	0	0
/net25	~4.43656	1.71554f	0	0
/net039	NS	1.80868f	0	0
/inn	NS	2.04981f	0	0
/inp	NS	2.74816f	0	0
/R_bar	~28.6624	3.17138f	0	0
/outn	~25.0026	3.35626f	0	0
/CK	NS	3.52201f	0	0
/outp	~22.2419	3.53081f	0	0
/VDD	0	3.56998f	0	0
/S_bar	~32.7463	4.26385f	0	0
/VSS	0	11.2129f	0	0

Parameter	Nominal	SS	FF	FS	SF				
T_CLKtoQ	145.4p	< 250p	pass	105.2p	216.6p	106.1p	105.2p	198.7p	
T_DtoQ	285.4p			245.2p	356.6p	356.6p	245.1p	245.2p	338.7p
T_setup	140p			140p	140p	140p	140p	140p	140p

# Analog Design Environment

## Create Datasheet

- Auto-generate the output of the simulation result and graph to the datasheet

**Test HS\_SA:SAFF\_tran\_sethoid\_PAD\_GFS\_1:1**

Source and Contents

The run mode is: Single Run, Sweeps and Corners.  
Parasitics run mode: Extracted.

- [Results Summary](#)
- [Detailed Results](#)
- [Waveforms](#)

**Results Summary**

Test	Calculation	Expression	Target	Minimum Value	Maximum Value
HS_SA:SAFF_tran_sethoid_PAD_GFS_1:1	T_CLKtoQ	(cross(v("OUT" ?result ?tran) 0.5 1 "falling" nil nil) - cross(v("CLK" ?result ?tran) 0.5 2 "rising" nil nil))	< 250p	105.2p	216.8p
HS_SA:SAFF_tran_sethoid_PAD_GFS_1:1	T_DtoQ	(cross(v("OUT" ?result ?tran) 0.5 1 "falling" nil nil) - cross(v("Vin" ?result ?tran) 0.5 1 "falling" nil nil))	245.2p	356.8p	

**Detailed Results**

	Conditions		Outputs	
	Model Specification	T_CLKtoQ	T_DtoQ	
Design Point 1		Value	Value	
Nominal	gpd090.sc3 IN	145.4p	285.4p	
FF	gpd090.sc3 FF	106.1p	246.1p	
FS	gpd090.sc3 FS	105.2p	245.2p	
SF	gpd090.sc3 SF	198.7p	338.7p	
SS	gpd090.sc3 SS	216.8p	356.8p	

**Waveforms**

Transient Response

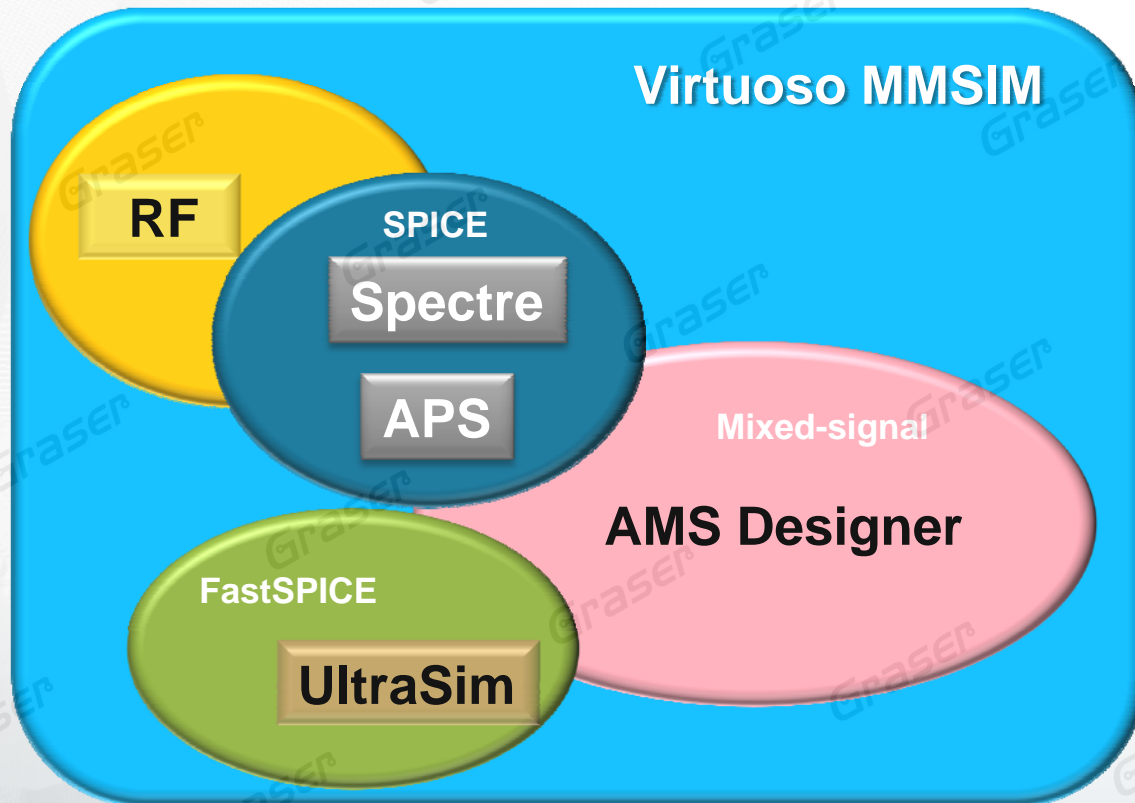
T\_ClkQ\_T\_DtoQ

T\_ClkQ

T\_DtoQ

# Multi-Mode Simulation

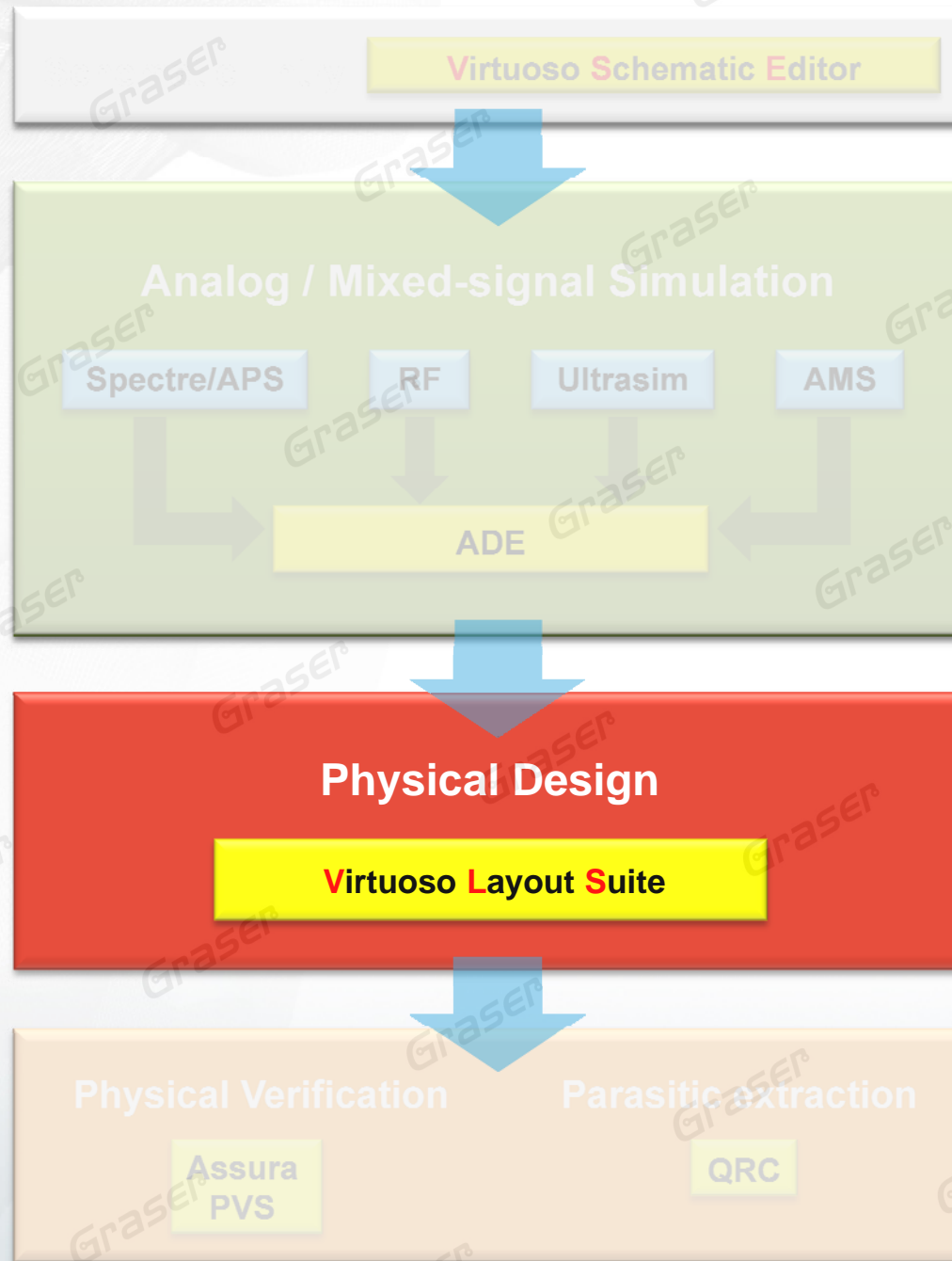
- For Custom Analog and Mixed Signal Design Verification
- MMSIM with multi-core deliver to meet your performance and accuracy



- ✓ Optimized Packaging : Scalability and Flexibility
- ✓ RF Analysis
- ✓ High Performance : AMS- APS Post layout
- ✓ Common model

# Virtuoso Custom Implement

# Virtuoso Custom Implement



# Agenda

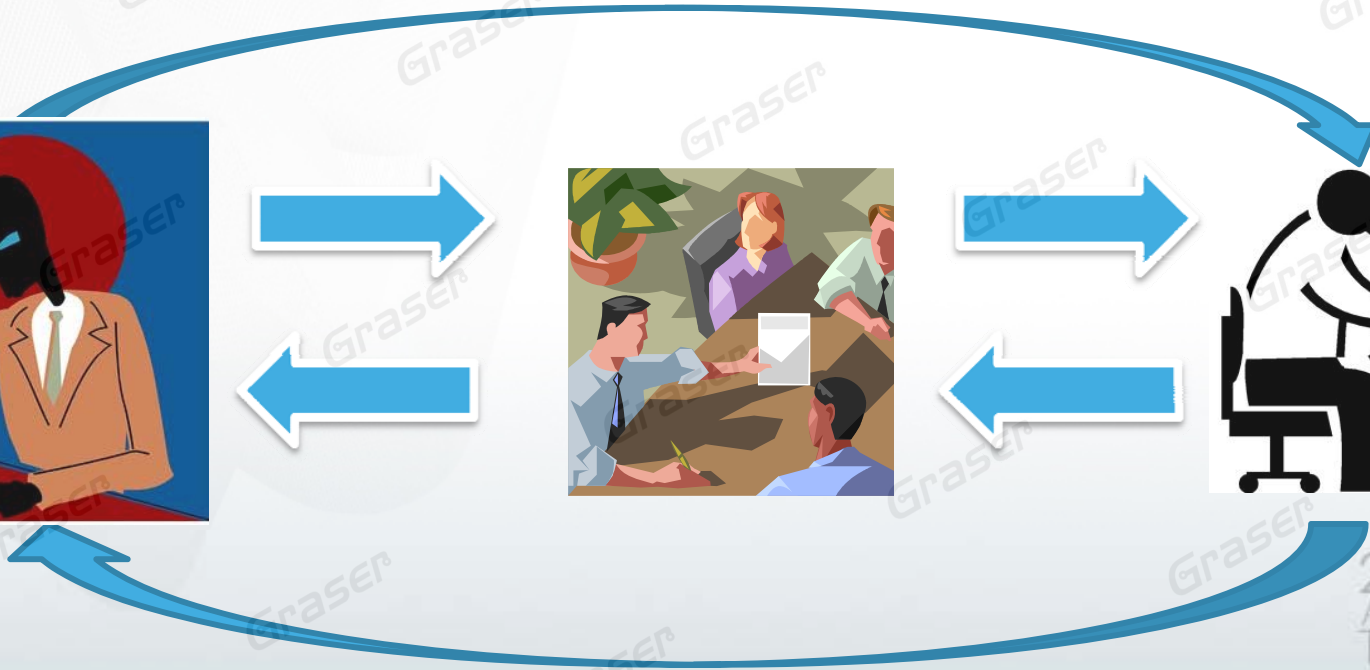
- How to increase Team collaboration and productivity ?
- Customize back-end IC design
  - Manually
    - Accelerate Placement & Editing
  - Semi-Auto
    - Interactive Routing
  - Auto
    - Constrain & Generate From Source

# How to increase Team collaboration and productivity ?



# How to increase Team collaboration and productivity ?

- Capture requirements on How a design is intended to be implemented
- Minimize miscommunication problems with standard design team communications
- Simplify the procedure of Placement & Editing
- Resolve DRC & LVS errors

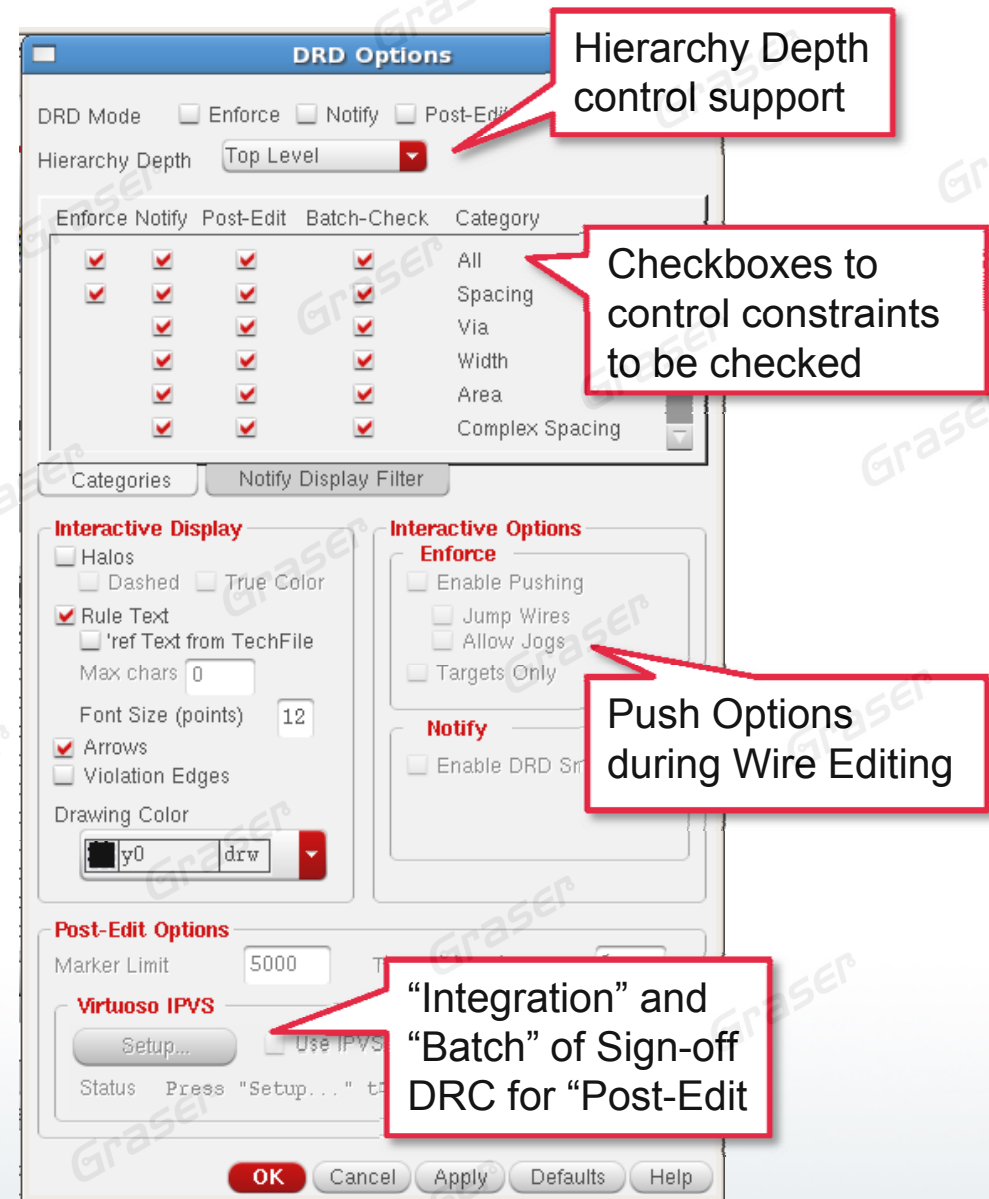


# Manually Accelerate Placement & Editing

# Design Rule Driven

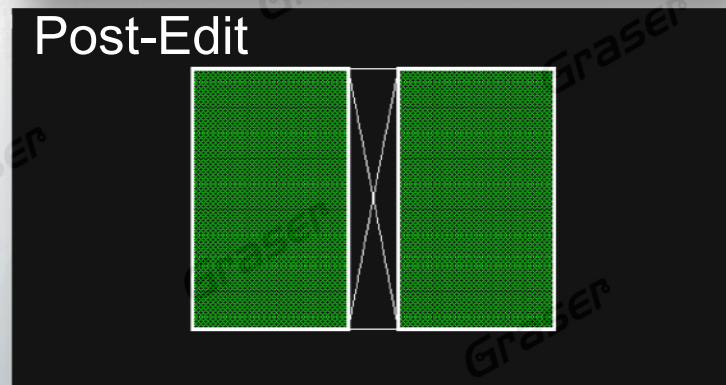
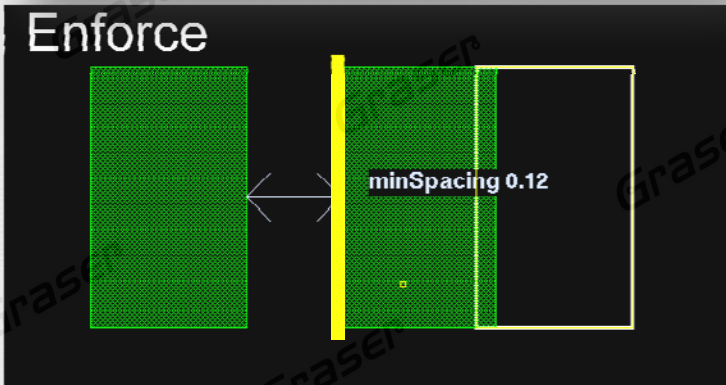
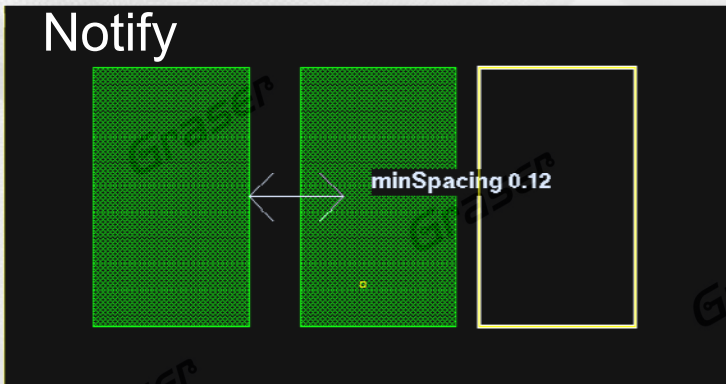
## Interactive Design Rule Checking

- Real-time DRC Checking
- Automatically enforces design rules
- Eliminate physical verification iterations
- Reduce the number of DRC violations during layout editing

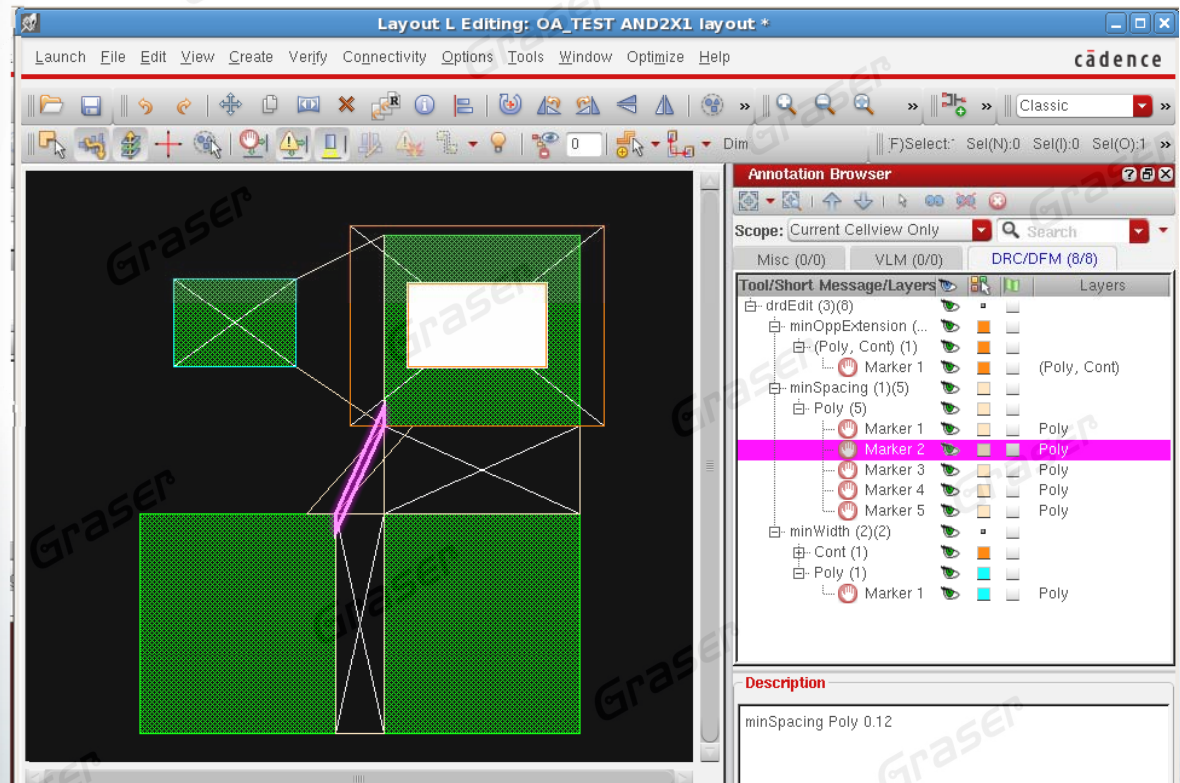


# Design Rule Driven

## Debugging DRC Violations



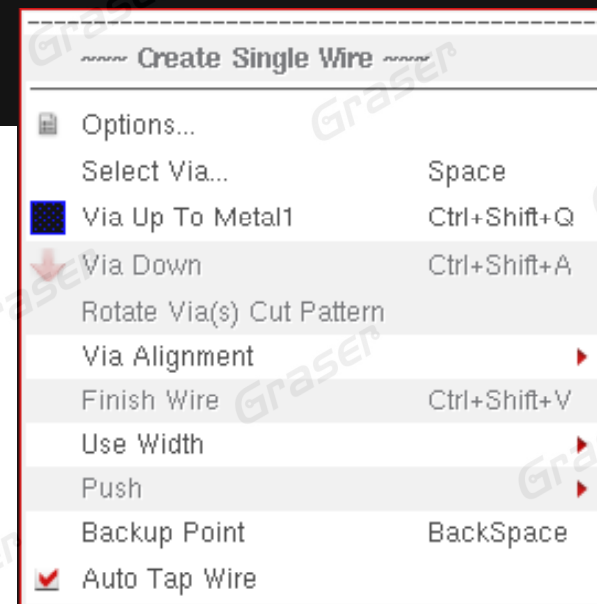
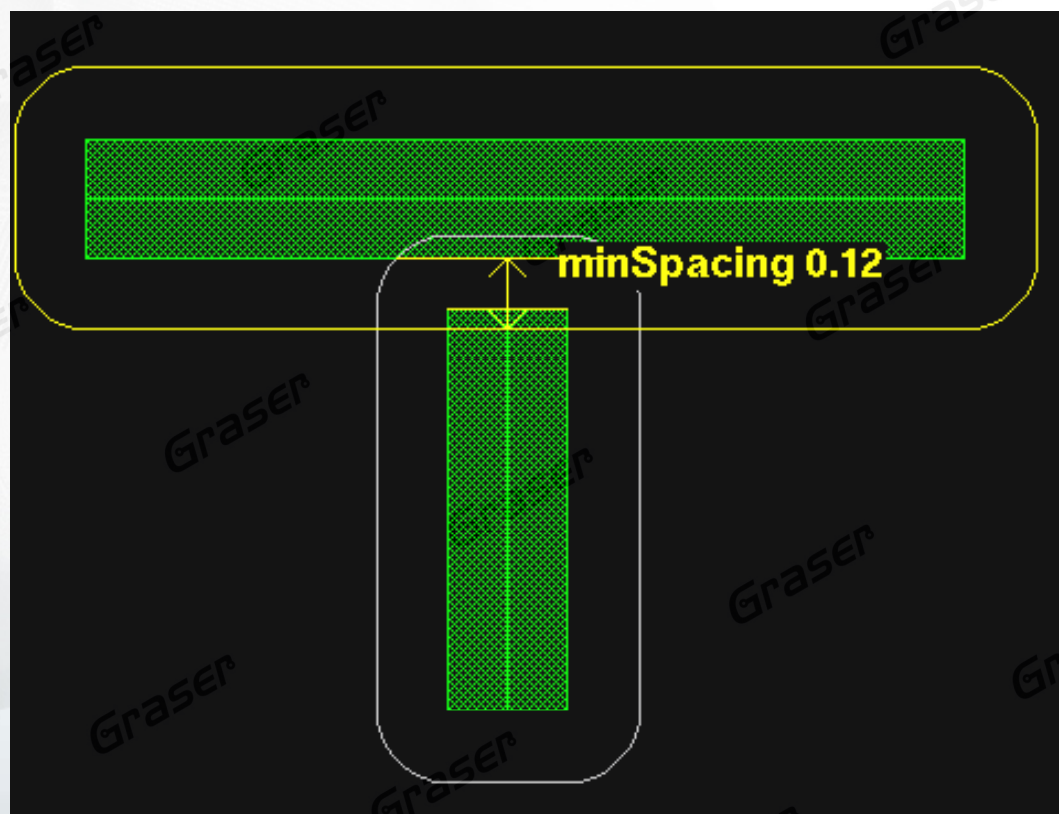
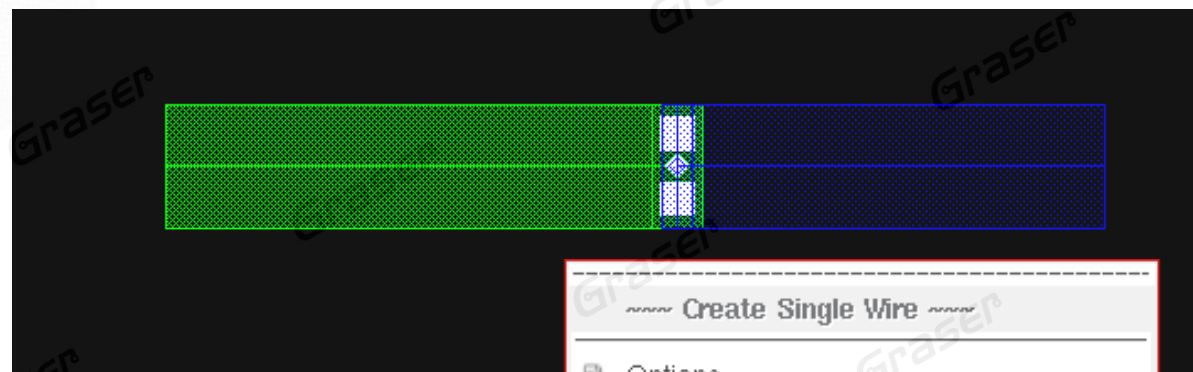
- The post-edit markers can be viewed, analyzed, and filtered in the DRC/DFM tab of Annotation Browser.
- The markers are the persistent objects, which can be saved.



# Interactive Wire Editing

## Wire Routing

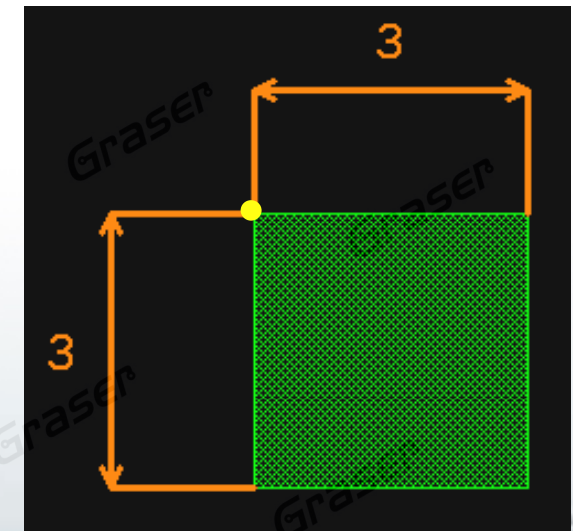
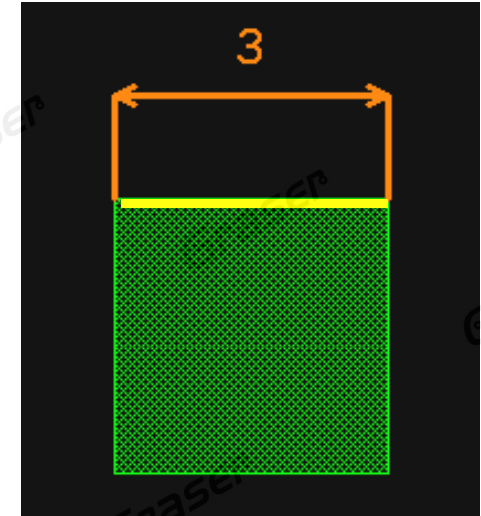
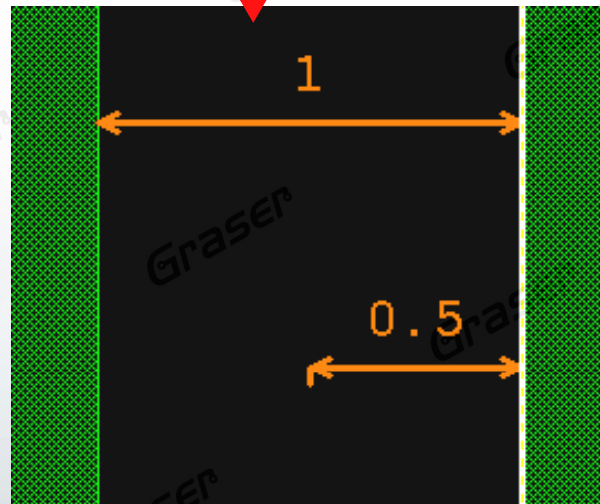
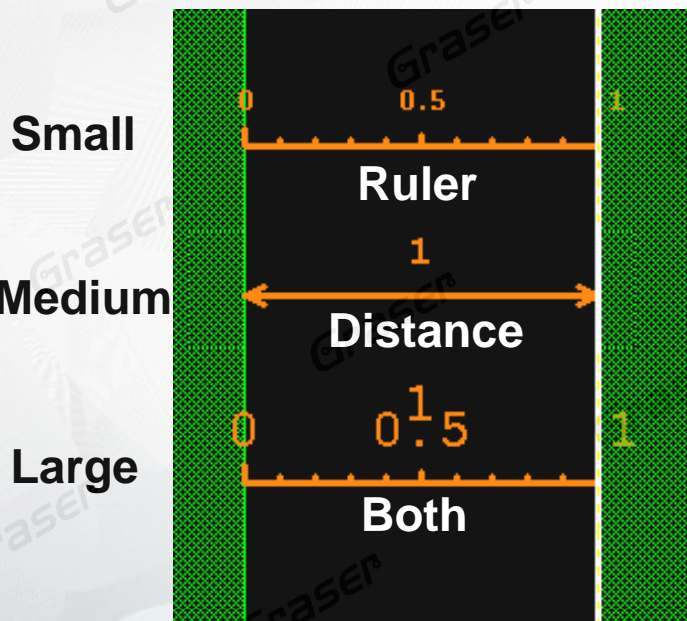
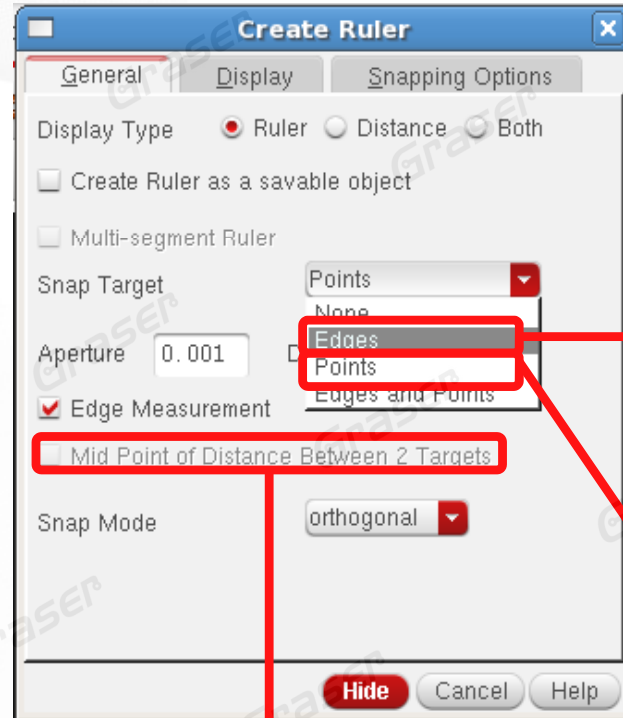
- Smart snapping
- Auto Tap wire
- Easy to change Layers



# Accelerate Manual-Editing

## Smart Ruler

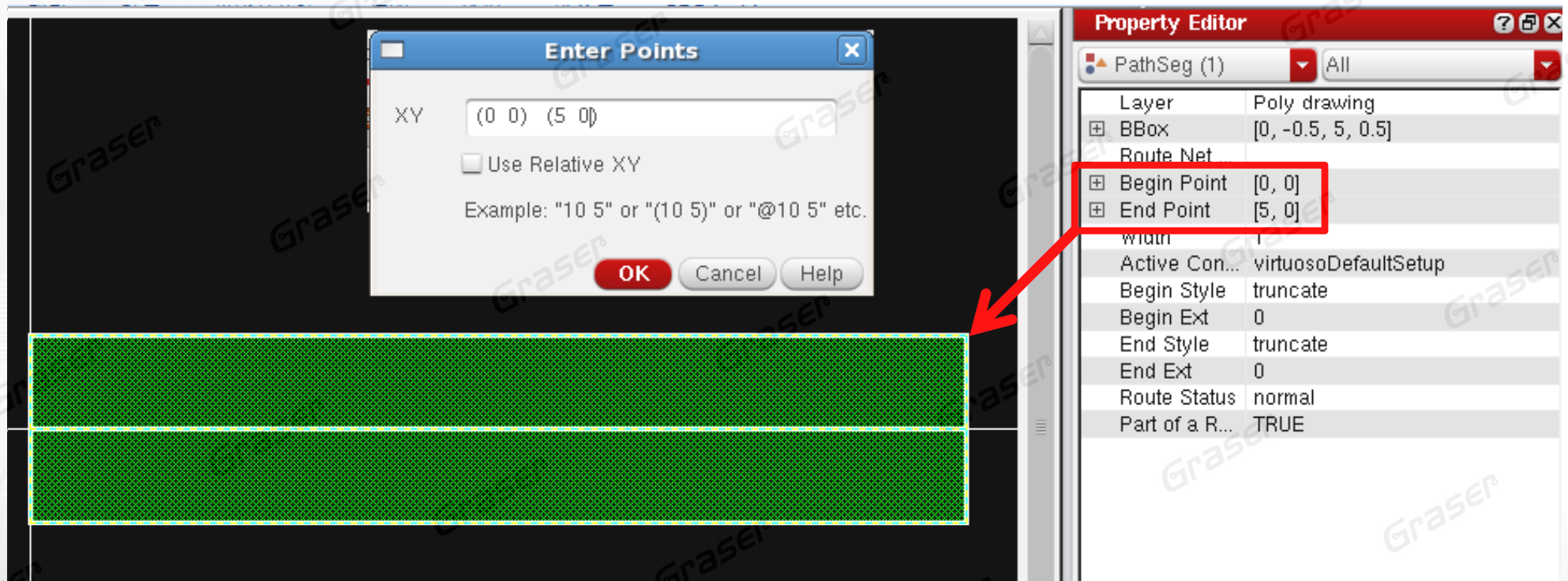
- Smart Snapping
- Multi-segments
- Customize general Ruler measurement and display type



# Accelerate Manual-Editing

## Enter Points

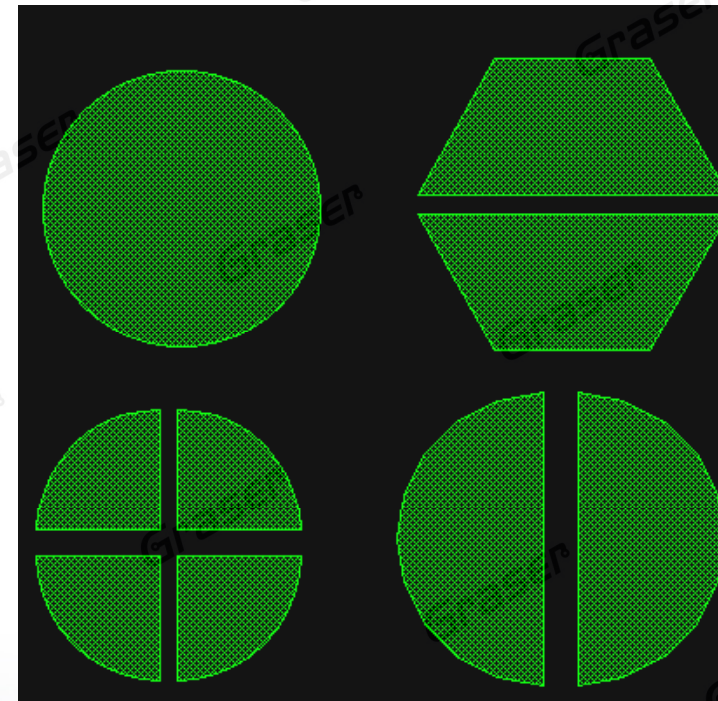
- Easy to specify points for any of the enter function based commands like Create, Move, Stretch, Copy command...



# Accelerate Manual-Editing

## Create Circle

- Support the Mode of “Draw” and “Click To Place”
- Multiple Shape Type

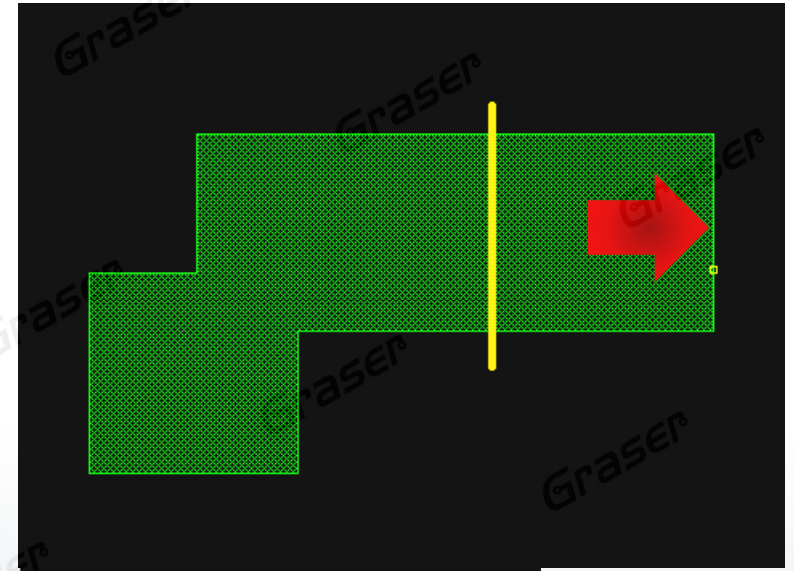
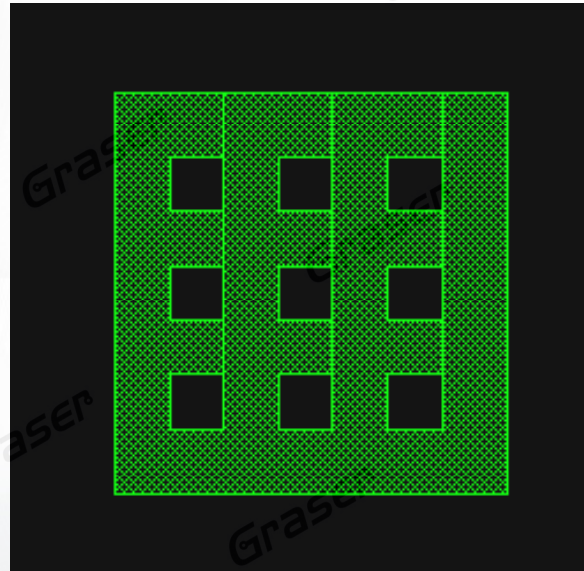
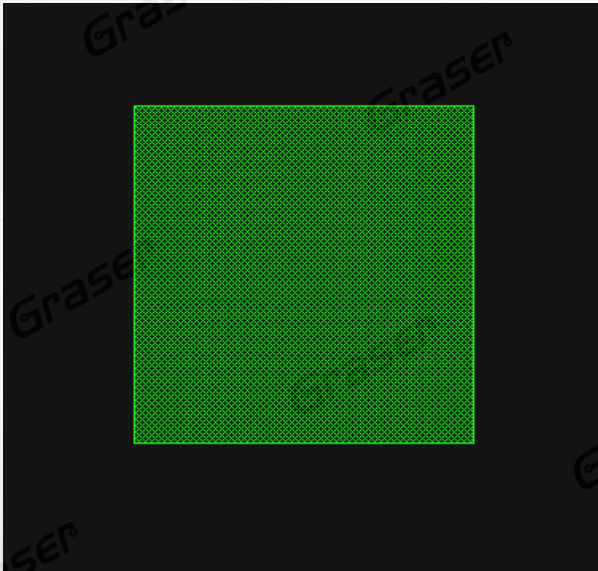




# Accelerate Manual-Editing

## Create Rectangle

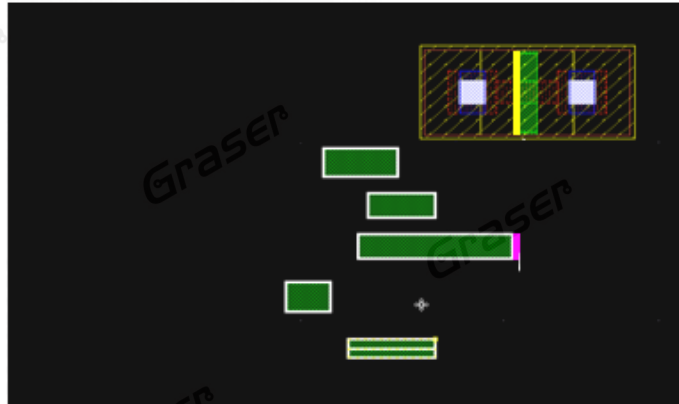
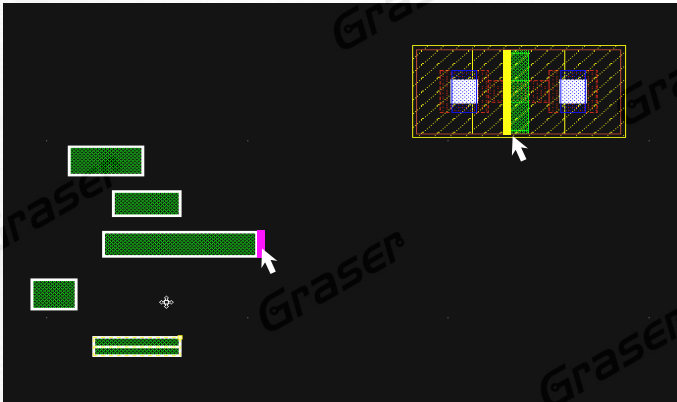
- Draw mode has the Smart Snapping
- Smart to create abutting rectangles to an existing shape
- Snapping can be restricted to Current Active Layer in Layer Palette
- Easy to customize the Dimension, spacing and Edge of Slot



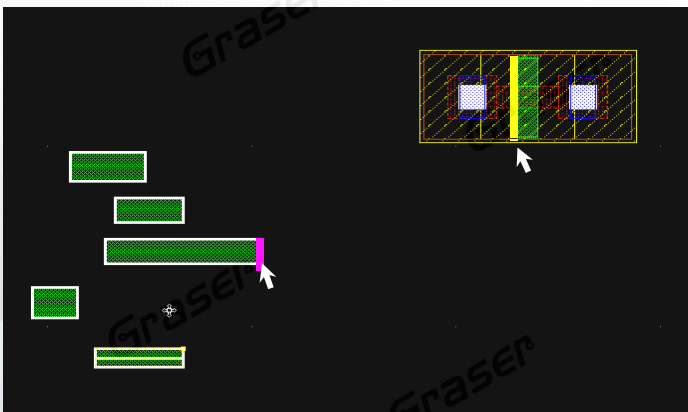
# Accelerate Manual-Editing

## Quick Align

- Quick Align allows users to align objects or instances
  - Full align is done in 1 click and 1 double click



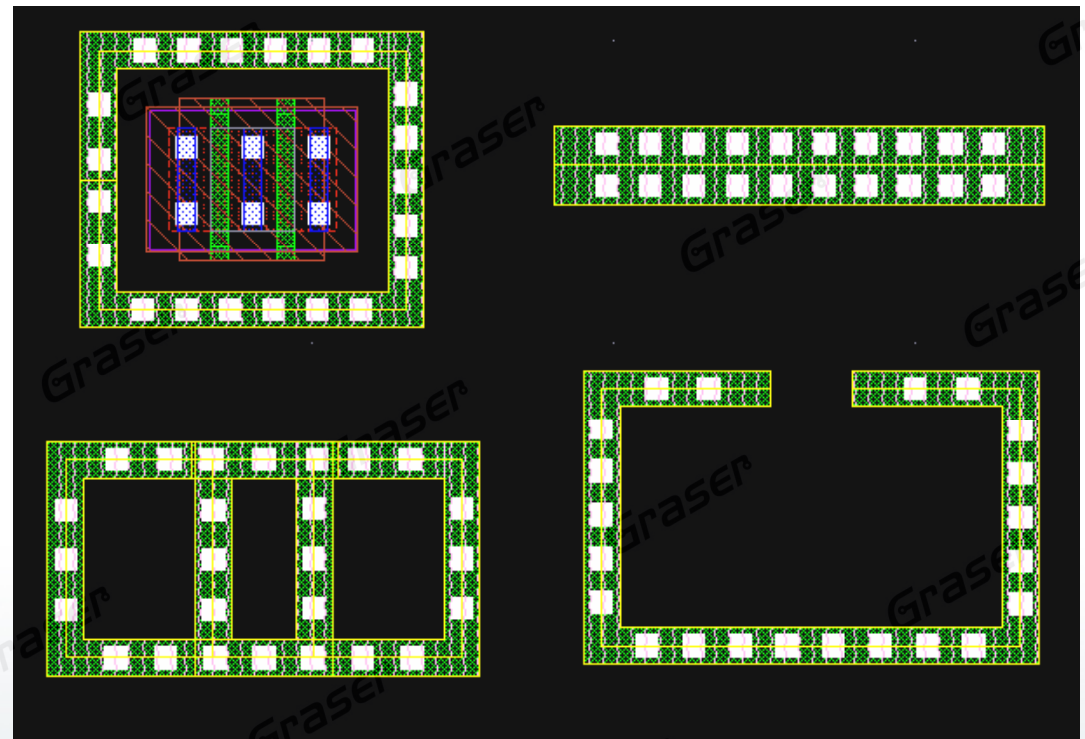
- Relative align is done in 2 clicks



# Accelerate Manual-Editing

## Create Guard Ring

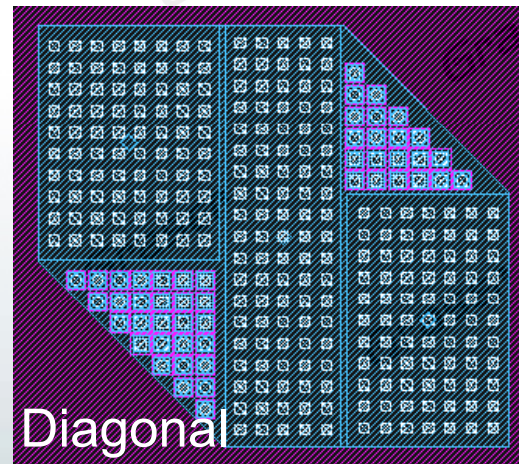
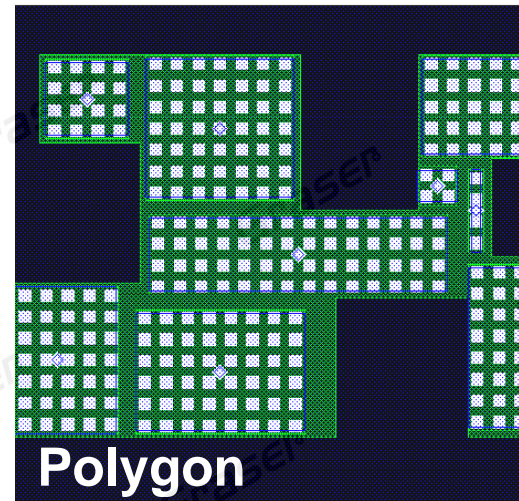
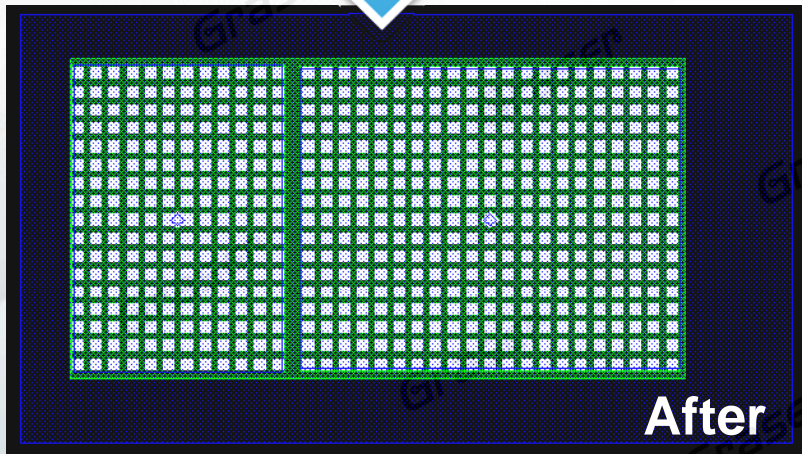
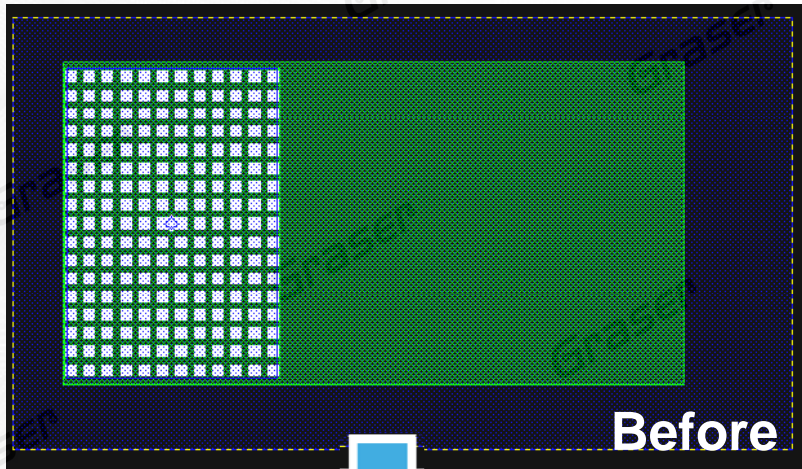
- Easy to customize the Guard Ring
- It can be created by four different ways: by drawing a path, rectangle, or polygon, or by using the wrap mode



# Accelerate Manual-Editing

## Create Via

- Supports polygonal shapes
- Autovia can fill a shape which already contains vias
- Supports 45 degree/diagonal shapes with below variables

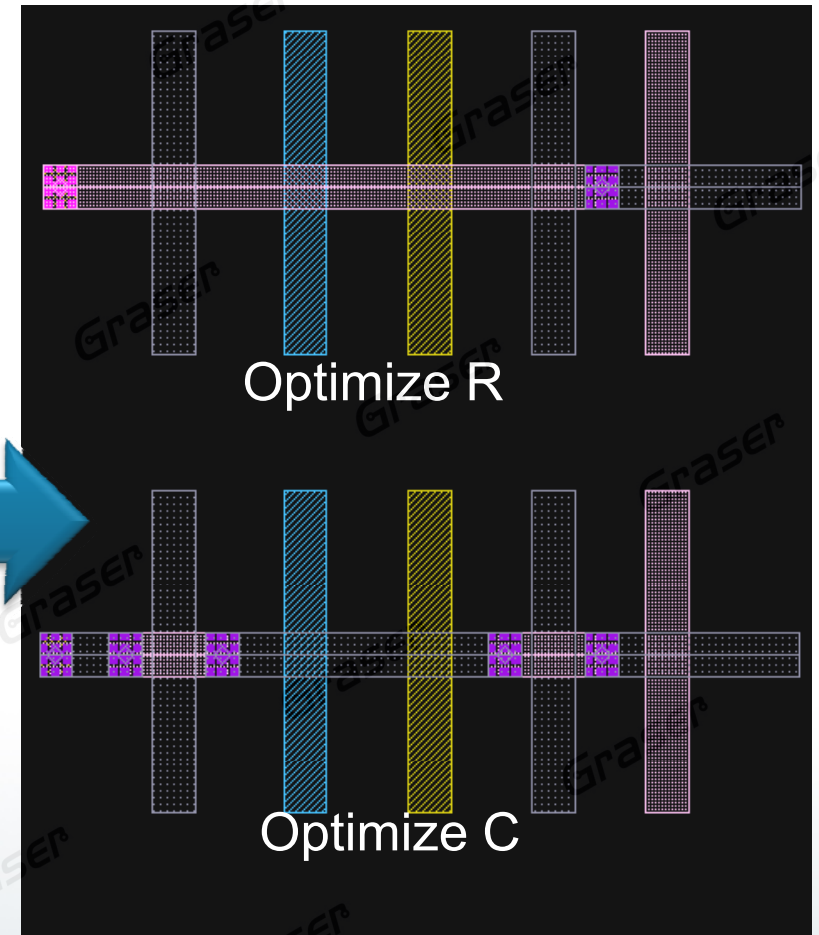
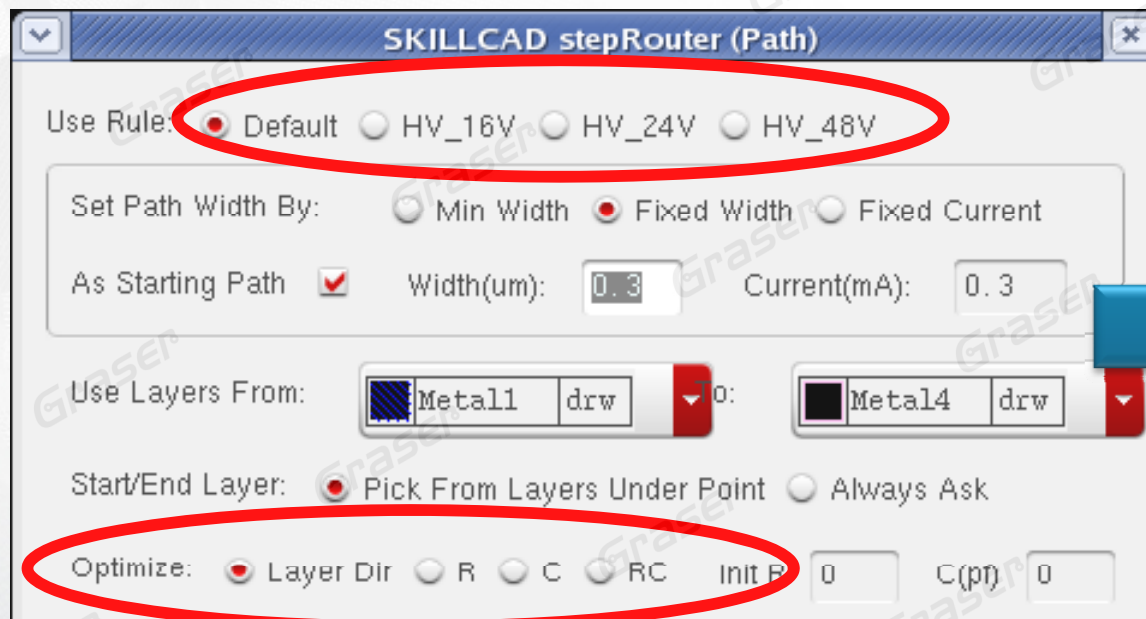


# Semi-Auto Interactive Routing

# Interactive Wire Editing

## Step Router

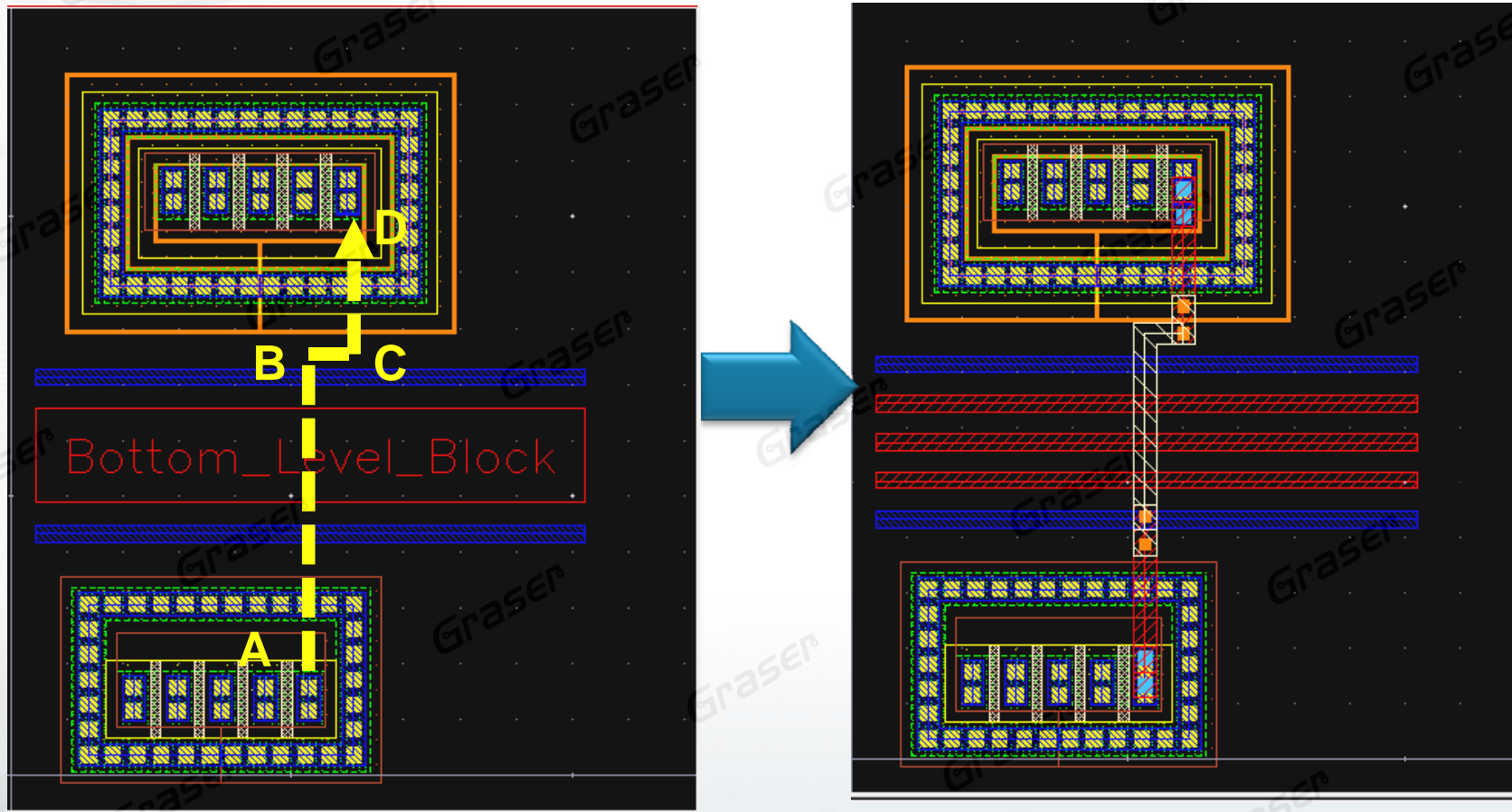
- Easy to choose rules
- Optimize auto-connections according to
  - Layer direction
  - Optimized RC effect



# Interactive Wire Editing

## Step Router

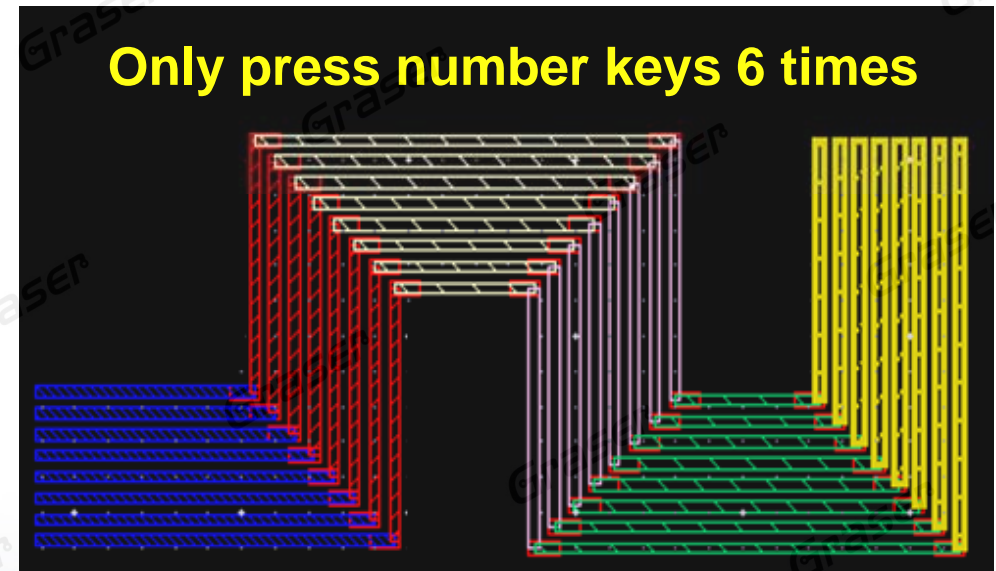
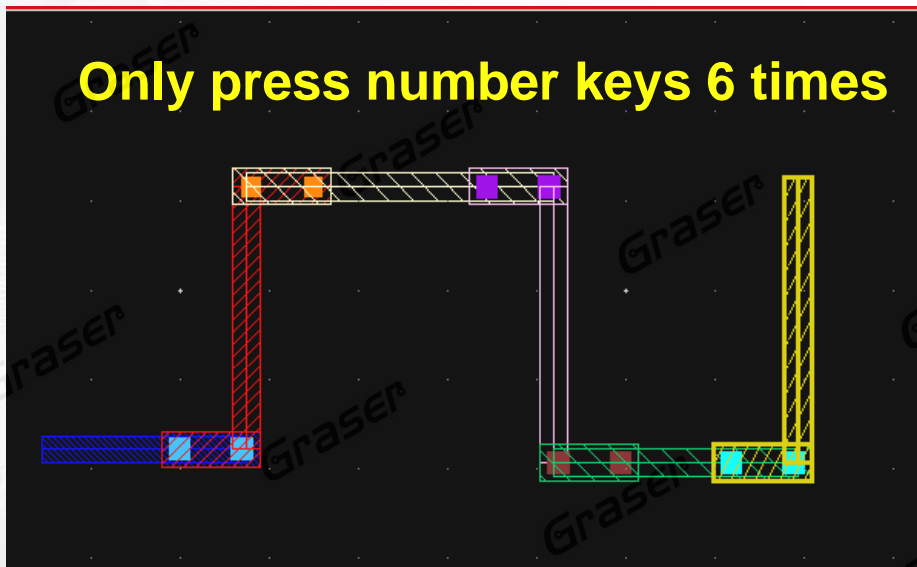
- Auto Tap the Width
- Auto change layer , snap pin & add vias



# Interactive Wire Editing

## Free Jumper

- Use number keys to change the layer what you want to route
- Add double via automatically
- Flexible via corner align style

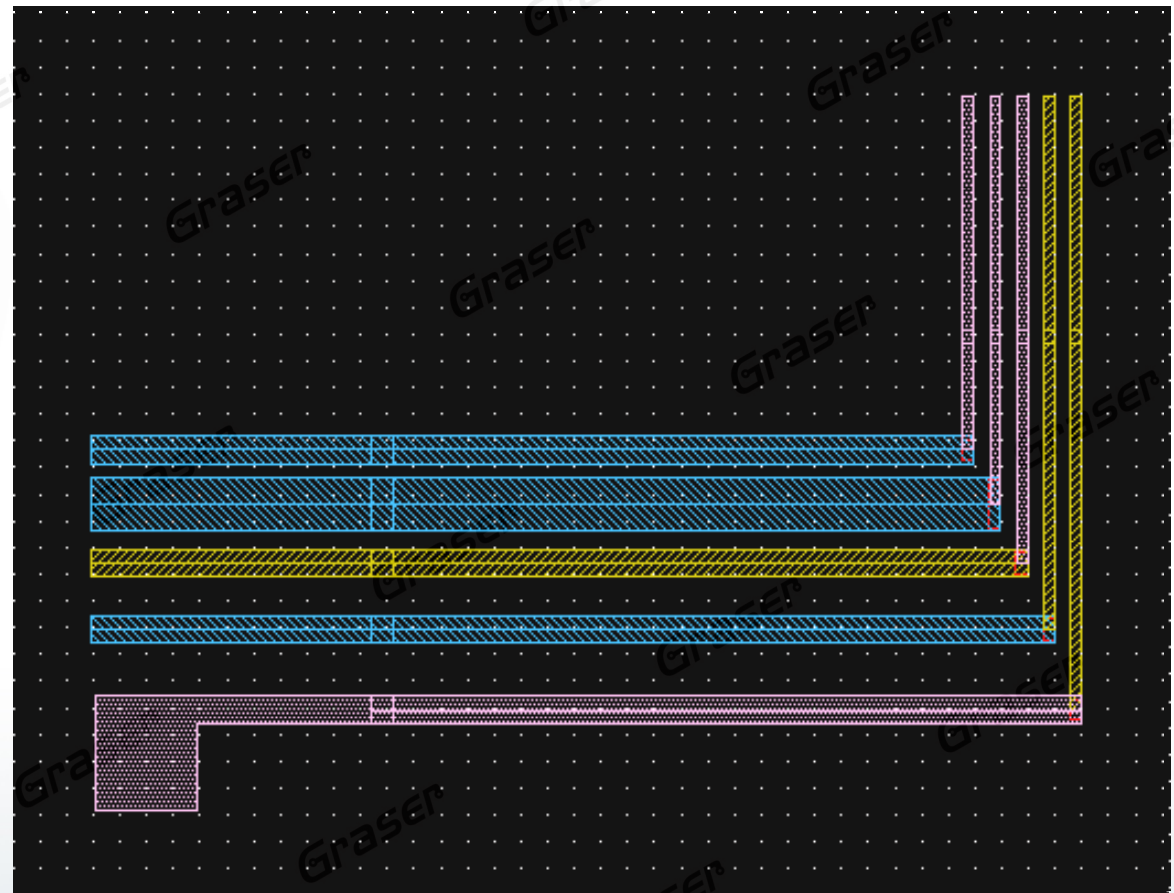
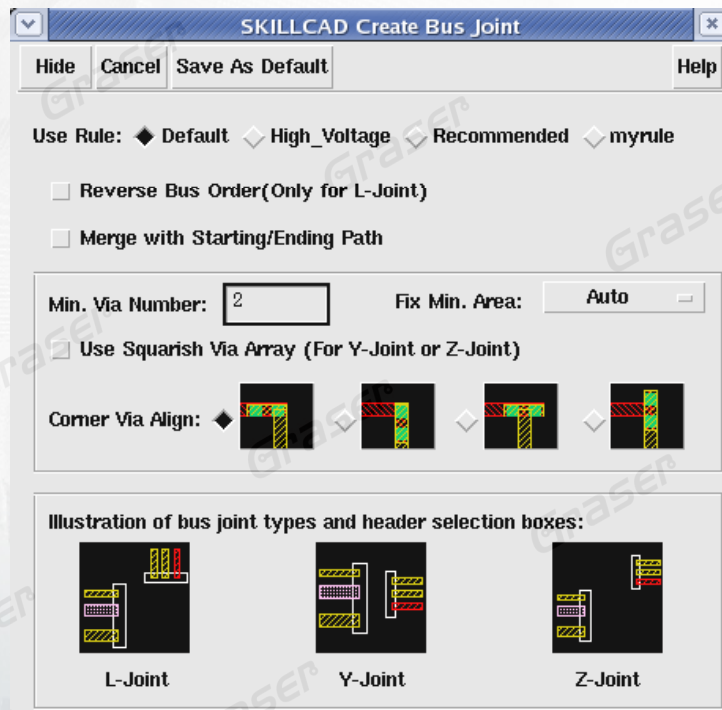




# Interactive Wire Editing

## Bus Joint

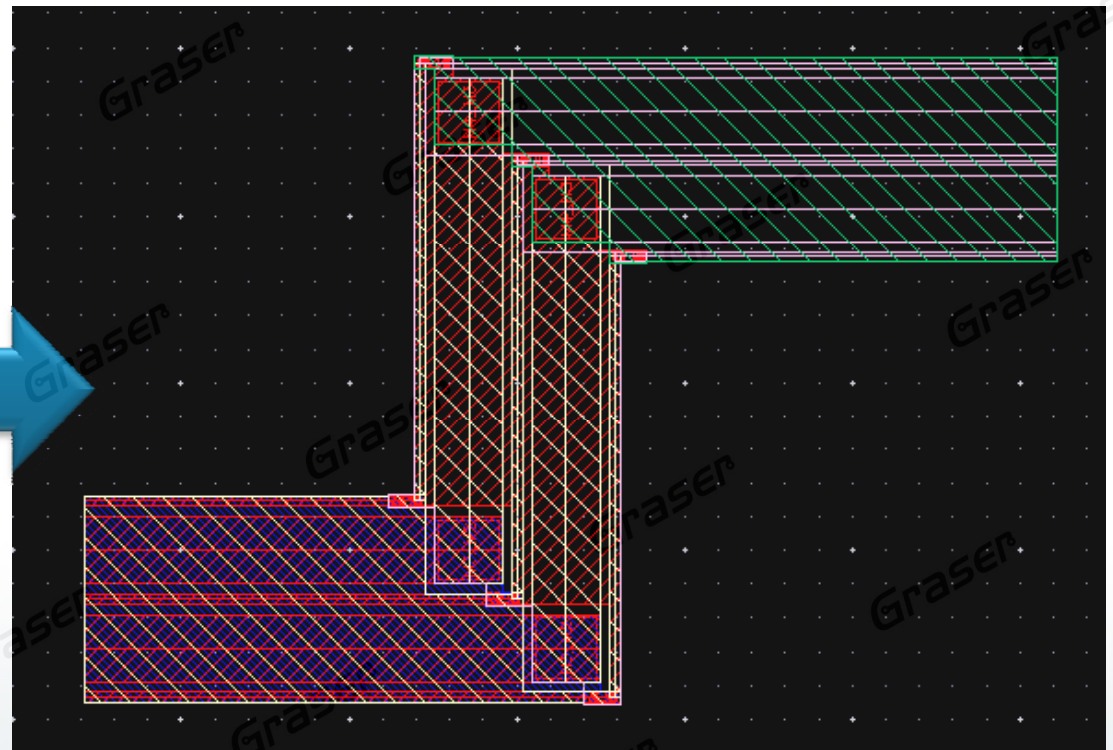
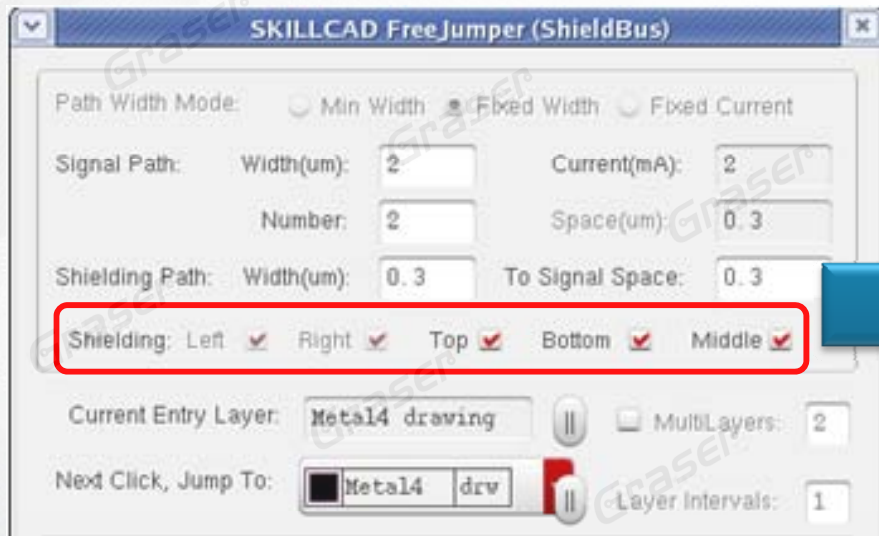
- Connected wire by user selection
- Auto change routing layers and add vias
- Easy to reverse order



# Interactive Wire Editing

## Shield Bus

- User-defined width / spacing of shielding path
- Number key to change connecting layers
- Auto-Via



# Auto Constrain & Generate From Source

# Constraint Driven & Generate From Source

## Layout Driven

- Constraint Driven
  - Make Circuit Designers closer to Layout Engineers
  - Common constraint environment to ensure correct-by-construction layout
  - Higher productivity, and fewer physical verification iterations
- Generate From Source (GFS)
  - Quickly generate layout device from schematic
  - Directly get Device type \ Parameter from schematic
  - Connectivity Highlight and Checking

# Constraint Driven Layout

## Constraints Setting in the Schematic

The screenshot displays the Cadence Schematic XL Editing interface for a schematic named "ether\_inv\_8X\_inline schematic". The interface includes a menu bar, a toolbar, a Navigator panel on the left, a Property Editor at the bottom left, and a Constraint Manager panel on the right. The main workspace shows a schematic diagram with four input signals (IN1, IN2, IN3, IN4) connected to a chain of inverters (labeled i0 through i7) and an OR gate (labeled i11). The output of the OR gate is labeled OUT1. The Navigator panel shows a tree view of the schematic components, with a red box highlighting the selected nets (net8, net10, net12, net14, net16). The Constraint Manager panel is open, showing a list of constraints. A red box highlights the "Routing" constraint, and a red arrow points to it. Another red box highlights the "Bus" constraint, and a red arrow points to it. A red box also highlights the "Editing" section of the Constraint Manager, with a red arrow pointing to it. A red box highlights the "Show:" section of the Constraint Manager, with a red arrow pointing to it. A red box highlights the "Diff Pair" constraint, with a red arrow pointing to it. A red box highlights the "Matched Length" constraint, with a red arrow pointing to it. A red box highlights the "Net Class" constraint, with a red arrow pointing to it. A red box highlights the "Net Priority" constraint, with a red arrow pointing to it. A red box highlights the "Process Rule Overrides" constraint, with a red arrow pointing to it. A red box highlights the "Shielding" constraint, with a red arrow pointing to it. A red box highlights the "Symmetry" constraint, with a red arrow pointing to it. A red box highlights the "Common Centroid" constraint, with a red arrow pointing to it. A red box highlights the "Matching (strength)" constraint, with a red arrow pointing to it. A red box highlights the "Rapid Analog Prototype" constraint, with a red arrow pointing to it. A red box highlights the "Rail" constraint, with a red arrow pointing to it. A red box highlights the "Max Capacitance" constraint, with a red arrow pointing to it. A red box highlights the "Alignment" constraint, with a red arrow pointing to it. A red box highlights the "Distance" constraint, with a red arrow pointing to it. A red box highlights the "Matched Orientation" constraint, with a red arrow pointing to it.

1. Select nets from the Navigator  
2. Apply appropriate constraints

# Constraint Driven Layout

## Setting Constraints in the Schematic

The screenshot displays the Cadence Schematic XL Editing interface for a schematic named "ether\_inv\_8X\_inline schematic". The interface includes a menu bar (Launch, File, Edit, View, Create, Check, Options, Migrate, Window, Help), a toolbar, and a Navigator panel on the left. The Navigator panel shows a hierarchy of components, including a 4-bit bus component named "(or4\_1x\_hv) i11". The main schematic area shows a circuit with four input signals (IN1, IN2, IN3, IN4) connected to a 4-bit bus. The bus is connected to a 4-bit OR gate (i11) which outputs OUT1. The bus is highlighted in yellow, and a red text box at the bottom of the schematic area states "Bus constraints are now applied". The Constraint Manager panel on the right shows the "inv\_8X\_inline (1)" constraint applied to the bus, with a list of nets (net12, net10, net8, net14) associated with it. The Property Editor panel at the bottom shows the constraint details, including the name "Constr\_0", owner "ether\_inv\_8X\_inline...", and status "not checked".

**Bus constraints are now applied**

Name	Constr_0
Owner	ether_inv_8X_inline...
Enabled	true
Status	not checked
Notes	
Default Gro...	Empty
Within Group	Empty
Group to O...	Empty
hierarchica...	local

# Constraint Driven Layout

## Automatic Constraint Generators

- Single **Rapid Analog Prototype(RAP)** Category in the Circuit Prospector containing all the finders/generators required to automatically constrain a design with just a few mouse clicks

Run all respective actions for the Current Cellview  
Run all respective actions for Each Sub-Cell

**Choose Finders**

- MOS Cascoded Current Mirror
- MOS Cascoded Current Mirror2
- MOS Transmission Gate
- MOS Differential Pair
- MOS Common Gate
- MOS Parallel
- MOS Active Load
- MOS Inverter
- MOS Cross Coupled Pair
- Symmetric Instance Pairs - By Pre-selection
- Symmetric Instance Pairs - By Connectivity
- Self Symmetric Instances - By Connectivity
- Placement Path
- Passive Arrays
- Active Same Cell large mfactor
- Capacitor Cluster
- Vertical Orientation
- Negative Supply
- Positive Supply
- Enforce Precedence

**Circuit Prospector**

Category: Rapid Analog Prototype

Search for: ALL

Within: All objects

Groups (9)	Finder
<input type="checkbox"/> (3) /mp0 /mp1 /mp2	Vertical Orientation
<input type="checkbox"/> (3) /mn1 /mn2 /mn0	Vertical Orientation
<input type="checkbox"/> (1) /VSS!	Negative Supply
<input type="checkbox"/> (1) /VDD!	Positive Supply
<input type="checkbox"/> (1) /VDD:2	Top Pins (Alignment)
<input type="checkbox"/> (1) /VSS:1	Bottom Pins (Alignment)
<input type="checkbox"/> (2) /A:4 /B:3	Left Pins (Alignment)
<input type="checkbox"/> (1) /Y:5	Right Pins (Alignment)
<input type="checkbox"/> (0) /mp1 /mp0 /mp2 /m	Enforce Precedence

**Constraint Manager**

Editing: constraint (modified)

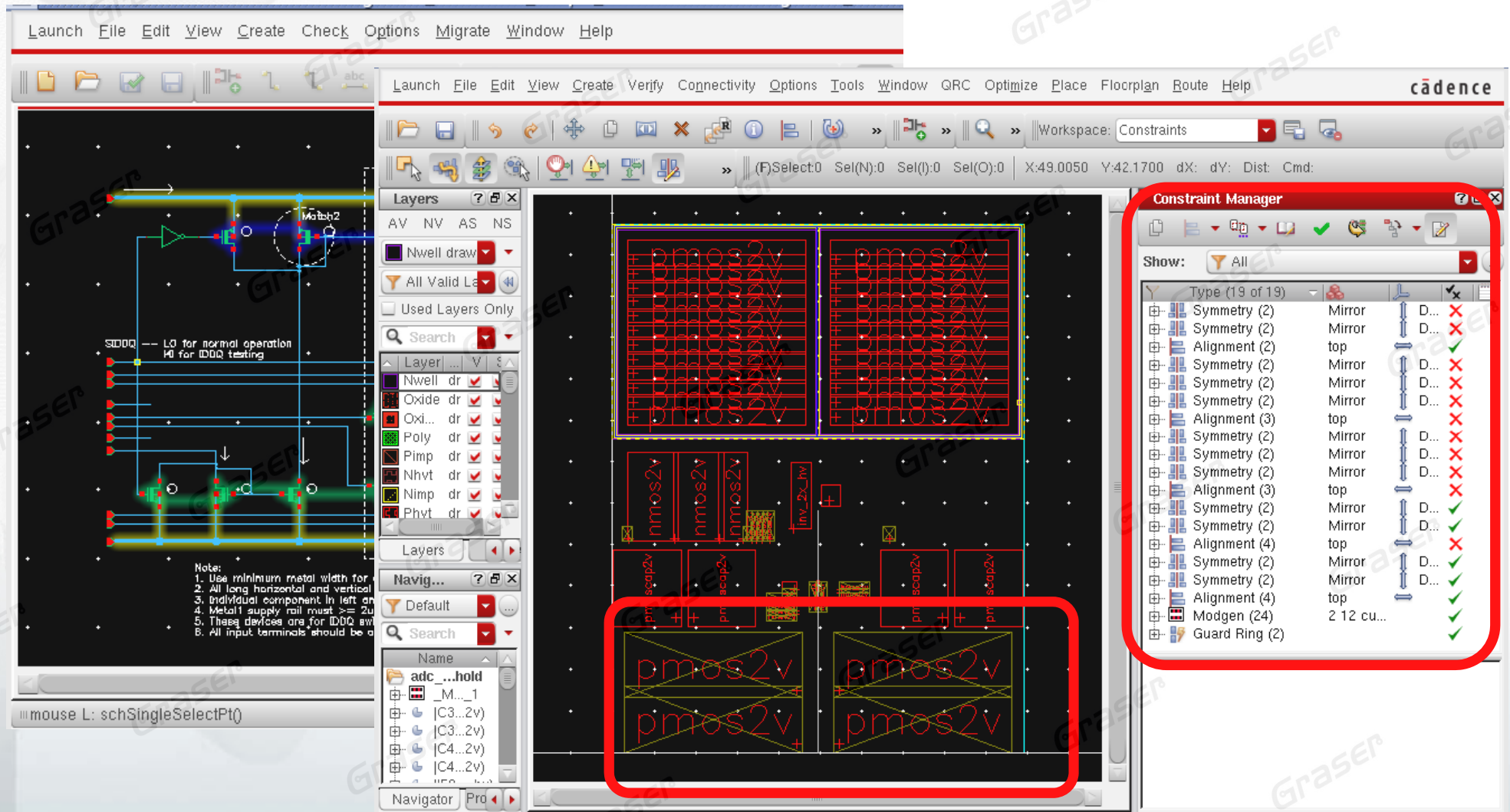
Show: All

Type (5)	constr
AND2X2 (5)	R0, MY
Orientation (3)	R0, MY
Orientation (3)	R0, MY
Net Priority (1)	1
VSS!	
Process Rule Over...	Empty I
Rail (2)	horizon

# Constraint Driven Layout

## Constraint Manager

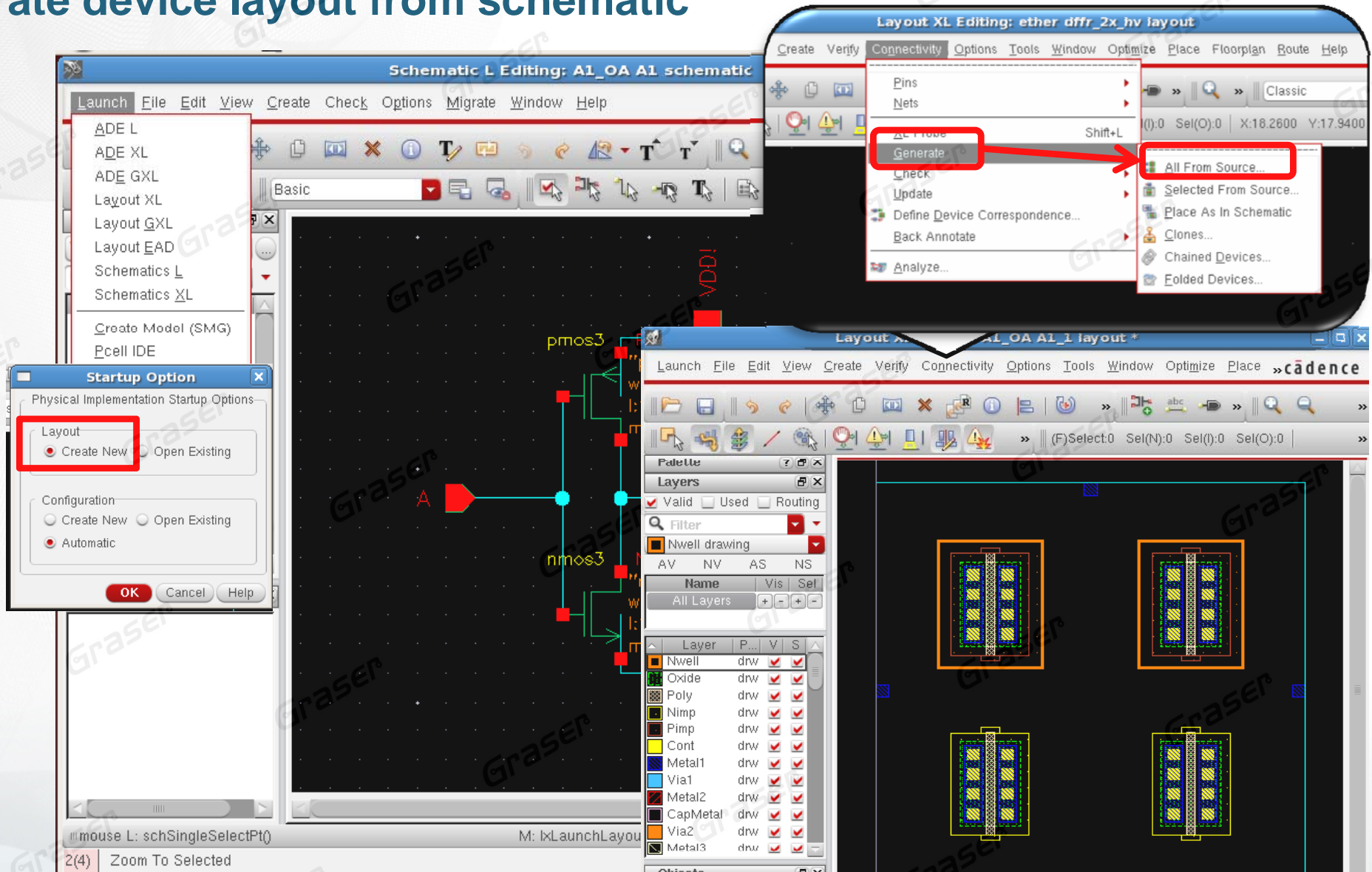
- Common constraint environment to ensure correct-by-construction layout





# Generate From Source

## Generate device layout from schematic



- Quickly generate layout device from schematic

# Generate From Source

## Generate device layout from schematic

- Cross probing
- Connectivity highlight and checking
- Show incomplete nets and check For Opens/Short

The image displays four screenshots from the Cadence software interface, illustrating the process of generating a device layout from a schematic. The top-left screenshot shows the Schematic XL Editing window for 'OA\_TEST AND2X1 schematic'. The top-right screenshot shows the Layout XL Editing window for 'OA\_TEST AND2X1 layout'. The bottom-left screenshot shows the Schematic XL Editing window for 'OA\_TEST AND2X1 schematic' with a different circuit diagram. The bottom-right screenshot shows the Layout XL Editing window for 'OA\_TEST AND2X1 layout' with a different layout view. A circular inset on the right shows a list of nets and their status, with some nets highlighted in red.

Name	XL Status
(...n1) conn...	
(...n2) conn...rence	
(...p0) OK	
(...p1) OK	
(...p2) OK	
A	opens(2)
B	opens(2)
n0	opens(4)
n...7	opens(1)
VDDI	opens(6)
VSSI	opens(2)
Y	opens(2)
B:B	OK

# Summary

- Integration with Virtuoso front-to-back custom & analog solution
- Virtuoso is New, fast, easy-to-learn, easy-to-use for design
- Virtuoso Schematic Editor speeds up the largest and most complex custom designs
- Virtuoso ADE is the direct access to MMSIM to realize your silicon
- Virtuoso Layout Suite speeds custom designs to the market
  - Quick placement, routing and editing
  - Reduce DRC and LVS errors
  - Enhance the productivity and efficiency of layout
- Reduces a risk by maintaining design intent between design specification and implementation with unified common constraint environment