PDS Impact for DDR3-1600 Low Cost Design

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Agenda

- Current DDR3 design trend and challenge
- Timing and Signal Integrity Impacted by PDS
- PDS design challenge
- Co-simulation for System Level PDS
- Summary

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- Power aware timing and signal integrity 
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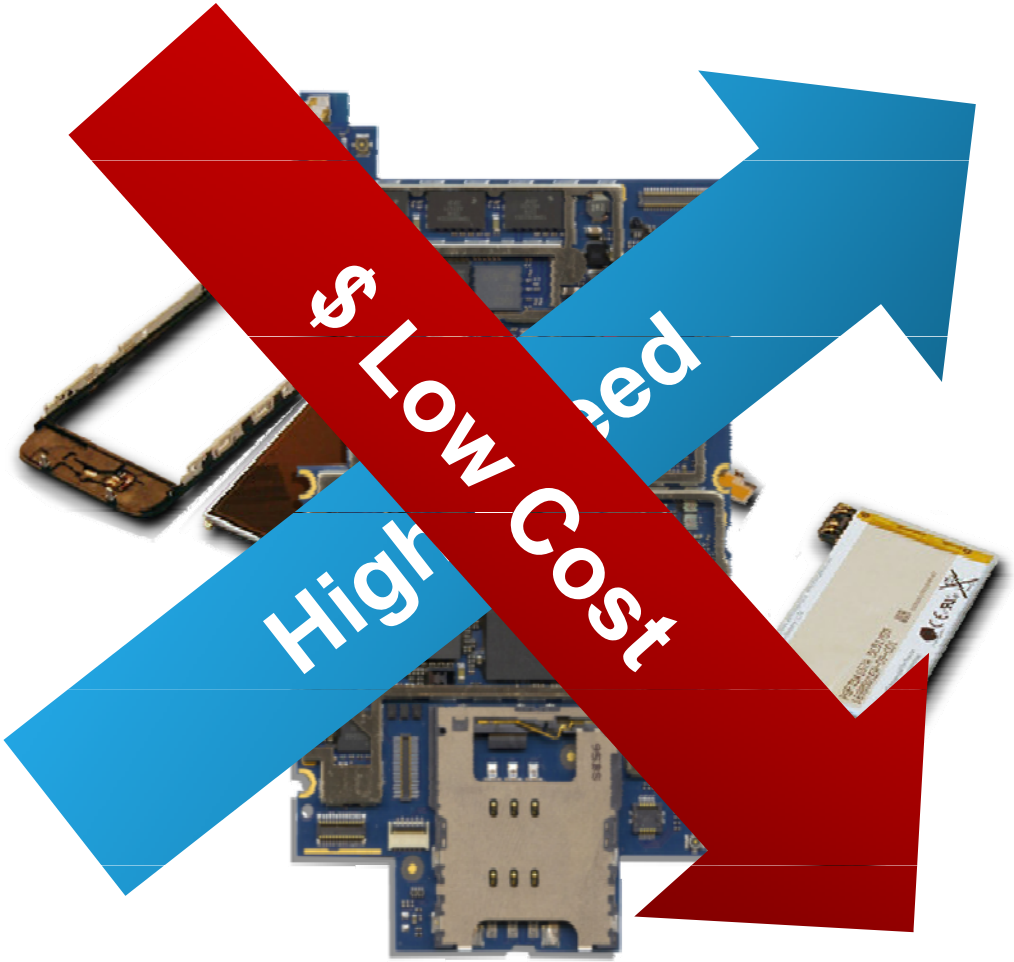
Low Cost and High Performance



- DDR3 & LPDDR3 are dominant in current consumer market
- Low-cost package like wirebond BGA, CSP, LQFP
- Fewer layers of PCB, even 2 layers PCB is adopted

It is challenging……

- Problem we will meet:
  - High density route and leads to serious crosstalk
  - Imperfect reference plane that cause signal with bad return path discontinuity (RPD)
  - Wirebond/lead inductance that causes larger insertion loss of signal at high frequency
  - Higher current loop inductance for P/G pins and leads to larger impedance
  - Traditional equal length requirement is no longer valid
  - Timing margin is power/noise aware

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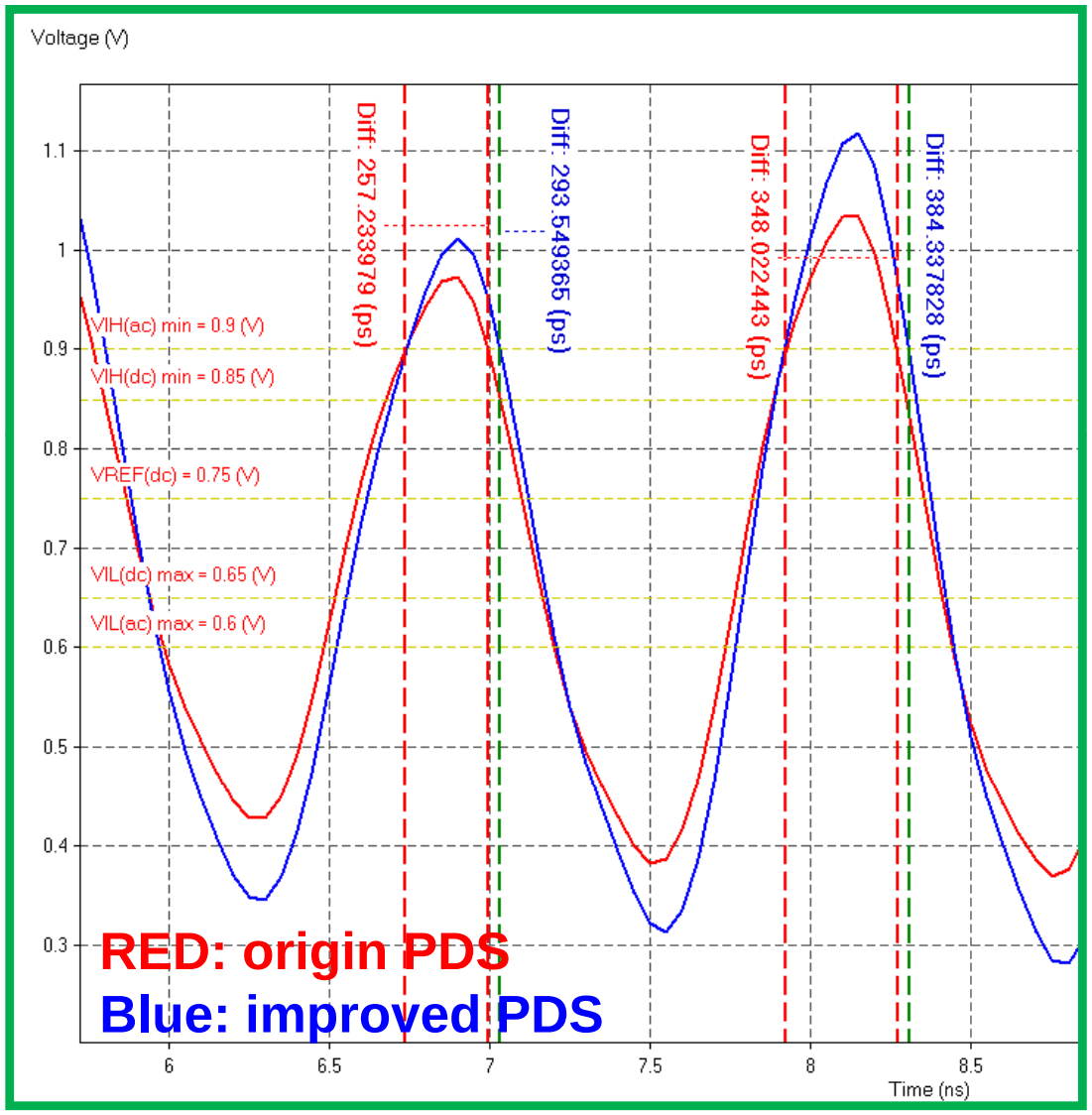
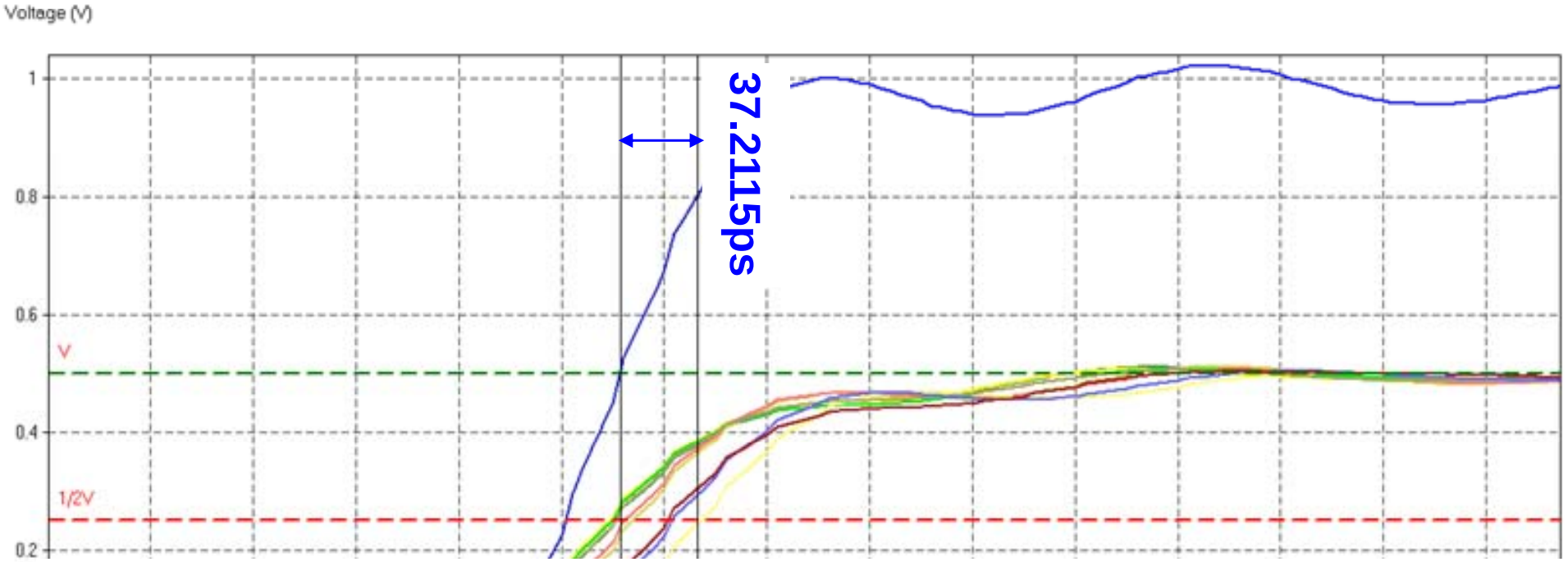
Timing and Signal integrity impacted by PDS



- What did we see from the signal measurement?
  - Signal rise and fall change to faster slew rate
  - Signal pulse width becomes wider (high time and low time)
  - Signal amplitude becomes larger
- Does **PDS** impact a lots?
- If your design has bad **PDS** and how to improve it?

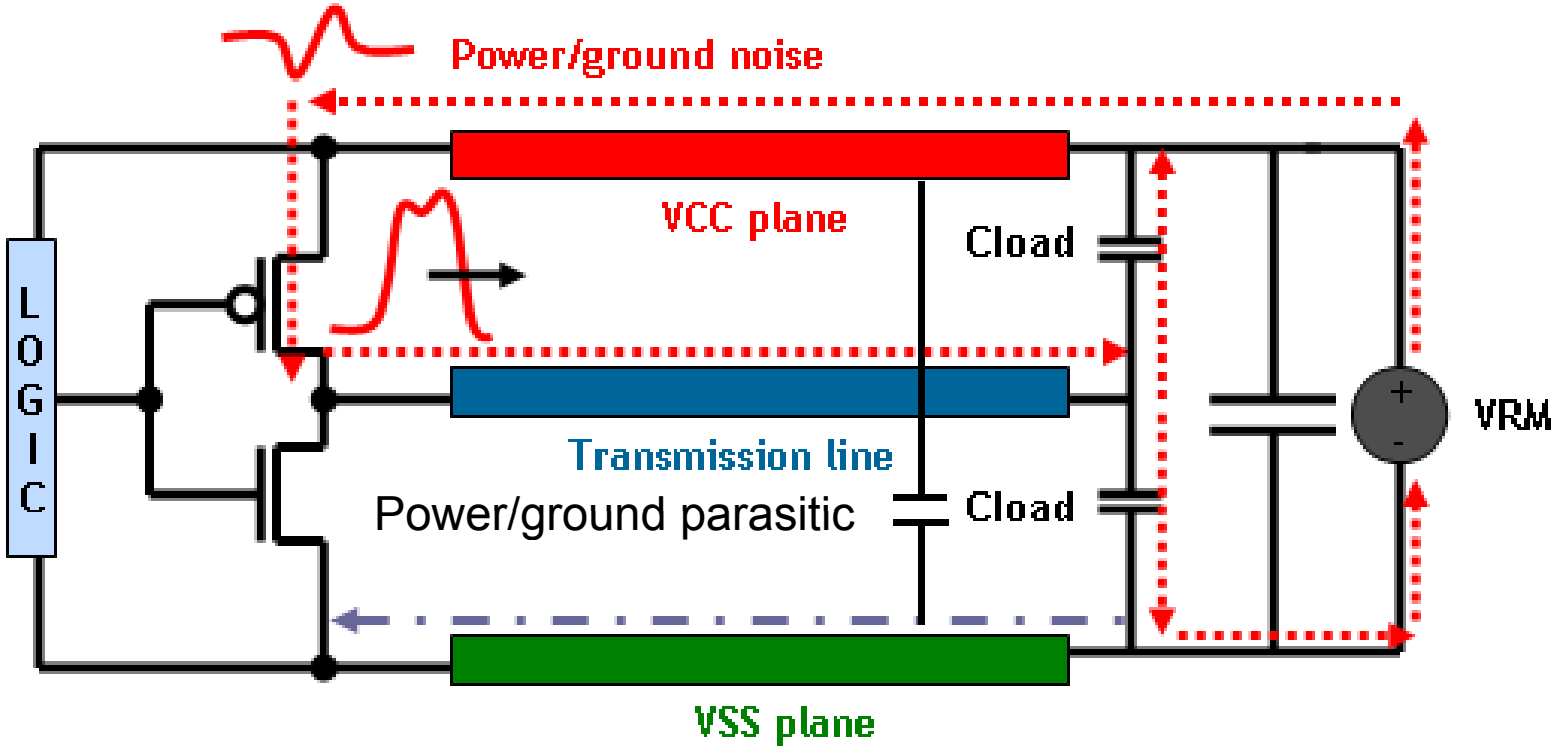
Timing and Signal Integrity Impacted by PDS



Bus Type: Data, Edge Type: BothEdges, Bus Group: data1, Timing Ref: LDQS-LDQSB

Rx Signal			Tx Buffer Output			MeasDelay (ps)	BufferDelay (ps)	Max InterconnectDelay (ps)	|Max| InterconnectSkew (ps)	Max StrobeInterconnectSkew (ps)
Waveform	Pin	IO Model	Signal	Pin	IO Model					
LDM	E7	DM_ODT_60	dm0	33	se_drv15_odtoff	1579.98	1189.73	390.253	100.191	NA
LDQ0	E3	DQ_ODT_60	dq0	1	se_drv15_odtoff	1588.09	1189.73	398.365	108.303	NA
LDQ1	F7	DQ_ODT_60	dq1	2	se_drv15_odtoff	1585.25	1189.73	395.523	105.461	NA
LDQ2	F2	DQ_ODT_60	dq2	3	se_drv15_odtoff	1593.3	1189.73	403.573	113.511	NA
LDQ3	F8	DQ_ODT_60	dq3	4	se_drv15_odtoff	1590.86	1189.73	401.131	111.069	NA
LDQ4	H3	DQ_ODT_60	dq4	5	se_drv15_odtoff	1625.74	1189.73	**436.01**	**145.948**	NA
LDQ5	H8	DQ_ODT_60	dq5	6	se_drv15_odtoff	1596.85	1189.73	407.116	117.054	NA
LDQ6	G2	DQ_ODT_60	dq6	7	se_drv15_odtoff	1611.99	1189.73	422.265	132.203	NA
LDQ7	H7	DQ_ODT_60	dq7	8	se_drv15_odtoff	1625.69	1189.73	435.963	145.901	NA
LDQS-LDQSB	F3, G3	DQ_ODT_60	dqs0p, dqs0n	37, 38	se_drv15_odtoff	1444.77	1154.71	290.062	NA	**0**

Timing and Signal Integrity Impacted by PDS



- Signal output from I/O buffer is affected by PDS impedance.
- Current demand by I/O buffer is limited if impedance of PDS is large.
- Smaller I/O current (sink from PDS) that causes signal amplitude becoming smaller (slow charge/discharge to the load).
- For such high switching rate I/Os, try to stay system PDS in low impedance is the best policy.

Timing and Signal Integrity Impacted by PDS

- Physical equal length can’t guarantee zero skew
- Electrical timing skew without buffer still can’t reflect timing skew in the real world
- Crosstalk among signals, large PDS noise (SSO noise) and strong coupling among signals and P/G planes that causes timing push-out/pull-in and small high/low time of the signal pulse.
- Even 1/4T timing offset at controller is still likely to get failed timing at memory.
- Strobe signals need to be isolated from DQs and keep least return path for reducing coupling with P/G.

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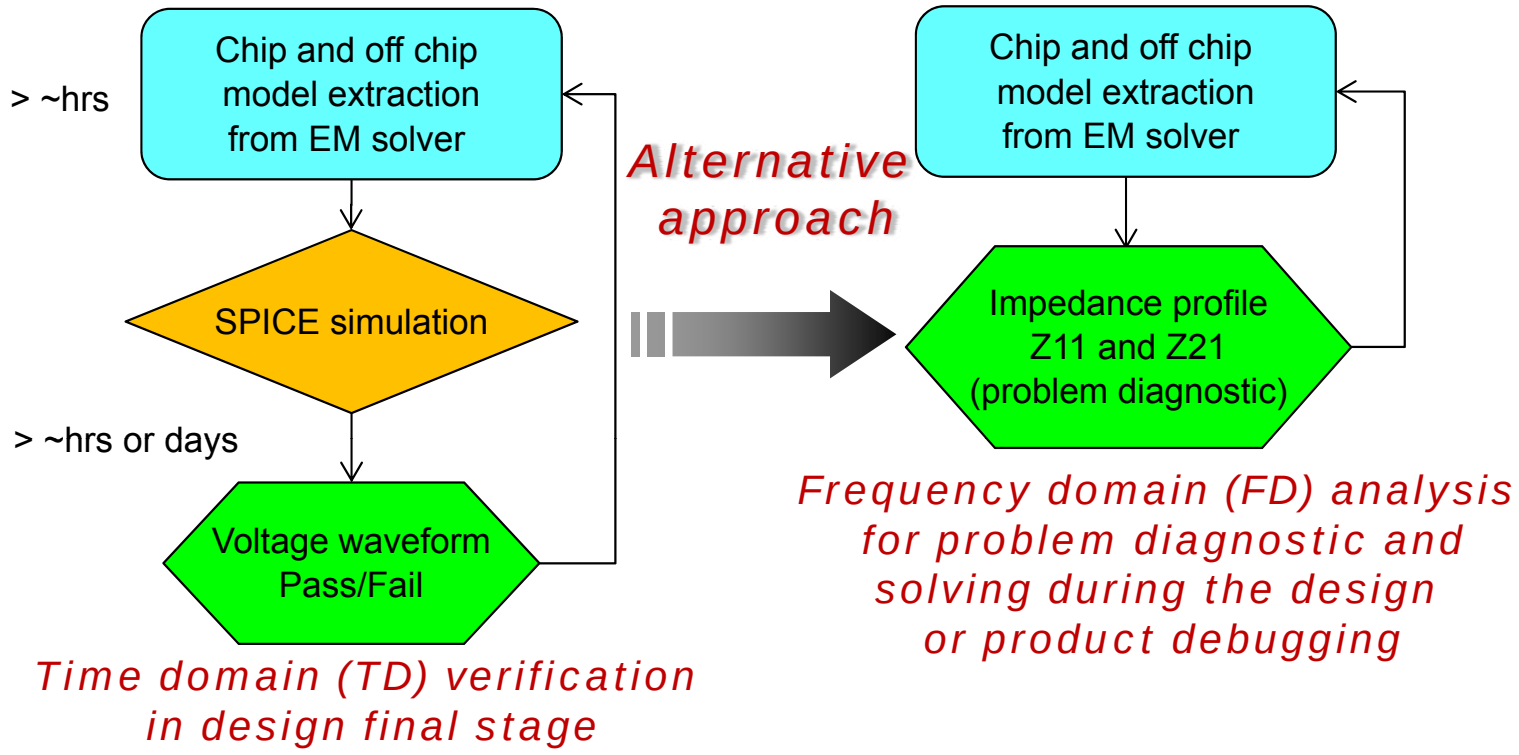
- **PDS Design Challenge**
- Solutions for system Level PDS Co-simulation
- Summary

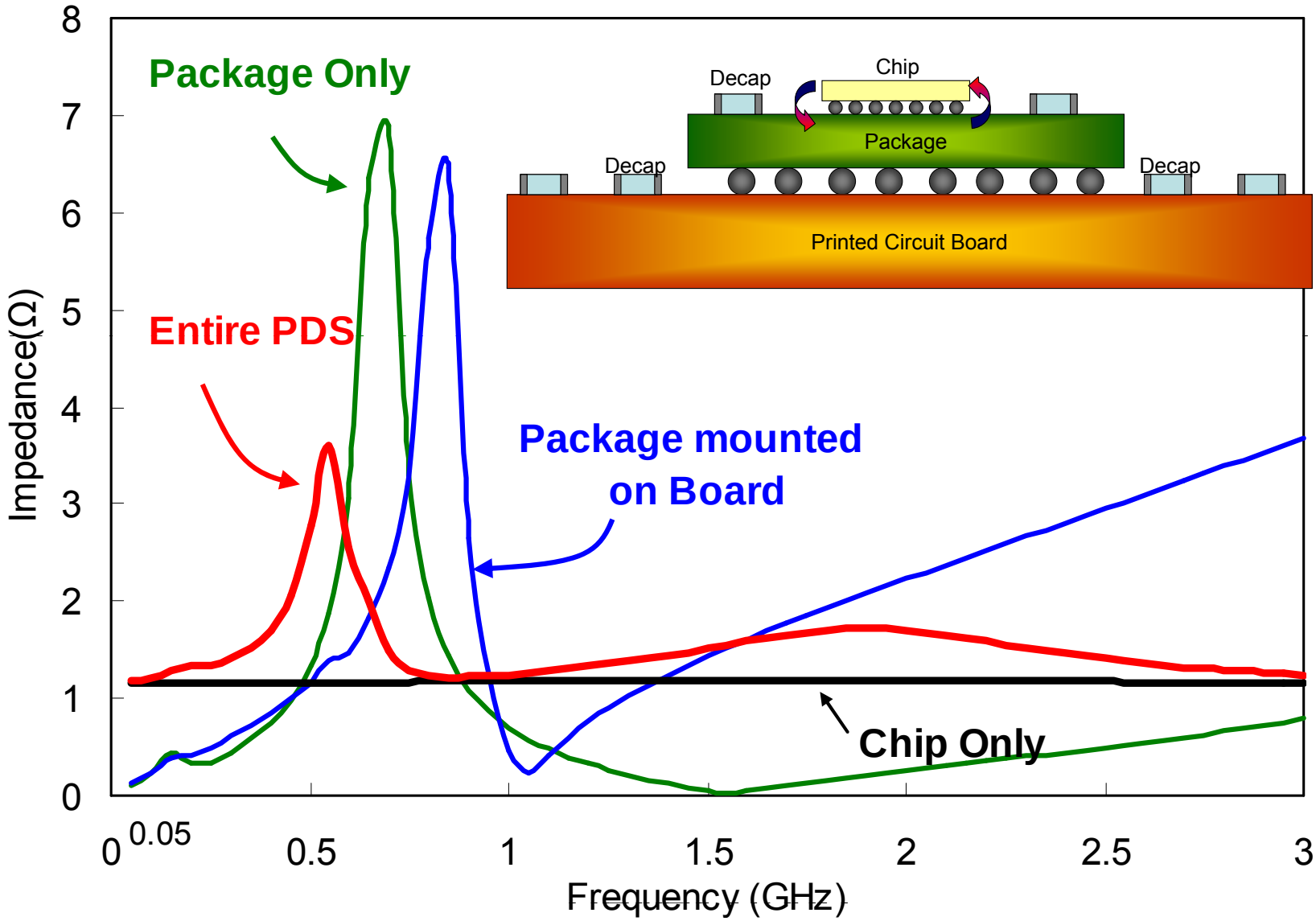
PDS Design Challenge



- Traditional TD analysis is time consuming and hard to diagnose the root caused that make PDS failed
- FD analysis will reveal the characteristic of PDS easily and reveal the physics behind that make PDS failed

PDS Design Challenge

Behavior of input impedance in system level



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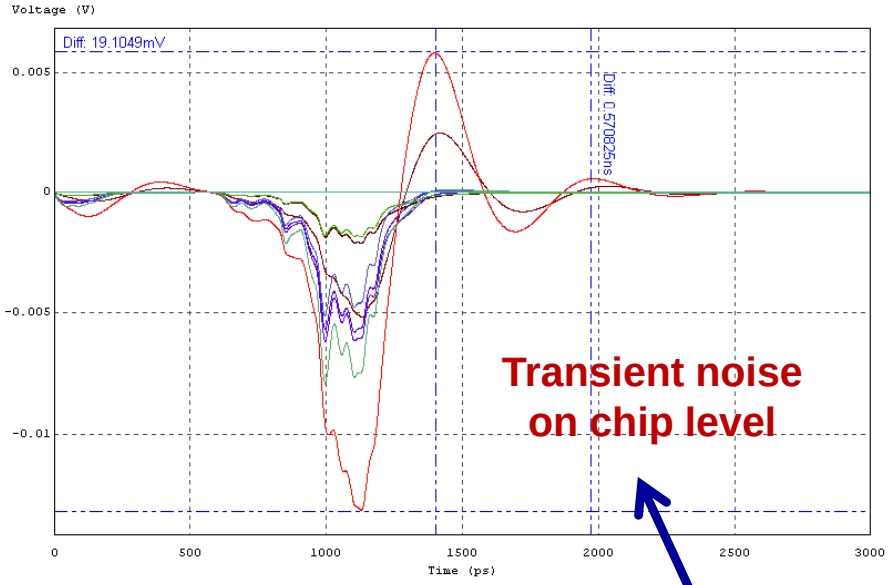
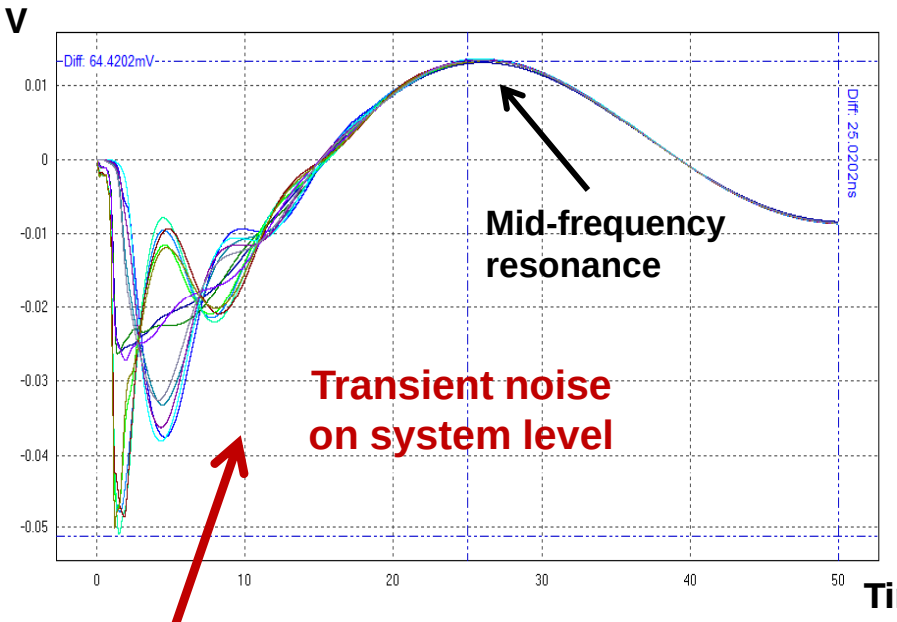
PDS Design Challenge
Mid-frequency resonance

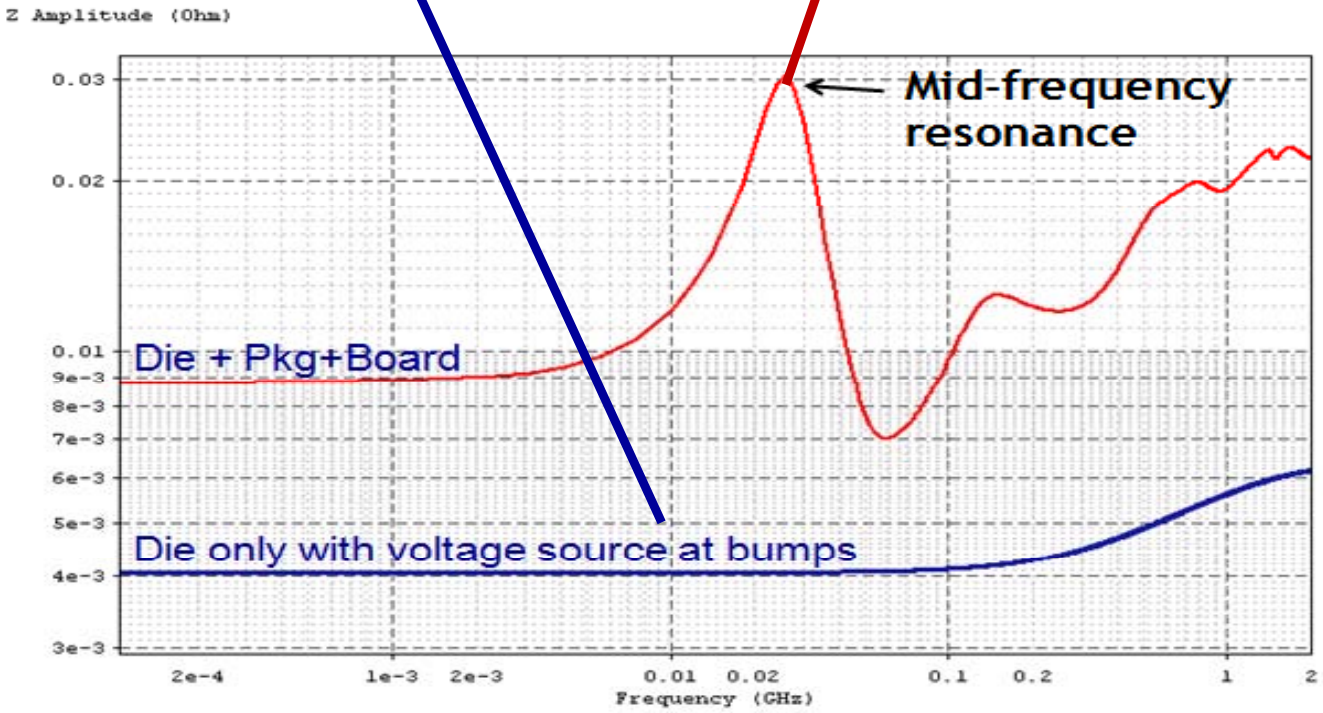


Transient noise on chip level



Mid-frequency resonance

Transient noise on system level



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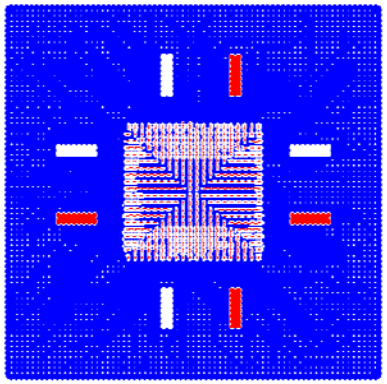
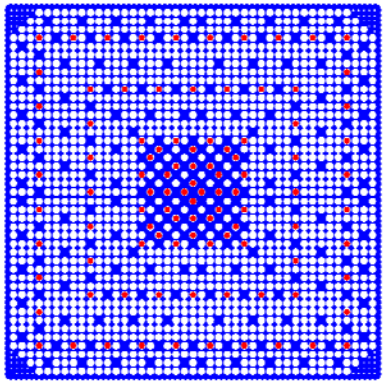
PDS Design Challenge

400 VDD bumps
2007 VSS bumps

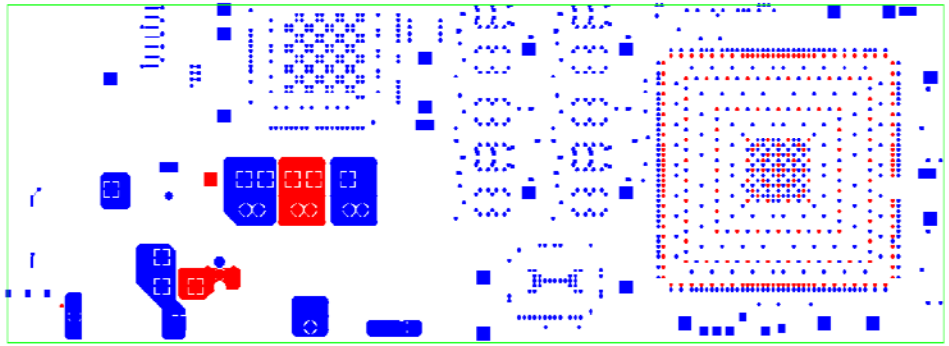


Top

Bottom



98 VDD balls
227 VSS balls

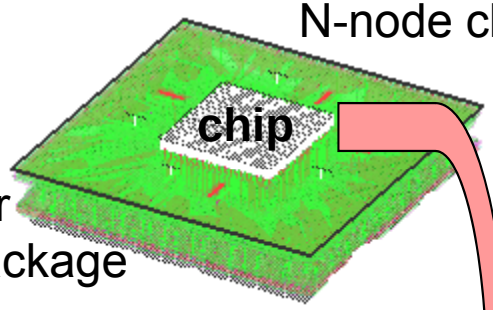


(1)Chip PDS models can vary from 2-node to N-nodes, where N is the number of physical pins.

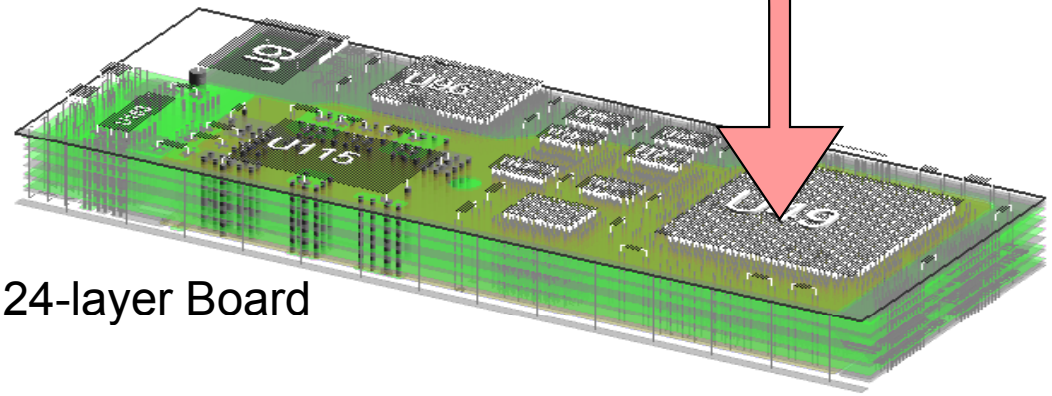
(2)How to generate model from 2 to N nodes for accounting PDS noise at different frequency bandwidth with executable model size?

(3)It needs a platform that can cascade all circuit blocks automatically to complete such complex system level simulation

N-node chip model



10-layer
BGA package



24-layer Board

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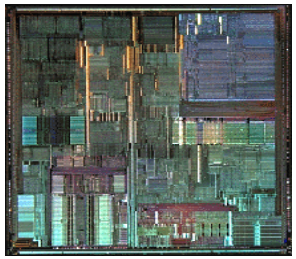
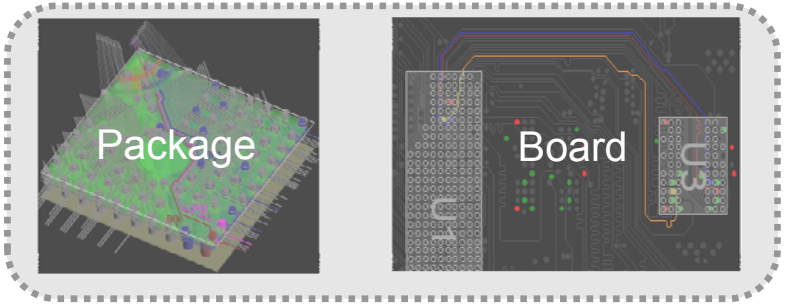
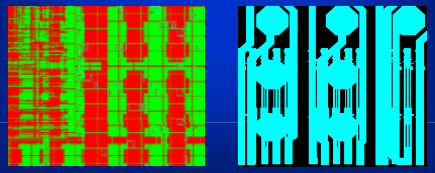
Co-simulation for system Level PDS





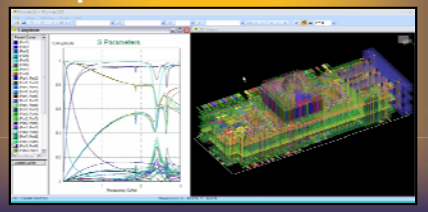
XcitePI

PDN Z Extraction



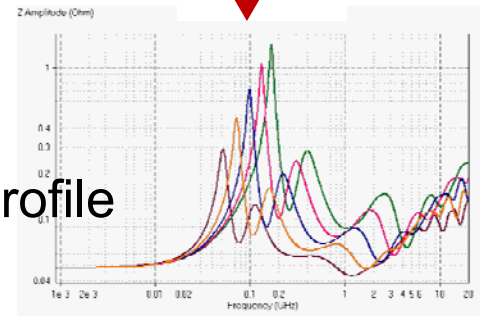
OptimizePI

PDN S-parameter Extraction



SPICE Model with MCP Headers

System level impedance profile



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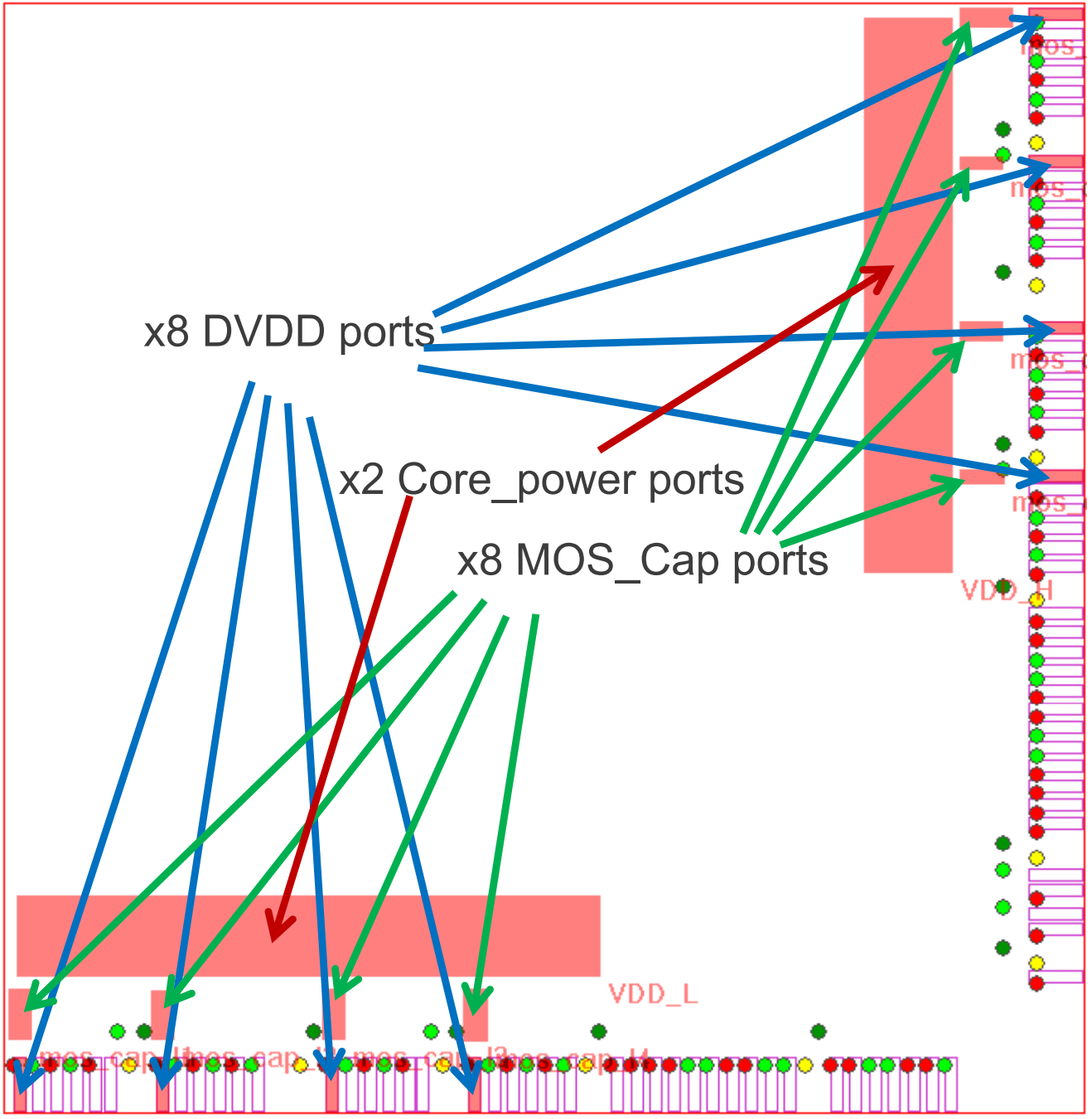
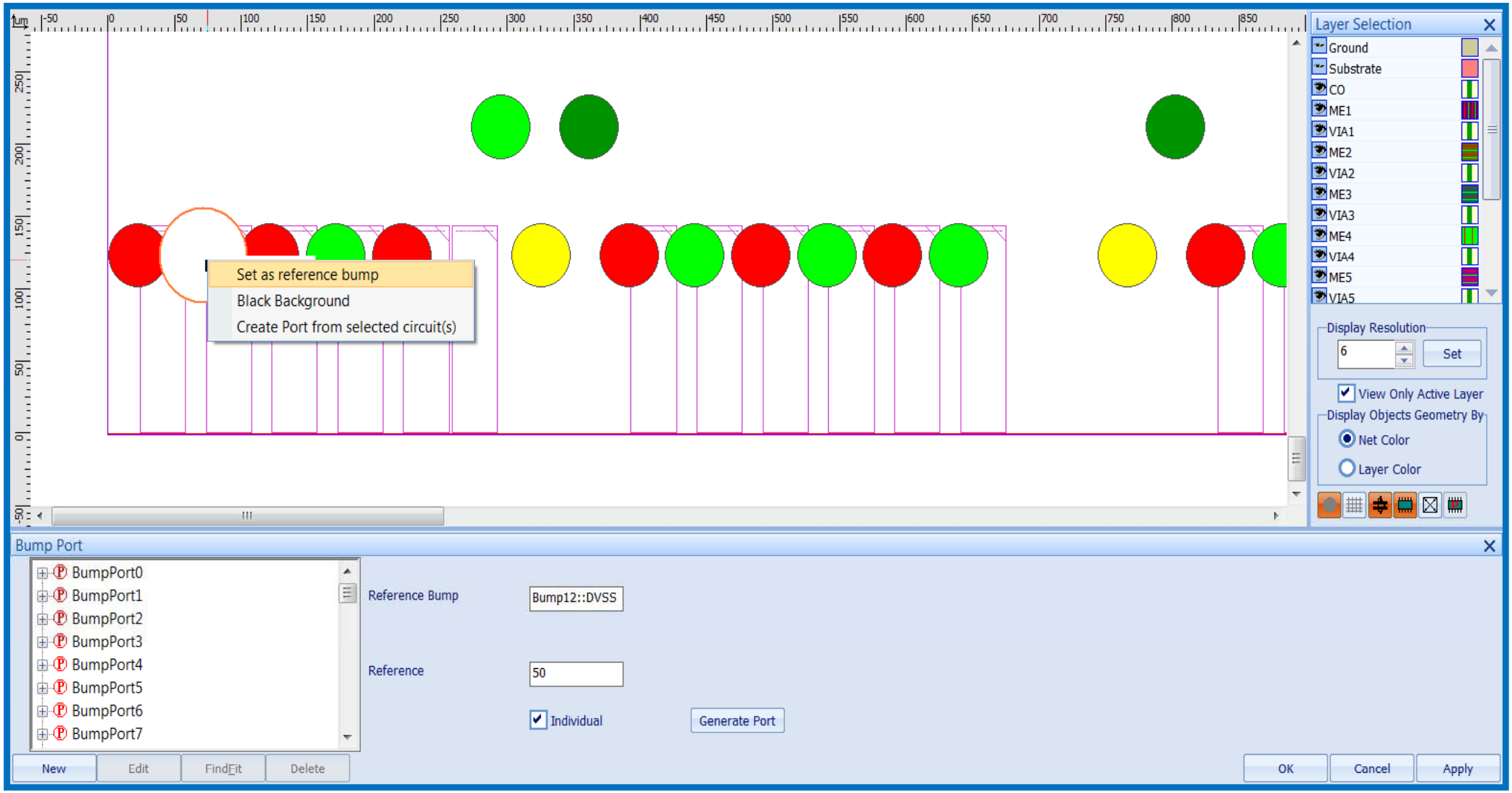
Step1. create observation ports on chip design

- To create Vio and Vcore observation ports.
- Vio/Vcore ports can be selected and created from IO/Core circuits.
- Any extra observation ports can be setup manually.
- To create MOS cap ports manually



Step2. create bump ports



- To set a reference bump and generate bump ports automatically for later MCP connection with die pads of the package

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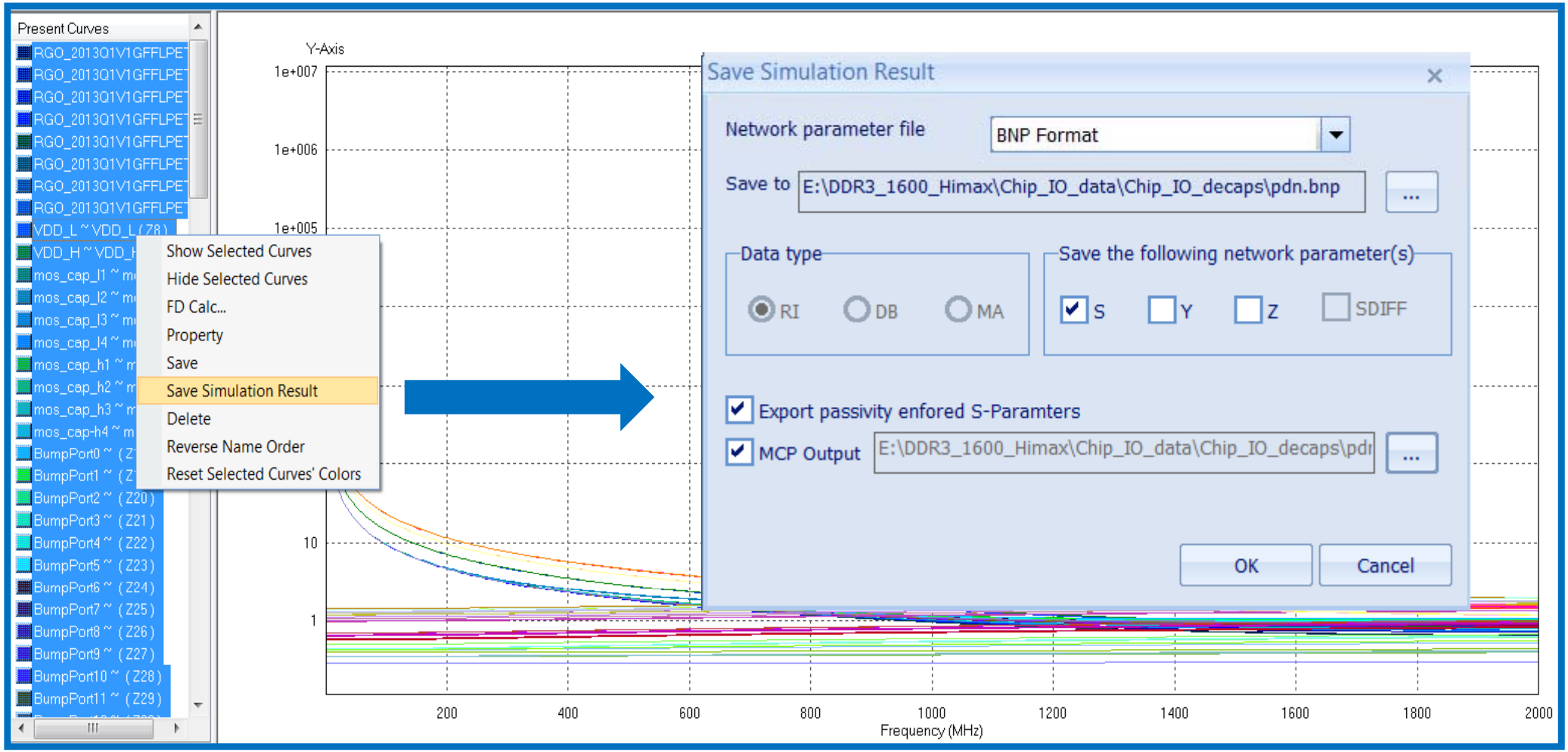
Step3. Run FD simulation and save as MCP circuits



- Enforce passivity (in case you would like to perform TD PDN simulation) and MCP generation are enable.

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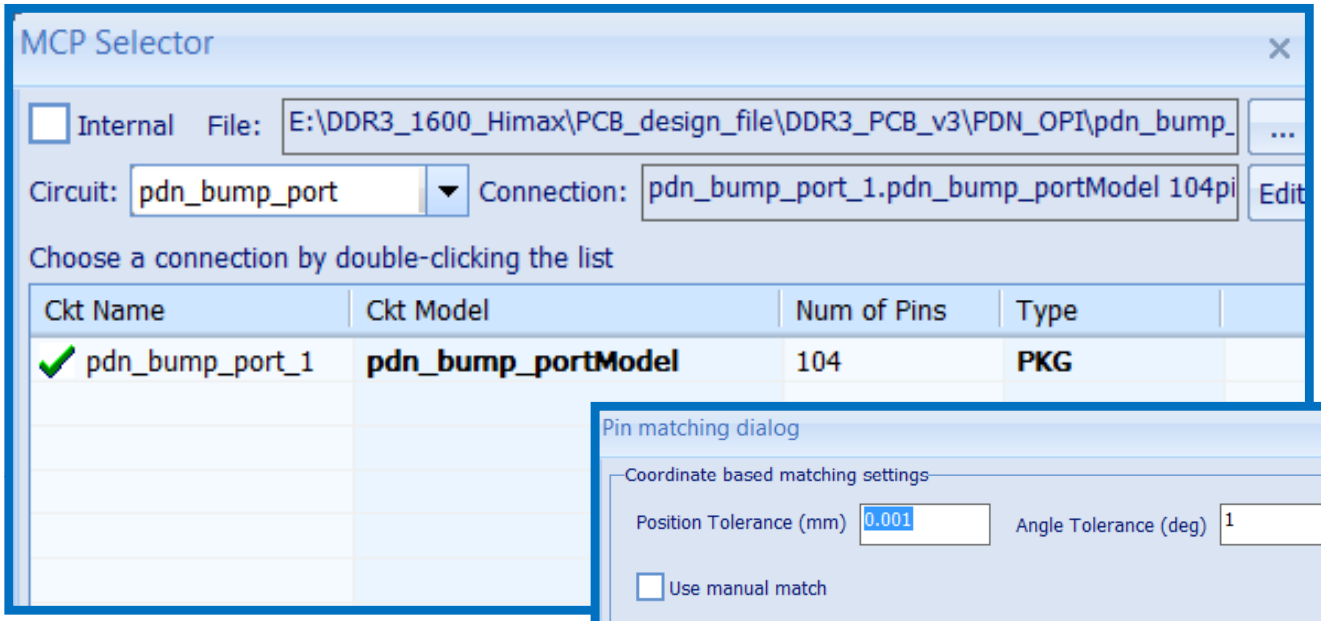
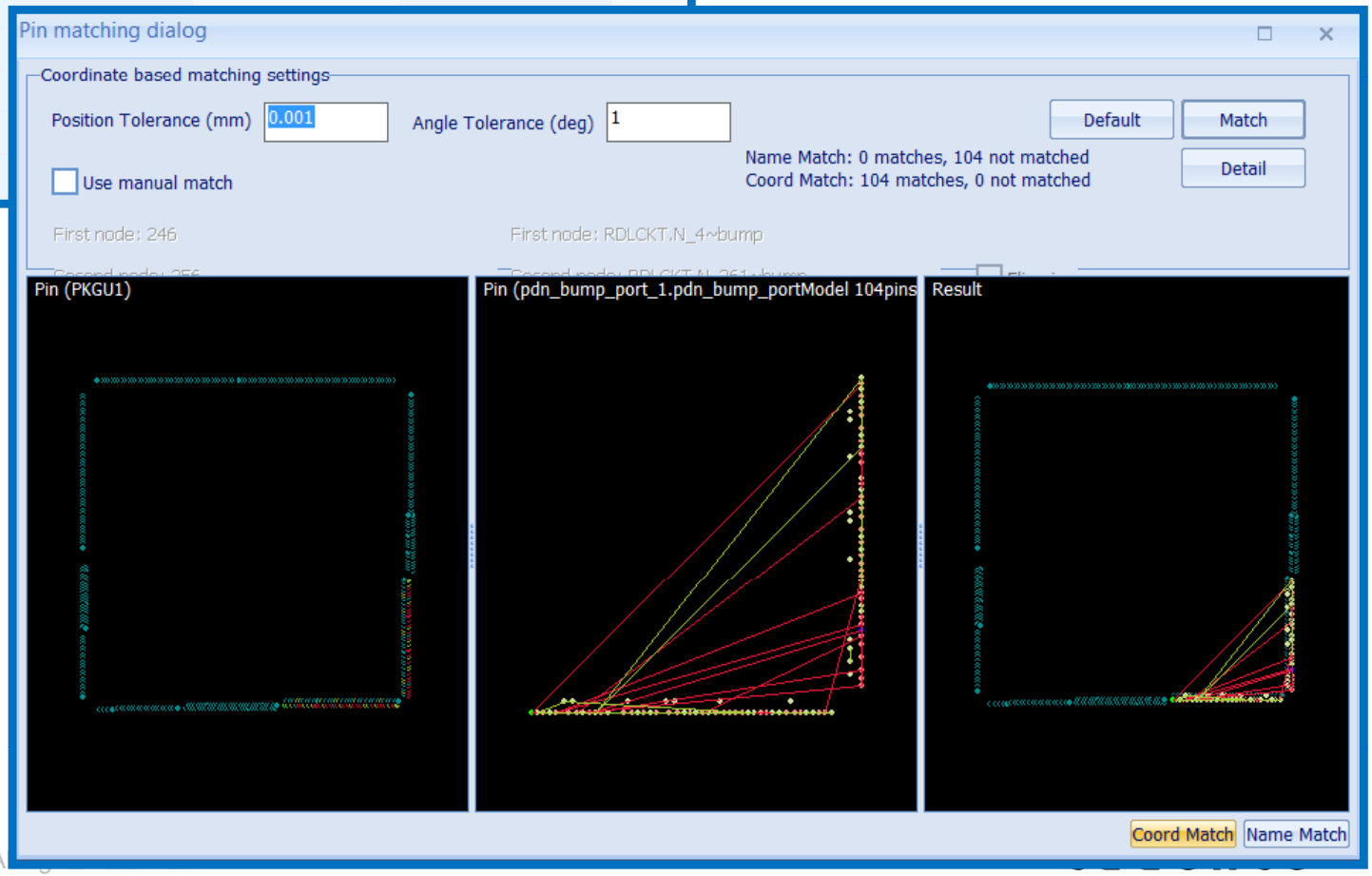
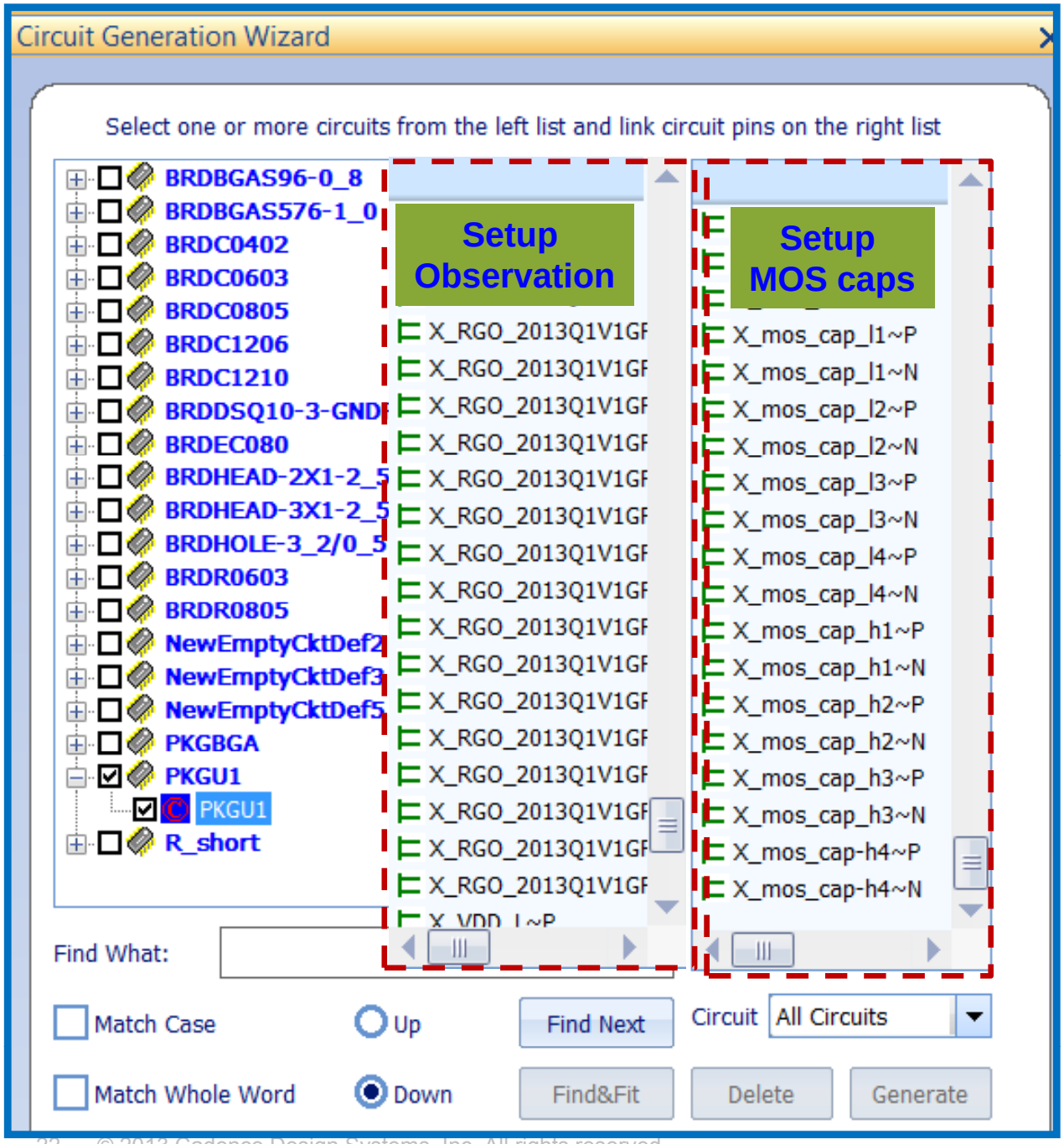
Step4. load chip MCP circuit into OptimizePI



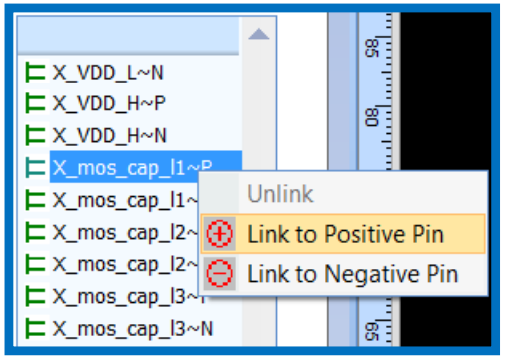


- To choose chip MCP model file and enable bump ports circuit..
- Either Coord or Name Match can help to link chip model with die pads of the package automatically.

Step5. setup MOS caps and on-die observation

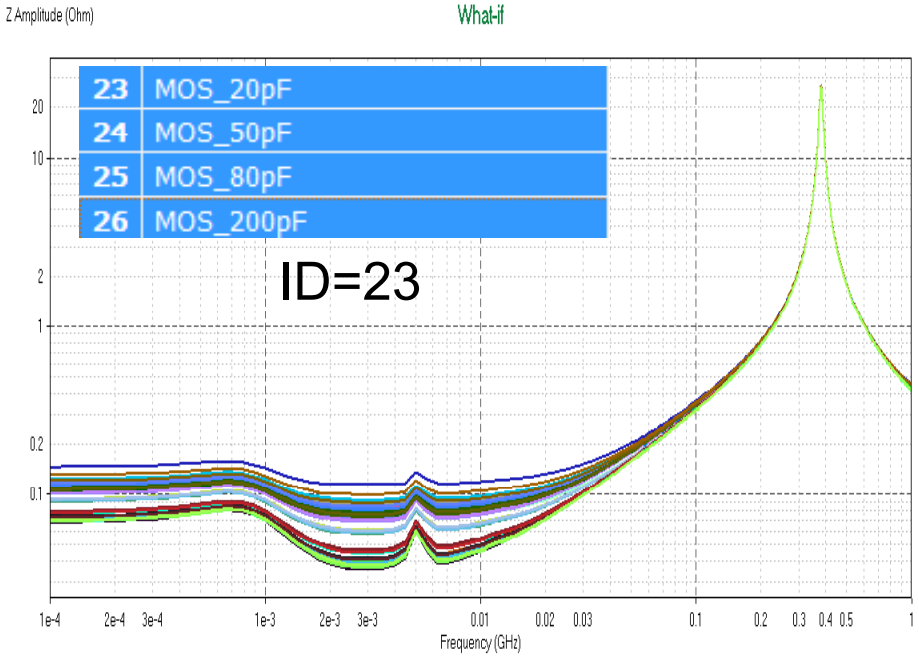


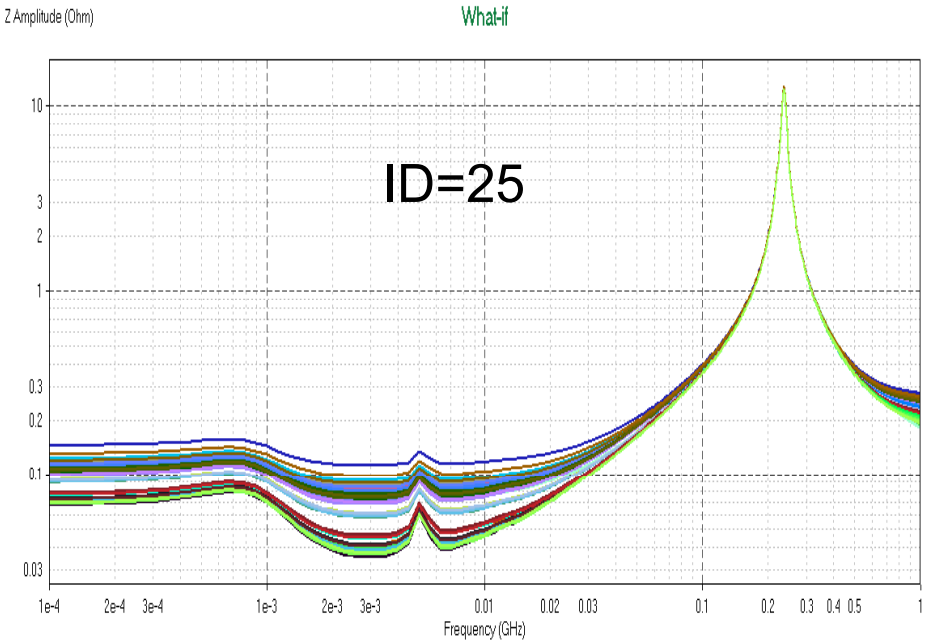
- Choose package die circuit and sub-circuit of chip model will show up.
- To find out circuit terminals of MOS caps and set decap ports for later optimization.
- To find out circuit terminals of on-die observations

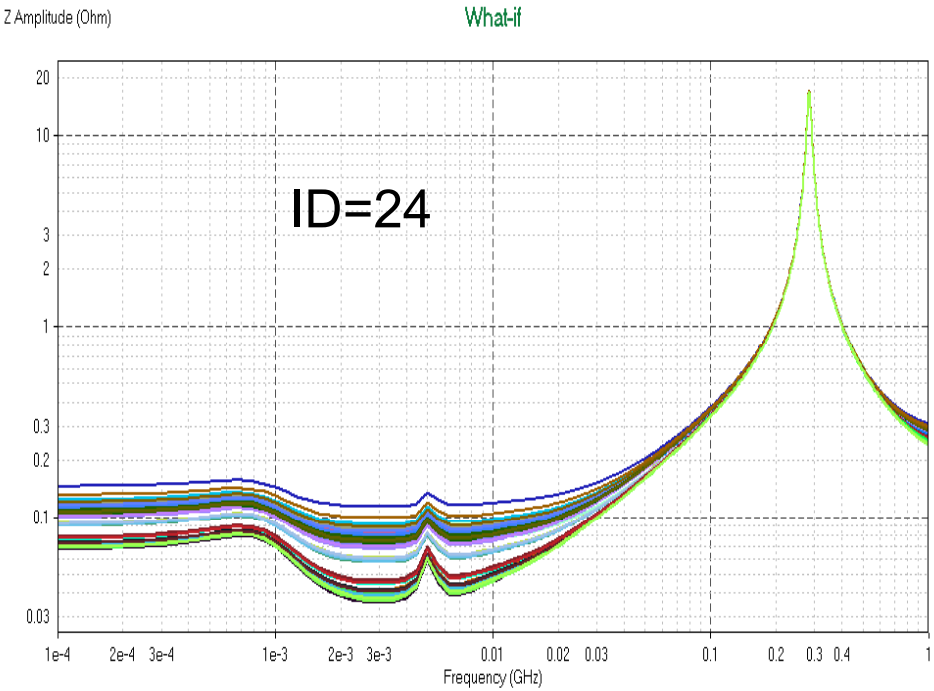


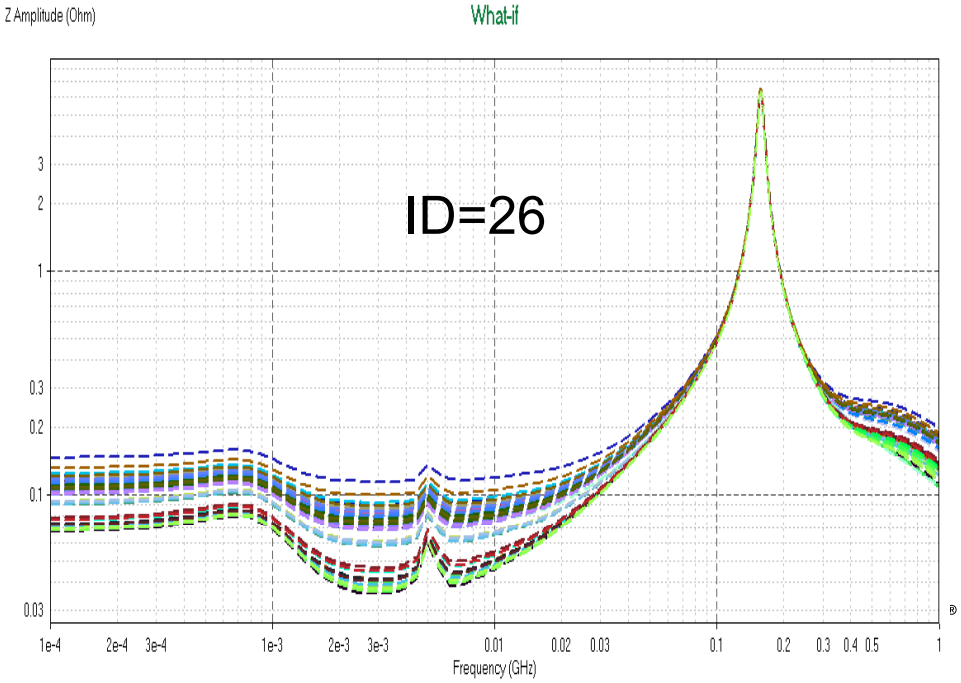
Step6. MOS caps Optimization

- Make original decaps fixed on PCB and study MOS caps effect only.



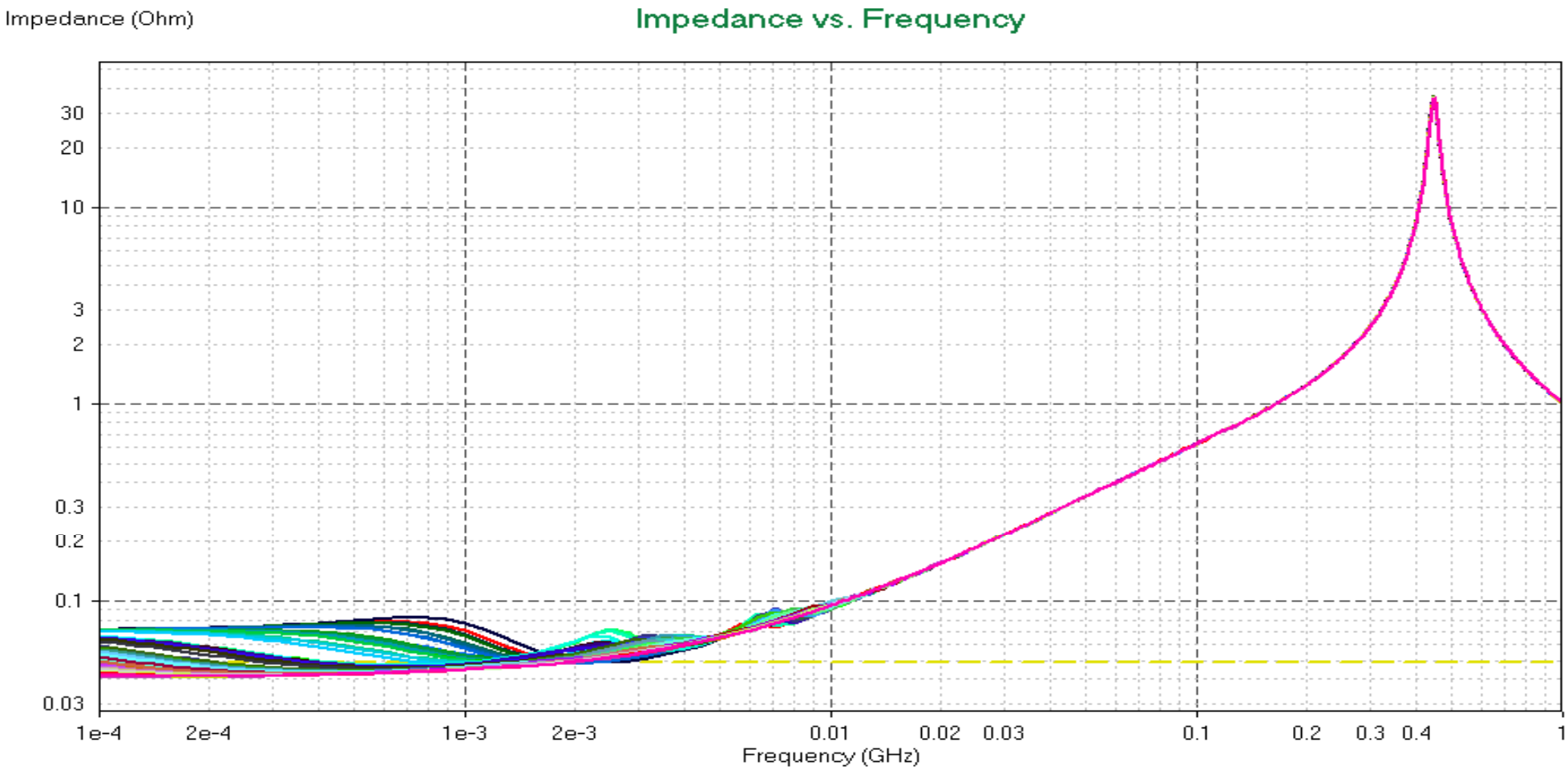






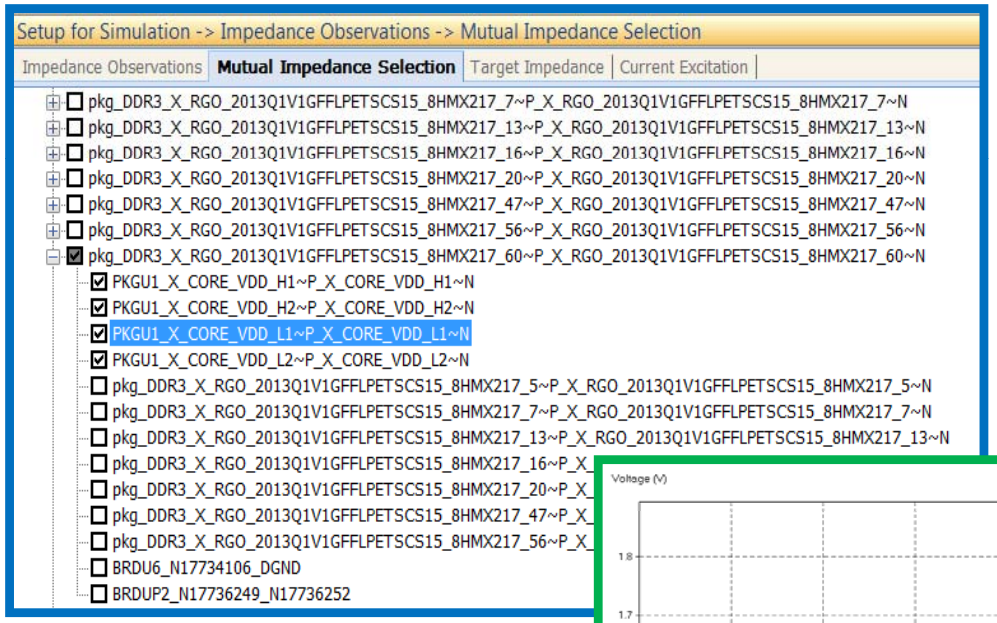
Step7. “off-chip decaps Optimization”

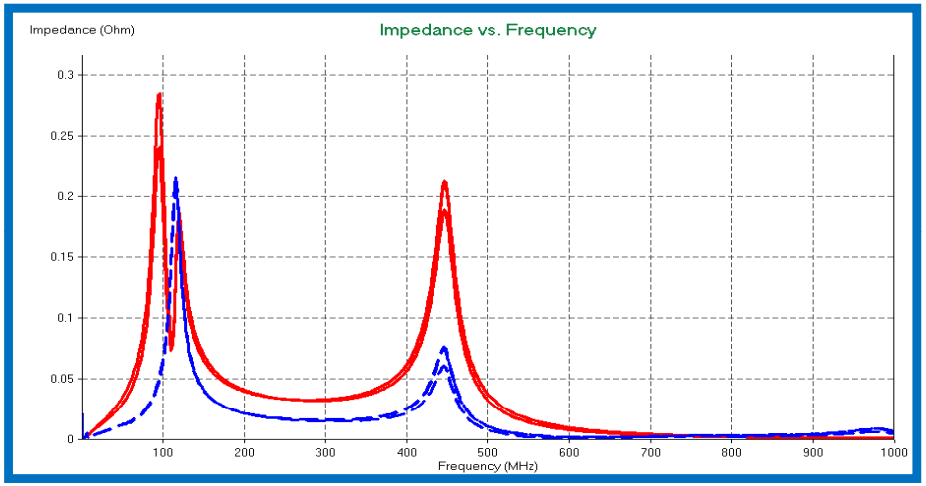
- Fixed optimized MOS caps as we found in step7
- Allow decaps on board can be optimized.

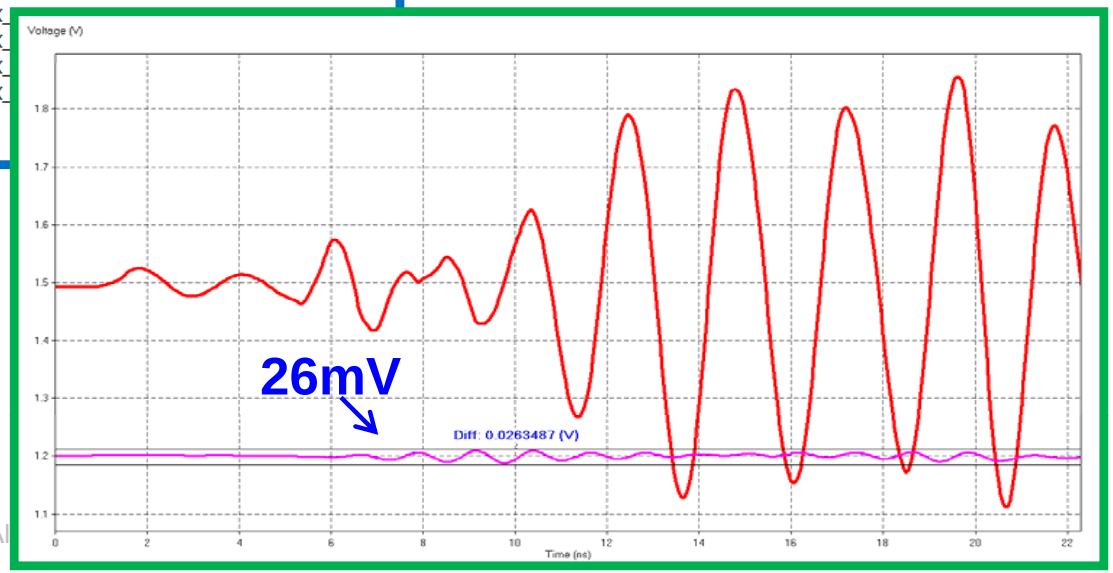


Step8. coupling between core and IO power domain through “Device Optimization” with off-chip decaps

- Mutual impedance observations between Vio and Vcore can be monitored during input impedance optimization. Mutual impedance will be optimized as well.







Summary

- Low cost design implies more technical challenge to be overcome.
- System level PDS becomes an critical issue that impacts timing and signal integrity.
- Co-simulation between chip and off-chip that helps to dig out potential PI problems which may not be found in the sub-system of chip + package + board.
- To face LPDDR3/DDR3 or DDR4, how to make P/G stay at low impedance is first priority.
- To control signal and P/G current loops that help to reduce coupling between them and lead to better timing skew control.