An Alternative for Design Checking through Electrical Performance Assessment

Paddy Wu
Principal AE
Aug.13 2013

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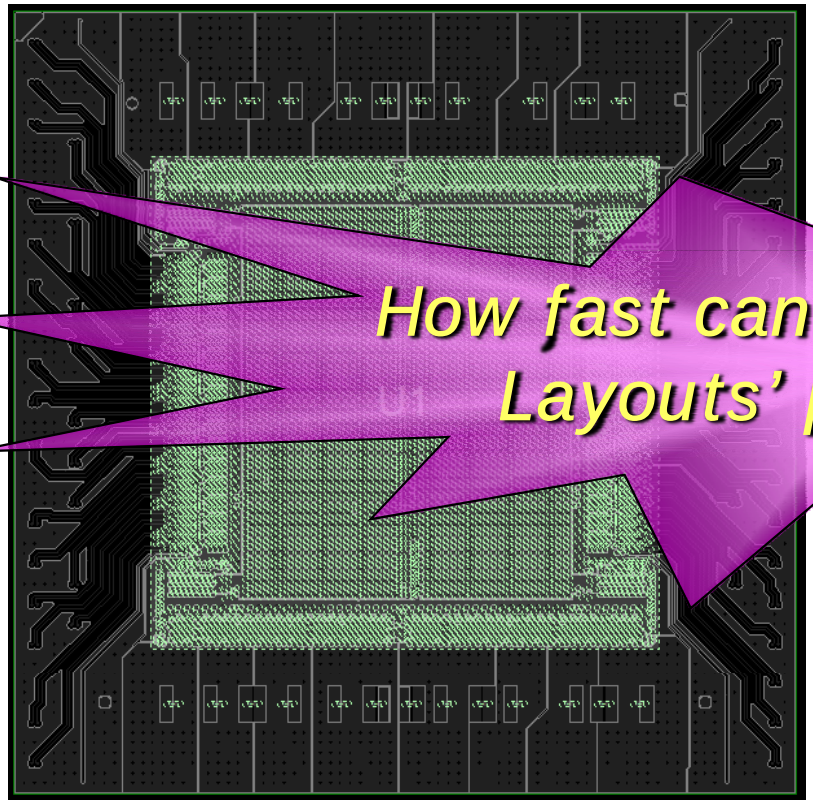
Agenda

- The Package/PCB Electrical Performance Checking Challenge
- Allegro Sigrity Integration for Package/PCB Checking Flow
- Electrical Performance Checking for PKG/PCB items-
  - ❑Trace Impedance / Coupling Check
- Electrical Performance Checking for PKG items-
  - ❑Power/Ground Inductance
  - ❑Power/Ground Current Density
- Customer real case
- Summary

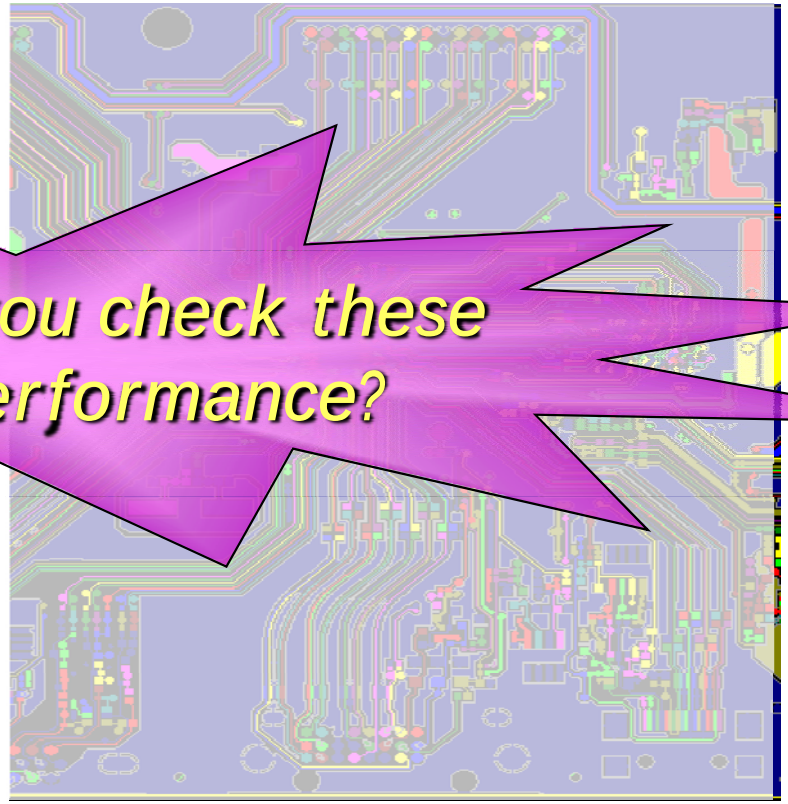
The Electrical Performance Checking Challenge

- Two basic questions and request for high speed signals
  - Impedance & Timing

10Layers FCBGA



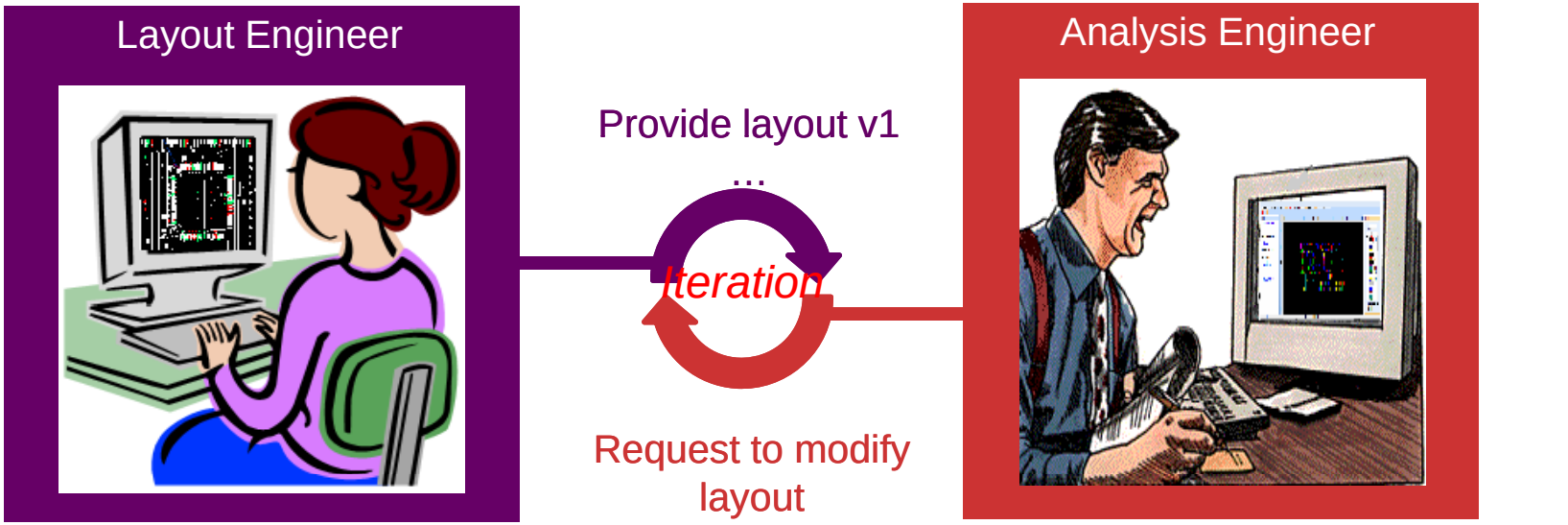
4L PCB 22x12cm



How fast can you check these Layouts' performance?

Layout and Analysis Engineers Co-work Flow

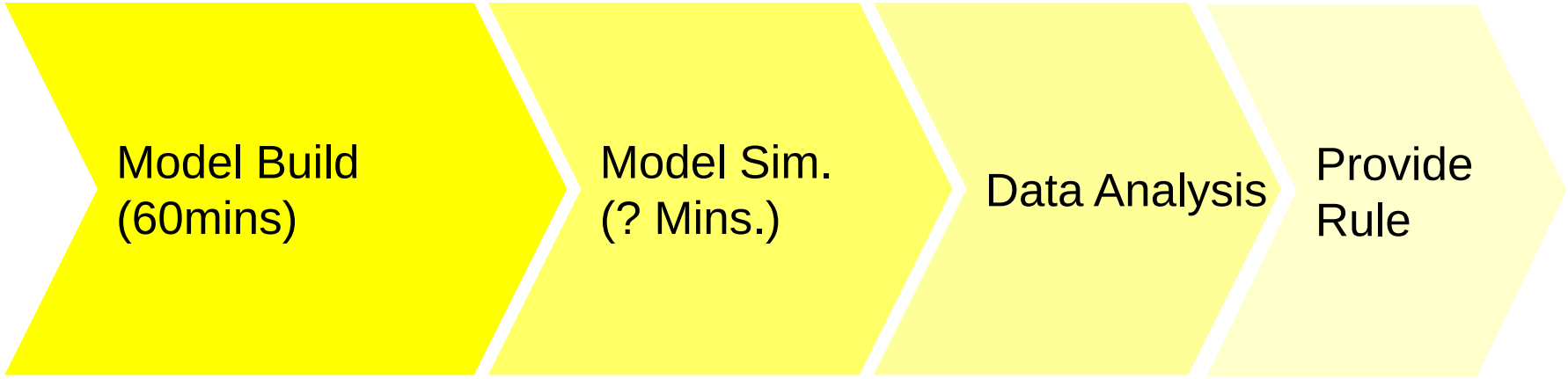
- Different tool environments
- Different languages



Cadence can provide the seamless working environment.

Analyzed/Checking Work Flow (Cont'd)

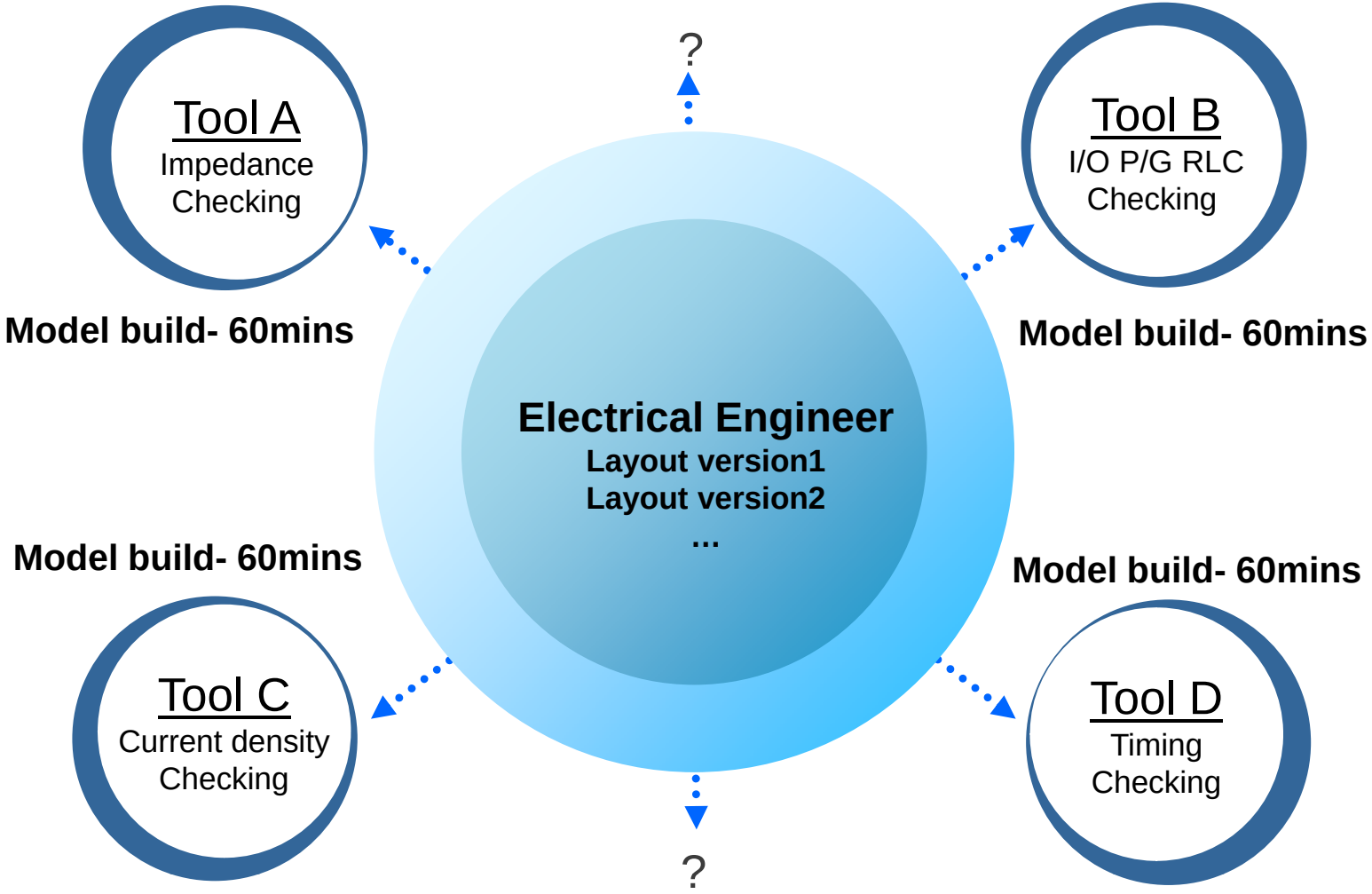
- One layout, one model build
- One kind of simulation, one model build



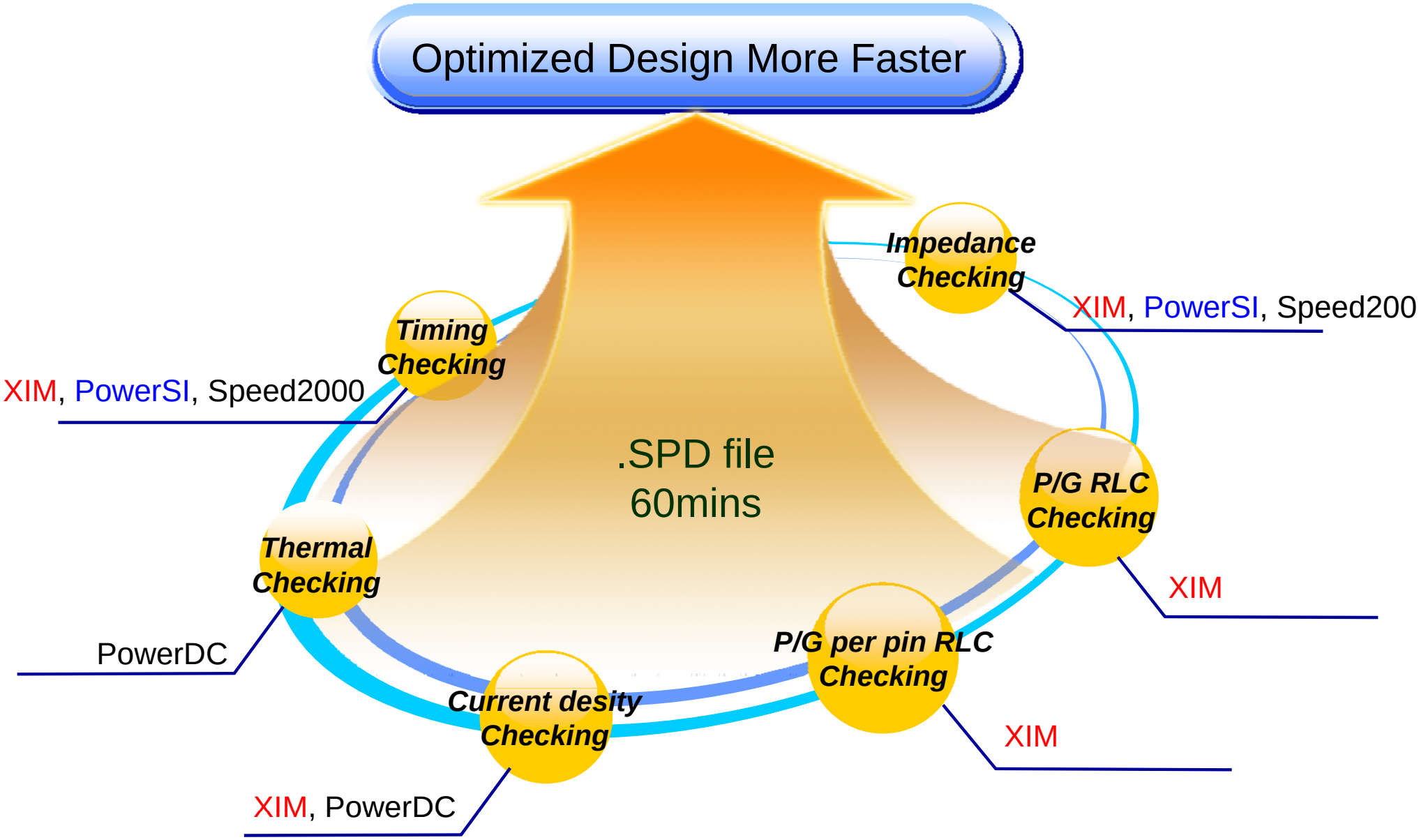
Cadence can provide model re-used function for specific simulation.

Analyzed/Checking Work Flow

- Time consumed for model build and exchanged



Allegro Sigrity Integration for Checking Flow



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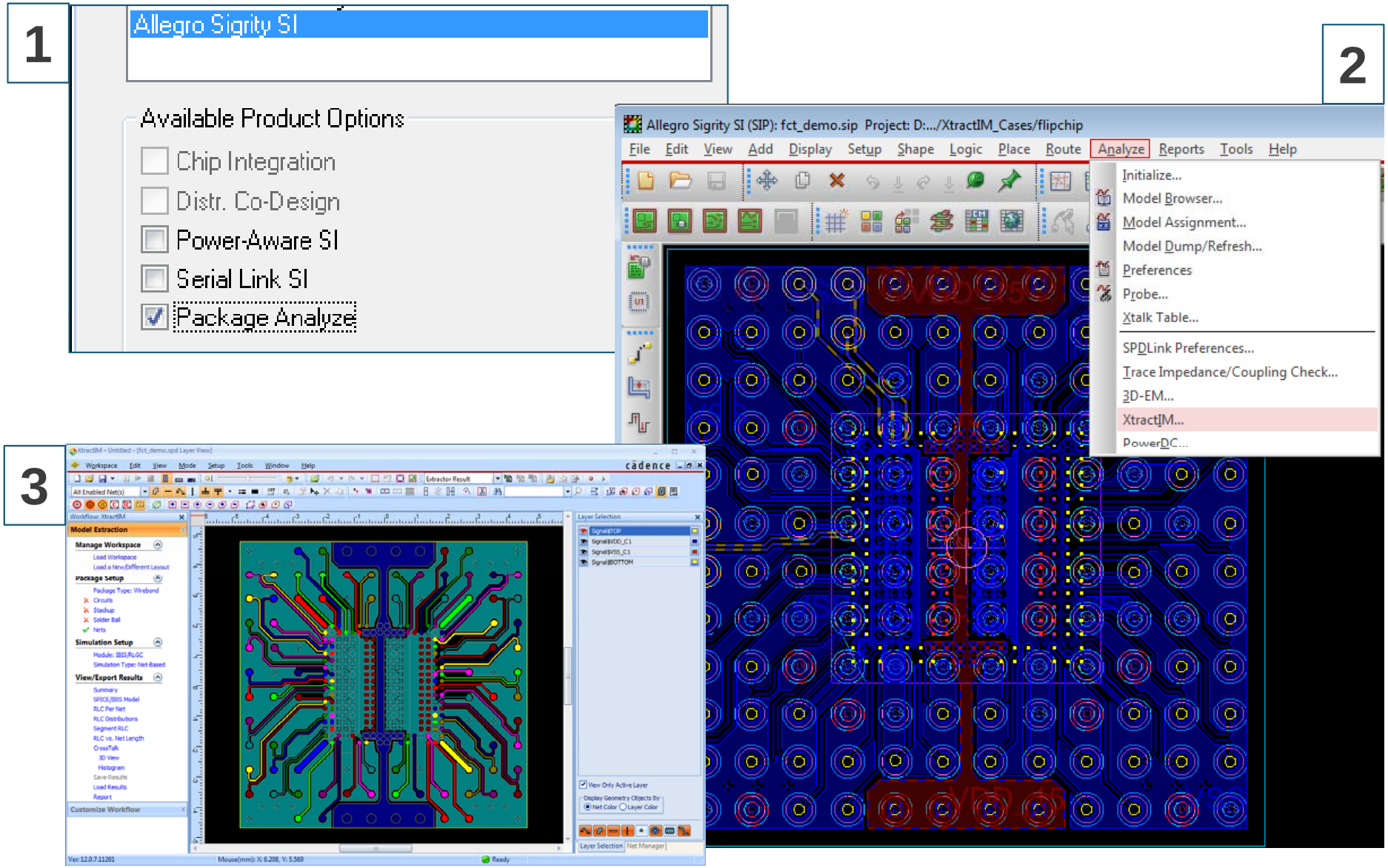
What is Allegro Sigrity Suite

Edits can be made in base tool and quickly investigated in XIM, PDC, 3D-EM,..



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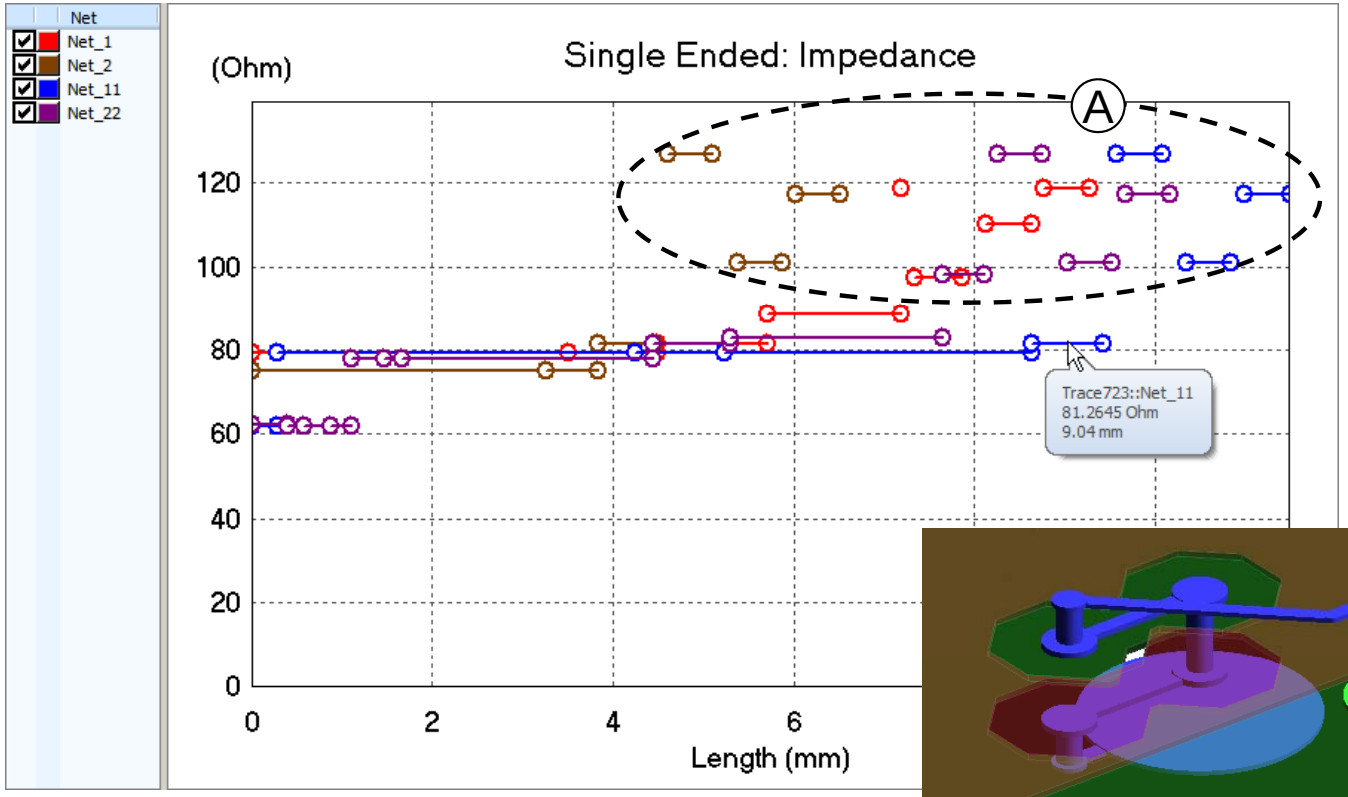
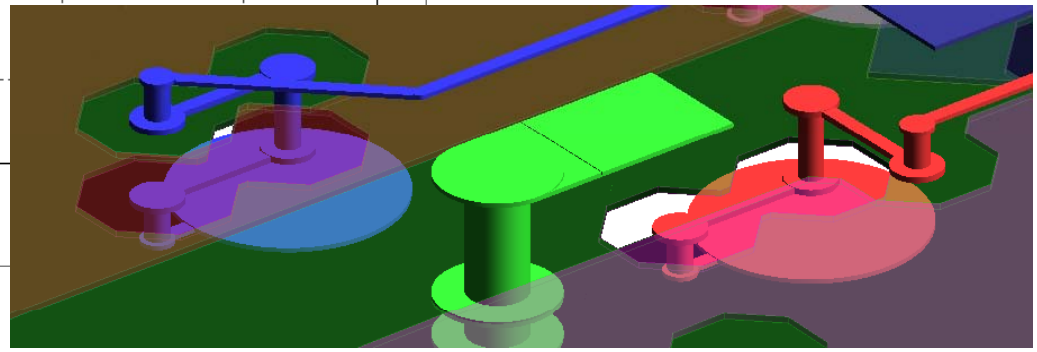
Electrical Checking for PKG/PCB items

- Trace Impedance --- function1

- Impedance are displayed along the length of the nets
  - Potential issue
    - Top-to-bottom layer transition dogleg traces do not have good reference planes



Ⓐ
top-to-bottom
transitions

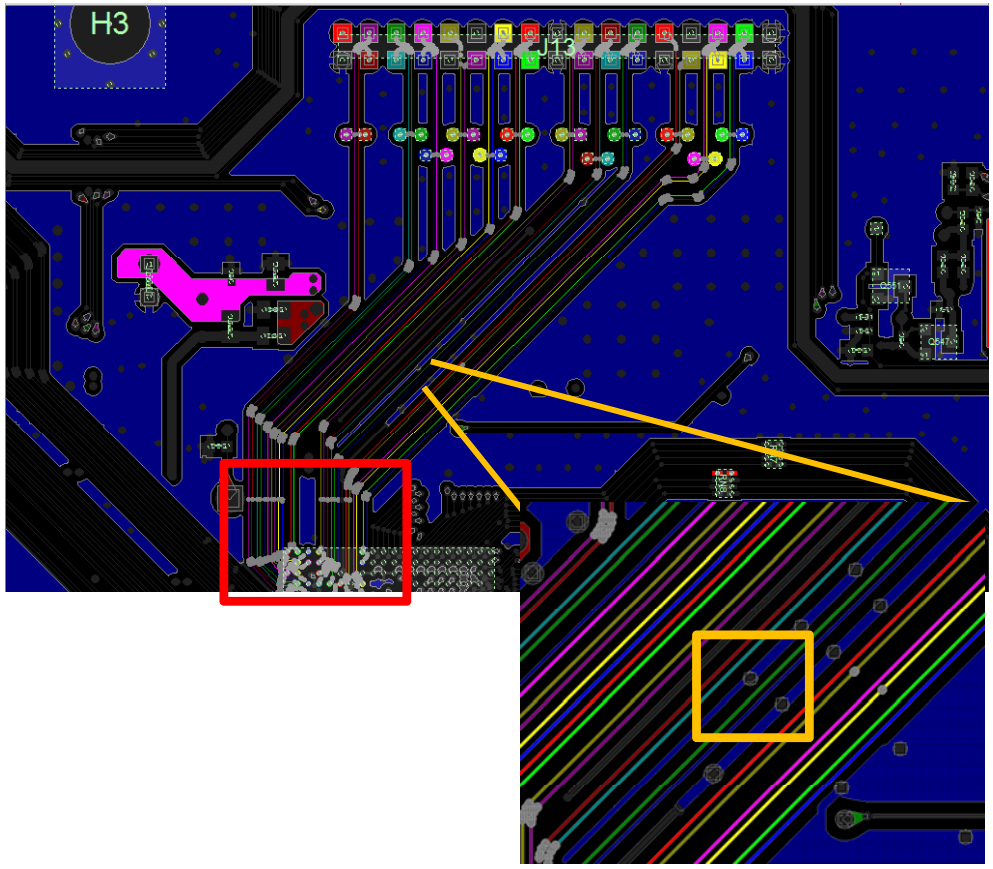


Electrical Checking for PKG/PCB items

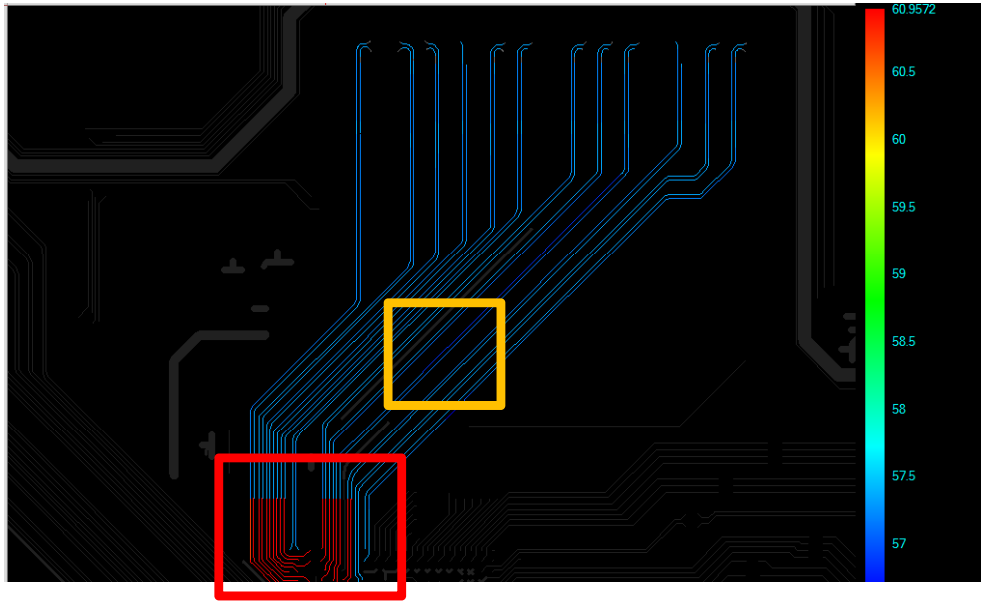
- Trace Impedance --- function2

- Fast find out the impedance discontinuity location
  - Potential issue
    - The traces do not have the same trace width

Layer1



Impedance value



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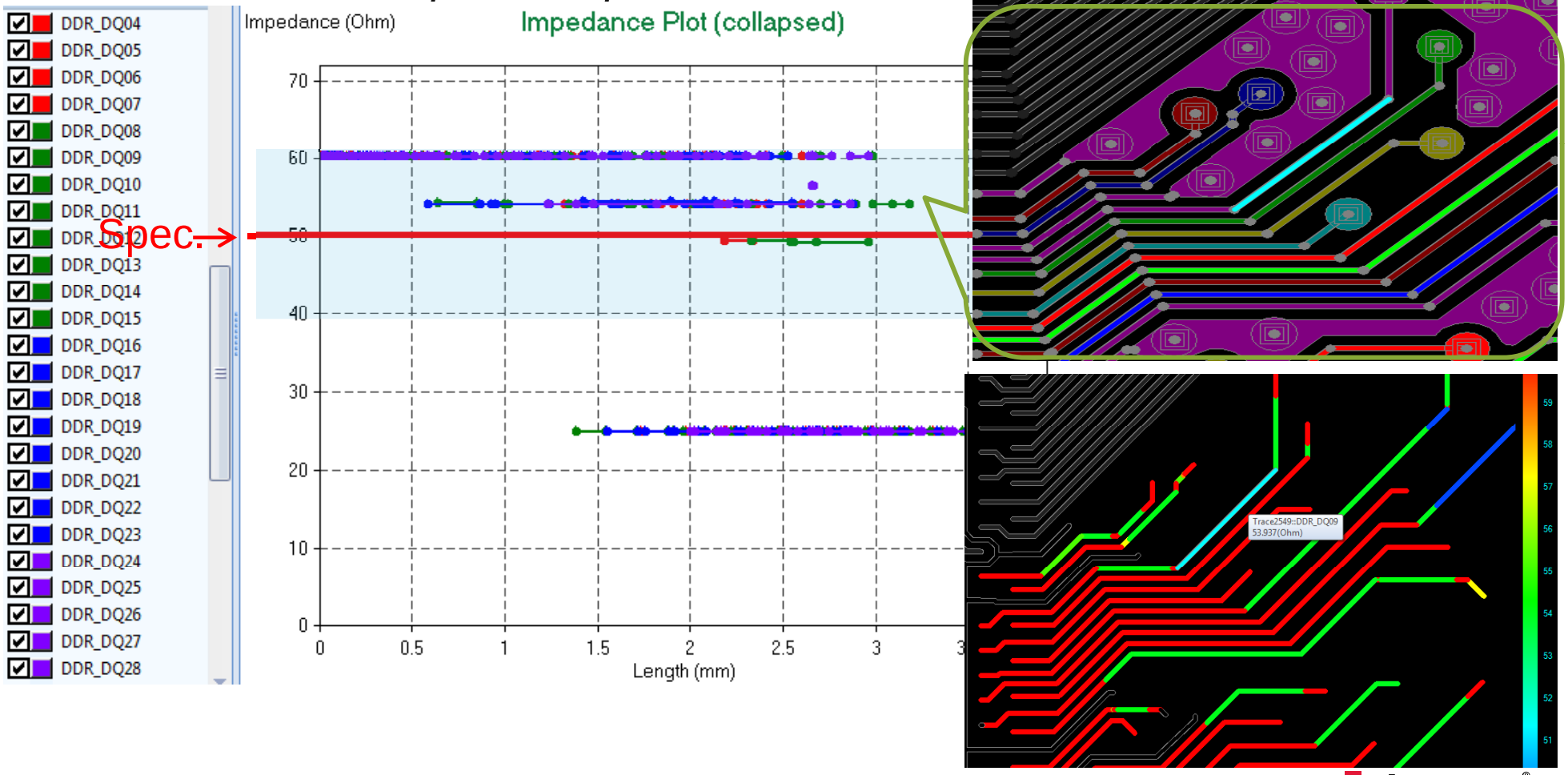
Electrical Checking for PKG/PCB items
- Trace Impedance --- Applications

- Find the each groups impedance and define limited impedance zone
  - Simulation time – 3 min.

Impedance plot

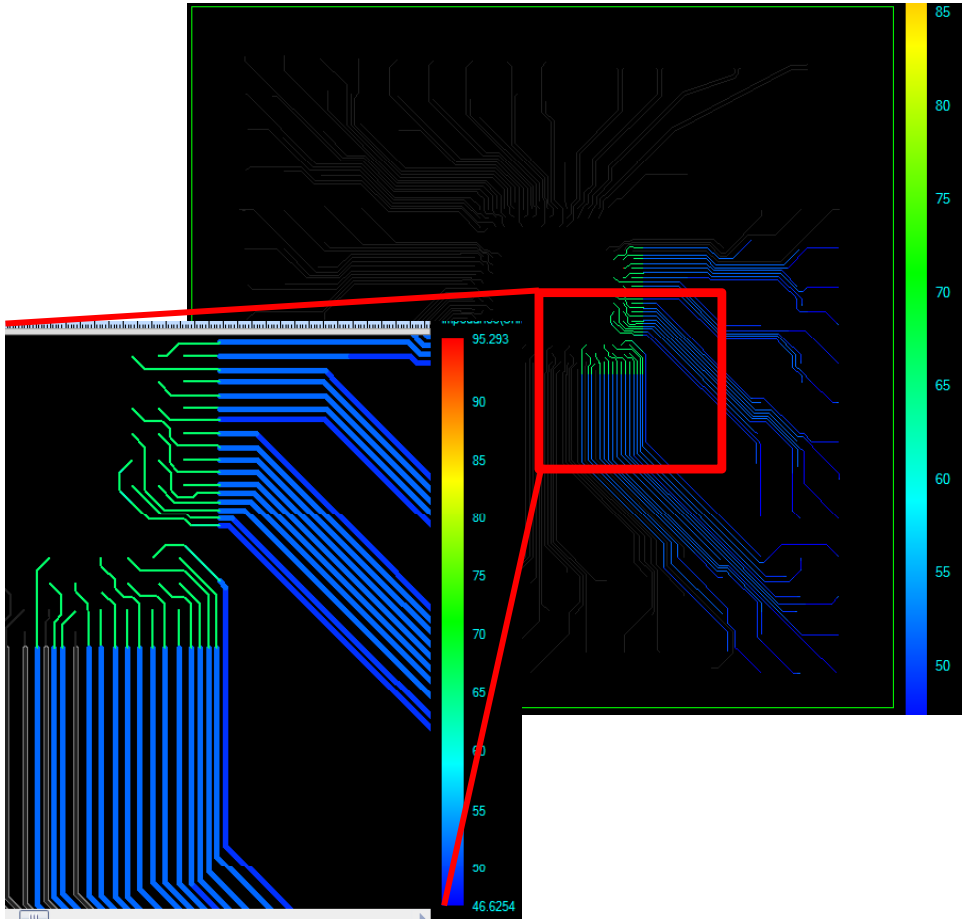
DDR_DQ9



Electrical Checking for PKG/PCB items
- Trace Impedance --- Applications

- Fast find out the numbers of impedance discontinuity on each nets

Layer1 impedance



Impedance table

Net Coui	Net Name	# of Trace Reference Discontinuities	# of Vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)
1	X_MAC_TXDATA_0	1	7	65.871	19.950
2	X_MAC_TXDATA_1	0	7	65.871	19.950
3	X_MAC_TXDATA_2	3	7	65.871	19.950
4	X_MAC_TXDATA_3	2	7	65.871	19.950
5	X_MAC_TXDATA_4	3	7	95.293	19.950
6	X_MAC_TXDATA_5	10	6	49.977	28.290
7	X_MAC_TXDATA_6	6	7	65.871	19.950
8	X_MAC_TXDATA_7	1	7	65.871	19.950
9	X_MAC_TXDATA_8	4	7	95.605	19.950
10	X_MAC_TXDATA_9	3	7	65.871	19.950
11	X_MAC_TXDATA_10	2	7	65.871	19.950
12	X_MAC_TXDATA_11	15	6	49.977	28.257
13	X_MAC_TXDATA_12	3	7	65.871	19.950
14	X_MAC_TXDATA_13	7	7	65.871	19.950
15	X_MAC_TXDATA_14	0	7	65.871	19.950
16	X_MAC_TXDATA_15	3	7	65.871	19.950

More discontinuities, SI more worse.

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Electrical Checking for PKG/PCB items
- Trace Timing

Different languages

Complicated relationships

Layout Design Rules
multiple
individual
geometry-based

Layout SI Performance
collective
combined
electrical-based

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Electrical Checking for PKG/PCB items
- Trace Timing --- Applications

- Find the each nets and groups timings

Timing table

	Net	Total trace length(mm)	Total trace delay(ns)
Group1	DDR_DQ00	2.275	0.016
	DDR_DQ01	2.397	0.016
	DDR_DQ02	1.958	0.013
	DDR_DQ03	3.032	0.021
	DDR_DQ04	2.461	0.017
	DDR_DQ05	2.845	0.019
	DDR_DQ06	2.200	0.015
	DDR_DQ07	2.416	0.017
Group2	DDR_DQ08	2.191	0.015
	DDR_DQ09	2.438	0.017
	DDR_DQ10	2.131	0.015
	DDR_DQ11	3.528	0.024
	DDR_DQ12	1.599	0.011
	DDR_DQ13	2.828	0.019
	DDR_DQ14	2.715	0.019
	DDR_DQ15	3.240	0.022
Group3	DDR_DQ16	3.213	0.022
	DDR_DQ17	2.570	0.018
	DDR_DQ18	2.859	0.020
	DDR_DQ19	2.563	0.018
	DDR_DQ20	2.494	0.017
	DDR_DQ21	1.769	0.012
	DDR_DQ22	1.972	0.014
	DDR_DQ23	2.586	0.018
Group4	DDR_DQ24	3.109	0.021
	DDR_DQ25	2.631	0.018
	DDR_DQ26	2.712	0.019
	DDR_DQ27	2.216	0.015
	DDR_DQ28	3.297	0.023
	DDR_DQ29	2.372	0.016
	DDR_DQ30	2.246	0.015
	DDR_DQ31	2.748	0.019
	DDR_DQM0	1.994	0.014

DDR_DQ0 per layer timing

Trace/wirebond Name	% of its net length	Impedance(Ohm)	Length(mm)	Trace/wirebond distance from Starting Componen...	Trace delay(ns)
Trace3273::DDR_DQ00	12.28%	60.166	0.308	0.000	0.002
Trace3272::DDR_DQ00	14.14%	60.166	0.355	0.308	0.002
Trace3271::DDR_DQ00	26.60%	60.166	0.667	0.662	0.005
Trace3270::DDR_DQ00	11.63%	60.166	0.291	1.329	0.002
Trace3269::DDR_DQ00	12.64%	60.166	0.317	1.621	0.002
Trace3268::DDR_DQ00	6.96%	24.851	0.175	2.054	0.001
Trace3267::DDR_DQ00	6.49%	24.851	0.163	2.228	0.001

These timing table can give electrical/layout engineers with the same languages.

Electrical Checking for PKG/PCB items
- Trace Coupling --- Applications

- Coupling is defined with Near-ended Crosstalk as a victim.

$$K = \frac{Vp}{4}(C_{12}Z_{20} + \frac{L_{12}}{Z_{10}})$$

Net	Length(mm)
X_USBH3_DM	9.609
X_USBH3_DP	9.402
X_USBH3_RREF	6.979

Trace Name	Length(mm)	% of its net length	Coupled Lines	Coupling Coefficient
Wirebond109::X_USBH3_DP	2.653	28.22%		
Trace2035::X_USBH3_DP	0.323	3.44%		
	0.112	1.19%		
	0.212	2.25%	**Trace2054::X_USBH3_DM**	12.17%
Trace2036::X_USBH3_DP	0.111	1.18%		
Trace2037::X_USBH3_DP	0.515	5.48%		
	0.399	4.24%	**Trace2056::X_USBH3_DM**	12.16%
	0.116	1.23%		
Trace2038::X_USBH3_DP	0.769	8.18%		
	0.044	0.46%		
	0.725	7.71%	**Trace2058::X_USBH3_DM**	11.87%
Trace2039::X_USBH3_DP	2.670	28.40%		
	2.627	27.94%	**Trace2059_Auto_5::X_USBH3_DM**	11.73%
	0.043	0.46%		
Trace2040::X_USBH3_DP	1.123	11.94%		
	0.044	0.46%		
	1.079	11.48%	**Trace2060::X_USBH3_DM**	11.76%
Trace2041::X_USBH3_DP	0.249	2.65%	Trace2061_Auto_1::X_USBH3_DM	12.17%

User can define the coupling coefficient for each of nets.

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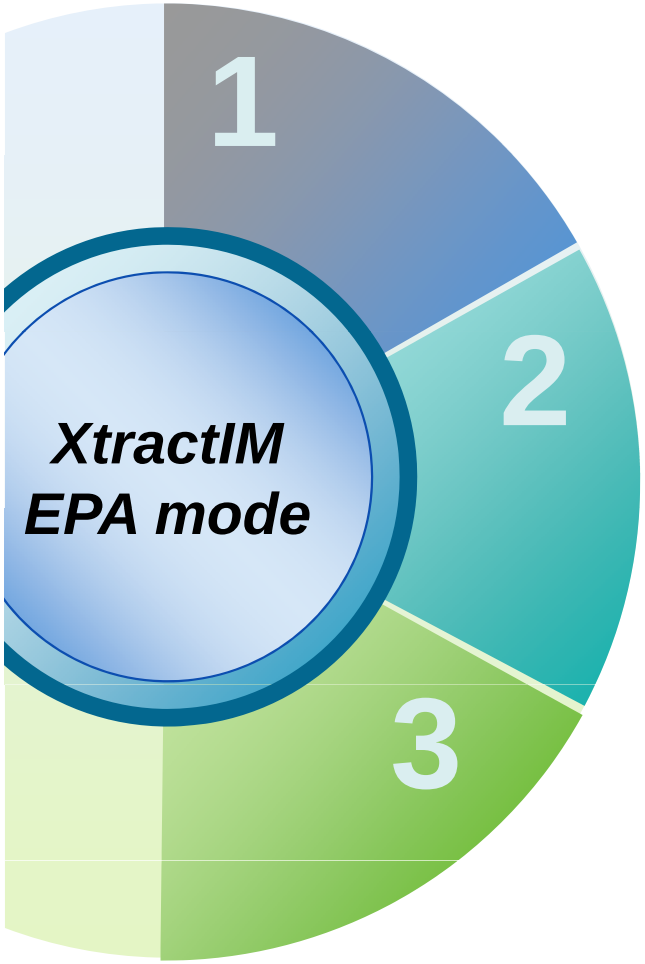
Electrical Performance Checking for PKG items
- XtractIM Electrical Performance Assessment (EPA)



For Signal Analysis

- ❑ Impedance and discontinuity, Trace timing
- ❑ Coupling co-efficient

For P/G Analysis

- ❑ Per net-pair properties
- ❑ Per pin-based properties

For DC Current Analysis

- ❑ Check DC current density
- ❑ IR drop

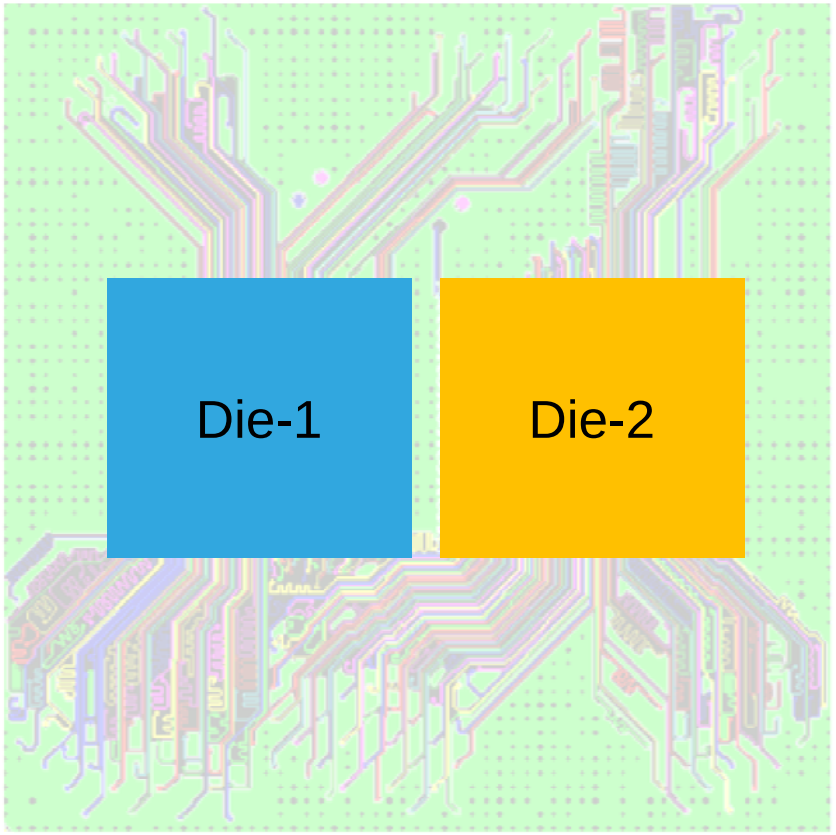
For P/G Analysis (Cont'd)
- Per net-pair properties --- function1

- 6-layer side-by-side flipchip package
  - Run time 1 hour.

One common reference GND (pH)

Net	Die-1	Die-2
VDD	3.722	3.746
VCCQ	27.589	25.002

Find worse loop inductance & unbalance inductance!



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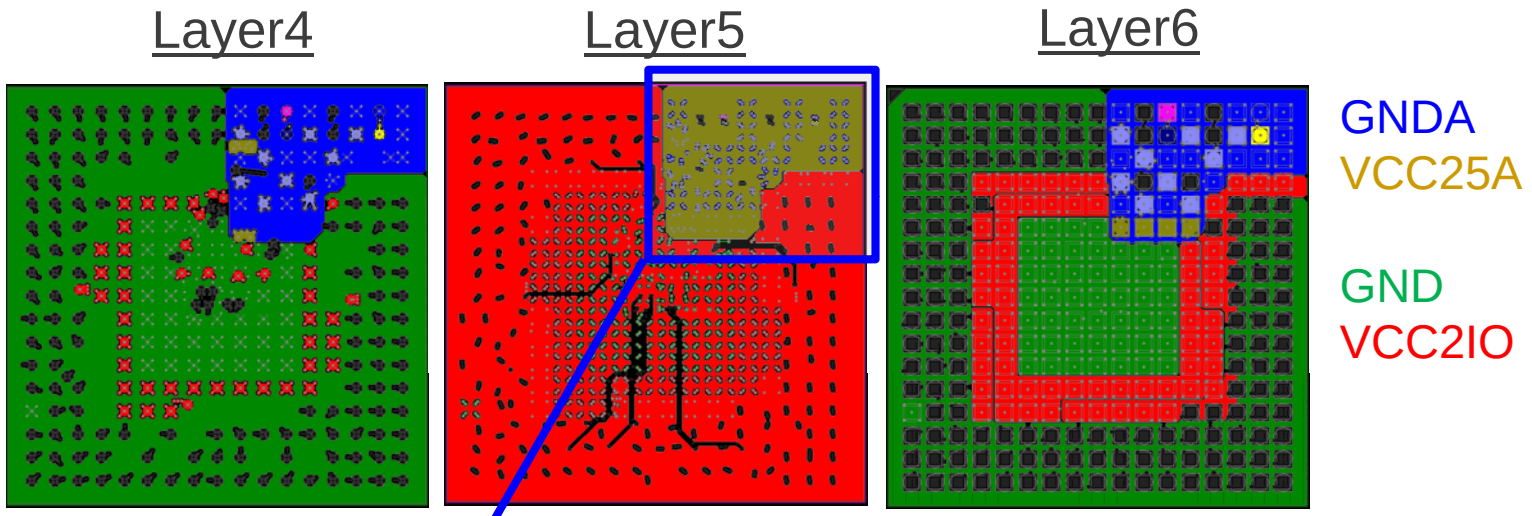
For P/G Analysis (Cont'd)

- Per net-pair properties --- function2

- 6-layer single-die flipchip package
  - Find which ground net with the minimum loop inductance.



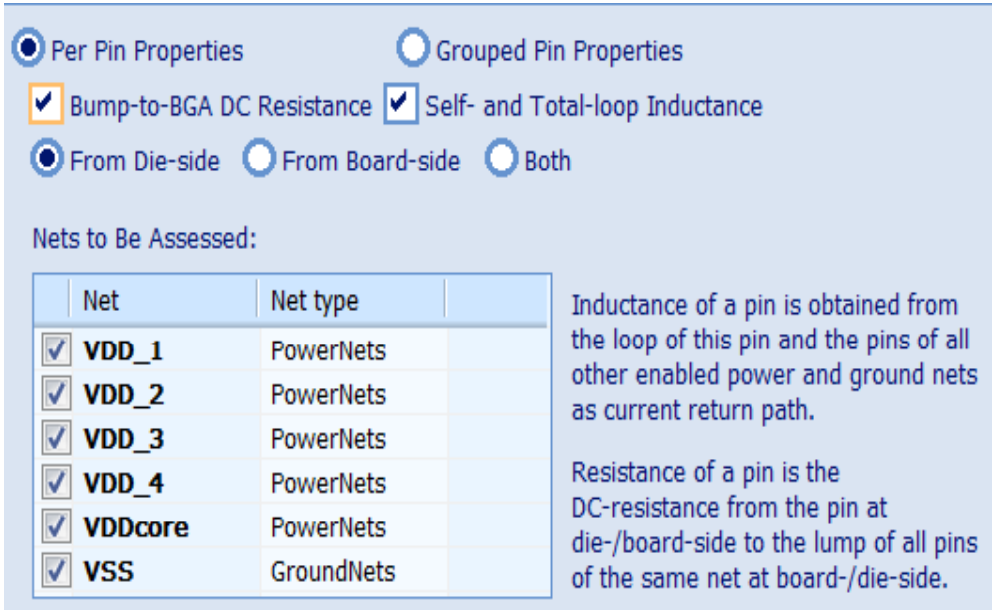
Power N...	Ref Ground Net	L(nH)	C(pF)
VCC11K	GND	0.057...	222.365
VCC2IO	GND	0.099...	310.351
VCC11A	GNDA	0.147...	34.1867
VCC25A	GND	0.377...	0.3791...

Ground Net	L(nH)
GND	0.37756
GNDA	0.536209

Wrong ground net for VCC25A !!

For P/G Analysis (Cont'd)
- Per pin-based properties

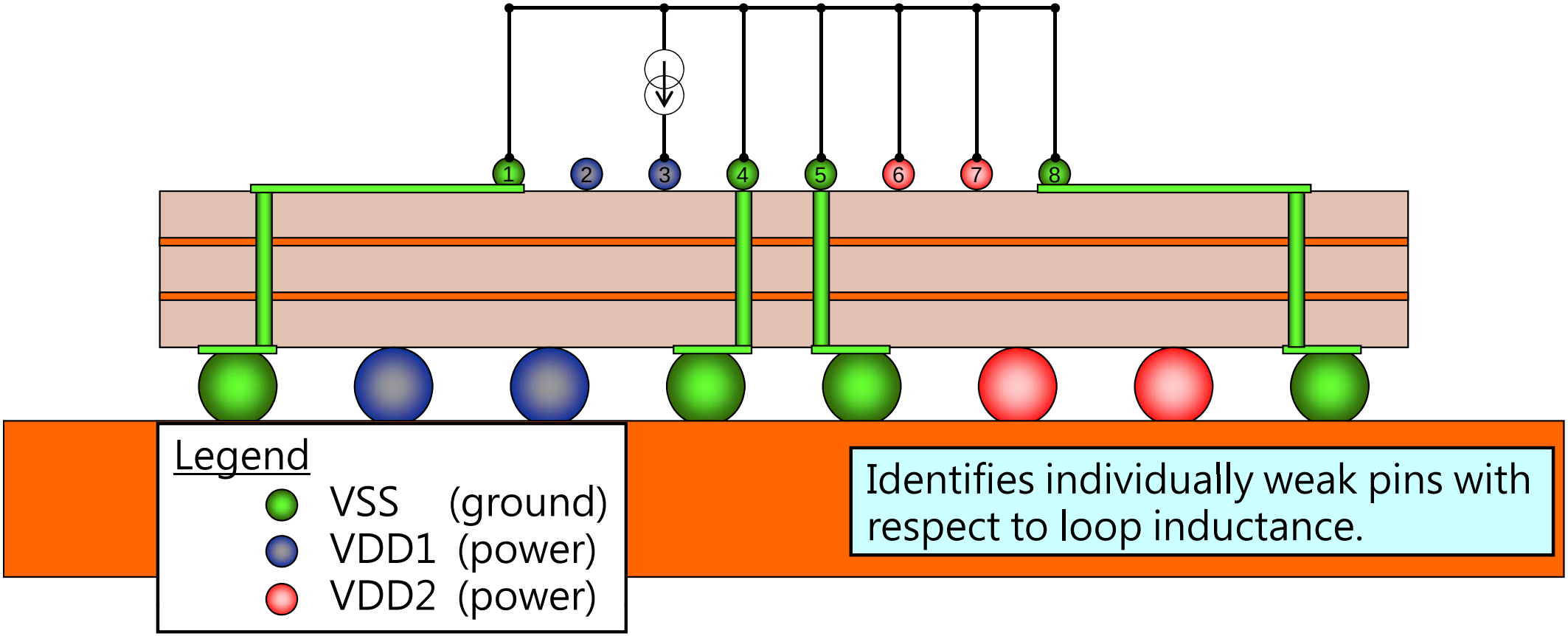
- Assess Bump/BGA pin properties
  - Self loop inductance
  - Total loop inductance
  - Resistance
- Intuitive 2D and 3D graphics
- Both die-side and board-side assessment
- With the assessment, pins with R&L higher than specified value will be found.



The problematic area in the power/ground distribution system can be optimized to avoid design risk!

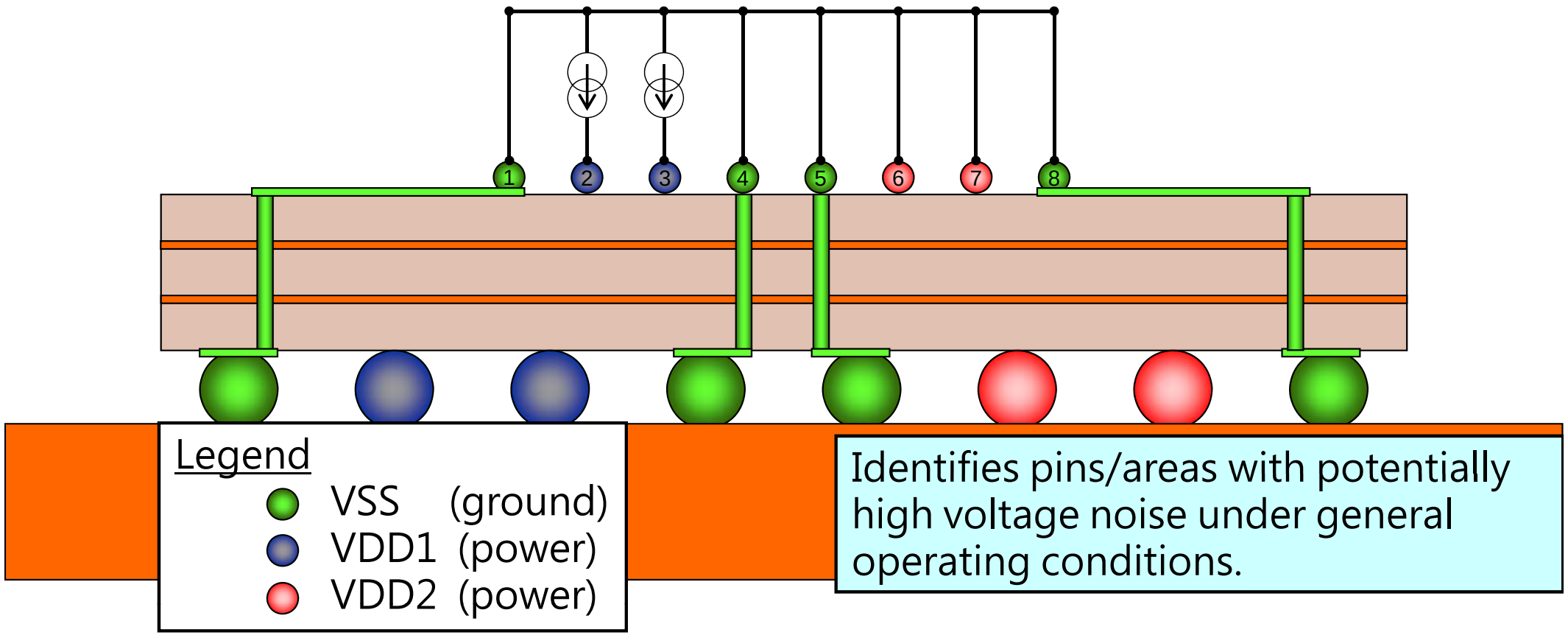
Per-pin “self” loop inductance

The loop inductance seen looking into one pin of the net being assessed when all other pins of all other enabled nets can serve as potential return paths.
The jωL voltage at pin 3 with AC current forced into only pin 3 with return current flowing in pins {1,4,5,6,7,8}.
The noise voltage at a pin due to current flow in that pin.



Per-pin “total” loop inductance

The sum of self and all mutual inductances seen looking into one pin for the net being assessed.
The jωL voltage at a pin with the same AC current forced into all pins of the net being assessed.
The noise voltage at a pin due to current flow in all pins of that net.



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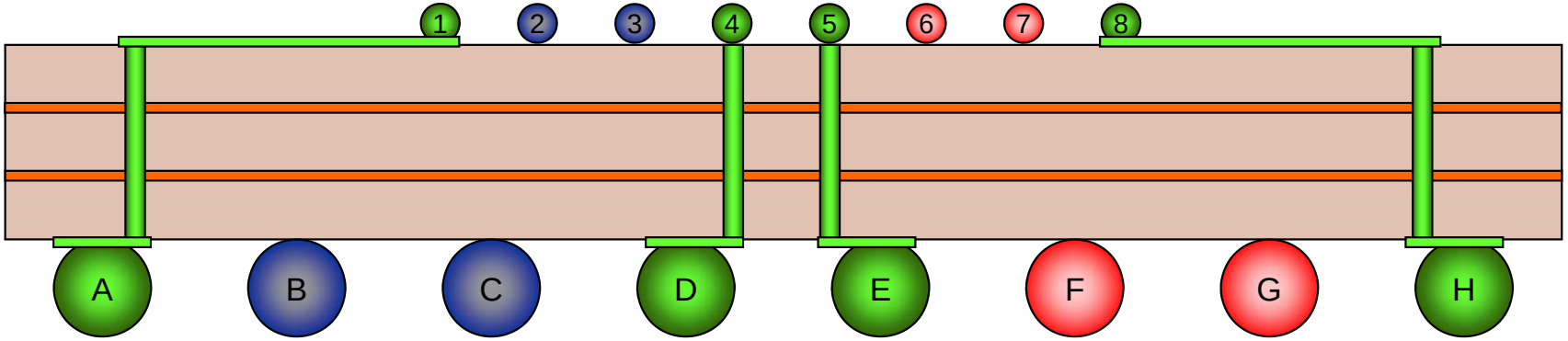
Per-pin R_{DC}

The DC resistance from a pin on one side of the package to the other side of the package where all pins of the same net on the other side are shorted together.
For example:

$$R_1 = R_{1\text{-}ADEH}\ ,\ R_2 = R_{2\text{-}BC}\ ,\ R_F = R_{F\text{-}67}$$



Legend

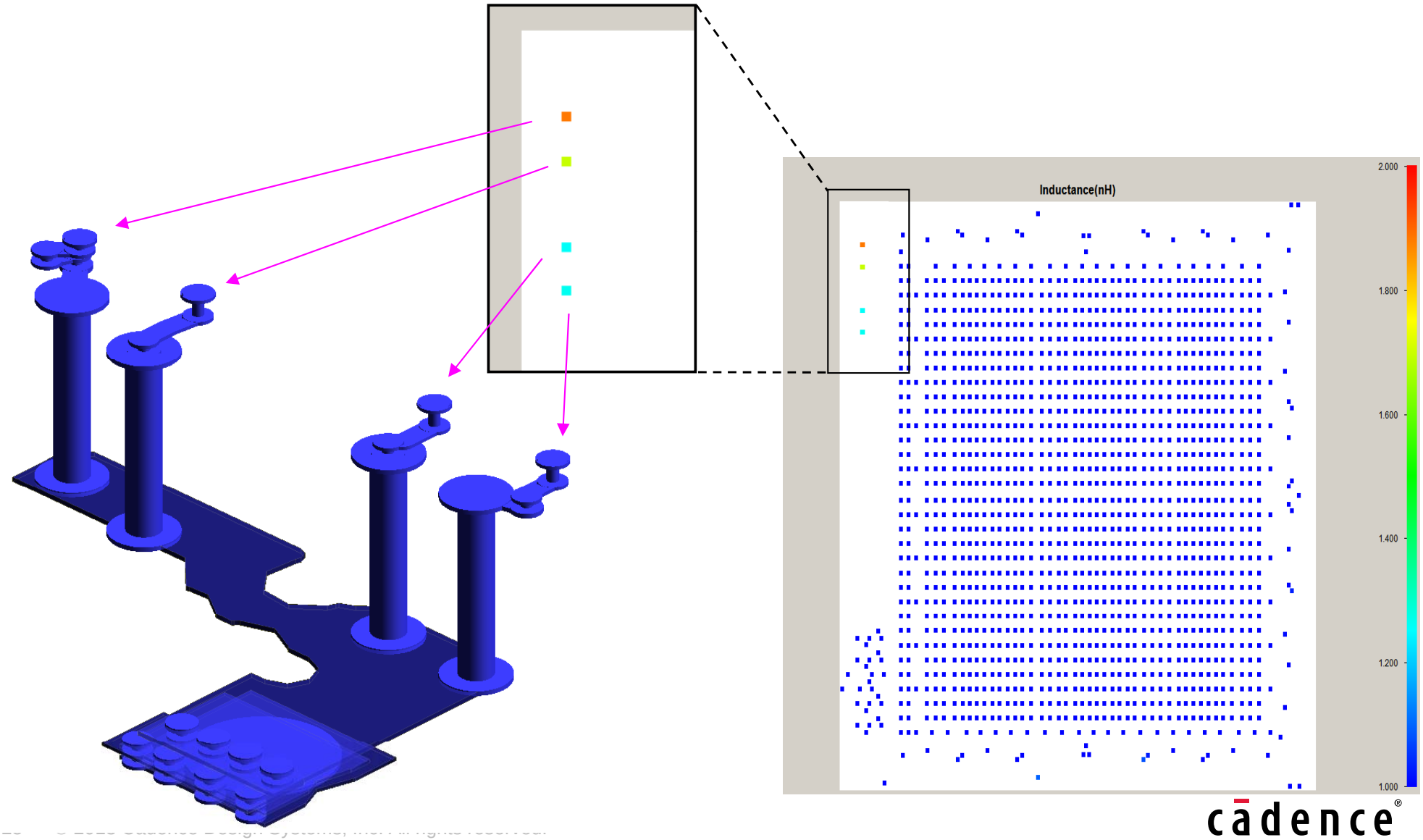
- VSS (ground)
- VDD1 (power)
- VDD2 (power)

Identifies individually weak pins for DC IR drop.

For P/G Analysis (Cont'd)

- Per pin-based properties --- Self loop inductance

- Easy to find per pin inductance



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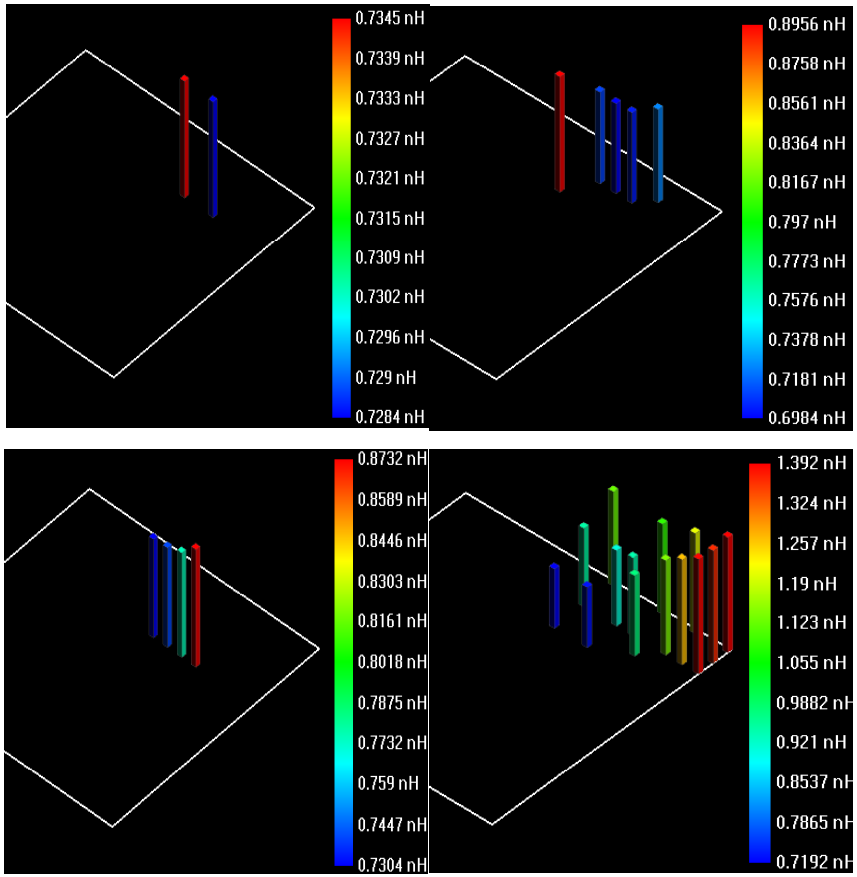
For P/G Analysis (Cont'd)

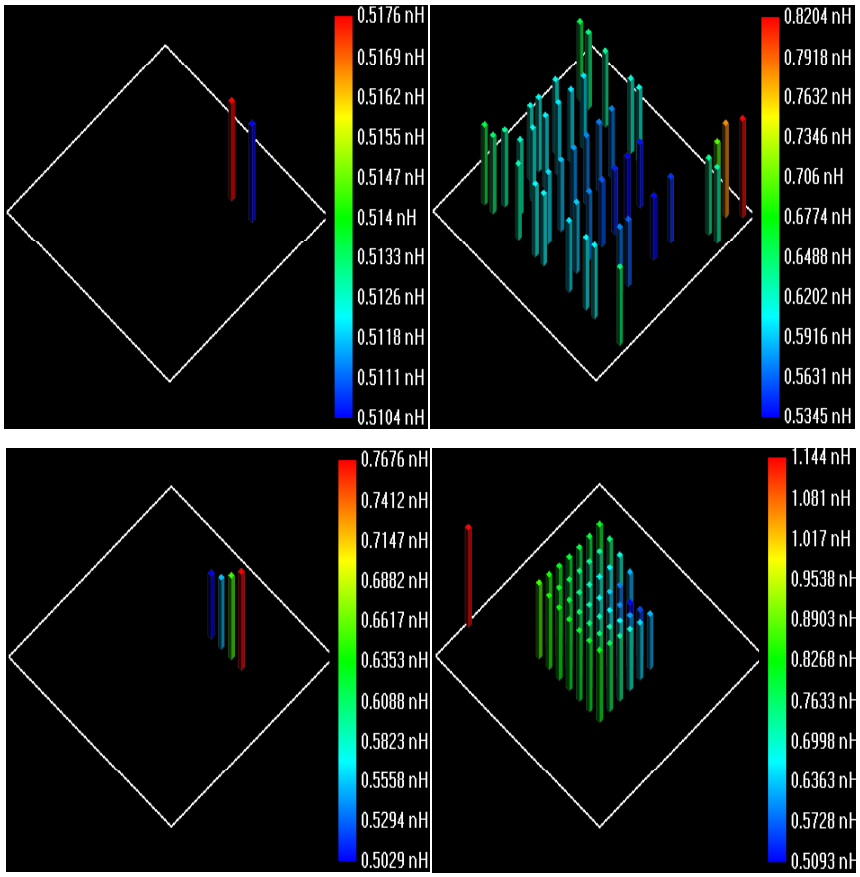
- Per pin-based properties --- Self loop inductance

- 6-layer flipchip package

VCC25A to GNDA



VCC25A to GND

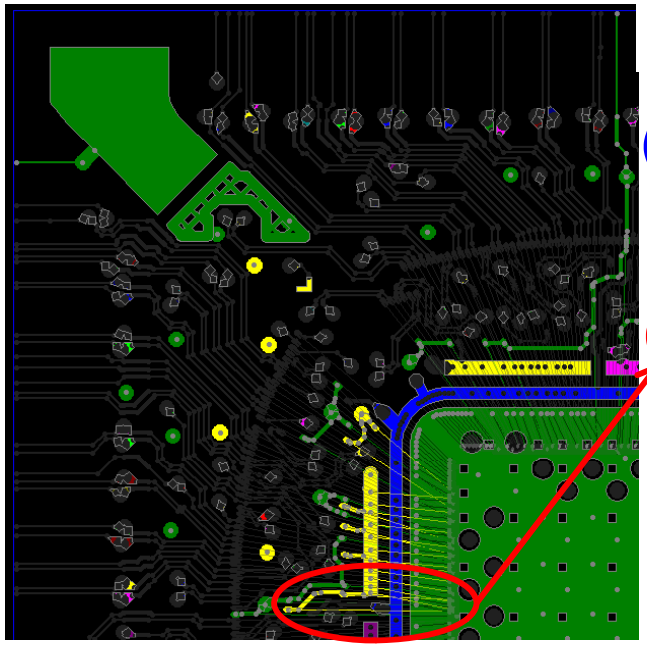


For the per-pin results, the lump inductance of VCC25A/GND should be smaller than VCC25A/GNDA.

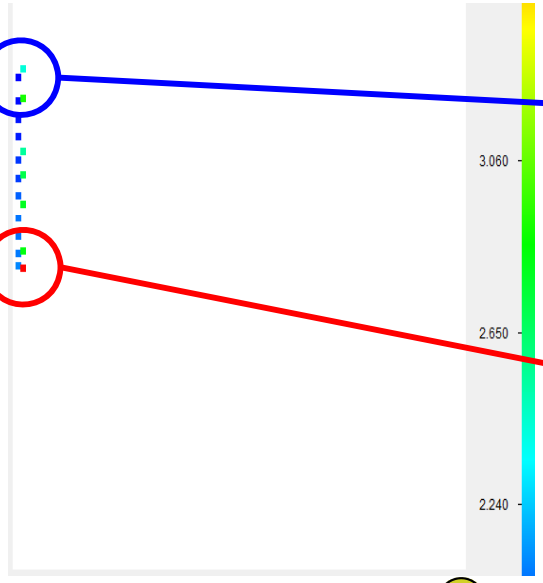
For P/G Analysis (Cont'd)

- Per pin-based properties --- "Total" loop inductance

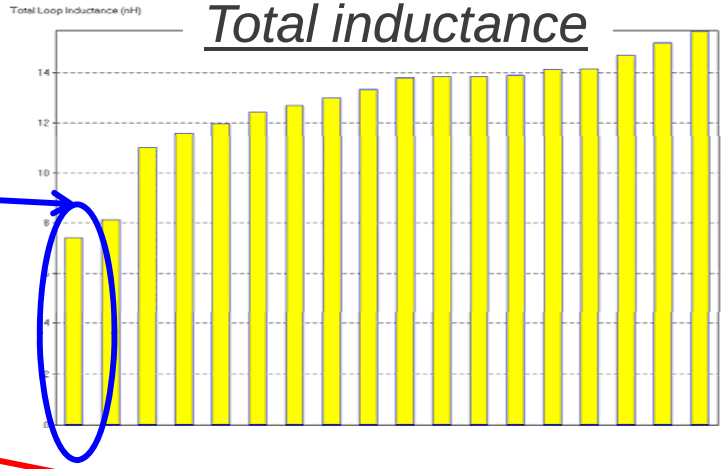
- Find the power pin with the lowest coupling



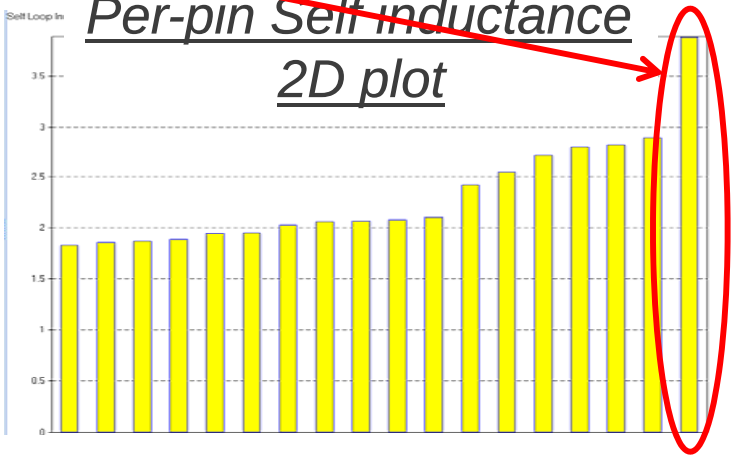
Per-pin Self inductance



Total inductance



Per-pin Self inductance 2D plot



Link the minimum loop inductance for the critical nets

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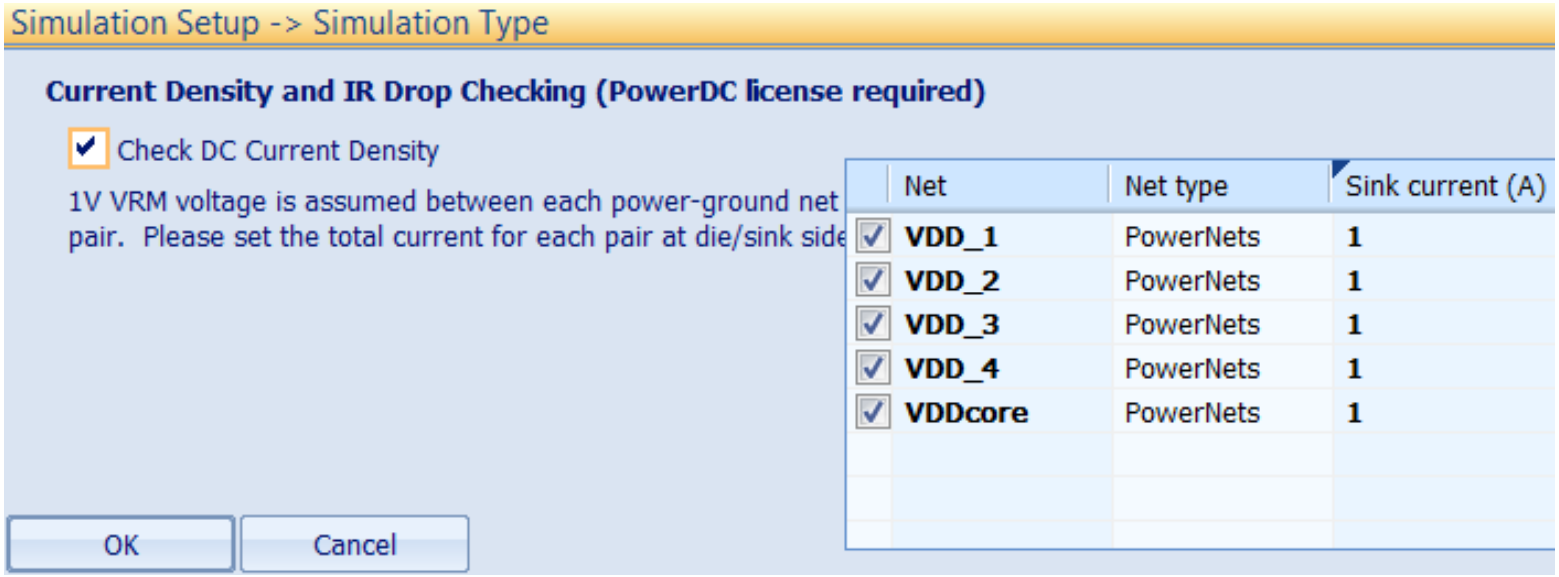
For DC Current Analysis (Cont'd)

- IR drop
  - Calculate IR drop on vias, traces and planes
  - Identify IR drop bottleneck area
- Current density
  - Calculate current density on vias, traces and planes
  - Identify high current density area that exceeds limit
  - Avoid regional over-heat caused by high current density

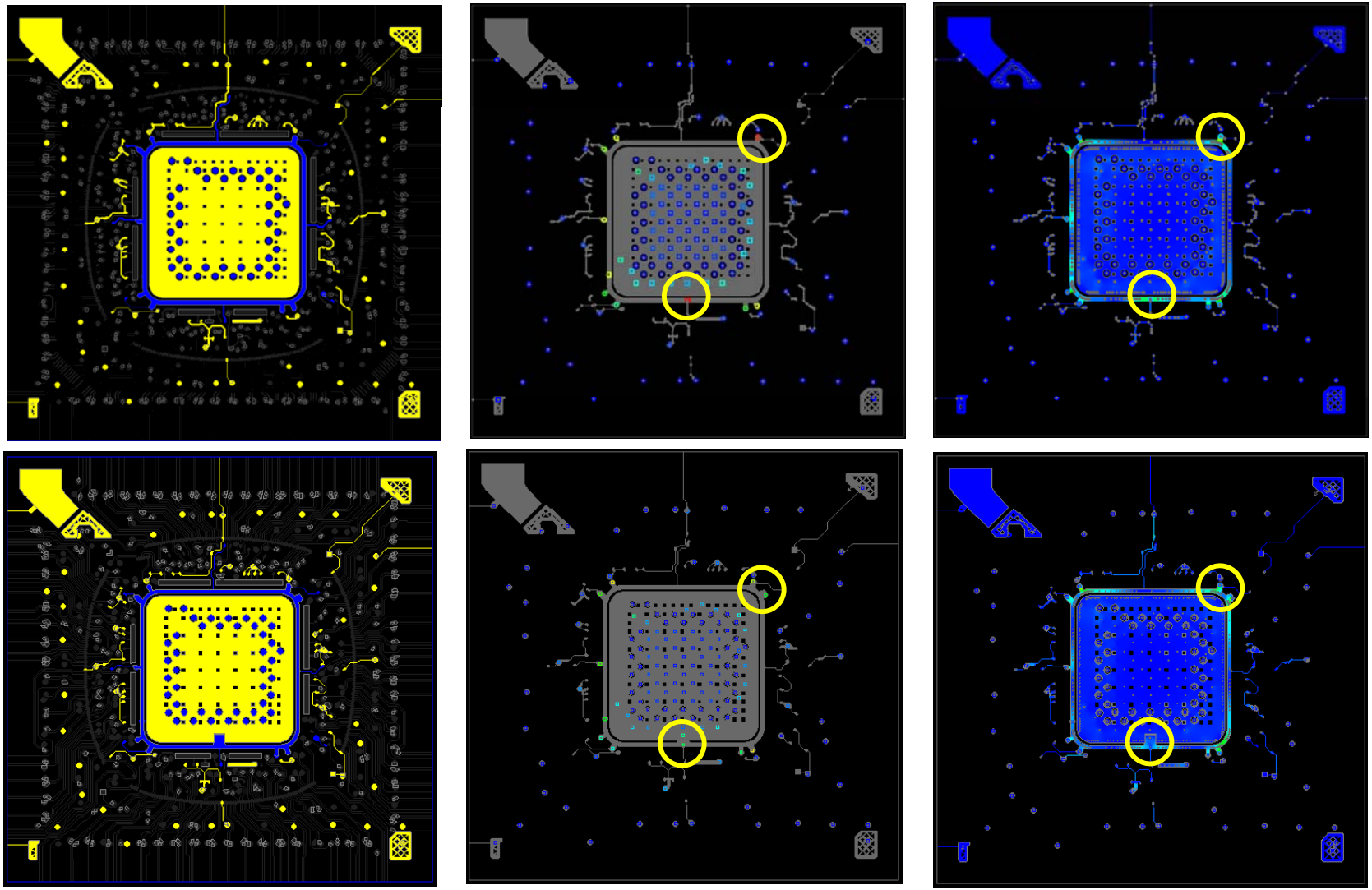


For DC Current Analysis (Cont'd)

- Check DC Current Density

- 4-layer wirebond package

Layout *Via current density* *Plane current density*

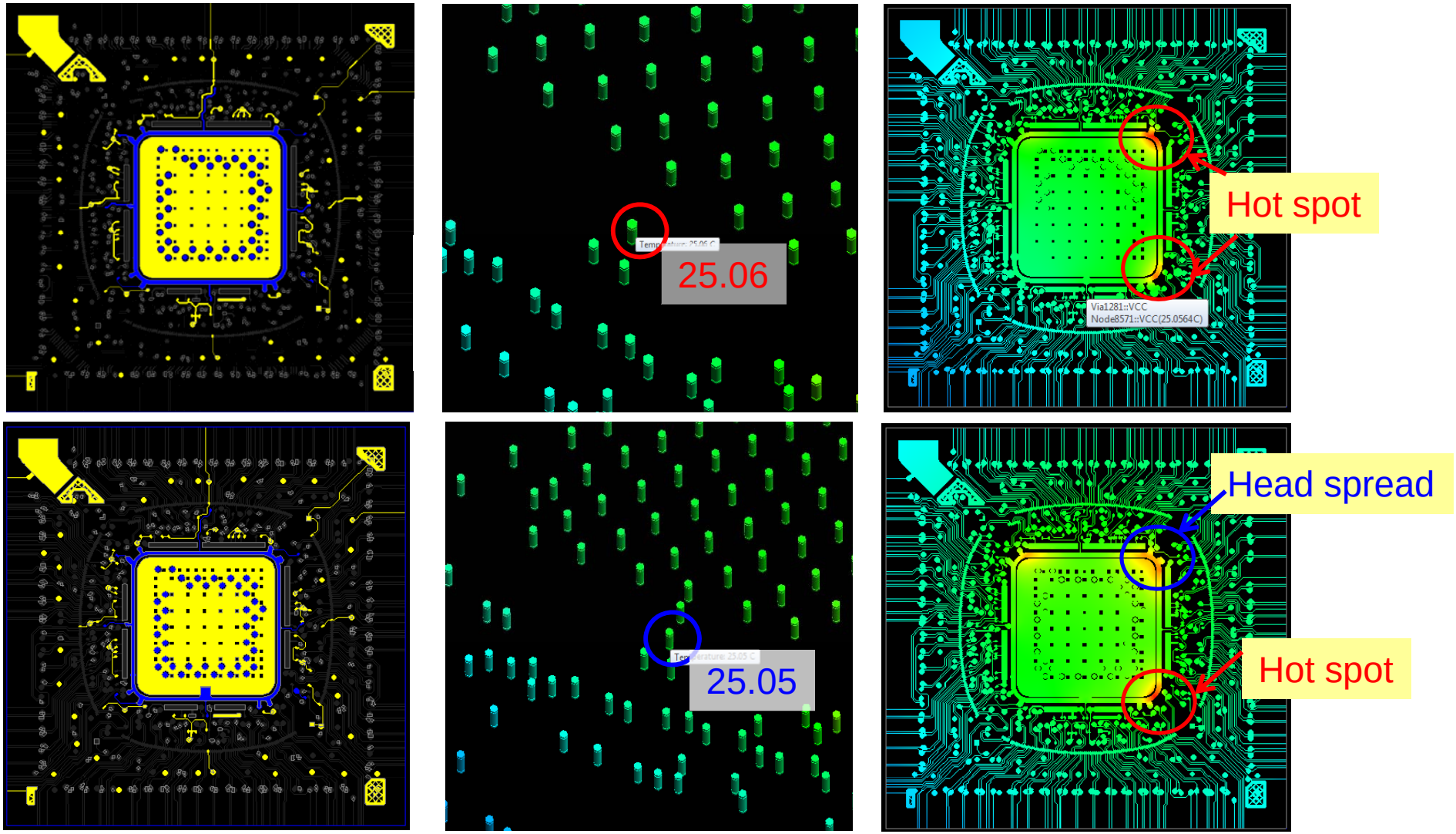


For DC Current Analysis (Cont'd)

- Check Thermal Effect (PowerDC)

- 4-layer wirebond package

Layout *Via temperature* *Plane temperature*



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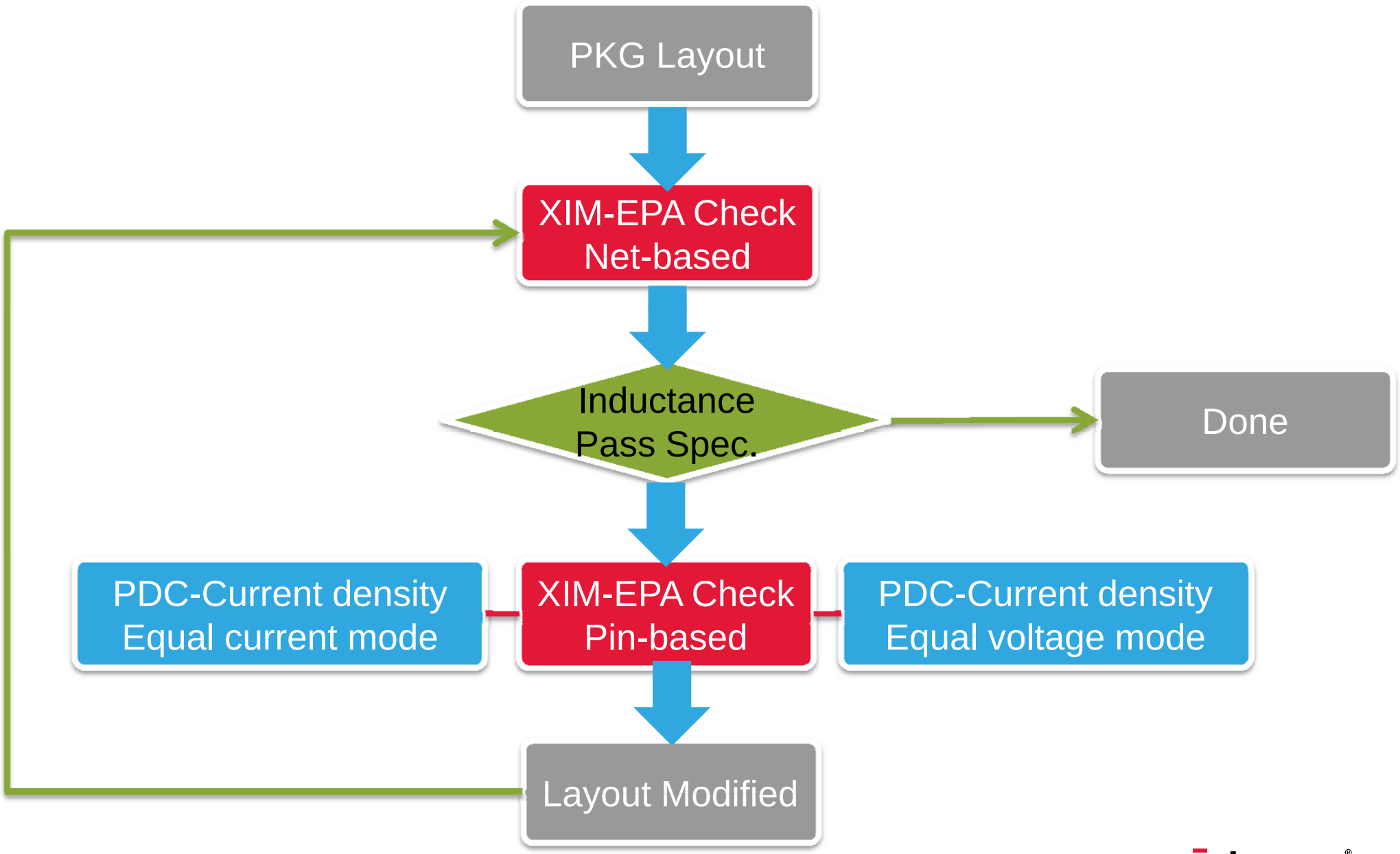
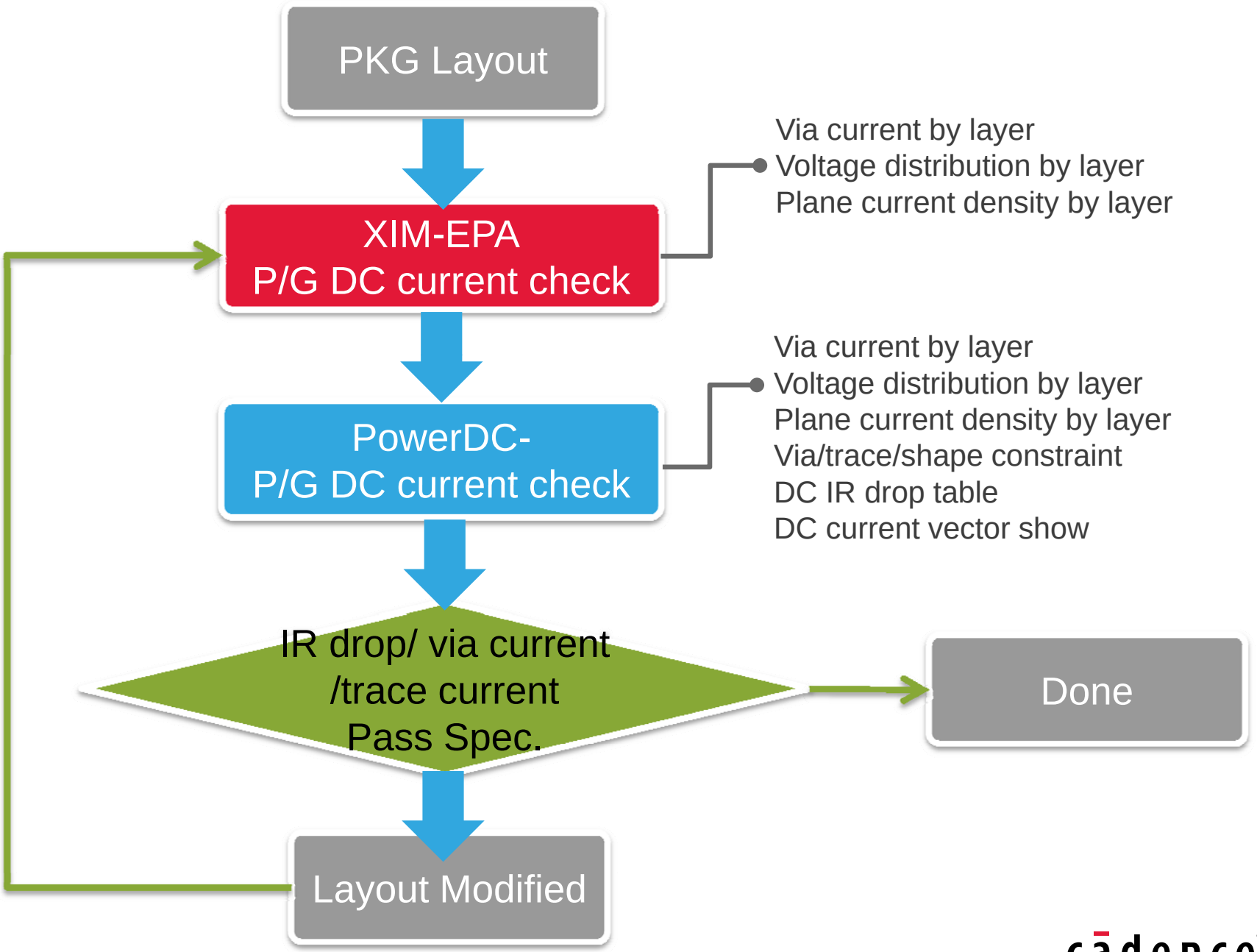
The P/G performance checking flow for AC field



The P/G performance checking flow for DC field

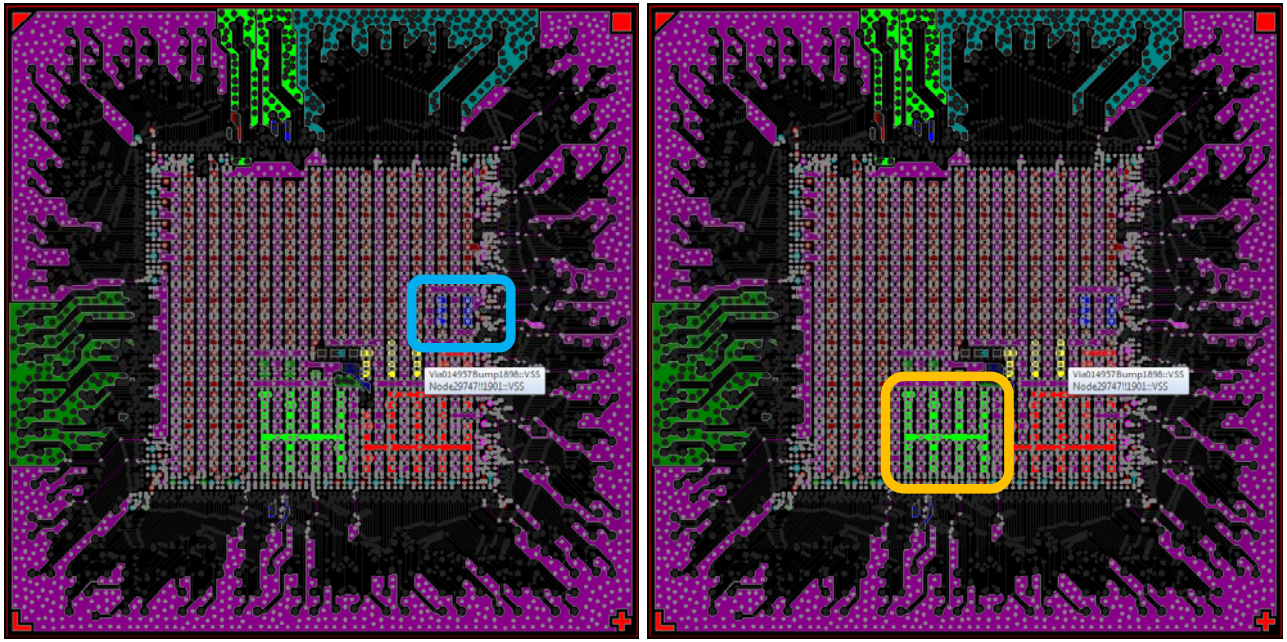


Step1 - Net based inductance checking

- 745L FCCSP 13.5x13.5mm 2+2+2 layers
  - Bump height: 90um (Sim.1); 40um (sim.2)
  - Simulation time – 5 mins

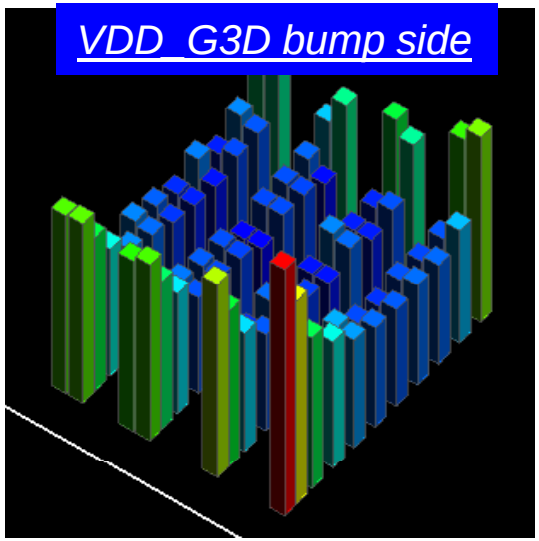
Net	VDD	VDD_AP	VDD_APMEM	VDD_DDR	VDD_G3D	VDD_ON
Spec.	3.5	18	80	130	20	50
Sim.1	5.0	23.8	84.2	161.2	27.7	56.9
Sim.2	4.9	23.1	81.0	156.7	26.8	53.4

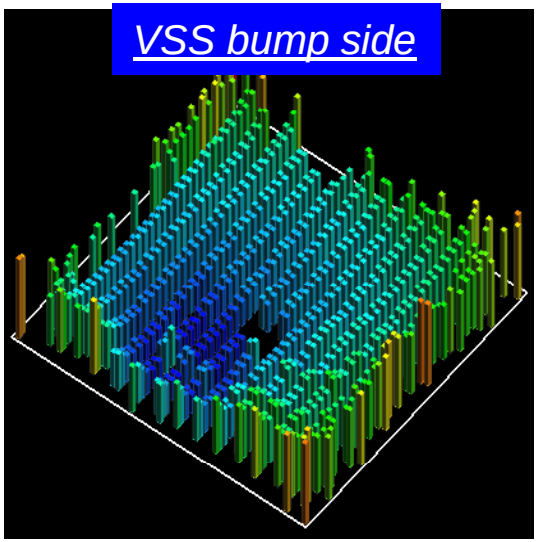
Unit:pH

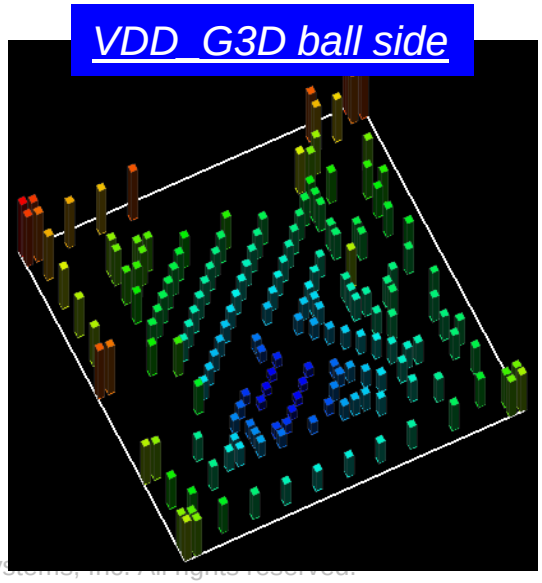


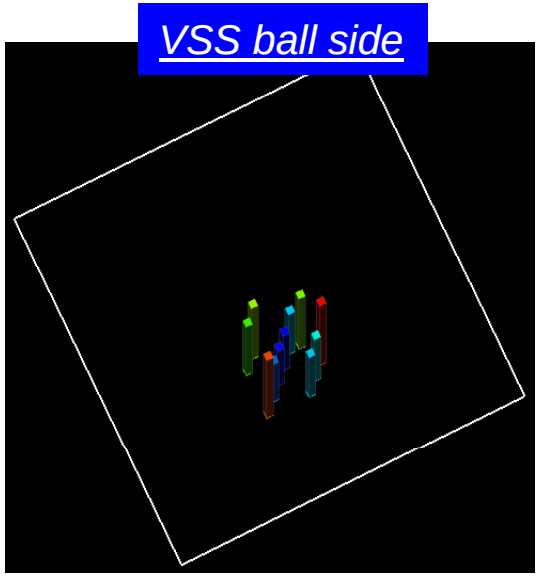
Step2 – Pin-based inductance checking

- VDD_G3D/VSS per pin-based properties
  - imulation time – 24 mins



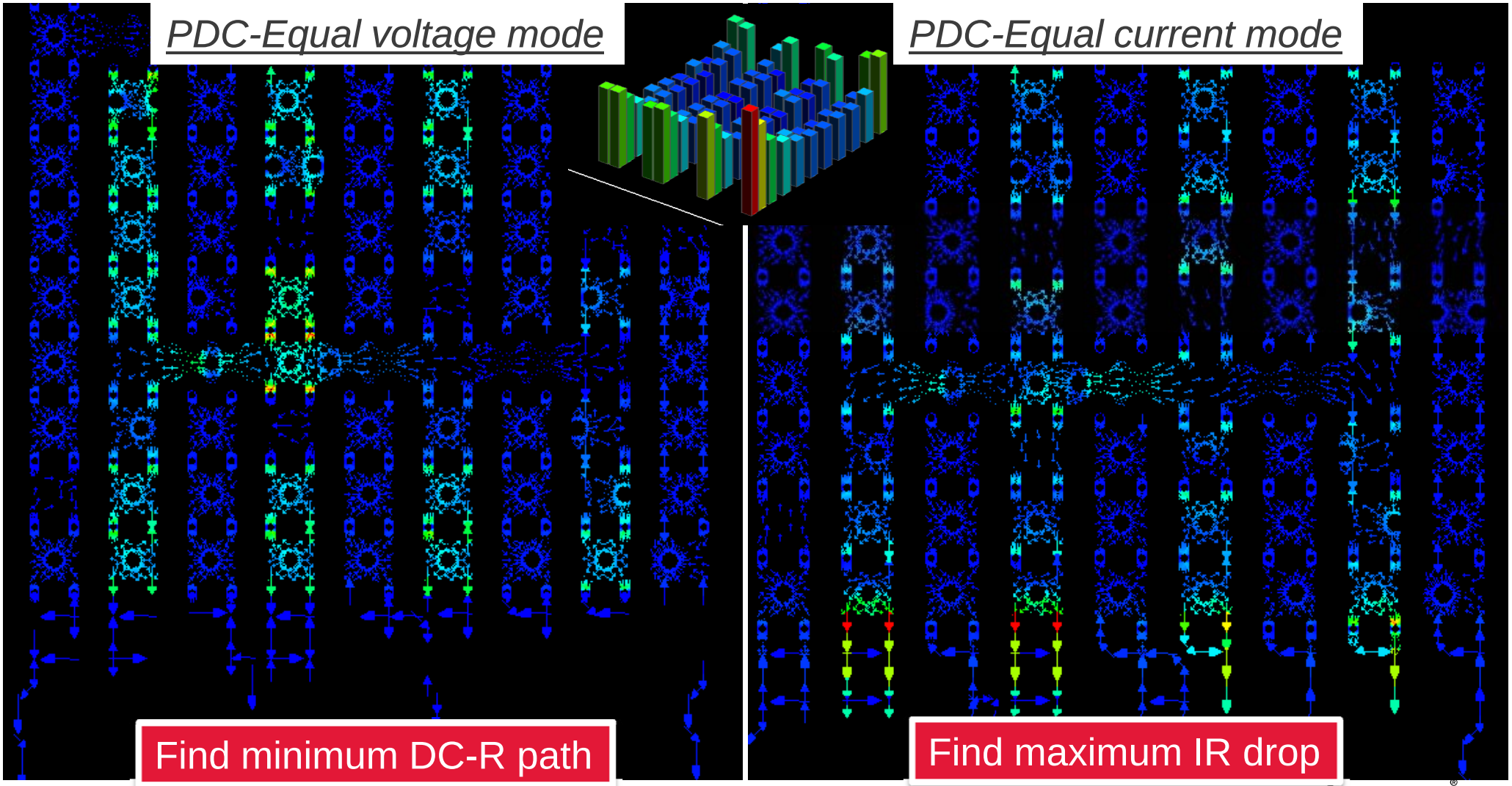






VDD_G3D/VSS DC current density plot

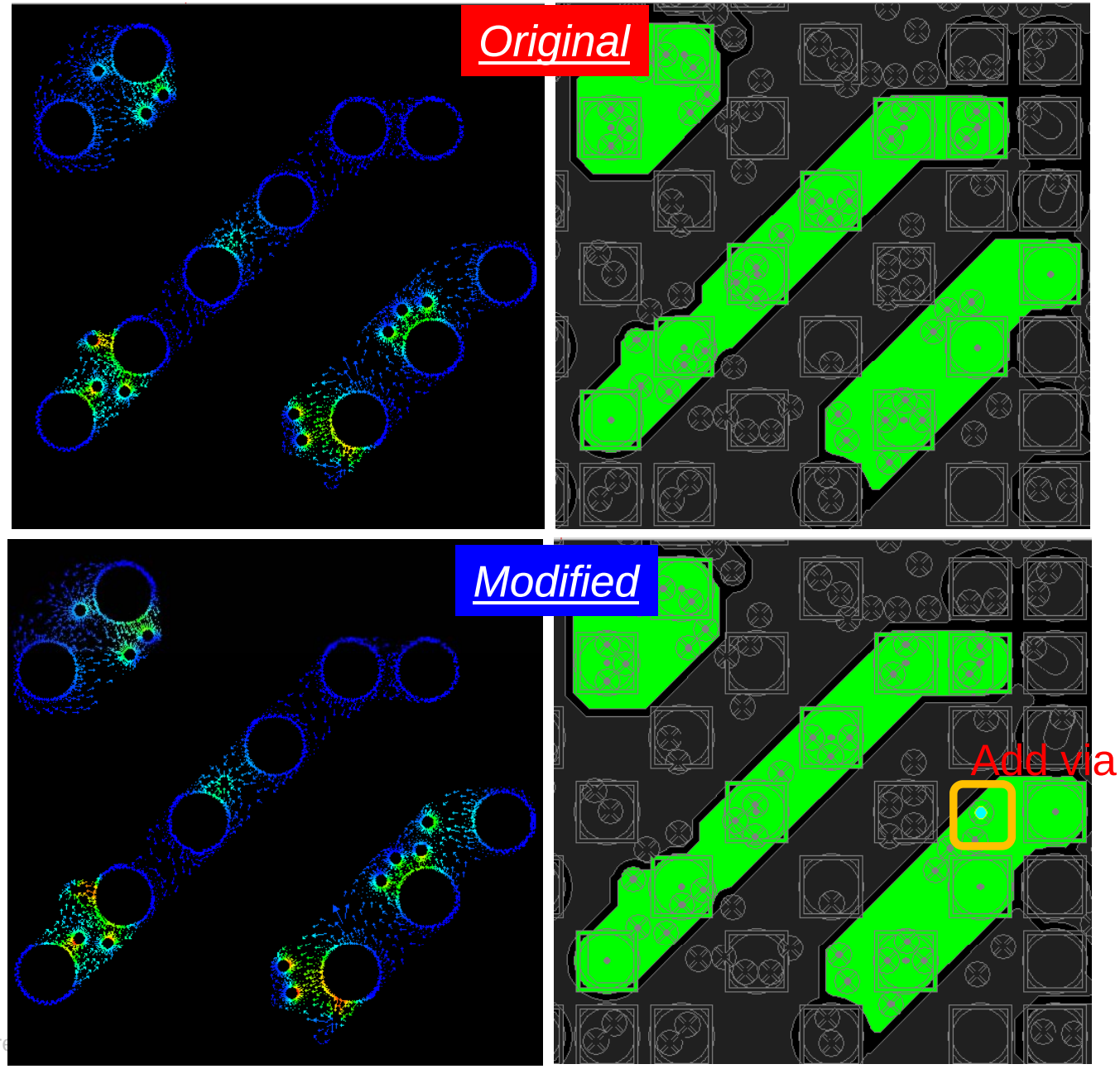
- DC current density plot checking
  - Simulation time – 24 mins



VDD_G3D/VSS DC current density plot

- PDC current plot
  - Simulation time – 2 mins

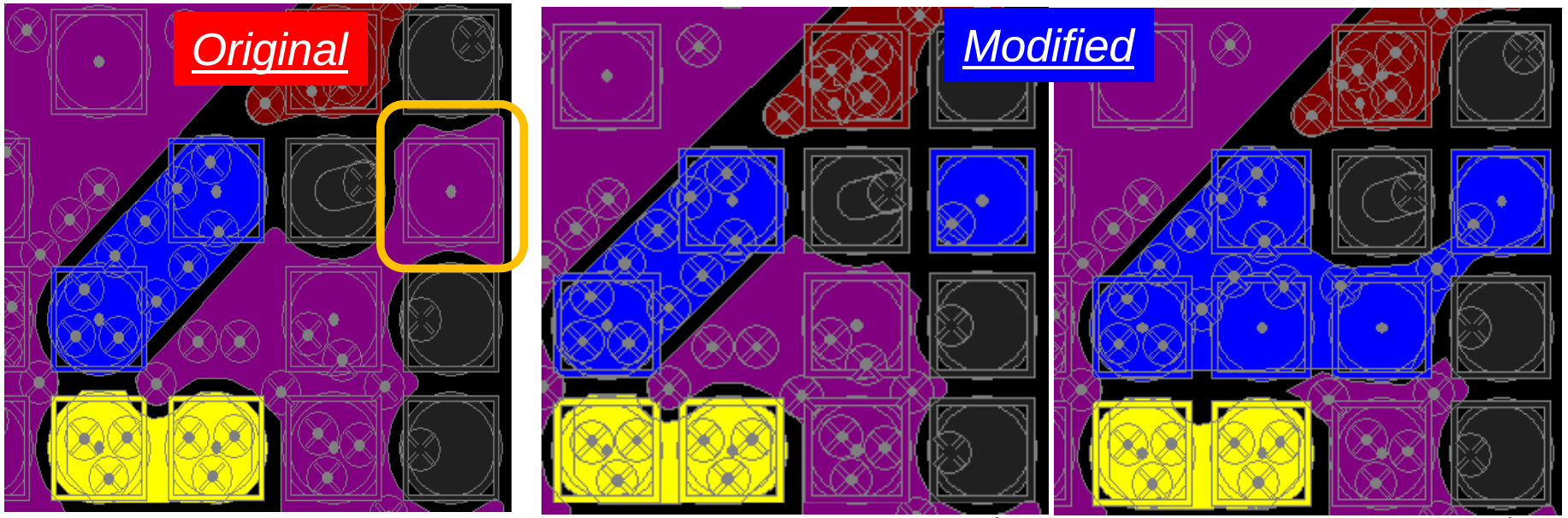
Net	VDD_G3D
Spec.	20pH
Sim.1	27.7
Sim.2 (Lower bump)	26.8
Sim.3 Add via with lower bump	26.7



VDD_DDR/VSS loop inductance reduction

- Add/Change VDD_DDR/VSS ball locations
  - Simulation time – 5 mins

Net	VDD_DDR
Spec.	130pH
Sim.1	161.2pH
Sim.2 (lower bump)	156.7pH
Sim.3	122.8pH
Sim.4	111.7pH



Agenda

- Package Performance Checking Challenge
- Allegro Sigrity Integration for Package Checking Flow
- Package Performance Checking Items-
  - ❑Impedance / Trace Timing
  - ❑Power/Ground Inductance
  - ❑Power/Ground Current Density
  - ❑Thermal Effect
- ASE Case Studied Results & ASI Live Demo
- Summary

Summary

- Allegro + Sigrity enables seamless physical and electrical design flow
  - Easy for use
  - Well layout version control for simulation
  - Fast for simulation

- Fast to find and optimize potential risk
  - Impedance/ Trace Timing
  - Power/Ground Inductance
  - Power/Ground Current Density
  - Thermal Effect
  - …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