

Power Integrity

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Acknowledgement

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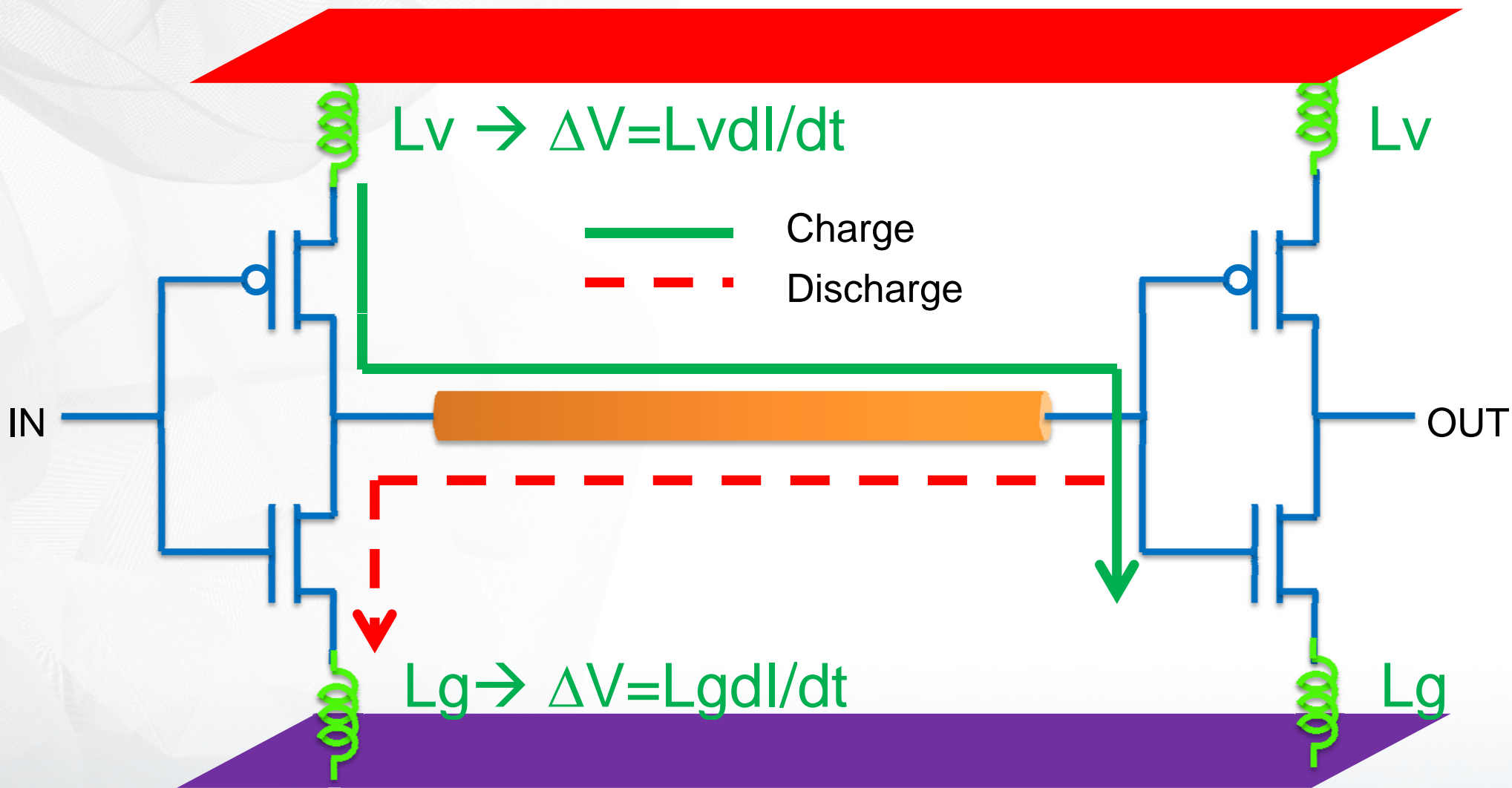
The author would like to specially thank Dr. Ching Ku Liao, who works for MediaTek, for many useful advises in EM and transient co-simulation

Acknowledgement

感謝映陽科技林有俊先生與陳志忠先生在軟體設定與安裝上的諸多協助

The author would like to specially thank Christ Lin and Eric Chen, who work for Graser, for many kindly help in Sigrity Installation and Settings.

Root Cause of PI

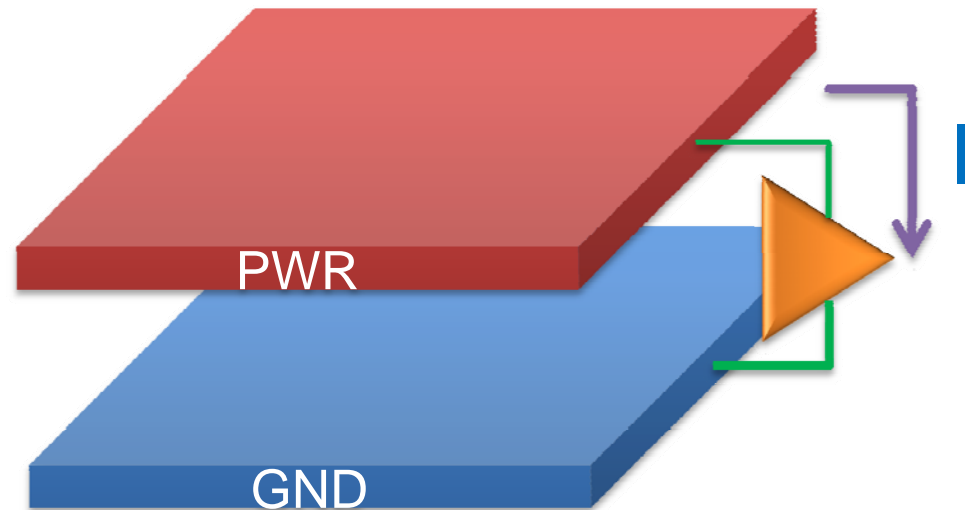
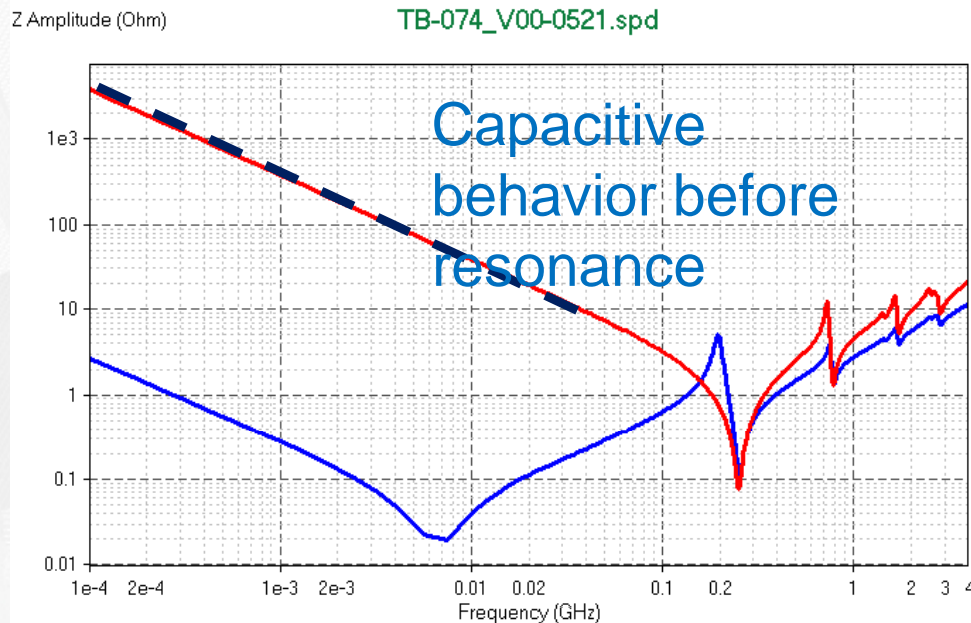


CPU/DSP/Switching chip are the class of **low-voltage high current** applications

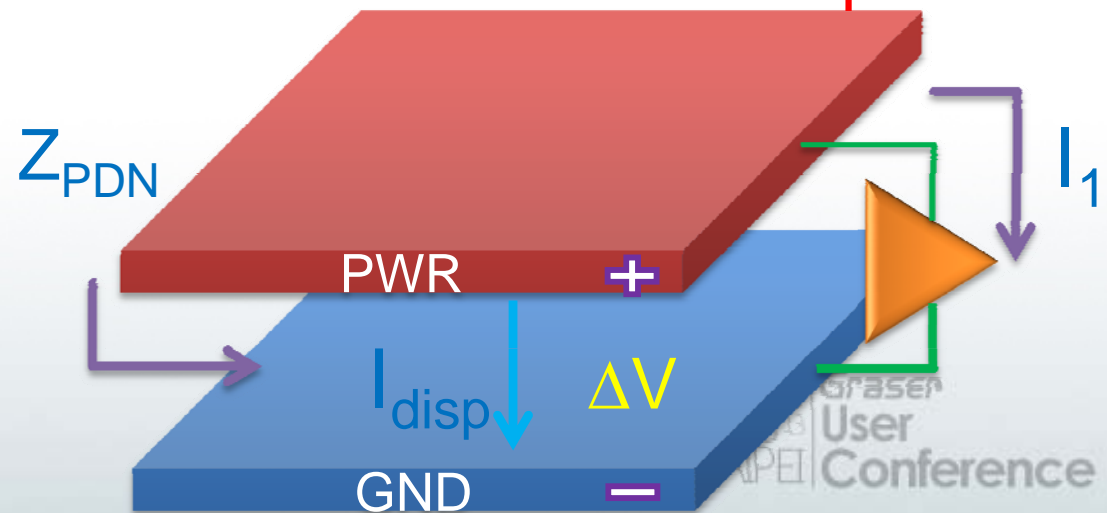
Z-Profile of PWR/GND Planes

Value goes to infinity at DC

@ DC → Open

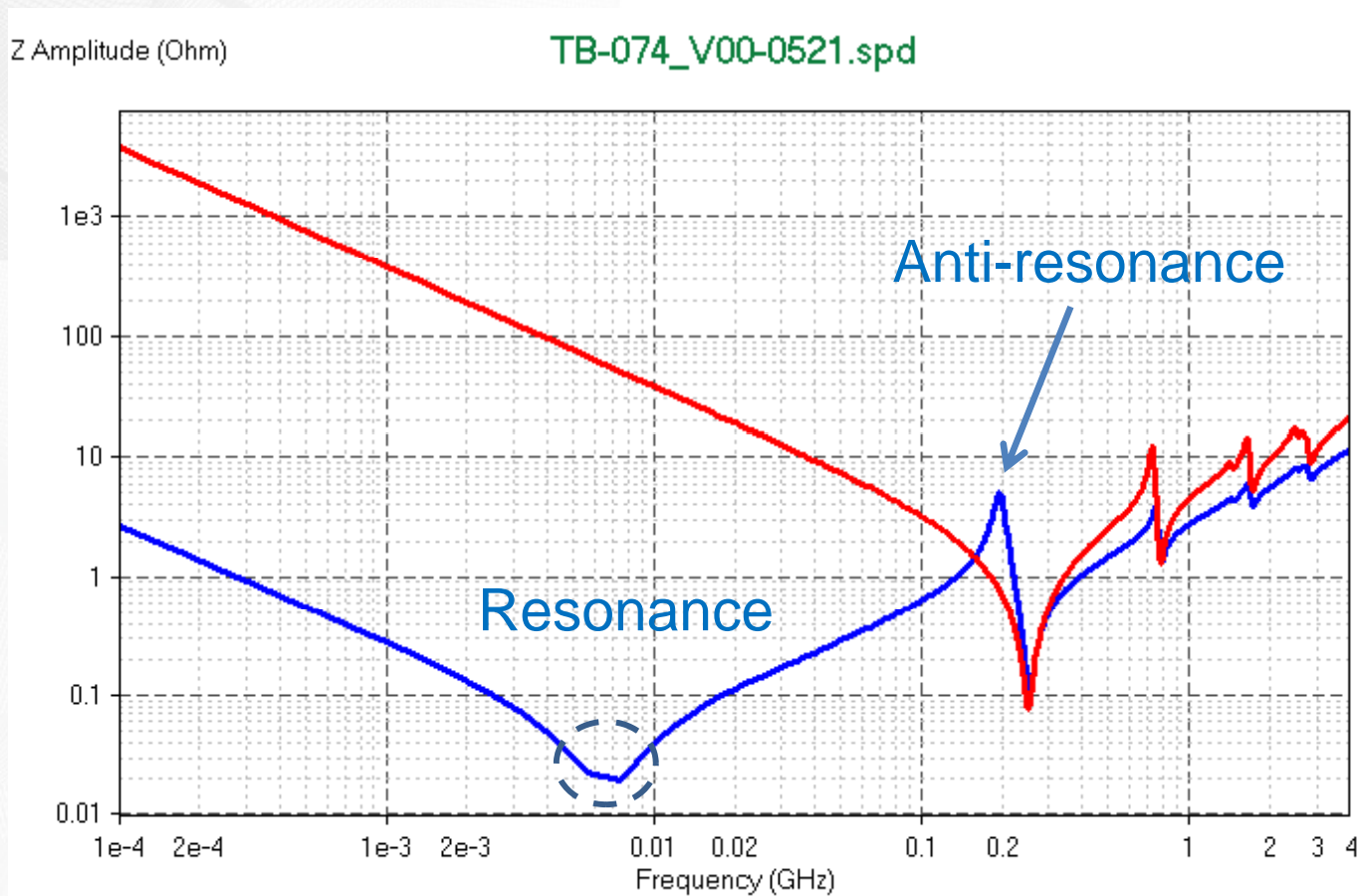


@ HF → Behave as capacitive



$$\begin{aligned}
 V(f) &= I(f) \times Z(f) \\
 &= \underbrace{I \times Z_{DC}}_{V_{dd}} + \underbrace{I_1 Z_{PDN @ HF}}_{\pm 5\% V_{dd}}
 \end{aligned}$$

Resonance/Anti-resonance



$$Z = \frac{V}{I}$$

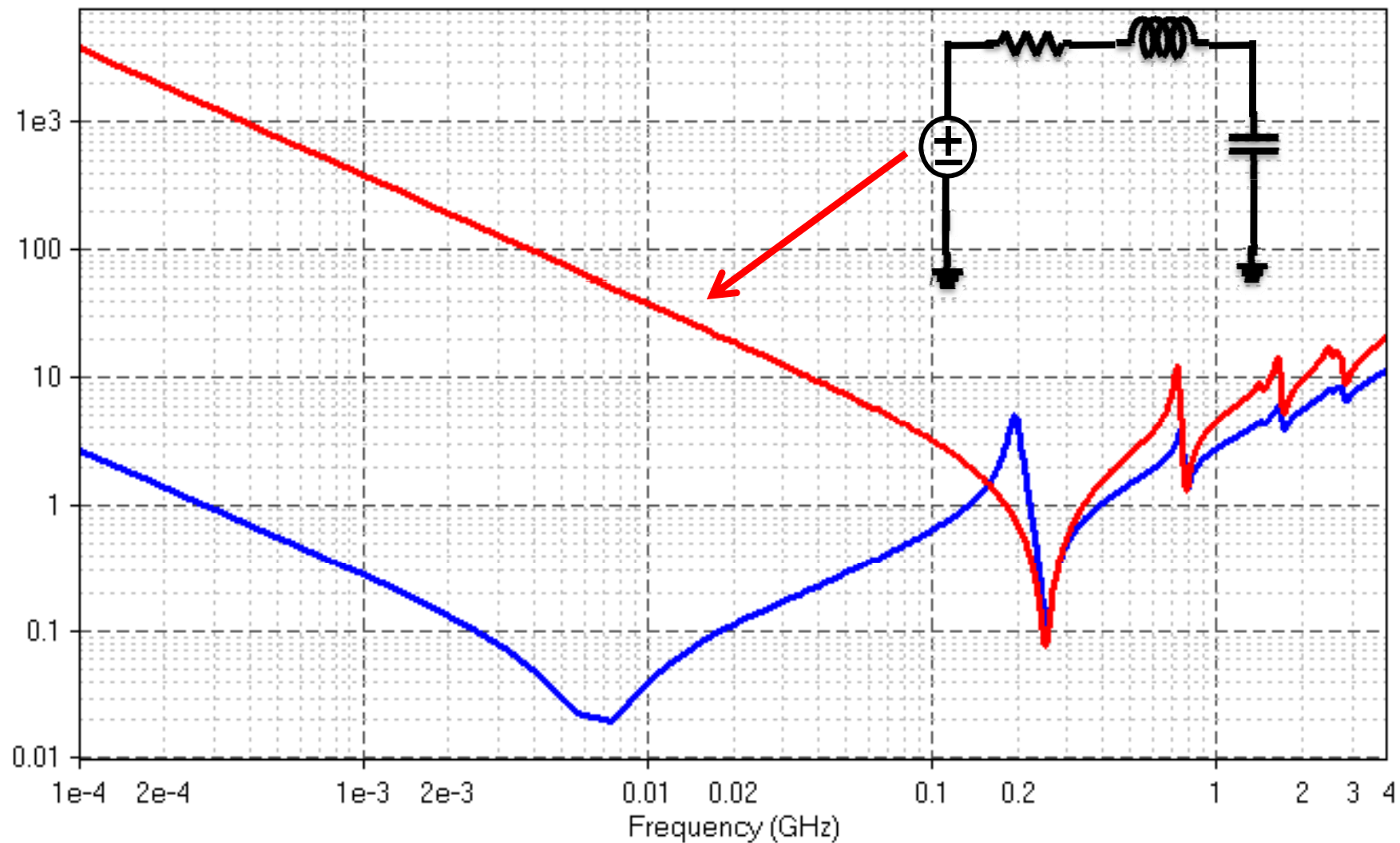
Resonance → Z approaches to zero
no matter how large the current is, there is no voltage drop
→ No reliability issue

Anti-resonance → Z approaches to infinity
Even very small current will drive an huge voltage drop
→ Reliability issue

Equivalent Ckt of PDN

Z Amplitude (Ohm)

TB-074_V00-0521.spd



Target Impedance Estimation

- From the data sheet of the switching circuit, the consumed power and applied voltage are usually given, hence

$$I_{\max} = \frac{P}{V}$$

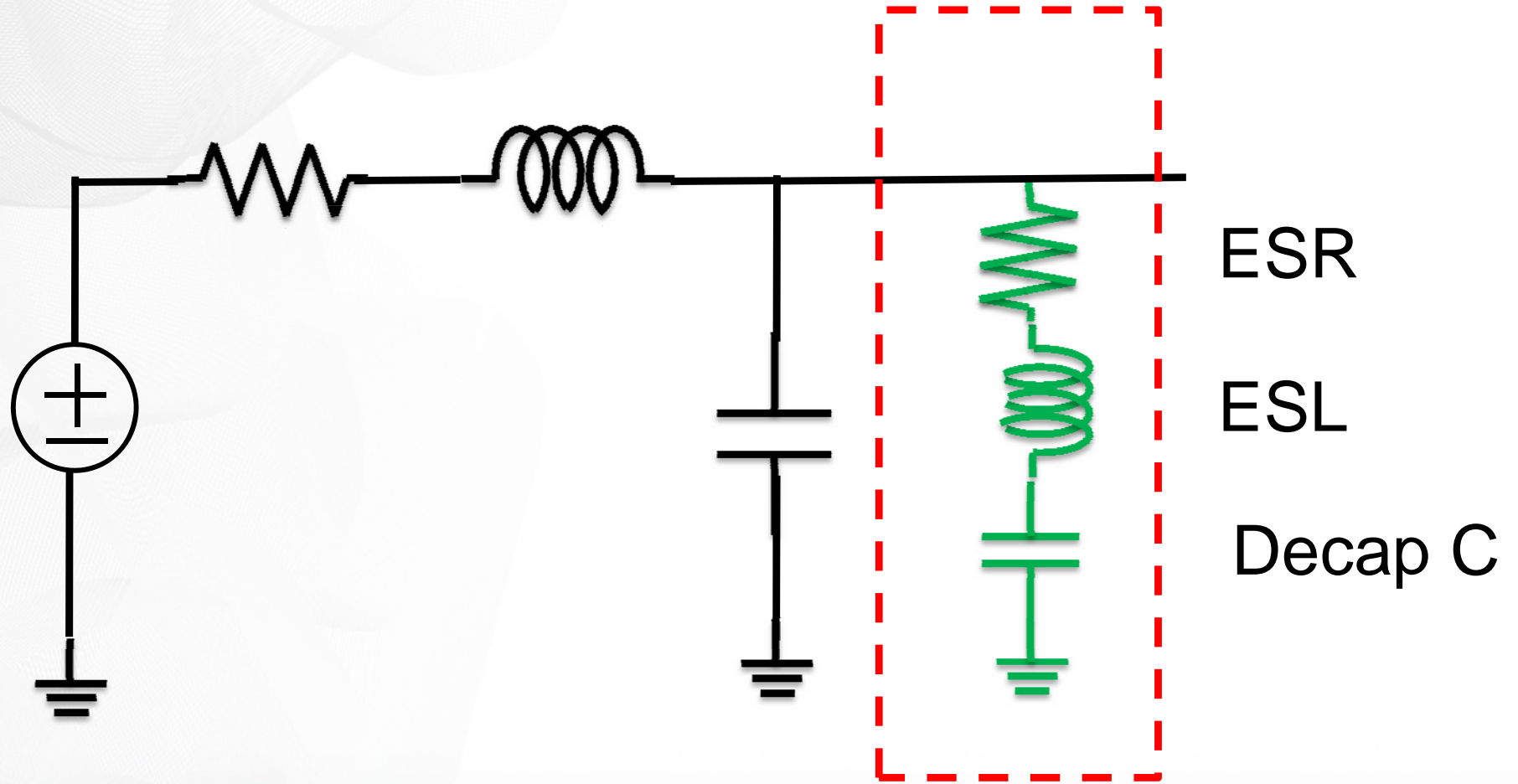
- The average current is assumed to be 50% of the maximum current, then

$$Z_T = \frac{V_{dd} \times \text{ripple}}{50\% \times I_{\max}}$$

Bypass/Decoupling Capacitors

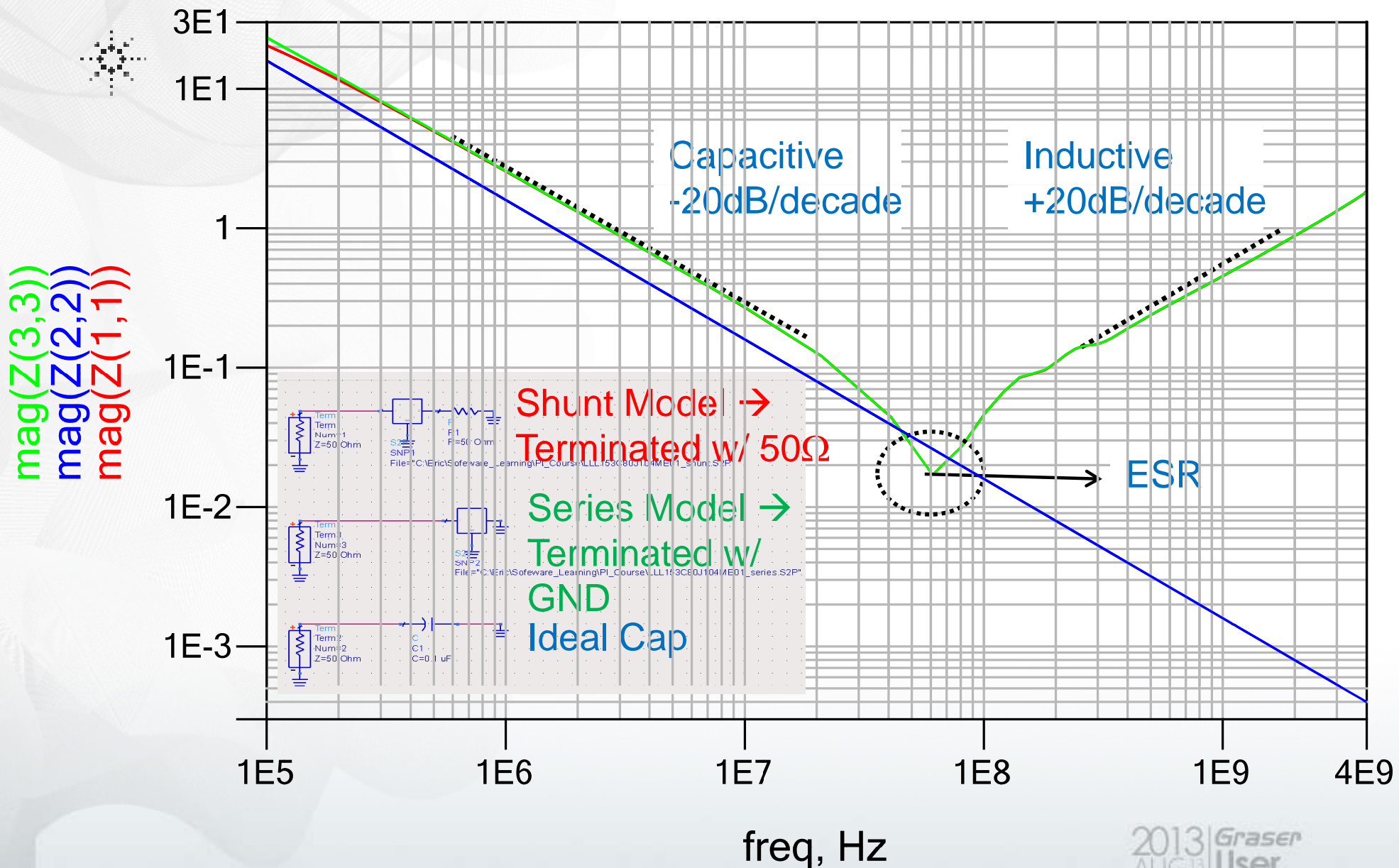
- Switching circuit requires current to charge the load
- If the output impedance is too high, then VRM is unable to respond well (VRM output impedance exceeds the desired impedance)
- External capacitors store charge. They bypass the VRM and supply the current to the switching circuit
- The bypass capacitors are also called decoupling capacitors (decouple the VRM from the switching circuit)

ESR & ESL of the Decoupling Capacitor



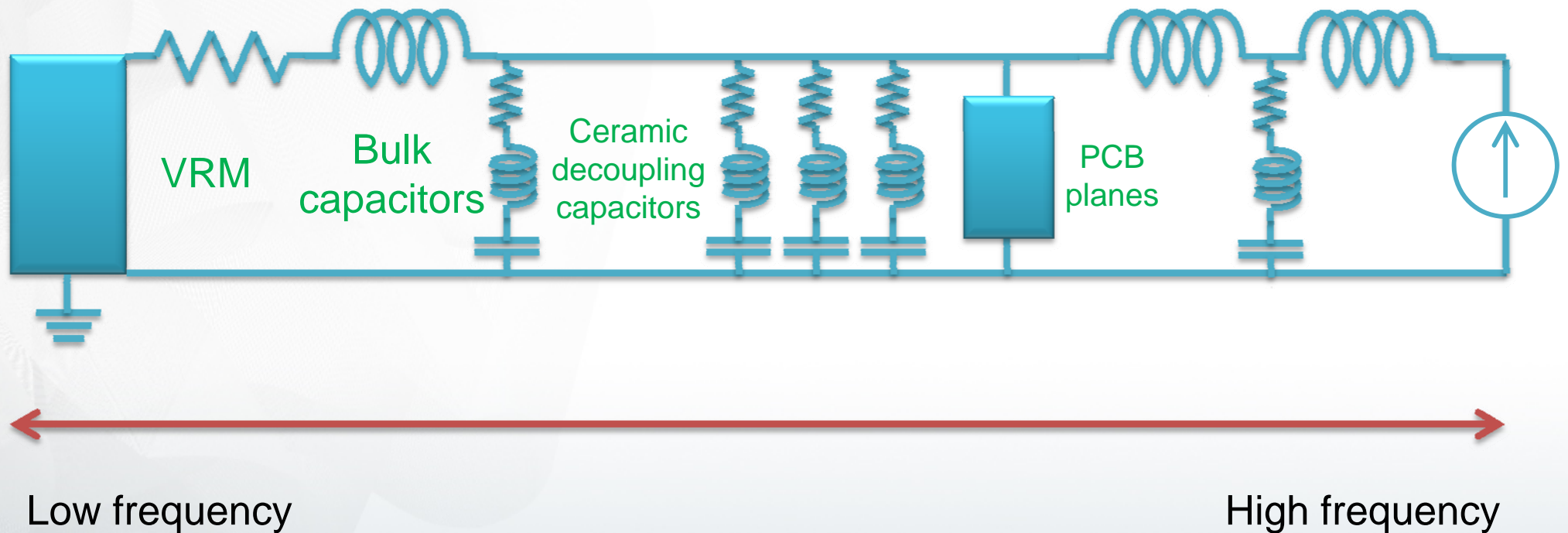
Equivalent circuit of
decoupling capacitor

Z-Profile of Decoupling Capacitor



Decoupling Capacitors

- Decouple the VRM from the switching circuit
 - Provides a low impedance path



Ultra Low Impedance Measurement

- 1-Port Measurement

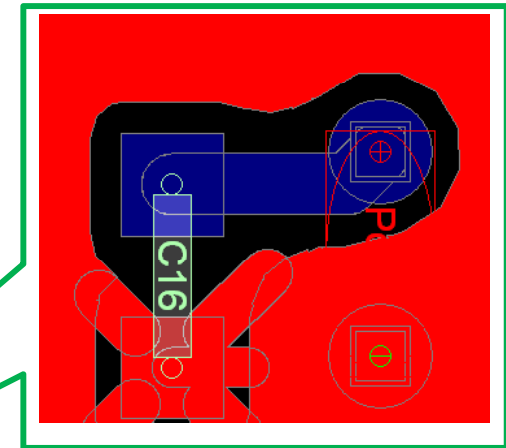
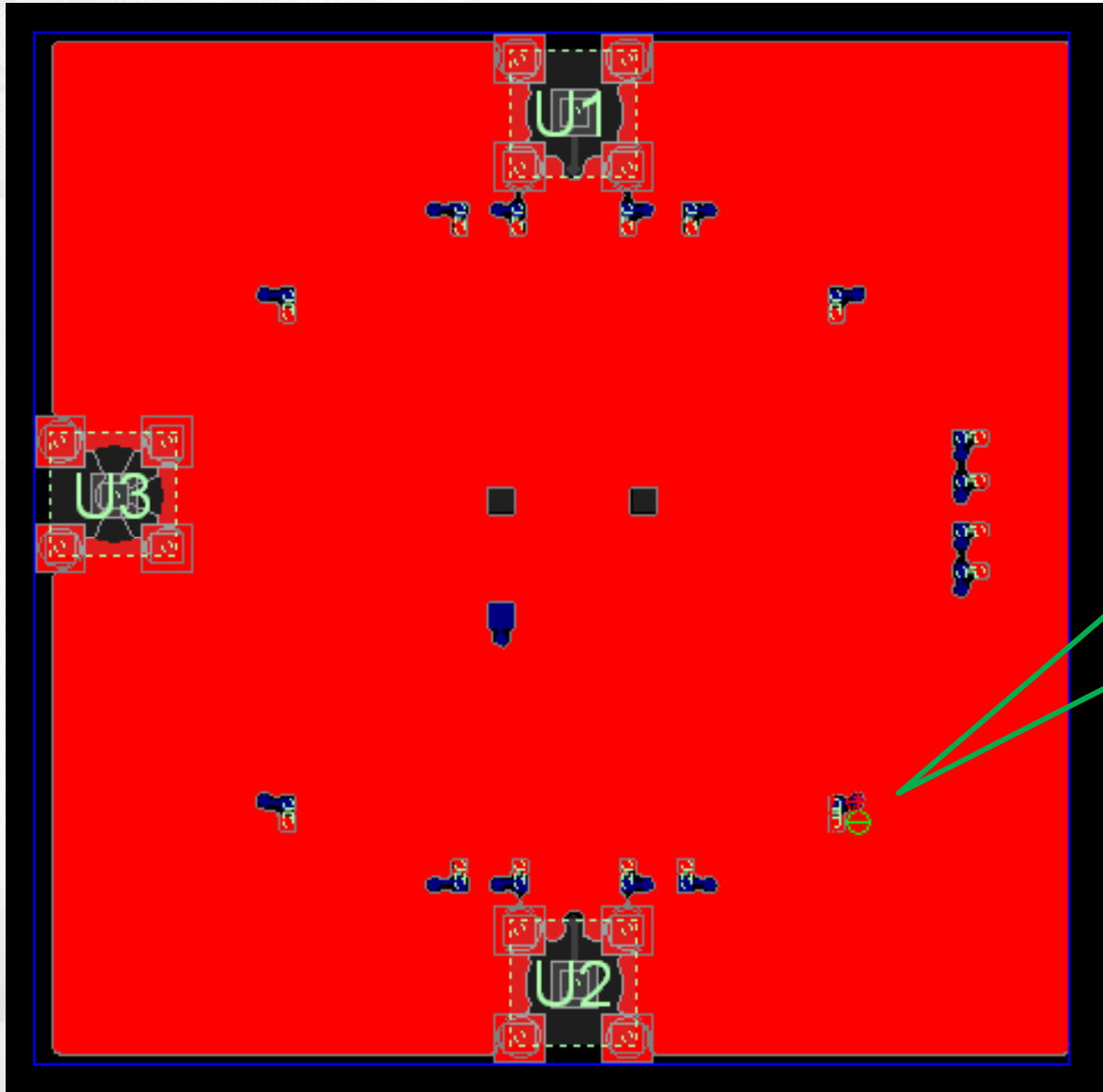
$$Z = \left(\frac{1 + S_{11}}{1 - S_{11}} \right) Z_0$$

Impedance of PDN is usually much smaller than 50Ω
 $\rightarrow |S_{11}| \approx 1$
It makes the Z cannot be slow enough

- 2-Port Measurement

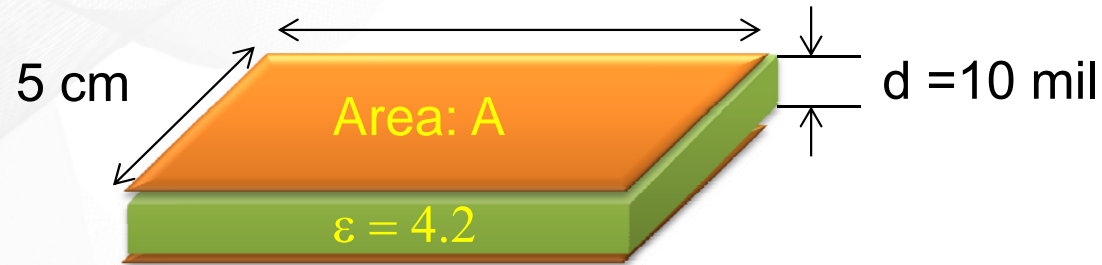
$$Z_{11} = 25 \times \left(\frac{S_{12}}{1 - S_{12}} \right)$$

Example 1



Calculated Z-Profile

Bare board

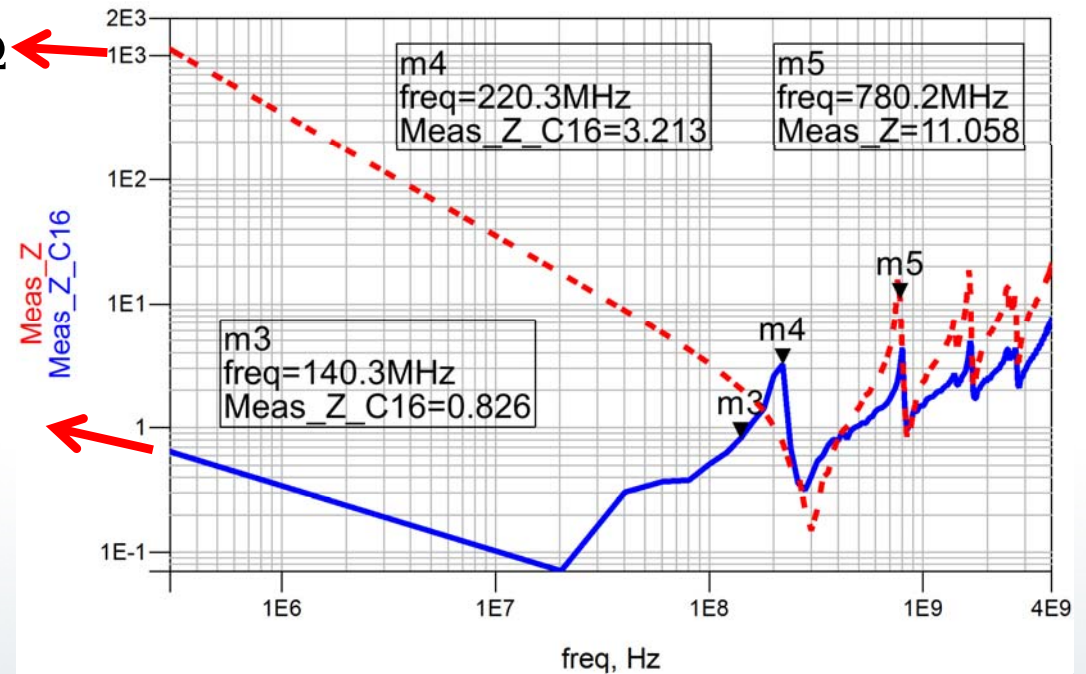


$$C = \epsilon_0 \epsilon_r A / d = 8.854 \cdot 10^{-12} \text{ F/m} \cdot 4.2 \cdot 0.05^2 \text{ m}^2 / (10/40 \cdot 10^{-3} \text{ m}) = 372 \text{ pF}$$

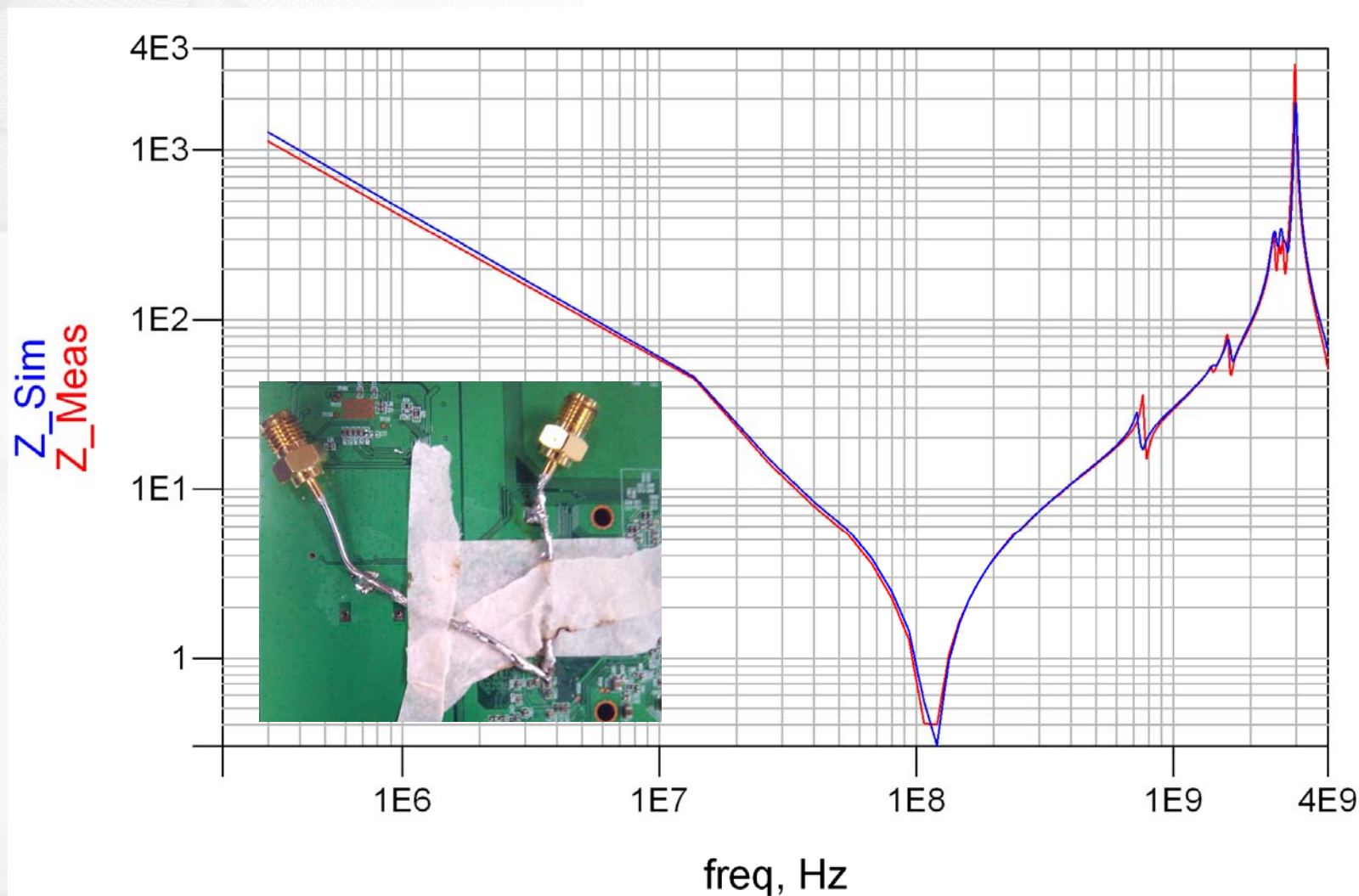
At 300 kHz, $Z_c = 1/(\omega C) = 1.426 \cdot 10^3 \Omega$

De-Cap: 1uF

At 300 kHz, $Z_c = 1/(\omega C) = 0.5305 \Omega$



Measurement: Bare Board

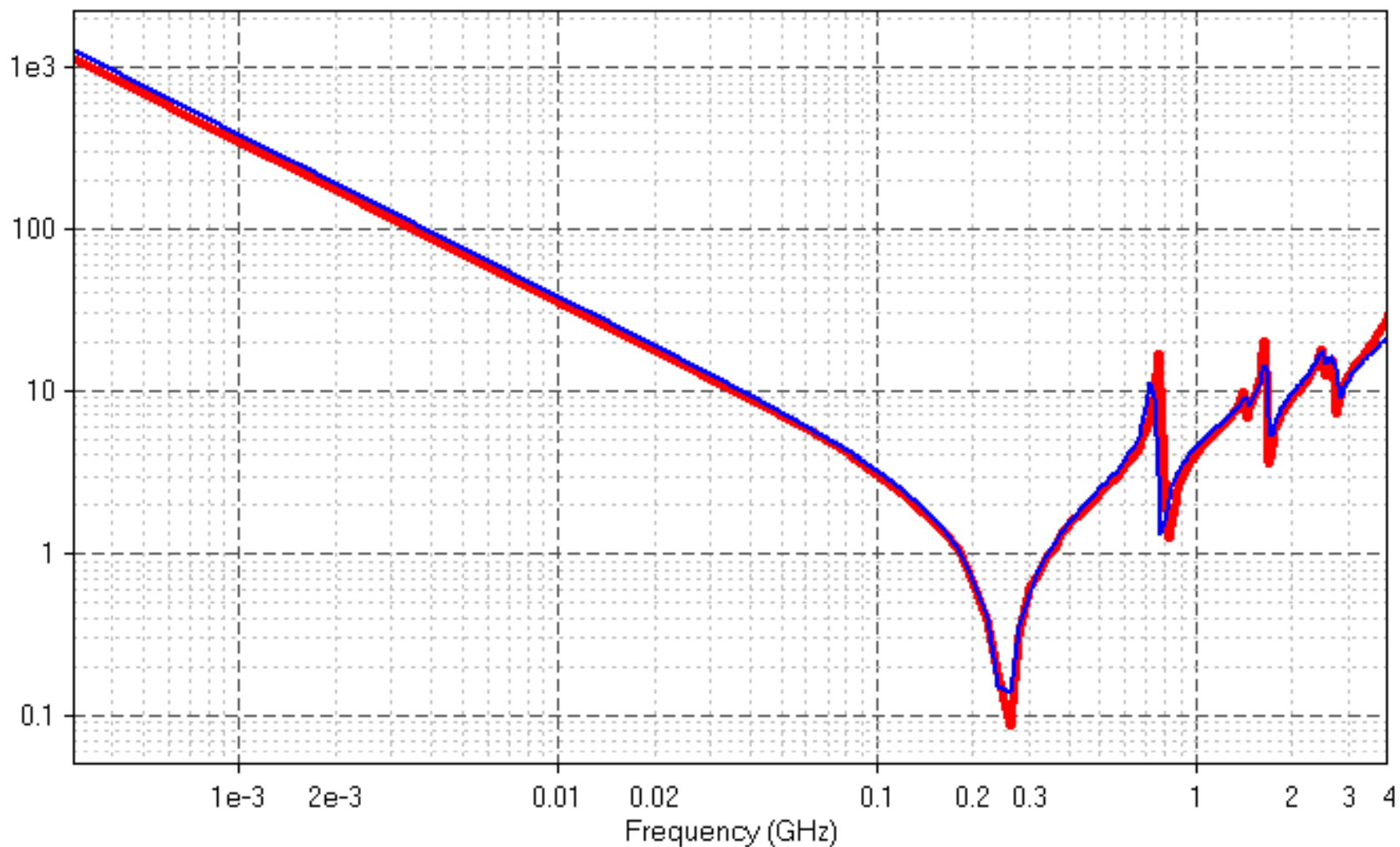


Simulation w/ transmission line effect

Measurement: Bare Board De-embedded

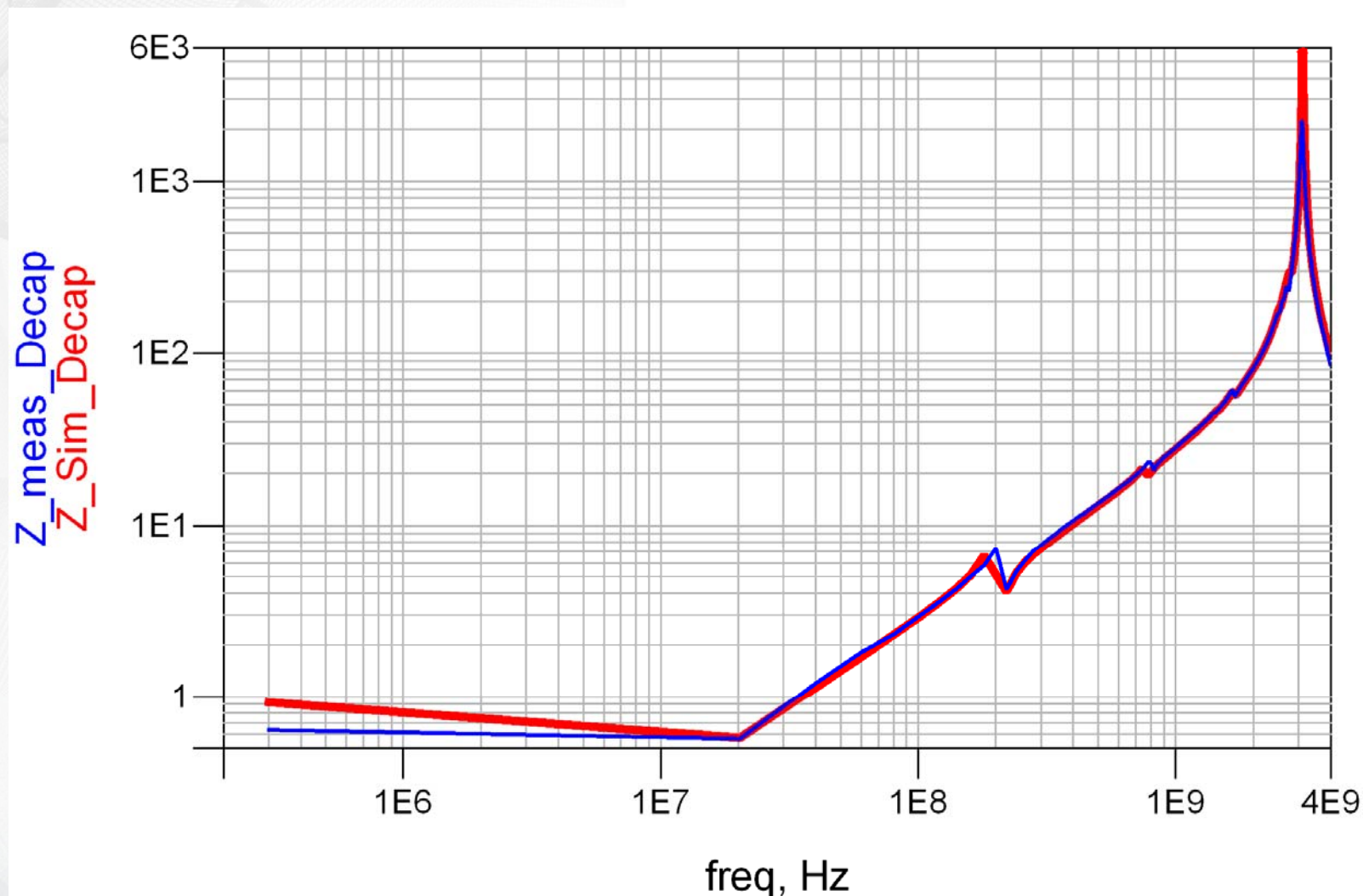
Z Amplitude (Ohm)

TB-074_V00-0521_noDecap.spd



— D:\Sigirty_Course\David_TestBoard\VC16_bare_Deembedded.slp - Z1[1,1] - Z(1:1:, 1:1:)
— SIMULATION - Z0[1,1] - Z(1:Port1::VCC_LAYER3, 1:Port1::VCC_LAYER3)

Measurement: Board W/ Decap

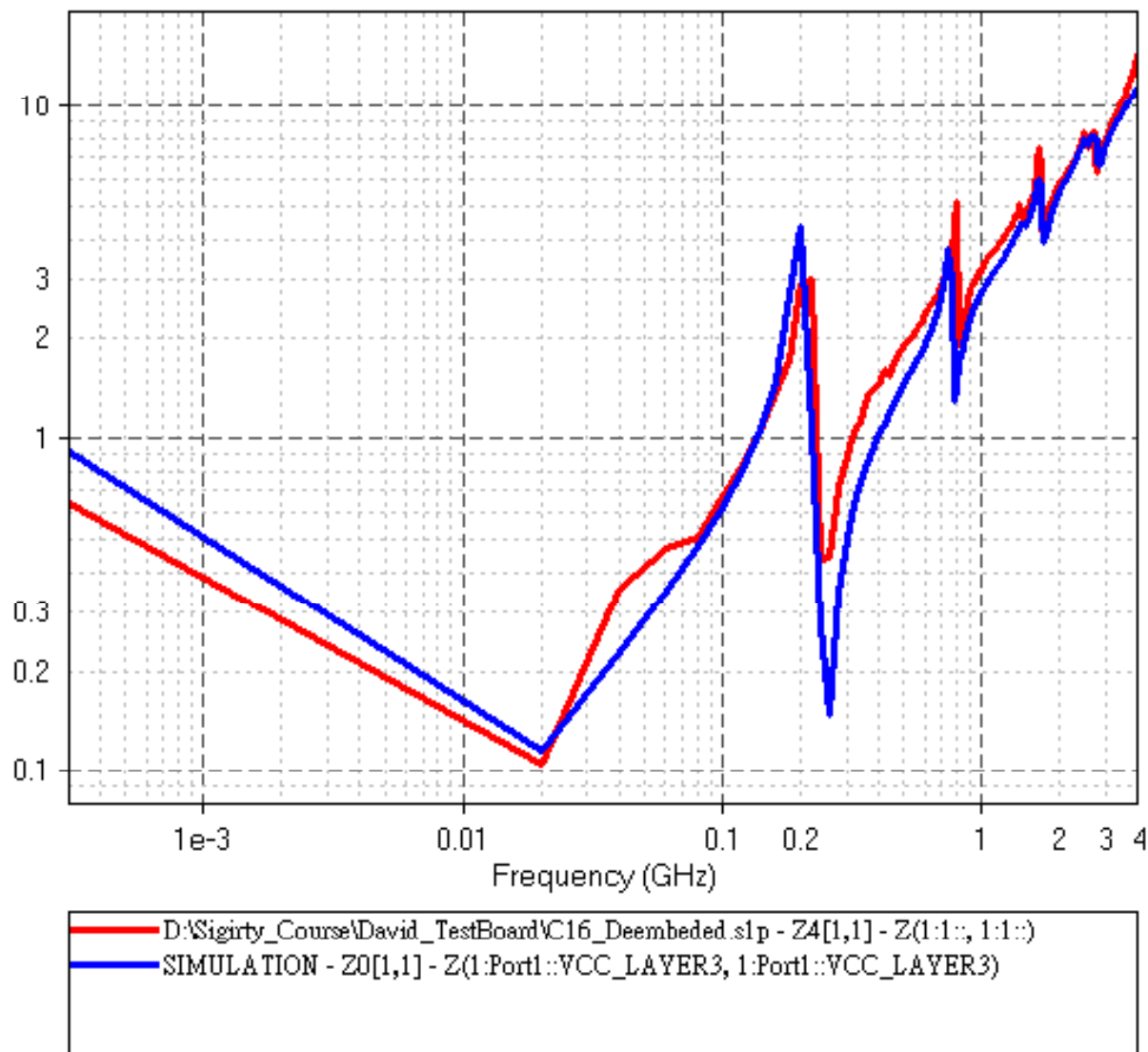


Simulation w/ transmission line effect

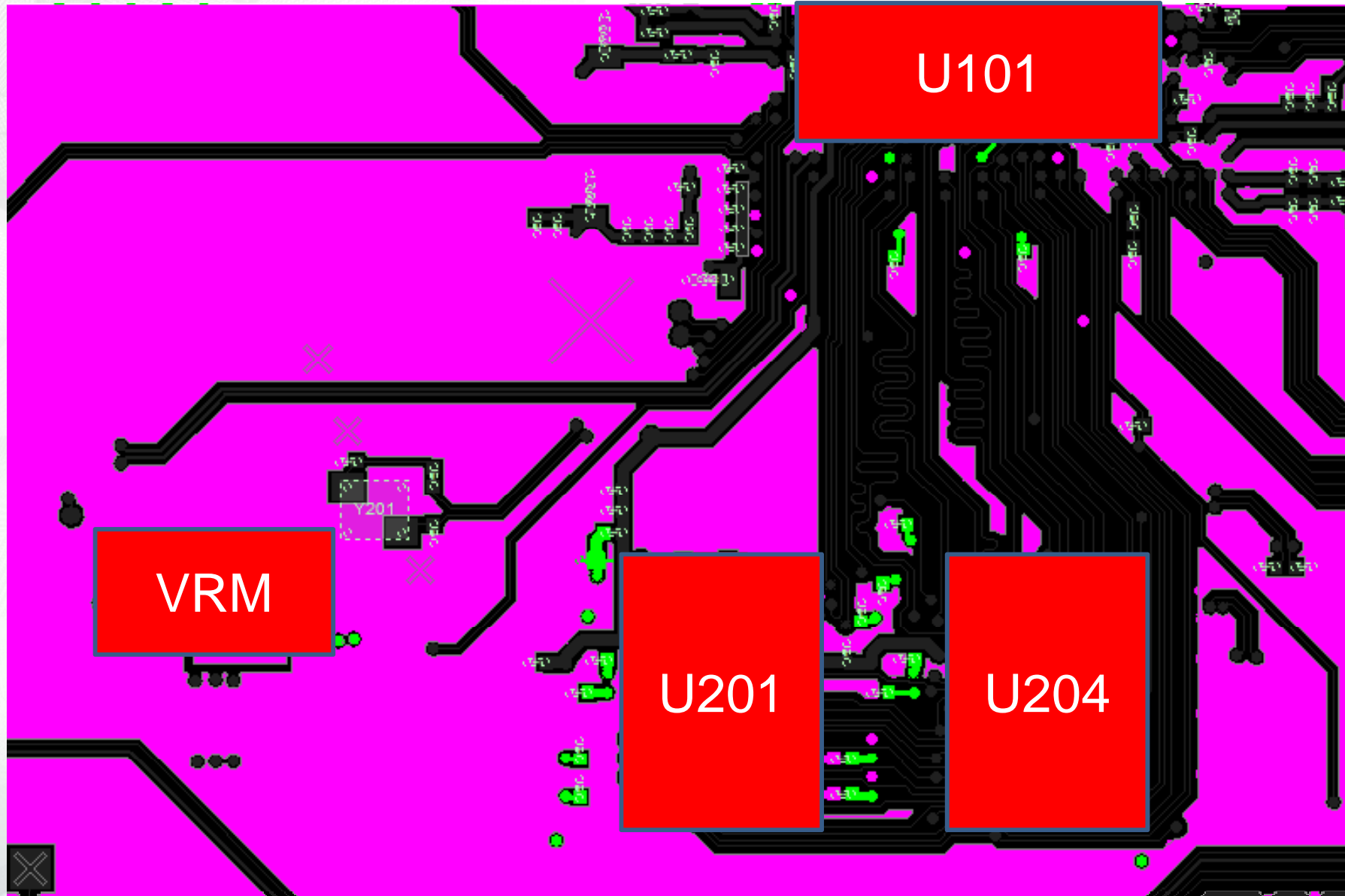
Measurement: Board W/ Decap De-embedded

Z Amplitude (Ohm)

TB-074_V00-0521.spd



Example 2: DDR3-1600

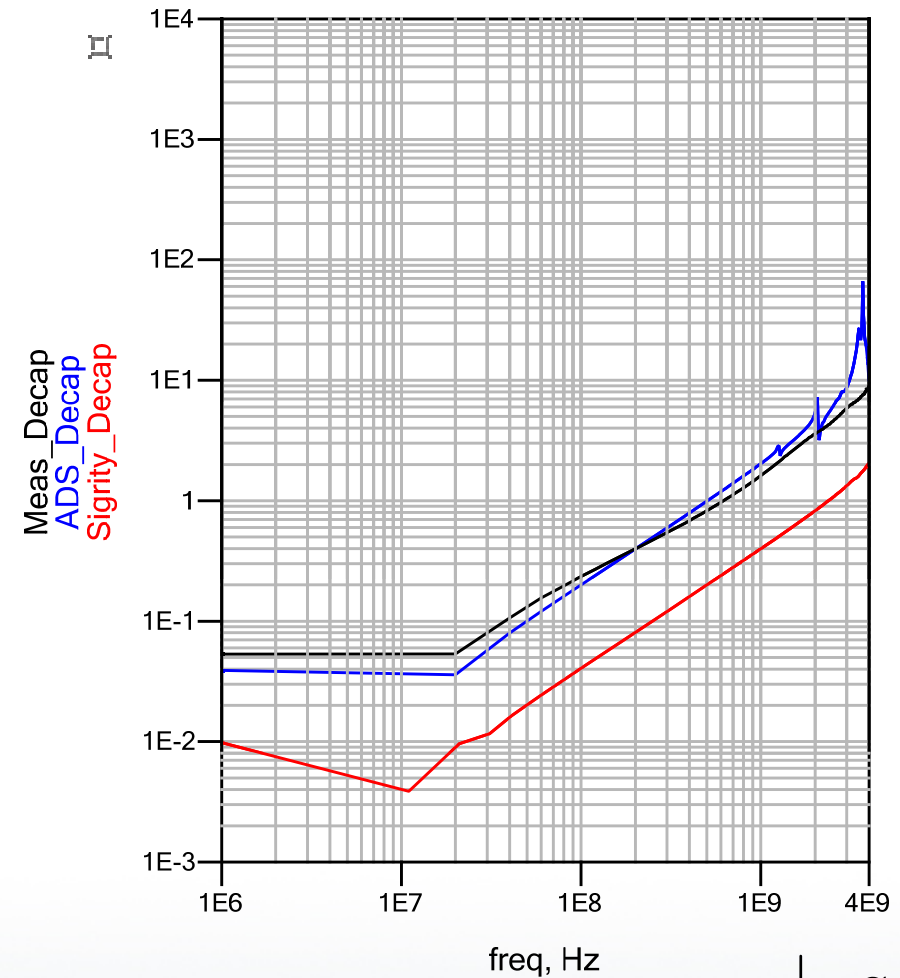
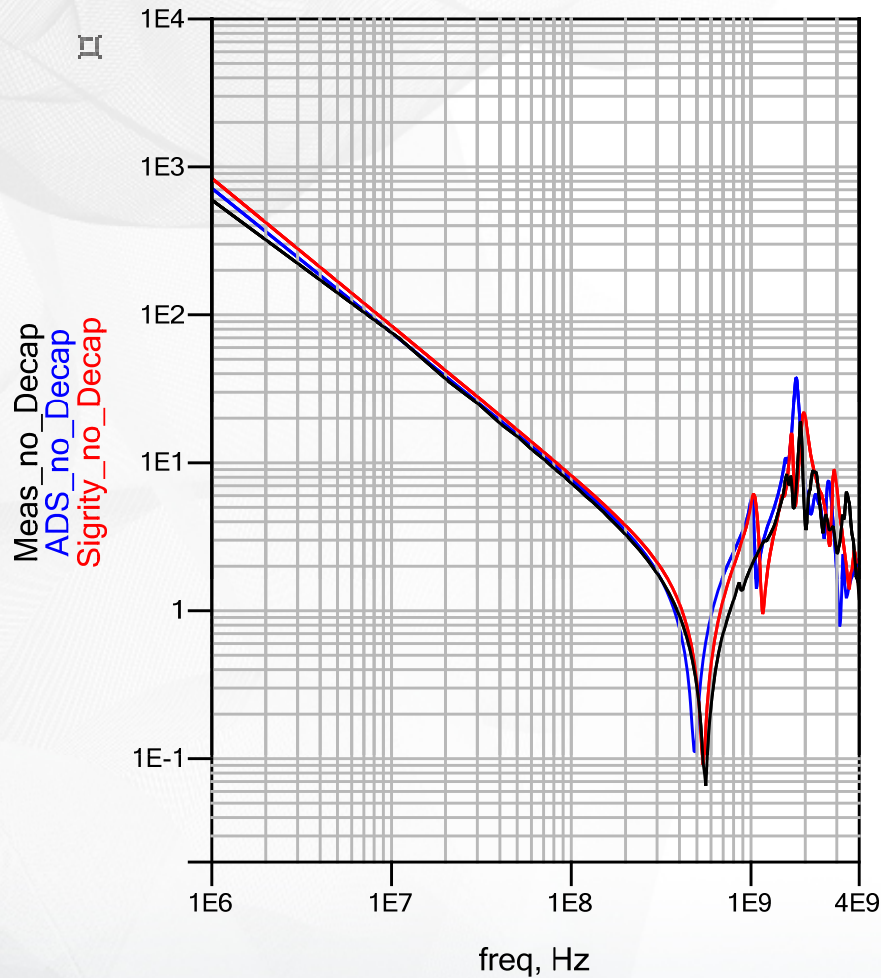


Target Impedance Estimation

- In data sheet, the $I_{\max} = 210\text{mA}$
- The swing is from 1.4V to 1.6V (ripple is +/- 6.67%)
- Hence the target impedance can be calculated as

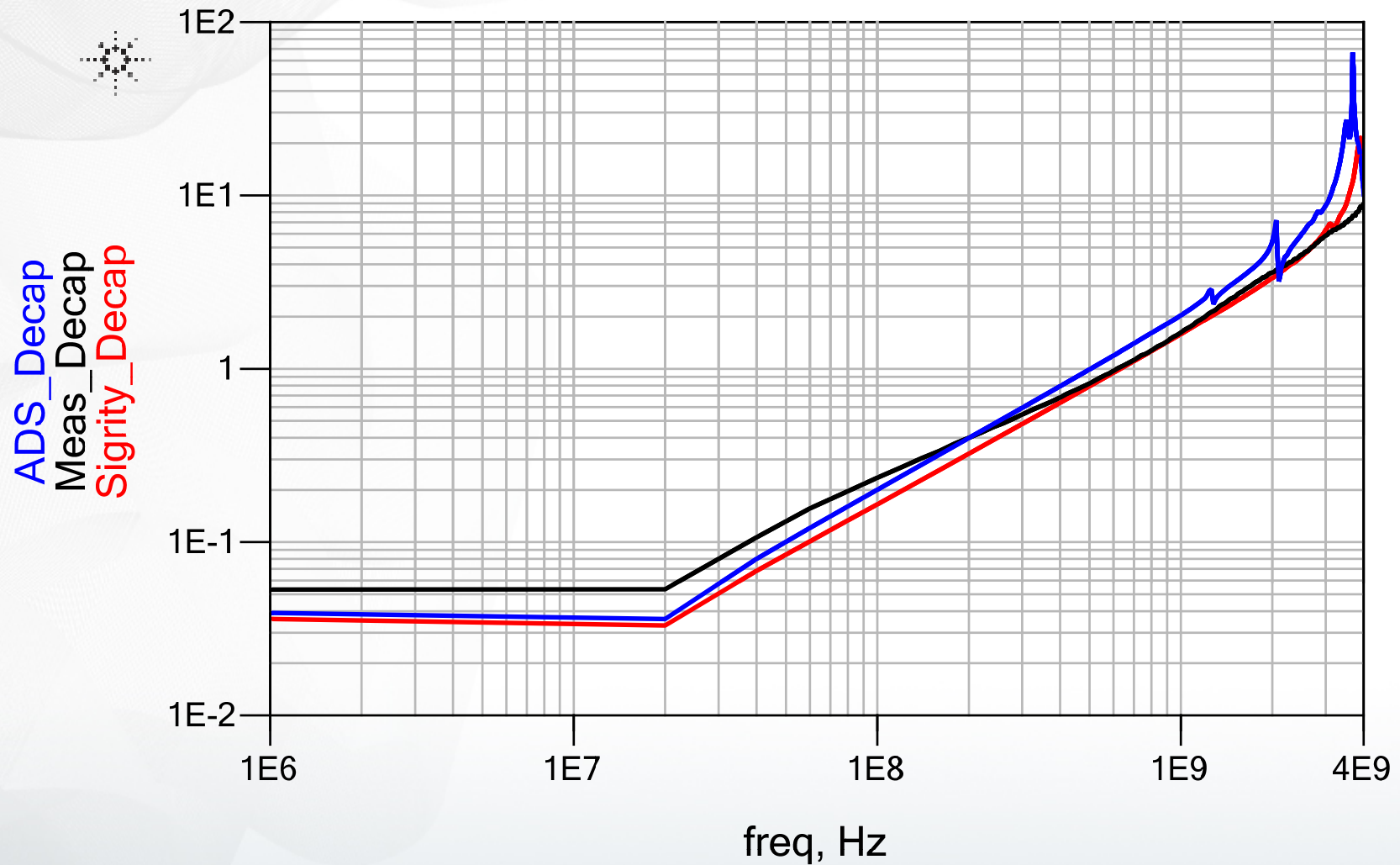
$$Z_T = \frac{V_{dd} \times \text{ripple}}{50\% \times I_{\max}} = \frac{1.5 \times 0.067}{0.5 \times 0.21} = 0.957\Omega$$

Correlation Ultra Low Impedance Measurement



2-Port measurement to capture the ultra low impedance $Z = 25 \times \left| \frac{S_{21}}{1 - S_{21}} \right|$

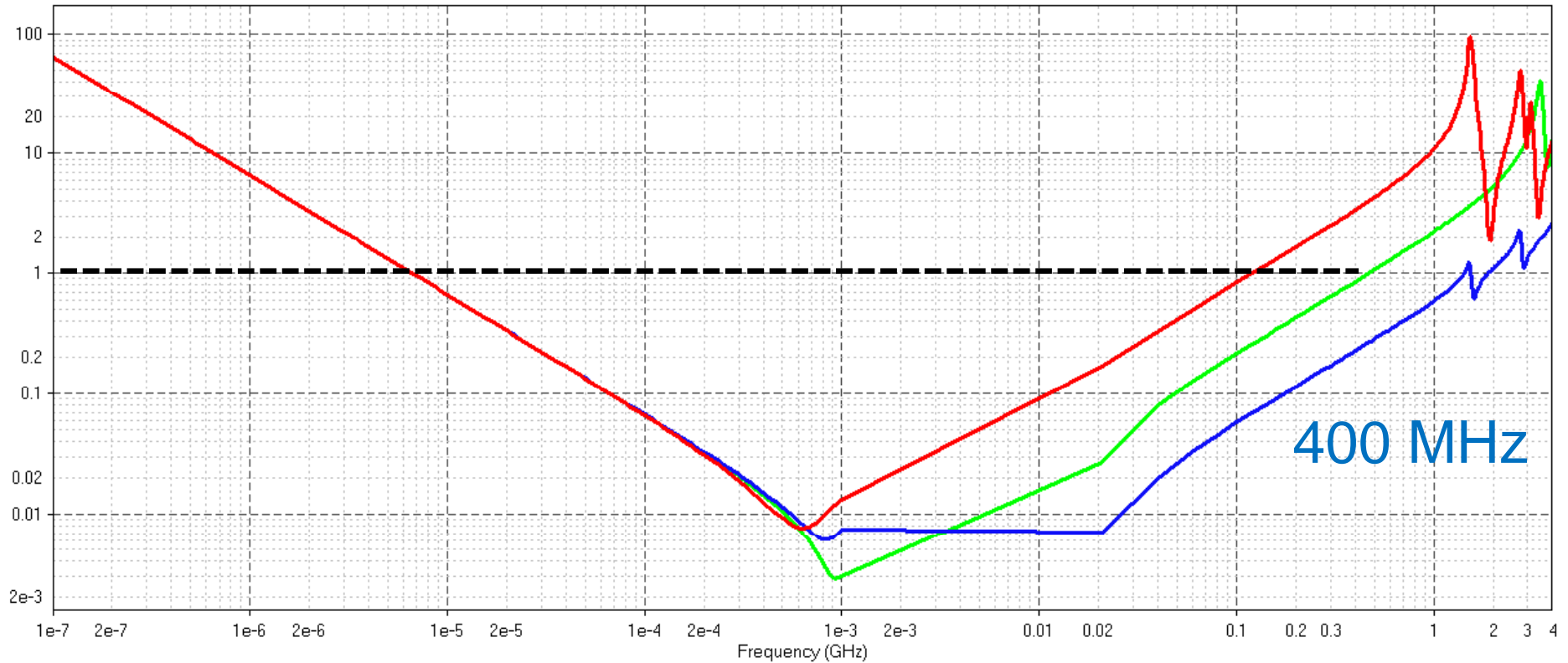
ESL & ESR Effect



Z-Profile @ U101, U201, and U204

Z Amplitude (Ohm)

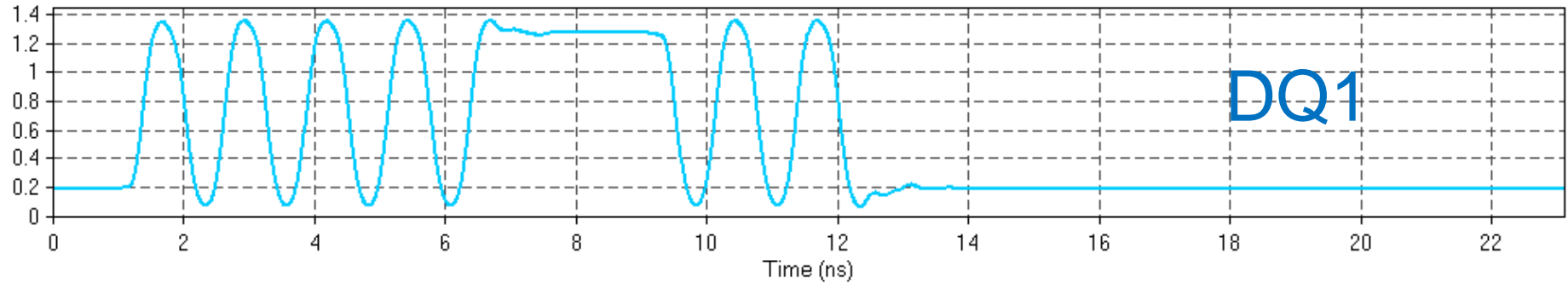
P2_test_Decap_Spara.spd



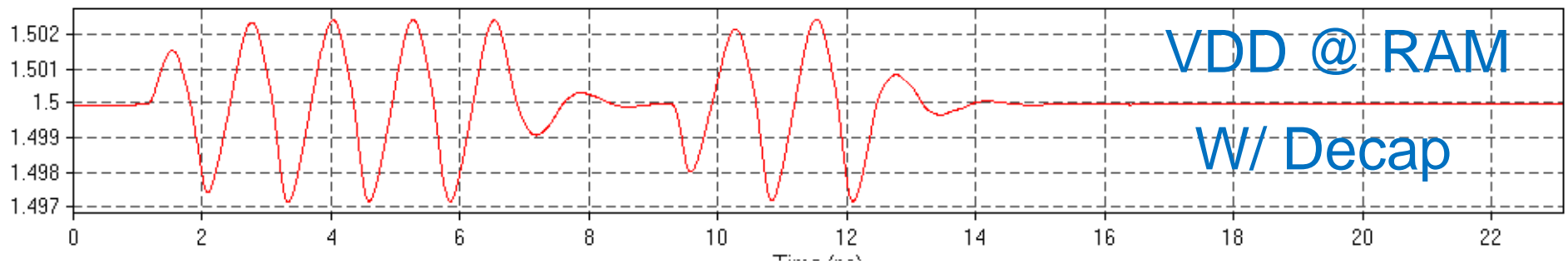
- SIMULATION - Z0[1,1] - Z(1:Port1_U101::+1.5V, 1:Port1_U101::+1.5V)
- SIMULATION - Z0[3,3] - Z(3:Port3_U204::+1.5V, 3:Port3_U204::+1.5V)
- SIMULATION - Z0[5,5] - Z(5:Port5_VRM_1::+1.5V, 5:Port5_VRM_1::+1.5V)

DQ1 Only: Write

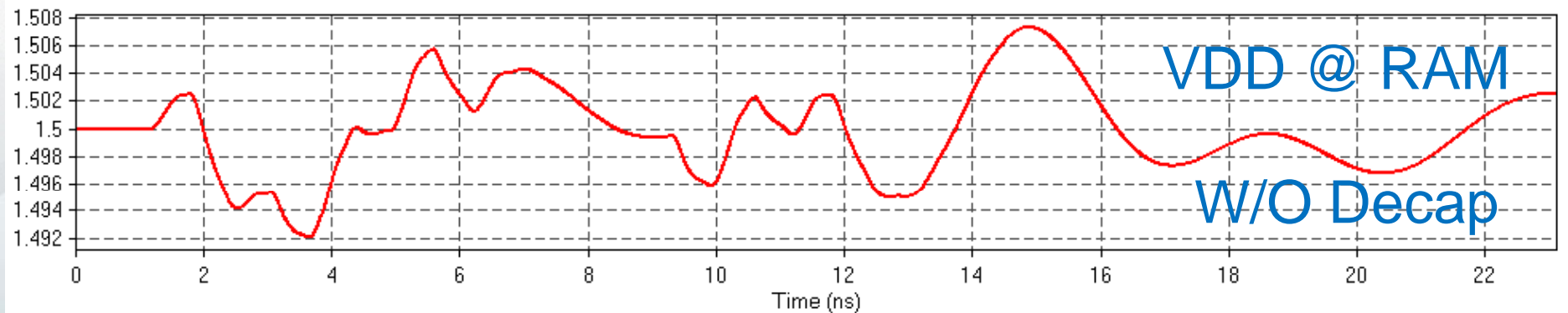
Voltage (V)



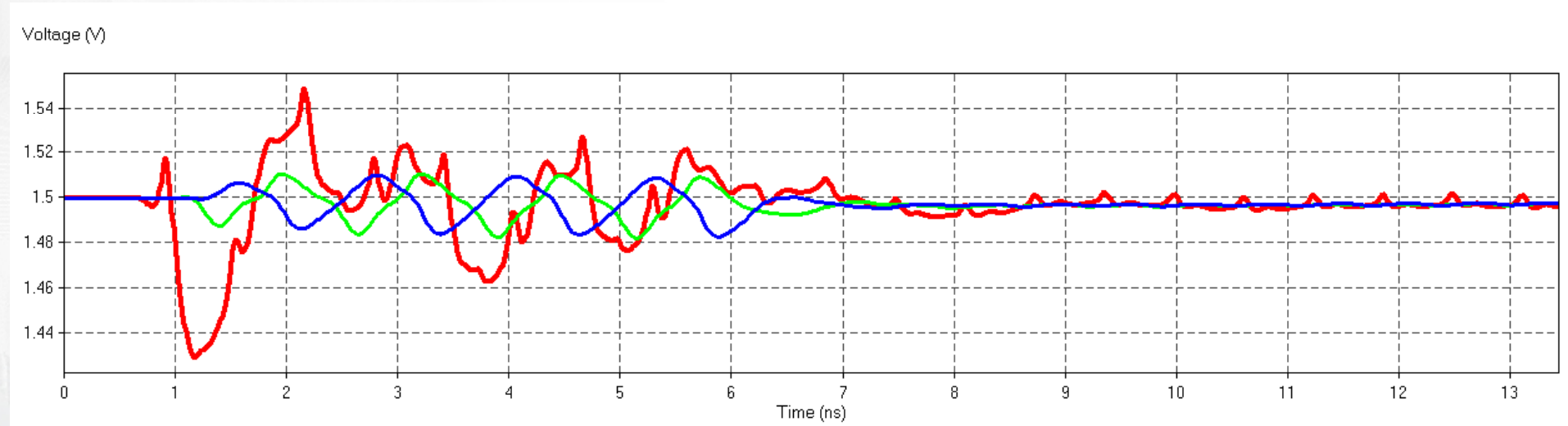
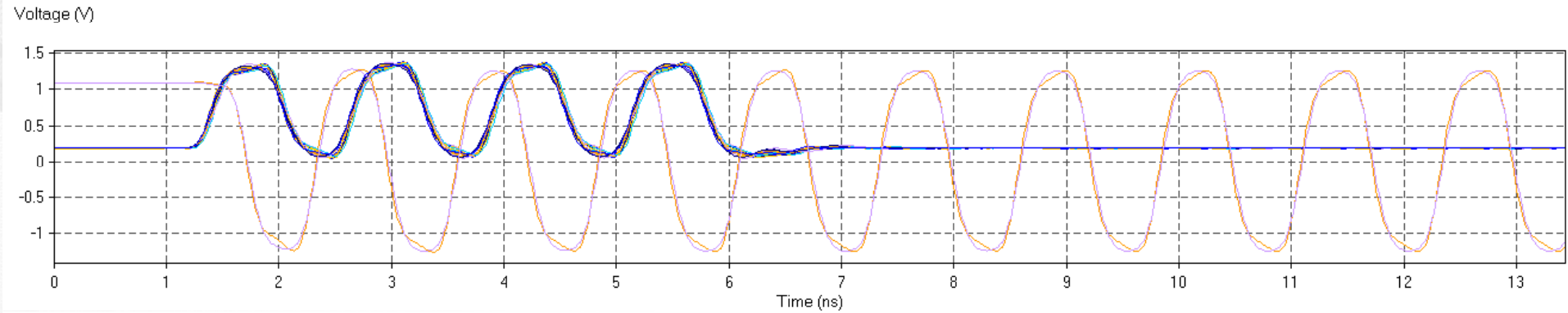
Voltage (V)



Voltage (V)

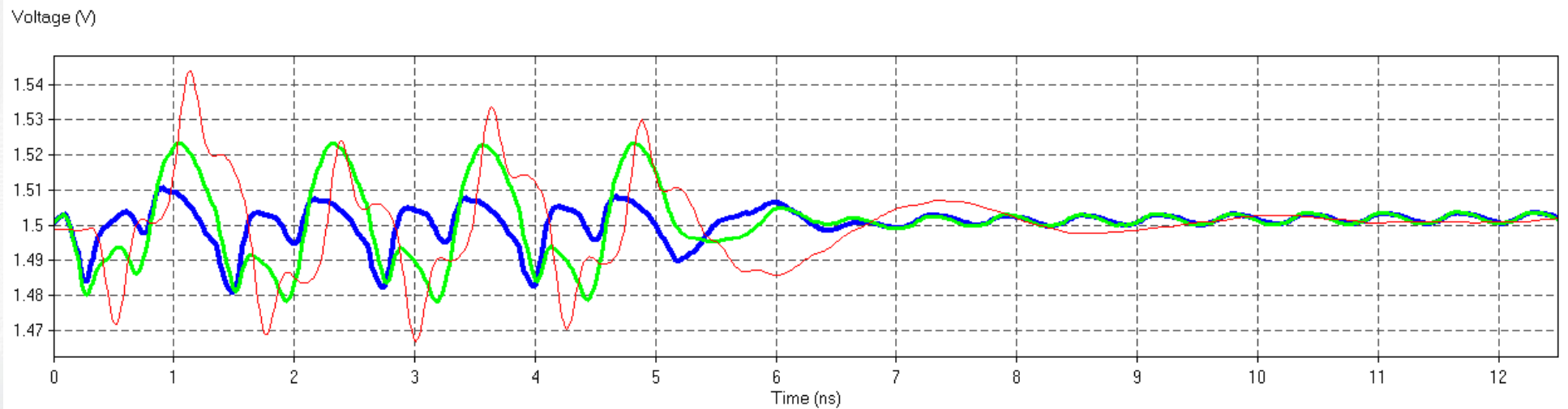
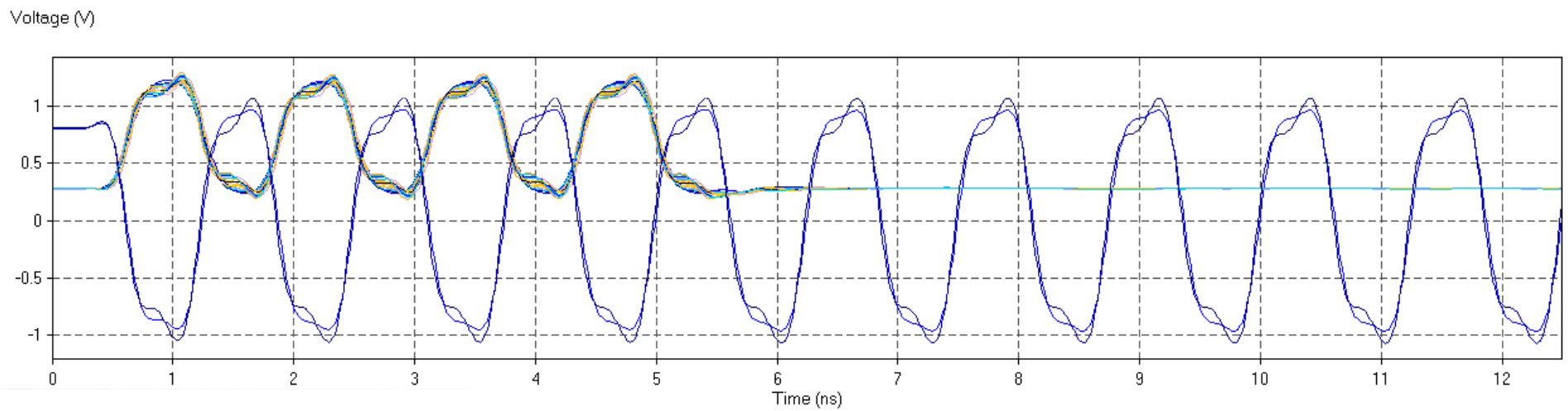


All DQ: Write



VDD swing from 1.42 ~ 1.55, within the spec (1.5 +/- 6.67%)

All DQ: Read



VDD swing from 1.45~ 1.55, within the spec (1.5 +/- 6.67%)

Conclusions

- Target impedance is the main parameter to design the power plane
- Ultra-low impedance measurement and proper embedded technique should be applied to obtain the good correlation
- Sigrity PowerSI and SystemSI provides an user-friendly workflow to speed up the design flow

References

- M. Swaminathan and A. E. Engin, *Power integrity modeling and design for semiconductors and systems*, NJ: Prentice-Hall, 2007
- *Agilent ultra-low impedance measurements using 2-port measurement*, application note, 2007