

2013 AUG 13 TAIPEI **Graser**
User
Conference

Allegro v16.6 New Enhancements

Graser - Mika

13/Aug/2013

Topic

STEP 3D Model Support

STEP

STEP File Mapping

Mapping Mechanical STEP Models

Export Board Drawing to STEP Model

Auto-Interactive Technologies for High-Speed Routing

Timing Vision

Auto-interactive Phase Tuning (AiPT)

Auto-interactive Delay Tuning (AiDT)

Flow Planning

Auto-interactive Breakout (AiBT)

Auto-interactive Add Connect (AiAC)

Auto-interactive Convert Corner (AiCC)

Topic

What's New in 16.6 Super HotFix

Logo Import

Net assignment to Multiple Shapes

Expand / Contract Voids in Shapes

Detune

Drafting Enhancements

Measure Support of Angle

Highlight to Vias

DRC Marker - Link to Constraint Manager

Database Locks / Tiering

STEP 3D Model Support

STEP

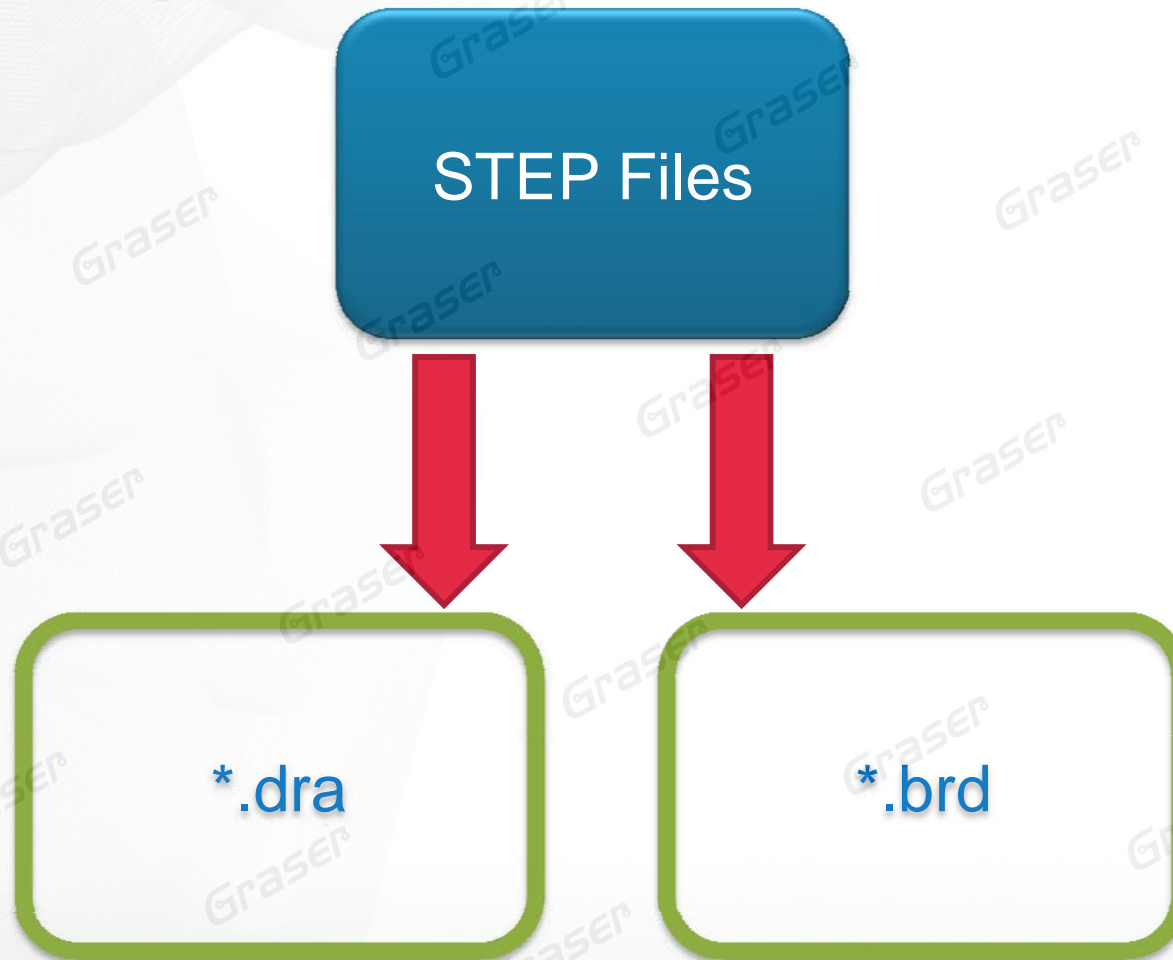
STEP-File is the most widely used data exchange form of STEP. Due to its **ASCII** structure, it is easy to read with typically one instance per line. The format of a STEP-File is defined in **ISO 10303-21** *Clear Text Encoding of the Exchange Structure*.

ISO 10303-21 defines the encoding mechanism on how to represent data according to a given EXPRESS schema, but not the EXPRESS schema itself. STEP-File are also called *p21-File* and *STEP Physical File*. The file extensions **.stp** and **.step** indicates that the file contain data conforming to STEP Application Protocols while the extension **.p21** should be used for all other purposes.

STEP



STEP File Mapping



STEP File Mapping

Once STEP model mapping is completed, the Allegro 3D viewer will display the graphical representations of the STEP models. The 3D viewer relies on the currently visible layers in the Allegro PCB editor to determine what is displayed in the viewer.

To view the 3D STEP models, the following CLASS/SUBCLASSES must be visible in the Allegro PCB Editor window:

PACKAGE GEOMETRY/PLACE_BOUND_TOP

PACKAGE GEOMETRY/PLACE_BOUND_BOTTOM

MANUFACTURING/STEP3D_ASSEMBLY_ENCLOSURE

STEP File Mapping

The screenshot shows the 'User Preferences Editor' window. On the left, a tree view shows the 'Library' category selected under 'Paths'. The main area displays a list of preferences for the 'Library' category. The 'steppath' preference is highlighted in yellow. A 'steppath Items' dialog box is open, showing the directory path 'C:/Allegro_test/2013_STEP_workshop/STEP_models/' entered in the 'Directories:' field. The 'Expand' checkbox is checked. At the bottom of the main window, a 'Summary description' box contains the text: 'Search path for STEP files(.stp .step). steppath = \$steppath'.

Preference	Value	Effective	Favorite
devpath	...	Command	<input checked="" type="checkbox"/>
interfacepath	...	Command	<input type="checkbox"/>
miscpath	...		
modulepath	...		
padpath	...		
parampath	...		
psmpath	...		
steppath	...		
techpath	...		
topology_template_path	...		

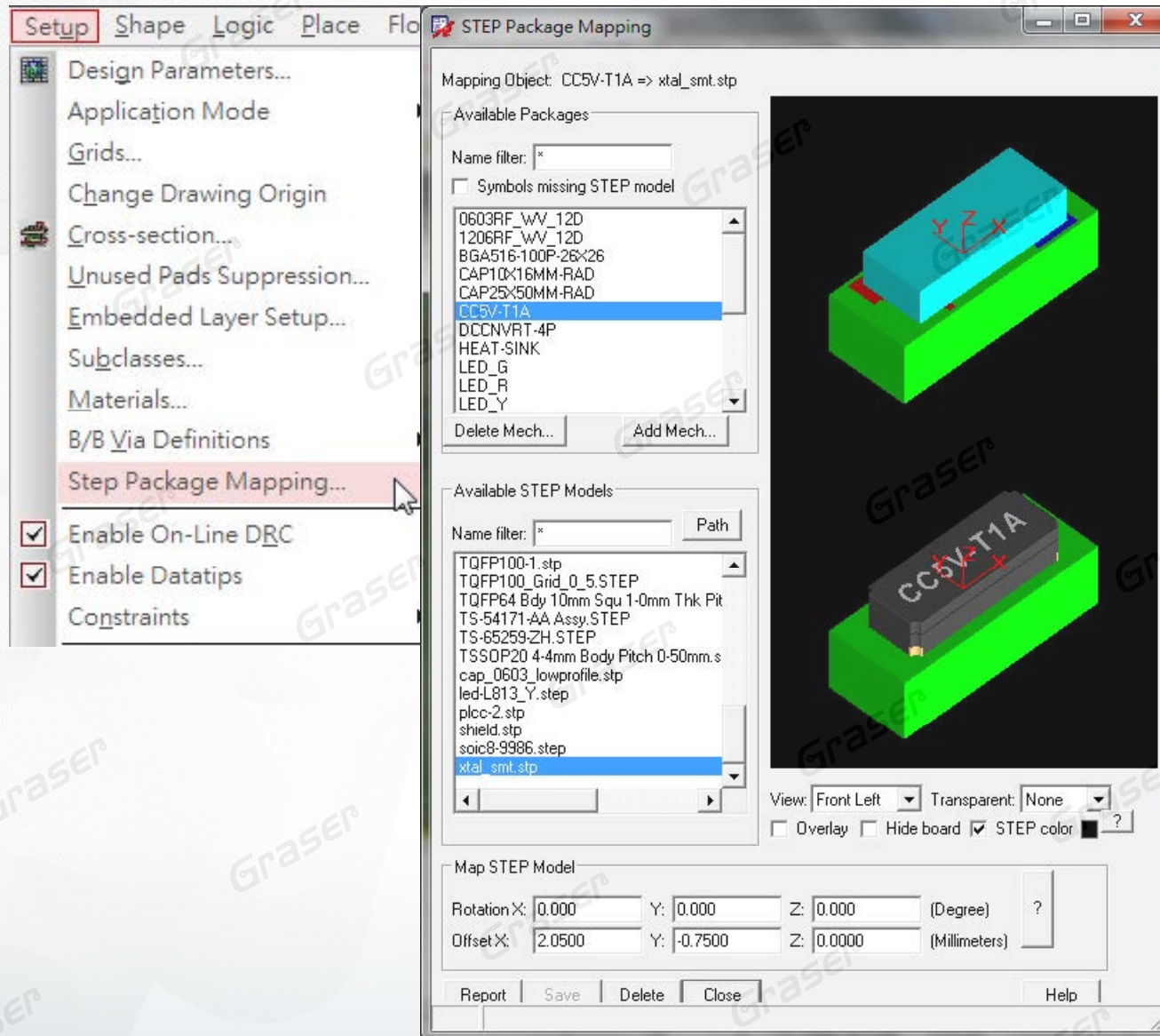
Directories:
C:/Allegro_test/2013_STEP_workshop/STEP_models/

Expand

OK Cancel

Summary description
Search path for STEP files(.stp .step).
steppath = \$steppath

STEP File Mapping



STEP File Mapping

STEP Package Mapping Report

Search: Match w

Design Name C:/Allegro_test/2013_STEP_workshop/star
Date Mon Apr 01 17:27:24 2013

SYMBOL_NAME	STEP_FILE
0603RF_WV_12D	cap_0603_lowprofile
1206RF_WV_12D	1206SMD.step
BGA516-100P-26X26	BGA516C100P.stp
CAP10X16MM-RAD	Cap10x16.STEP
CAP25X50MM-RAD	Cap25x50.STEP
CC5V-T1A	xtal_smt.stp
DCCNVRT-4P	4pDCCConv.step
HEAT-SINK	HS-54171-AA Assy.
LED_G	LED-L813_G.step
LED_R	LED-L813_R.step
LED_Y	led-L813_Y.step
PCI-26PCONN	
PLCC32	PLCC32.stp
PLCC68	PLCC68.stp
RES-400	AXIAL_RESISTOR_0
RES_VERT	User Library-Axial Re
SOIC16	SOIC16 3-9mm Bod
SOIC20W	SOIC20_W.stp
SOIC8	soic8-9986.step
STEP3D_MECH_SHIELD	shield.stp
TQFP100	TQFP100-1.stp

STEP Package Mapping

Mapping Object: CC5V-T1A => xtal_smt.stp

Available Packages

Name filter: *

Symbols missing STEP model

- 0603RF_WV_12D
- 1206RF_WV_12D
- BGA516-100P-26X26
- CAP10X16MM-RAD
- CAP25X50MM-RAD
- CC5V-T1A**
- DCCNVRT-4P
- HEAT-SINK
- LED_G
- LED_R
- LED_Y

Delete Mech... Add Mech...

Available STEP Models

Name filter: * Path

- TQFP100-1.stp
- TQFP100_Grid_0_5.STEP
- TQFP64 Bdy 10mm Squ 1-0mm Thk Pit
- TS-54171-AA Assy.STEP
- TS-65259-ZH.STEP
- TSSOP20 4-4mm Body Pitch 0-50mm.s
- cap_0603_lowprofile.stp
- led-L813_Y.step
- plcc-2.stp
- shield.stp
- soic8-9986.step
- xtal_smt.stp**

View: Front Left Transparent: None

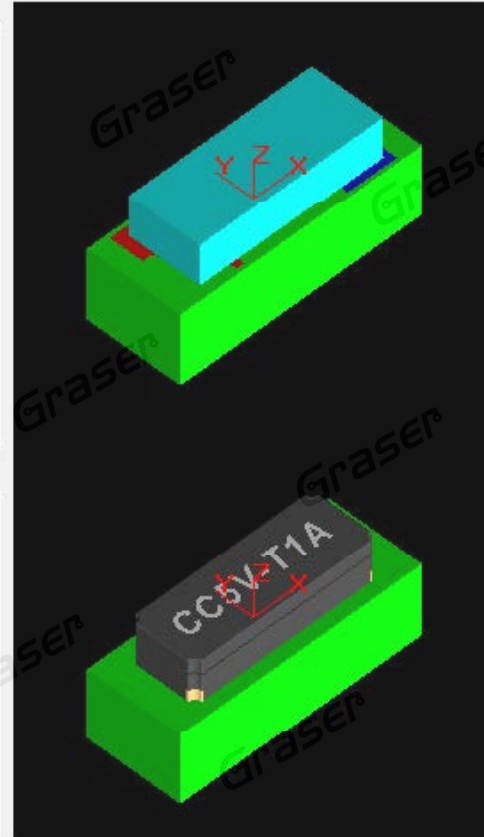
Overlay Hide board STEP color

Map STEP Model

Rotation X: 0.000 Y: 0.000 Z: 0.000 (Degree) ?

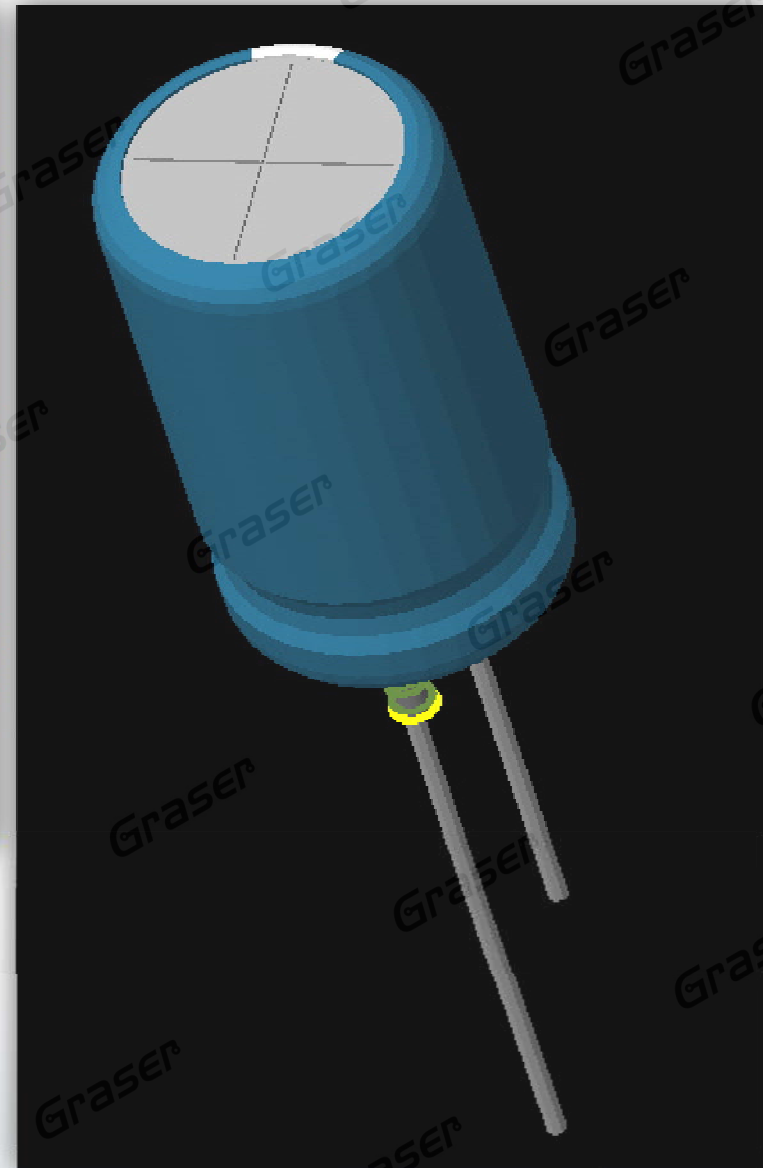
Offset X: 2.0500 Y: -0.7500 Z: 0.0000 (Millimeters)

Report Save Delete Close Help

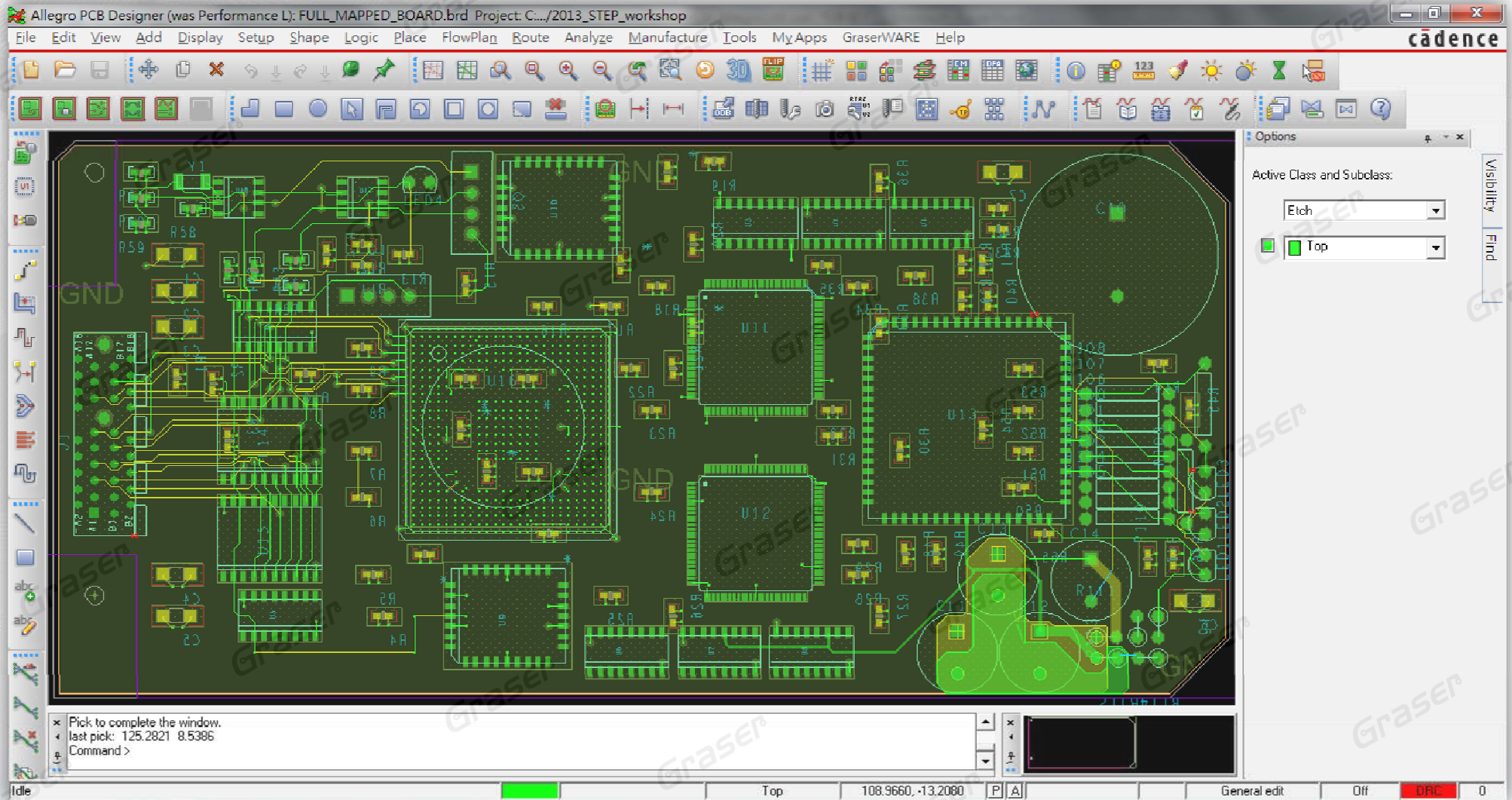


ROTATION_Z	OFFSET_X	OFFSET_Y	OFFSET_Z
0.000	0.0000	0.0000	0.0000
0.000	0.0000	0.0000	0.0000
90.000	0.0000	0.0000	0.0000
0.000	175.1000	62.9000	9.0000
0.000	581.5000	229.5000	0.0000
0.000	2.0500	-0.7500	0.0000
0.000	0.0968	0.1290	0.0000
0.000	0.3226	0.0710	0.0258
90.000	0.0000	0.0000	10.0000
90.000	0.0000	0.0000	10.0000
90.000	0.0000	0.0000	10.0000
0.000	0.0000	0.1729	0.0000
0.000	0.0000	0.0000	0.0000
0.000	0.0000	0.0000	0.0000
0.000	1.2500	0.0000	0.0000
270.000	0.0000	0.0000	0.9000
270.000	0.0000	0.0000	0.0000
0.000	0.0000	0.0000	0.2000
0.000	0.0000	0.0000	0.0000
0.000	0.0000	0.0000	0.8000

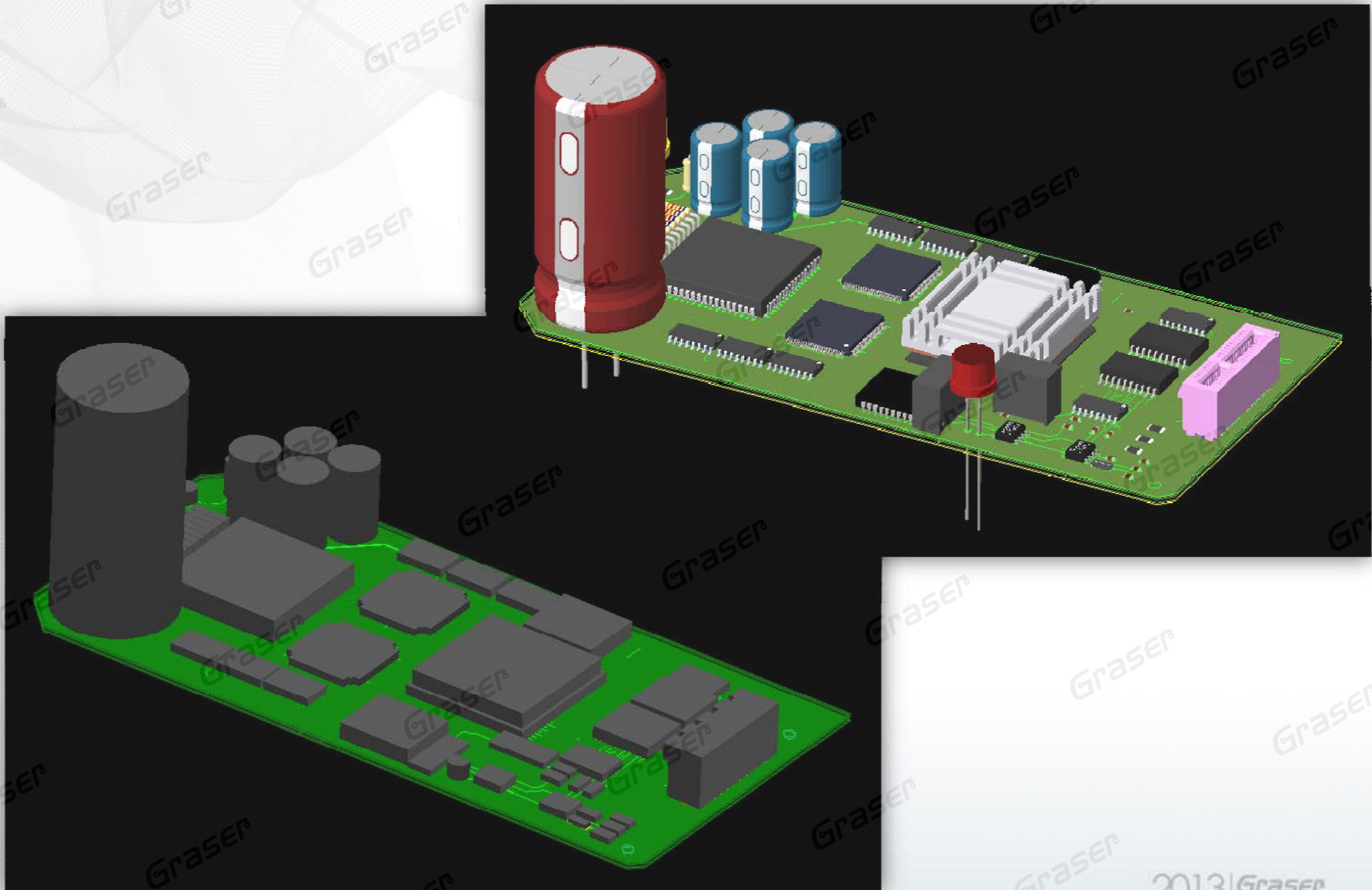
STEP File Mapping



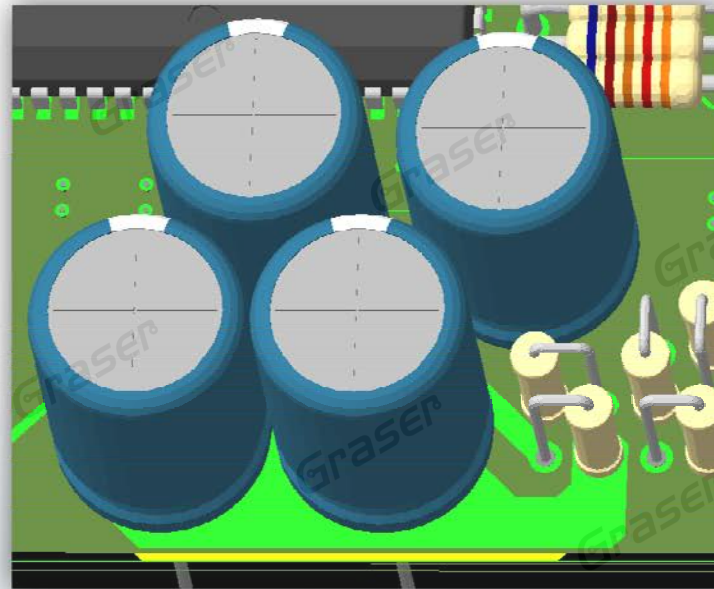
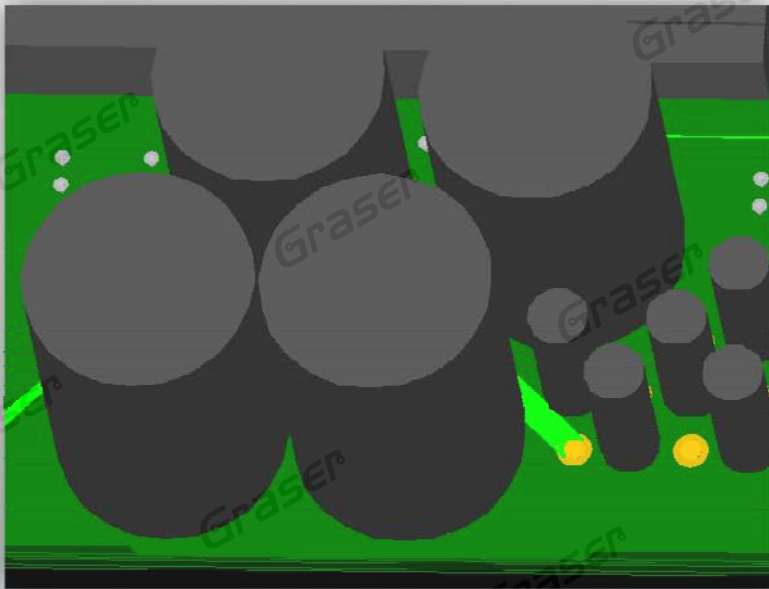
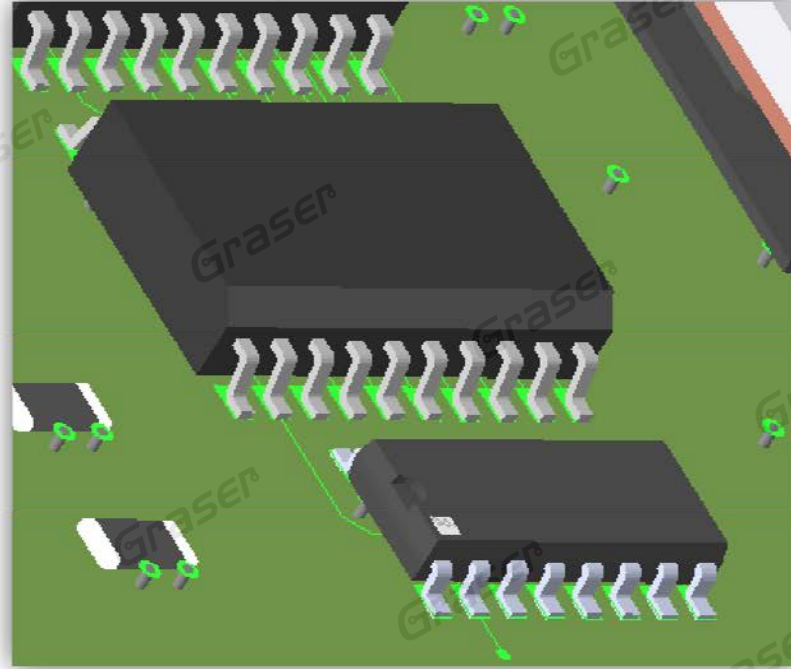
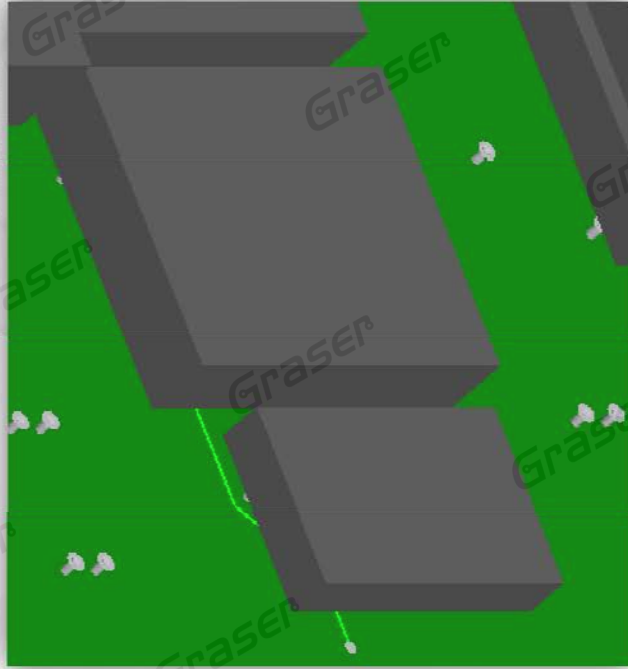
STEP File Mapping



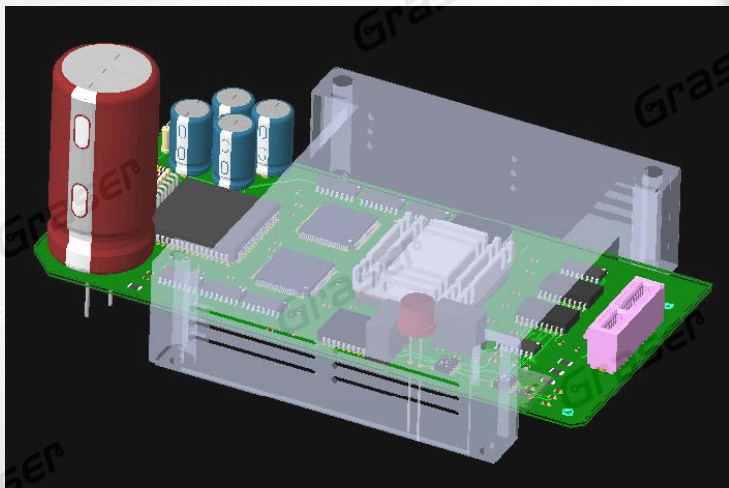
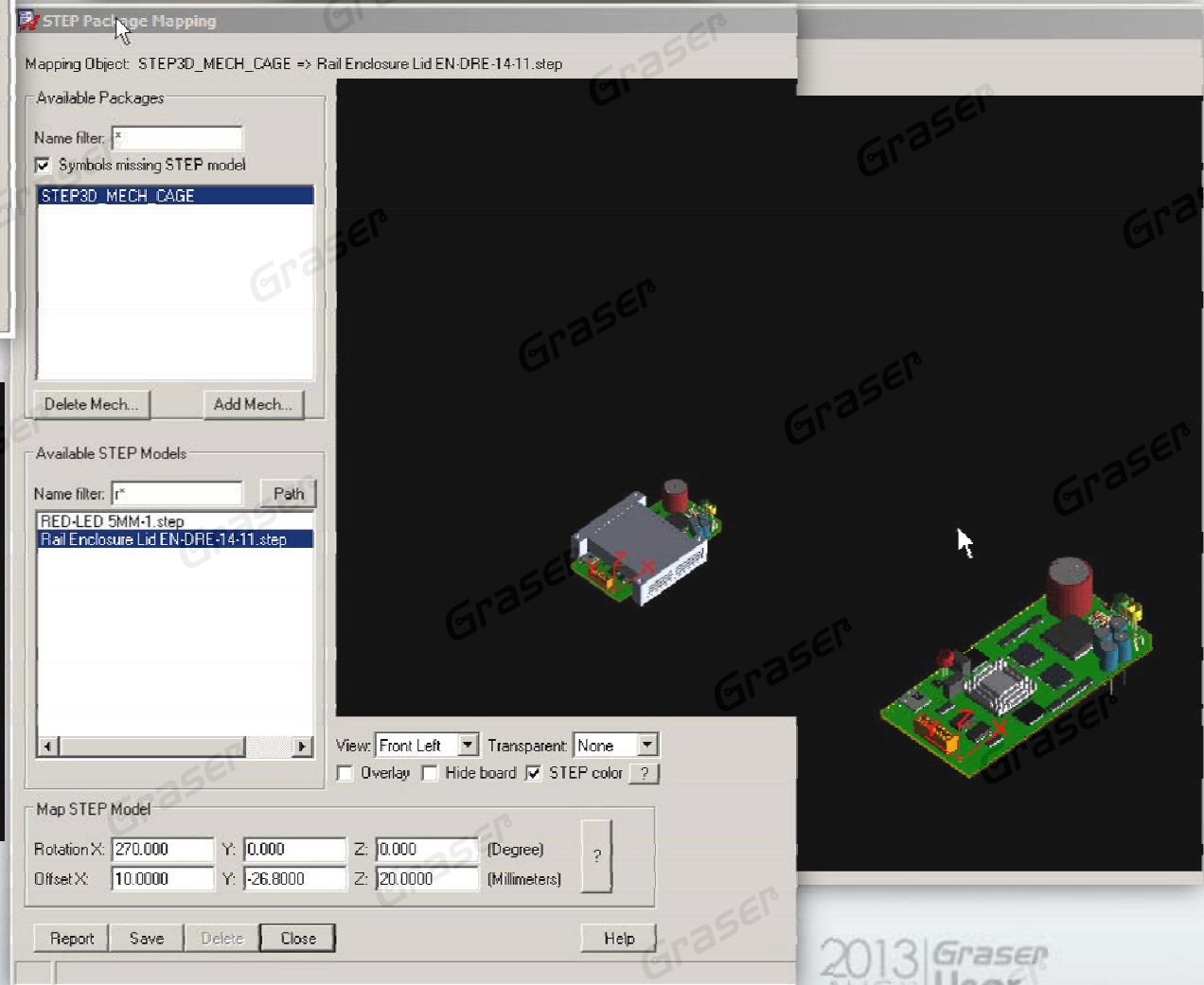
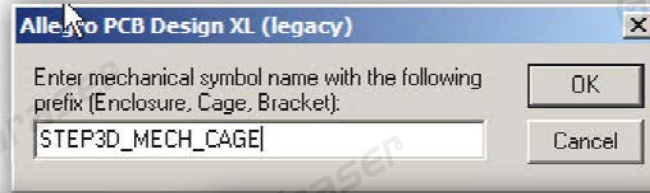
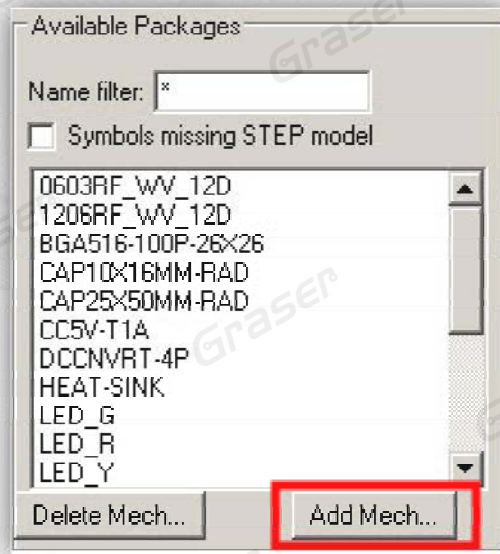
STEP File Mapping



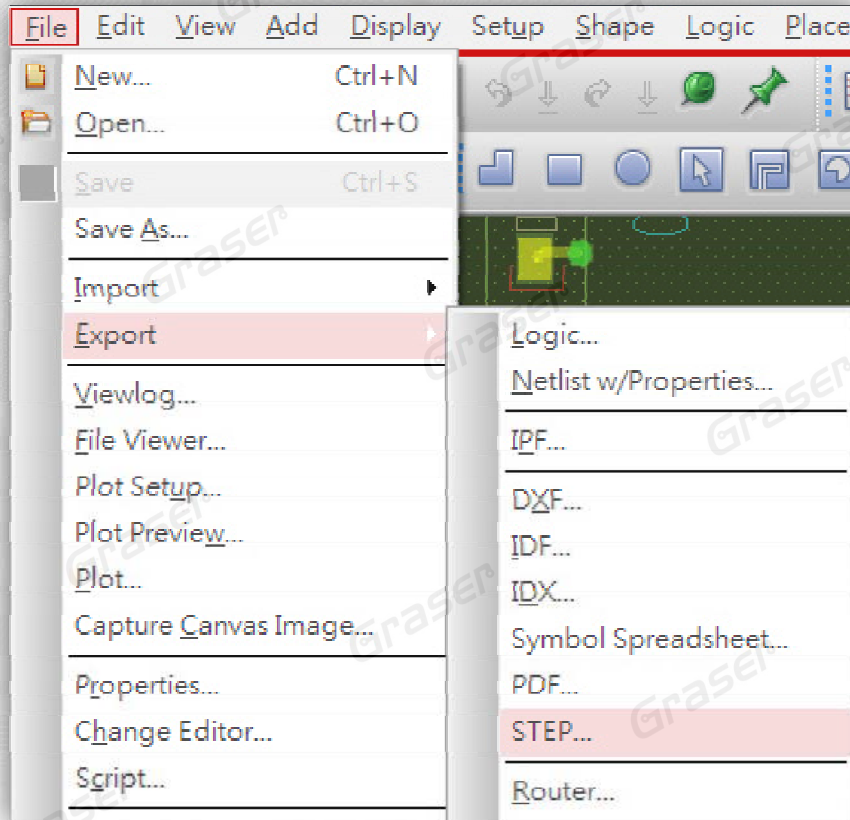
STEP File Mapping



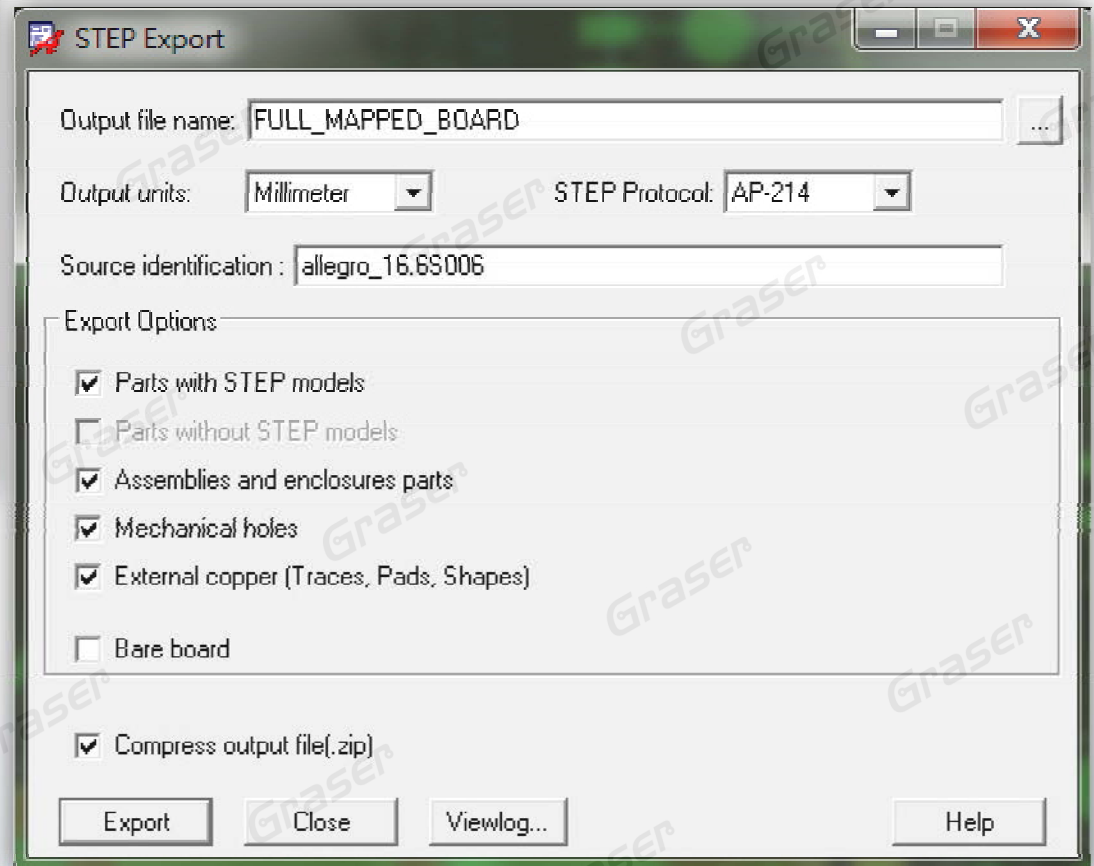
Mapping Mechanical STEP Models



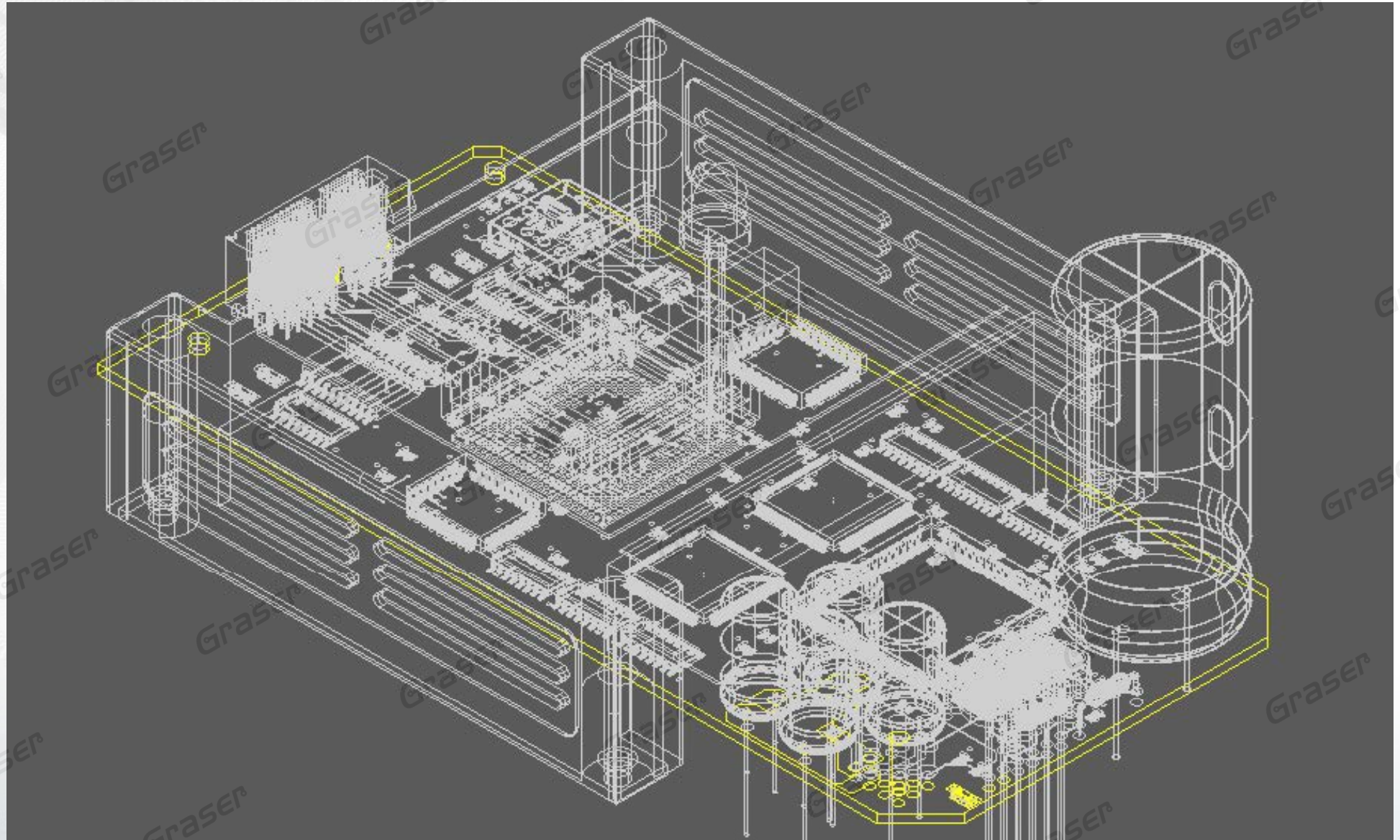
Export Board Drawing to STEP Model



STEP Protocol: There are three possible output protocol formats available, **AP-203**, **AP-214**, and **AP-242**. **AP-214** is the recommended default.



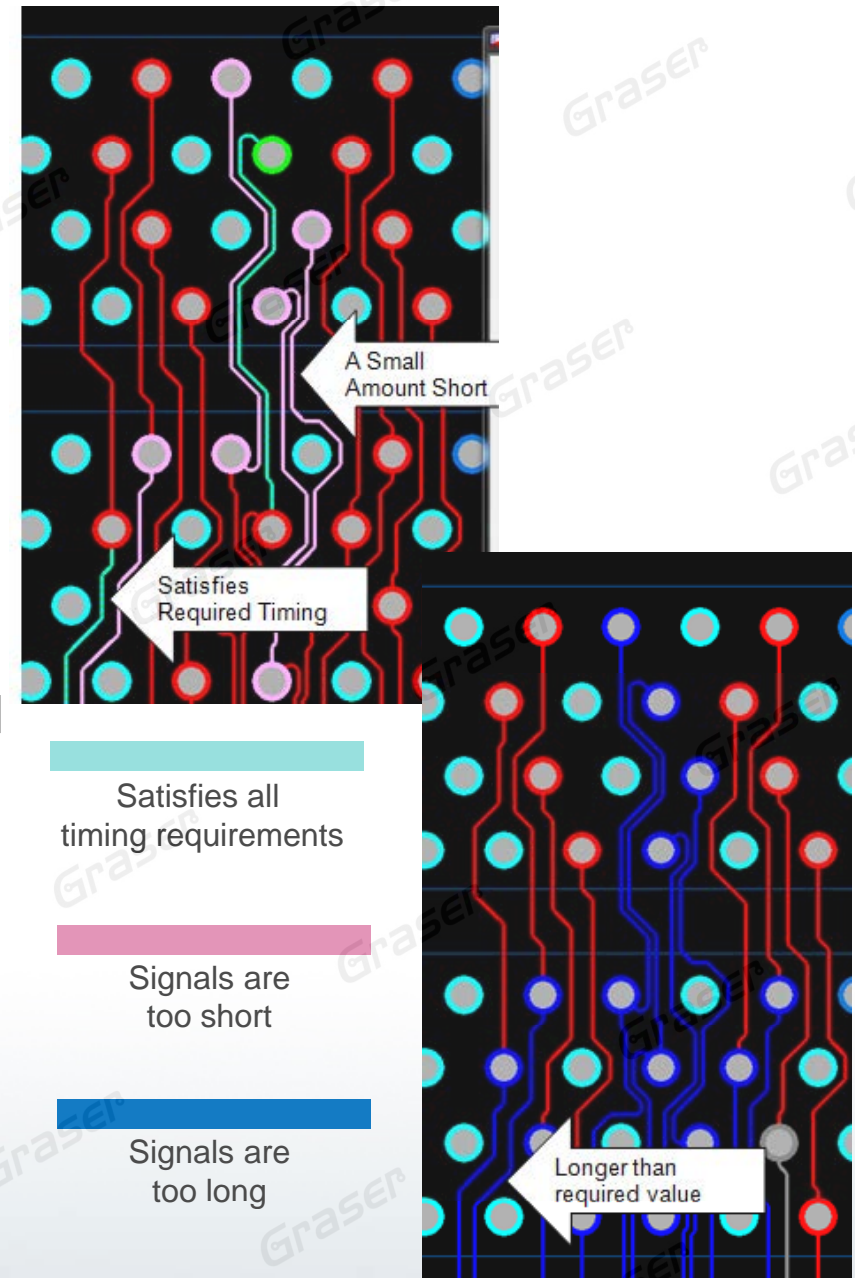
Export Board Drawing to STEP Model



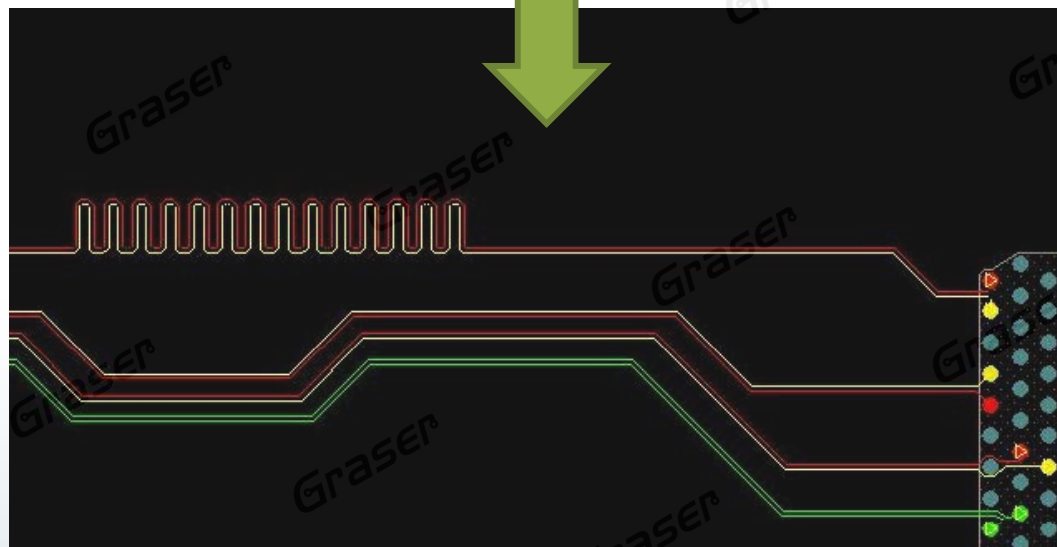
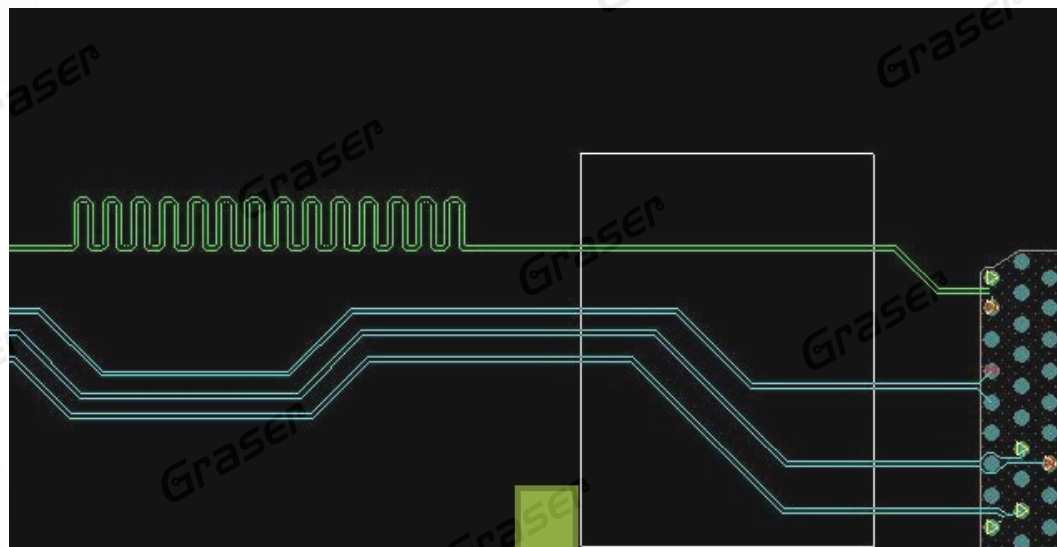
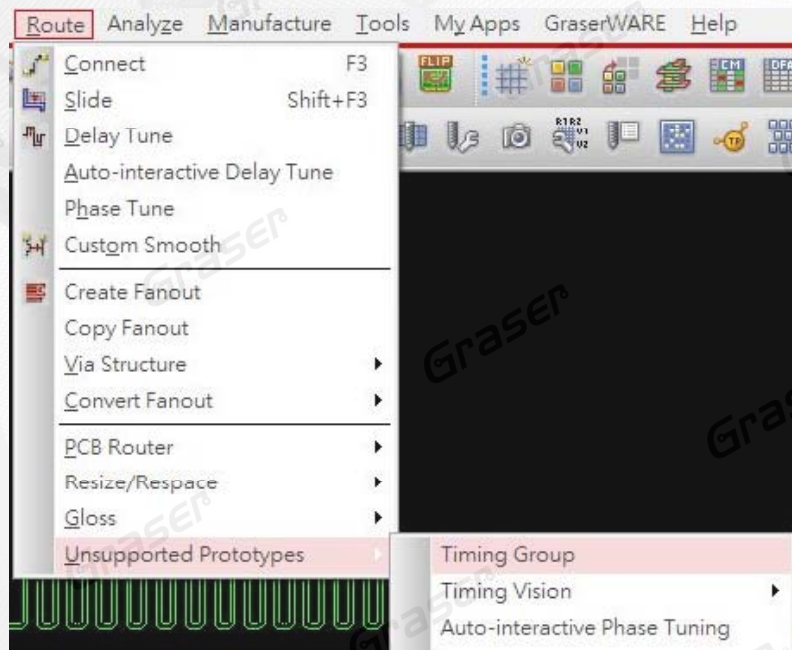
Auto-Interactive Technologies for High-Speed Routing

Timing Vision

- Visualize real-time delay / phase information directly on clines
- Significantly reduces time / effort to implement timing requirements
 - Reduce trips to Constraint Manager and reports
- User-defined cline feedback
 - Coloring, stipple patterns, and customized data tip information



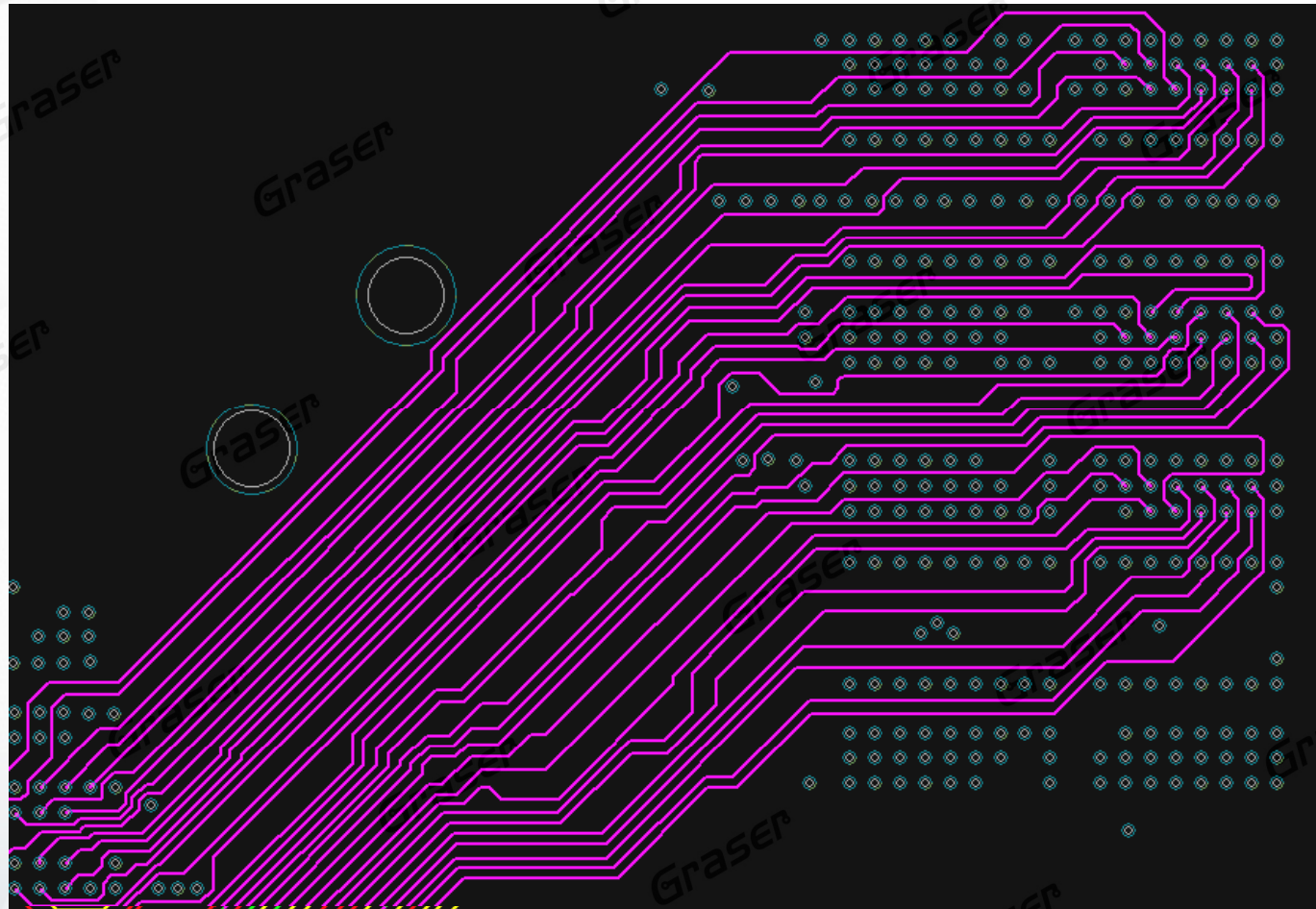
Timing Vision



Timing Vision

- Allow users to see beyond their physical routing

Green = good; **Red** = short; **Yellow** = long; Stripes = target



Auto-interactive Phase Tuning (AiPT)

Options

Compensation Loc.: Any

Compensation Techniques

Pad Entry Shortening Yes

Pad Entry Lengthening Yes

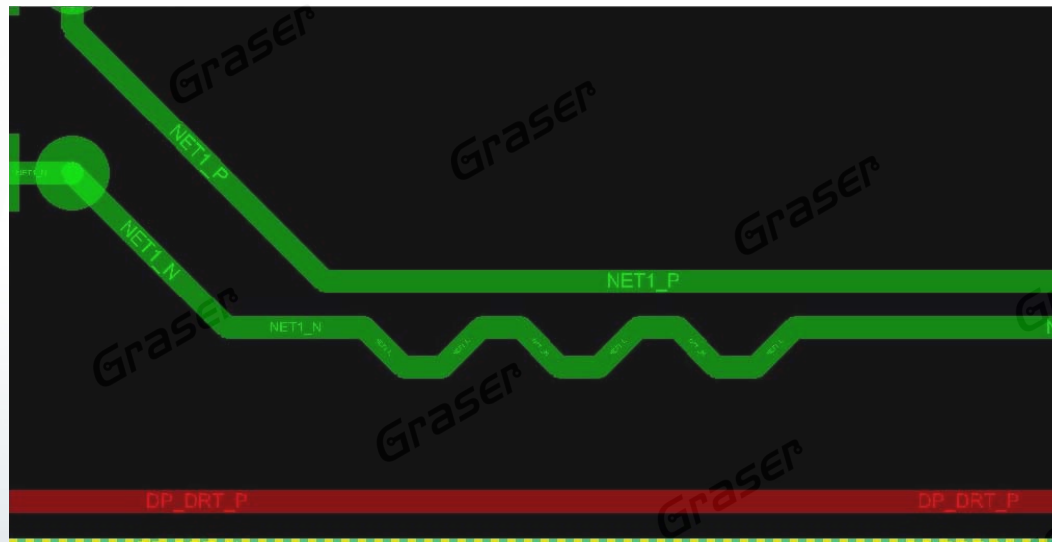
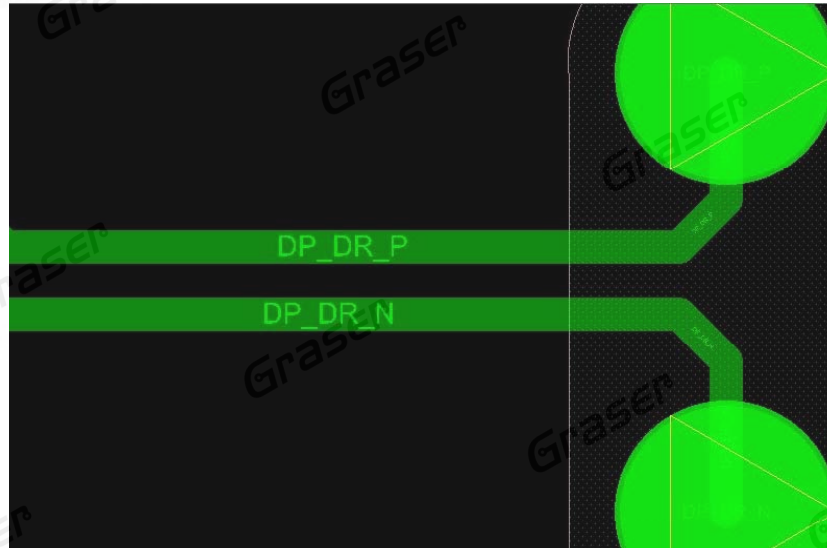
Allow off-angle segs Yes

Allow gather move Yes

Allow Uncoupled Bumps No

Height: 10.00

Length: 10.00



Auto-interactive Delay Tuning (AiDT)

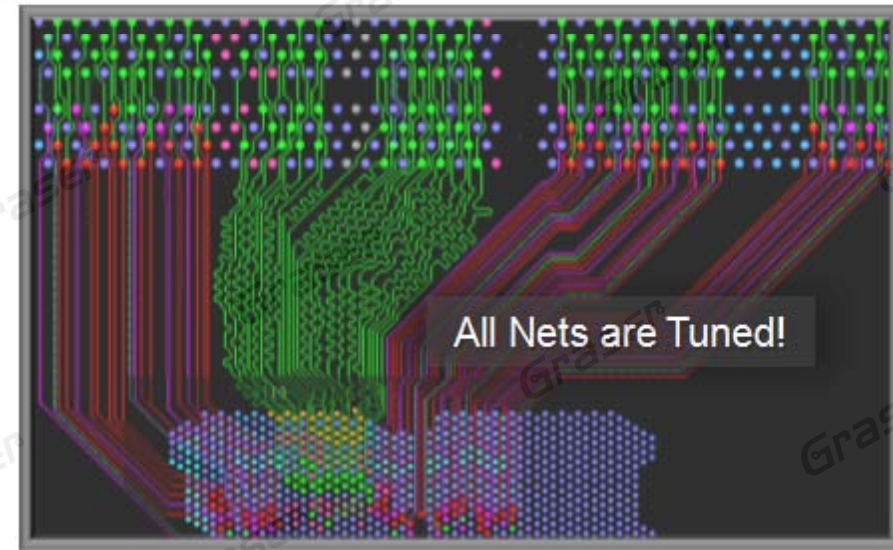


Before

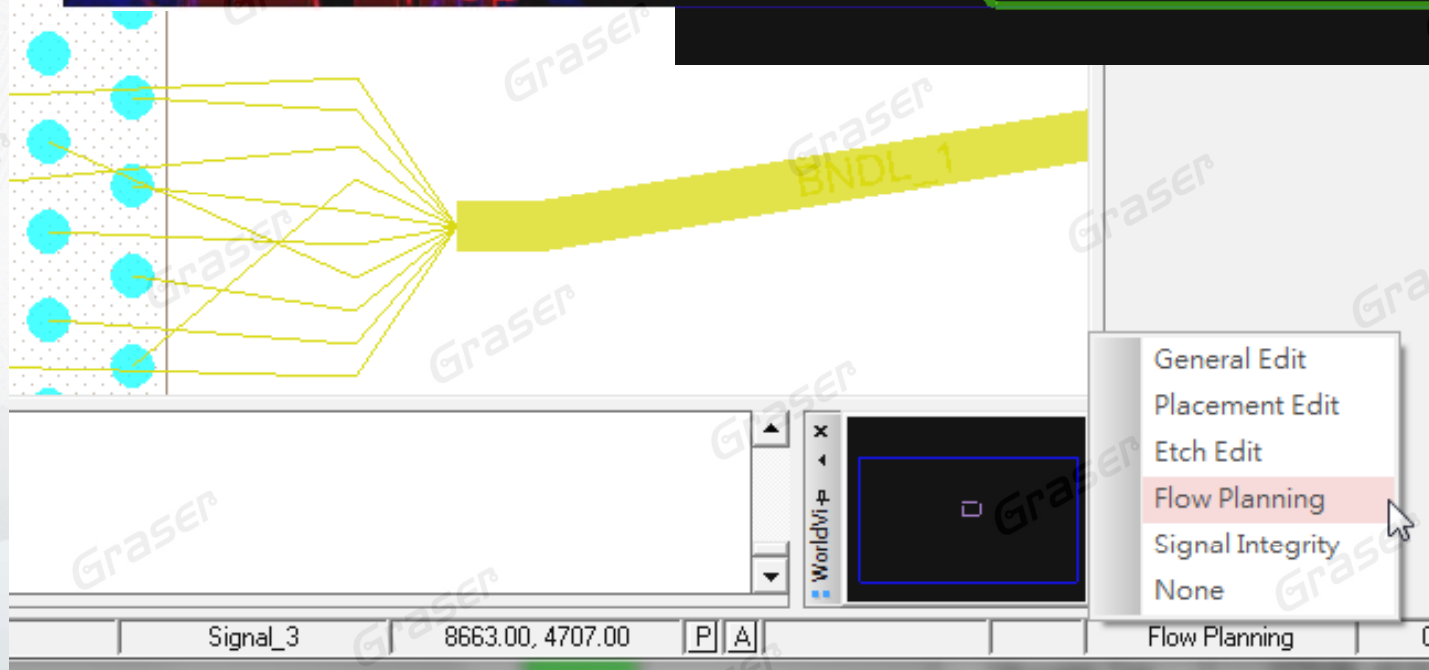
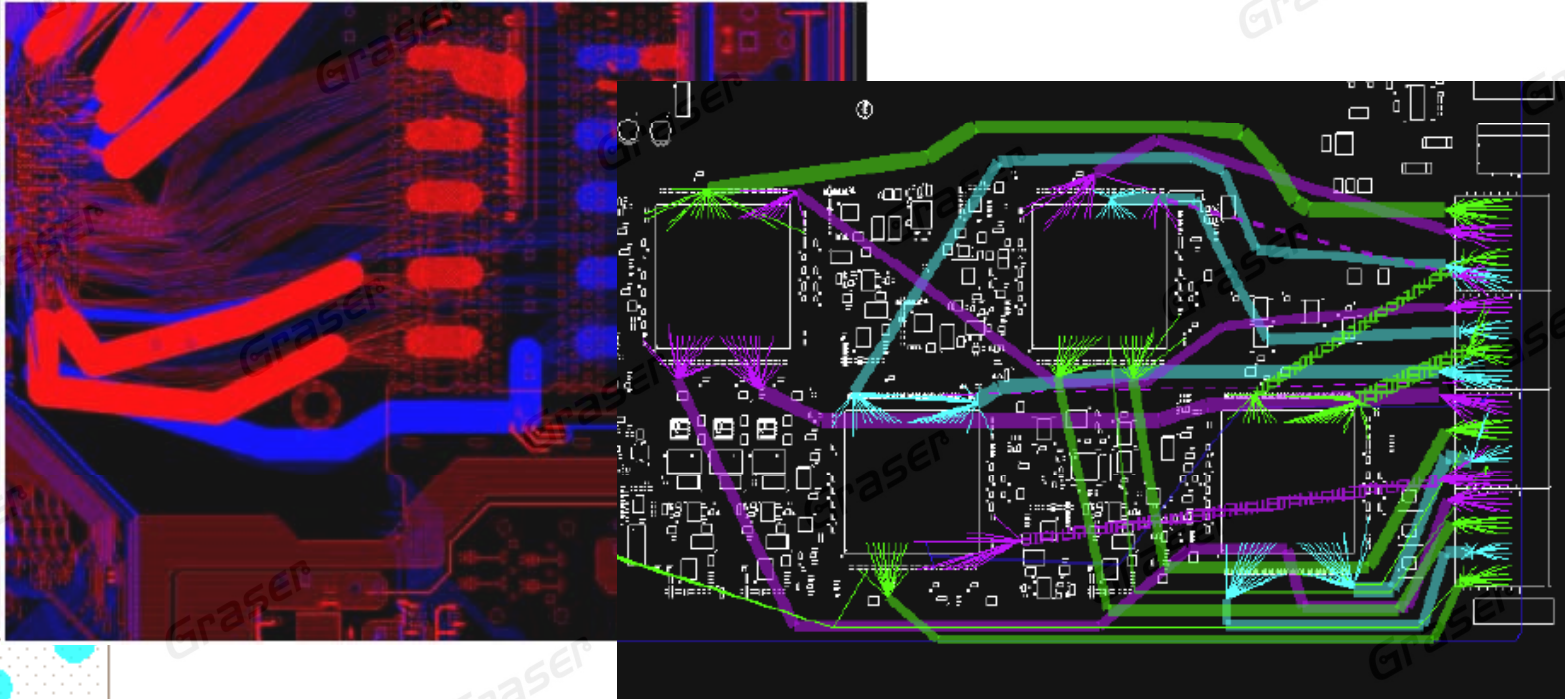
Options



After

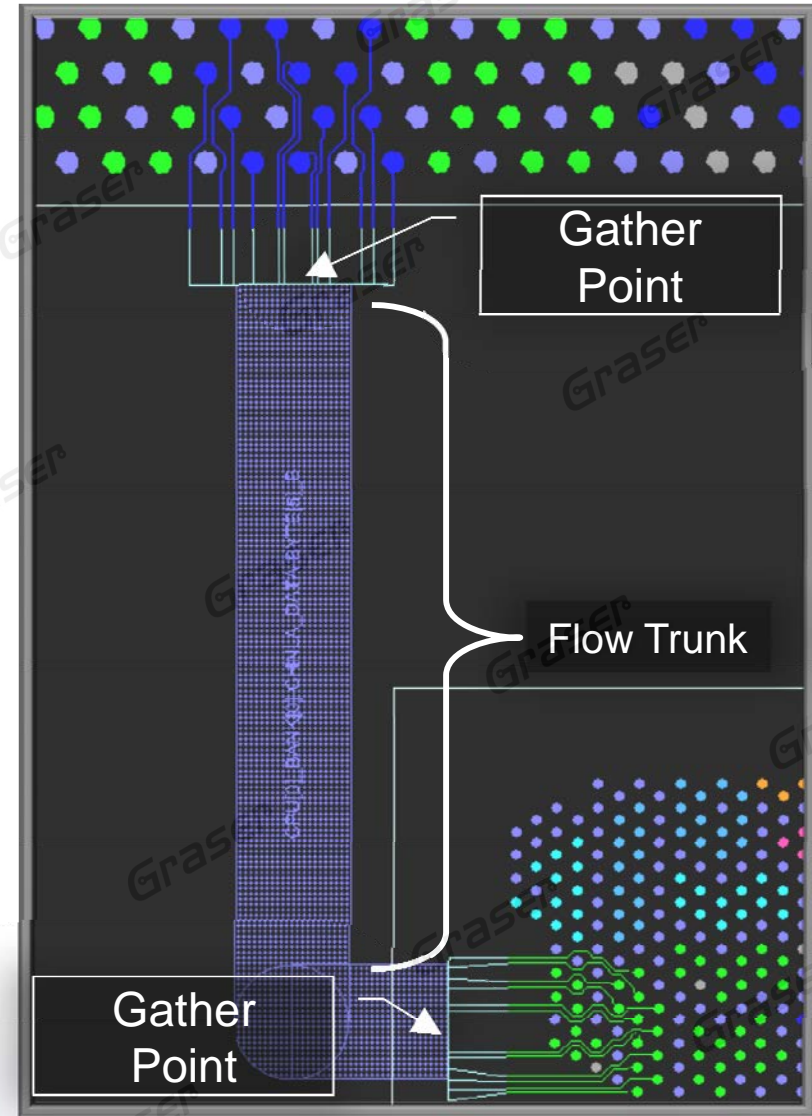
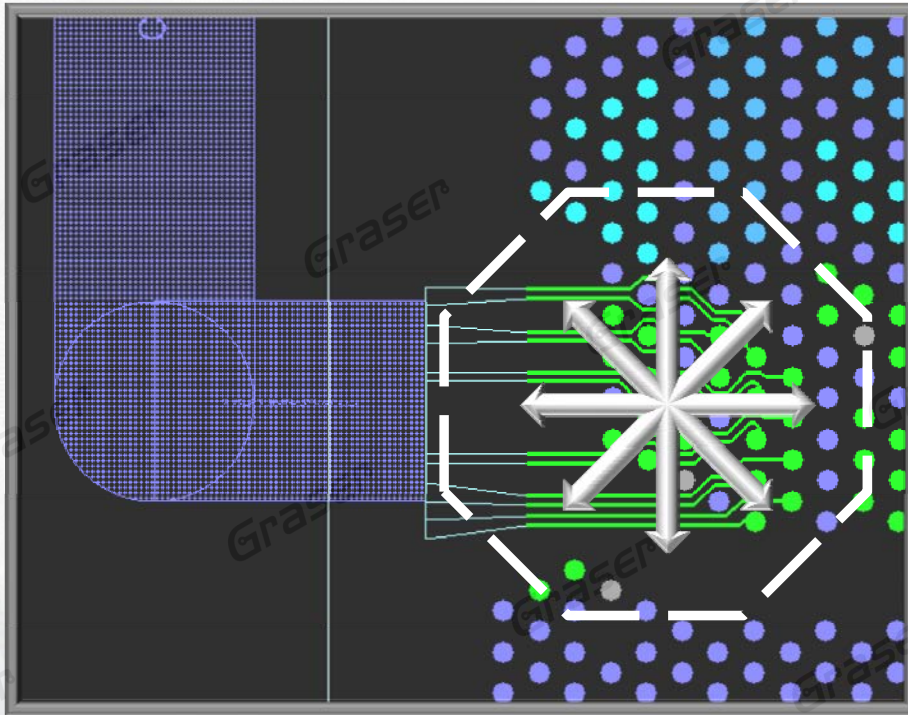


Flow Planning



Auto-interactive Breakout (AiBT)

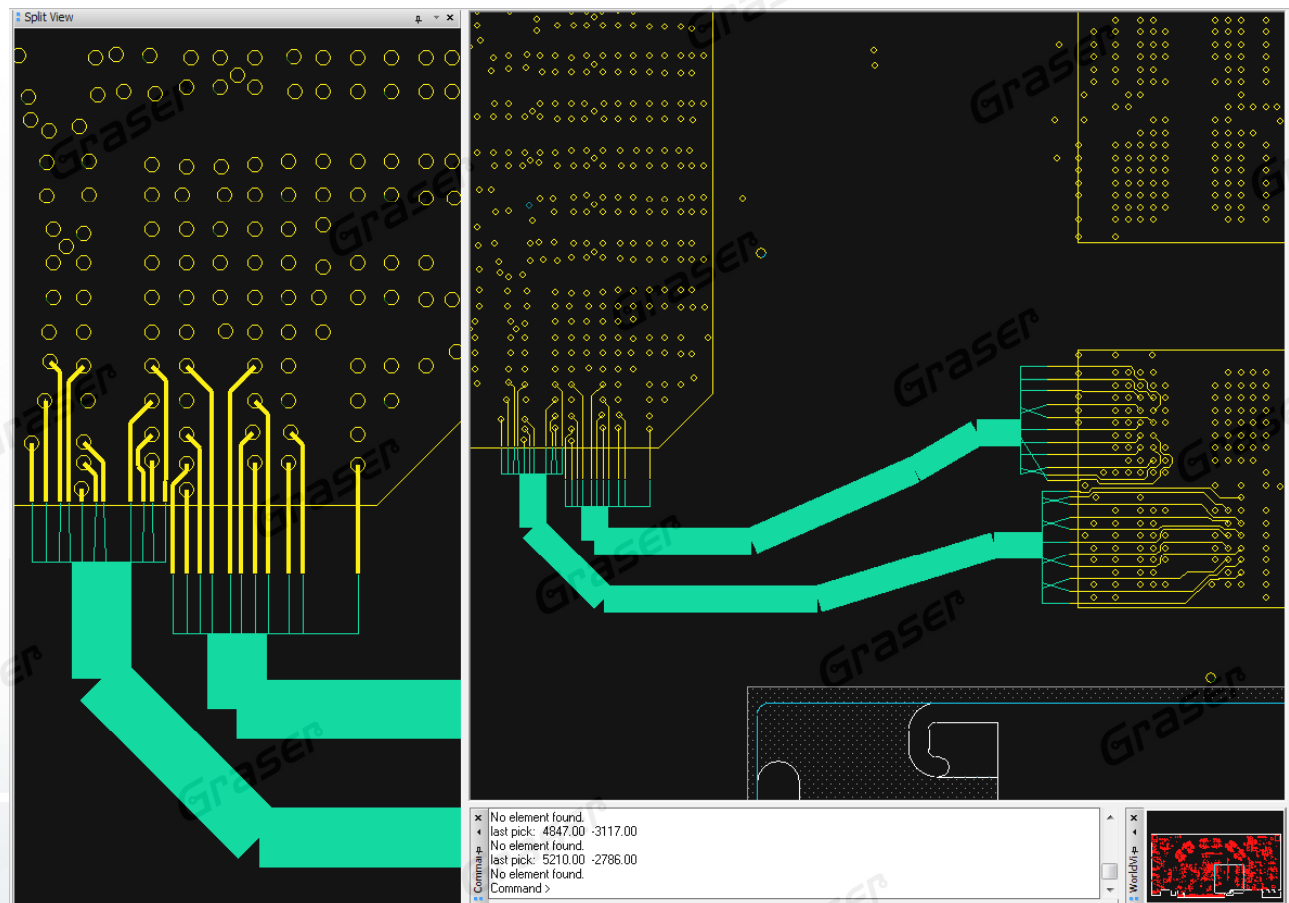
- **Rotation (8 “Pre-Defined”)**
 - Determines Breakout Direction
- **Location**
 - Determines Breakout Length



Auto-interactive Breakout (AiBT)



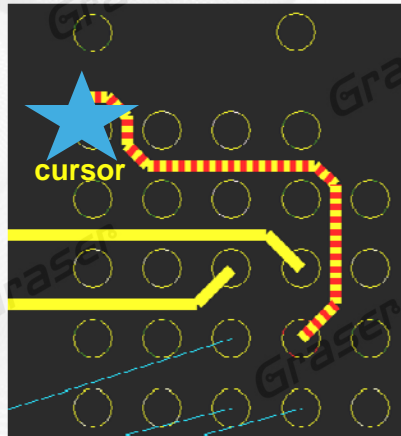
- **Automatic breakout routing**
 - Canvas driven inputs for direction, distance, sequence, layer
- **Rat management**
 - Ordering & layering
- **Split Views**
 - Work both sides



Auto-interactive Add Connect (AiAC)

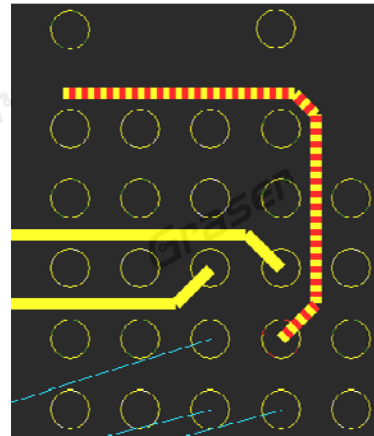
- Manual Mode

- Simple direct path to cursor and avoiding DRCs

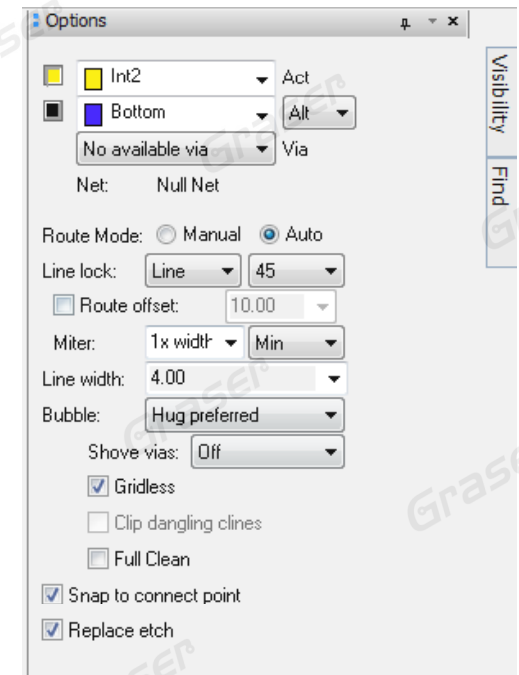
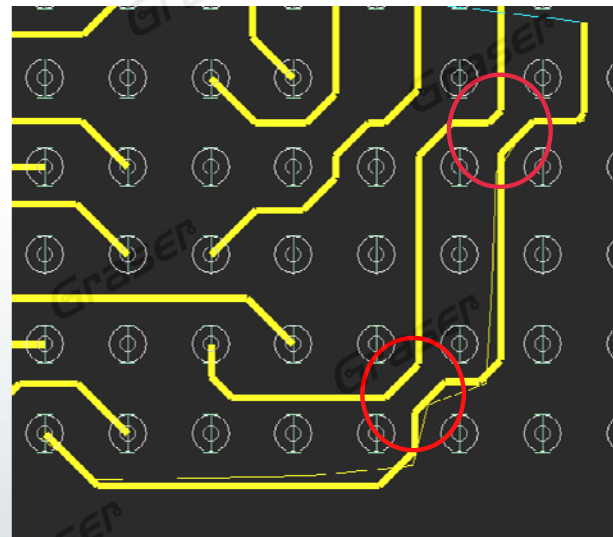
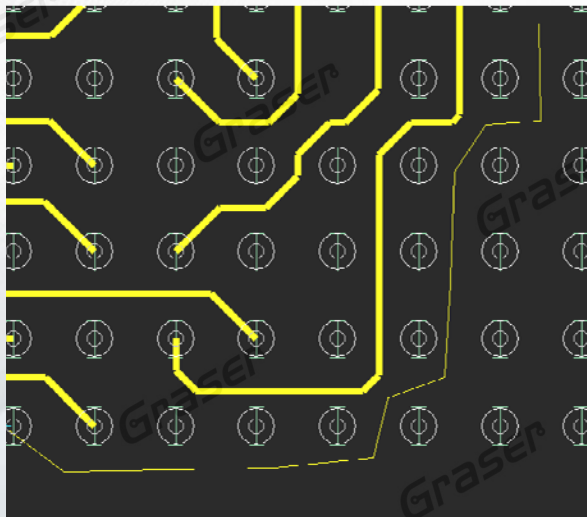


- Auto Mode

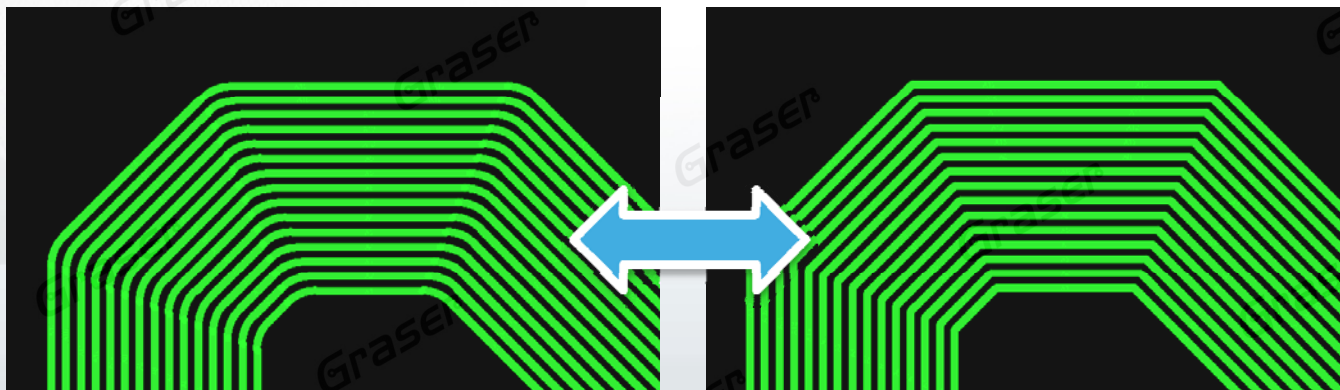
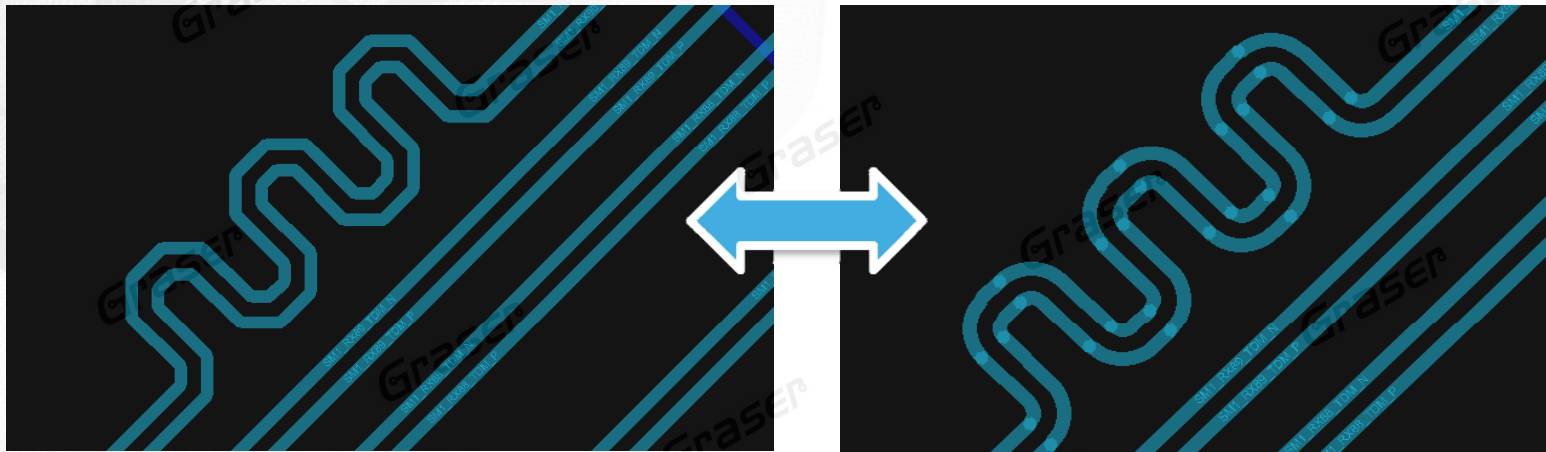
- Auto-routed low cost path and avoiding DRCs



- Scribble Mode

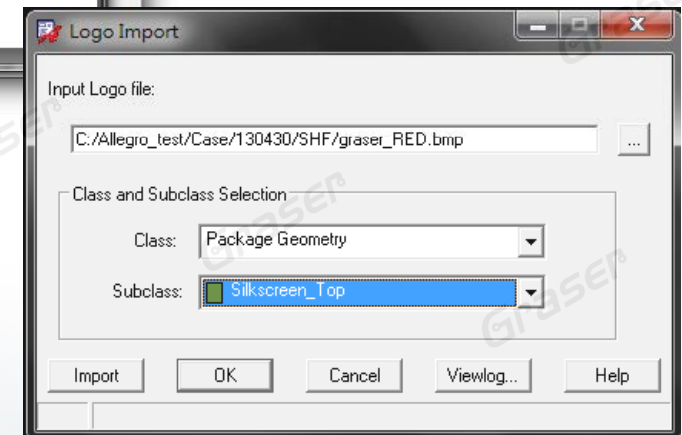
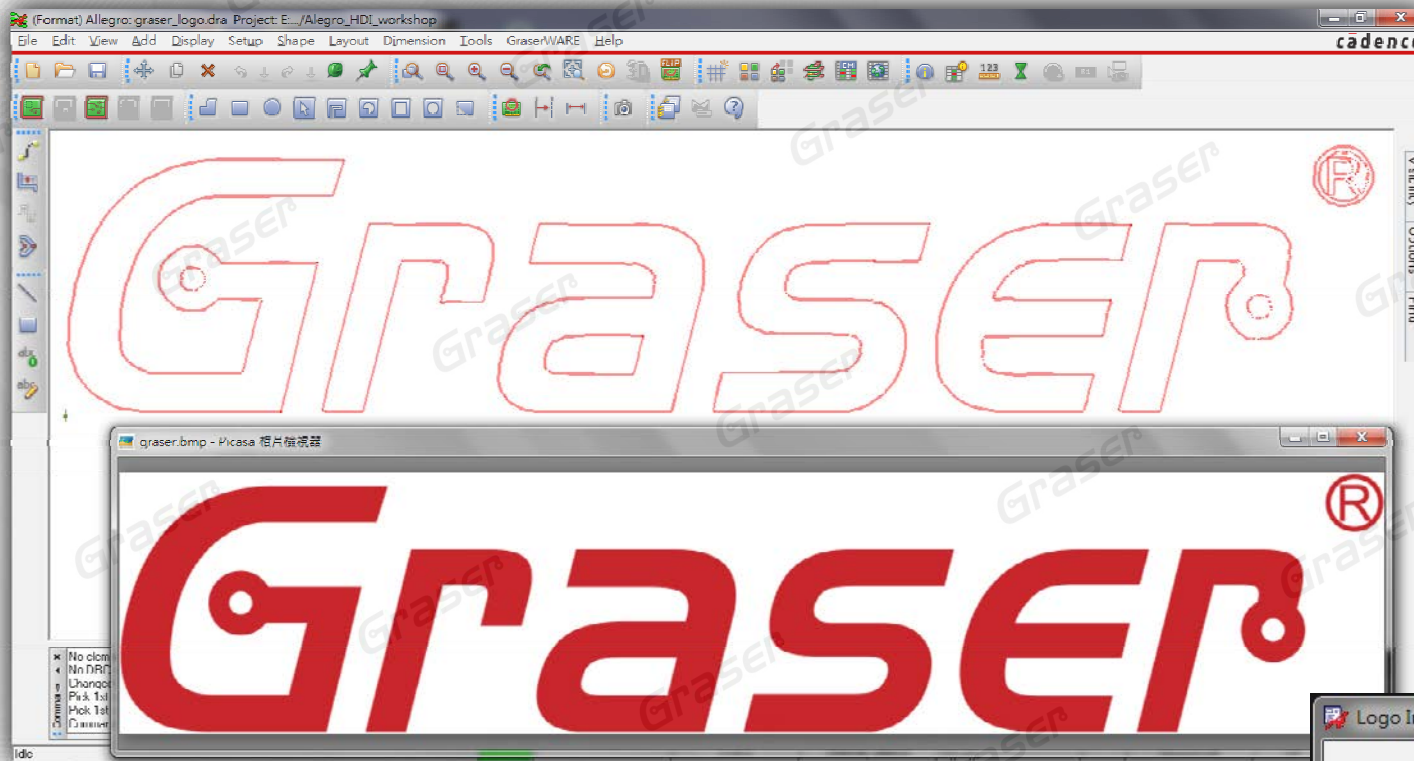


Auto-interactive Convert Corner(AiCC)

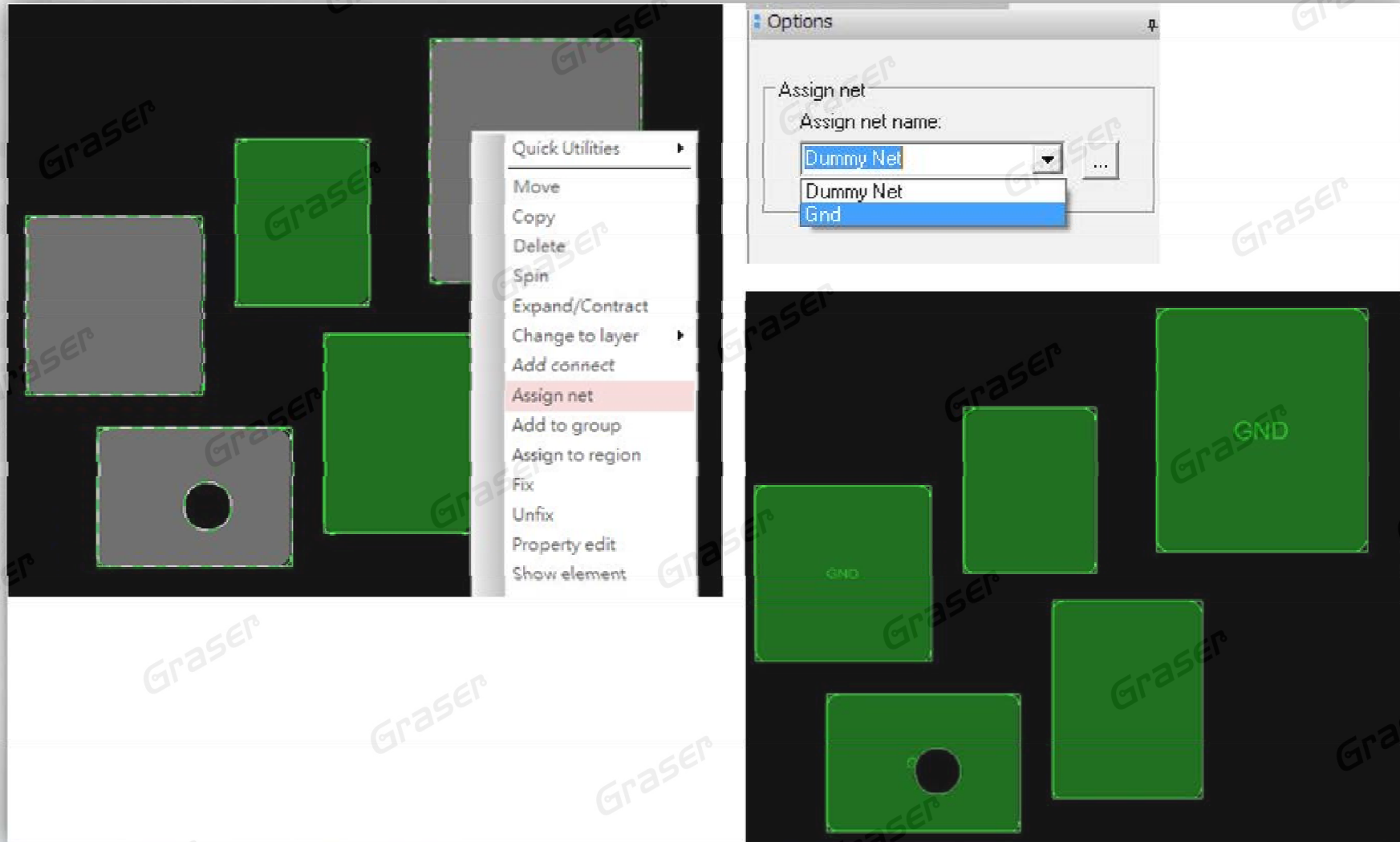


What's New in 16.6 Super HotFix

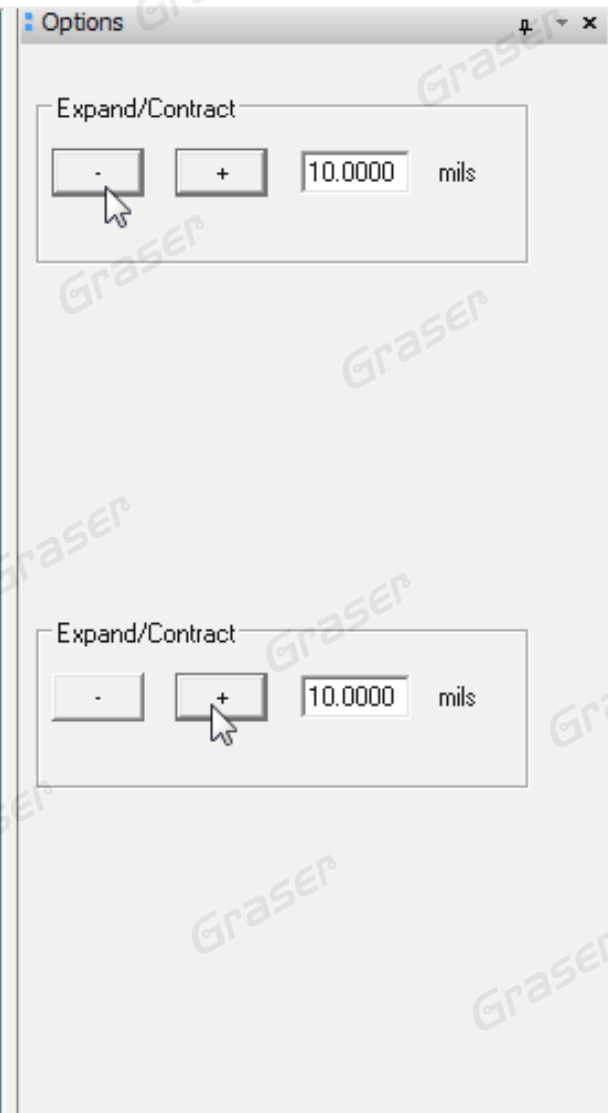
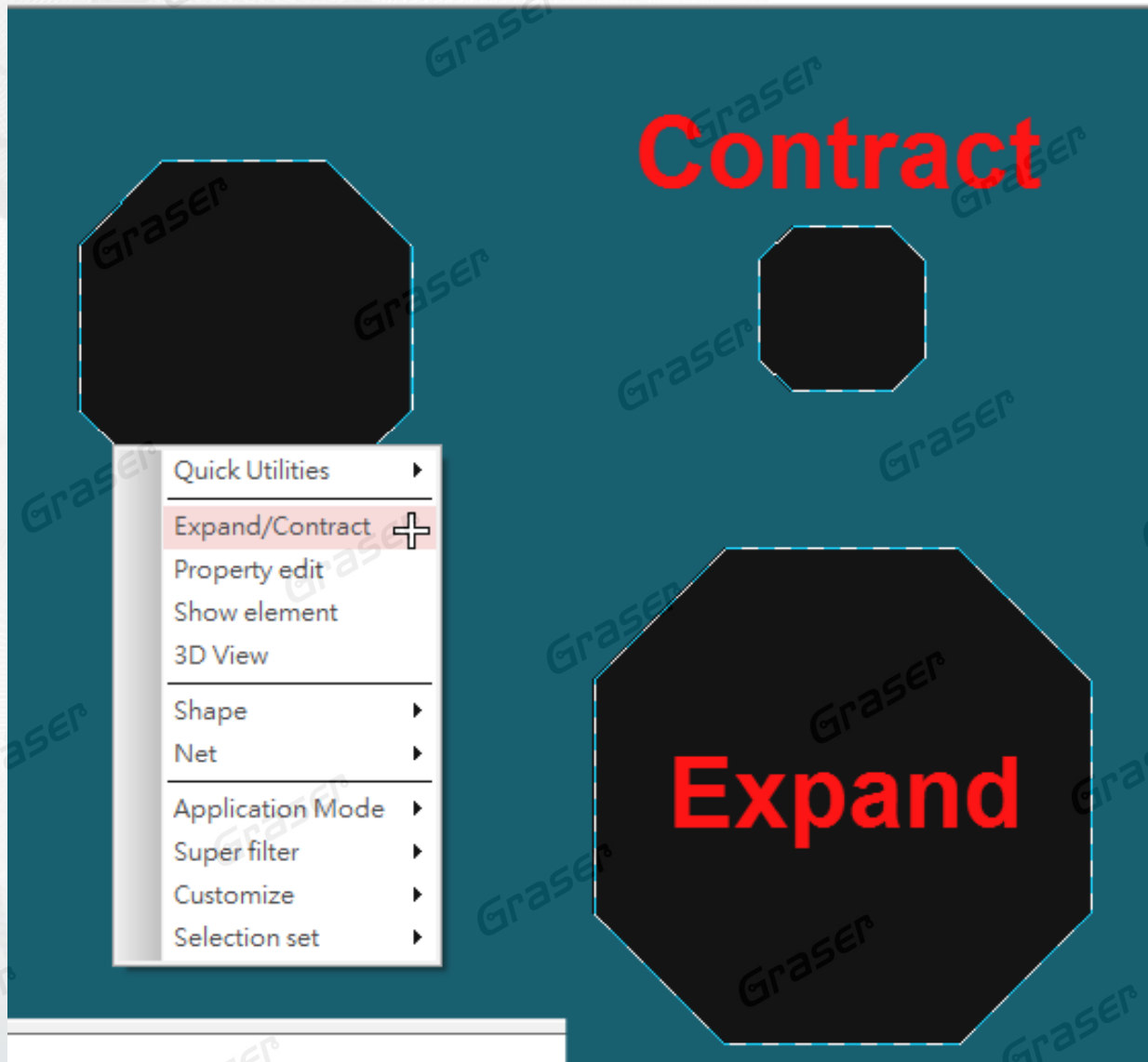
Logo Import



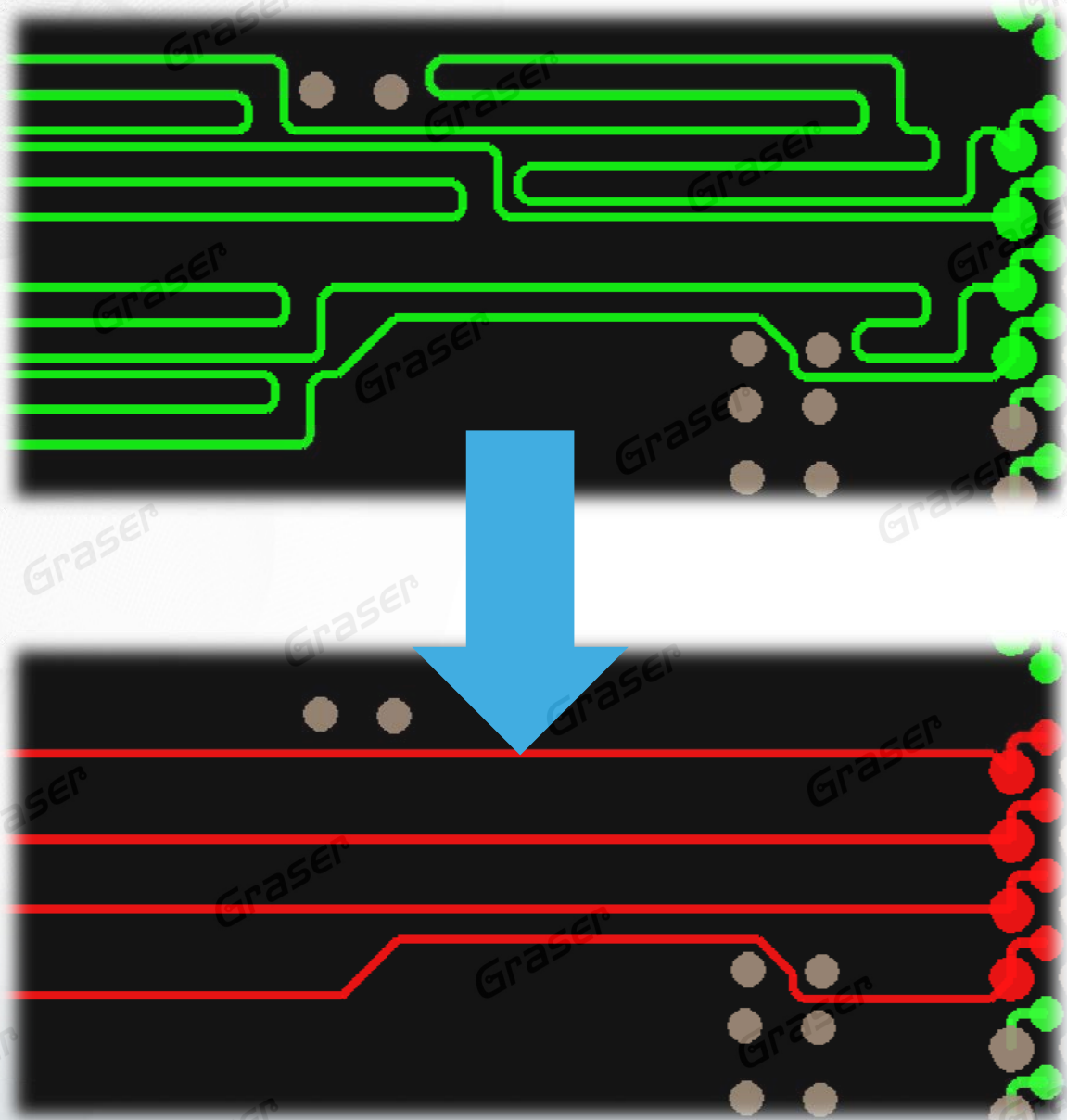
Net Assignment to Multiple Shapes



Expand / Contract Voids in Shapes



Detune

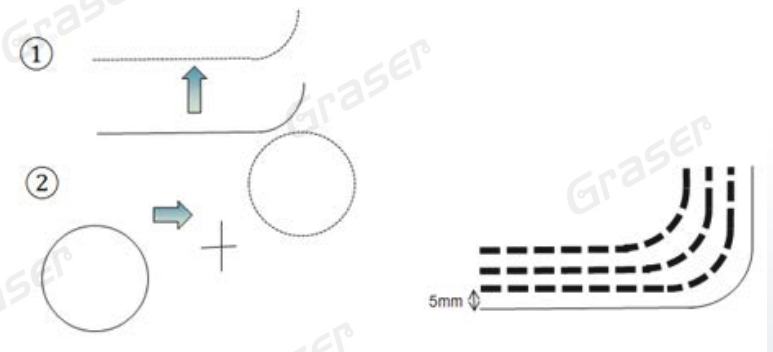
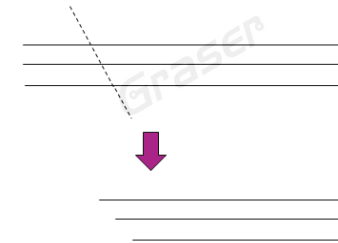
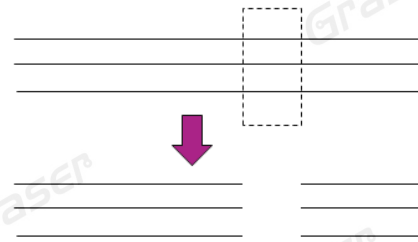


Drafting Enhancements

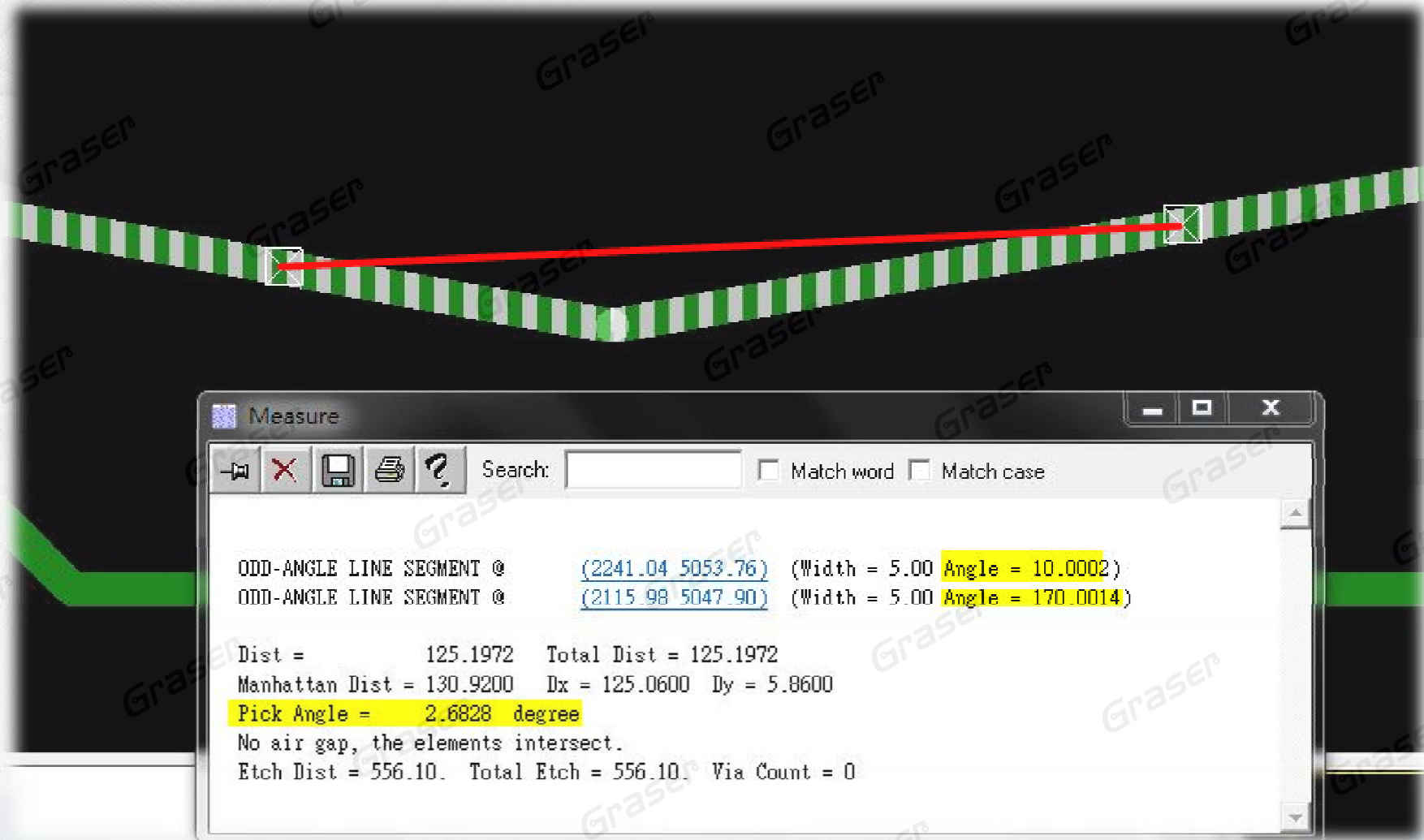
For customers who create advanced manufacturing / documentation package for their PCB designs

Shortens time to create documentation package

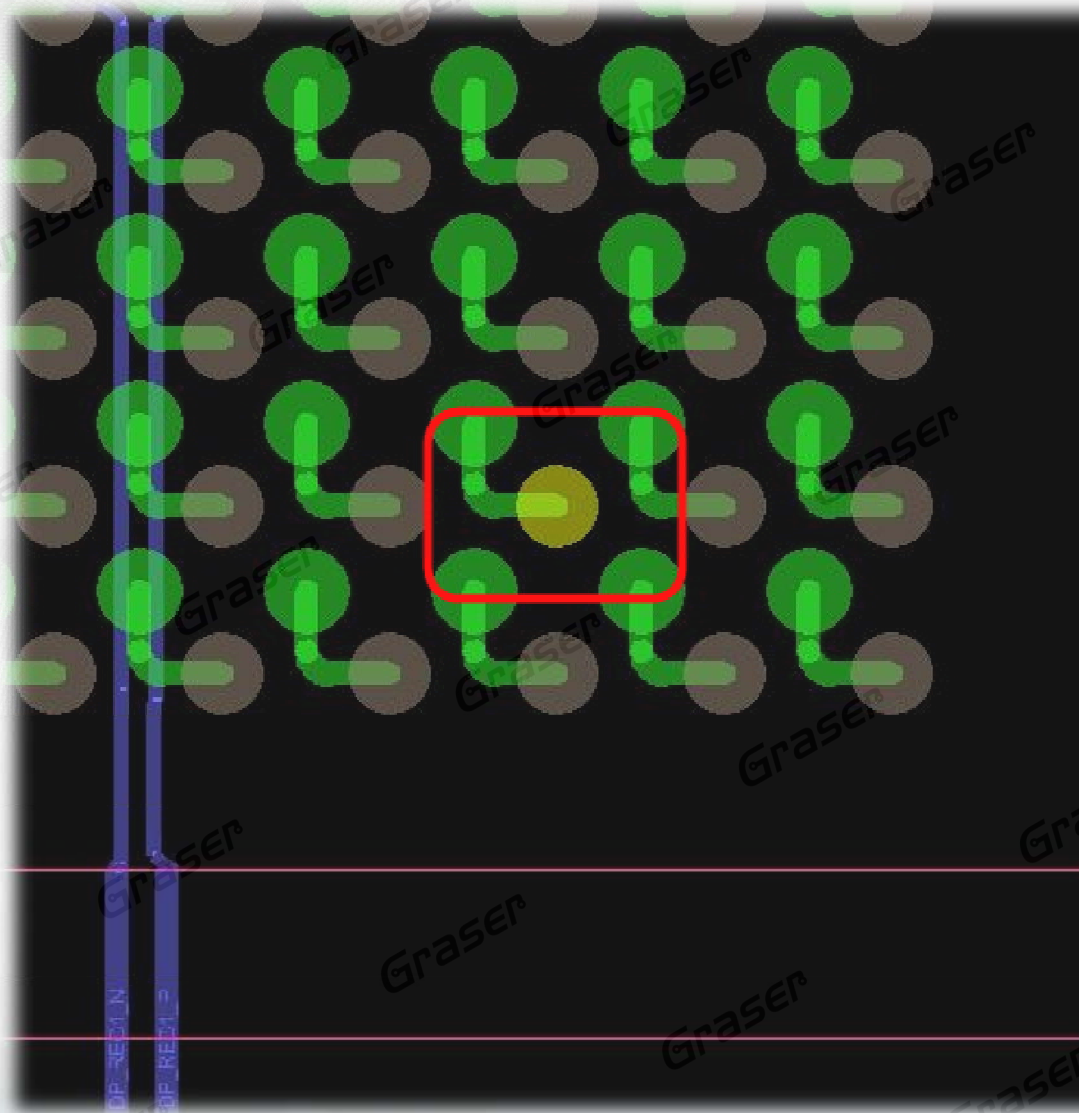
- Cut by area
 - Delete line segments inside area
- Trim by line intersection
 - Delete segment on either side of intersecting line
- Offset Copy / Offset Move
 - Parameters to control offset distance, line style, width, repeated instances



Measure Support of Angle



Highlight to Vias



Options

Selected color

Highlight Pattern: Solid

Selected pattern

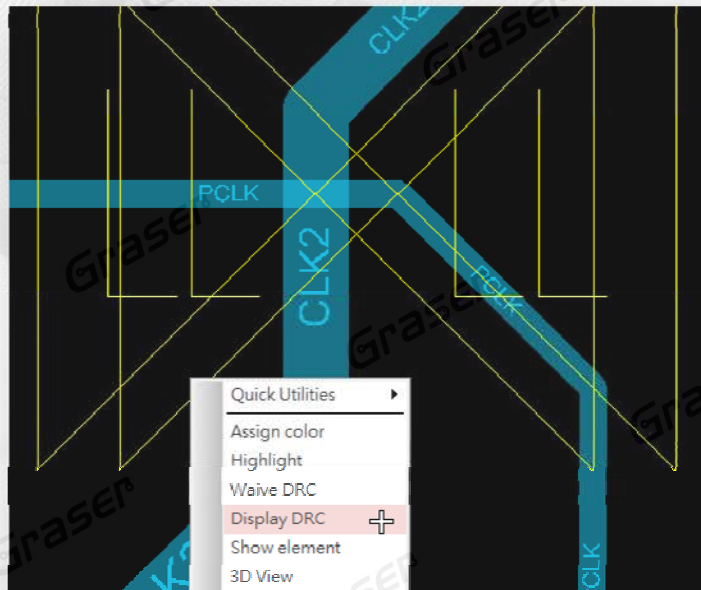
Find

Design Object Find Filter

All On All Off

- Groups
- Comps
- Symbols
- Functions
- Nets
- Pins
- Vias
- Shapes
- Voids/Cavities
- Dline segs
- Other segs
- Figures
- DRC errors
- Text

DRC Marker - Link to Constraint Manager



was Performance L) 16.6) [cds_routed_Rat_165_GROUPSSS] - [DRCs: Spacing [cds_routed_Rat_165_GR]

indow Help

Objects	Constraint Set	DRC Subclass	Values		Object 1	Object 2
			Required	Actual		
cds_routed_Rat_165_GROUPS						
Line to Line Spacing (3)						
Line to SMD Pin Spacing (1)						
(525.00 3362.50)	Default	Top	5 MIL	0 MIL	Vertical Line Seg...	Pin "U9.8 (Reset)"

Worksheet selector

- Electrical
- Physical
- Spacing
- Same Net Spacing
- Properties
- DRC**
 - Electrical
 - Physical
 - Spacing
 - Same Net Spacing
 - Design
 - External

New Reports

- Film Area



- Via per net
- Via per layer per net

Via List

Net Name	Total Vias	Through Vias	BB Vias	Micro Vias	Via Names
HDI_STACK	1	0	0	1	BB1-2
NET3	6	0	1	5	BB1-2, BB2-3, BB3-4, BB-CORE3-6
NET9	4	0	1	3	BB1-2, BB2-3, BB3-4, BB-CORE3-6
NET14	3	0	0	3	BB7-8
NET15	2	0	0	2	BB7-8
NET17	1	0	0	1	BB1-2
NET20	1	0	0	1	BB1-2
NET30	17	0	4	13	BB1-2, BB2-3, BB-CORE3-6, BB-CORE3-6
NET31	4	0	1	3	BB1-2, BB2-3, BB3-4, BB-CORE3-6
NET34	5	0	1	4	BB1-2, BB2-3, BB-CORE3-6, BB-CORE3-6
PECL1_P	7	0	1	6	BB1-2, BB2-3, BB3-4, BB-CORE3-6
Totals	51	0	9	42	

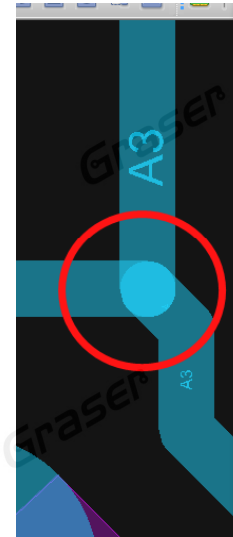
Via per net

Via List

Layer	Net Name	Total Vias	Through Vias	BB Vias	Micro Vias	Via Names
TOP	HDI_STACK	1	0	0	1	BB1-2
	NET3	1	0	0	1	BB1-2
	NET9	1	0	0	1	BB1-2
	NET17	1	0	0	1	BB1-2
	NET20	1	0	0	1	DD1-2
	NET30	4	0	0	4	BB1-2
	NET31	1	0	0	1	BB1-2
	NET34	1	0	0	1	BB1-2
	PECL1_P	1	0	0	1	BB1-2
Totals		12	0	0	12	
SIGNAL 2	HDI_STACK	1	0	0	1	BB1-2
	NET3	2	0	0	2	BB1-2, BB2-3
	NET9	2	0	0	2	BB1-2, BB2-3
	NET17	3	0	0	3	BB1-2
	NET20	1	0	0	1	BB1-2
	NET30	8	0	0	8	BB1-2, BB2-3
	NET31	2	0	0	2	BB1-2, BB2-3
	NET34	2	0	0	2	BB1-2, BB2-3
	PECL1_P	3	0	0	3	BB1-2, BB2-3

Via per layer per net

- Missing Fillets



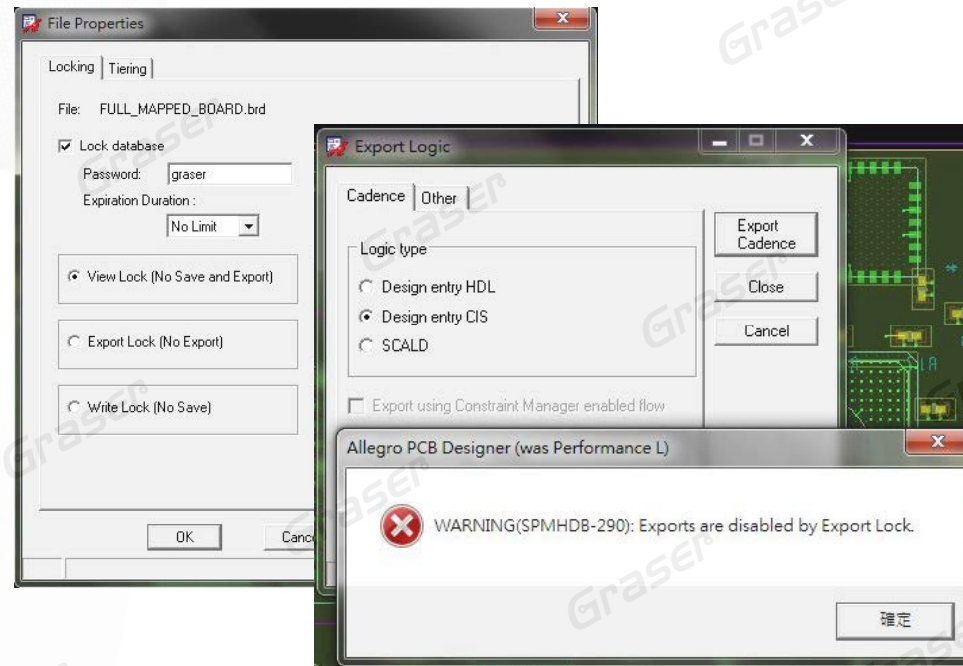
Missing Fillets

Subclass	Net	Item	Location	Partial
BOTTOM	CLK3-	VIA	(801.50 2925.00)	yes
BOTTOM	CLK4+	T	(1316.00 2965.00)	
BOTTOM	GND	VIA	(2330.50 2983.00)	
BOTTOM	GND	VIA	(369.50 3117.00)	
BOTTOM	GND	VIA	(480.50 3413.00)	
BOTTOM	W_R	VIA	(800.00 1308.00)	yes
TOP	A1	SYMBOL PIN	(1348.00 2550.00)	
TOP	A1	SYMBOL PIN	(1580.00 1360.00)	
TOP	A1	T	(811.49 690.50)	
TOP	A1	VIA	(811.49 690.52)	
TOP	A10	SYMBOL PIN	(902.00 2300.00)	
TOP	A13	SYMBOL PIN	(1225.00 2177.00)	
TOP	A3	SYMBOL PIN	(902.00 800.00)	
TOP	A3	T	(1292.00 2475.00)	
TOP	A3	T	(869.50 920.49)	
TOP	A4	SYMBOL PIN	(902.00 850.00)	
TOP	A7	T	(1305.00 2240.00)	
TOP	ADDR5	SYMBOL PIN	(1692.50 3420.00)	
TOP	CLK2	SYMBOL PIN	(1580.00 1438.00)	
TOP	CLK2	SYMBOL PIN	(1580.00 1438.00)	
TOP	D1	SYMBOL PIN	(315.00 2050.00)	

Database Locks / Tiering

Database Locks

- View Only
- No Export
- No Save



Database Tiering

The following capabilities will be checked:

- All electrical DRC modes
- Differential pair static and dynamic phase control
- Pin Delay
- Via Z
- Constraint Regions
- Micro via padstacks
- Embedded layers
- Dynamic fillets

