

High-Speed Option (AiDT)

PEGATRON

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CAE

Agenda

Timing Vision

Auto-interactive Delay Tuning (AiDT)

PIN_DELAY

Timing Vision

Design Parameters

The screenshot displays the 'Design Parameter Editor' window with several panels:

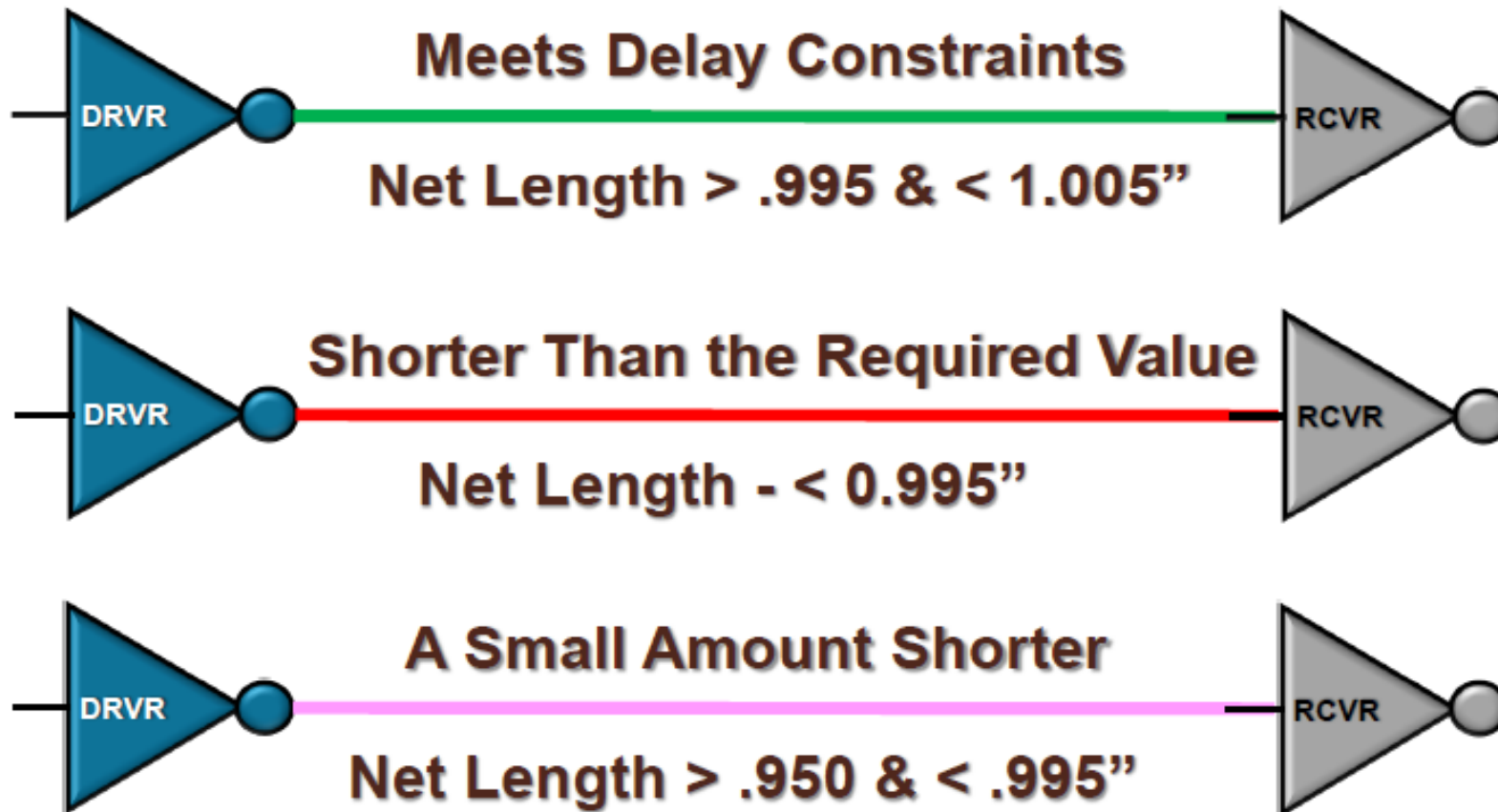
- Commands:** A list of design commands including Add Connect, Delay Tune, Edit Vertex, Slide, Auto-I. Delay Tune, Timing Vision, Auto-I. Convert Corner, Gloss, and Create Fanout.
- Display control (Left):** Style: Solid Striped. Colors: Satisfies required timing (green), Shorter than required value (red), A small amount shorter (pink), Longer than required value (blue), A small amount longer (grey). Pattern for critical signals: (diagonal lines).
- Timing Control (Left):** Data: DRC Smart Off. Mode: Timing Phase. Minimum for Smart Goal calc (% of total length): .
- Display control (Right):** Style: Solid Striped. Colors: Satisfies required timing (green), Shorter than required value (red), A small amount shorter (pink), Longer than required value (blue), A small amount longer (grey). Pattern for critical signals: (diagonal lines).
- Timing Control (Right):** Data: DRC Smart Off. Mode: Timing Phase. Minimum for Smart Goal calc (% of total length): .

A large yellow arrow points from the right-side panels towards the left-side panels.

Parameter description
Select an etch edit command to display its parameters.

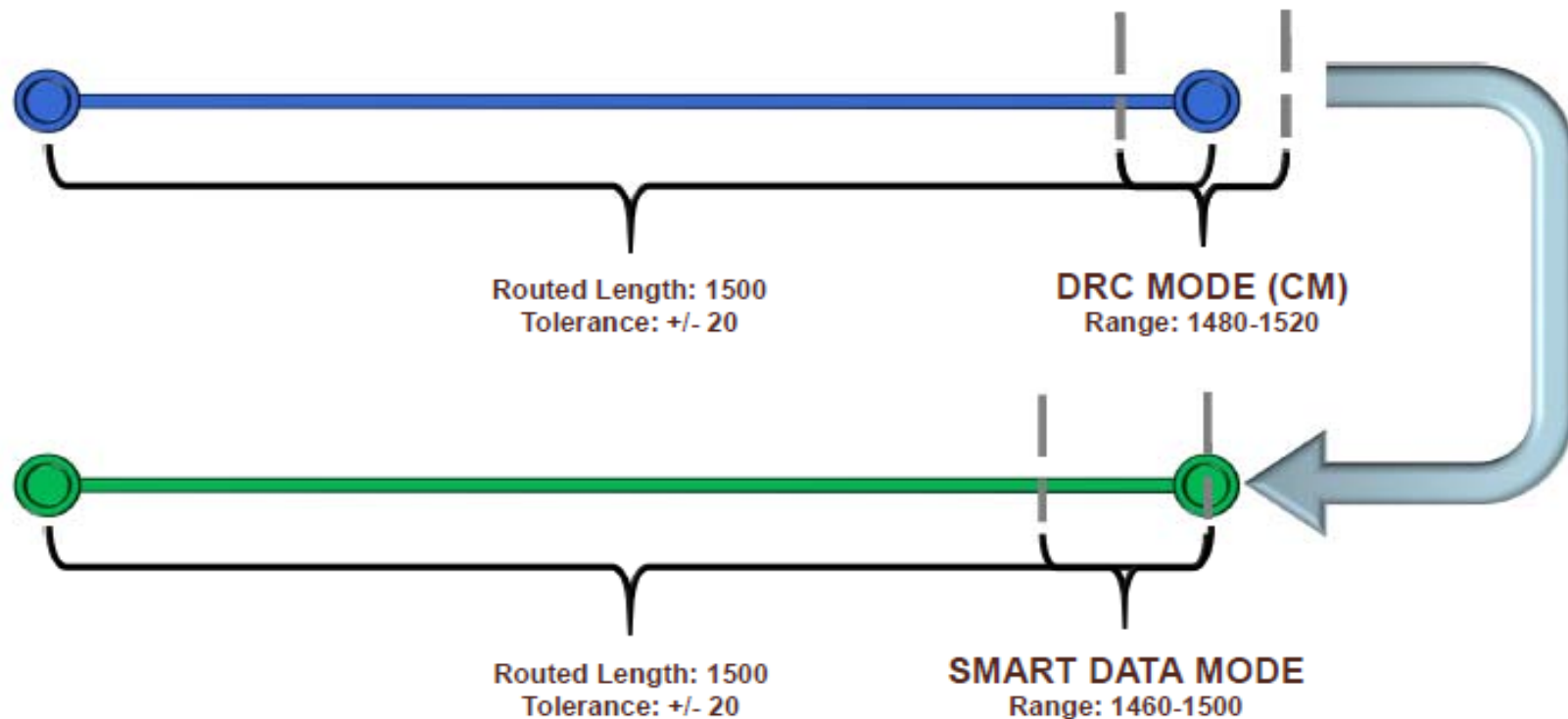
Timing Vision

Color Delay Example 1.000" Delay Requirement +/- .005



Timing Vision

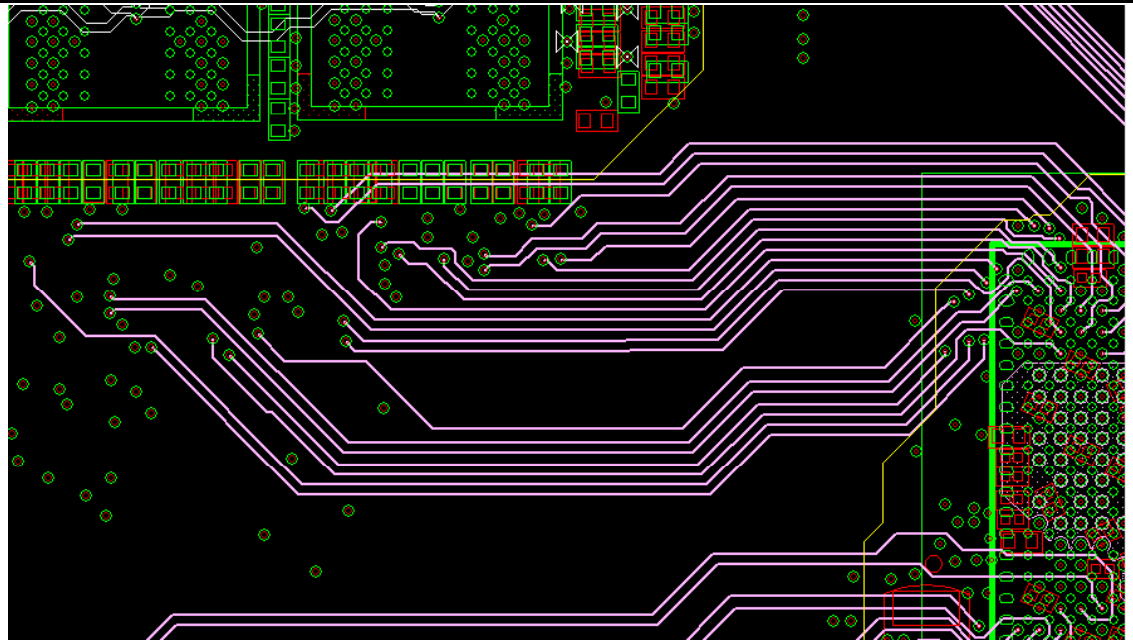
Routing Methodologies Timing Vision Calculation Methods - DRC vs. SMART DATA



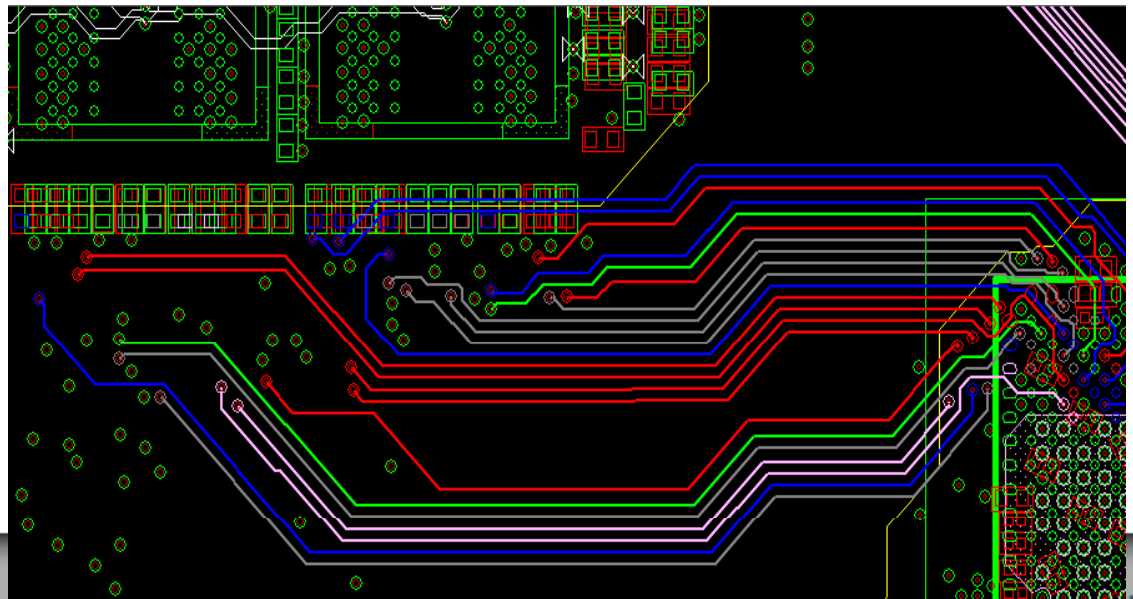
SMART DATA's Concept is to Keep All Routes As Short as Possible!

Timing Vision

傳統的顯示方式不易
得知是否符合
constraint



Timing Vision可直接
顯示實際constraint
的情況



Timing Vision

Strength

- Cline上即時顯示timing的資訊.
- 減少往來 Constraint Manager 與 show element時間.
- 支援使用者定義
 - Color
 - stipple patterns

```
Net "Ddr3_G2_Dqs2_Dp" Length: 1799.9 MIL
(Dly) (Xnet=DDR3_G2_DQS2_DP) R1604.2 to U96.C3 max= 800.00 length= 209.14 MIL
(Dly) (Xnet=DDR3_G2_DQS2_DP) U96.C3 to U67.AF26 max= 4000.00 length= 2402.46 MIL
(RDly) (Xnet=DDR3_G2_DQS2_DP) U96.C3 to U67.AF26 min= 2576.33 max= 2046.64 length= 2402.46 MIL
  grp= R_DDR3_G2_U67_U96
  target= (DDR3_G2_DQS2_DP) U96.C3 to U67.AF26
```

Limitation

- 無法儲存已設定之Timing group狀態.

Auto-Interactive Delay Tune (AiDT)

三種自動繞線模式

◉ **Single Cline Tuning**

- 針對單一走線。 (適用空間充足且不用推擠相鄰走線)

◉ **Cline Segment Tuning**

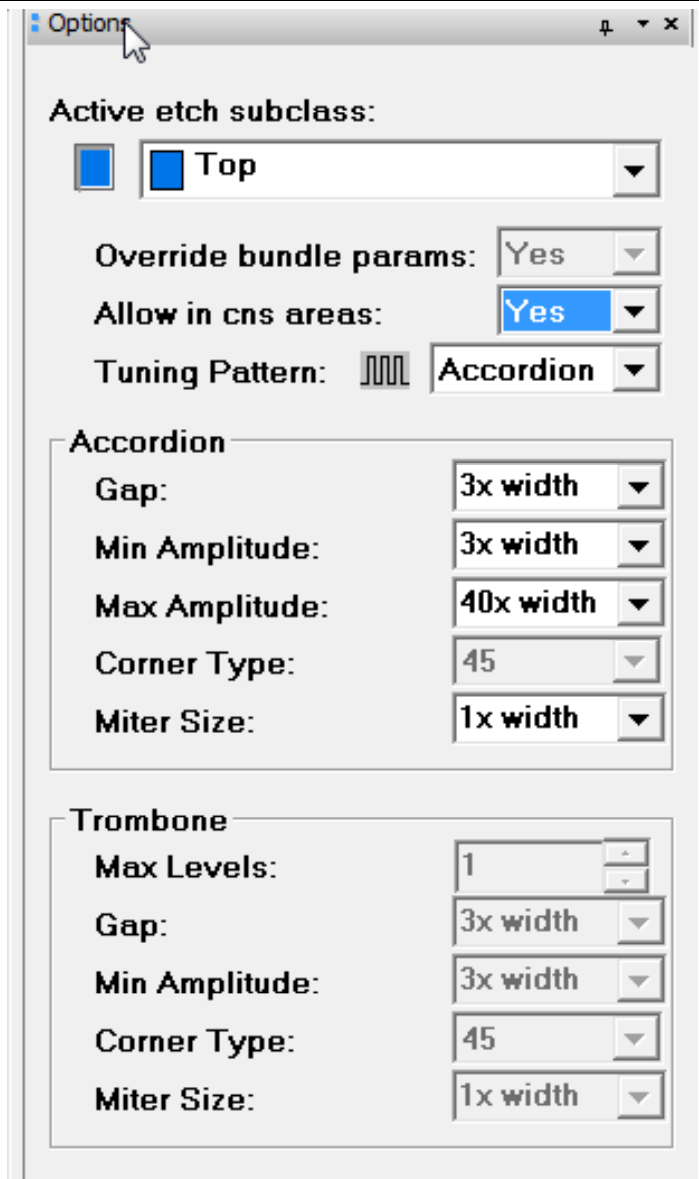
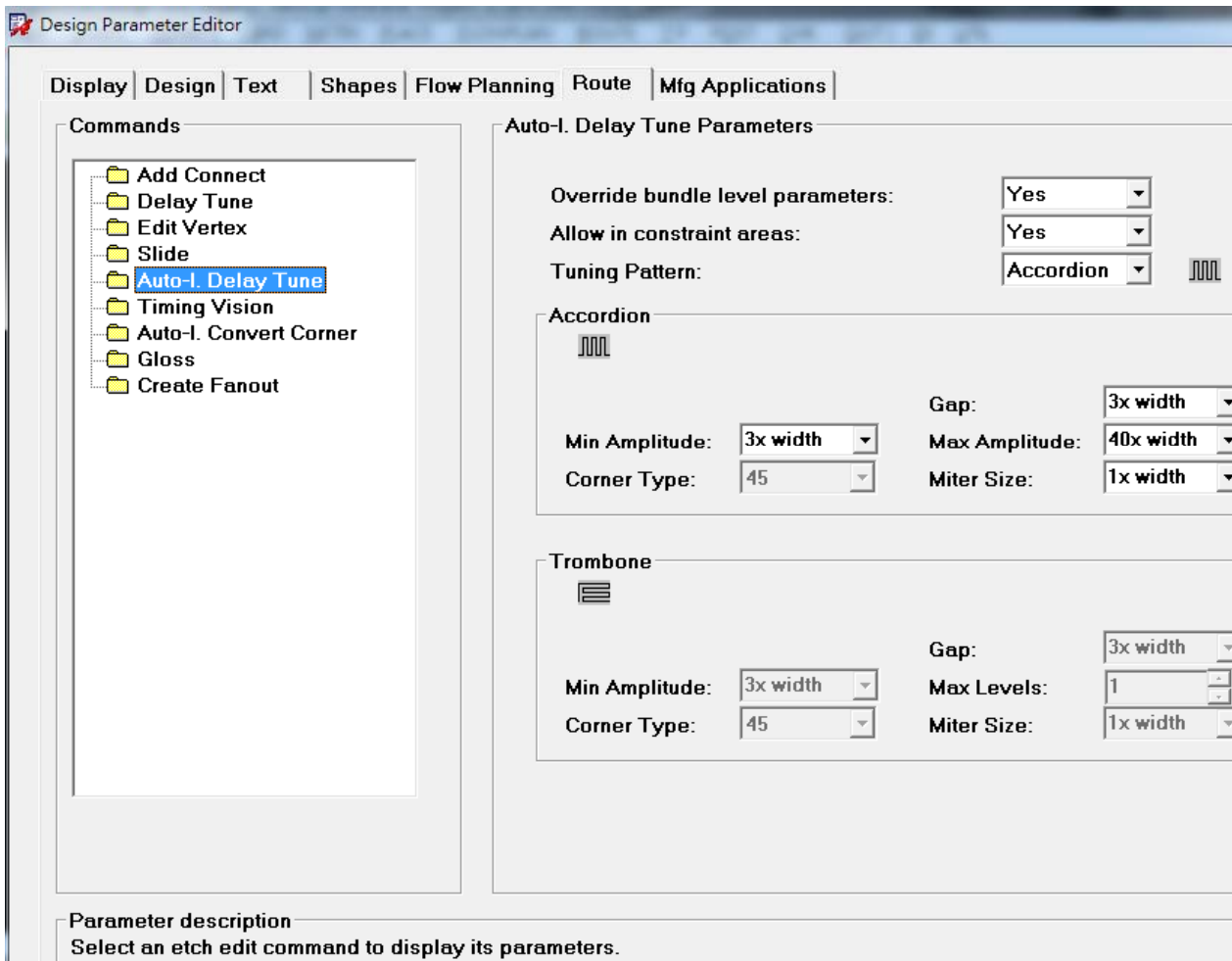
- 針Cline Segment。 (適用於部分繞線或推擠)

◉ **Tuning entire match group**

- 針對group中所有走線同時進行處理。 (適用於群組繞線)

Auto-Interactive Delay Tune (AiDT)

Design Parameters



Case 1 - Server extend board

Board Information

Layer : 10 (6L for routing)

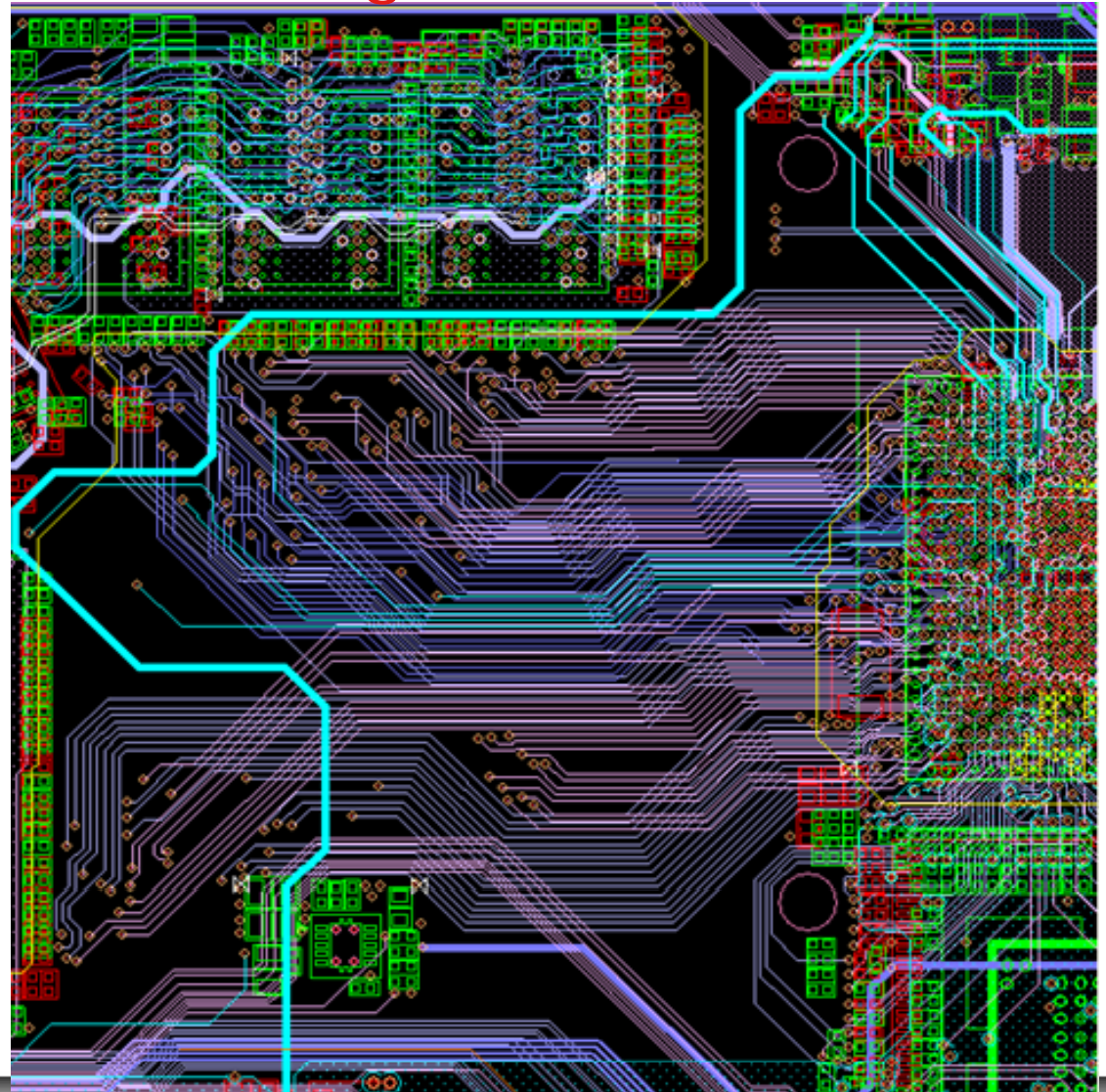
Size : 6.7x3.5 in^2

DDR : 12 chips

DDR3 routing constraints

CLK(0:1),DATA(0:63),DQS(0:7)
ECC(0:7),CTRL 14,CMD 14,QA
26,QB26,address(0:9)

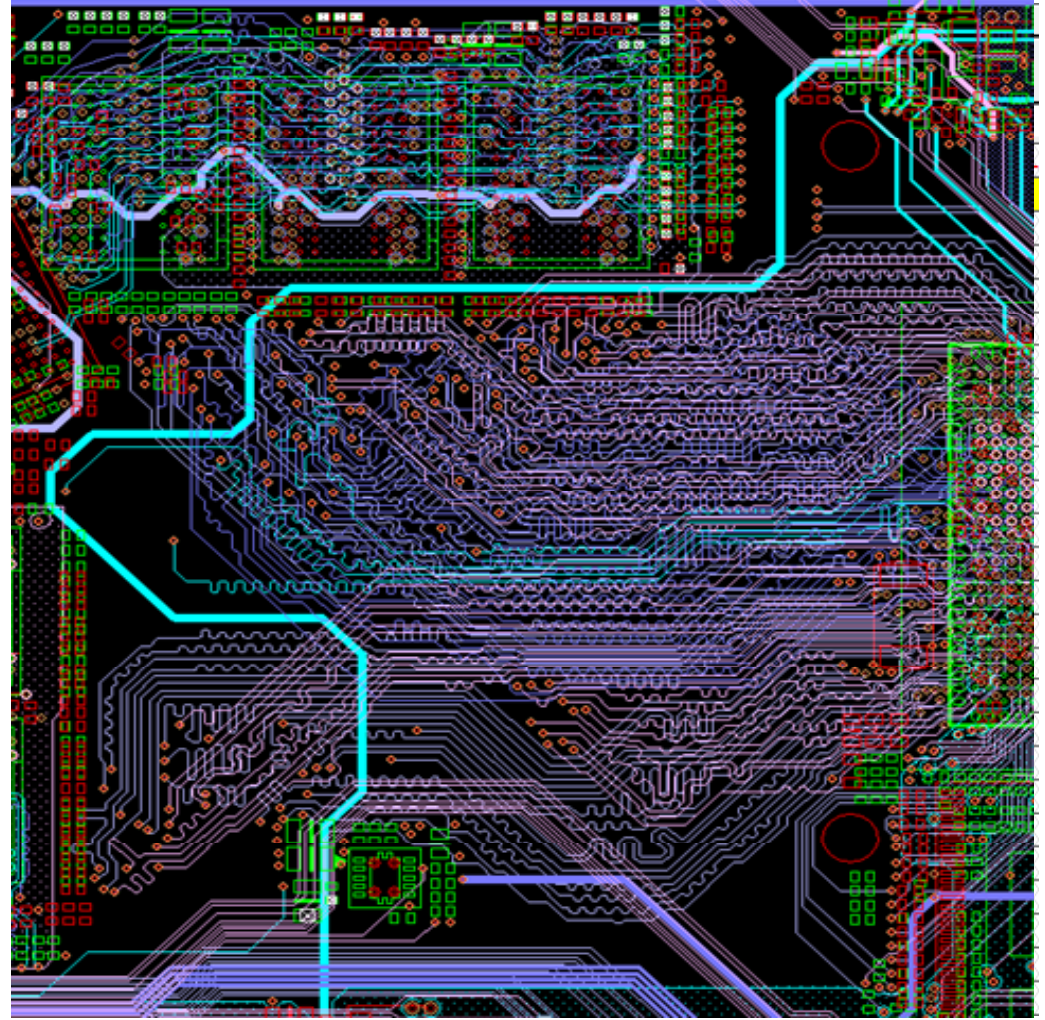
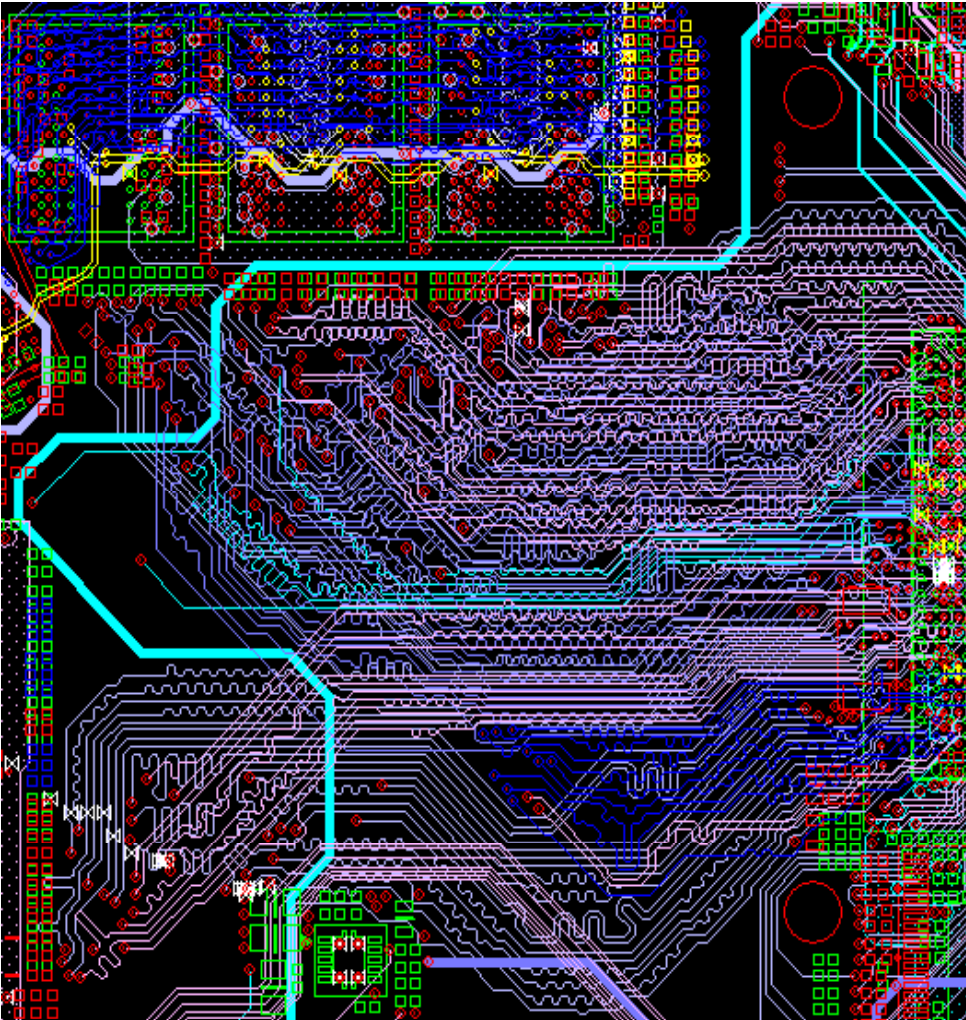
Original status



Case 1 - Server extend board

AiDT

manual editing after AiDT



Case 2 - Tablet PC

Board Information

Layer : 10 (6L for routing)

Size : 2.8x5.1 in^2

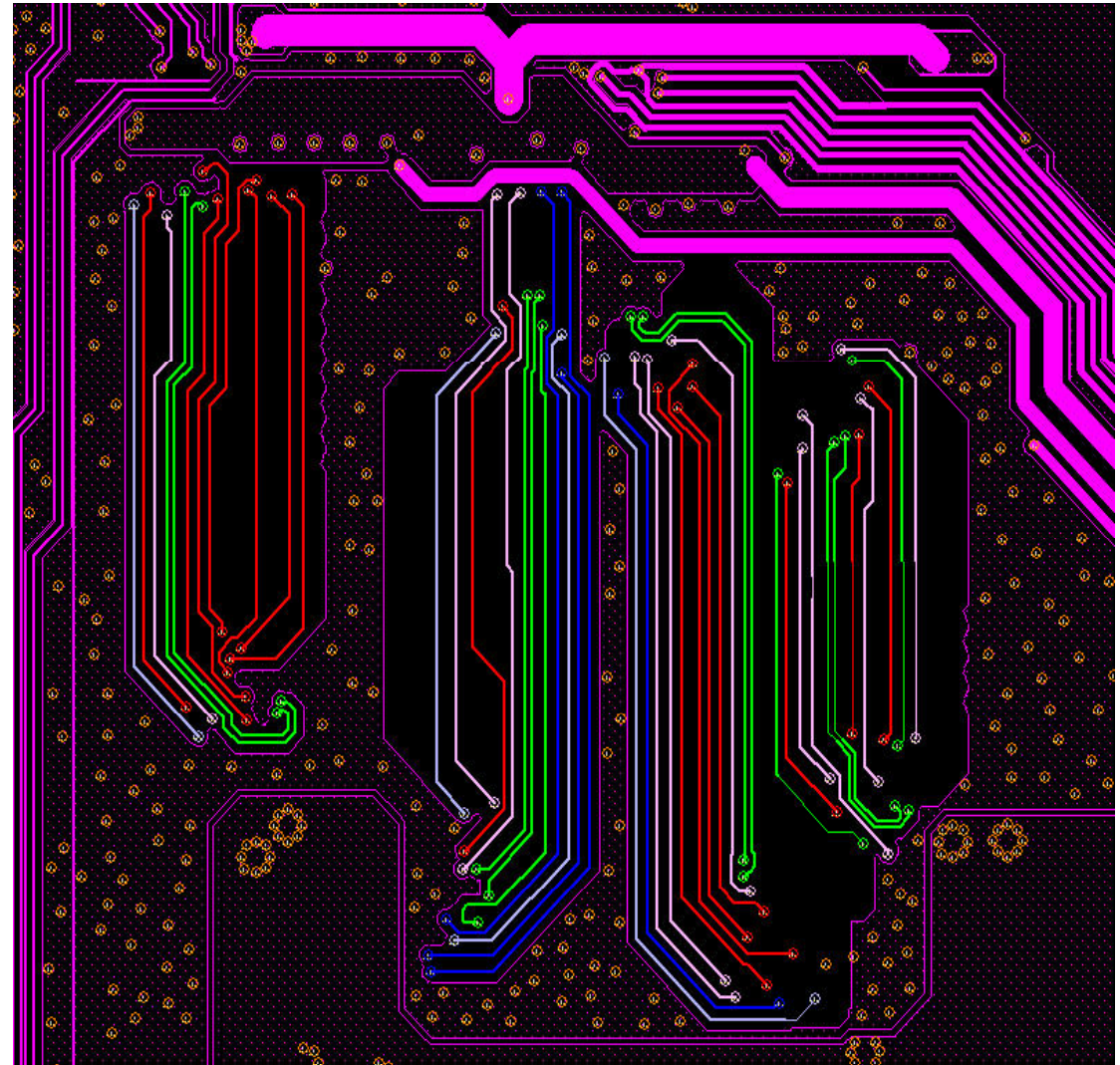
DDR : 2 chips

Low power DDR

DDR3 routing constraints

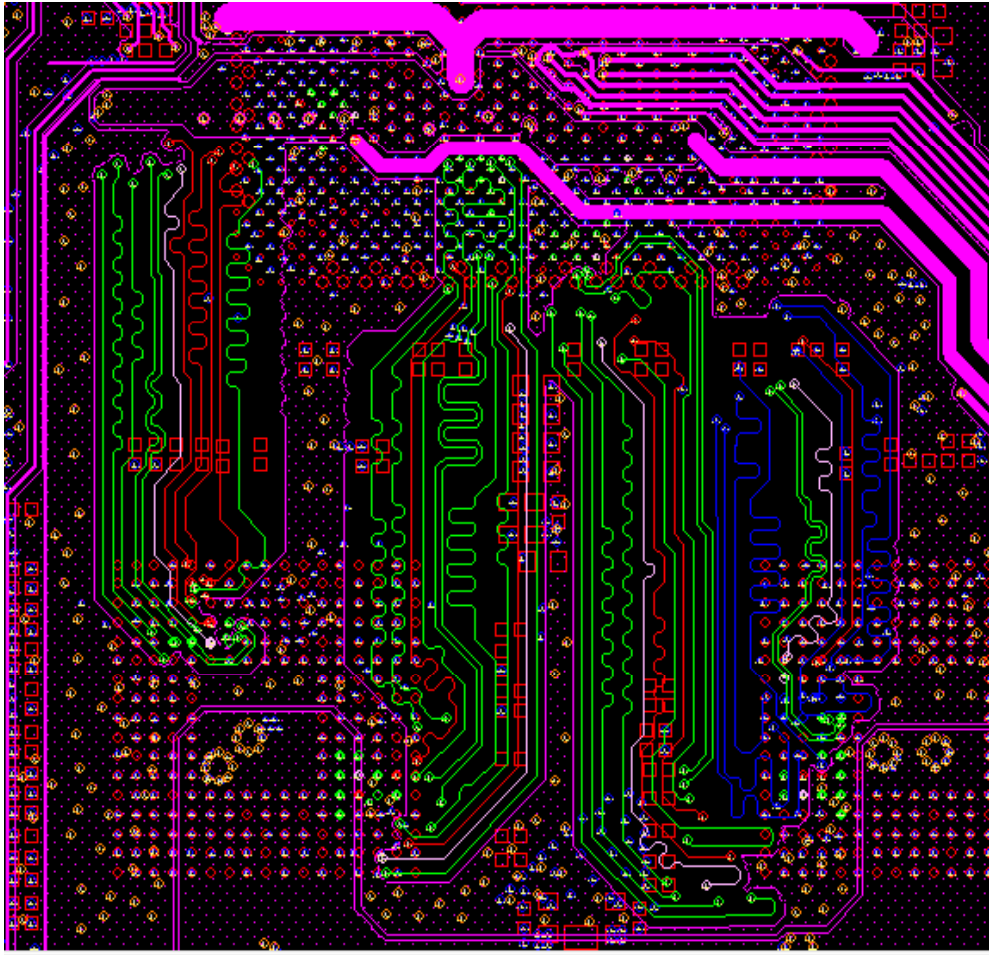
CLK(0:1),DATA(0:63),DQS(0:7)
DM(0:7),CTRL+CMD+address31

Original status

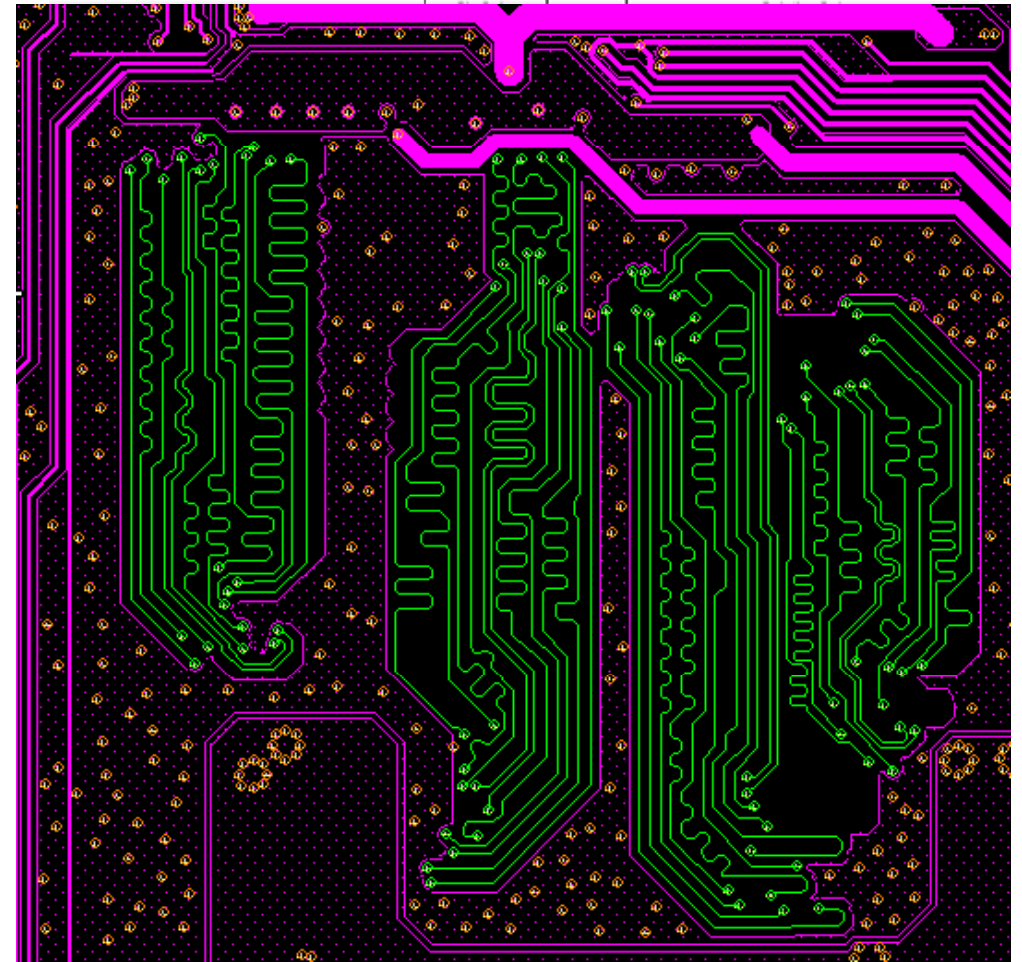


Case 2 - Tablet PC

AIDT



manual editing after AiDT



Auto-Interactive Delay Tune (AiDT)



Case	(AiDT + modify) / manual	Reduce Ratio %
Case 1	(1+4) / 15	67%
Case 2	3.8 / 12	68%

Auto-Interactive Delay Tune (AiDT)

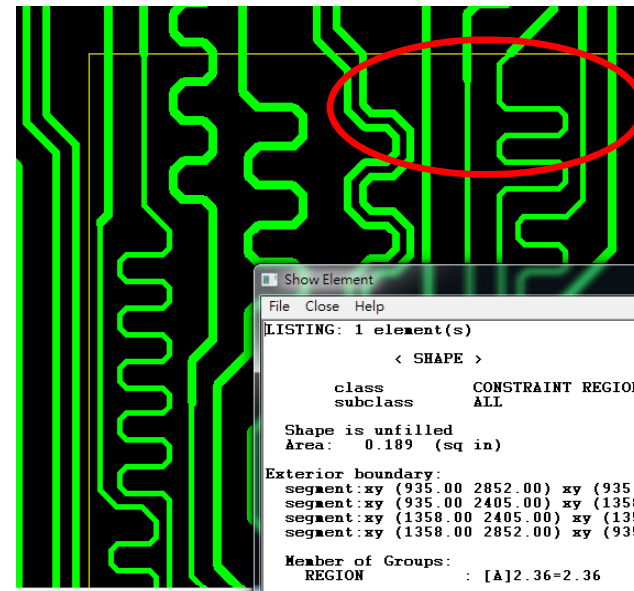
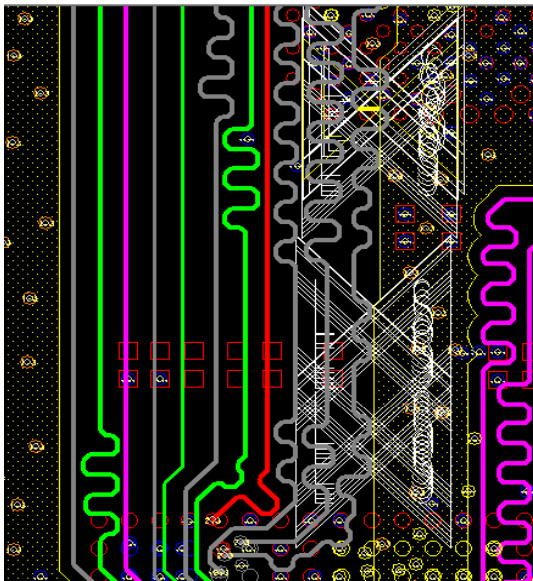
Experience share

- ◉ 選取的走線中Cline segs fixed時,此seg不會繞線.
- ◉ 選取的走線中有Clines fixed時,會造成AiDT立即停止.
- ◉ 已符合長度或已過長之走線勿使用AiDT.
- ◉ 當Group中有設target時,可先完成target後,再對其它走線執行AiDT.
- ◉ 建議by group選取,執行AiDT.

Auto-Interactive Delay Tune (AiDT)

Limitation

- ◎ 只支援45度走線,不支援 Arcs與 Offset Routing.
- ◎ 無法支援相鄰層繞線不重疊.
- ◎ 無法完全利用可繞線的空間.(spacing DRC)
- ◎ 無法支援 Constraint Region 中的 line width rule.



Auto-Interactive Delay Tune (AiDT)

Compare in 16.5 and 16.6 same board(11 constraint in one group) on same pc

- Performances

16.5 : 1m30s

16.6 : 1m

- Complete ratio

16.5

```
x Clines Selected: 11; Timing constraints: 11; Timing violations: 2; Outside ideal range: 2
+ E- No command active
P last pick: 387.00 2895.80
Command W- Save Pending
> Command >
```

16.6

```
x Loaded existing interconnect file 'D:\pro.166\15t_frida.100\interconn.iml'
+ Loaded existing interconnect file 'c:\Cadence\SPB_16.6\share\pcb\signal\cds_interconn.iml'
P Finished loading SigNoise interconnect libraries
Command Clines Selected: 11; Timing constraints: 11; Timing violations: 2; Outside ideal range: 2
> Command >
```

Summary

- ◉ 16.6 better than 16.5

PIN_DELAY

Symbol

U?

15	D1	O1	8
14	D2	O2	10
13	D3	O3	12
23	D4	O4	4
22	D5	O5	2
21	D6	O6	24
16	DE1		
17	DE2		
20	DE3		
19	E		
18	VEE		
6	VCC		
1	VCCA		
3	VCCA		
7	VCCA		
9	VCCA		
11	VCCA		
5	VCCA		

PKG EXCEL

	A	B	C	D	E	F
1	REFDES	U0301				
2	DEVICE	HASWELL_MCP_E_HASWELL_MCP_HASWE				
3	AR36	383.5				
4	AU40	376.22				
5	AV40	379.57				
6	AY39	427.96				
7	AW39	393.53				
8	AY41	451.19				
9	AU41	397.51				
10	AW41	411.44				
11	AU42	372.1				
12	AV42	394.85				
13	AR35	375.15				

OLB with pkg length



Set Package Length

Set Package Length

Select OLB: K:/parts/02_CHIPSET_V.OLB

- LE89116QVC
- LE89810BSC
- LM3S3Z26_IQR50_C1T
- LM3S5R31
- MCP85ML**
- MSD3701PX_LF
- MSD5041L
- MST69981DLD_LF_1
- MX_88SE9128B1_4V
- MX_89HMPEB383ZAEMG

Bound Length File: D:/pegatron/OrCADProject/PKG_Lengths/Test/BondLength_0402. ...

Execute Close

Report

SetPkgLength_report.txt - 記事本

検索(F) 編集(E) 格式(O) 檢視(V) 說明(H)

Part: MCP85ML
 Pin Count: 1168
 Library: K:\parts\02_CHIPSET_V.OLB

Excel File: D:\PKG_Lengths\BondLength_0402.xlsx
 Defined PKG Length Pin: 226

Add the PKG Length Success (76/226)

Pin No.	Length
AD37	370.44 mil
AN28	242.25 mil
AV19	360.18 mil
AR25	329.90 mil
AN29	242.33 mil
AR26	306.54 mil
AV22	365.37 mil
AV23	335.02 mil
AR28	307.69 mil
AK20	241.08 mil
AR29	304.18 mil

PIN_DELAY

Net in flow

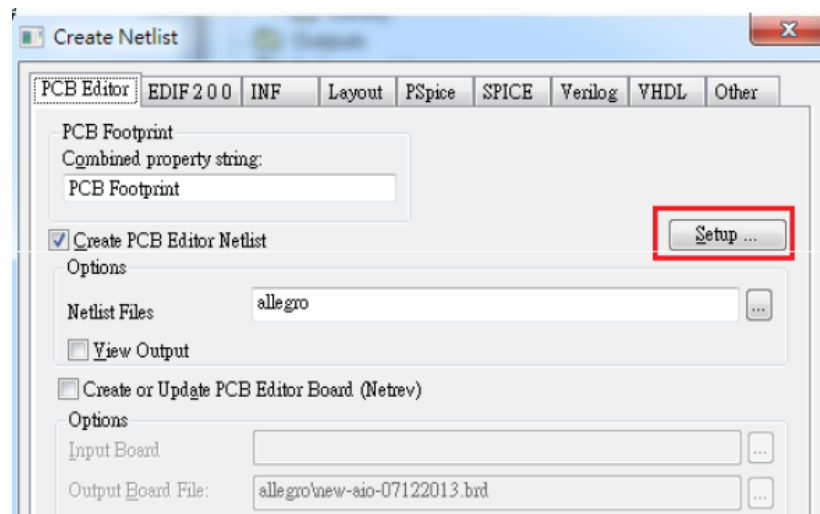
Type	Objects	Referenced Electrical CSet	Pin Pairs	Pin Delay	
				Pin 1	Pin 2
				mil	mil
*	*	*	*	*	*
Dsn	<input type="checkbox"/>				
MGrp	<input type="checkbox"/> R_DDR3A_DIMM3_ADD (22)		All Drivers/All Receivers		
PPr	XU1.AT18:XMM3.56 [M_CHA_MAA7]			476.79 MIL	
PPr	XU1.AT19:XMM3.175 [M_CHA_MAA9]			486.44 MIL	
PPr	XU1.AT20:XMM3.172 [M_CHA_MAA14]			515.24 MIL	
PPr	XU1.AT21:XMM3.52 [M_CHA_BA2]			512.16 MIL	
PPr	XU1.AU9:XMM3.74 [M_CHA_CAS#]			649.99 MIL	
PPr	XU1.AU11:XMM3.73 [M_CHA_WE#]			544.14 MIL	
PPr	XU1.AU12:XMM3.192 [M_CHA_RAS#]			520.90 MIL	
PPr	XU1.AU13:XMM3.188 [M_CHA_MAA0]			576.42 MIL	
PPr	XU1.AU16:XMM3.61 [M_CHA_MAA2]			513.00 MIL	
PPr	XU1.AU17:XMM3.59 [M_CHA_MAA4]			495.79 MIL	
PPr	XU1.AU18:XMM3.177 [M_CHA_MAA8]			547.08 MIL	
PPr	XU1.AU19:XMM3.174 [M_CHA_MAA12]			528.07 MIL	
PPr	XU1.AU21:XMM3.171 [M_CHA_MAA15]			552.69 MIL	
PPr	XU1.AV12:XMM3.71 [M_CHA_BA0]			554.11 MIL	
PPr	XU1.AV16:XMM3.181 [M_CHA_MAA1]			541.87 MIL	
PPr	XU1.AV17:XMM3.178 [M_CHA_MAA6]			589.77 MIL	
PPr	XU1.AV19:XMM3.55 [M_CHA_MAA11]			577.30 MIL	
PPr	XU1.AW11:XMM3.70 [M_CHA_MAA10]			635.55 MIL	
PPr	XU1.AW17:XMM3.180 [M_CHA_MAA3]			604.08 MIL	
PPr	XU1.AW18:XMM3.58 [M_CHA_MAA5]			613.64 MIL	
PPr	XU1.AY10:XMM3.196 [M_CHA_MAA13]			741.83 MIL	

PIN_DELAY

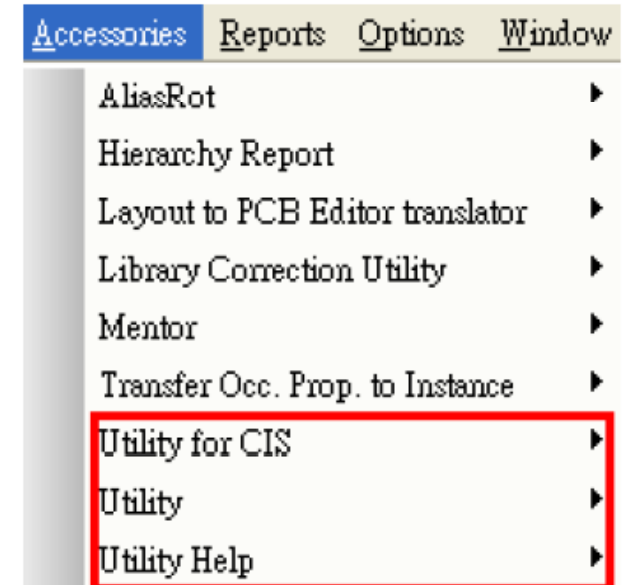
Limitation

- 需手動將變數填入allegro.cfg

Add PIN_DELAY=YES in allegro.cfg



```
[pinprops]  
NO_DRC=YES  
NO_PIN_ESCAPE=YES  
NO_SHAPE_CONNECT=YES  
NO_SWAP_PIN=YES  
PIN_ESCAPE=YES  
PIN_DELAY=YES
```



- V16.5客製化的menu僅能掛在 Accessories 功能列下.

