

OrCAD SI for Electrical Constraints Determination

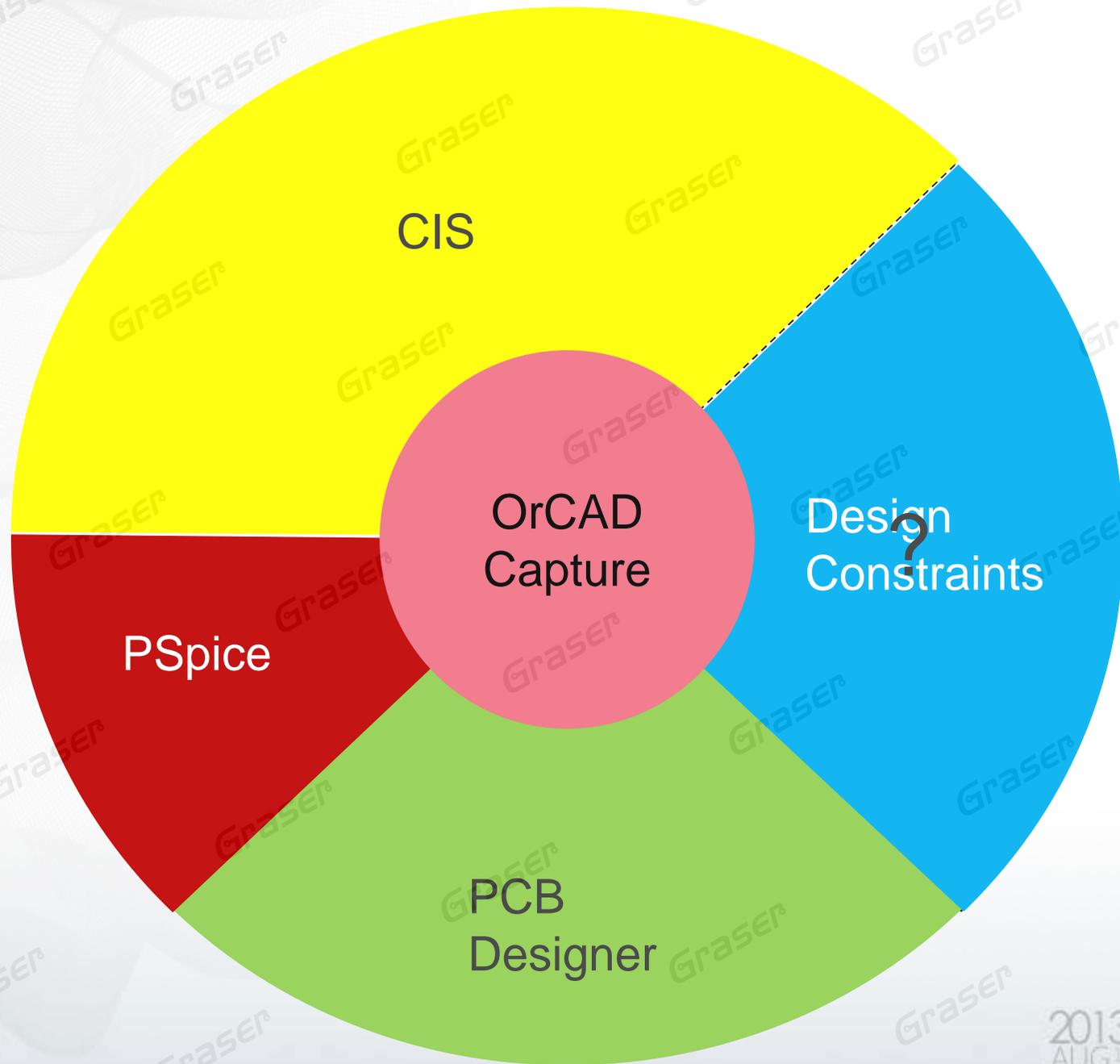
Mark Wu

13/Aug/2013

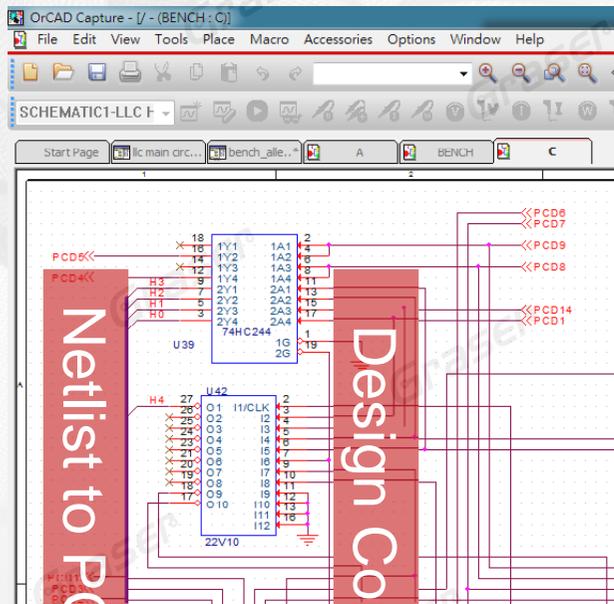
Enhance your design flow to decide design constraints

- When high-speed PCB design constraints are determined, let's begin in schematic drawing.

Design Flow Chart

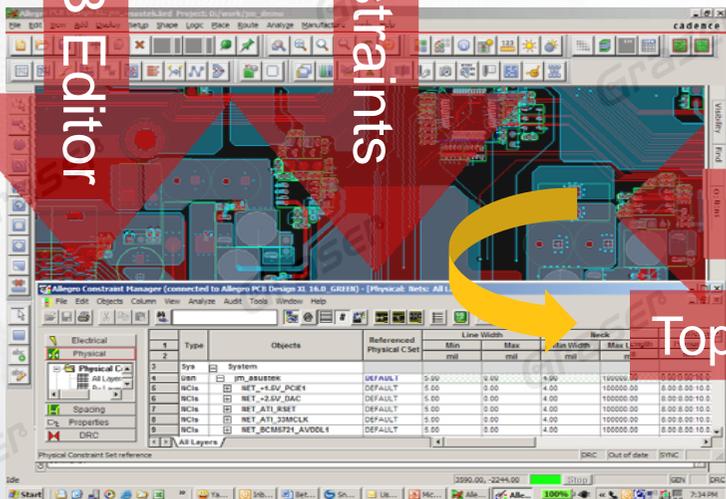


Traditional Signal Integrity Flow



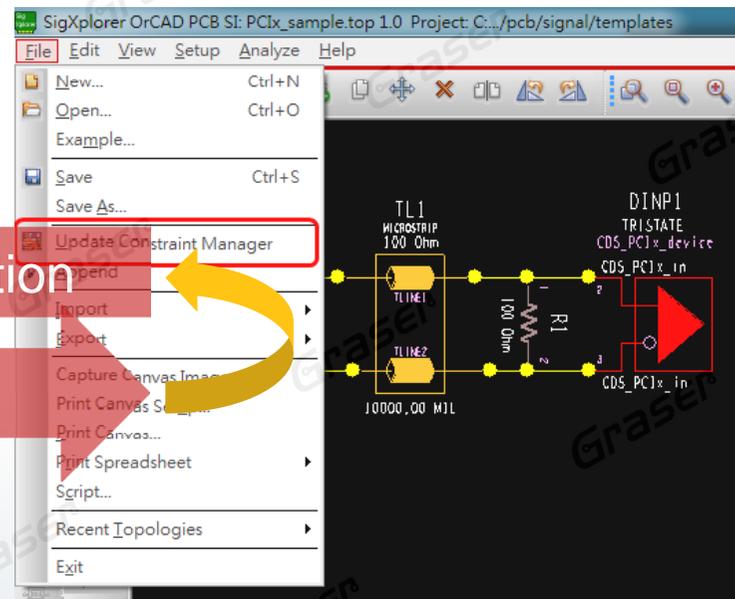
Design Reuse?
 Constraints Update ?

Analyze / Edit Topology



Topology Association

Topology Extraction



SI Model Association

Topic

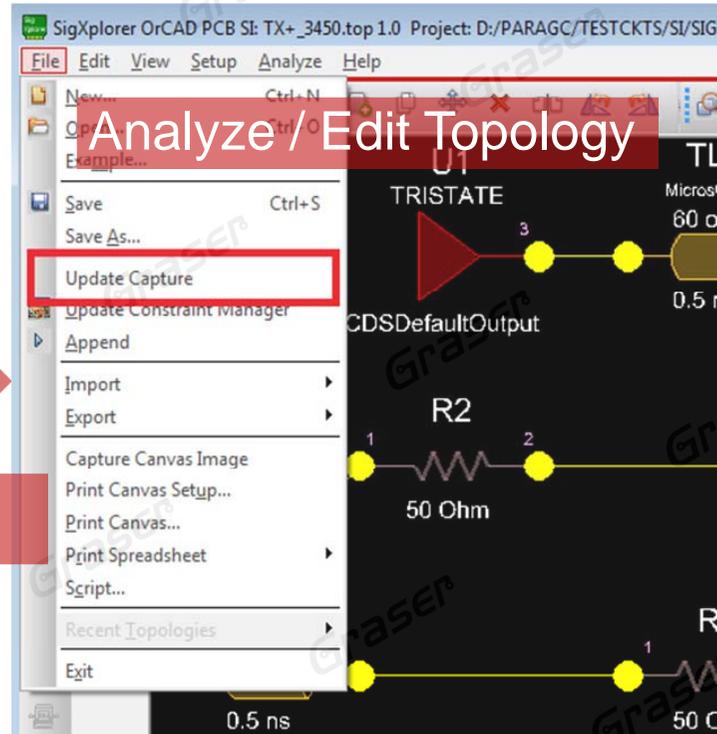
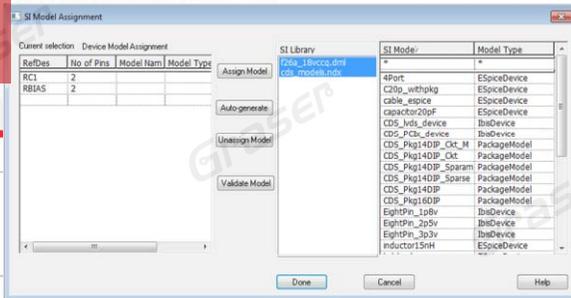
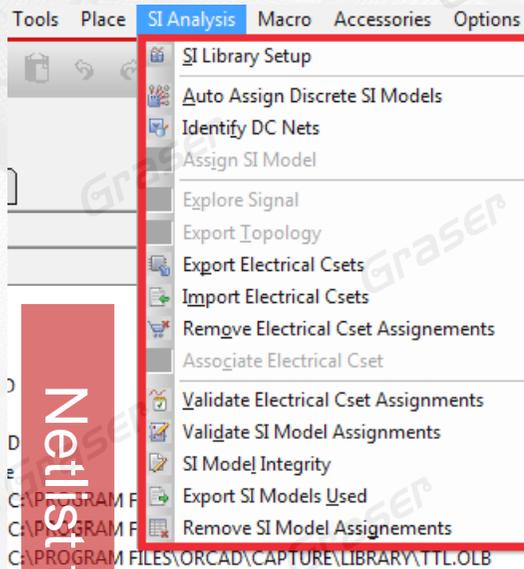
- Change your constraints design flow with OrCAD SI
 - Determine design constraints from Capture to OrCAD SI
 - Back annotate ECsets and store information in Capture
 - Directly translate design constraints from netlist files.

Much Easier and more simplified for PCB Layout Guide writing and reading

Enhance the smoothness for PCB design flow

OrCAD Schematic w/ Signal Integrity Flow

SI Model Association

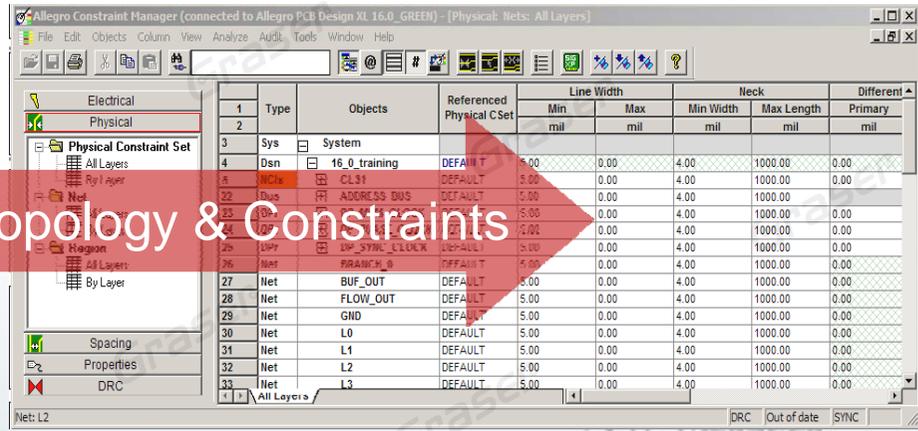
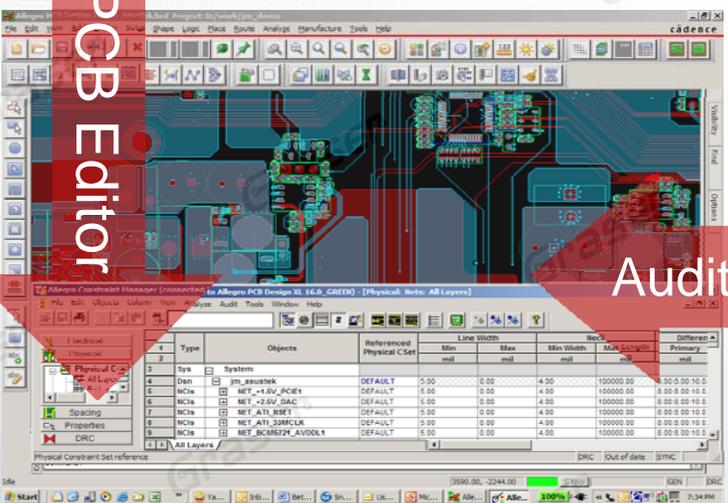


Topology Extraction

Topology Association

Netlist to PCB Editor

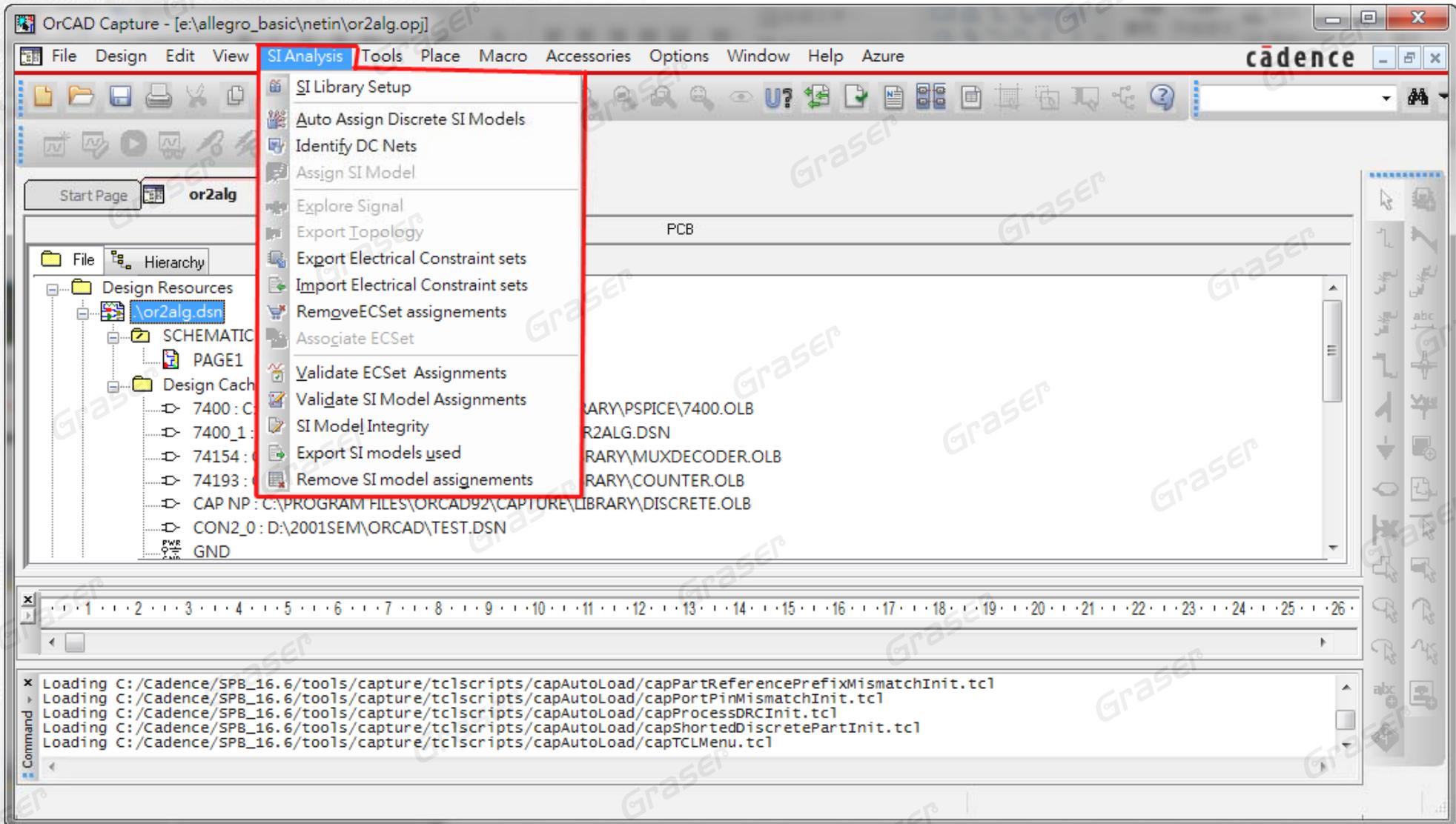
Audit / Refine Topology & Constraints



Determine Hi-Speed Constraints in OrCAD SI

- 1. Impedance control
- 2. Timing control

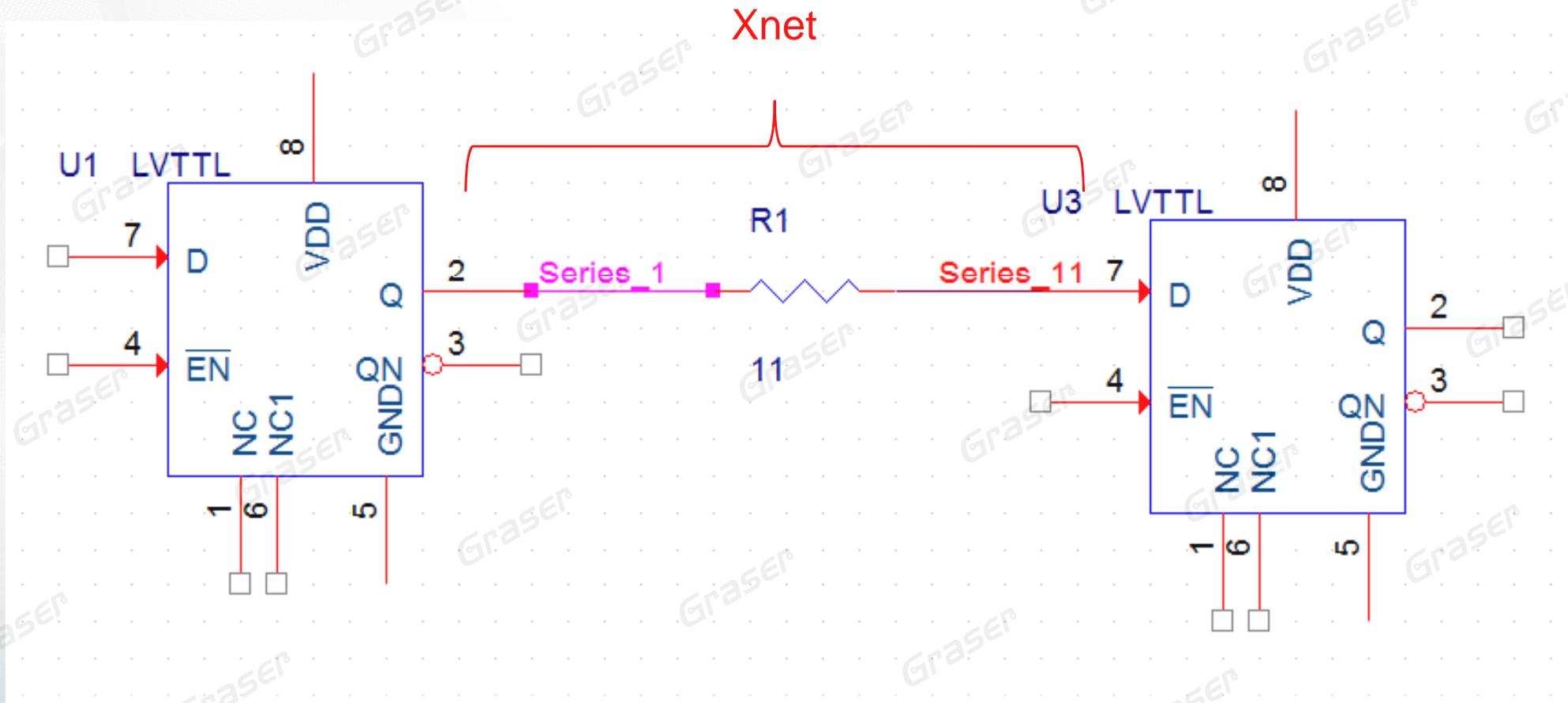
SI Analysis in Capture



Support from V16.6

Assign SI Model

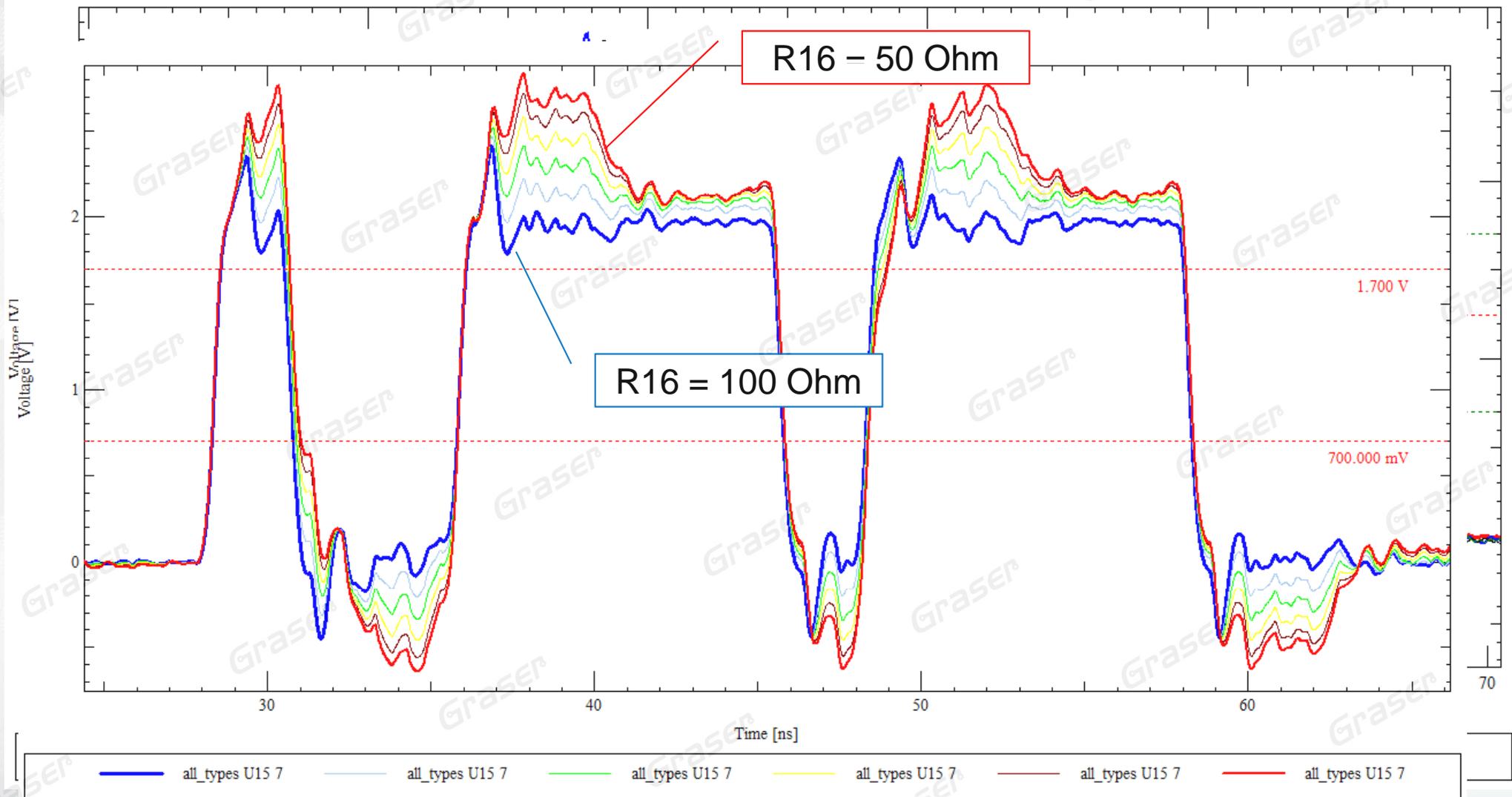
- Auto assign discrete SI model by component value
- Assign SI model for others



OrCAD Signal Integrity for Pre -Simulation

From OrCAD Capture to OrCAD SI

Impedence Control - Terminator



From Idea to Virtual Practicality

From OrCAD Capture to OrCAD SI

Virtual Layer Stackup

SigXplorer OrCAD PCB SI: unnamed.top 1.0 Project: C:/SPB_Data

File Edit View **Setup** Analyze Help

- Constraints...
- Defaults...
- Strobe Pins...
- Vectors...
- Optional Pins
- Manage LayerStacks...**

LayerStack Manager

LayerStacks

- 8 Layers
- 4 Layers
- 2 Layers

Edit...

New...

Rename

2 Layers

4 Layers

6 Layers

8 Layers

Layout Cross Section

	Subclass Name	Type	Thickness (MIL)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)	Coupling Type	Spacing (MIL)	DiffZ0 (ohm)
1		SURFACE		1	0							
2		DIELECTRIC	0.6	3.8	0							
3	TOP	CONDUCTOR	1.8	4	0	<input type="checkbox"/>	5.00	53.581	EDGE	5.00	84.612	
4		DIELECTRIC	4	4	0.035							
5	PLANE_2	PLANE	1.3	4	0.035	<input type="checkbox"/>						
6		DIELECTRIC	4	4	0.035							
7	SIGNAL_3	CONDUCTOR	1.3	4	0.035	<input type="checkbox"/>	5.00	50.284	EDGE	5.00	80.457	
8		DIELECTRIC	6.5	4	0.035							
9		DIELECTRIC	22.9	4	0.035							
10		DIELECTRIC	6.5	4	0.035							
11	SIGNAL_4	CONDUCTOR	1.3	4	0.035	<input type="checkbox"/>	5.00	50.284	EDGE	5.00	80.457	
12		DIELECTRIC	4	4	0.035							
13	PLANE_5	PLANE	1.3	4	0.035	<input type="checkbox"/>						
14		DIELECTRIC	4	4	0.035							
15	BOTTOM	CONDUCTOR	1.8	4	0	<input type="checkbox"/>	5.00	53.581	EDGE	5.00	84.612	
16		DIELECTRIC	0.6	3.8	0							
17		SURFACE		1	0							

Total Thickness: 61.9 MIL

Layer Type: ALL

Material: ALL

Field to Set: Thickness

Value to Set: []

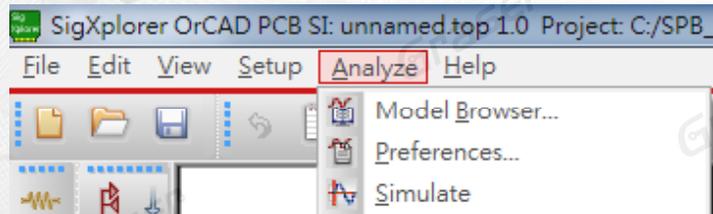
Update Fields

Show Single Impedance

Show Diff Impedance

OK Apply Cancel Refresh Materials -> Report Help

Virtual Via Padstack



Via Model Generator

Description Modeling Options (Add Model)

Via Selection
Via Type: Single Via
Separation (S): 35mil
of GND Vias: 1

Signal Via

Layer Span Information
Stackup: F:/PCBSI/PCBSI_162/Lab_1/denman.brd
Via: Signal Via
Copy From:
Begin Layer: TOP
End Layer: INT2
Drill Diameter: 12mil
AntiPad Diameter: 34mil
Pad Diameter: 24mil

Layer Type Filter: Conductors Expanded View:

No.	Layer Name	Pad	Conn.	Node	Trace Width (mil)	Trace Angle	Pad Diameter (mil)
1	TOP	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	5.00	0	24.00
2	INT1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
3	INT2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	5.00	0	24.00
4	INT3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			

Via Model Name: Single_Via_1

Close Generate Help

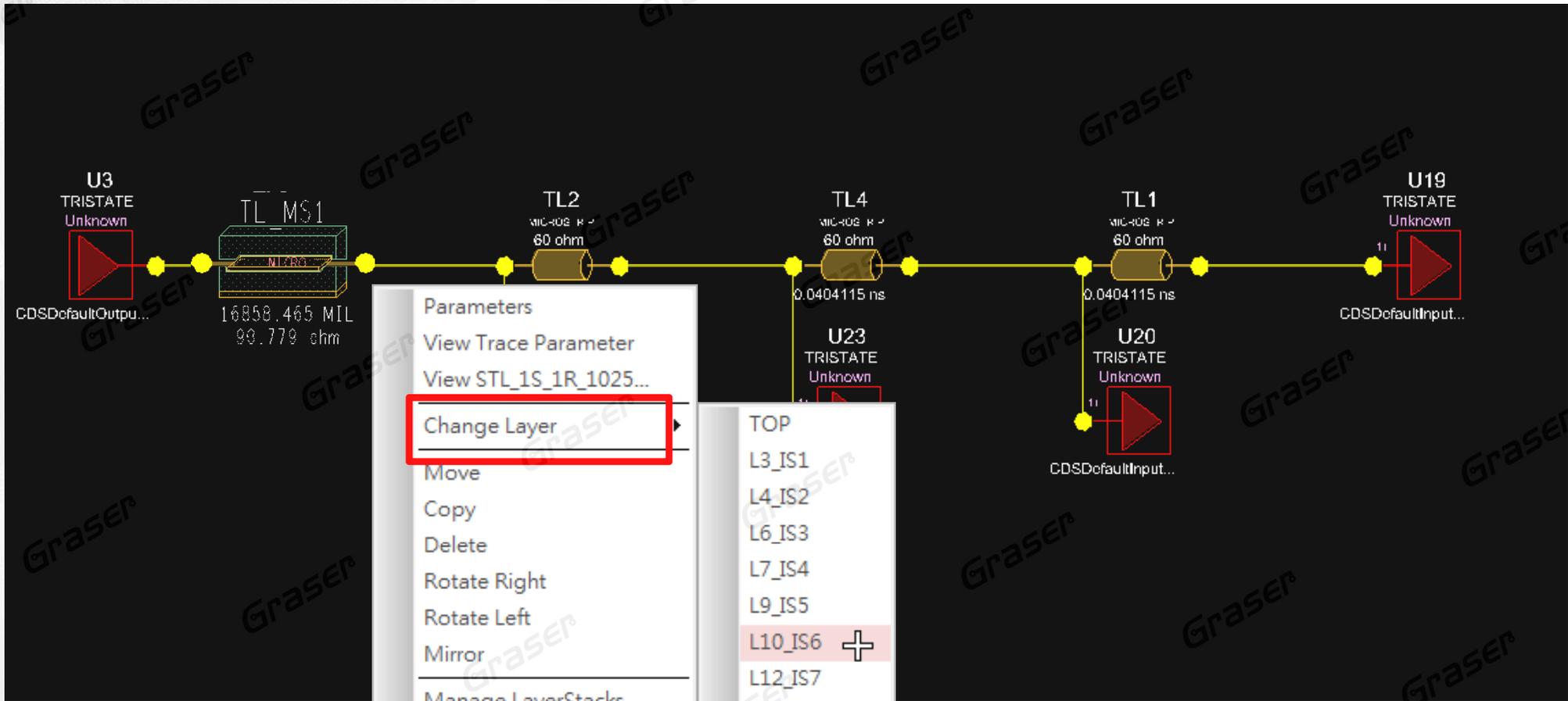
LayerSpan Expanded View

Layer Type Filter: *

No.	Layer Name	Pad	Conn.	Node	Trace Width (mil)	Trace Angle	Pad Diameter (mil)
1	SURFACE_1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
2	DIELECTRIC_1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
3	TOP	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	5.00	0	24.00
4	DIELECTRIC_2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
5	PWR1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
6	DIELECTRIC_3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
7	GND1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
8	DIELECTRIC_4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
9	INT1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
10	DIELECTRIC_5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
11	INT2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	5.00	0	24.00
12	DIELECTRIC_6	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
13	GND2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
14	DIELECTRIC_7	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
15	INT3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
16	DIELECTRIC_8	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
17	INT4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
18	DIELECTRIC_9	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
19	PWR2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
20	DIELECTRIC_10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
21	GND3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			
22	DIELECTRIC_11	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>			

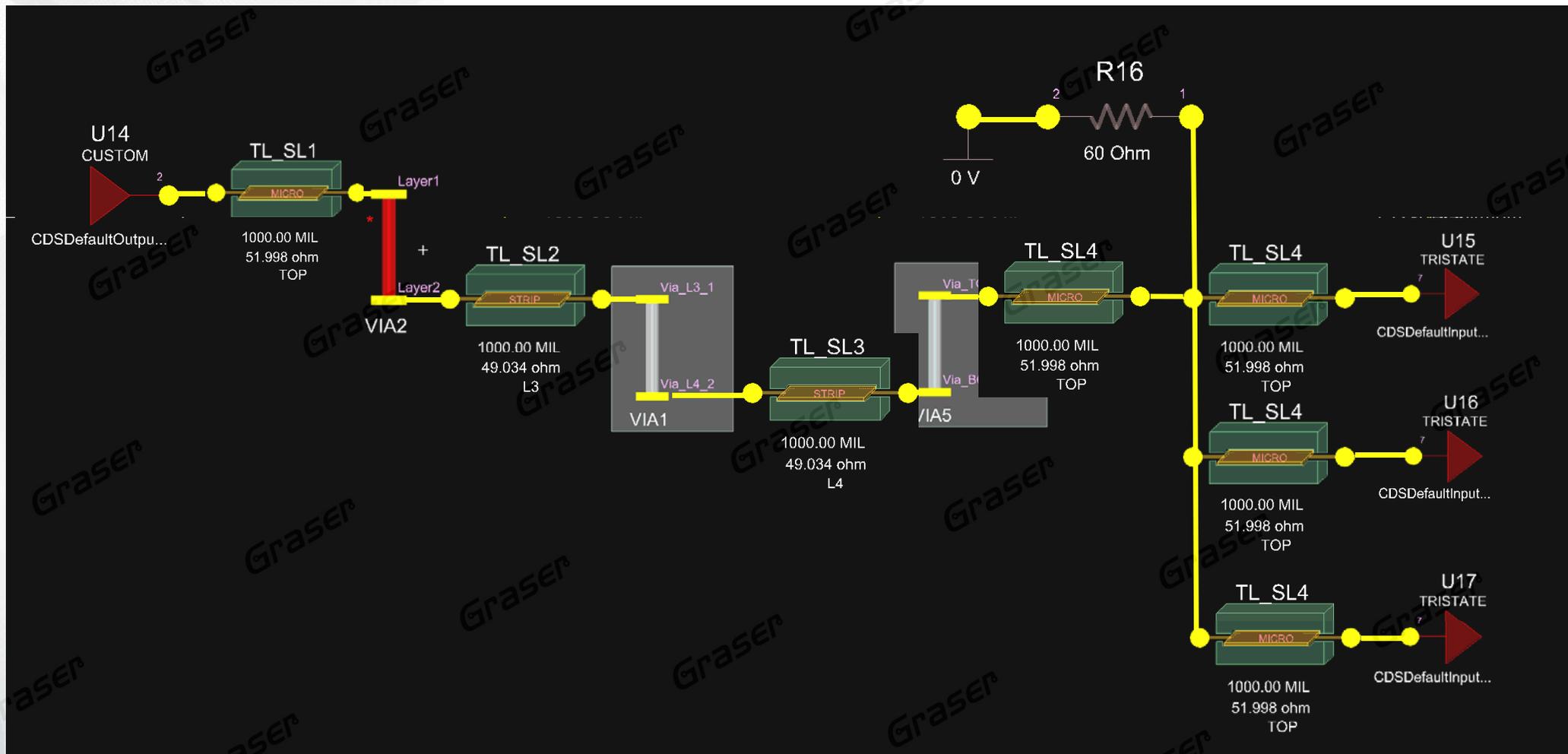
Close

Edit & Assume Transmission Line

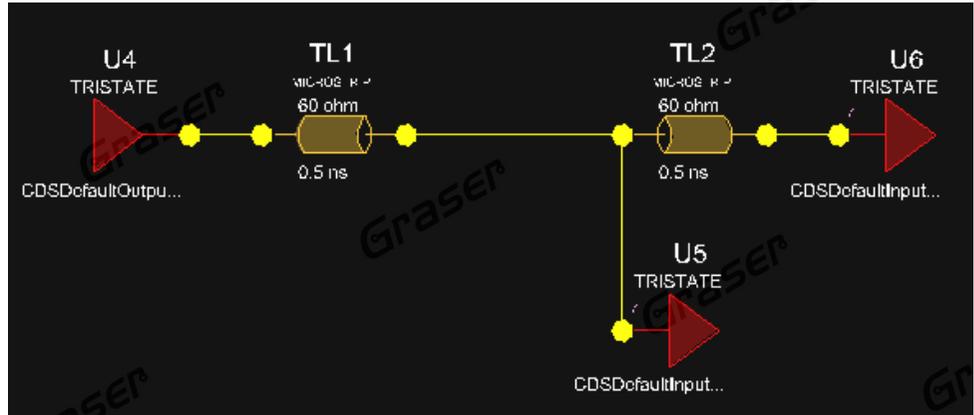
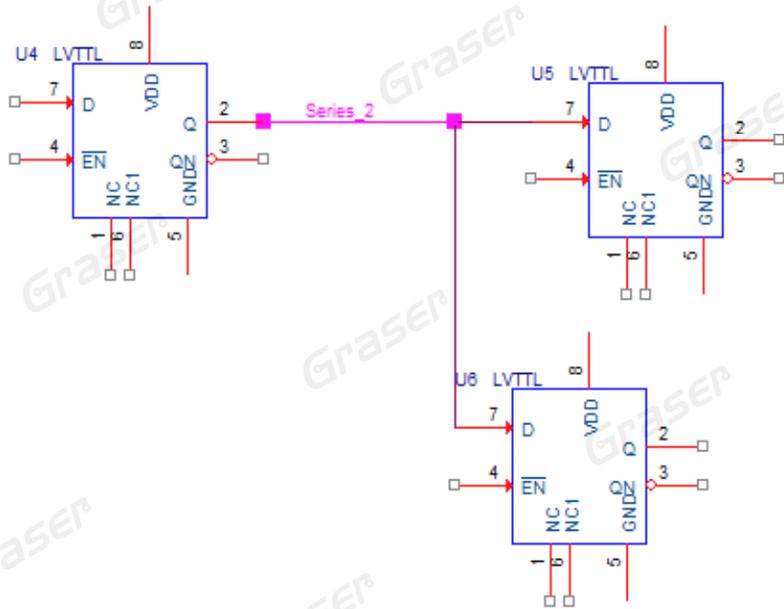


Edit & Assume Layer Stackup for Transmission Line Via Model

Re-Organize Topology



Define Constraints in OrCAD SigXplorer



Set Topology Constraints

Max Parallel	Wiring	User-Defined	Signal Integrity	Usage
Switch-Settle	Prop Delay	Impedance	Rel Prop Delay	Diff Pair
Existing Rules				
From	To	Rule-Type	Min-Delay	Max-Delay
T.1	U5.7	LENGTH	1000.00 mil	1050.00 mil
T.1	U6.7	LENGTH	1000.00 mil	1050.00 mil
U4.2	T.1	LENGTH	2000.00 mil	2050.00 mil

Pins/Tees

Name	Usage
ALL DRVRS/RCVRS	
DRIVER/RECEIVER	
LONGEST/SHORTEST	
T.1	TEE
U4.2	OUT
U5.7	IN
U6.7	IN

Rule Editing

From:

To:

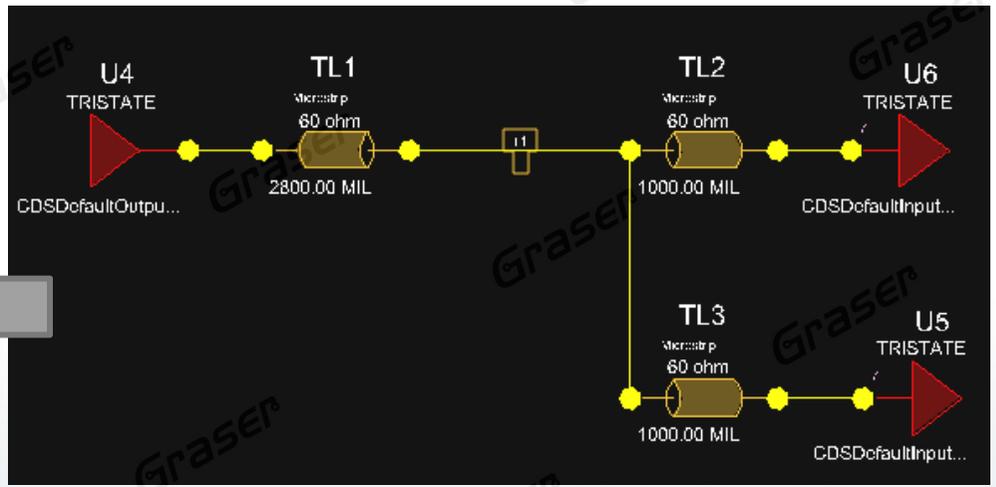
Rule Type: Length

Min Delay:

Max Delay:

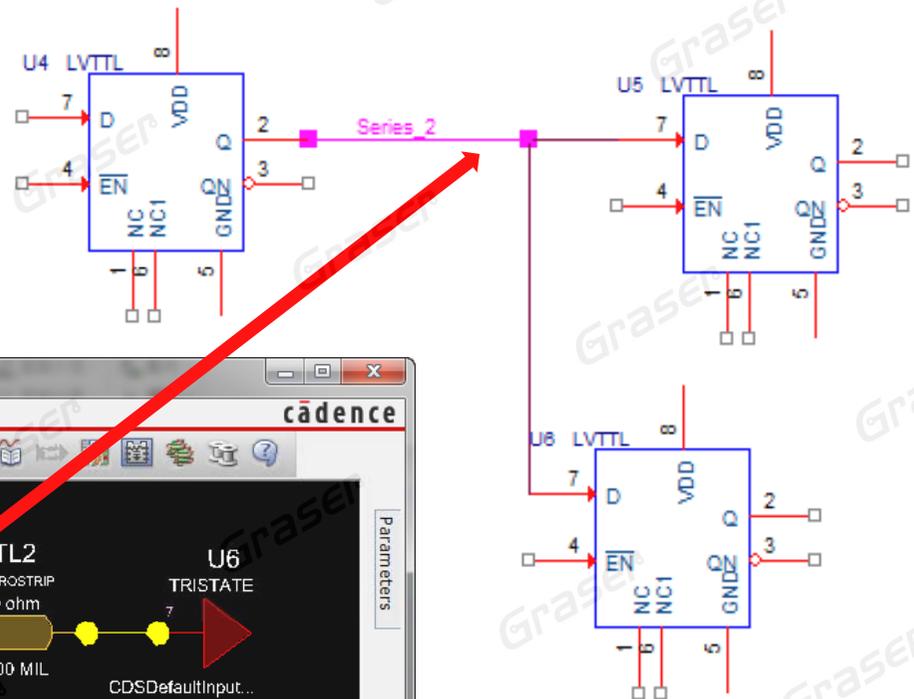
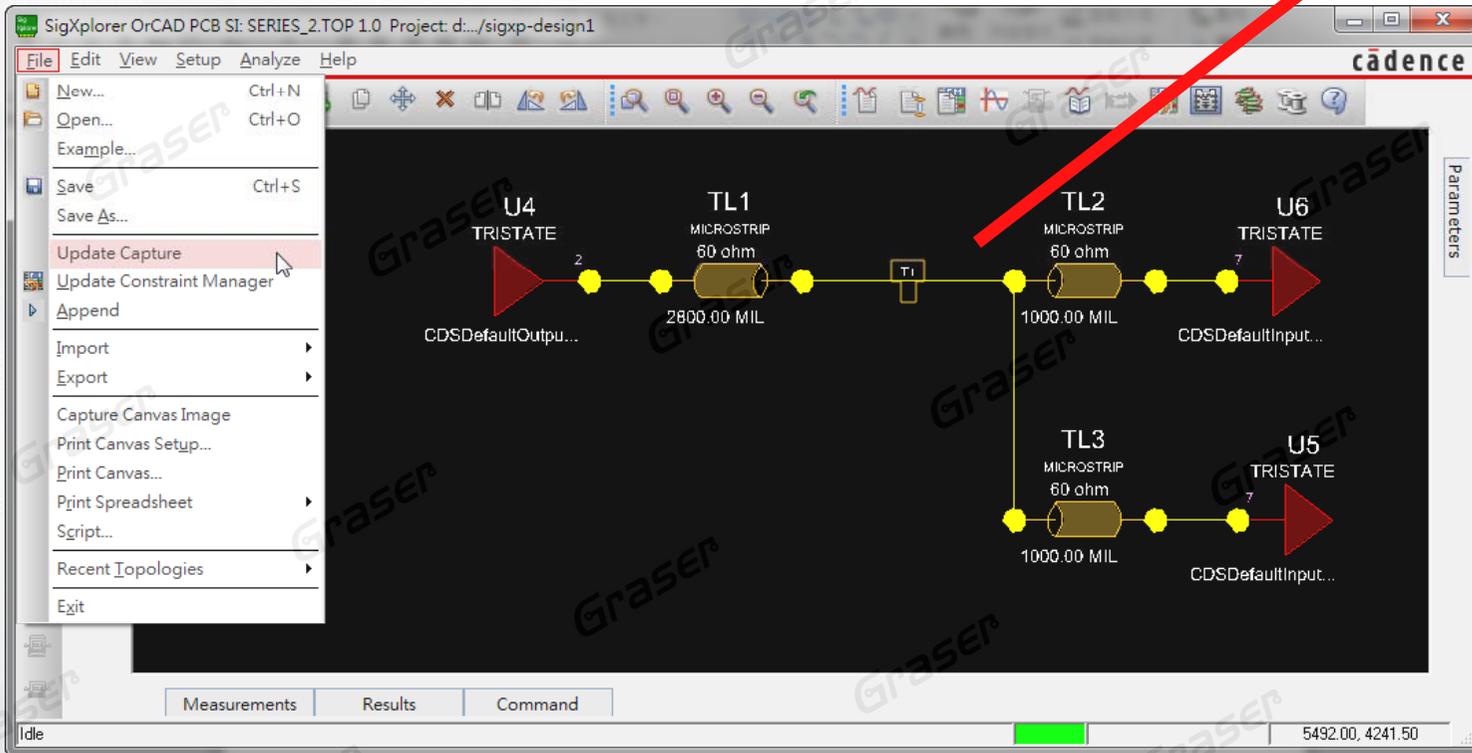
Buttons: Add, Modify, Delete

Buttons: OK, Apply, Cancel, Help

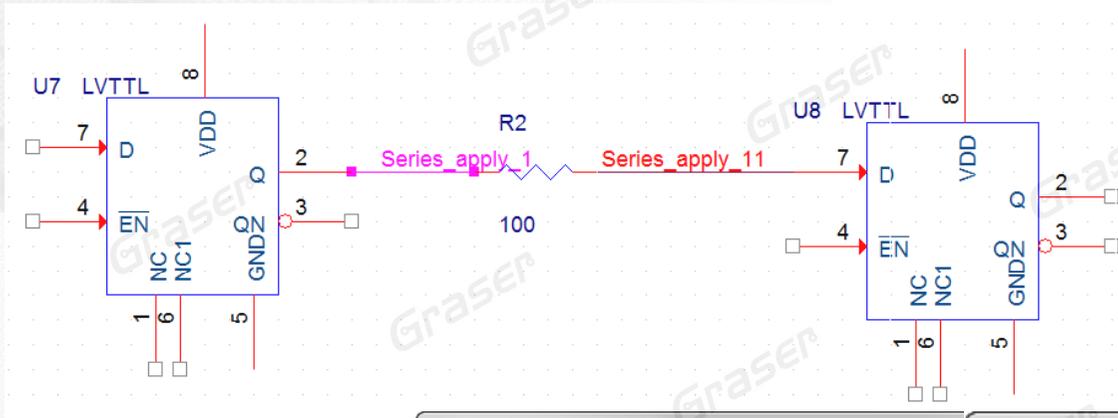


Update to Capture

- Reusable Schematic & Constraints



Replicate ECSet in Schematic



- Mirror Horizontally
- Mirror Vertically
- Mirror Both
- Rotate
- Edit Properties...
- Select Entire Net
- Edit Wire Properties
- Edit Net Properties
- Connect to Bus
- Signal Integrity**
- Assign Power Pins
- Ascend Hierarchy
- Selection Filter
- Fisheye view

Select an ECSet to associate

搜尋位置(I): sigxp-design1

名稱

- dml_model
- signoise.run
- sigxp.run
- SERIES_2.TOP
- SERIES_11.TOP**

檔案名稱(N): SERIES_11.TOP

檔案類型(T): Topology File (*.TOP)

以唯讀方式開啟(R)

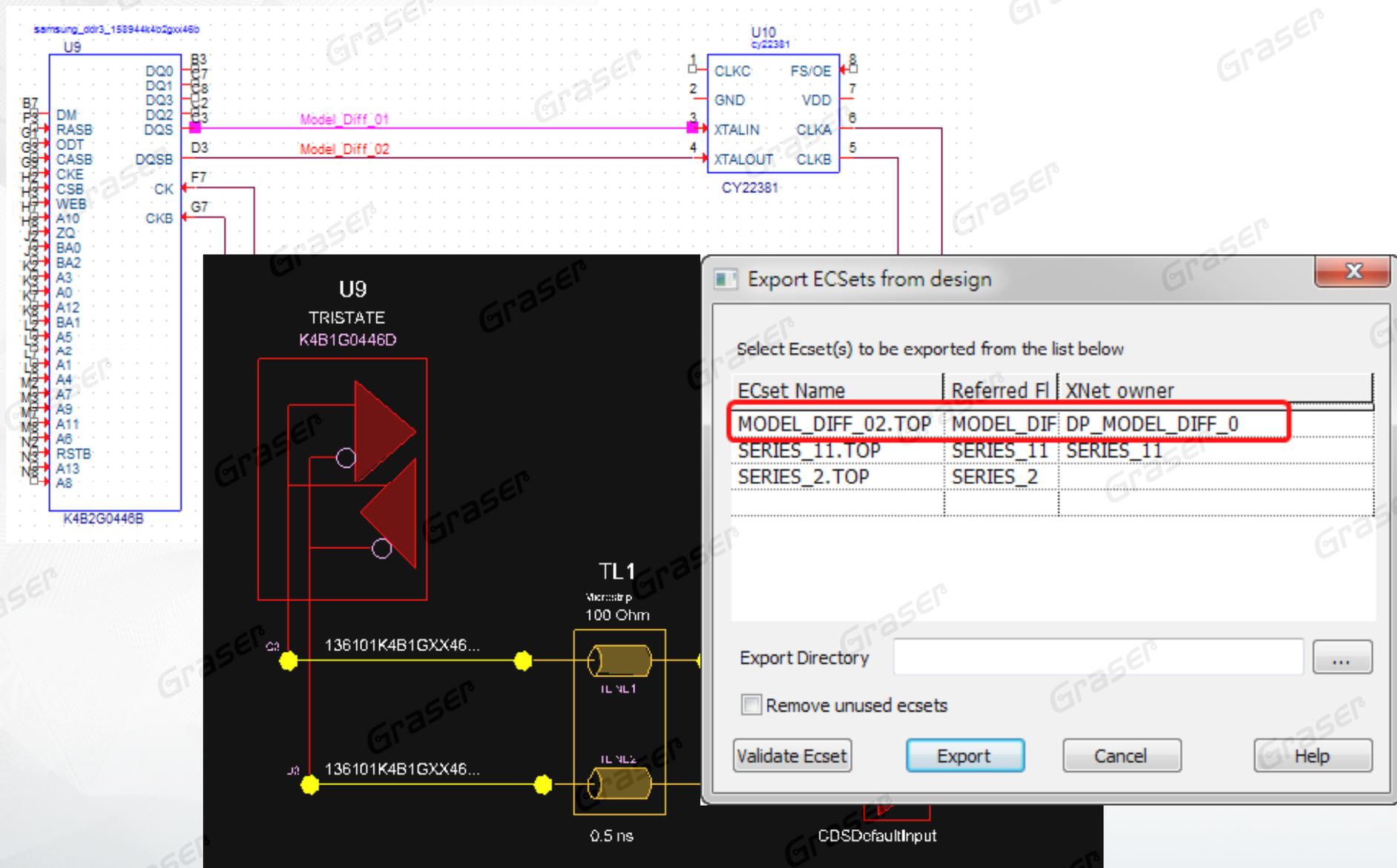
- Explore Signal
- Export Topology
- Associate ECSet**
- Validate ECSet Assignments
- Remove ECSet assignments

Browse Spreadsheet

	Line Style	Line Width	Name	Color	ELECTRICAL_CONSTRAINT_SET
1	Default	Default	SERIES_1	Default	
2	Default	Default	SERIES_2	Default	SERIES_2
3	Default	Default	SERIES_11	Default	SERIES_11
4	Default	Default	SERIES_APPLY_1	Default	
5	Default	Default	SERIES_APPLY_11	Default	SERIES_11

OK Cancel New... Copy Remove Paste Help

Apply Differential Pair ECSet



Update To Capture and Netin to Allegro/OrCAD PCB

Worksheet selector

Electrical

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Delay
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay

Net

- Signal Integrity
- Timing
- Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Delay
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay

DEMO_CD2

Objects		Pin Pairs	Min Delay	Max Delay
Type	S		ns	ns
*	*	*	*	*
Dsn		DEMO_CD2		
ECS		SERIES_2		

XNet		ADDRESS_10				
XNet		ADDRESS_11				
XNet		ADDRESS_12				
XNet		ADDRESS_13				
XNet		DATA_0				
XNet		DATA_1				
XNet		DATA_2				
Net		MODEL_DIFF_01				
Net		MODEL_DIFF_02				
XNet		SERIES_APPLY_11				
XNet		SERIES_BE_APPLY_11				
Net		SERIES_2	SERIES_2			
XNet		SERIES_11				

Import ECSet From Constraint Manager

Allegro Constraint Manager (connected to Allegro PCB SI XL 16.6) [DEMO_CD2] - [Electrical Constraint Sets: Routing [DEMO_C

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Delay:

DEMO_CD2

Objects		Pin Pairs	Min Delay	Max Delay
Type	Name		ns	ns
*	*	*	*	*
Dsn	DEMO_CD2			
ECS	SERIES_2			
ECSP	NET.T.1:U5.7		1000 mil	1050 mil
ECSP	NET.T.1:U6.7		1000 mil	1050 mil
ECSP	U4.2:NET.T.1		2800 mil	2850 mil

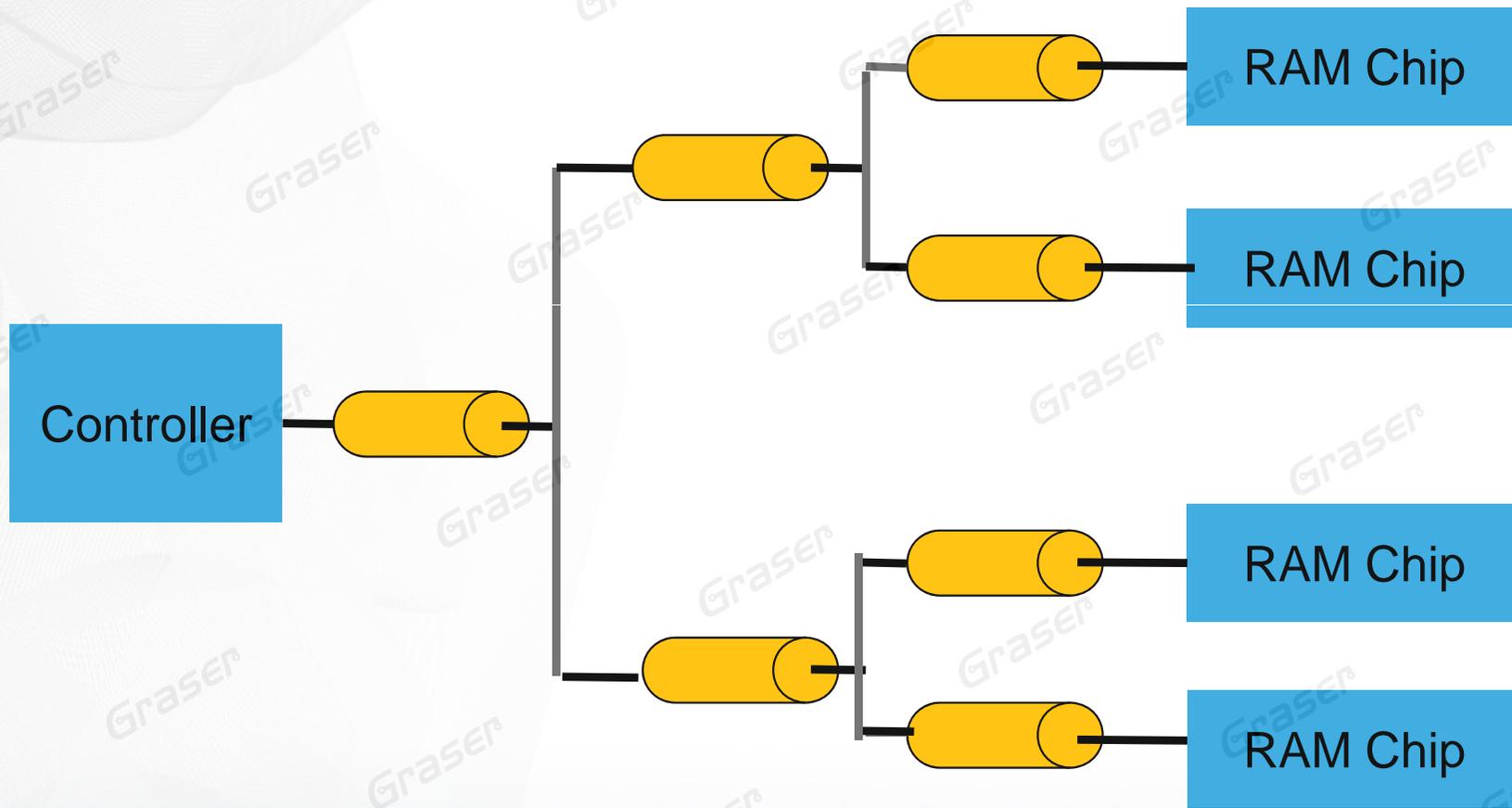
Net

- Signal Integrity
- Timing
- Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Delay:
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay

Physical

XNet	ADDRESS_10									
XNet	ADDRESS_11									
XNet	ADDRESS_12									
XNet	ADDRESS_13									
XNet	DATA_0									
XNet	DATA_1									
XNet	DATA_2									
Net	MODEL_DIFF_01									
Net	MODEL_DIFF_02									
XNet	SERIES_APPLY_11									
XNet	SERIES_BE_APPLY_11									
Net	SERIES_2	SERIES_2							50 MIL	
PPr	SERIES_2.T.1:U5.7				1000.0...		1050.0...	100.0...	950 MIL	
PPr	SERIES_2.T.1:U6.7				1000.0...		1050.0...	1000.0...	50 MIL	
PPr	U4.2:SERIES_2.T.1				2800.0...		2850.0...	1100.0...	1750 ...	

DDRx Routing Topology

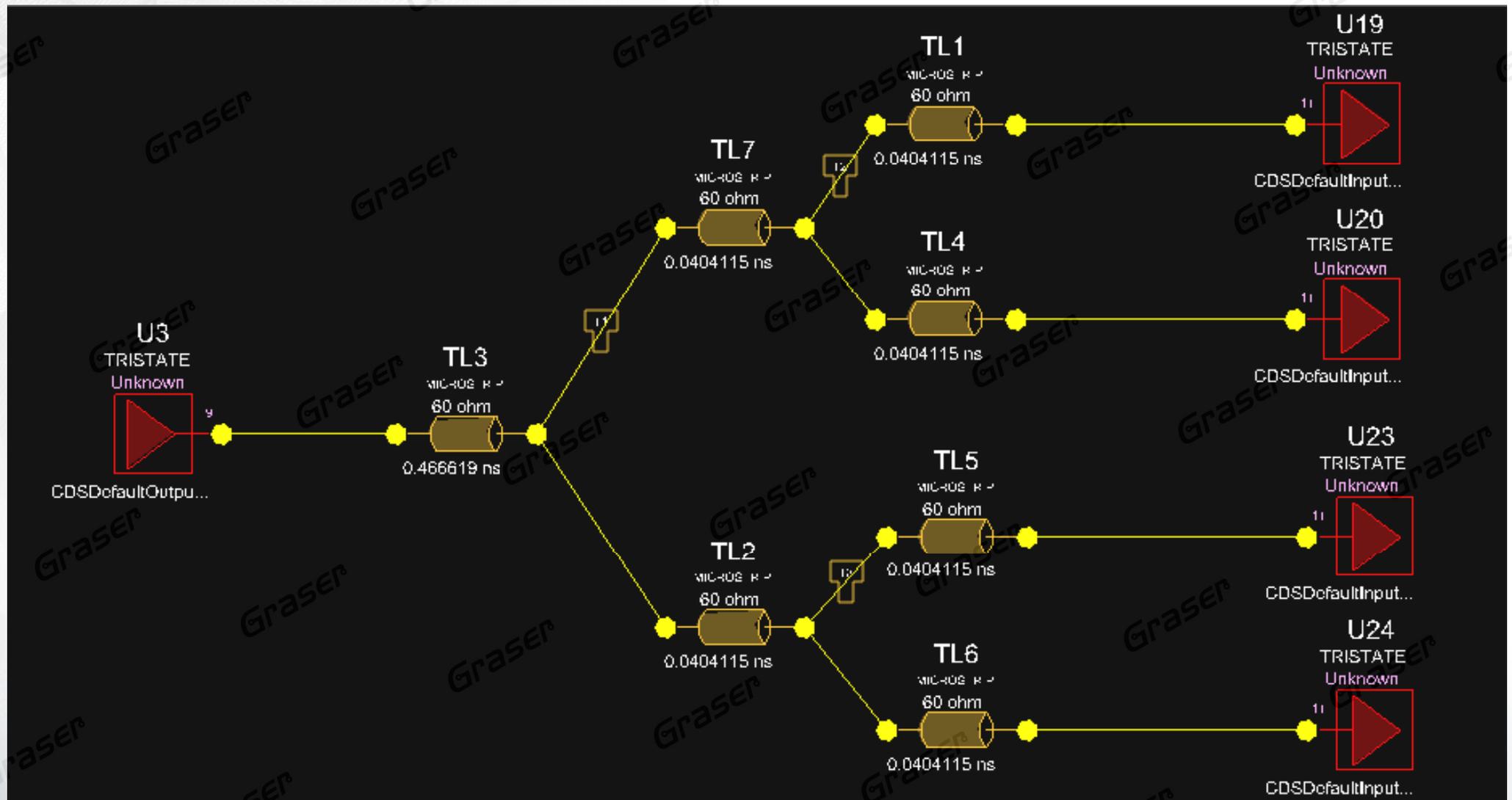


Determine Relative Propagation Delay Constraints

- Build BUS Group
- Create pin-pair by each net
- Match Group by pin-pair
- Assign constraints by each pin-pair
- Determine who is the target for each group

Is it possible to be much faster and easier ?

Determine Relative Propagation Delay Constraints from OrCAD SI



Define Relative Propagation Delay Constraints

The screenshot shows the 'Set Topology Constraints' dialog box in SigXplorer OrCAD PCB SI. The 'Rel Prop Delay' tab is selected. The 'Existing Rules' table is as follows:

Name	From	To	Scope	Delta	Tolerance
A1	U3.9	T.1	GLOBAL	150.00 mil	10 %
B1	T.1	T.2	GLOBAL	100.00 mil	10 %
B2	T.1	T.3	GLOBAL	100.00 mil	10 %
C1	T.2	U19.11	GLOBAL	150.00 mil	5 %
C2	T.2	U20.11	GLOBAL	150.00 mil	5 %
C3	T.3	U23.11	GLOBAL	150.00 mil	5 %

The 'Rule Editing' section for rule A1 shows the following settings:

- Rule Name: A1
- From: U3.9
- To: T.1
- Scope: Global
- Delta Type: Length
- Delta: 150.00 mil
- Tol Type: Percent
- Tolerance: 10 %

The 'Pins/Tees' section shows the following usage:

Name	Usage
ALL DRVRS/RCVRS	
DRIVER/RECEIVER	
LONGEST	
T.1	TEE
T.2	TEE
T.3	TEE
U3.9	OUT
U19.11	IN
U20.11	IN
U23.11	IN
U24.11	IN

- Save topology file for ECSet

Apply ECSets in Constraint Manager

Allegro Constraint Manager (connected to Allegro PCB Designer (was Performance L) 16.6) [demo_place-0] - [Electrical: Nets: Routing [demo_place-0]]

File Edit Objects Column View Analyze Audit Tools Window Help

cadence - x

Worksheet selector: demo_place-0

Electrical

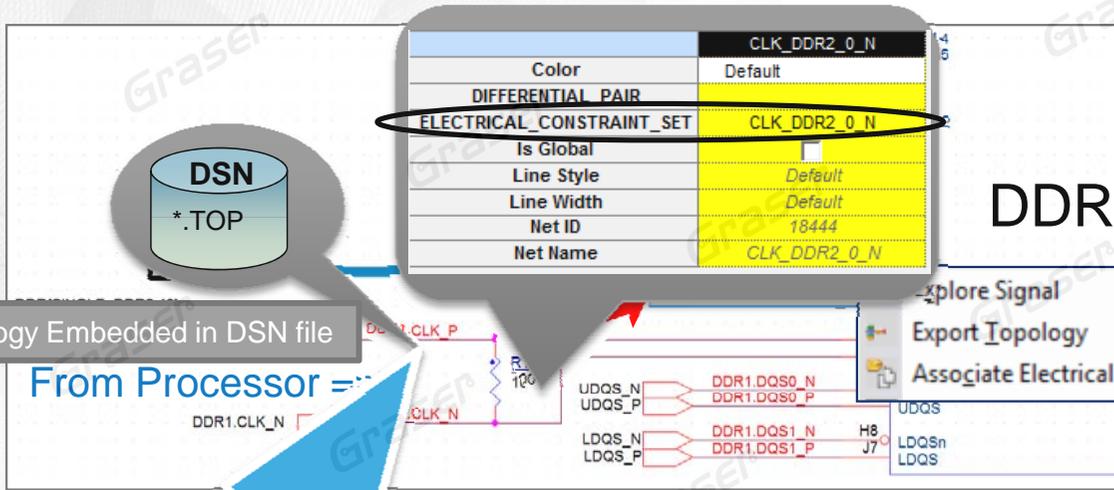
- Electrical Constraint Set
 - Signal Integrity
 - Timing
 - Routing
- Net
 - Signal Integrity
 - Timing
 - Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Delay
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay

Type	S	Name	Referenced Electrical C Set	Pin Pairs	Pin Delay		Scope	Relative Delay				Length mil	Delay ns
					Pin 1 mil	Pin 2 mil		Delta: Tolerance mil	Actual	Margin	+/-		
Dsn		demo_place-0											
MGrp		A1 (8)											
PPr		U1.7:ADDR5.T.1 [ADDR5]					Global	150 MIL:10 %	36.80164...	26.8016 %	-	1233	0.2215
PPr		U1.9:ADDR4.T.1 [ADDR4]					Global	150 MIL:10 %	25.16658...	15.1666 %	-	1460	0.2622
PPr		U2.7:ADDR3.T.1 [ADDR3]					Global	150 MIL:10 %	13.37775...	3.37776 %	-	1690	0.3035
PPr		U2.9:ADDR2.T.1 [ADDR2]					Global	150 MIL:10 %	TARGET			1801	0.3235
PPr		U3.7:ADDR1.T.1 [ADDR1]					Global	150 MIL:10 %	19.93849...	9.93849 %	-	1562	0.2806
PPr		U3.9:ADDR0.T.1 [ADDR0]					Global	150 MIL:10 %	14.24910...	4.2491 %	-	1673	0.3005
PPr		U101.7:ADDR7.T.1 [ADDR7]					Global	150 MIL:10 %	49.20553...	39.2055 %	-	991	0.1780
PPr		U101.9:ADDR6.T.1 [ADDR6]					Global	150 MIL:10 %	37.62173...	27.6217 %	-	1217	0.2186
MGrp		B1 (8)											
PPr		ADDR0.T.1:ADDR0.T.2 [ADDR0]					Global	100 MIL:10 %	14.18685...	4.18685 %	-	992	0.1782
PPr		ADDR1.T.1:ADDR1.T.2 [ADDR1]					Global	100 MIL:10 %	19.11764...	9.11765 %	-	935	0.1679
PPr		ADDR2.T.1:ADDR2.T.2 [ADDR2]					Global	100 MIL:10 %	TARGET			1056	0.1897
PPr		ADDR3.T.1:ADDR3.T.2 [ADDR3]					Global	100 MIL:10 %	13.49481...	3.49481 %	-	1000	0.1796
PPr		ADDR4.T.1:ADDR4.T.2 [ADDR4]					Global	100 MIL:10 %	23.52941...	13.5294 %	-	884	0.1588
PPr		ADDR5.T.1:ADDR5.T.2 [ADDR5]					Global	100 MIL:10 %	33.30449...	23.3045 %	-	771	0.1385
PPr		ADDR6.T.1:ADDR6.T.2 [ADDR6]					Global	100 MIL:10 %	33.99654...	23.9965 %	-	763	0.1370
PPr		ADDR7.T.1:ADDR7.T.2 [ADDR7]					Global	100 MIL:10 %	43.85813...	33.8581 %	-	649	0.1166
MGrp		B2 (8)											
PPr		ADDR0.T.1:ADDR0.T.3 [ADDR0]					Global	100 MIL:10 %	19.15887...	9.15888 %	-	692	0.1243
PPr		ADDR1.T.1:ADDR1.T.3 [ADDR1]					Global	100 MIL:10 %	25.81775...	15.8178 %	-	635	0.1141
PPr		ADDR2.T.1:ADDR2.T.3 [ADDR2]					Global	100 MIL:10 %	TARGET			756	0.1358
PPr		ADDR3.T.1:ADDR3.T.3 [ADDR3]					Global	100 MIL:10 %	18.22429...	8.2243 %	-	700	0.1257
PPr		ADDR4.T.1:ADDR4.T.3 [ADDR4]					Global	100 MIL:10 %	31.77570...	21.7757 %	-	584	0.1049
PPr		ADDR5.T.1:ADDR5.T.3 [ADDR5]					Global	100 MIL:10 %	44.97663...	34.9766 %	-	471	0.08459
PPr		ADDR6.T.1:ADDR6.T.3 [ADDR6]					Global	100 MIL:10 %	45.91121...	35.9112 %	-	463	0.08316
PPr		ADDR7.T.1:ADDR7.T.3 [ADDR7]					Global	100 MIL:10 %	59.22897...	49.229 %	-	349	0.06268
MGrp		C1 (8)											
PPr		ADDR0.T.2:U19.11 [ADDR0]					Global	150 MIL:5 %	23.13527...	18.1353 %	-	608	0.1092
PPr		ADDR1.T.2:U19.12 [ADDR1]					Global	150 MIL:5 %	26.67509...	21.6751 %	-	580	0.1042
PPr		ADDR2.T.2:U19.13 [ADDR2]					Global	150 MIL:5 %	TARGET			641	0.1151
PPr		ADDR3.T.2:U19.14 [ADDR3]					Global	150 MIL:5 %	22.62958...	17.6296 %	-	612	0.1099
PPr		ADDR4.T.2:U19.16 [ADDR4]					Global	150 MIL:5 %	29.96207...	24.9621 %	-	554	0.09950
PPr		ADDR5.T.2:U19.17 [ADDR5]					Global	150 MIL:5 %	37.04171...	32.0417 %	-	498	0.08944
PPr		ADDR6.T.2:U19.18 [ADDR6]					Global	150 MIL:5 %	37.67383...	32.6738 %	-	493	0.08855
PPr		ADDR7.T.2:U19.19 [ADDR7]					Global	150 MIL:5 %	44.75347...	39.7535 %	-	437	0.07849
MGrp		C2 (8)											
PPr		ADDR0.T.2:U20.11 [ADDR0]					Global	150 MIL:5 %	32.33215...	27.3322 %	-	383	0.06079
PPr		ADDR1.T.2:U20.12 [ADDR1]					Global	150 MIL:5 %	37.27915...	32.2792 %	-	355	0.06376

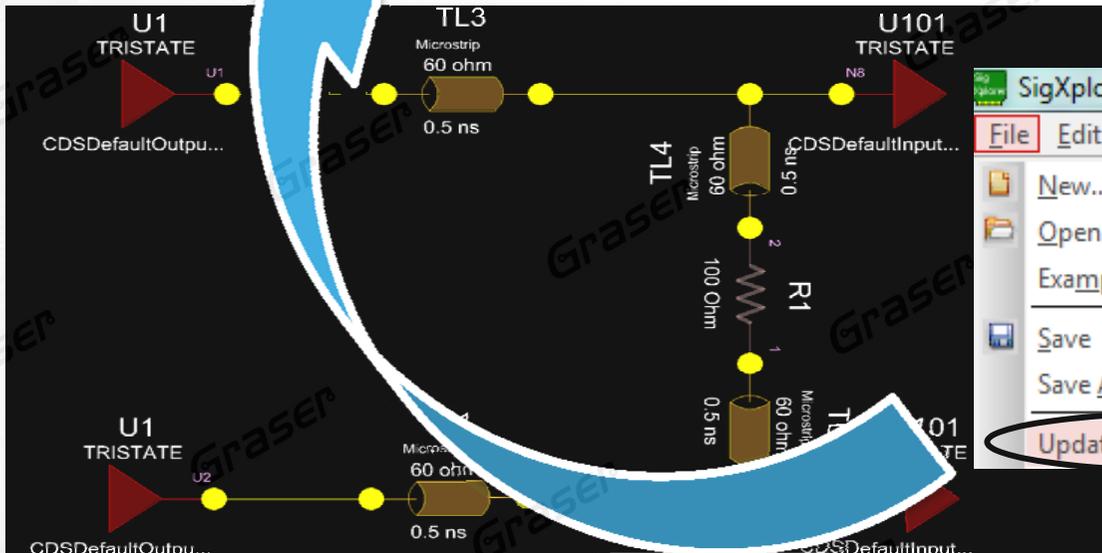
Pin Pair: ADDR3.T.1:ADDR3.T.3 [Match Group B2, Net ADDR3]

DRC SYNC XNET

- Auto create Pin-Pair by Each Net
- Auto match Group by Pin-Pair
- Auto assign constraints by each Pin-Pair



- One mouse click makes you ready for SI Analysis



SigXplorer OrCAD PCB SI: CLK_DDR2_0_N

File Edit View Setup Analyze

New... Ctrl+N
Open... Ctrl+O
Example...
Save Ctrl+S
Save As...

Update Capture

To	Scope	Delta	Tolerance
U101.N8	LOCAL	0 ns	5 ns
U101.N8	LOCAL	5 ns	5 ns

Rule Editing

Rule Name: CLK_DDR2_0_N_M1

From: U1.U1
To: U101.N8
Scope: Local
Delta Type: Delay
Delta: 0 ns
Tol Type: Delay
Tolerance: 5 ns

OK Apply Cancel Help

F.A.B.

- **Enhance constraints design flow with OrCAD SI**
 - OrCAD SI can help us to determine design constraints
 - It can back annotate ECsets and store information in Capture
 - Directly translate design constraints from netlist files
 - Drawing and constraints reuse