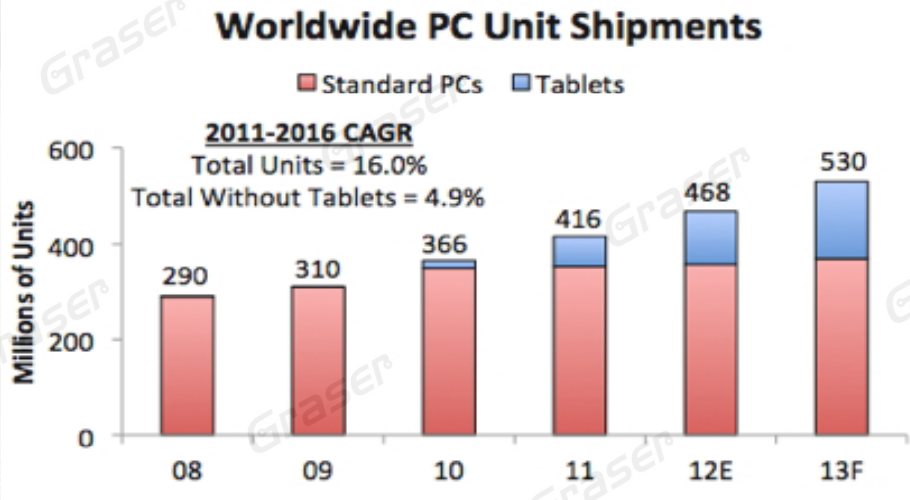
2013 Graser User Conference

13/Aug/2013

Predictions and Highlights in the WW

- Global tablet shipments will overtake Standard PCs shipments in 2013



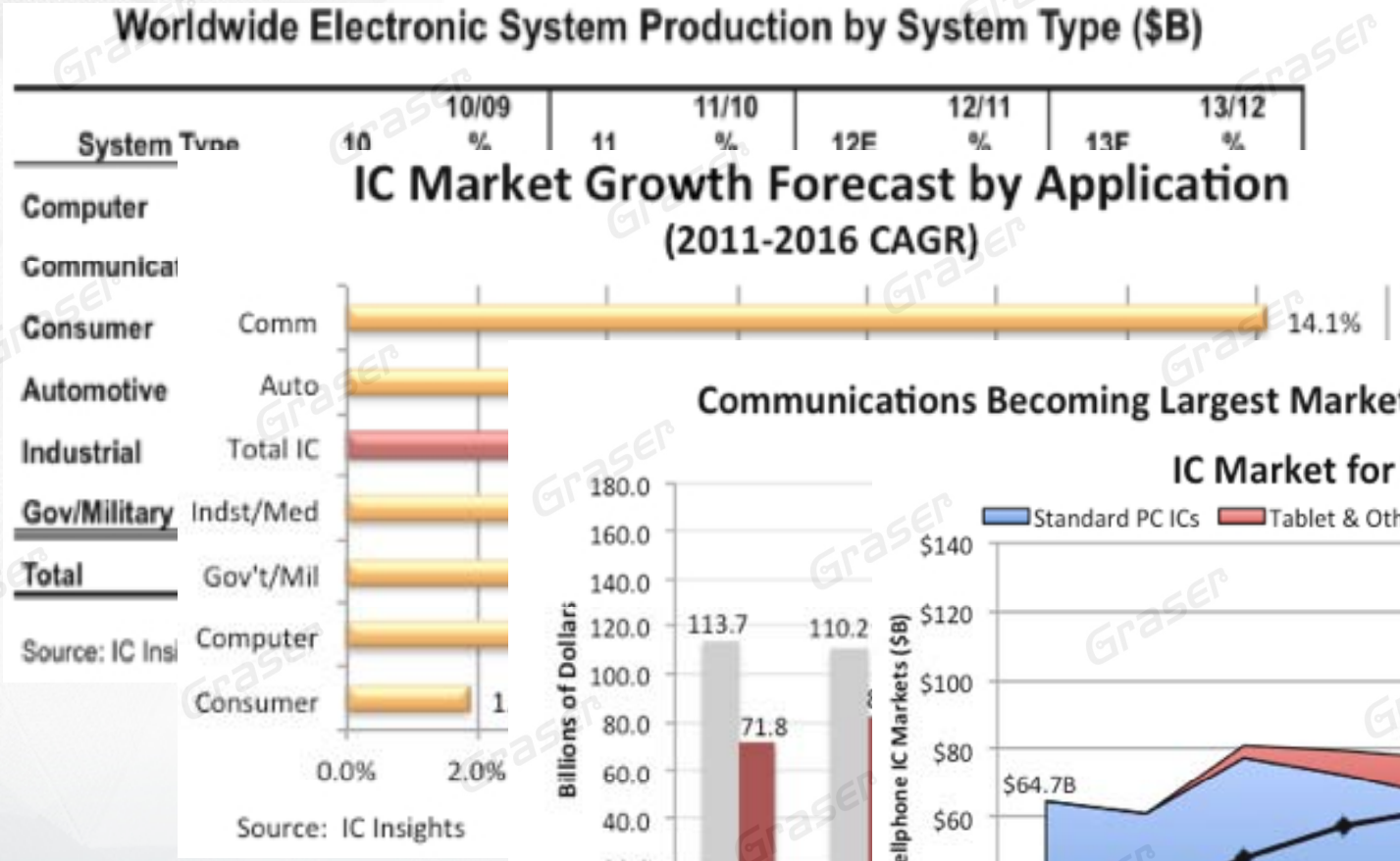
Source: IC Insights

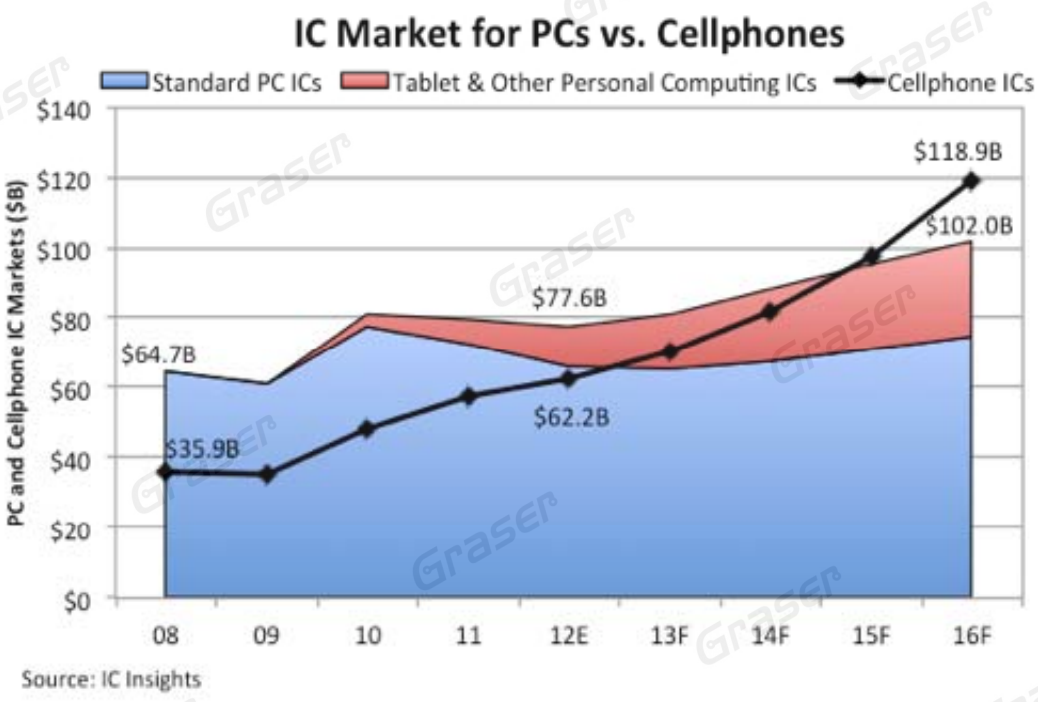
Global and Taiwan shipment forecasts, 2013 (m units)				
Product line	**Global shipments**	**Growth from 2012**	**Total Shipments by Taiwan-based makers**	**Growth from 2012**
Notebook	182	(5.3%)	154	(9.9%)
Tablet	228	62.2%	120.8	24.5%
Server	8.8	3.5%	5.0	4.2%

Source: MIC, compiled by Digitimes, May 2013

Predictions and Highlights in the WW

- Communications to Surpass Computers As Leading Application for ICs



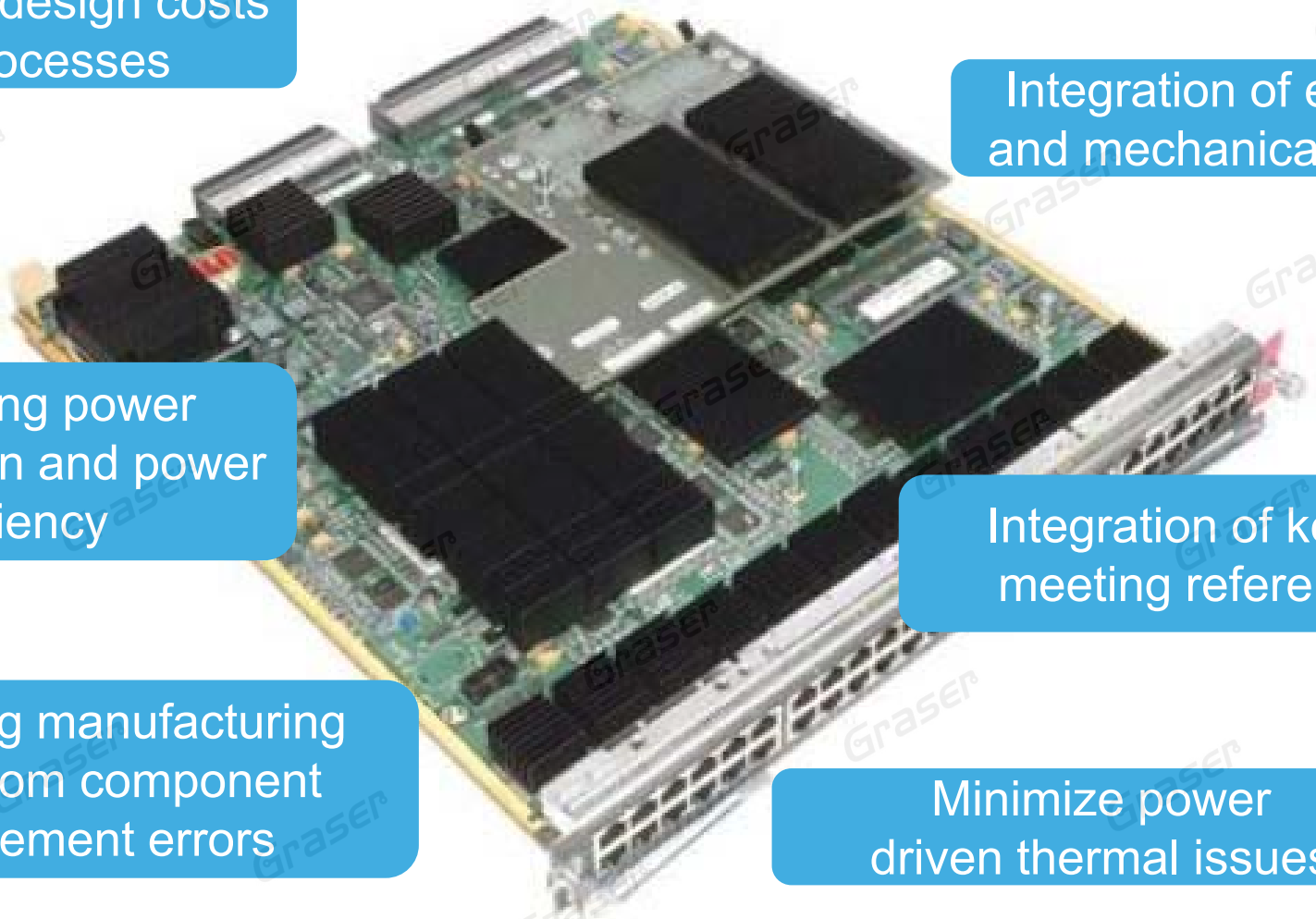


High End Consumer Electronics Design Challenges

Common Product Creation Design Challenges

Optimizing design costs and processes

Integration of electronics and mechanical enclosure



Optimizing power consumption and power efficiency

Integration of key silicon meeting reference data

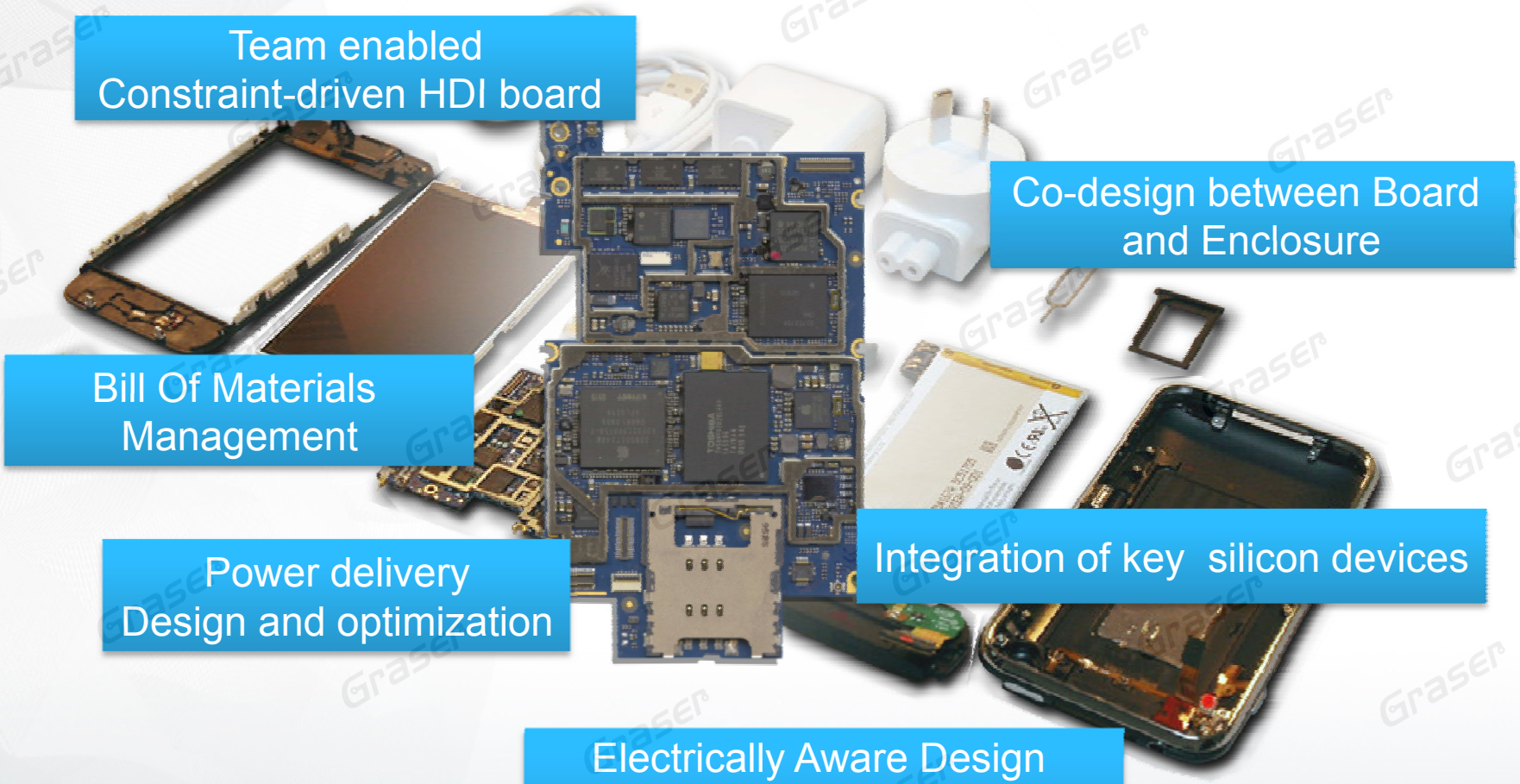
Preventing manufacturing delays from component procurement errors

Minimize power driven thermal issues

Maximize electrical and signal performance

High End Consumer Electronics Design Key Challenges

Mechanical/PCB/Package/IC



Efficient Product Creation Needs

- Best-in-class co-design enabled IC, Package and PCB design environment
- Electrical and physical constraint driven design architecture
- Best-in-class Power Aware Signal Integrity signoff analysis
- Collaborative, managed, predictable and productive team design across the ECAD/MCAD hardware design process
- Design data integration into corporate data systems to manage cost, quality and productivity
- On-time, efficient standard release into manufacturing

Why Cadence for High End Consumer Electronics Hardware Design

2013 AUG TAIPEI Graser User Conference

Topics

- Optimizing across IC, Package and PCB
- Custom IC and Digital IC Design Solution
- Constraint Driven Design Architecture
- Characterized Design-in IP Beyond the Reference Board
- Electrical Performance Analysis, Verification and Compliance Signoff
- High Speed PCB Design
- Driving Design Density and Enclosure Integration
- Team Enabled Project Collaboration and Management
- Driving the Path to Manufacture

Optimizing across IC, Package and PCB

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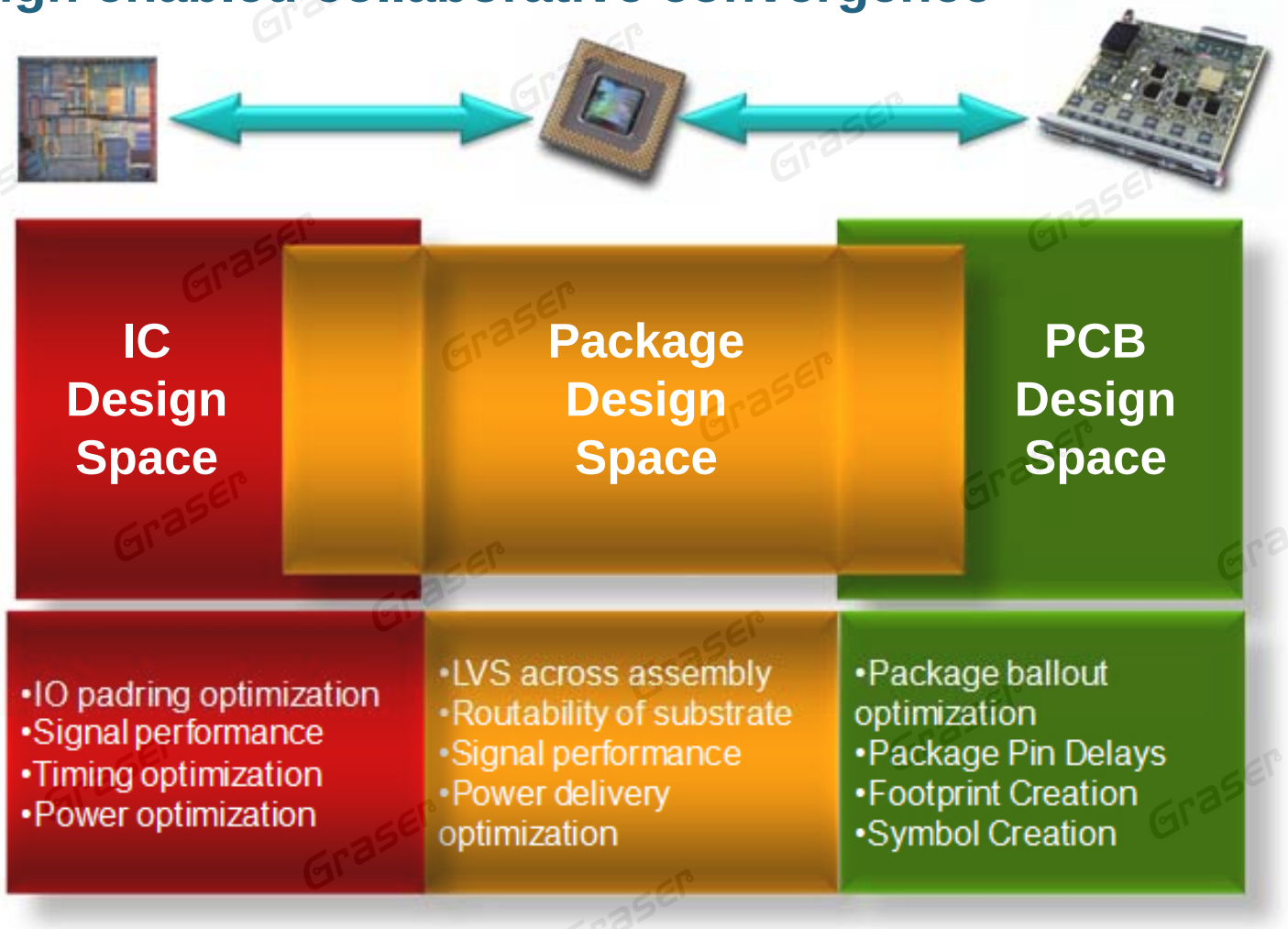
Optimizing across IC, Package and PCB

Co-design enabled collaborative convergence

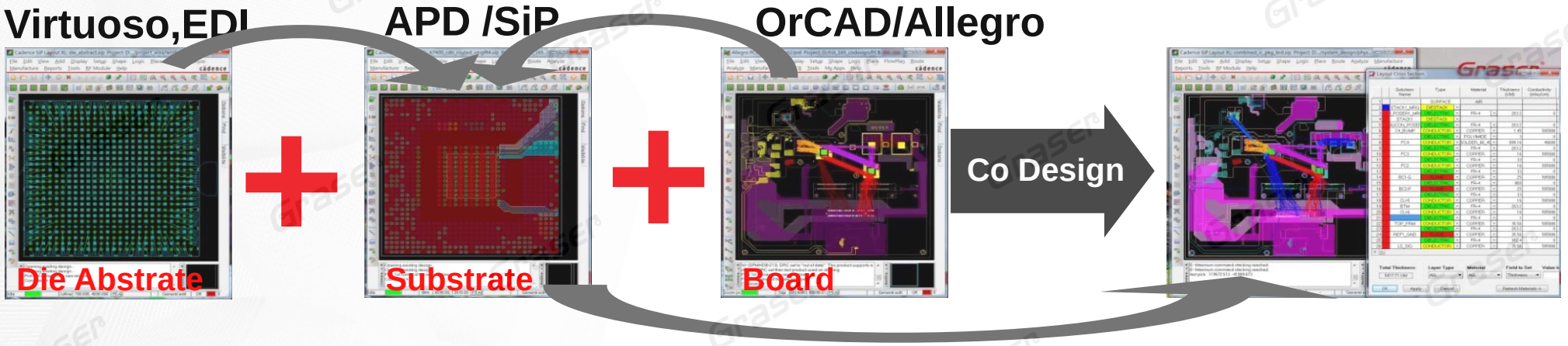


- Delivers optimal package and chip (size, cost, performance, power)
- Validates device-level timing and power performance
- Minimizes board complexity and cost
- Reduces ECO risk providing schedule predictability

Optimizing across IC, Package and PCB

S-P-B EcoSystem

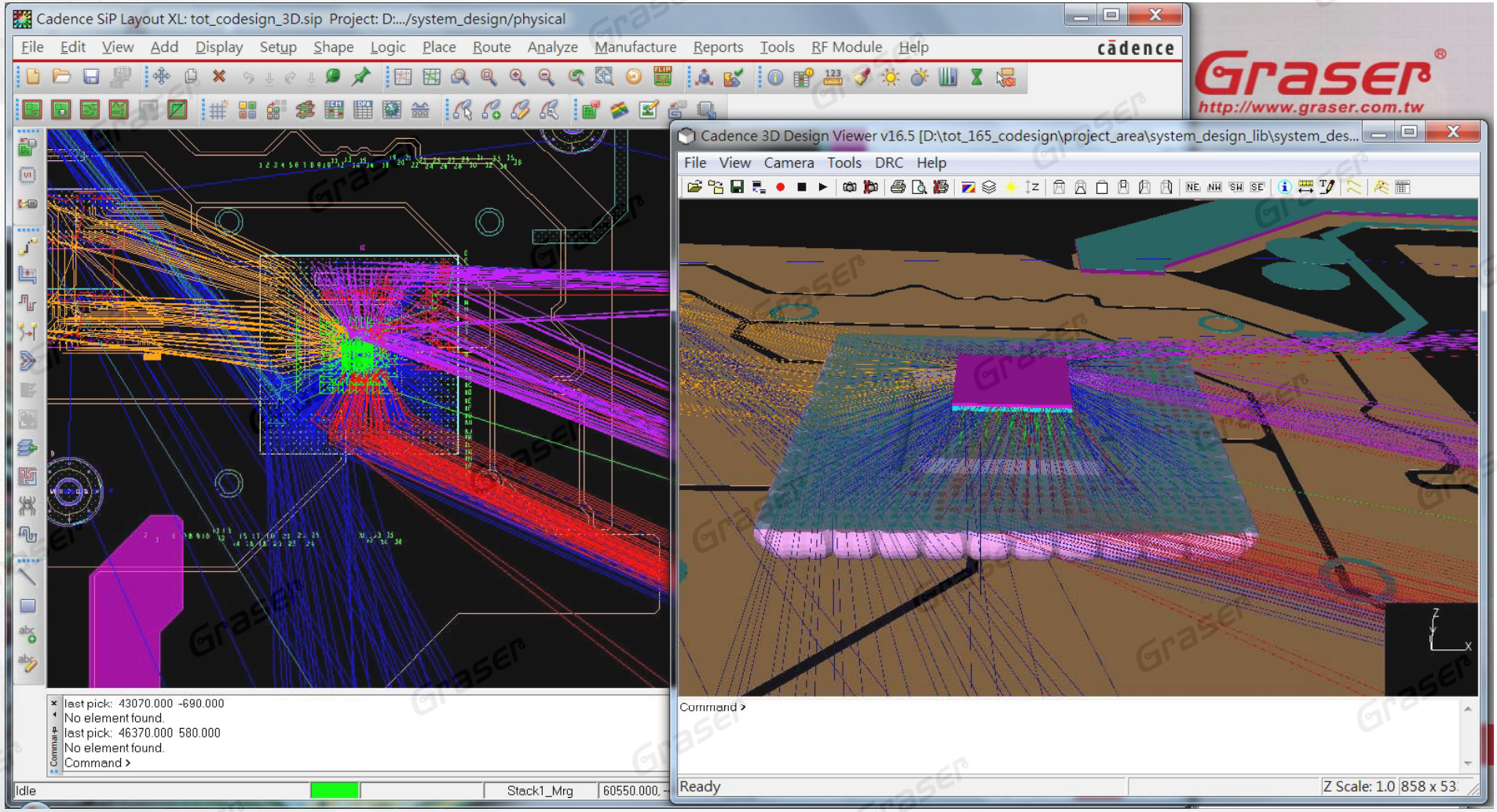
- Flexible IC and Package Co-Design Environment
  - (F.E.) System level connectivity & constraint management
  - (B.E) Tight integration for IC, Package (SiP) or PCB driven flows & Database



- Concurrent and Distributed Co-design modes
  - IC tool/database for IC tasks, IC Packaging tool/database for Packaging tasks.
    - Mask quality RDL routing
    - Artwork quality bump escape routing
  - IC awareness at the Package Substrate level for optimum designs
    - Fully supports Rapid Prototyping and design implementation flows
  - IC extraction/modeling for chip level interconnect
  - Package extraction/modeling for package and PCB level interconnect

Optimizing across IC, Package and PCB

S-P-B EcoSystem

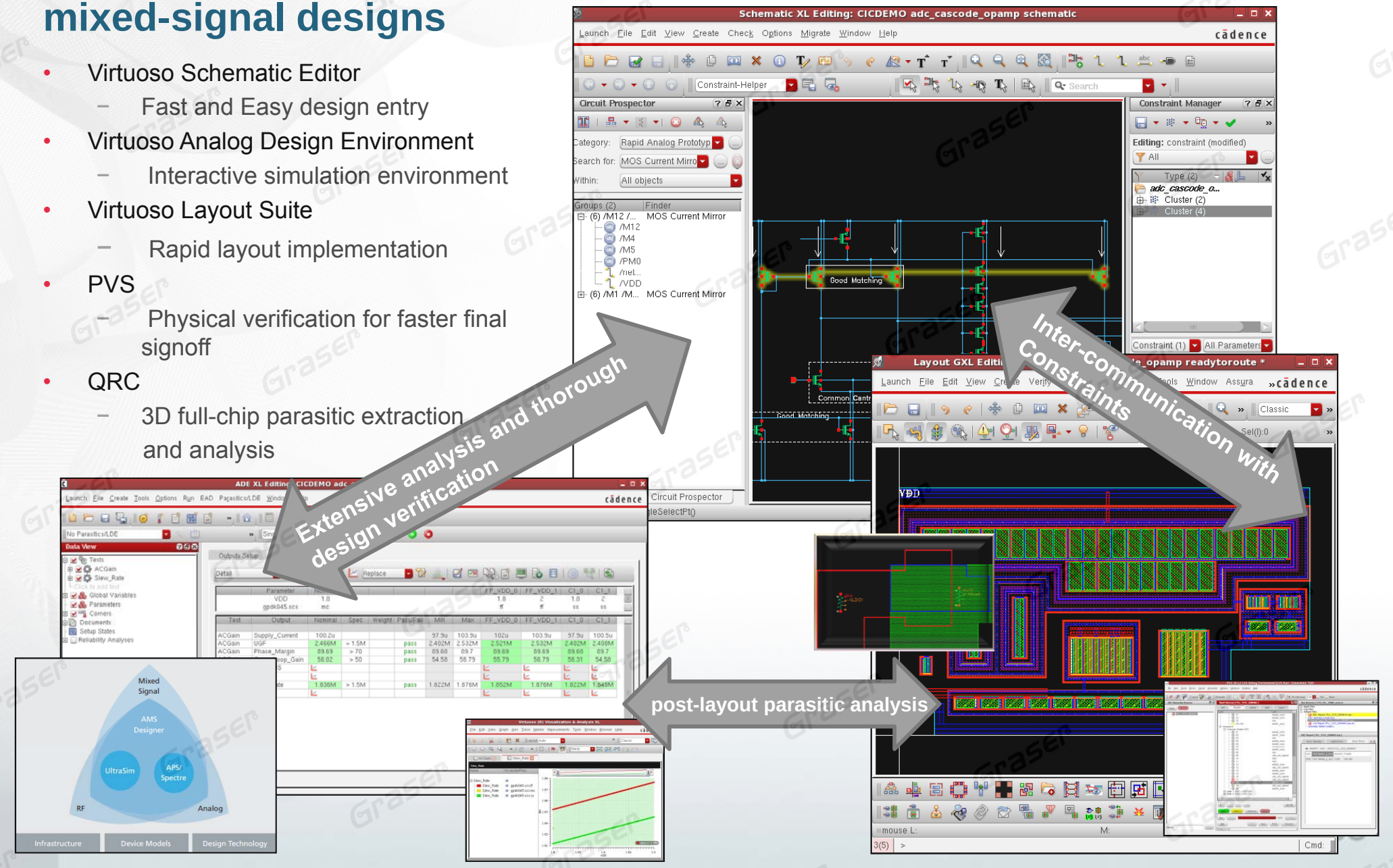


Custom IC and Digital IC Design

Cadence Custom IC Design solution

The complete solution for front to back end custom-analog, RF, and mixed-signal designs

- Virtuoso Schematic Editor
  - Fast and Easy design entry
- Virtuoso Analog Design Environment
  - Interactive simulation environment
- Virtuoso Layout Suite
  - Rapid layout implementation
- PVS
  - Physical verification for faster final signoff
- QRC
  - 3D full-chip parasitic extraction and analysis



Incisive Enterprise Simulator

The complete solution for front end digital simulation

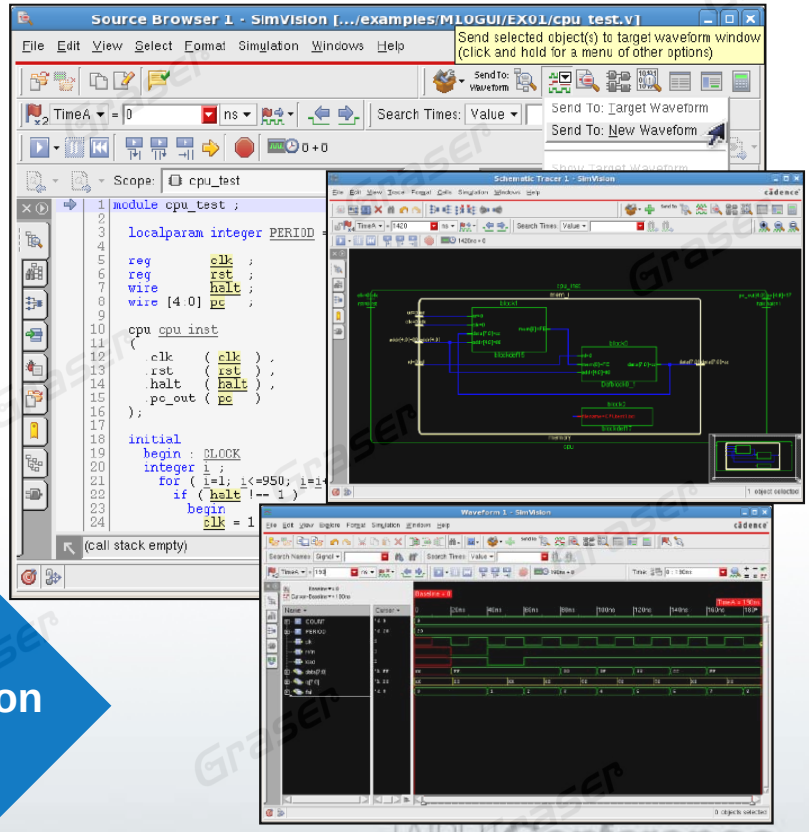
Sources

Single Step Execution

- Invokes Compilers
- Invokes Elaborator
- Invokes Simulator

irun sources_files [options]

Debug/Verification

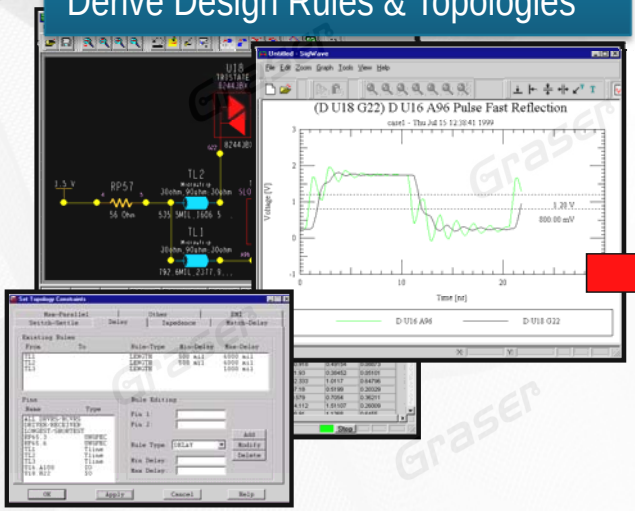


Constraint Driven Design Architecture

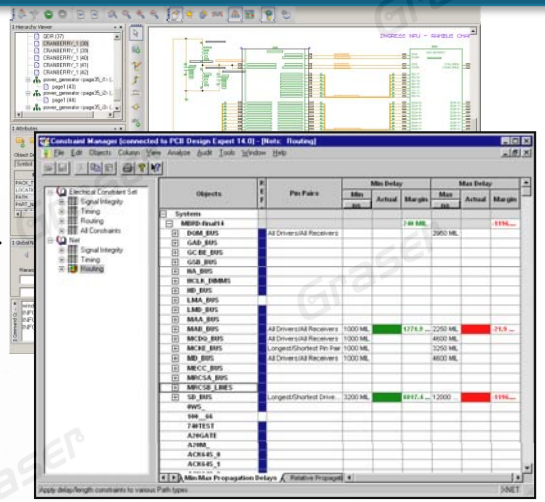
Constraint Driven Design Architecture

Enabling First Pass Success

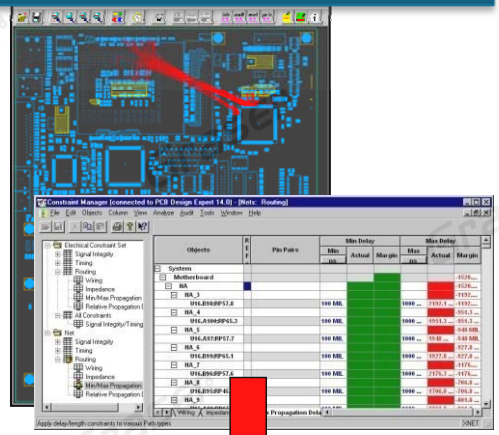
Exploration:
Derive Design Rules & Topologies

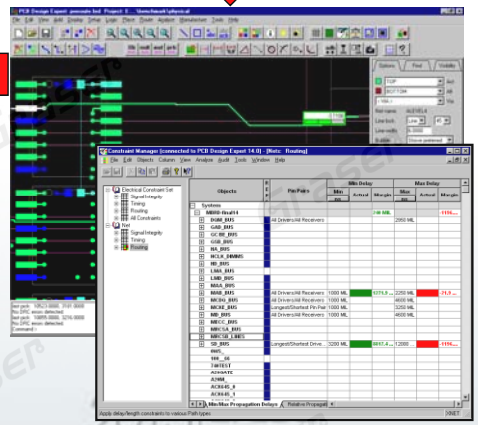


Implementation:
Schematic Entry & Rules Application

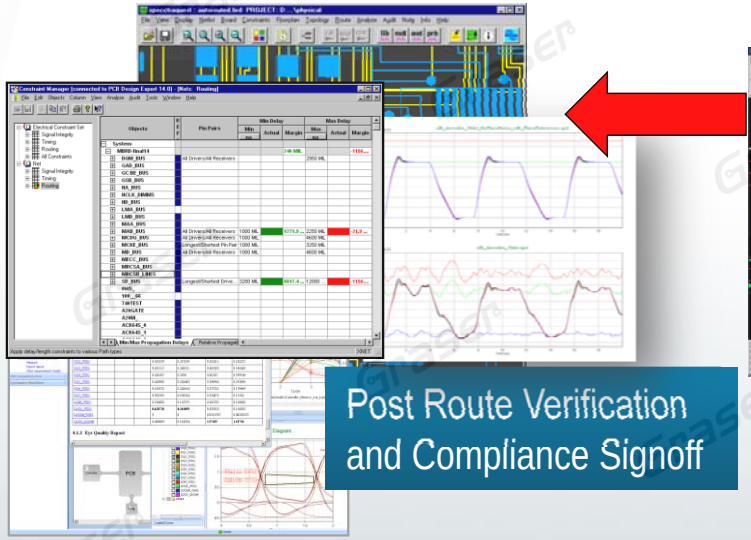


Constraint Driven
Floorplanning and Placement





Constraint Driven Routing



Post Route Verification
and Compliance Signoff

- Correct-By-Design Methodology
- Enter and Manage Constraints in Schematic or PCB Layout
- Single Constraint Environment accessed at any stage of design
- No constraint translation required
- Supports IP Design Reuse and Team Design

Smartphone/Tablet Design Using Cadence

Mechanical/PCB/Package Optimization

- Constraint Driven design reduces design cycles, risks and costs and enables intelligent Design-In IP Kits
- Single BOM Management prevents components procurement errors and unexpected cost overrun
- Co-design optimization between board and enclosure ensures optimal integration without unpredictable design re-work or design compromise
- Power Delivery Analysis ensure performance and efficiency while minimizing board and capacitor costs
- Power Driven Thermal Hotspot management prevents premature hardware failures or need for expensive cooling solutions
- Electrically aware design ensures system performance without the need for physical prototyping
- Co-design optimization between SoC/ASIC/PCB and package ensures design performance with minimized overall hardware cost and risk

Characterized Design-in IP Beyond the reference board

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Challenges with Design-in of Complex Devices

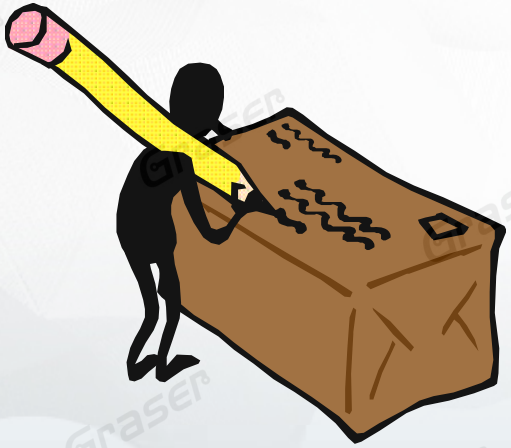
- Complex chip set evaluations can be time consuming
- Design-in onto to a PCB tends to be time consuming
- Support for evaluations and design-in across geographies can be challenging
- Desired Outcomes:
  - Faster and more predictable evaluations
  - Shorter time to ramp-up
  - Efficiently scale faster across the world

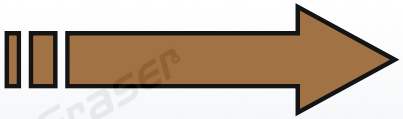
Characterized IP Design-in Kit Definition

A “Design-in Kit” is

packaged and executable design data,

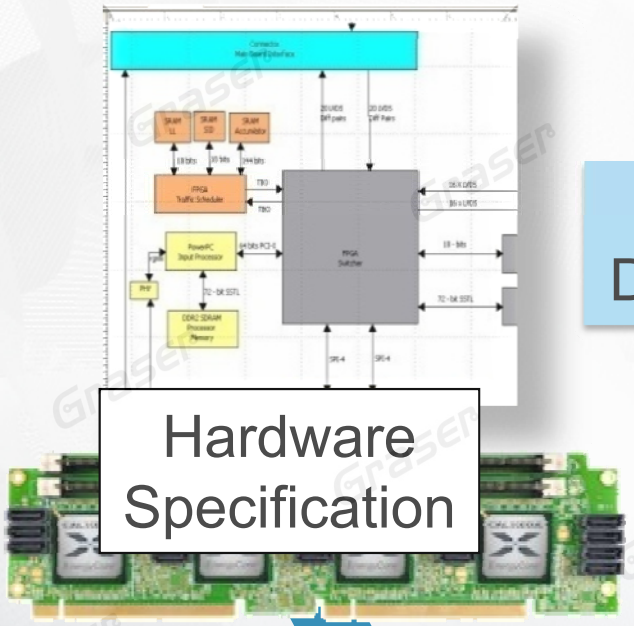
built by IC companies and used by System companies.





Characterized IP Driven Hardware Design

- Streamlined process for design implementation and verification of hardware
  - Driven by specification characterized Design-in and Verification IP
- Raises the level of design abstraction – reducing design cycles & costs
  - Interface protocol level design authoring, implementation and verification compliance
  - System block architecture, detailed design authoring, PCB implementation



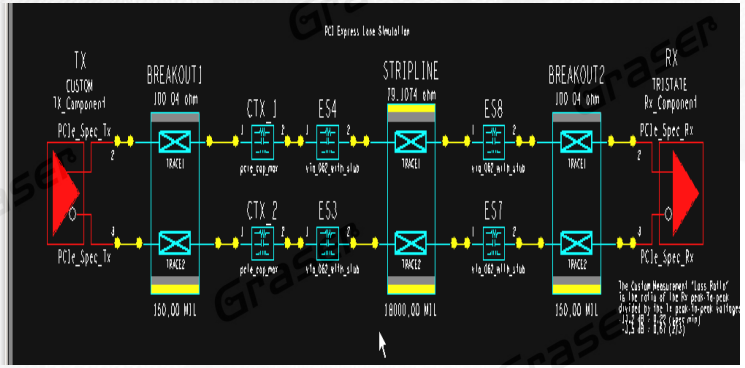
Hardware Specification

Characterized Design & Verification IP Kit

Kits available for:
DDR3, LPDDR3 PCIe Gen 3, SFP+, HDMI, 10G-Base KR
In development:
SATA, USB3

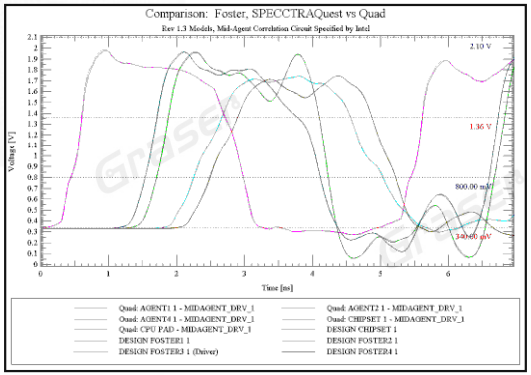
IP driven hardware design and verification solution

Reference Design versus Design-in Kit

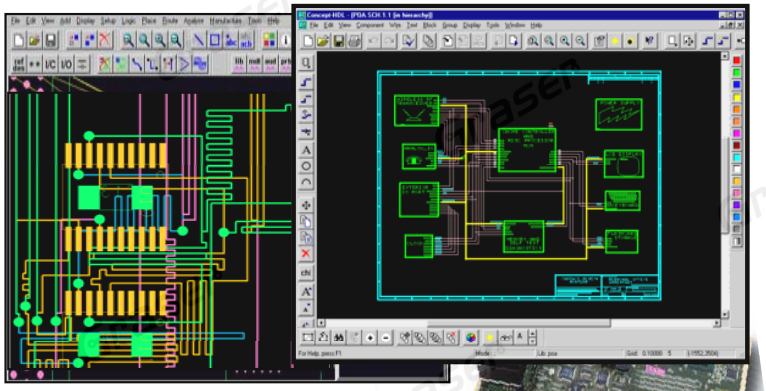


Simulation Files

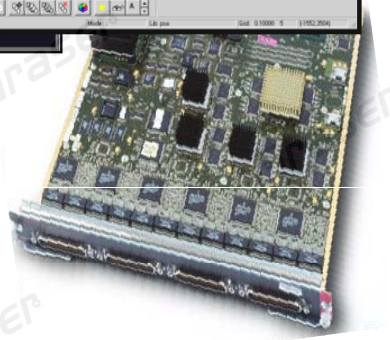
Models, Topologies, etc.

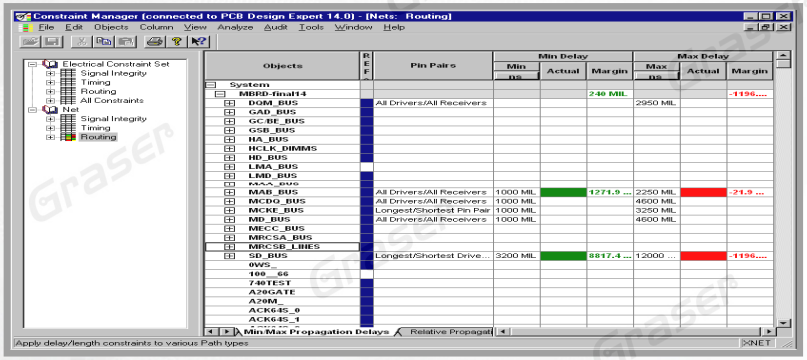


Correlation Data



Schematics and PCB Layout for Reference Design





Automated Layout Guidelines (Constraints)

- Applied to Reference Design
- Ready to be re-used

"Ready to simulate in minutes"

Tutorials

- Web based documentation
- Movie clips showing tools and IP in action

Electrical Performance Analysis, Verification and Compliance Signoff

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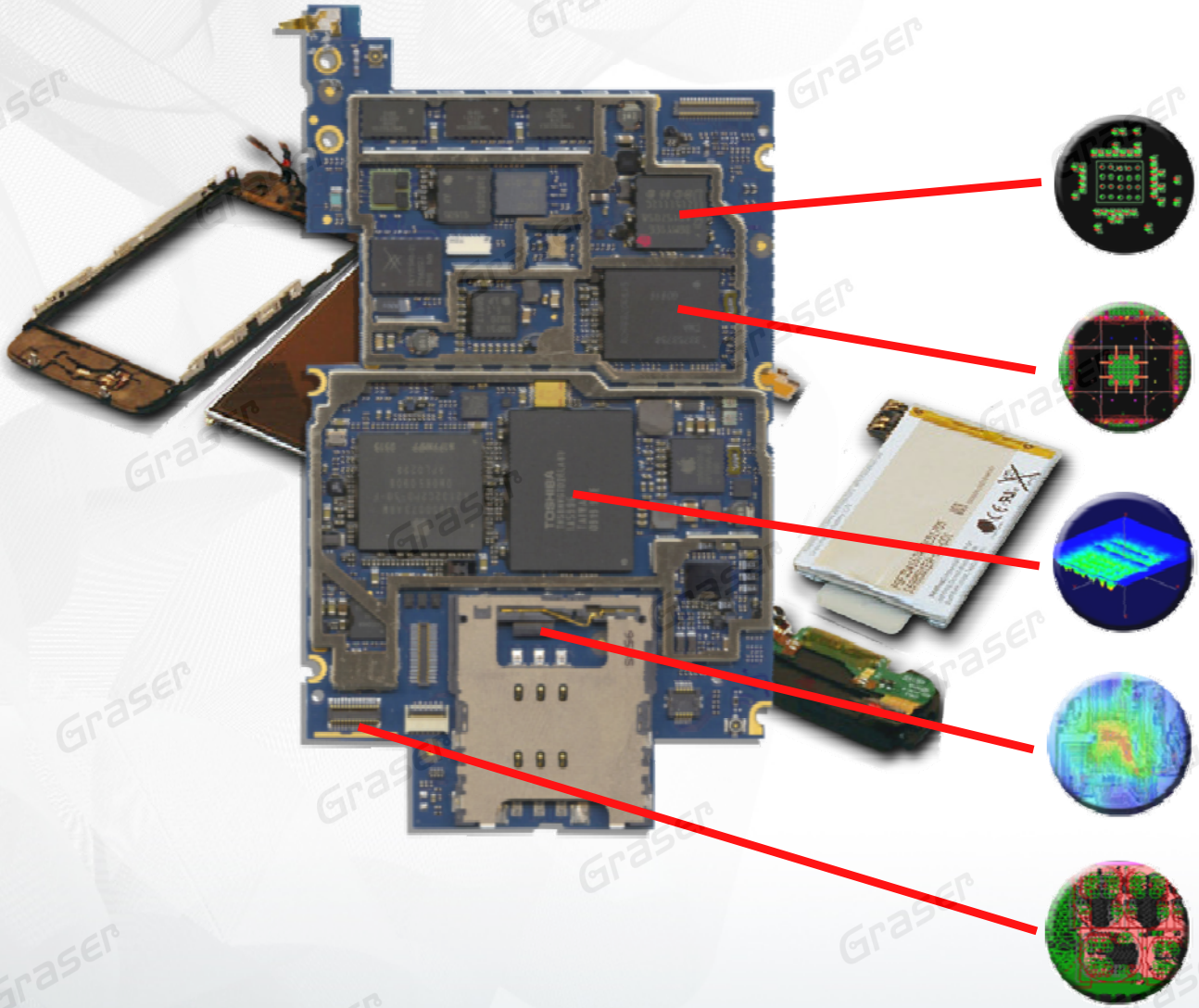
High-Speed Analysis, Verification and Compliance



Decap Optimization *

Assure power delivery system performance constraints are met while also targeting a decoupling scheme that is cost effective and conserves space.

Chip-Package-Board Modeling

Create ports for individual or grouped pins to achieve the desired level of abstraction when using models for either chip-centric or system-centric simulations.

Co-Design

Simultaneously simulate the entire chip power grid with the package / board in the time and frequency domain to find power integrity issues that are otherwise missed.

EMI / EMC *

Gain design stage visibility into potential hot spots with near and far-field radiation studies to compliment signal and power integrity analysis.

High-Speed Interface Analysis *

Effectively deal with parallel (DDR) and serial (PCI-E) design challenges by analyzing system-wide behavior using SSO and channel studies.

* - market unique capabilities

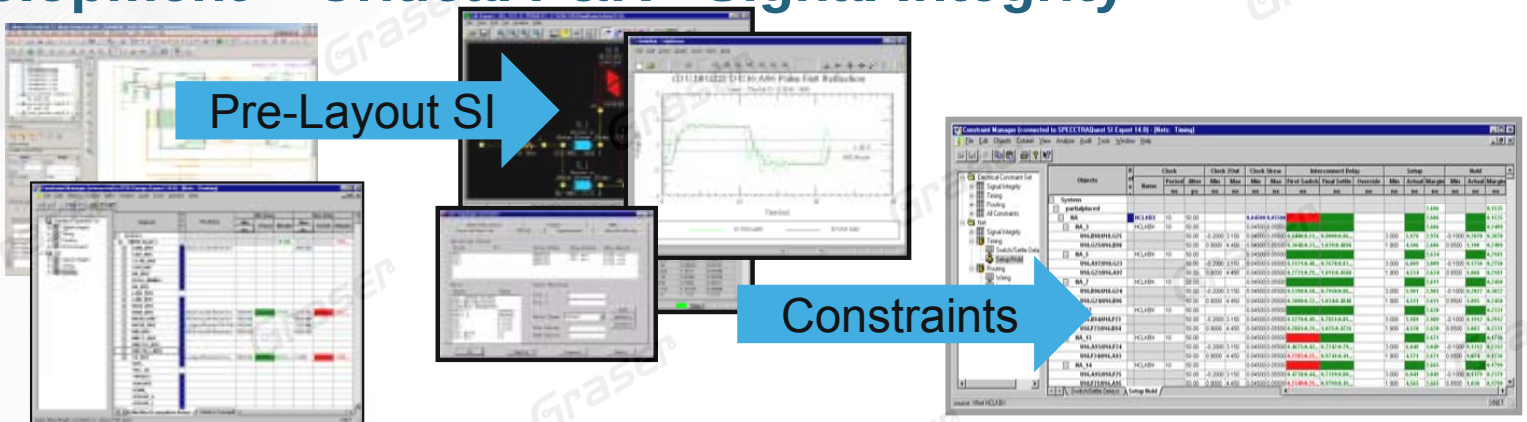
Sigrity Powered SI: Supports Multiple Engineers

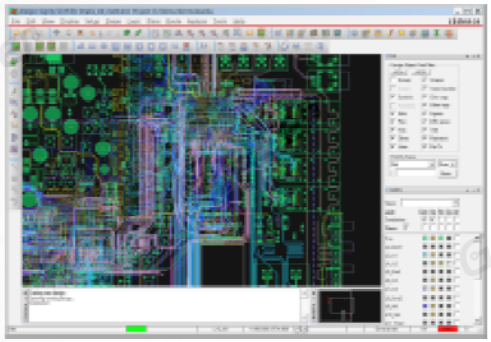
Constraint Development + Critical P&R+ Signal Integrity

Constraint Developer

Engineer

Signal Integrity Engineer



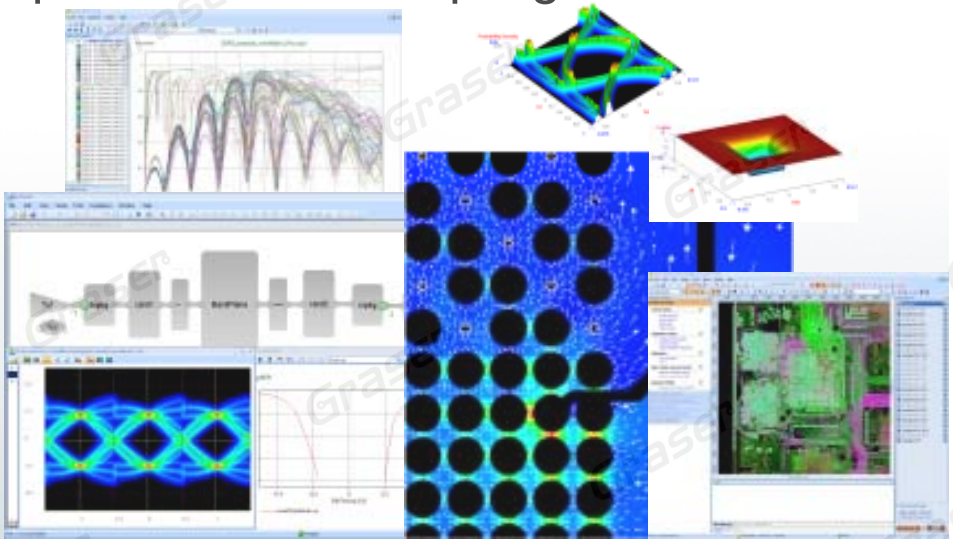


Layout Functionality for Engineers:

- Placement
- Padstack Editing
- Routing and Shape Editing
- Impedance and Coupling Check

Launch Detailed Analysis:

- Power Aware SI
- Serial Link Analysis
- 3D Package Extraction



Sigrity Powered SI:

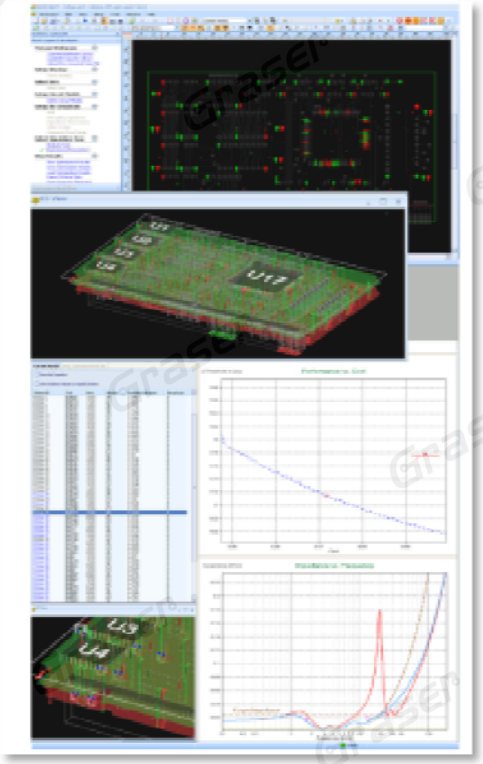
Constraint driven throughout the design flow

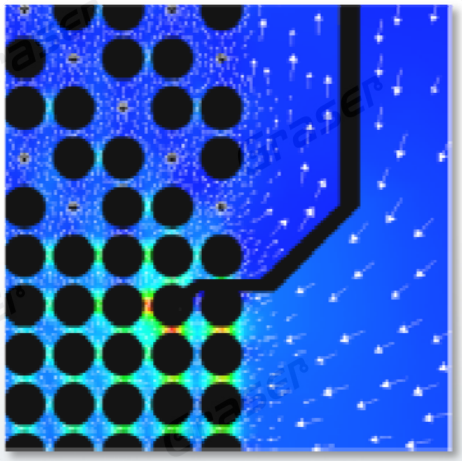
- Pre-Schematic / Pre-Layout
  - Prototype physical structures, analyze, and save for layout implementation
  - Generate constraints to drive layout
  - Generate plane shapes
  - 3D modeling and analysis (with Option)
- In-Design
  - Import/define/modify stack-up
  - Route critical signals
  - What-if SI analyses
- Post-Layout
  - Ideal Power/Ground SI Analysis
  - Power Aware SI Analysis (with Option)

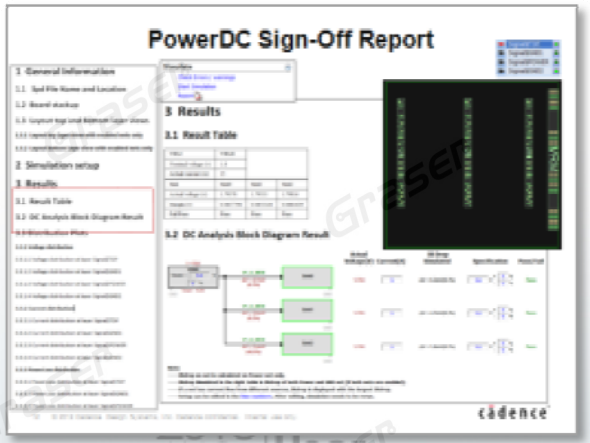
Sigrity Power Integrity

Optimize decoupling strategies and perform AC and DC Power Integrity sign-off level analysis

- Thermally-aware static IR Drop (DC analysis) can be performed through an intuitive user interface.
  - Verifies the power distribution system will provide stable and sufficient current to drive signals
  - Considers trace neck-down, swiss-cheese planes, partial planes
  - Considers all vias that connect multiple ground planes of the same net
  - Results can be viewed graphically or in a text report
- AC analysis
  - Integrated (no manual translation) design and analysis environment helps optimize decoupling strategy
- Frequency domain simulation
  - Quantify the impedance of the power delivery system across the frequency range of interest







Sigrity Power Integrity Solution

High Speed PCB Design

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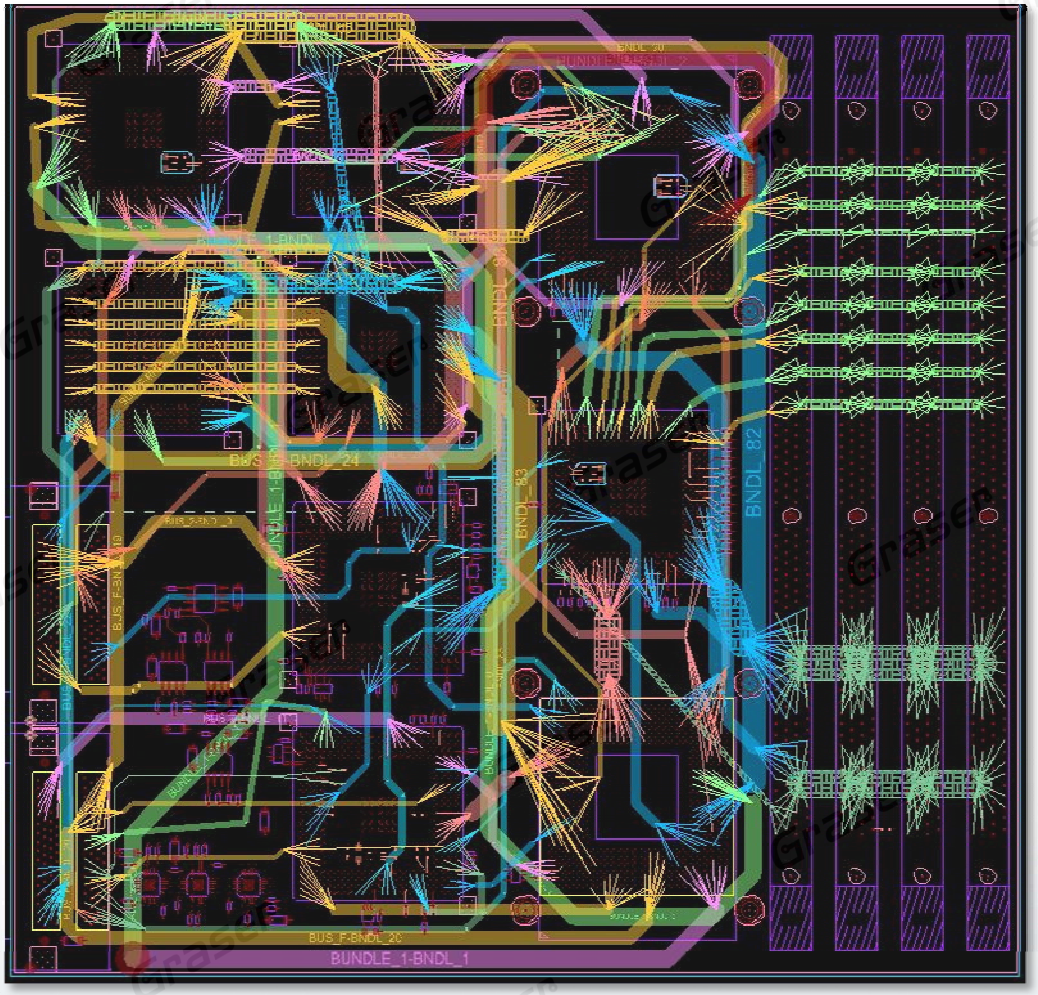
High Speed PCB Interconnect

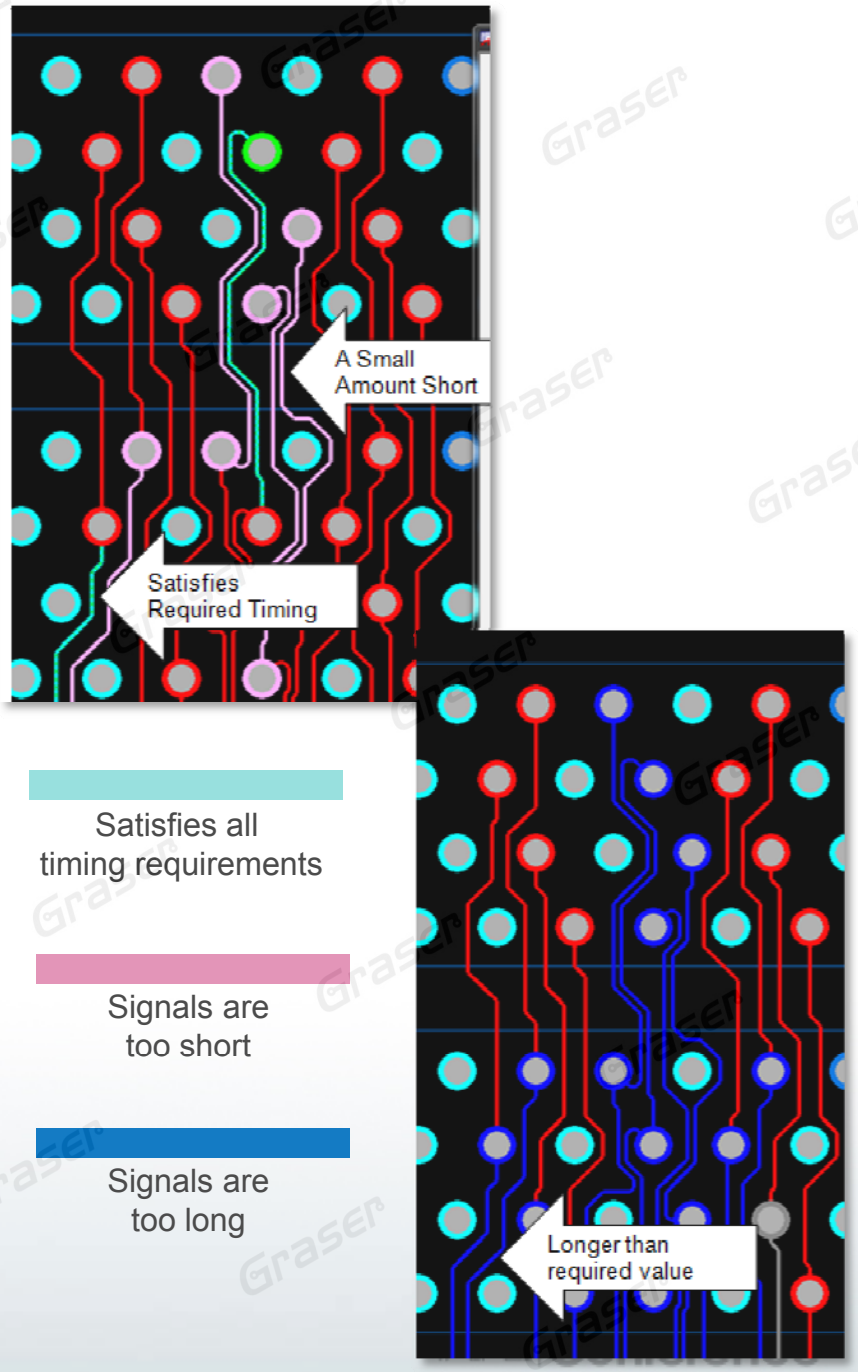
Design Planning

- Addresses challenges of high-speed (Gigabit) interfaces
  - DDR3/4, PCI Express, XAUI, eSATA etc
- Shortens design cycles, reduces unnecessary prototype iteration and makes design cycles predictable
- Enables optimized routing of high speed interfaces with reduced layer count
  - compared with traditional methods
- Unique interface flow based paradigm



Timing Vision

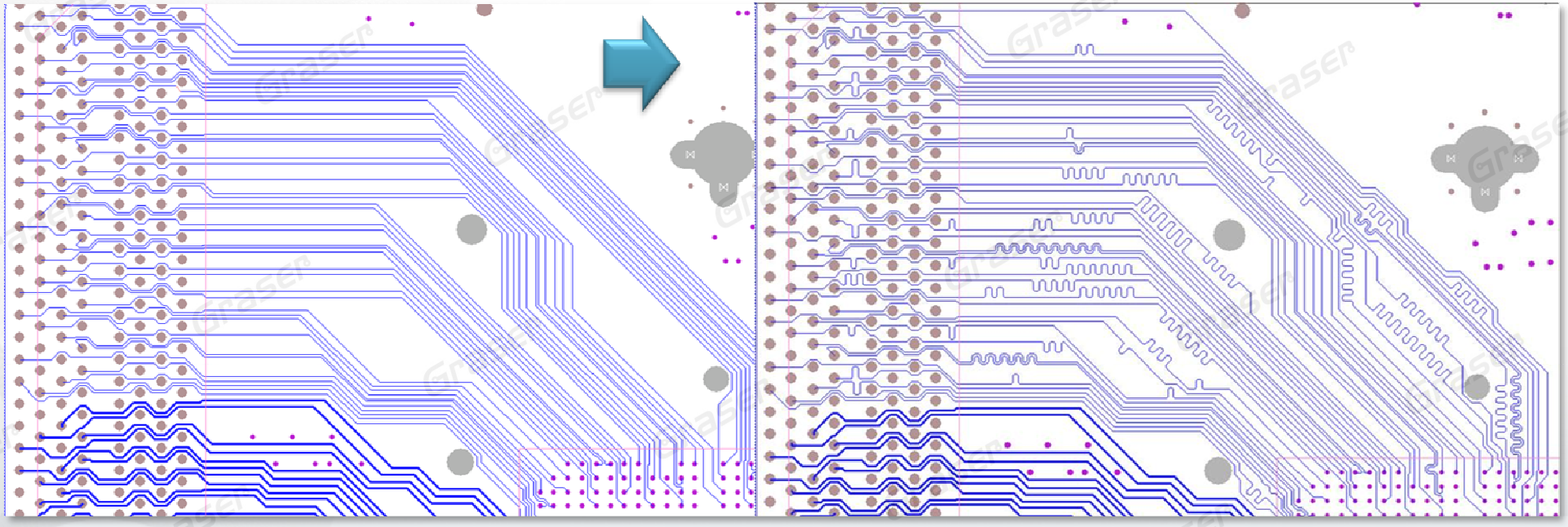
- Visualize real-time delay / phase information directly on clines
- Significantly reduces time / effort to implement timing requirements
  - Reduce trips to Constraint Manager and reports
- User-defined cline feedback
  - Coloring, stipple patterns, and customized data tip information



Auto-interactive Delay Tune (AiDT)

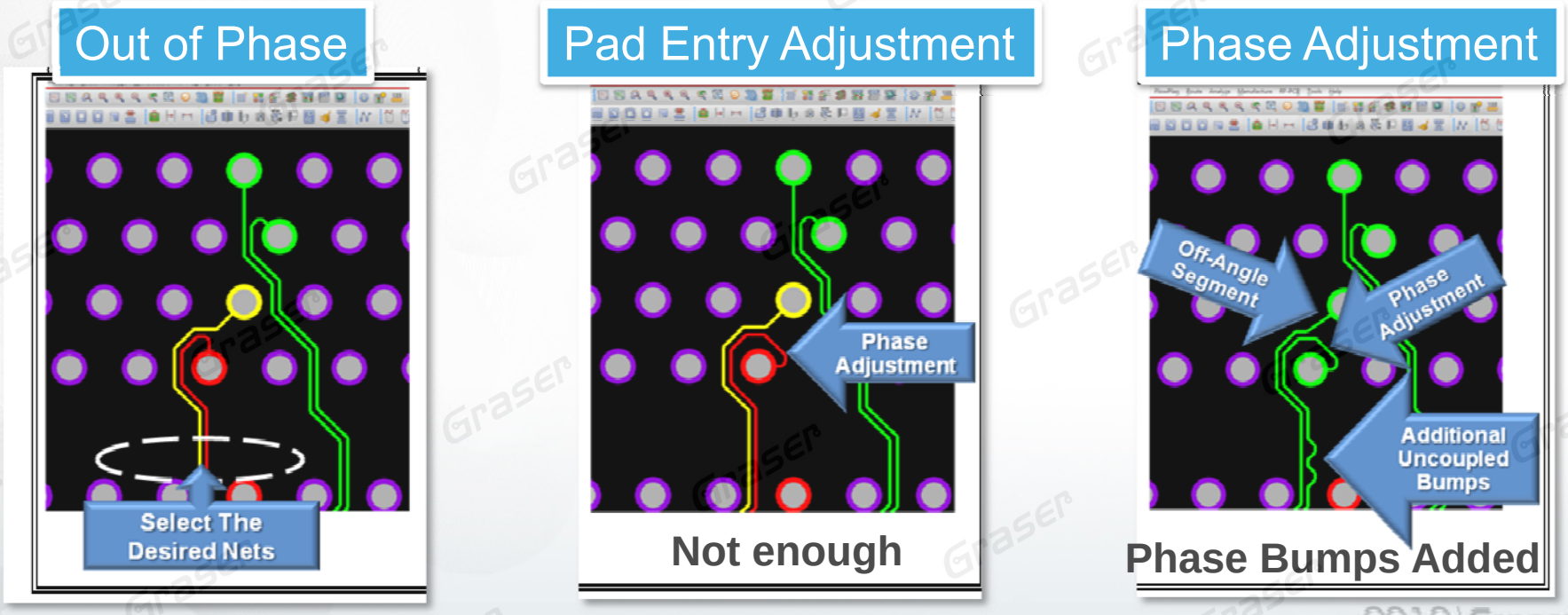
- Select a set of routed signals, AiDT adjusts timing of signals to meet defined constraints!

- Shortens time to tune high-speed signals by 30-50%



Auto-interactive Phase Tuning (AiPT)

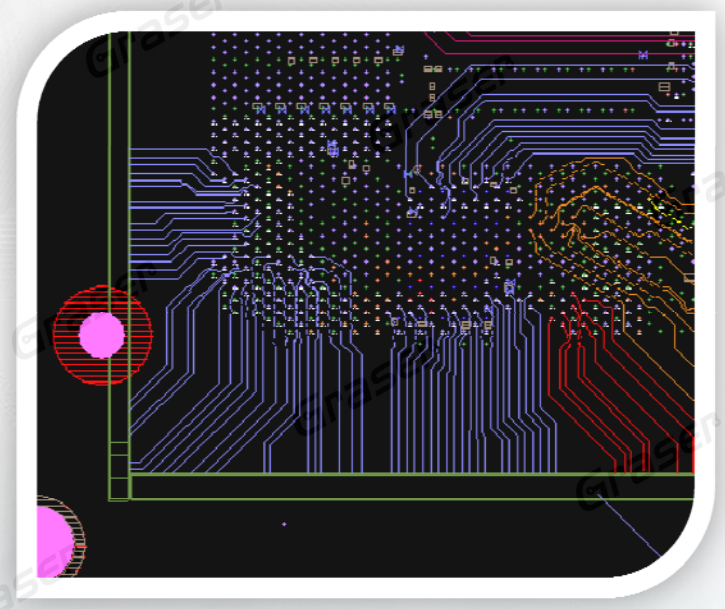
- Meet differential pair phase requirements easily
- Static and dynamic phase compensation
- User driven controlled compensation techniques

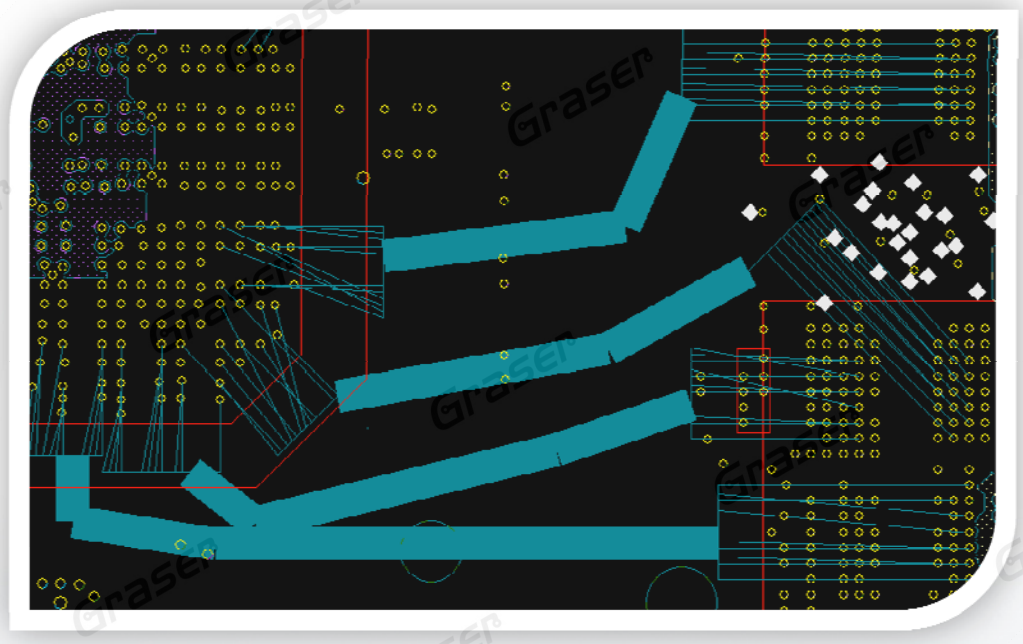


AiBT (Auto-interactive Breakout Technology)

Prototype Technology

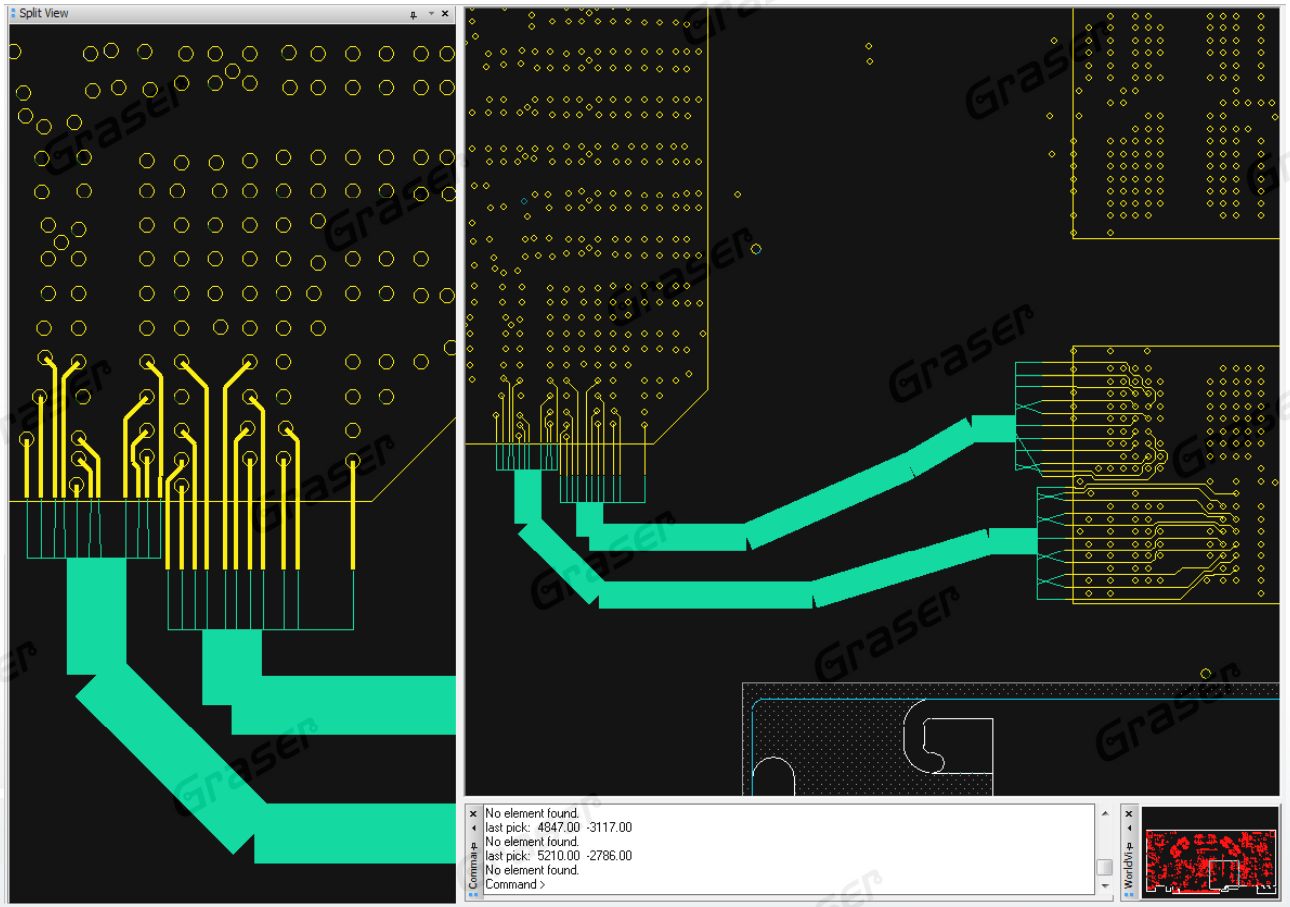
- Two use models
  - Single Component : A Focused Breakout For Layer And Feasibility Analysis
  - Bundle Based : An Interface Breakout (Both-Ends) Analysis





Auto-interactive Breakout (AiBT)

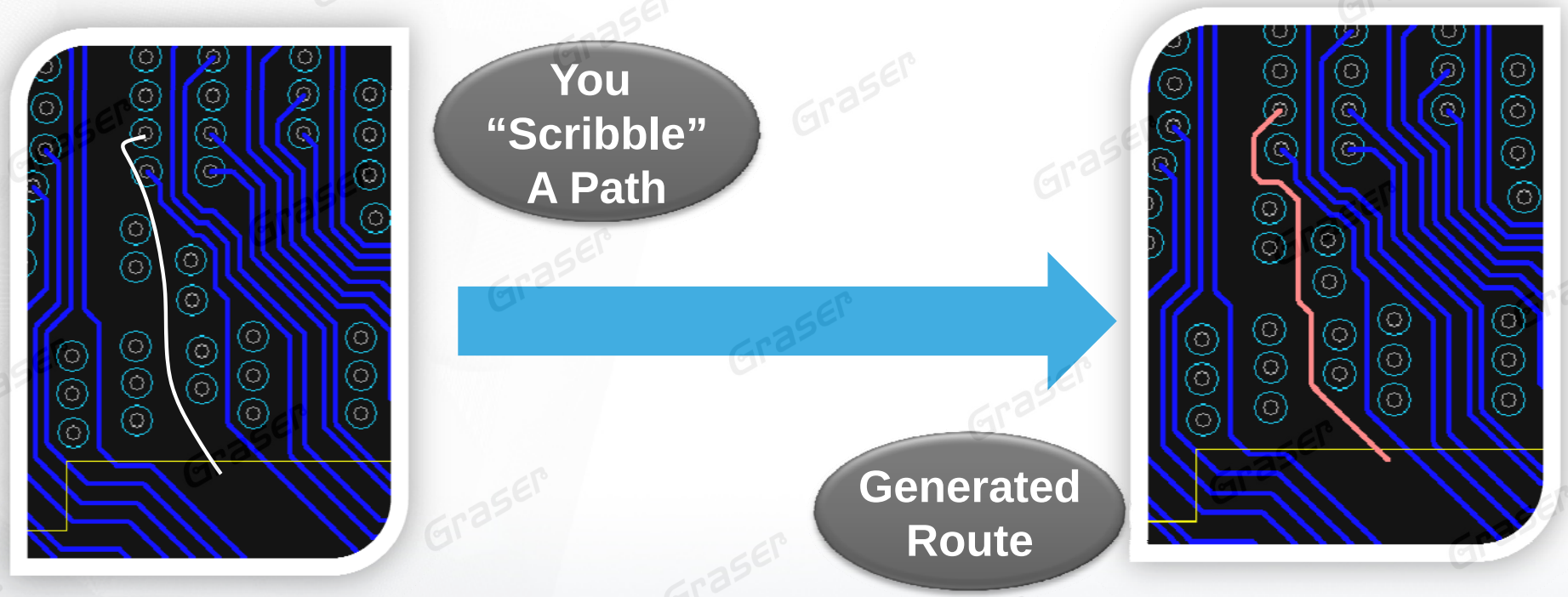
- **Automatic breakout routing**
  - Canvas driven inputs for direction, distance, sequence, layer
- **Rat management**
  - Ordering & layering
- **Split Views**
  - Work both sides



AiAC (Auto-interactive Add Connect)

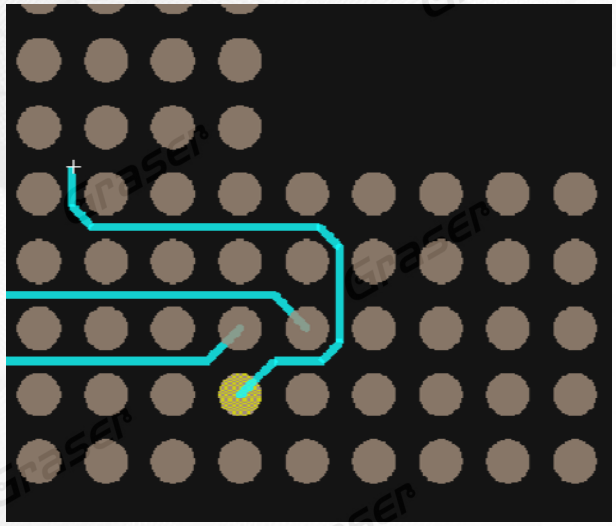
Prototype Technology

- Route To Cursor : Auto-router generated etch from last pick to cursor
- Freehand Route : Auto-route based On User drawn free-hand Path

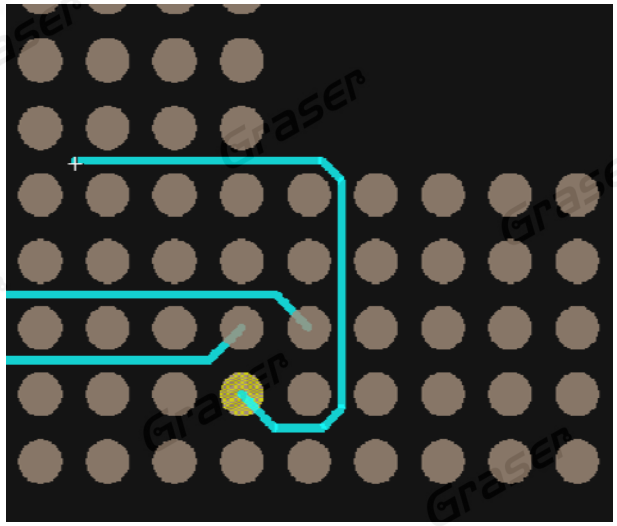


Auto-interactive Add Connect (AiAC)

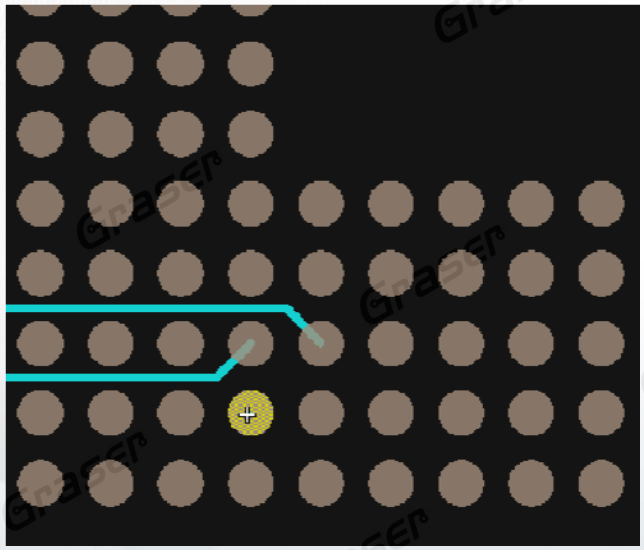
- Manual Mode

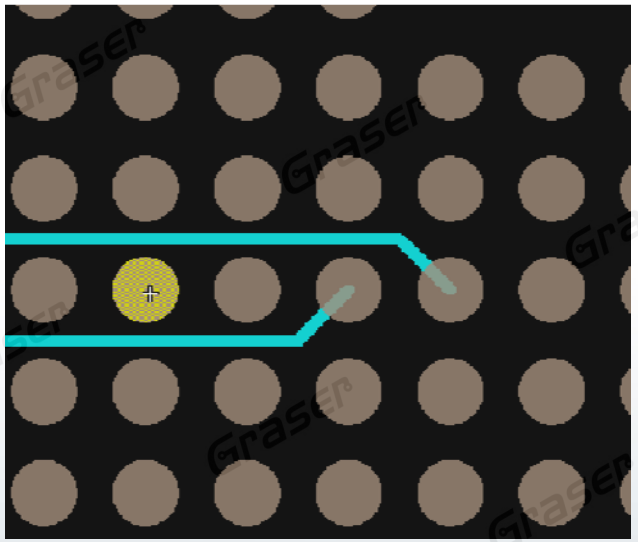


- Auto Mode



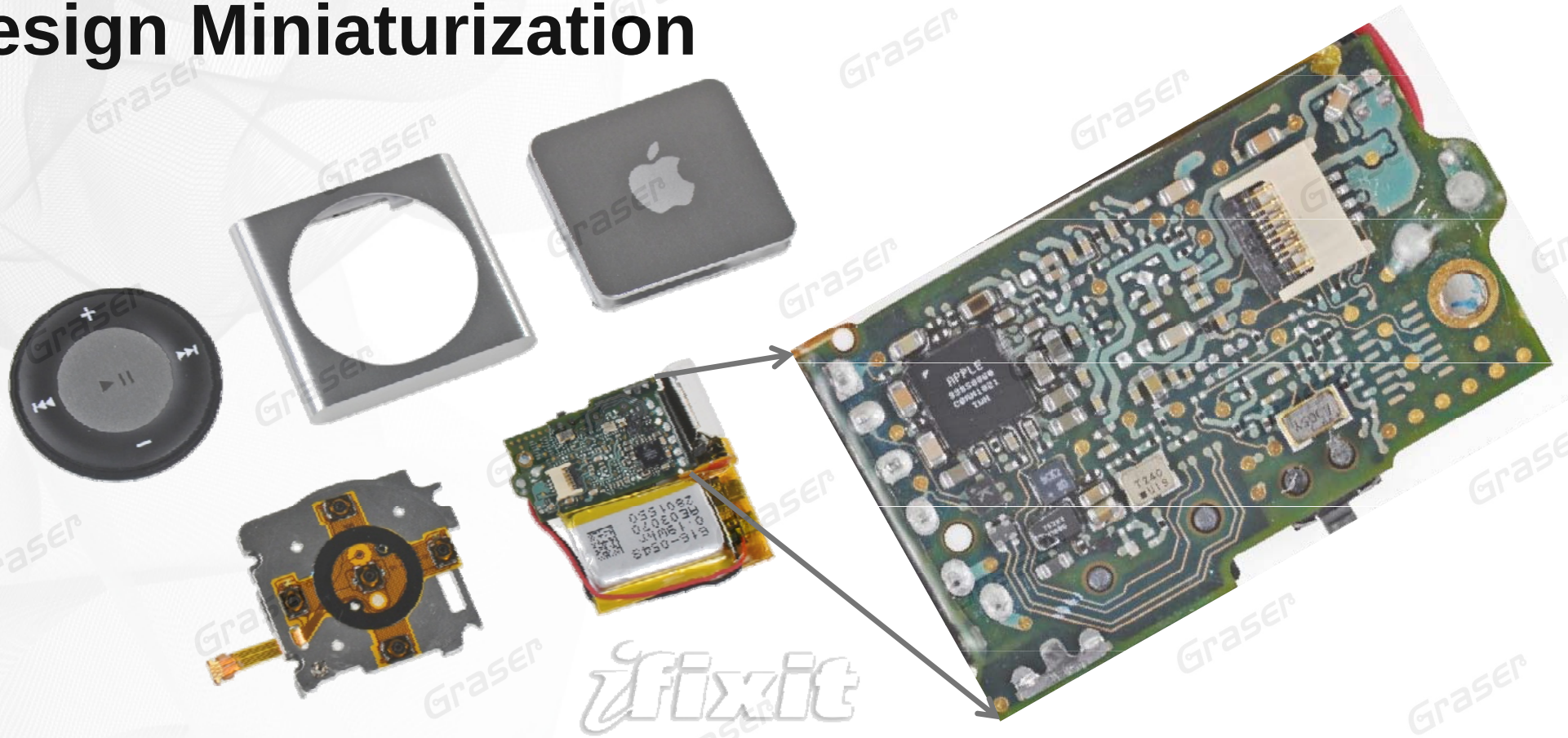
- Scribble Mode





Driving Design Density and Enclosure Integration

Design Miniaturization



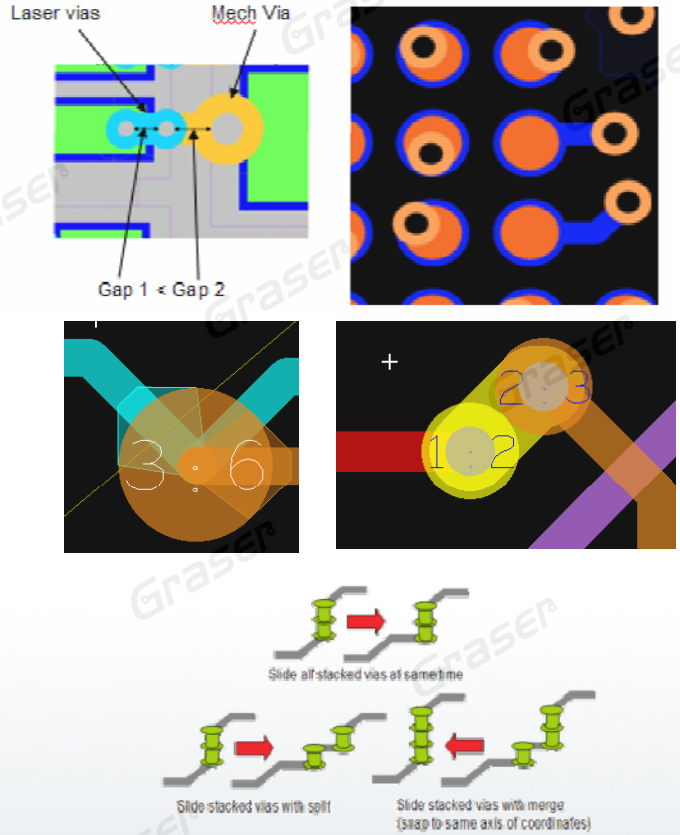
- Consumer, hand-held and body friendly products use flex-rigid to maximize form factor and functional density
- Drives design team with new challenges
  - Flex circuit co-designed with rigid circuit
  - Embedded components
  - New rules and constraints

Allegro ® Miniaturization

Miniaturization Option

Shortens the PCB design cycle by enabling a constraint-driven HDI design flow for designs using build-up and micro-via technology
Improves design cycle predictability and ensures manufacturing rules compliance improving yield

- Includes:
  - HDI Design Functionality
    - Micro-via object and associated spacing rules
    - Micro-via stacking rules, via use rules
    - Micro-via etch editing functionality
    - Single click multiple micro-via instantiation
    - Dynamic fileting, via line fattening, trace fileting
    - Contour hug w/multi-line routing for Flex designs
    - Unused micro-via removal utility
  - Embedded Components
  - Advanced Rigid-Flex Design Capabilities



Advanced Miniaturization Support

Evaluation of EDA Tools Embedded Capabilities by HERMES – a European Consortium focused on miniaturization using embedded components

Functionality for EC (Embedded Component)	Cadence	Vendor 2	Vendor 3	Vendor 4
EC placement between Cu layers				
EC pads available for via interconnect		N/A	N/A	
EC with pads on top & bottom sides				
Possibility to flip and/or rotate each EC separately				
Component span over several Cu layers				
Additional layers for EC assembly, adhesive pads, cavities				
Via-in-pad technology				
Filled/stacked via support for sequential build-up				
Separate assembly output for EC				
ODB++ support for EC				
Gerber/Excellon support for EC				

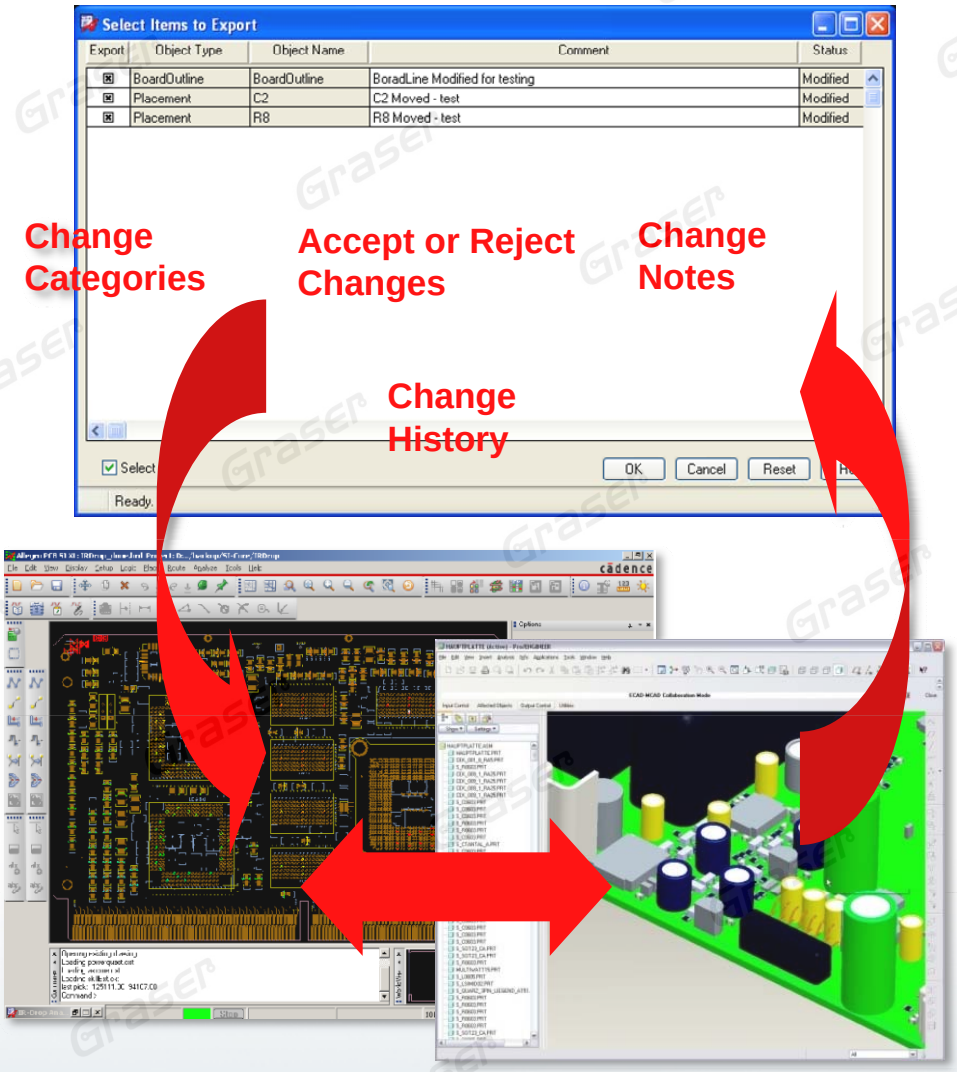
Supported
Work-around
Planned in the next release
Not supported

Figure 2 – Support of functionalities for embedded components for various CAD tools.

ECAD-MCAD Co-Design

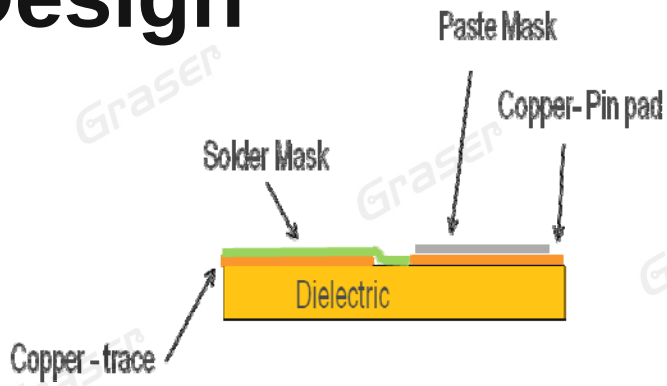
ECO/ECR incremental design

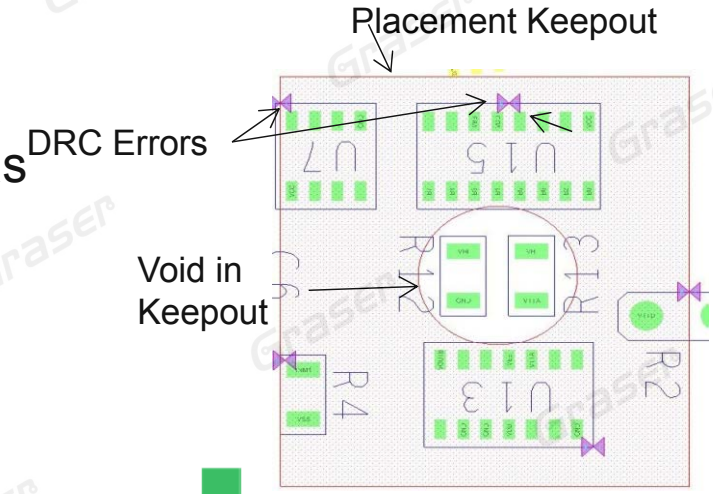
- Standard Based Approach
  - Incremental design data exchange
  - Ability to accept/reject
- Supported by PTC Creo, Siemens NX and Dassault SolidWorks

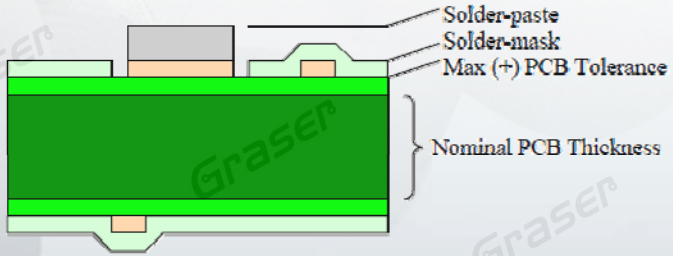


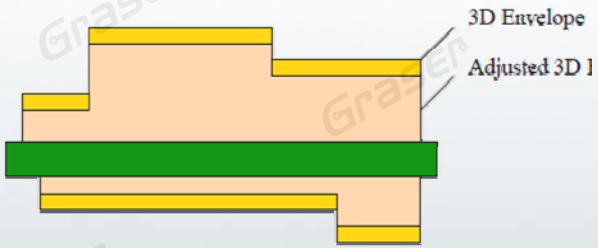
Streamlining ECAD-MCAD Co-Design Advanced Design Support

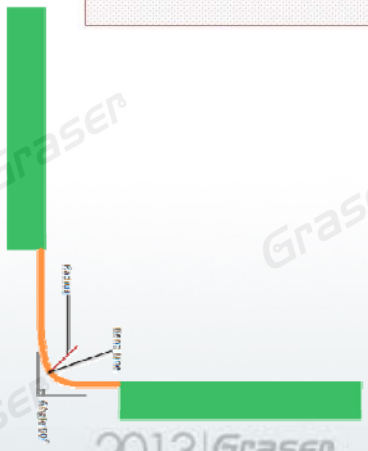
- Exchange user defined layers
  - Mask Layers, Adhesive areas, Silkscreen
- DRC checks for voids in keep-outs
  - Route, Placement, Via and Test probe
- Prevent putting components and vias in Flex bend areas
  - Convert bend area to Via Keepout / Package Keepout
  - Bend Line is the reference only within Allegro
- Board offset to represent true component heights
- Support for exporting etch to MCAD
  - Collaborate on selected set of nets
  - Export all cover layer copper for Thermal Analysis





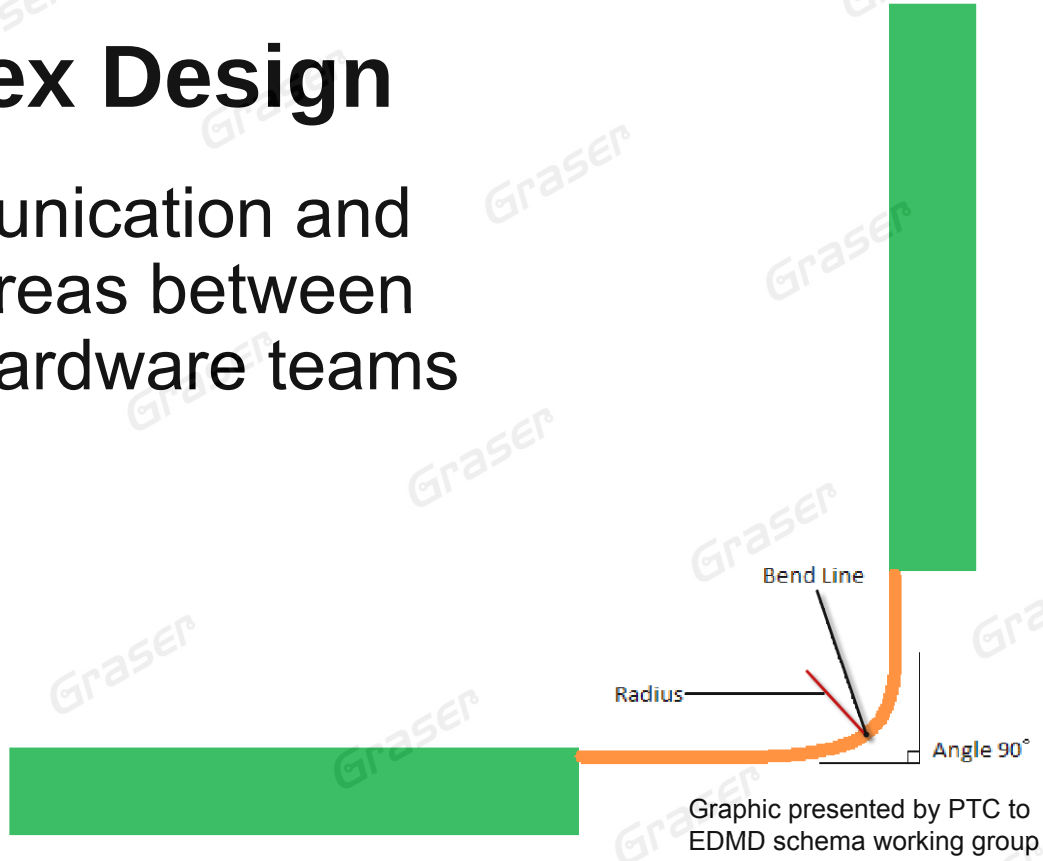




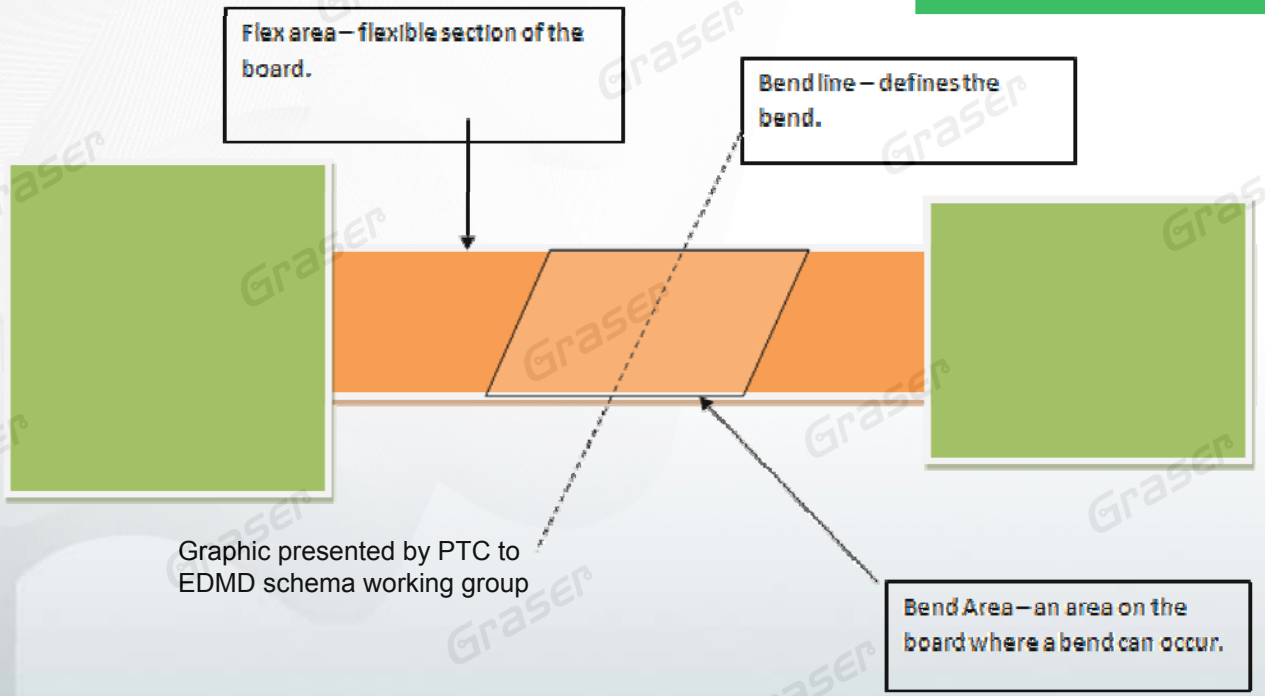


ECAD/MCAD Rigid-Flex Design

- Enable bi-directional communication and visualization of Flex bend areas between mechanical and electrical hardware teams



Graphic presented by PTC to EDMD schema working group

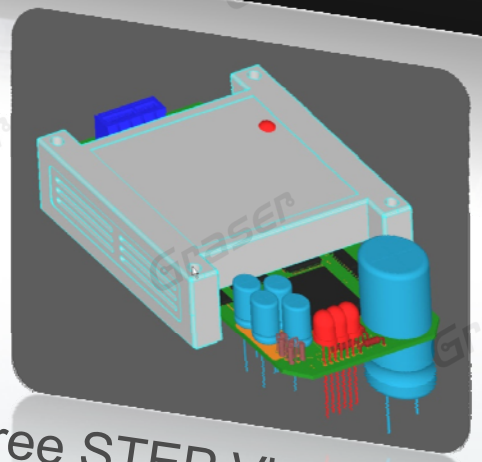


Graphic presented by PTC to EDMD schema working group

STEP Modeling and Viewing

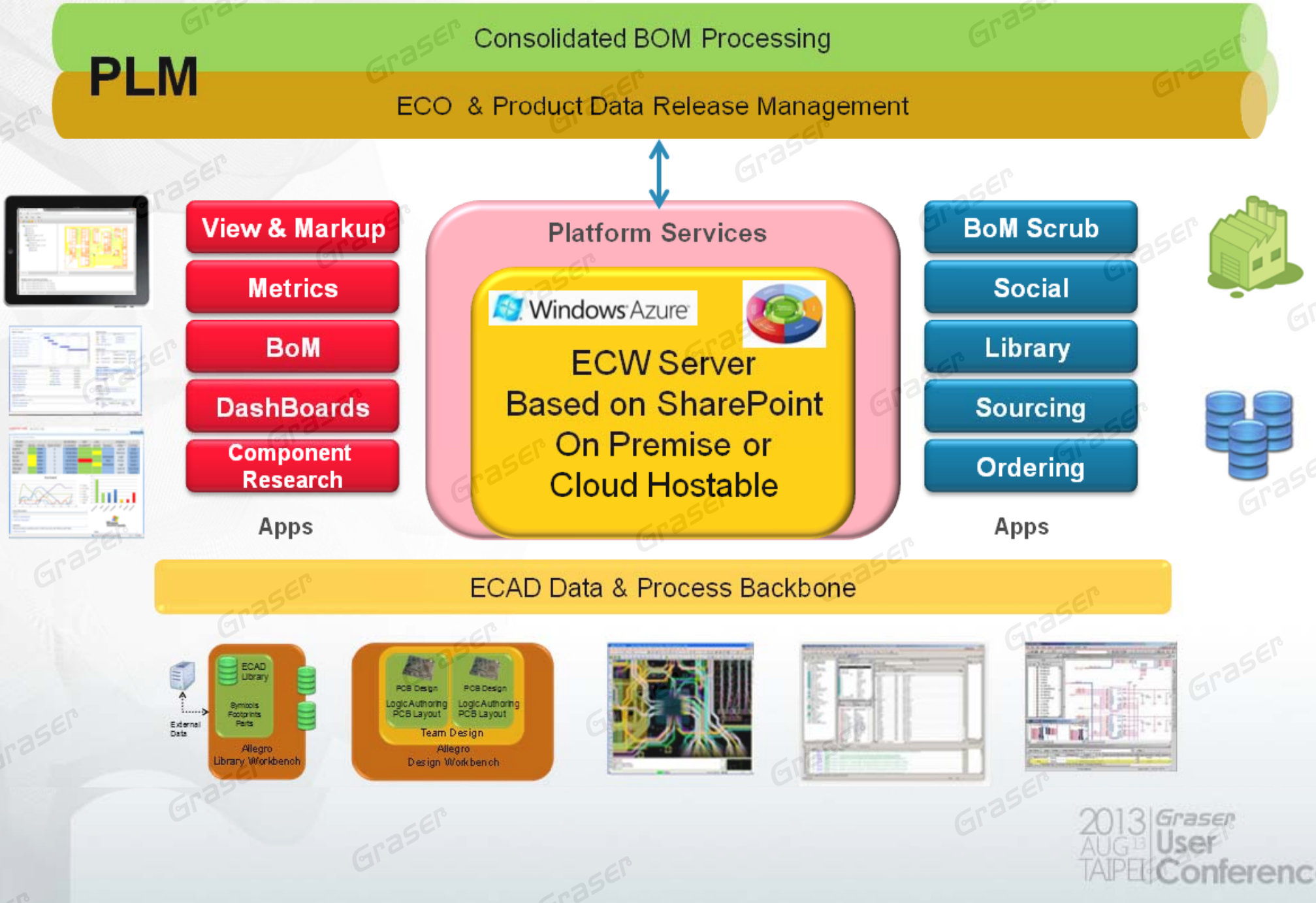
Bringing MCAD to ECAD

- Provide PCB designers with accurate visual 3D models of components
  - Aid placement, improve DFA
- Provide PCB designers with 3D models of mechanical enclosures
  - First-order “Does it fit?” analysis
- Provide MCAD team with accurate full 3D model of PCB and components
  - Detailed clash detection
- Provide customer documentation



Team Enabled Project Collaboration and Management

ECAD Collaboration Workbench

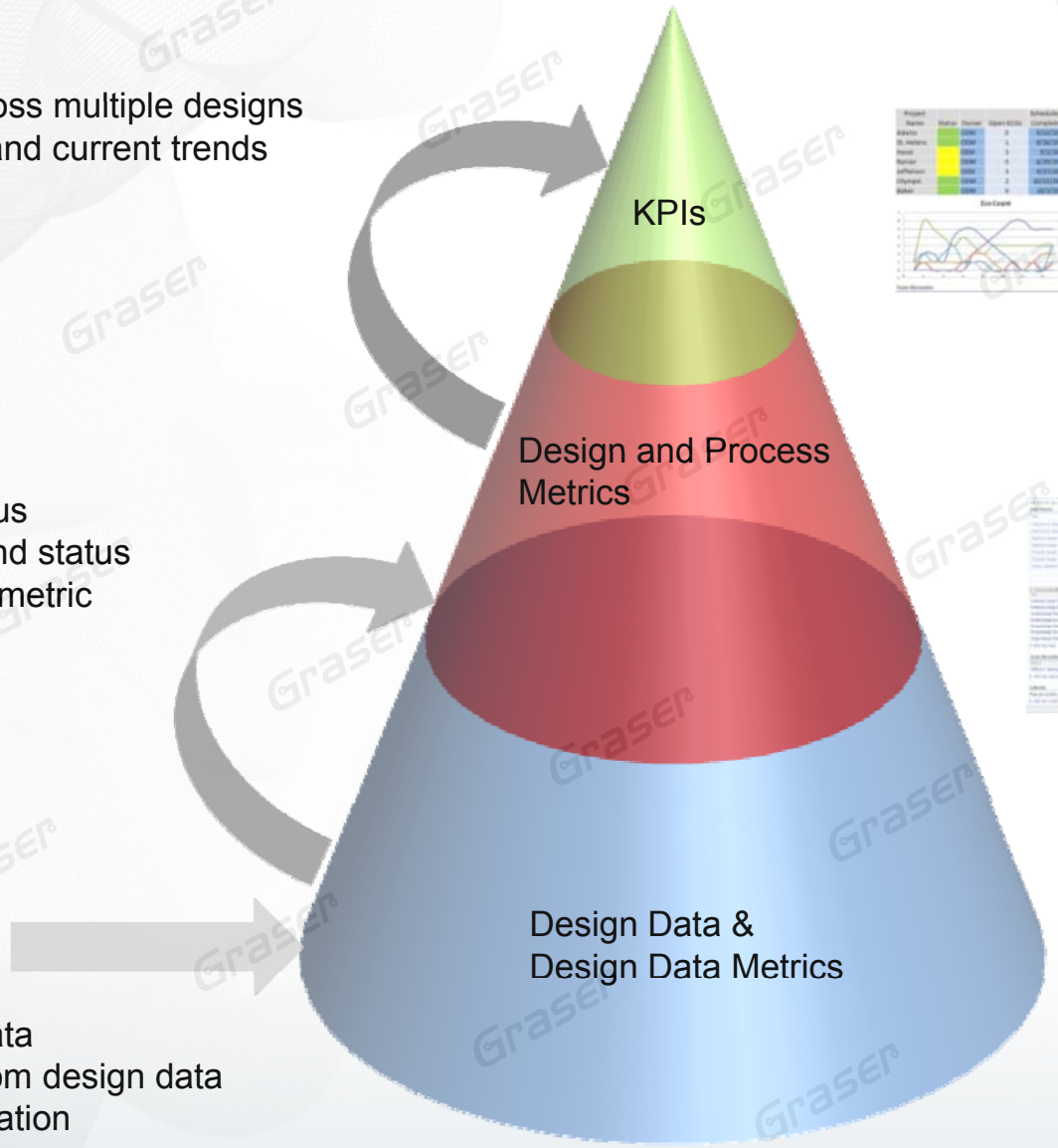


Collaboration with Management Visibility

Status across multiple designs
Historical and current trends

Overall Flow Status
ECO execution and status
Summary design metric information

Managed Design Data
Metrics extracted from design data
Process step information



Health of business

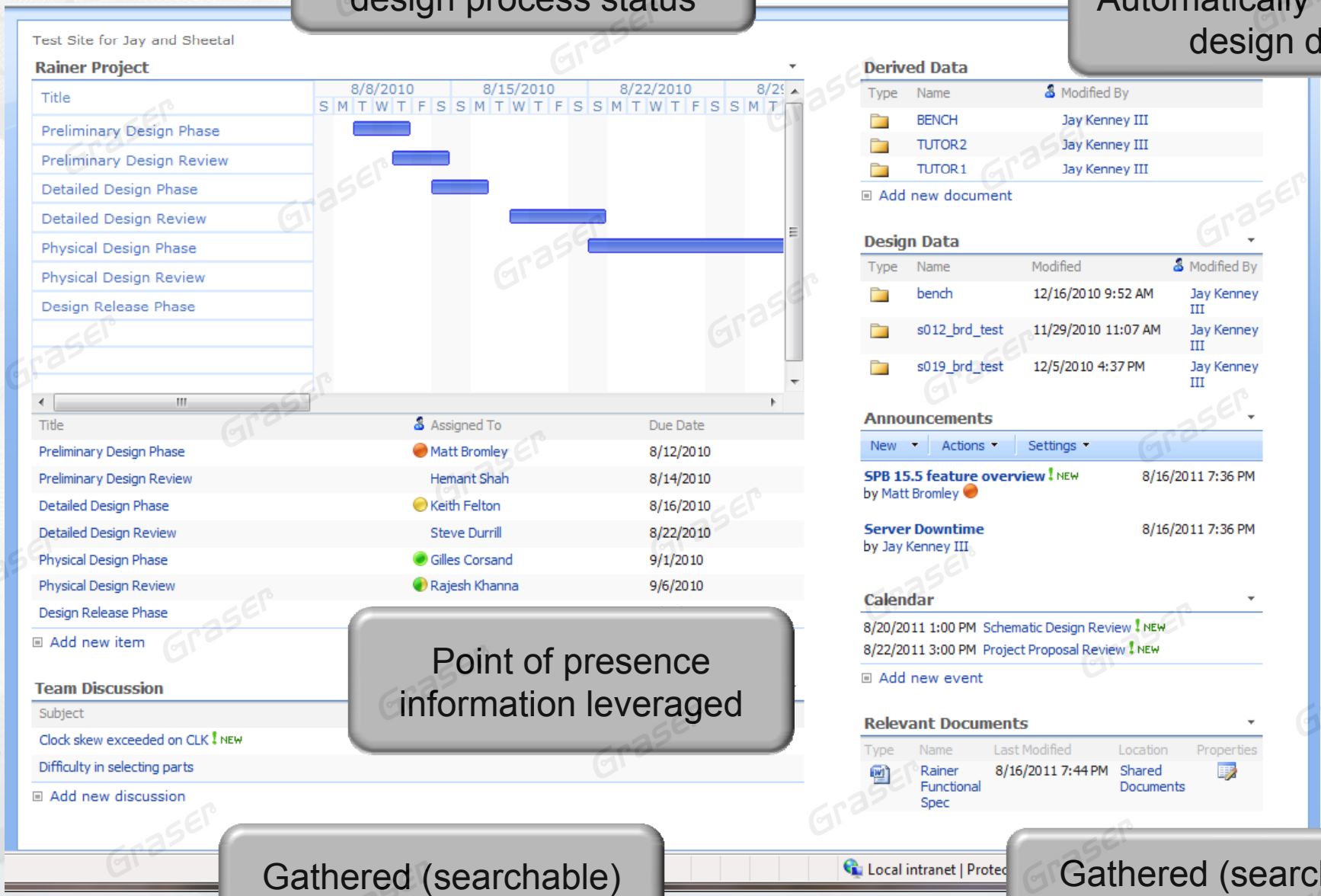
Project Status
Process Control
Change Analysis

Team Design
Access Control
Process Notification

Engineering / Project Manager's Dashboard

View of Engineer's design process status

Automatically uploaded design data



Point of presence information leveraged

Gathered (searchable) design discussions

Gathered (searchable) related design documents

Business Manager's Dashboard

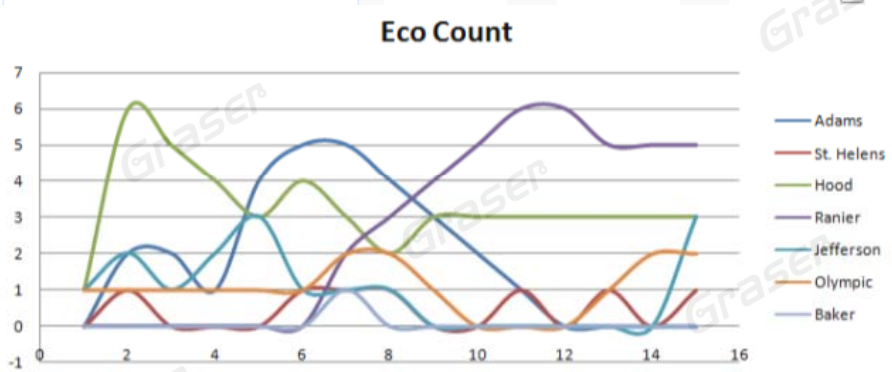
List of project and their status

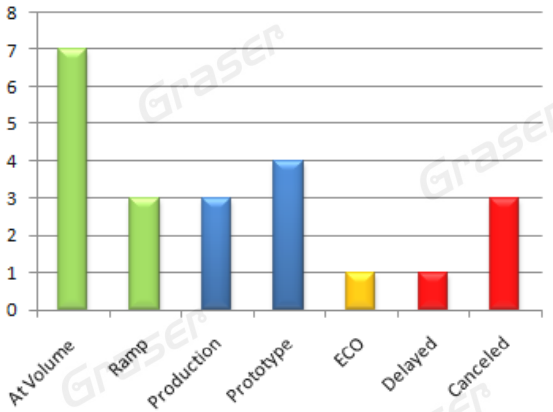
This Site: Demo for Jay

Site Actions

Test Site for Jay and Sheetal

Project Name	Status	Owner	Open ECOs	Scheduled Complete	Part Availabilit	Via Count	Reason	Process Step	Contact
Adams		ODM	0	9/12/2011				Layout	shah
St. Helens		ODM	1	8/26/2011				Review	felton
Hood		OEM	3	9/2/2011			Schedule	Logic	durrill
Ranier		ODM	5	8/29/2011			Part	Proto	lewis
Jefferson		OEM	3	9/27/2011			Schedule	Logic	bader
Olympic		ODM	2	10/23/2011				Layout	bromley
Baker		ODM	0	10/2/2011				Layout	charlie





Team Discussion

Subject

Difficulty in selecting parts

Add new discussion

Design quality Project Metrics

Design Production Status

Calendar

There are currently no upcoming events. To add a new event, click "Add new event" below.

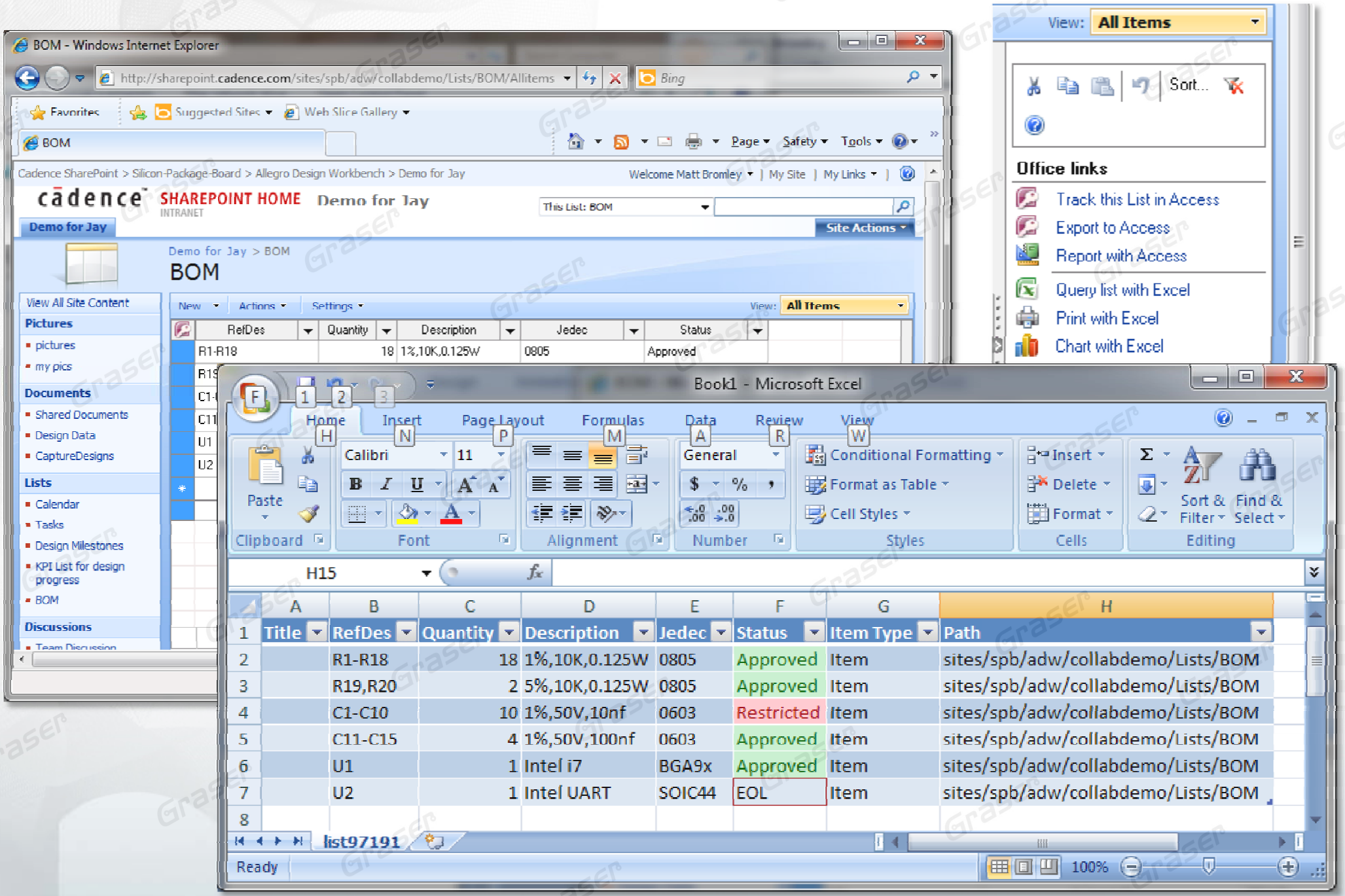
Add new event

Links

Local intranet | Protected Mode: Off

100%

BOM Management / Where Used

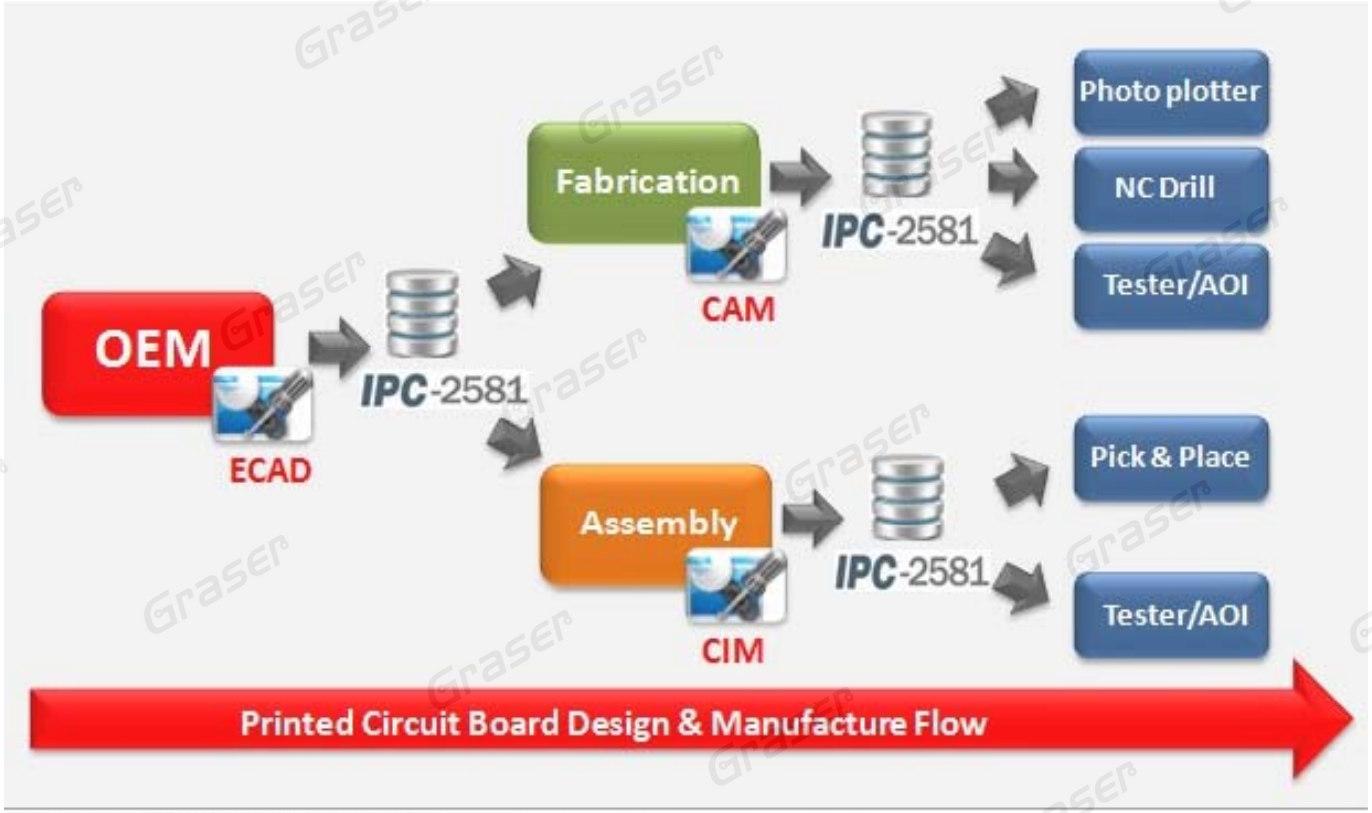


Title	RefDes	Quantity	Description	Jedec	Status	Item Type	Path
	R1-R18	18	1%,10K,0.125W	0805	Approved	Item	sites/spb/adw/collabdemo/Lists/BOM
	R19,R20	2	5%,10K,0.125W	0805	Approved	Item	sites/spb/adw/collabdemo/Lists/BOM
	C1-C10	10	1%,50V,10nf	0603	Restricted	Item	sites/spb/adw/collabdemo/Lists/BOM
	C11-C15	4	1%,50V,100nf	0603	Approved	Item	sites/spb/adw/collabdemo/Lists/BOM
	U1	1	Intel i7	BGA9x	Approved	Item	sites/spb/adw/collabdemo/Lists/BOM
	U2	1	Intel UART	SOIC44	EOL	Item	sites/spb/adw/collabdemo/Lists/BOM

Driving the Path to Manufacture

2013 AUG TAIPEI Graser User Conference

Open Single Path to Manufacturing



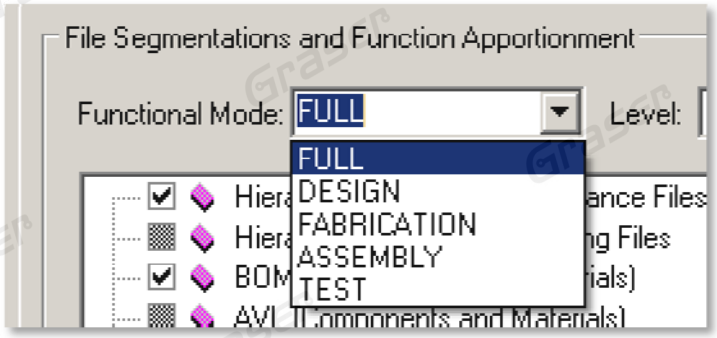
IPC-2581 CONSORTIUM
For an open, neutral global standard for efficient PCB design data transfer

Manufacturing Partner

Supply-chain adoption of IPC 2581 standard through global consortium:

- System Companies: Harris, Fujitsu, Ericsson, nVidia, Cisco, Qualcomm, Lockheed/ Martin
- EMS/ODMs: Sanmina-SCI, Vayo, Sedona International
- EDA: Cadence, Zuken, ADIVA, Downstream, WISE, Ucamco, Aegis, Polar Instruments, ScanCAD, Logicswap, Intercept, easylogix, Direct Logix, Siemens PLM

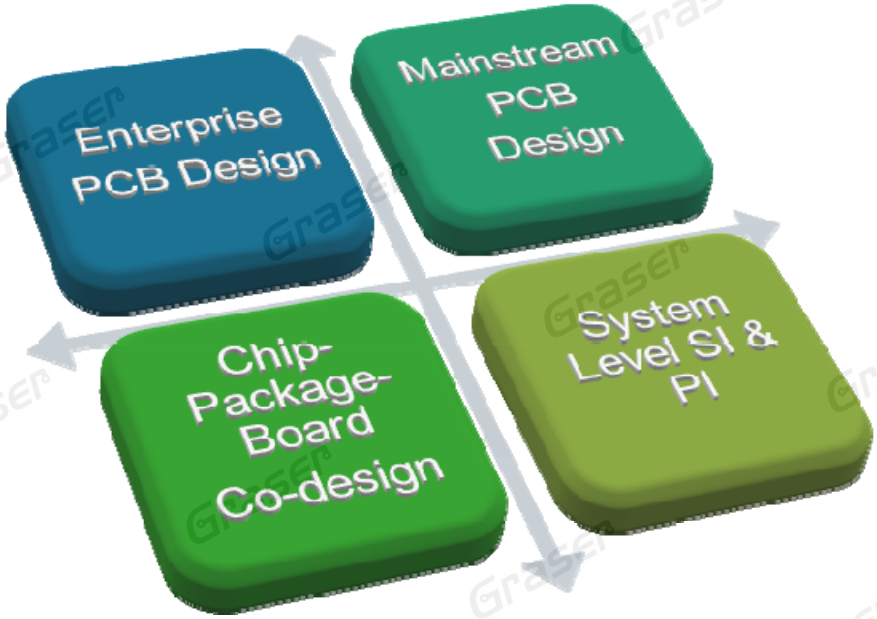
IPC-2581 Export

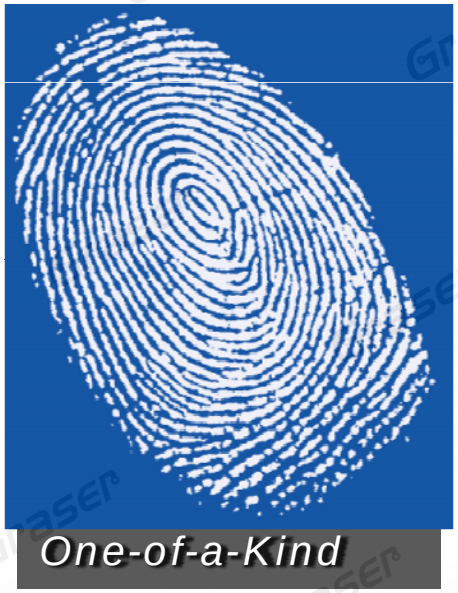


- 5 Export Functions/ 3 Levels Each
  - Each mode selects predefined output data
  - Each level selects sub-sets
- TEST
  - Export data related to test
  - Bareboard
  - In-circuit, impedance etc.
- Assembly
  - BOM, External circuit data
  - AVL with substitution
- Fabrication
  - Layer data
  - Materials and stack up
- Design
  - Each mode selects predefined output data
  - Each level selects sub-sets
- Full
- Exported Data can be selected individually

Summary

- Constraint Driven Flow delivers shorter and more Predictable design cycles
- Constraint-driven PCB layout with unmatched breadth and depth of constraints eliminates unnecessary prototype iterations
- Unmatched Integrated Signal & Power Integrity Simulation Solutions
- Available in cost effective and scalable efficient solutions to meet your needs



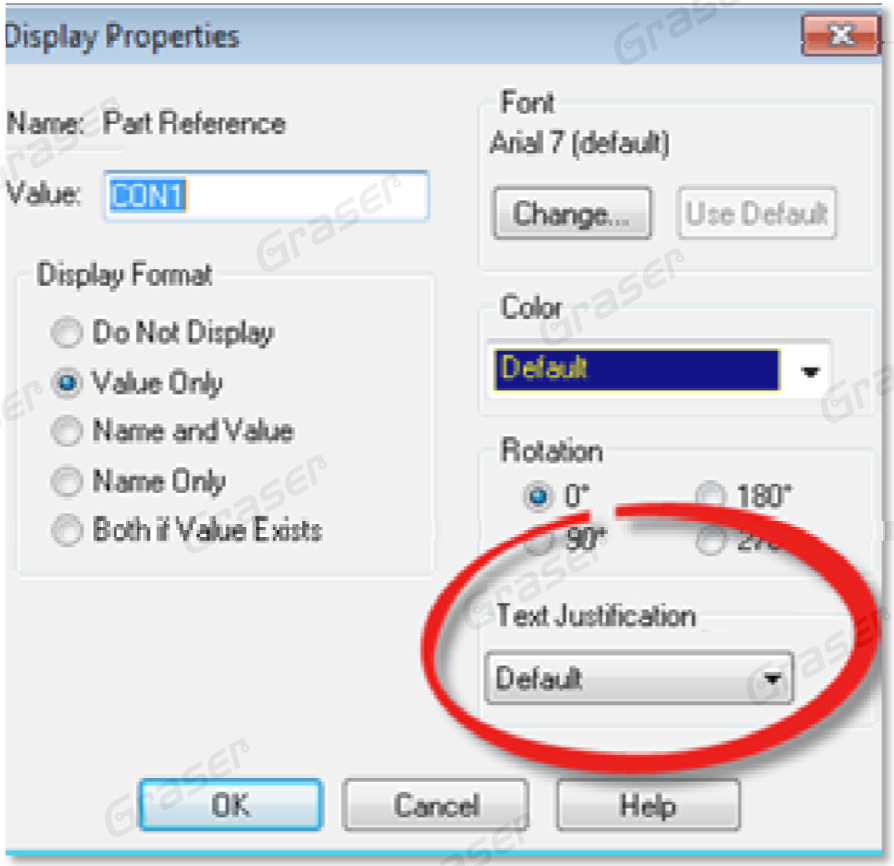


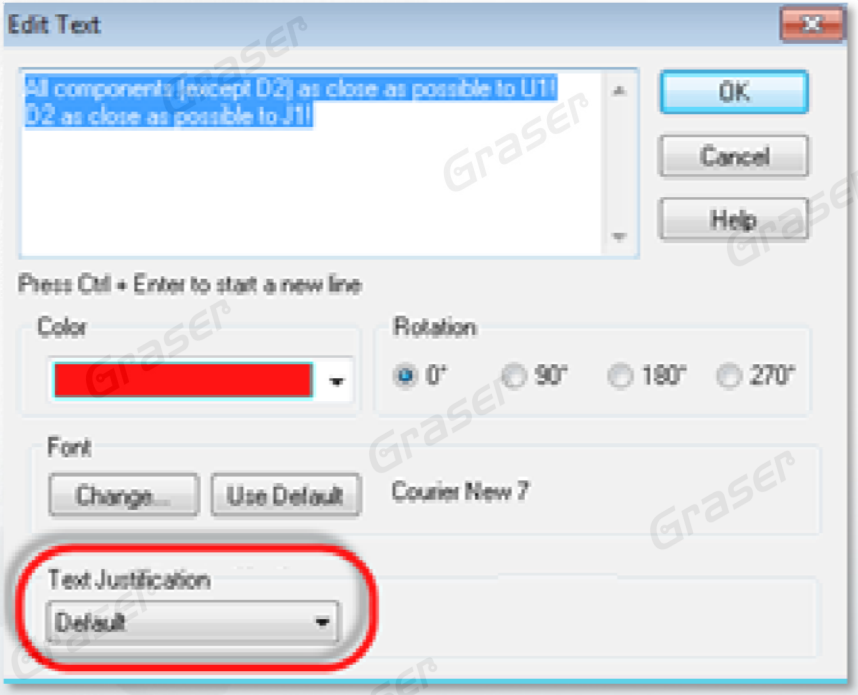
What's New in 16.6 HotFix

2013 AUG TAIPEI Graser User Conference

OrCAD Capture Text Justification

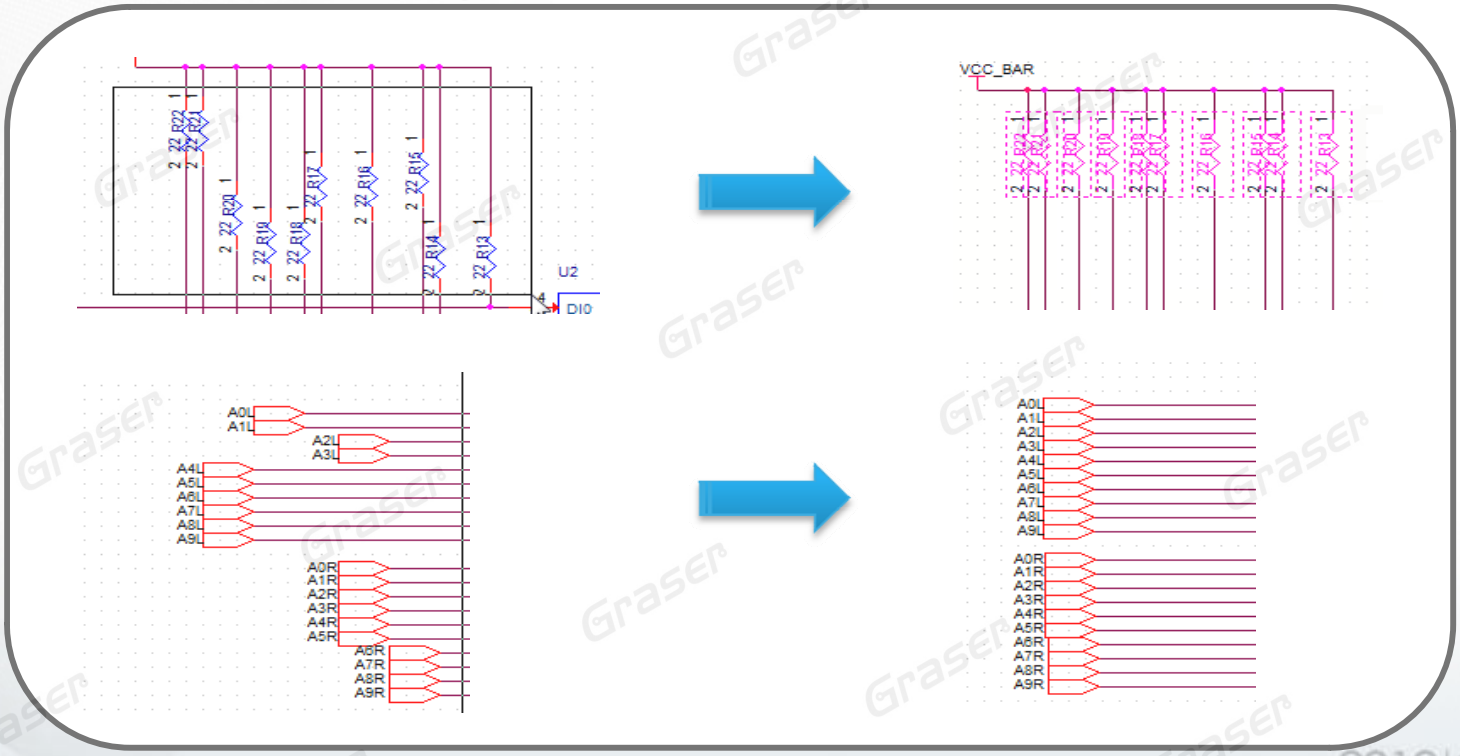
- Property Text
  - Display properties
- Text Objects
  - Edit text





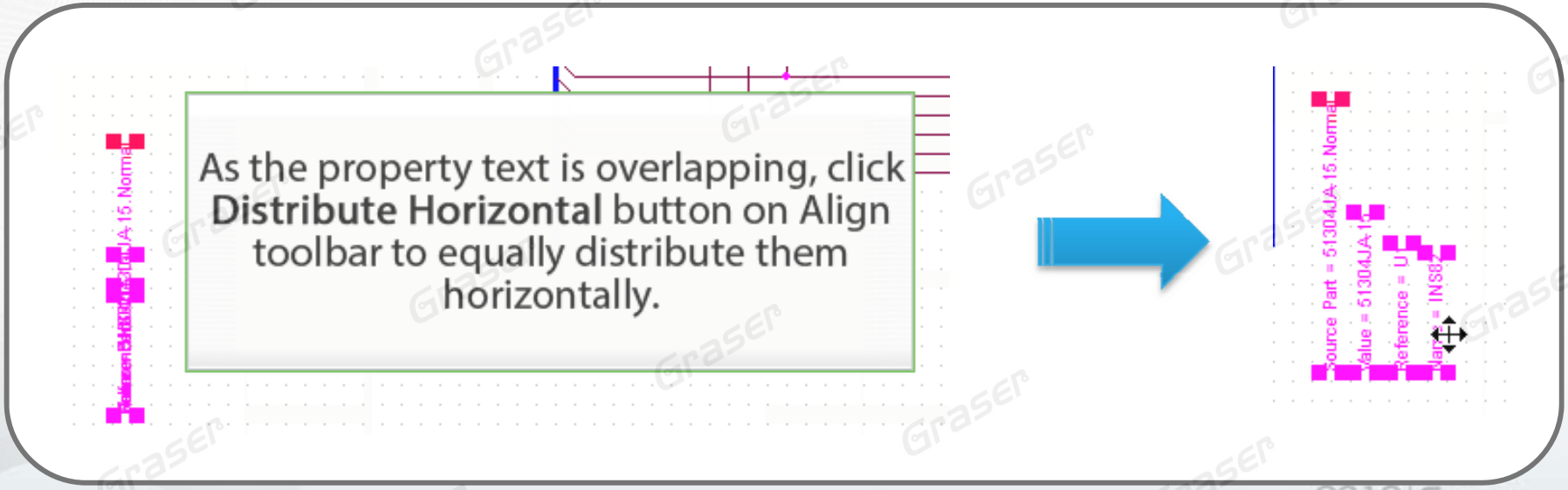
Object Alignment

- Select and Align objects on schematic
  - Horizontal Alignment – left, right or center
  - Vertical Alignment – top, bottom or center



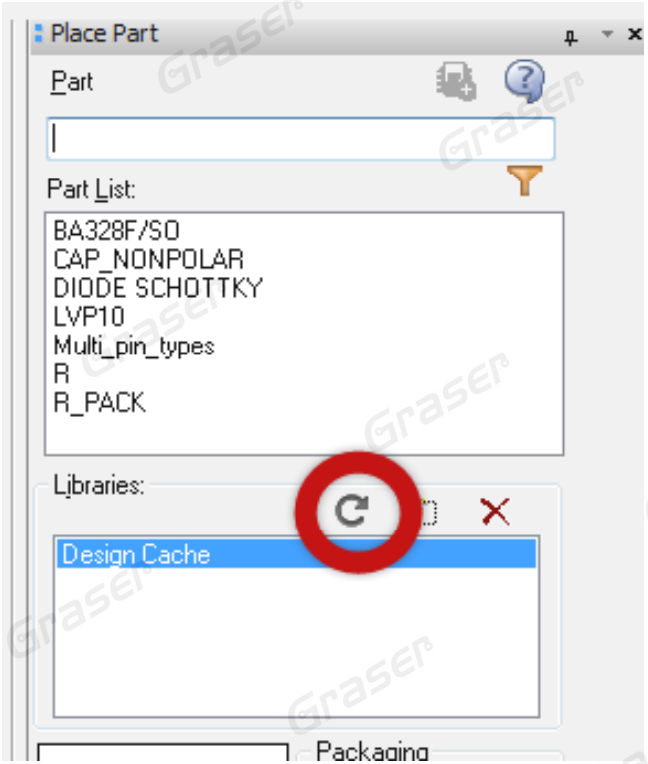
Object Distribution

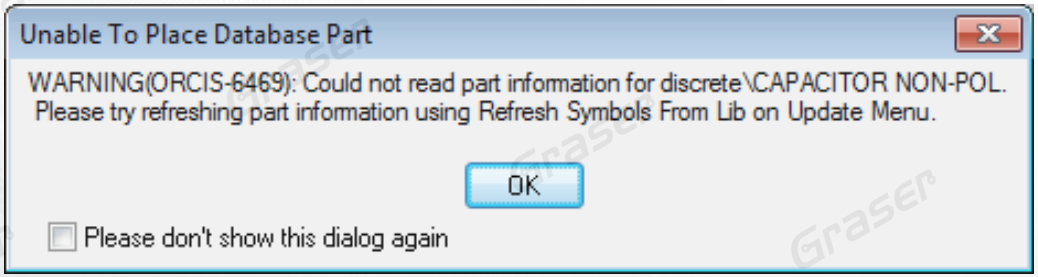
- Select objects and evenly distribute horizontally or vertically
- Mouse mode to select the point(s) of reference for alignment or distribution

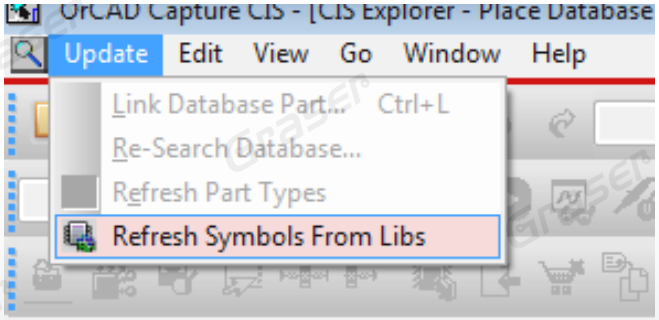


Library Refresh

- Provides Library Reload without exiting Capture/CIS
- User can reload libraries without exiting session when faced with "Unexpected error in database access"

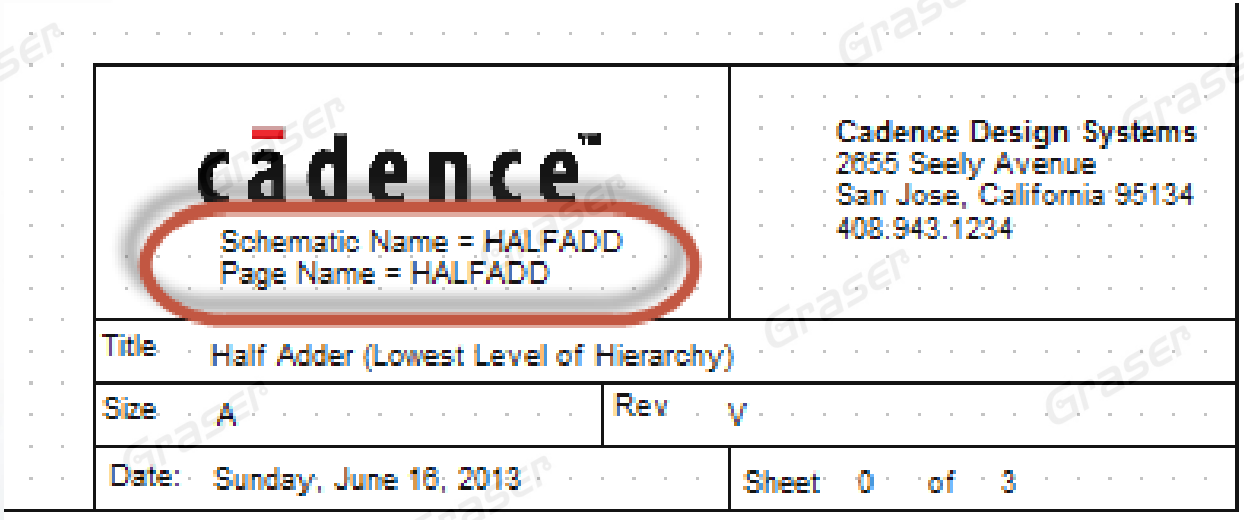






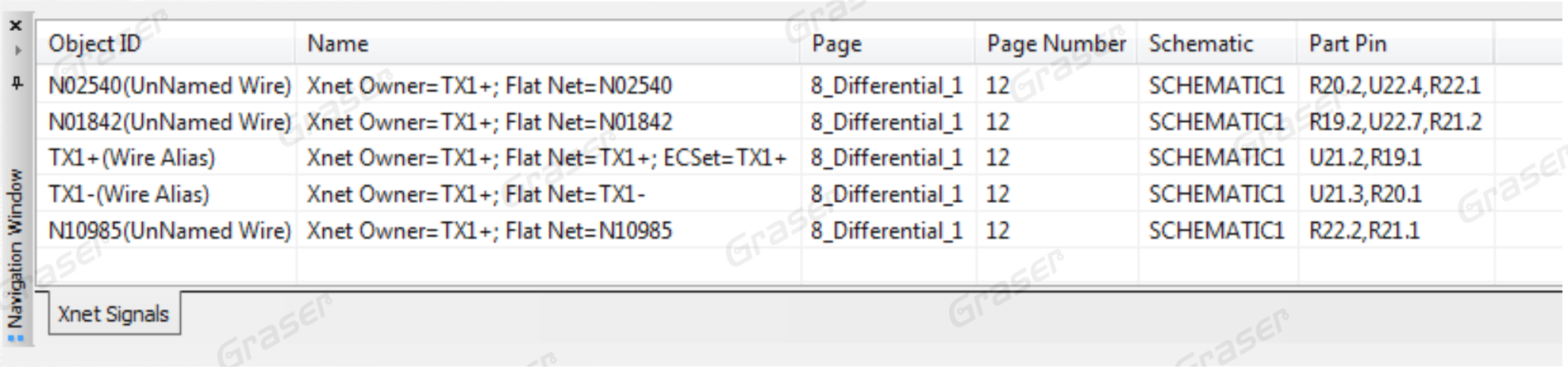
Title-block Property

- Schematic / page name available as property
- Name property in title block kept in synch with schematic page name
  - No longer need to manually add and update page name property on all pages



Xnet Query View

- All Xnets can be viewed for components and flat net members



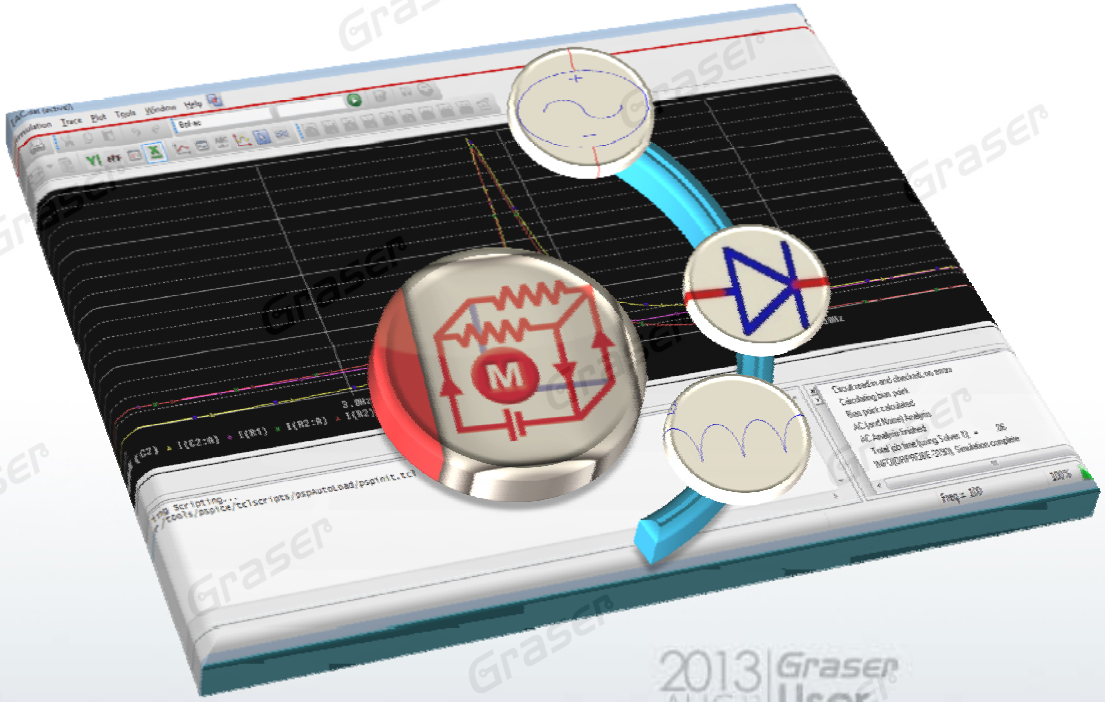
Navigation Window

Object ID	Name	Page	Page Number	Schematic	Part Pin
N02540(UnNamed Wire)	Xnet Owner=TX1+; Flat Net=N02540	8_Differential_1	12	SCHEMATIC1	R20.2,U22.4,R22.1
N01842(UnNamed Wire)	Xnet Owner=TX1+; Flat Net=N01842	8_Differential_1	12	SCHEMATIC1	R19.2,U22.7,R21.2
TX1+(Wire Alias)	Xnet Owner=TX1+; Flat Net=TX1+; ECSet=TX1+	8_Differential_1	12	SCHEMATIC1	U21.2,R19.1
TX1-(Wire Alias)	Xnet Owner=TX1+; Flat Net=TX1-	8_Differential_1	12	SCHEMATIC1	U21.3,R20.1
N10985(UnNamed Wire)	Xnet Owner=TX1+; Flat Net=N10985	8_Differential_1	12	SCHEMATIC1	R22.2,R21.1

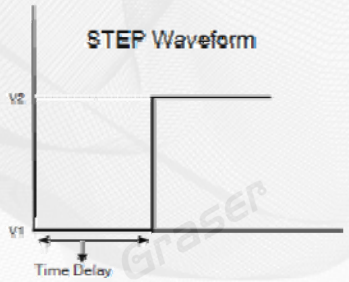
Xnet Signals

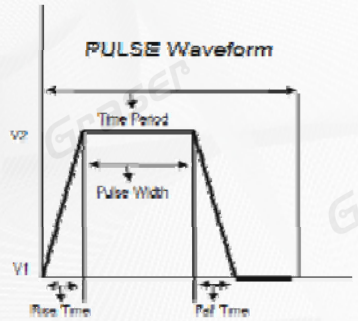
PSpice Modeling Apps

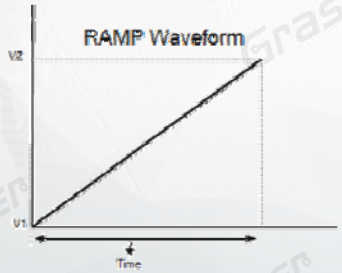
- New productivity applications for PSpice simulation
  - Independent Sources
  - Zener Diode
  - RF Inductor
- Parameter-driven dialog to automatically create symbol and model
- Parameters editable on the fly

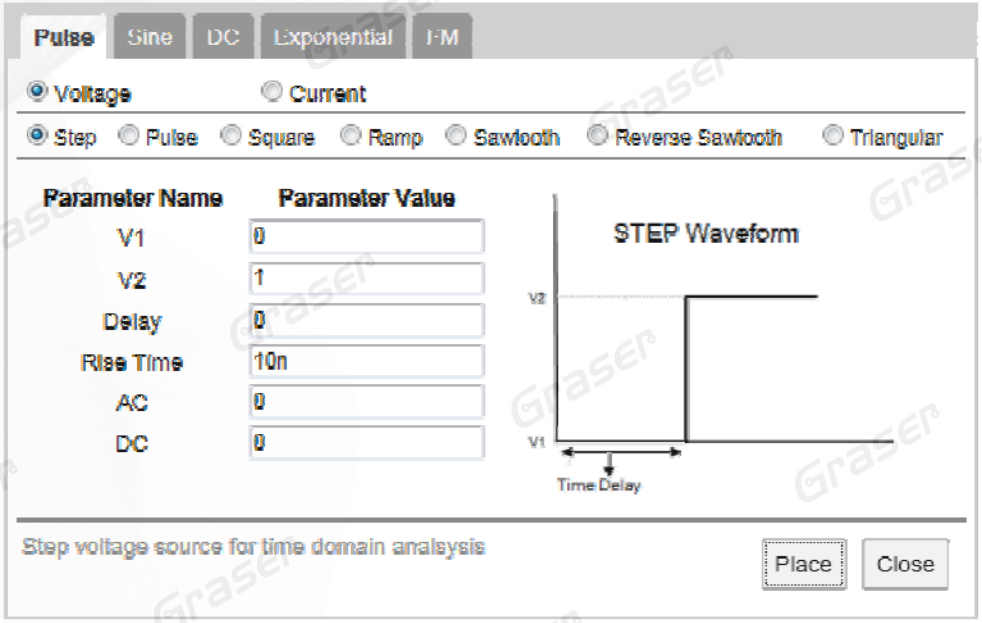


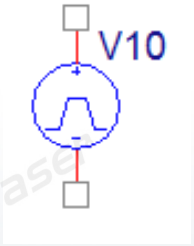
Pulse Generator

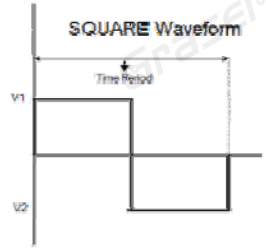


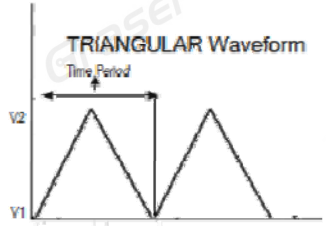


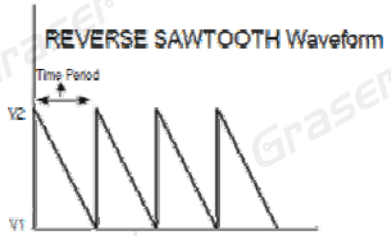


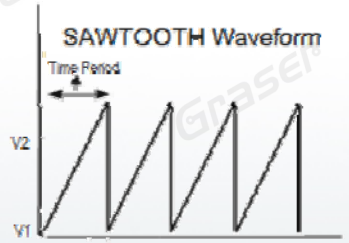




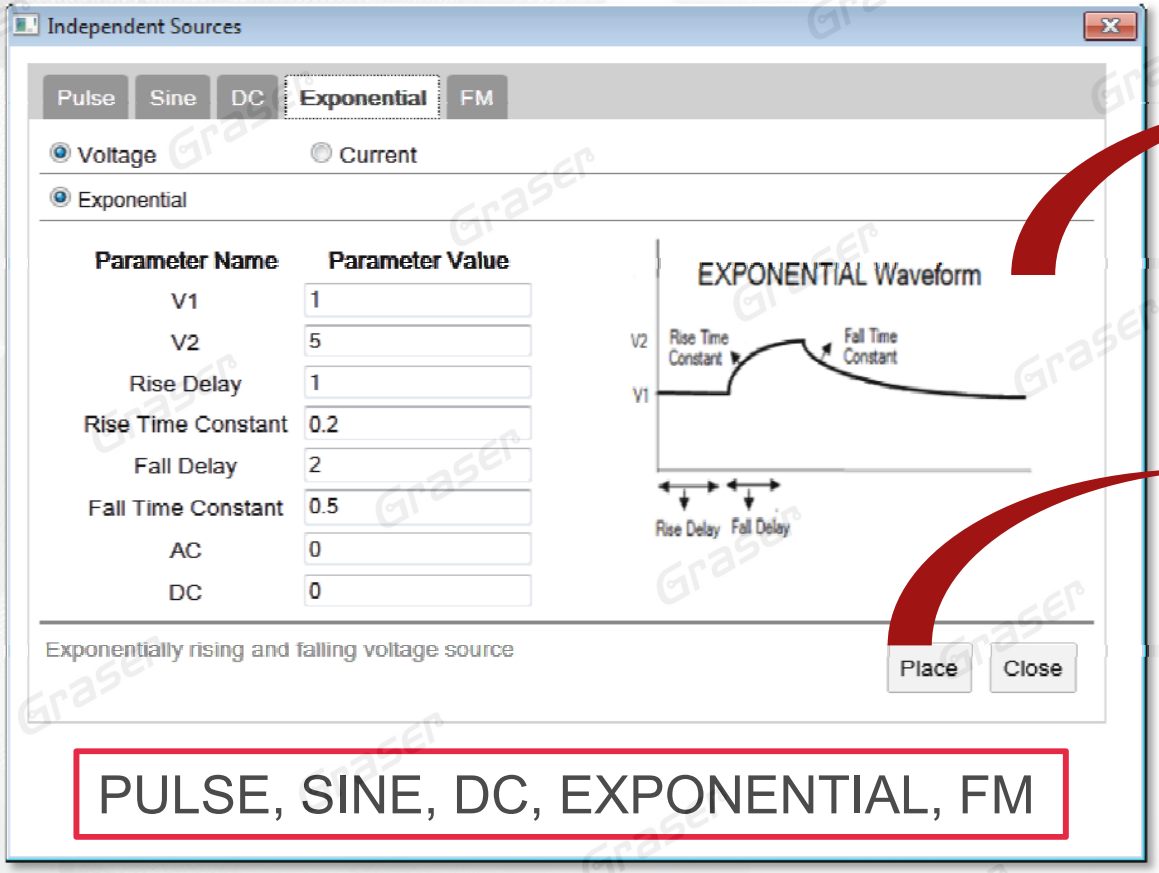








PSpice Modeling App
Independent Sources

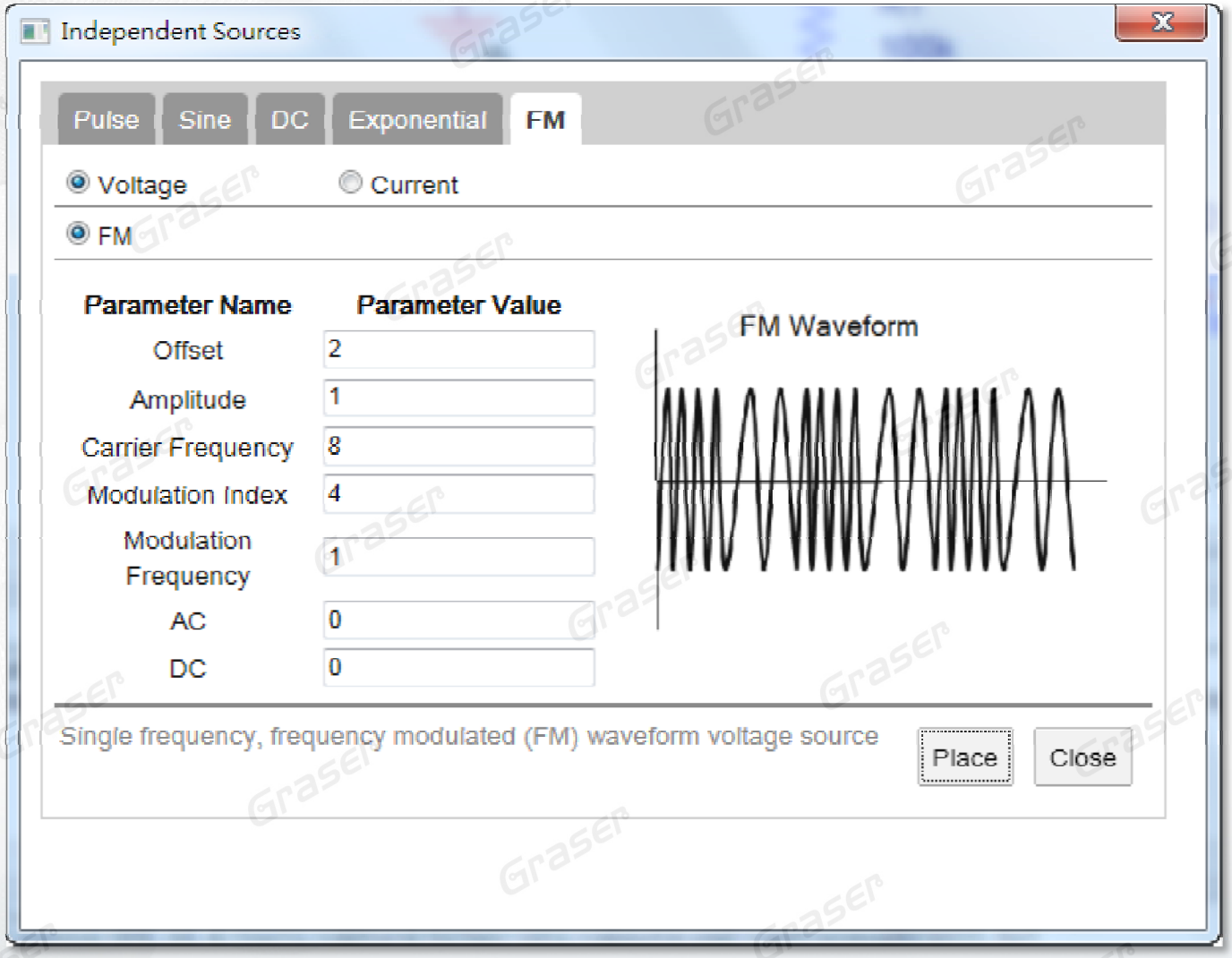


PULSE, SINE, DC, EXPONENTIAL, FM

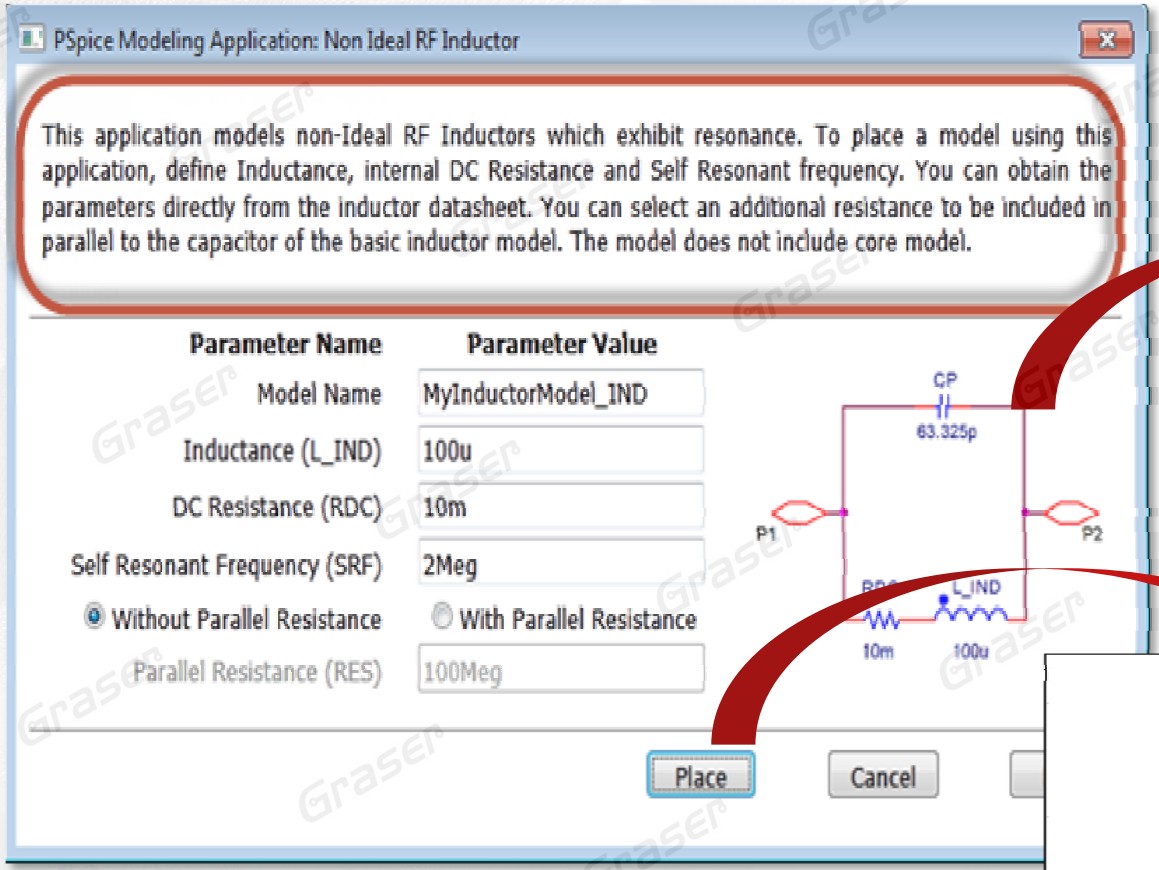
	A
	Example : PAGE1 : V
AC	0
Color	Default
DC	0
Designator	
FT	Exponential$Voltage$0
Graphic	VEXP.Normal
ID	
Implementation	
Implementation Path	
Implementation Type	PSpice Model
Location X-Coordinate	660
Location Y-Coordinate	160
Name	INS5057
Part Reference	V4
Footprint	
Power Pins Visible	
	DEFAULT
PSpiceOnly	TRUE
PSpiceTemplate	V^@REFDES %+ %- ?DC
Reference	V4
Source Library	D:\SPB166\TOOLS\CA
Source Package	VEXP
Source Part	VEXP.Normal
TC1	0.2
TC2	0.5
TD1	1
TD2	2
V1	1
	5
	VEXP

V1 = 1
V2 = 5
TD1 = 1
TC1 = 0.2
TD2 = 2
TC2 = 0.5

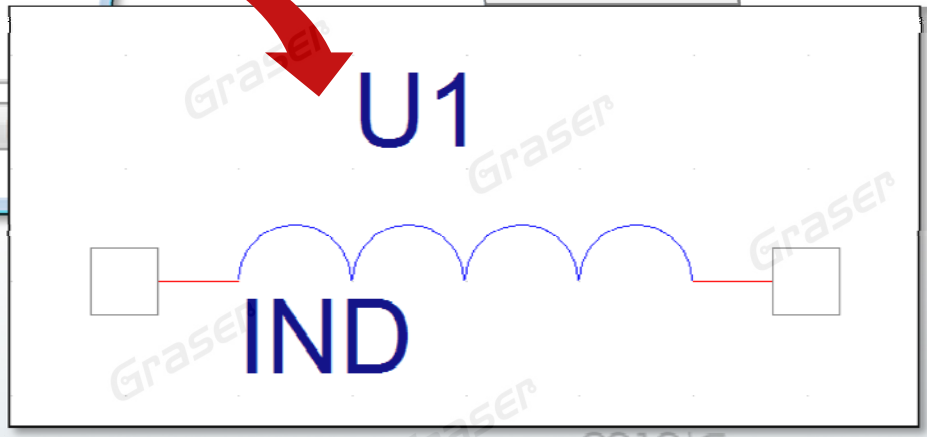
FM Waveform Generator



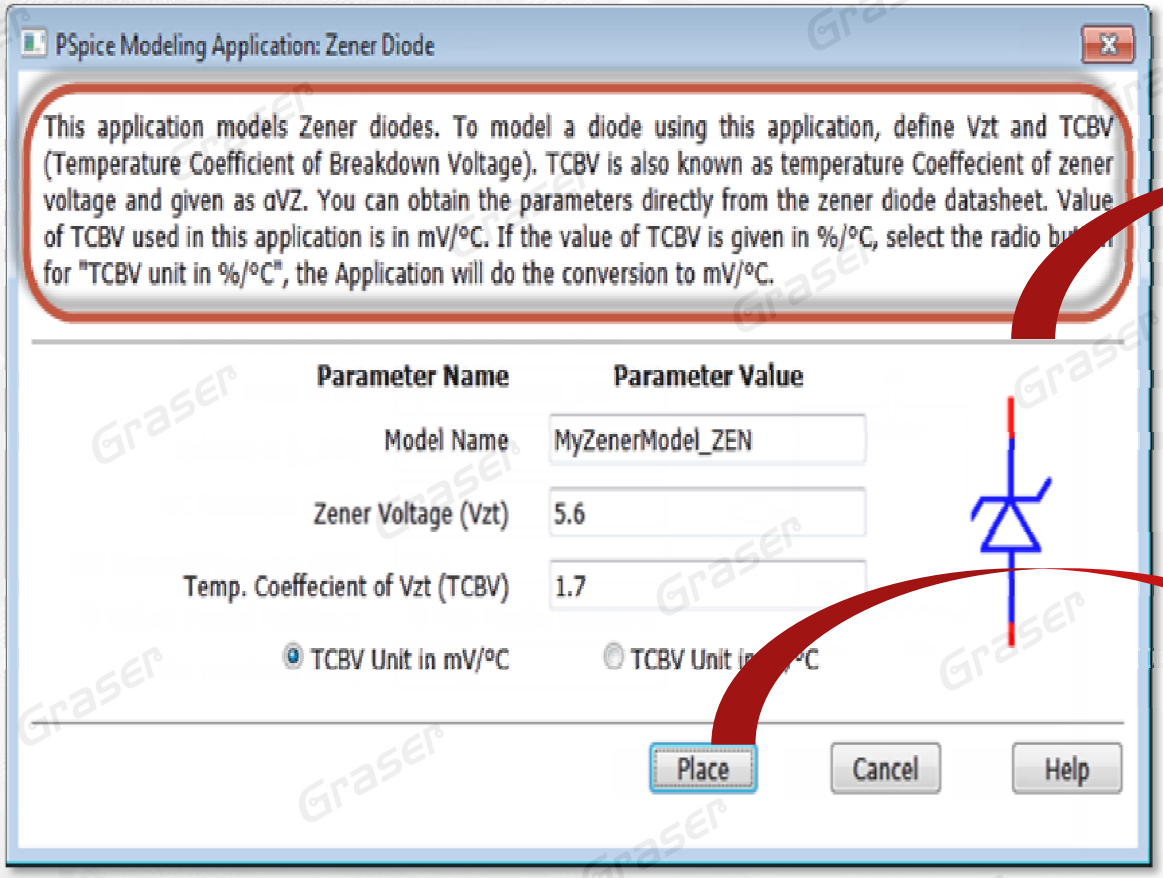
PSpice Modeling App
RF Inductor



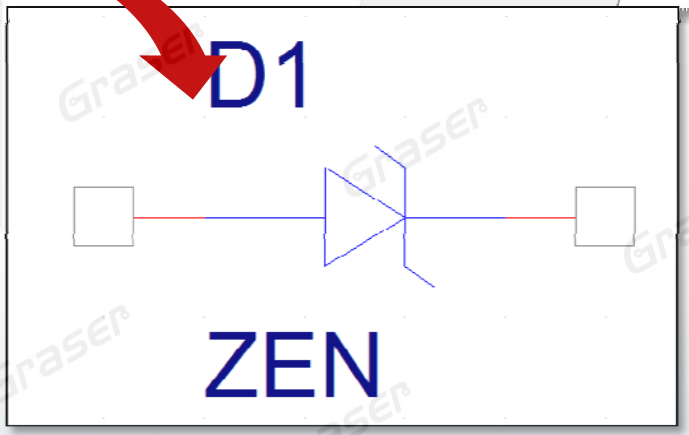
	A
	Example : PAGE1 : U1
Color	Default
Designator	
Graphic	IND.Normal
ID	
Implementation	MyInductorModel_IND1
Implementation Path	
Implementation Type	PSpice Model
Location X-Coordinate	610
Location Y-Coordinate	150
Name	INS5126
Part Reference	U1
PCB Footprint	
Pins Visible	
itive	DEFAULT
gAppType	Inductor
PSpiceTemplate	X^@REFDES %1 %2 @MO
Reference	U1
Source Library	D:\SPB166\TOOLS\CA
Source Package	IND
Source Part	IND.Normal
Value	IND



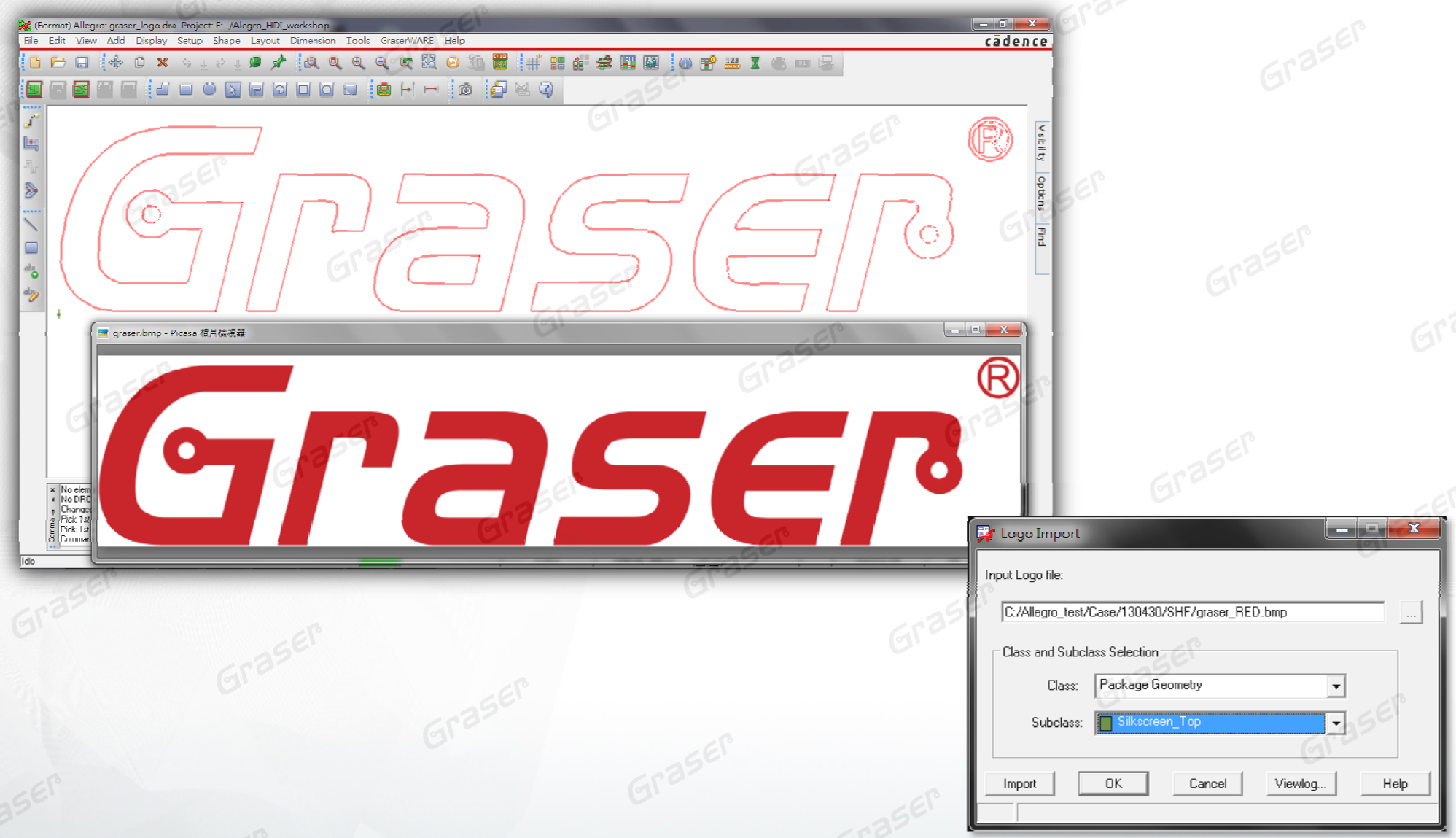
PSpice Modeling App
Zener Diode



	A
	Example : PAGE1 : D1
Color	Default
Designator	
Graphic	ZEN.Normal
ID	
Implementation	MyZenerModel_ZEN1
Implementation Path	
Implementation Type	PSpice Model
Location X-Coordinate	670
Location Y-Coordinate	170
Name	INS5151
Part Reference	D1
PCB Footprint	
r Pins Visible	
itive	DEFAULT
PSpiceM gAppType	Zener
PSpiceTemplate	X^@REFDES %AN %CAT
RCA	DEF
Reference	D1
Source Library	D:\SPB166\TOOLS\CA
Source Package	ZEN
Source Part	ZEN.Normal
STATE	ON
TOL_ON_OFF	ON
Value	ZEN



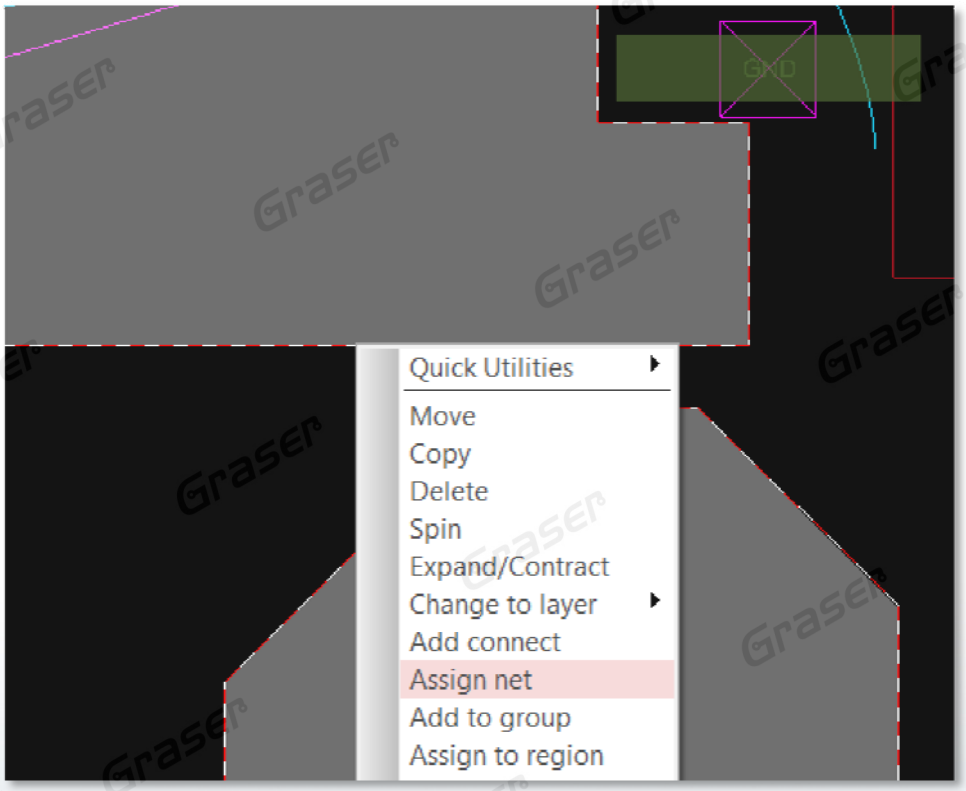
Logo Import



Net Assignment to Multiple Shapes

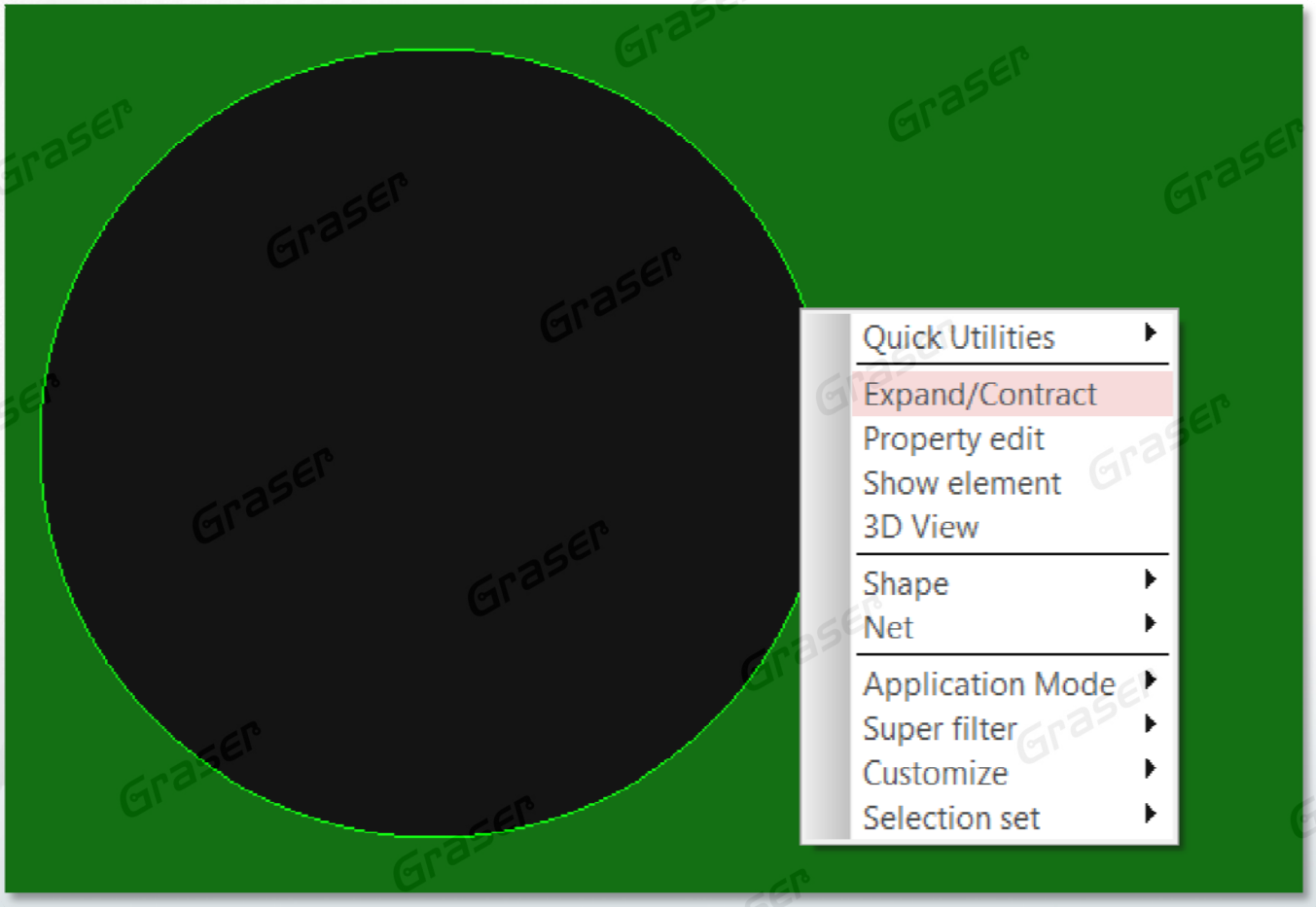
- Until now, the assignment of a net is limited to a single selected shape.

- Using “General Edit” or “Etch Edit” Application Modes, one can now pre-select multiple shapes then use the RMB context sensitive “Assign Net” command.



Expand/Contract Voids in Shapes

- Initial functionality targeted at shape boundary delivered in16.6
- Requires boundary subclass to be visible

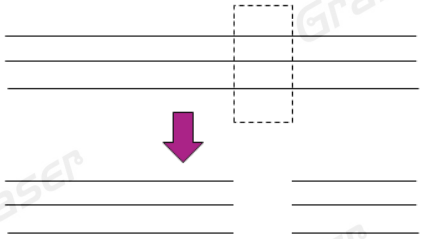


Drafting Enhancements

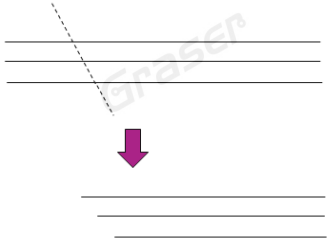
For customers who create advanced manufacturing / documentation package for their PCB designs

Shortens time to create documentation package

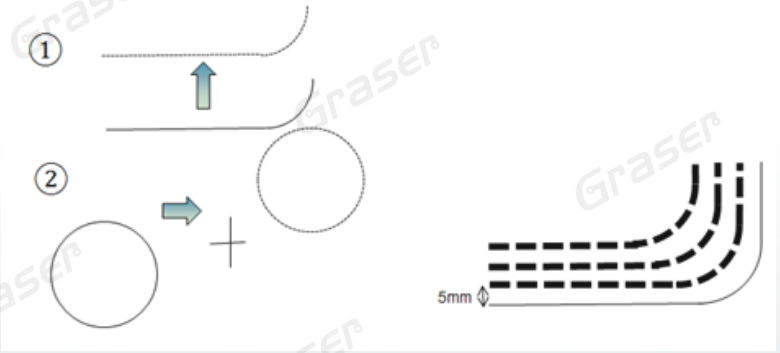
- Cut by area
  - Delete line segments inside area



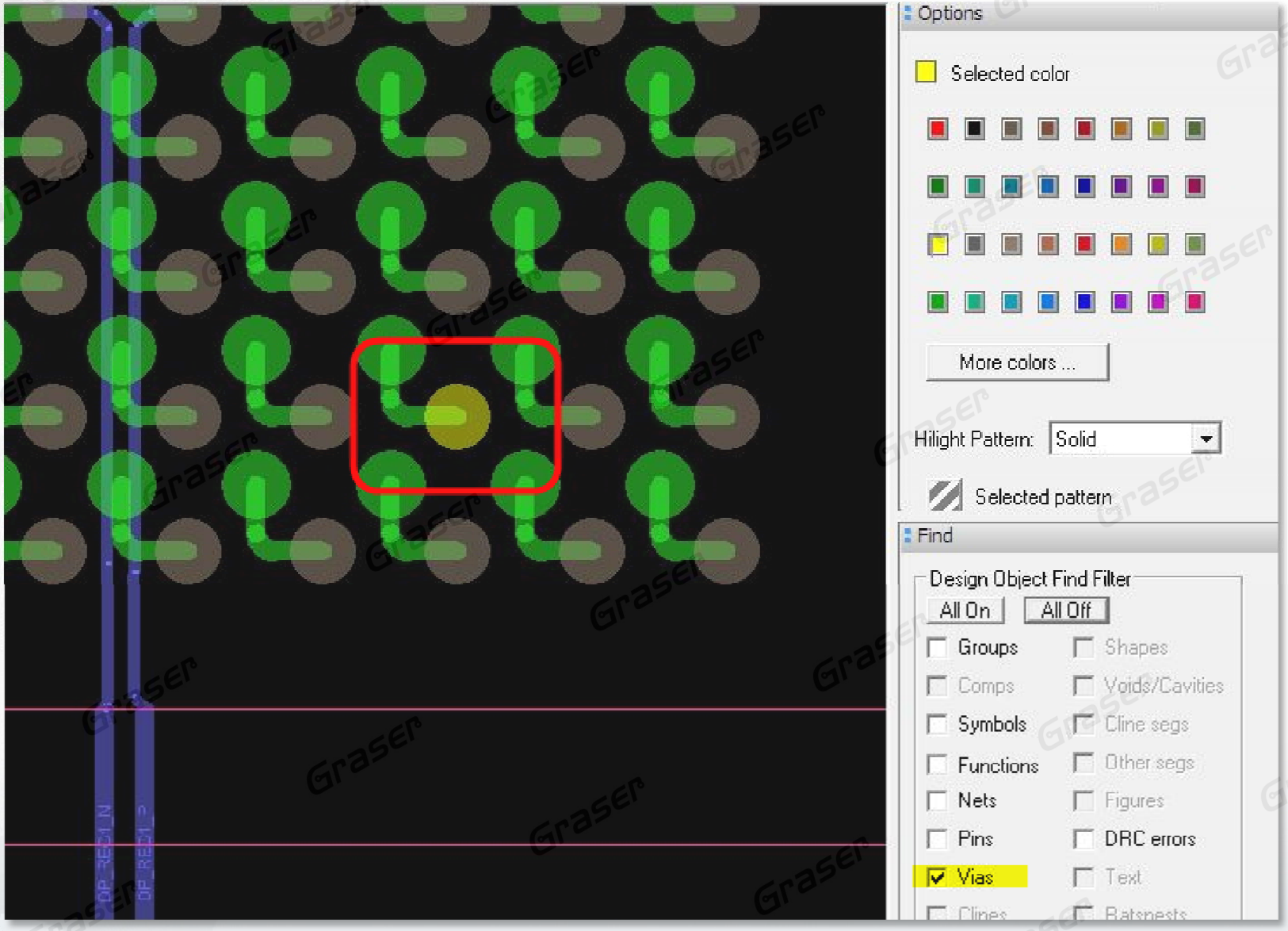
- Trim by line intersection
  - Delete segment on either side of intersecting line



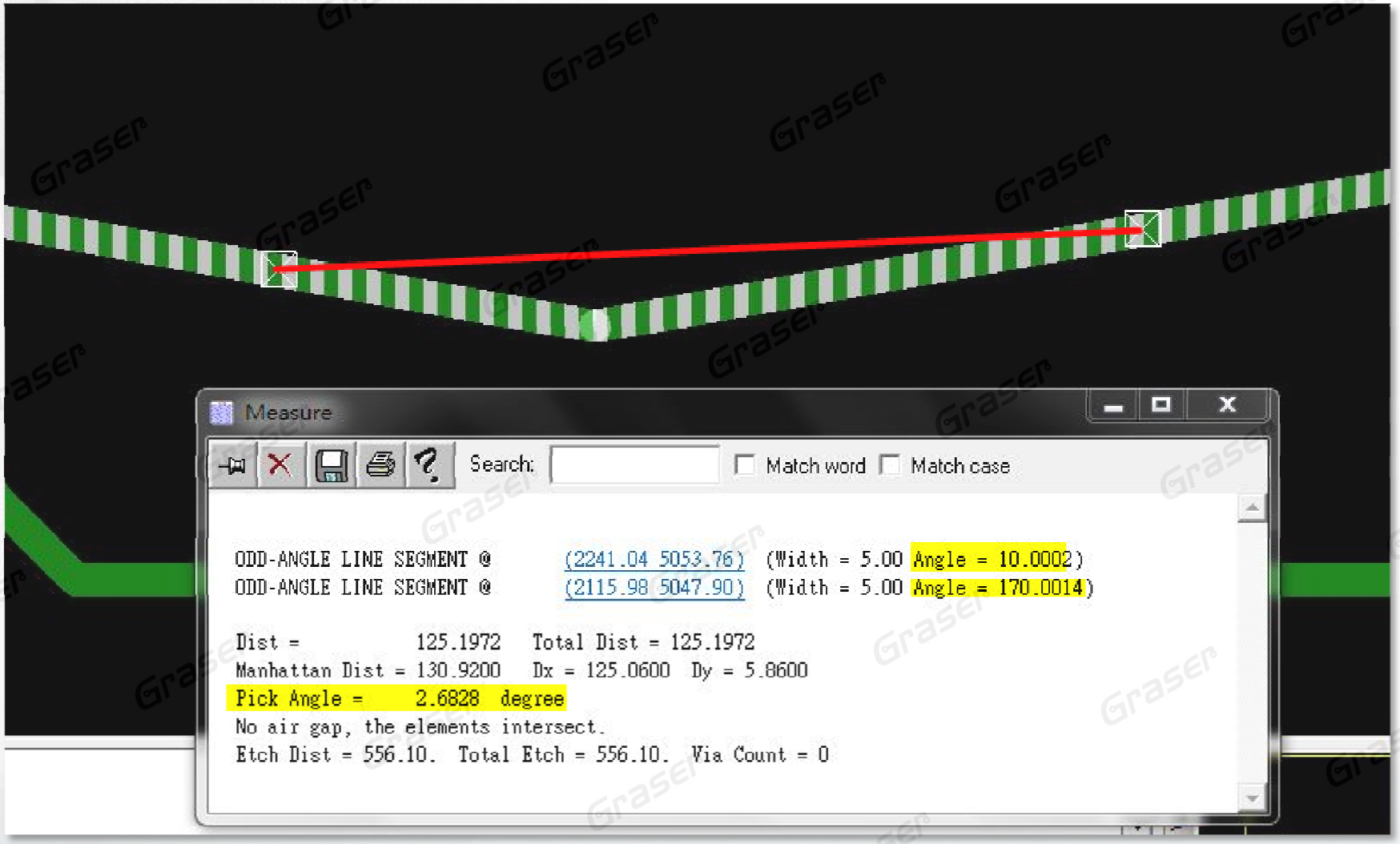
- Offset Copy / Offset Move
  - Parameters to control offset distance, line style, width, repeated instances



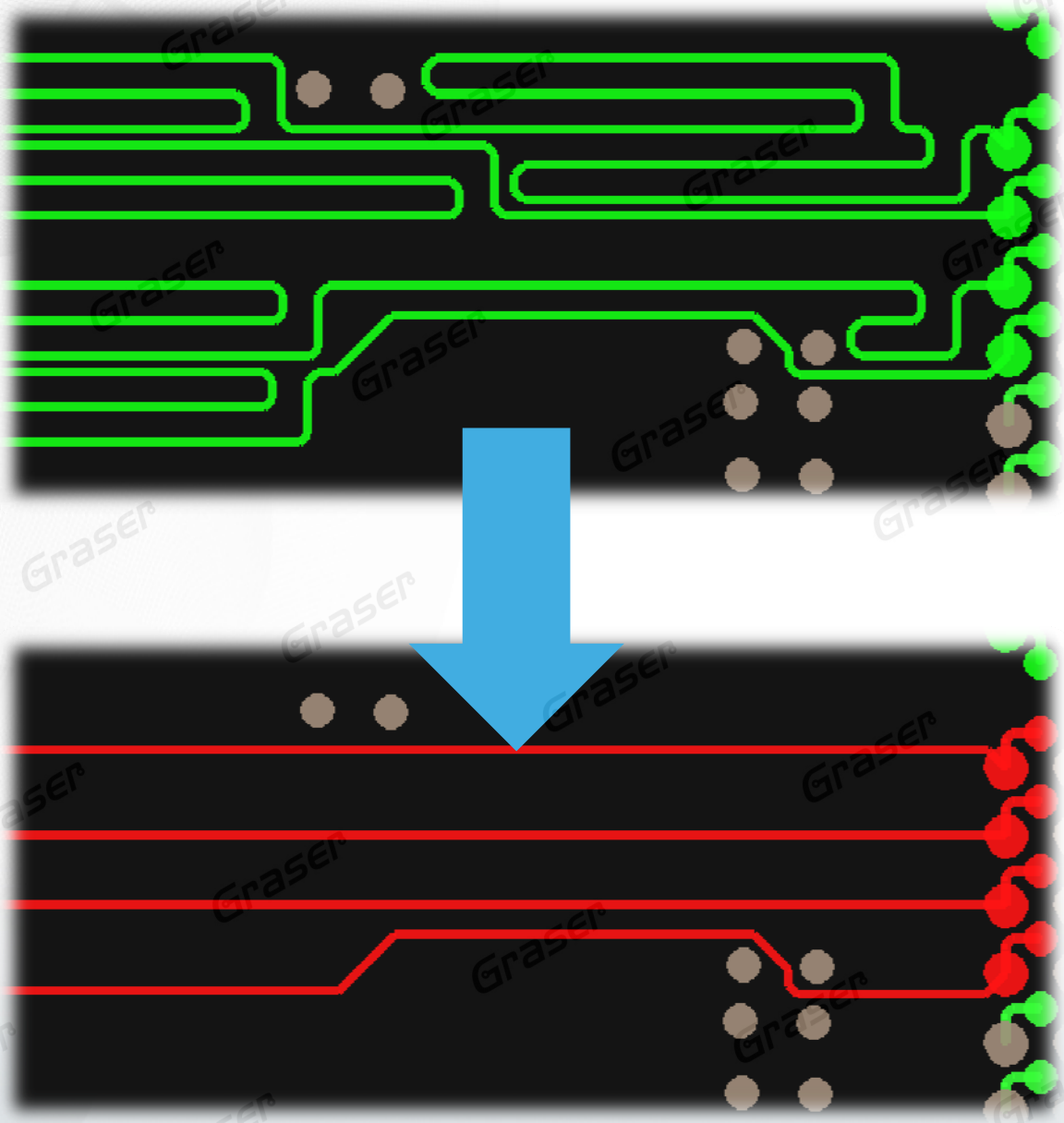
Highlight to Vias



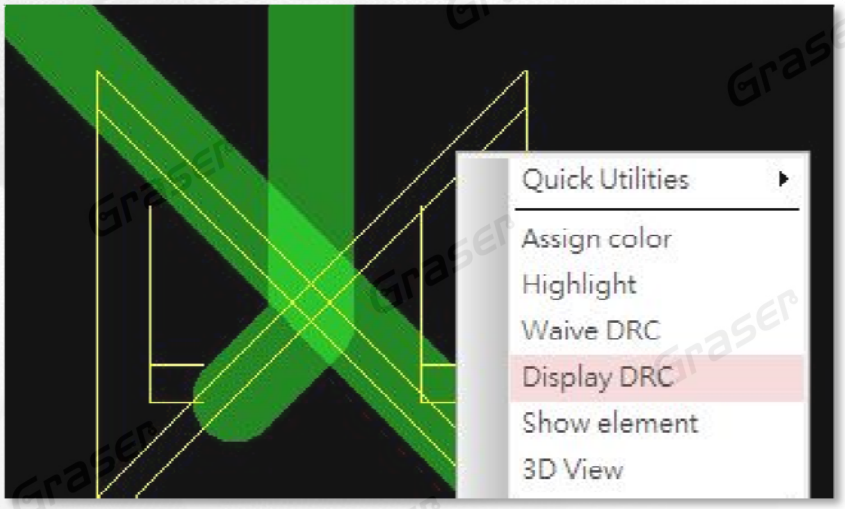
Measure Support of Angle

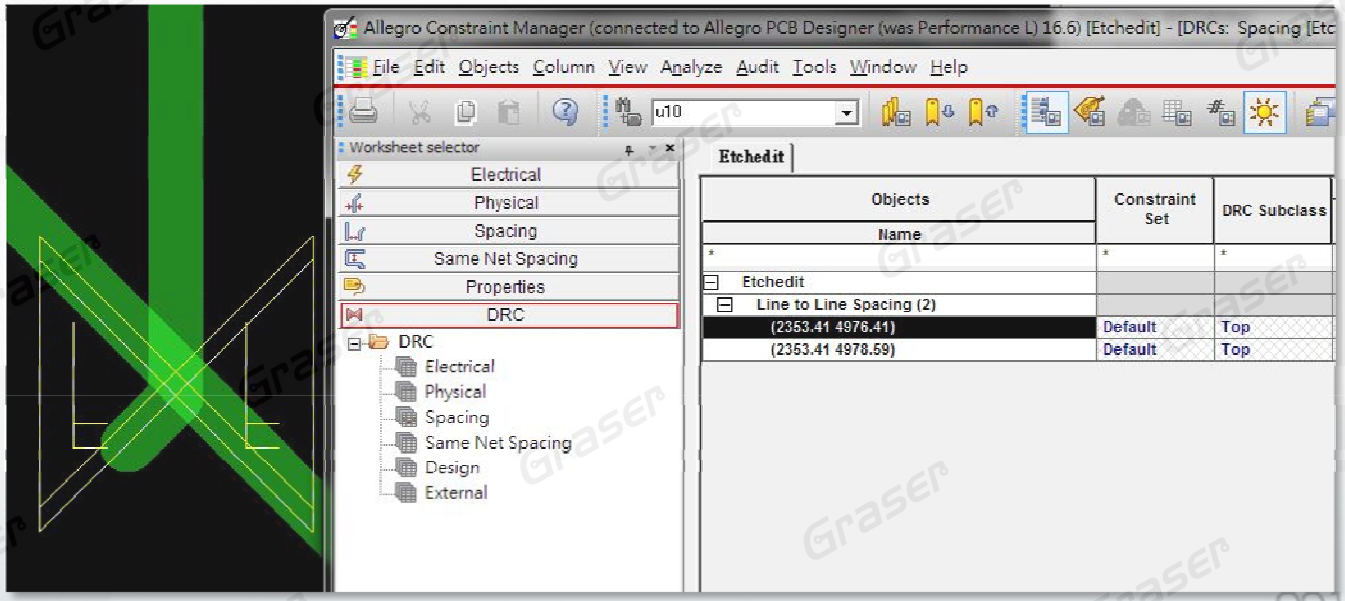


Detune



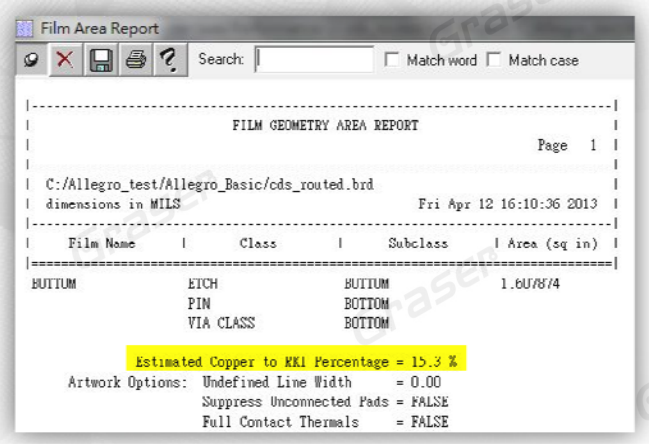
DRC – Link to CM





New Reports

- **Film Area**



- **Via per net**
- **Via per layer per net**

Via List

Net Name	Total Vias	Through Vias	BB Vias	Micro Vias	Via Names
HDI_STACK	1	0	0	1	BB1-2
NET3	6	0	1	5	BB1-2, BB2-3, BB3-4, BB-CORE
NET9	4	0	1	3	BB1-2, BB2-3, BB3-4, BB-CORE
NET14	3	0	0	3	BB7-8
NET15	2	0	0	2	BB7-8
NET17	1	0	0	1	BB1-2
NET20	1	0	0	1	BB1-2
NET30	17	0	4	13	BB1-2, BB2-3, BB-CORE3-6, BB
NET31	4	0	1	3	BB1-2, BB2-3, BB3-4, BB-CORE
NET34	5	0	1	4	BB1-2, BB2-3, BB-CORE3-6, BB
PECL1_P	7	0	1	6	BB1-2, BB2-3, BB3-4, BB-CORE
Totals	51	0	9	42	

Via per net

Via List

Layer	Net Name	Total Vias	Through Vias	BB Vias	Micro Vias	Via Names
TOP	HDI_STACK	1	0	0	1	BB1-2
	NET3	1	0	0	1	BB1-2
	NET9	1	0	0	1	BB1-2
	NET17	1	0	0	1	BB1-2
	NET20	1	0	0	1	BB1-2
	NET30	4	0	0	4	BB1-2
	NET31	1	0	0	1	BB1-2
	NET34	1	0	0	1	BB1-2
	PECL1_P	1	0	0	1	BB1-2
Totals		12	0	0	12	
SIGNAL_2	HDI_STACK	1	0	0	1	BB1-2
	NET3	2	0	0	2	BB1-2, BB2-3
	NET9	2	0	0	2	BB1-2, BB2-3
	NET17	1	0	0	1	BB1-2
	NET20	1	0	0	1	BB1-2
	NET30	8	0	0	8	BB1-2, BB2-3
	NET31	2	0	0	2	BB1-2, BB2-3
	NET34	2	0	0	2	BB1-2, BB2-3
	PECL1_P	3	0	0	3	BB1-2, BB2-3

Via per layer per net

- **Missing Fillets**

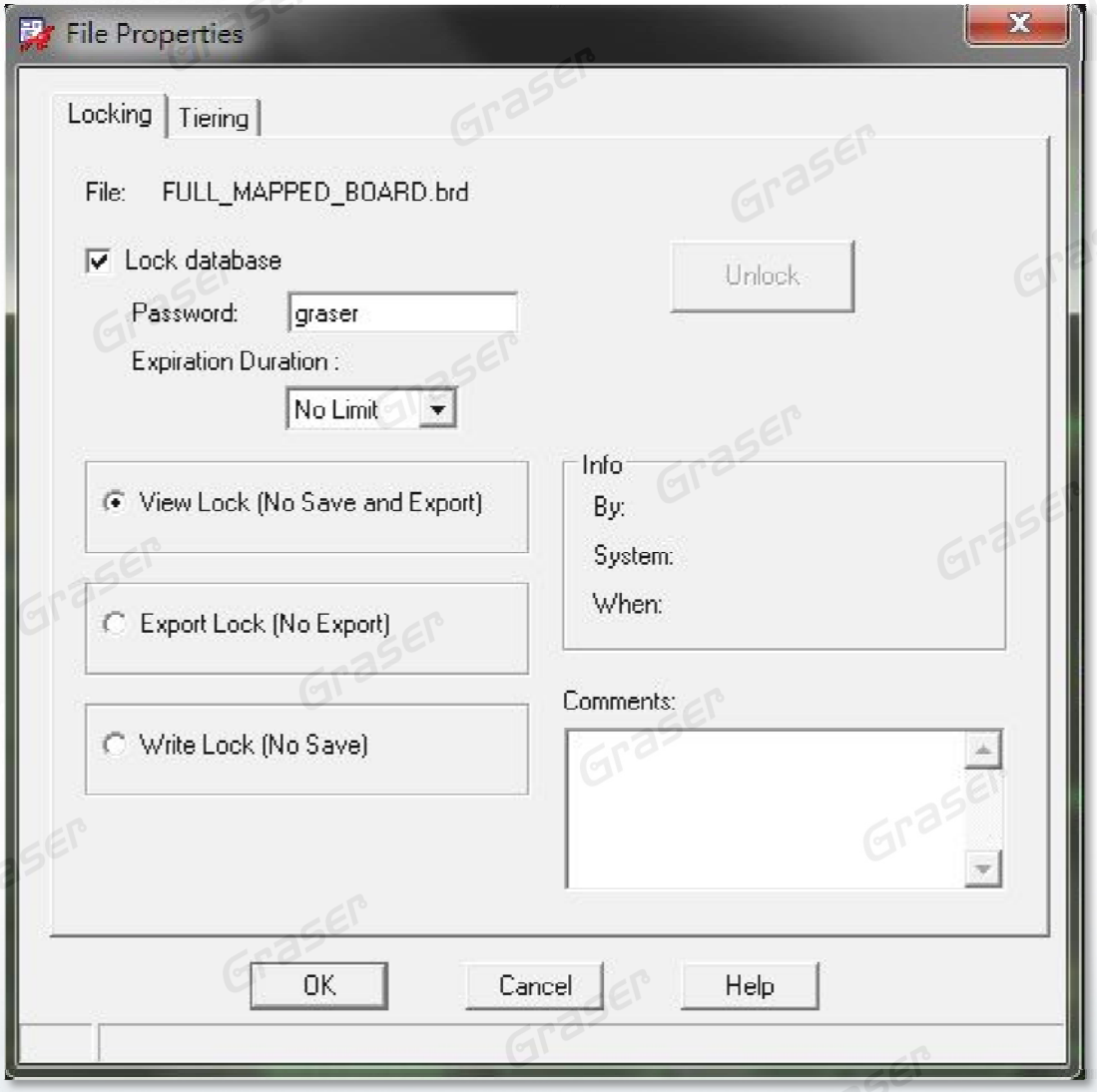
Missing Fillets

Subclass	Net	Item	Location	Partial
BOTTOM	CLK3-	VIA	(801.50 2925.00)	yes
BOTTOM	CLK4+	T	(1316.00 2965.00)	
BOTTOM	GND	VIA	(2330.50 2983.00)	
BOTTOM	GND	VIA	(369.50 3117.00)	
BOTTOM	GND	VIA	(480.50 3413.00)	
BOTTOM	W_R	VIA	(800.00 1308.00)	yes
TOP	A1	SYMBOL PIN	(1348.00 2550.00)	
TOP	A1	SYMBOL PIN	(1580.00 1360.00)	
TOP	A1	T	(811.49 690.50)	
TOP	A1	VIA	(811.49 690.52)	
TOP	A10	SYMBOL PIN	(902.00 2300.00)	
TOP	A13	SYMBOL PIN	(1225.00 2177.00)	
TOP	A3	SYMBOL PIN	(902.00 800.00)	
TOP	A3	T	(1292.00 2475.00)	
TOP	A3	T	(869.50 920.49)	
TOP	A4	SYMBOL PIN	(902.00 850.00)	
TOP	A7	T	(1305.00 2240.00)	
TOP	ADDR5	SYMBOL PIN	(1692.50 3420.00)	
TOP	CLK2	SYMBOL PIN	(1580.00 1438.00)	
TOP	CLK2	SYMBOL PIN	(1580.00 1438.00)	
TOP	D1	SYMBOL PIN	(315.00 2050.00)	

Database Locks

Enhanced database locking support

- View Only
- No Export
- No Saving



Database Tiering

- The following capabilities will be checked:
  - All electrical DRC modes
  - Differential pair static and dynamic phase control
  - Pin Delay
  - Via Z
  - Constraint Regions
  - Micro via padstacks
  - Embedded layers
  - Dynamic fillets