Cadence Virtuoso XL

CUSTOM DESIGN PLATFORM

DESIGN COMPOSITION

- Complete design hierarchy support
- Simplified automatic generation of an HDL template
- Support of multi-sheet schematics
- User-configurable command bindkeys and label display
- Dynamic highlighting for easy design correction
- Automated interactive connection router
- User-configurable selection with filtering
- Comprehensive symbol creation and editing features
- User-configurable undo/redo levels
- Move, copy, stretch, rotate, and delete editing options
- Search and replace features
- Customizable tool environment using Cadence SKILL
- Online help using HTML formatted publications

DESIGN SIMULATION AND ANALYSIS

- Design exploration with sweeps, corners, and Monte Carlo statistics
- Creation of specifications directly from simulation results
- Specifications sheets to compare design to design, design to model, or process to process
- Projects can be shared among multiple users and sites
- Distributed processing
- Parallel analysis of multiple tests
- Creation and tracking of dependencies among tests
- Calculator, Ocean, MDL, and MATLAB measurement strategies
- Tests overview window with specification checking
- Integrated with Virtuoso Multi-Mode Simulation
- Cross-probing and annotation to schematics
- Integrated Wavescan waveform display and waveform calculator for sophisticated analysis
- Integral documentation creation

PHYSICAL IMPLEMENTATION

- Automated device editing, including abutment, pin permutation, folding, chaining, and cloning
- Menu-driven or programmable multipart path (MPP) feature for guard rings, slotting, etc.
- Design-rule–driven editing with real-time notification or enforcement of process rules
- Dynamic measurement
- Constraint-driven specification, management, and real-time notification or enforcement
- Automatic constraint- and design-rule– driven placement of pins, devices, cells, and blocks
- Advanced shape-based constraint- and design-rule–driven interactive routing
- ECO support
- Legacy non-connectivity design importing and connectivity mapping
- AssuraR physical verification support

DESIGN INPUTS

- OpenAccess data objects
- Cadence proprietary languages: Ocean and MDL
- SPICE netlists
- EDIF 2 0 0 netlist
- Circuit design language (CDL)
- SPICE
- VHDL IEEE 1076-1993
- Verilog IEEE1364
- SKILL
- STREAM format
- CDL and SPICE netlist format
- Verilog and VHDL AMS languages

DESIGN OUTPUTS (VIRTUOSOSCHEMATIC EDITOR XL)

- EDIF 2 0 0 netlist
- CDL
- SPICE
- OpenAccess
- SKILL
- STREAM format

DESIGN OUTPUTS (VIRTUOSO ANALOG DESIGN ENVIRONMENT XL)

- PSF waveform format
- SST2 waveform format
- Perl scripts

PLATFORM/OS

- Sun/Solaris
- HP-UX
- Linux
- IBM AIX

THIRD-PARTY SUPPORT

- Access to other third-party simulators from Synopsys, Mentor Graphics,Silvaco, Magma, Berkeley Design Associates, and in-house proprietary simulators are supported through the Virtuoso Analog Design Environment interface
- Supports MATLAB from Mathworks for additional measurements and visualization

VIRTUOSO CUSTOM DESIGN PLATFORM XL FEATURES

	Virtuoso Schematic Editor XL	Virtuoso Analog Design Environment XL	Virtuoso Layout Suite XL
New Common Cockpit	X	X	X
New Icon Style	X	X	X
Multi-Tab Support	X	X	X
Bookmarks & History	X	X	X
Updated Pulldown Menus	X	X	X
Window Config Support	X	X	X
World View Assistant	X		X
Search Assistant	X		X
Property Editor Assistant	X		X
Navigator Assistant	X		X
Constraint Browser	X		X
Design Explorer	X		X
Single Test-bench		X	
Simple Parametric Analysis		X	
Device Checking		X	
Global Variable Support		X	
Updated Wavescan		X	
New Calculator		X	
Simulation Support: Virtuoso Multi-mode Simulation, HSPICE		X	
Basic Polygon Editing			X
Q-Cells			X
DRD Editing			X
Constraint Browser			X
Search Assistant			X
Property Editor Assistant			X