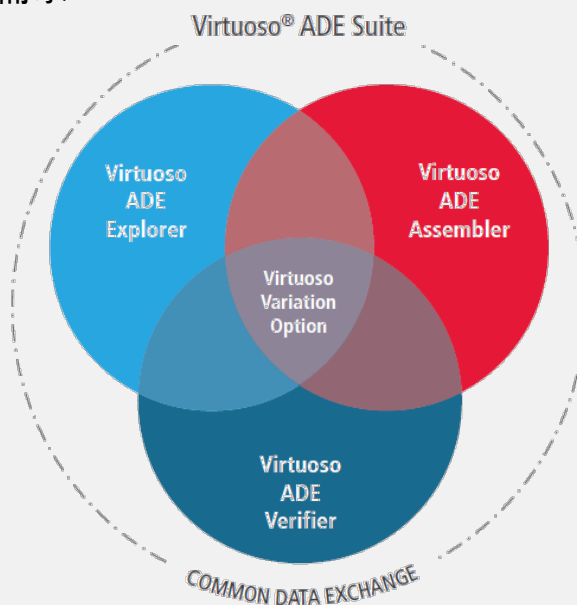


全新的類比設計環境 - Cadence Virtuoso ADE Product Suite

Cadence發表了新一代的類比設計環境，可為設計人員帶來**10倍跨**
平台效能與容量提升，且新一代的Cadence® Virtuoso® ADE Product Suite 能夠克服新的業界標準、先進節點設計以及系統設計需求興起帶來的挑戰，協助工程師充分地探索、分析與驗證設計，以確保在整個設計周期中都能維持設計意圖，因應汽車安全、醫療裝置與物聯網(IoT)應用等需求。



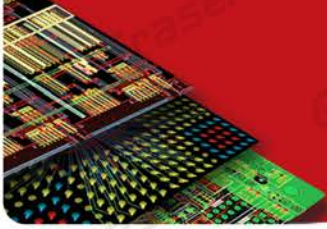
• **Date** : 2016 / 9 / 12

• **Author** : Scott

• **Revision** : 1.2

• **Version** : IC6.1.7

• **備註**:



Cadence® Virtuoso® ADE Explorer

實現快速、準確的設計規格即時調整，且可以依照使用者訂定的規格條件提示 Pass/Fail 的狀態，此外也提供完整的 Corner 與 Monte Carlo 統計環境，協助使用者偵測和修補變異性等問題，達到縮短設計時程的優勢。

Familiar ADE L menus

Design Window is opened in a tab

Define analysis, variables, corners, Monte Carlo directly in the Setup Assistant

Corners and Monte Carlo previously available only in the higher tiers

Name	Type	Details	Value	Plot	Save	Spec
/I0/M1	oppoint	/I0/M1 vdsat				
Swing	signal	/OUT				
Swing	expr	(value(VT("/OUT") 2.5e-08) - val...	1.136			> 0.98
SettlingTime	expr	settlingTime(VT("/OUT") 0 t 2.5...	7.565 ns			< 8n
RelativeSwingPercent	expr	((Swing / VAR("vdd")) * 100)	75.73 %			> 75
PhaseMargin	expr	getData("/phaseMargin" ?result...	18.69 degree			> 20
	signal	/I0/net6				
	signal	/I0/net10				
vdsat	expr	OT("/I0/M1" "vdsat")				

- Results are shown in the Value column for single point simulations (ADE L style)
- For multi-point simulations a Results tab opens (ADE XL style)
- Color coded specifications for easy visualization of design status

"Familiar" ADE L toolbar

Cadence® Virtuoso® ADE Explorer cockpit

Monte Carlo Setup

Statistical Variation: Process, Mismatch, All

Sampling Method: Low-Discrepancy Sequence

Max Number of Points: 88

Target Yield: 94%

Probability (1-alpha): 95.8%

Yield Table

Test Name	Yield	Min	Target	Max	Mean	Std Dev
Swing	100	1.131	> 980m	1.141	1.136	2.747m
Swing	100	1.131	> 980m	1.141	1.136	2.747m
SettingTime	100	7.485 ns	< 8n	7.648 ns	7.566 ns	42.46 ps
SettingTime	100	7.485 ns	< 8n	7.648 ns	7.566 ns	42.46 ps
RelativeSw...	100	75.43 %	> 75	76.1 %	75.75 %	183.1 m%
RelativeSw...	100	75.43 %	> 75	76.1 %	75.75 %	183.1 m%
PhaseMa...	0	17.77 degree	> 20	19.32 degree	18.61 degree	454.6 mdegree
PhaseMa...	0	17.77 degree	> 20	19.32 degree	18.61 degree	454.6 mdegree

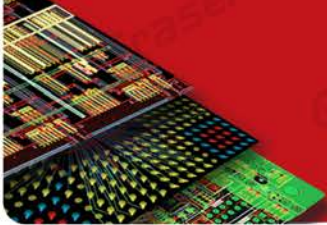
SettingTime Plot

Pass = 26/20 (100%)
Mean = 7.56641n
Std Dev = 42.4551p

normalQQ(SettingTime)

Normal
r = 0.9889
p = 0.9138

Monte Carlo analysis



Design Variables

M6_M8_finger_ratio	2
M6_M7_finger_ratio	4
M10_M9_finger_ratio	2
vdd	1.8

Parameters

M1/l	300n
M1/w	120u
NM0/l	300n
NM0/fw	12u

Slider bar: 900m ————— 2.7

Annotations:

- Design Variables section that lists all the design variables and their values defined in the Setup
- Parameters section that lists all the parameters and their values defined in the Setup
- Stop simulation button to stop running simulation after a value is changed.
- Undo button to bring back the changed variable and parameter values to the previous values
- Play button to put the simulator into listening mode
- Redo button to bring back the changes. It works in synchronization with the Undo button.
- Load button to load the design and variable values from the original setup
- Slider bar that you can use to dynamically change the values of variables and parameters. When these values are modified, the output results are simultaneously updated in the graph window.
- Save button to save the updated values back into the Explorer setup

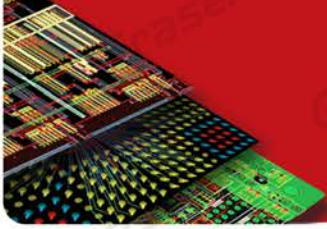
Real-Time Tuning in Simulations

Outputs only

Outputs with docked ViVA

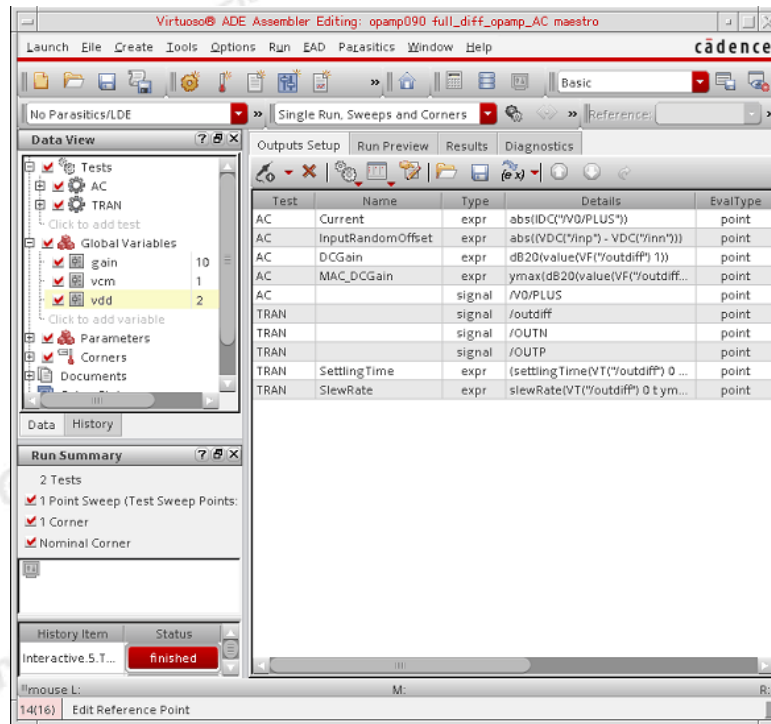
Schematic with waveform balloons and docked ViVA

Variety of waveform displays



Cadence® Virtuoso® ADE Assembler

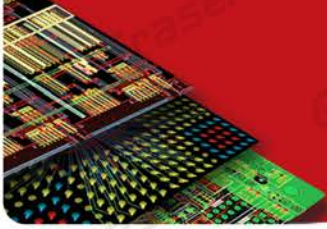
協助工程師在不同的製程—電壓—溫度(PVT) 組合條件分析其設計，並提供基於 GUI 的驗證計畫，因此設計人員能輕鬆地建立條件與相依性模擬。



Cadence® Virtuoso® ADE Assembler cockpit

Point	Corner	VDD	fclk	gpdck045.sc	temperature	Pass/Fail	tau_m	Probability of Error
1	C1_1	1.2	100M	mc	80	fail	8.89p	0
2	C1_2	1.2	100M	mc	120	fail	9.96p	0
3	C1_1	1.2	110M	mc	80	fail	8.811p	0
4	C1_1	1.2	120M	mc	80	fail	8.879p	0
5	C1_1	1.2	130M	mc	80	fail	8.873p	0
6	C1_1	1.2	140M	mc	80	fail	6.908p	0
7	C1_2	1.2	140M	mc	120	fail	9.923p	495.2e-312

Filtering of results



Copy of the active setup (2 tests at Nominal)

Copy of the active setup with modification (Monte Carlo run on 1 test)

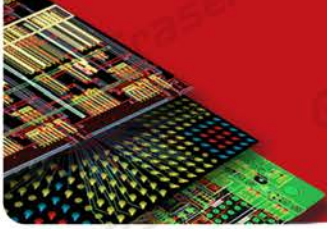
Run that is equal to active setup but VDD=3V

Test	Name
opamp090:full_diff_opamp_AC:1	Current
opamp090:full_diff_opamp_AC:1	InputRandomOffset
opamp090:full_diff_opamp_TRAN:1	SettlingTime
opamp090:full_diff_opamp_TRAN:1	Count 'All Checks/Asse

Run Plan Configuration:

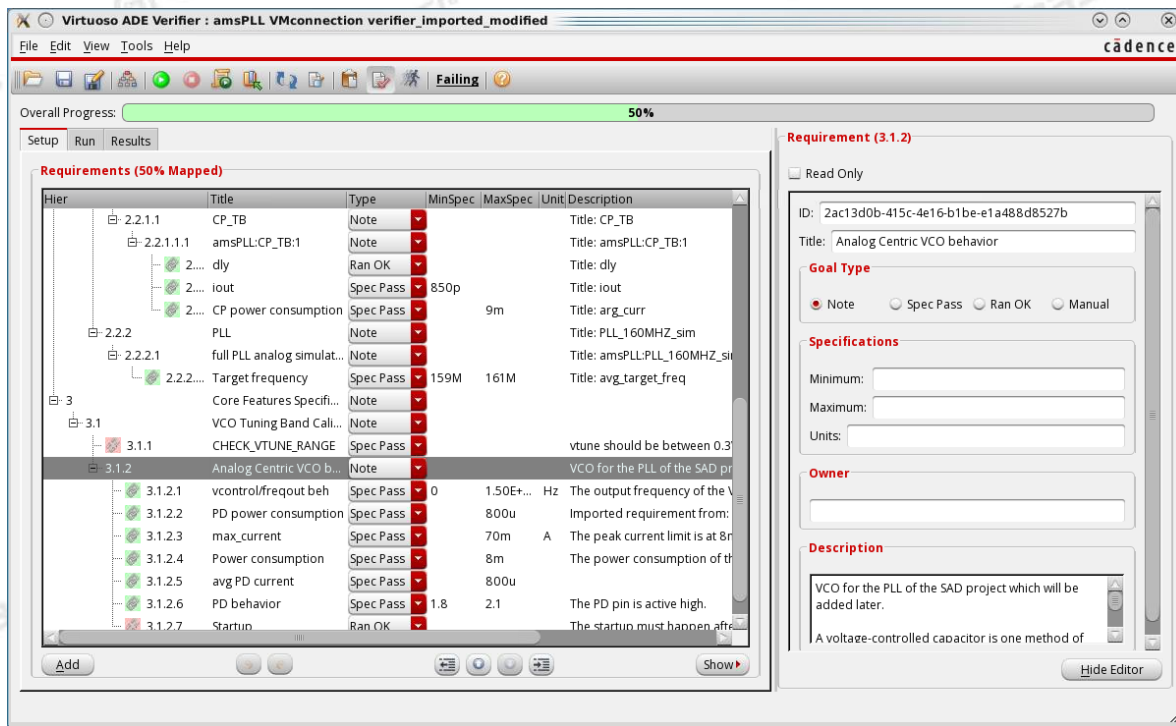
- Run.0: Single Run, Sweeps and Corners
 - Tests: opamp090:full_diff_opamp_AC:1, opamp090:full_diff_opamp_TRAN:1
 - Global Variables: gain (10), vcm (1), vdd (2)
- Run.1: Monte Carlo Sampling
 - Tests: opamp090:full_diff_opamp_AC:1 (selected), opamp090:full_diff_opamp_TRAN:1
 - Global Variables: gain (10), vcm (1), vdd (2)
- Run.2: Single Run, Sweeps and Corners
 - Global Variables: vdd (3)

Run Plan

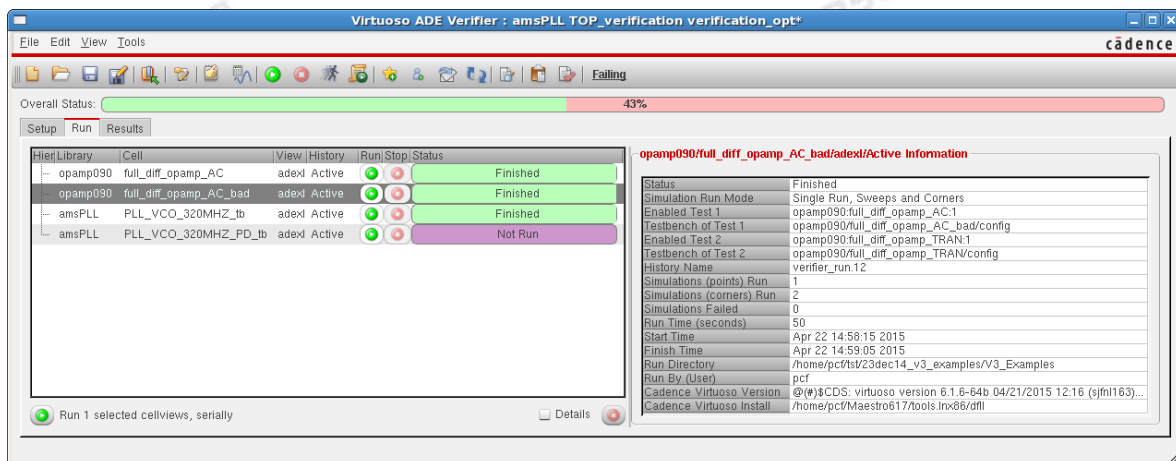


Cadence® Virtuoso® ADE Verifier

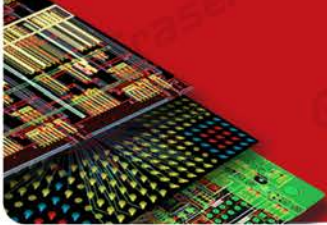
提供一個整合式驗證環境，可讓工程師/產品經理輕鬆連結到與設計有關的所有模塊去進行驗證與分析，進而掌控各模塊的執行進度以執行最佳資源分配。



Cadence® Virtuoso® ADE Verifier cockpit



Cadence® Virtuoso® ADE Verifier job monitor



Viewing TOP_verification_run.html

Failed (7/16)

43%

Run Information

ADC_XL Lib	ADC_XL Code	ADC_XL View	Status	Total Points	Failed Points	Deadline	Start	Finish	User	IC Version	IC Installation	Directory
opamp000	NA_BPT_opamp_AC_bnd	adcd	Finished	1	0	50s	Mon 1 17:59:10 2017	Mon 1 17:59:20 2017	pcd	QSPICE3-rt6000 version 8.1.1-64-bit (2017.04.04) (beta16C)	Andromeda\BSP\bin\170404\QSPICE3-rt6000\Andromeda\BSP\bin\170404\QSPICE3-rt6000	
opamp000	NA_BPT_opamp_AC_bnd	adcd	Finished	1	0	55s	Mon 1 17:59:11 2017	Mon 1 18:00:09 2017	pcd	QSPICE3-rt6000 version 8.1.1-64-bit (2017.04.04) (beta16C)	Andromeda\BSP\bin\170404\QSPICE3-rt6000\Andromeda\BSP\bin\170404\QSPICE3-rt6000	
msvPLL	PLL_VCO_320MHz_FD_b	adcd	Finished	5	0	120s	Mon 1 18:00:14 2017	Mon 1 18:02:10 2017	pcd	QSPICE3-rt6000 version 8.1.1-64-bit (2017.04.04) (beta16C)	Andromeda\BSP\bin\170404\QSPICE3-rt6000\Andromeda\BSP\bin\170404\QSPICE3-rt6000	
msvPLL	PLL_VCO_320MHz_FD_b	adcd	Running (15%)				Mon 1 18:02:23 2017					

Result Information

Contents

SAD1 - Project -> Schematics\AnalogDesign

SAD1.1 - OpAmp

- SAD1.1.1 - Analog Parametric AC Behavior
- IB1 - Max AC gain
- IB2 - DC Gain
- IB3 - Input offset
- SAD1.2 - Analog Parametric Tran Behavior
- IB3 - Max power consumption
- IB4 - Settling Time
- IB5 - Slew Rate
- SAD1.3 - Functional tests
- SAD1.4 - Power up behavior

Viewing TOP_verification_run.html

SAD4 : VCO

Goal in Order of Contents

Goal Type: Group, Success: 20/20, Pass Rate: 5, Requirements: 1 Failed, 1 Passed, 0 Not Run, 1 Unmapped

VCO2 for the PLL of the SAD project which will be added later. A voltage controlled oscillator is one method of making an LC oscillator vary its frequency in response to a control voltage. Any resonant bound semiconductor device exhibits a measure of voltage-dependent capacitance and can be used to change the frequency of an oscillator by varying a control voltage applied to the diode. General-purpose variable capacitance varactor diodes are available with well-defined device energy values of capacitance. Such devices are easy component in the manufacture of voltage-controlled oscillators (VCO). Other methods of varying the frequency (such as altering the charging rate of a capacitor in series of a voltage controlled current source) are used for function generator. The frequency of a ring oscillator is controlled by varying either the supply voltage, the current available to each inverter stage, or the capacitor loading on each stage.

ID	Requirement	Goal Type	Description	ADC_XL Lib	ADC_XL Code	ADC_XL Name	Test	Output	Specification	Min Spec	Max Spec	Total Points	Passing Points	Failing Points	Minimum	Maximum	Requirement Status
SAD4.1	vcontrol/freqout beh	Spec	The output frequency of the VCO should be above the following limit: 20M + (vcontrol-0.5)*300M@2.0V supply	msvPLL	PLL_VCO_320MHz_b	adcd	msvPLL.PLL_VCO_320MHz_b.1	freq_out	0 to 150M	None	None	5	4	1	2.623185e+07	5.19605e+08	Fail
SAD4.2	power consumption	Spec	The peak current limit is at 8m A	msvPLL	PLL_VCO_320MHz_b	adcd	msvPLL.PLL_VCO_320MHz_b.1	max_current	<70m	None	70m	5	5	0	0.0050062	0.08773005	Pass
SAD4.3	Power consumption	Spec	The power consumption of the VCO should be less than 800u														Not Mapped

Description	Min	Max	Owner	Description	Comment
OpAmp				Classical OpAmp design	This all looks good
Analog Parametric AC Behavior	Analog	Analog	Analog	Analog Parametric AC Behavior	
Max AC gain	20		Harry	The maximum AC gain	
DC Gain	25		Harry	DC Gain	
Input offset	0m		Harry	Input random offset value	
Analog Parametric Tran Behavior			Jane	Ensure correct tran beh.	
Max Current consumption	6.58m	7.42m	Jane	The maximal power consumption must be within the specified range	Hans: should be ok
Settling Time		21n	Fred	Settling time	
Slew Rate	1.25E+08		Fred	Slew Rate	
Functional tests				Make sure that the block is functionally correct. - digital control pins operate active low - power down mode - ...	
Power up behavior				Do a proper power up sim on full transister level	
Ensure Yield				The yield of this block must be ...	
VCO				The output frequency of the VCO should be above the following limit: 20M + (vcontrol-0.5)*300M@2.0V supply	
vcontrol/freqout beh	0	1.50E+08			Fred said that this should be fix next week
power consumption		800u			
max current		70m		The peak current limit is at 8m A	

Specification comparison sheets and datasheets