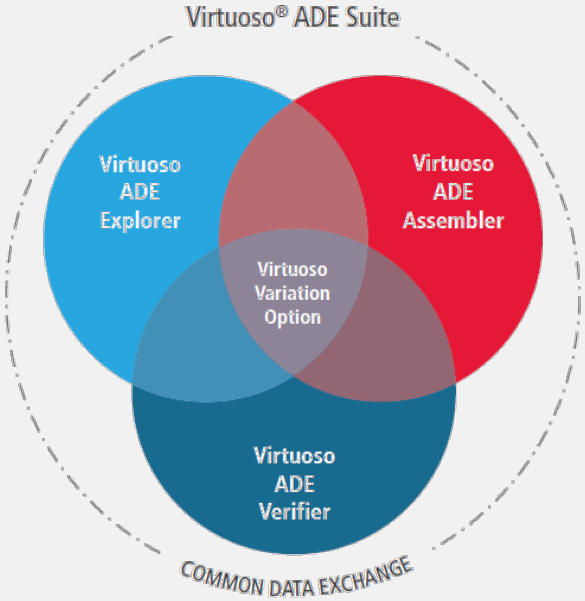
# 全新的類比設計環境 - Cadence Virtuoso ADE Product Suite

Cadence發表了新一代的類比設計環境，可爲設計人員帶來**10倍跨平台效能與容量提升**，且新一代的Cadence® Virtuoso® ADE Product Suite 能夠克服新的業界標準、先進節點設計以及系統設計需求興起帶來的挑戰，協助工程師充分地探索、分析與驗證設計，以確保在整個設計周期中都能維持設計意圖，因應汽車安全、醫療裝置與物聯網(IoT)應用等需求。




- **Date：** 2016 / 9 / 12
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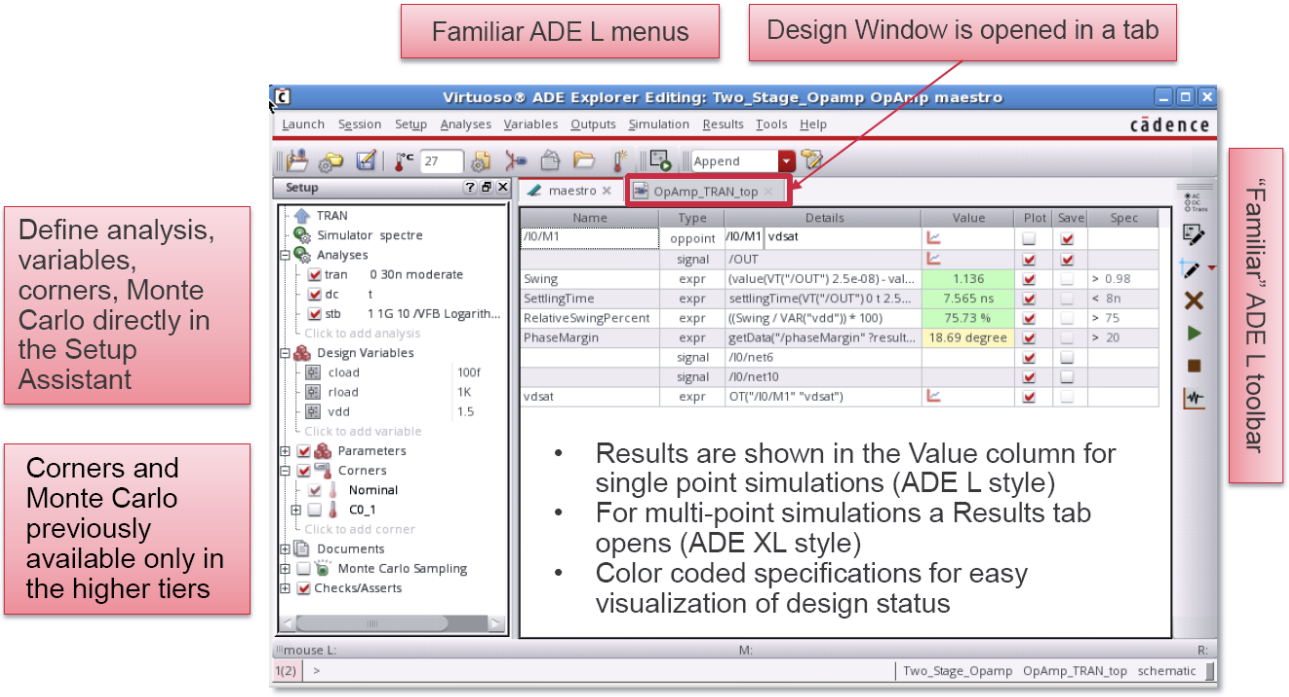
- **備註:**

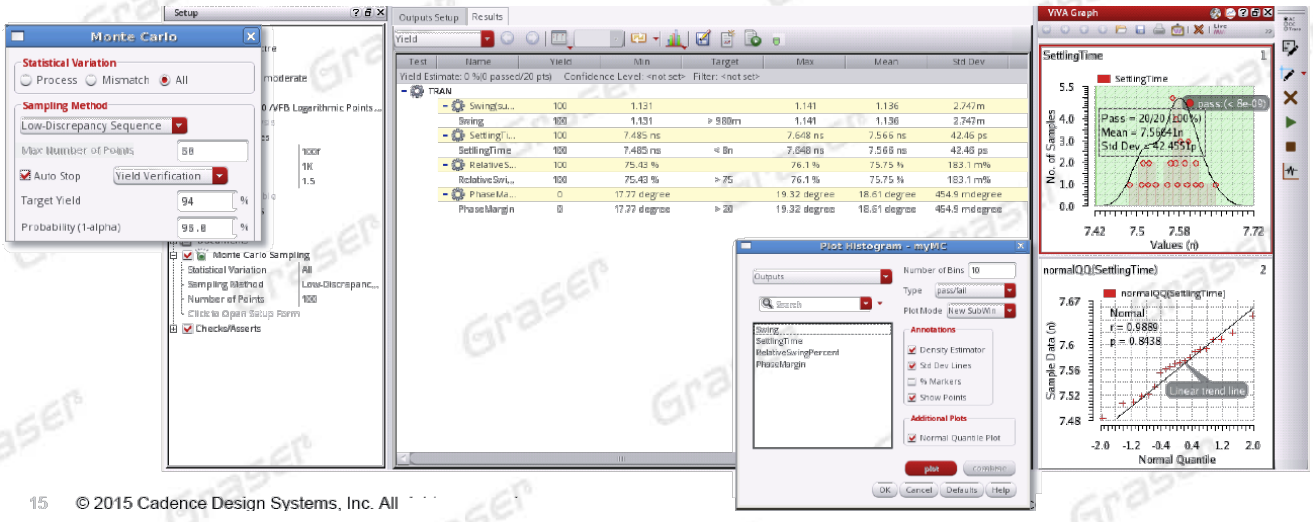
Graser® http://www.graser.com.tw

# Cadence® Virtuoso® ADE Explorer

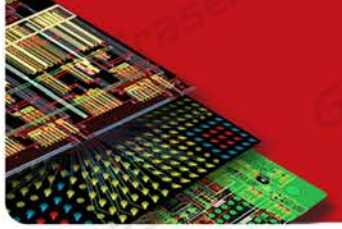
實現快速、準確的設計規格即時調整，且可以依照使用者訂定的規格條件提示 **Pass/Fail** 的狀態，此外也提供完整的 **Corner** 與 **Monte Carlo** 統計環境，協助使用者偵測和修補變異性等問題，達到縮短設計時程的優勢。




**Cadence® Virtuoso® ADE Explorer cockpit**




**Monte Carlo analysis**



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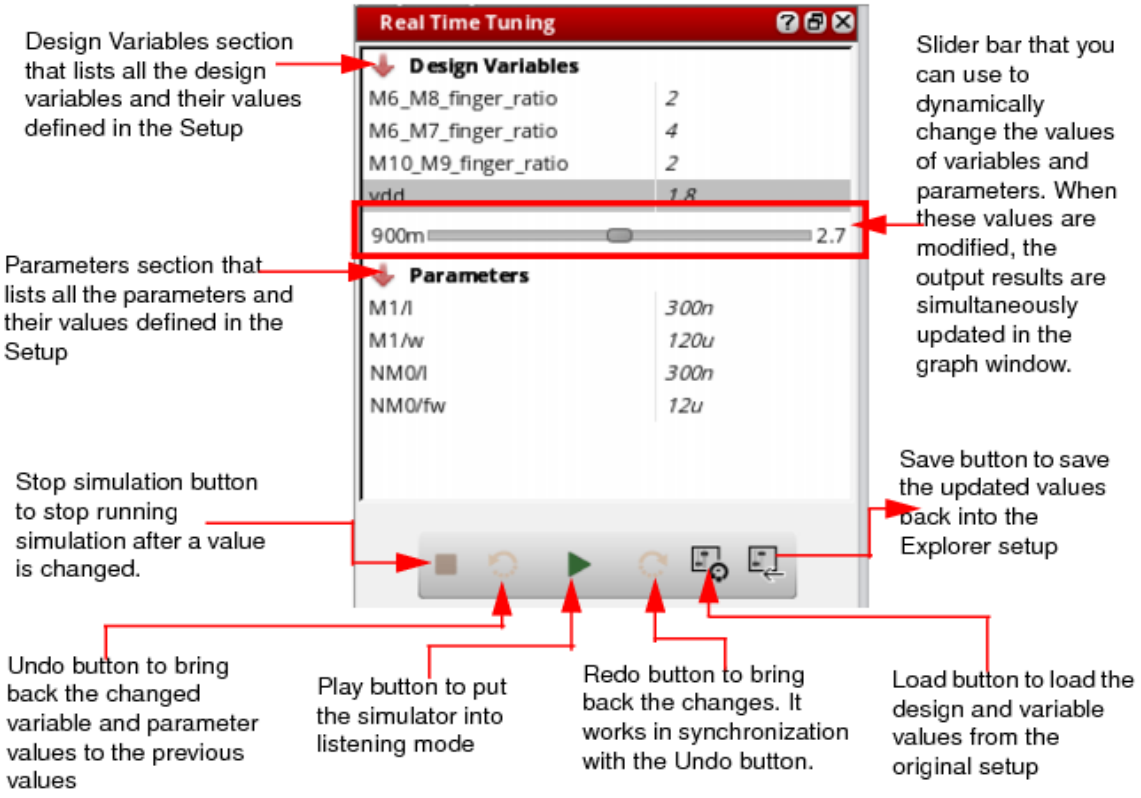
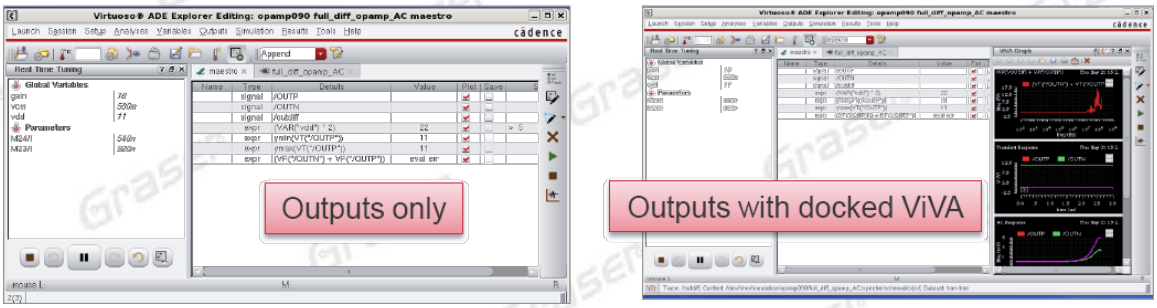
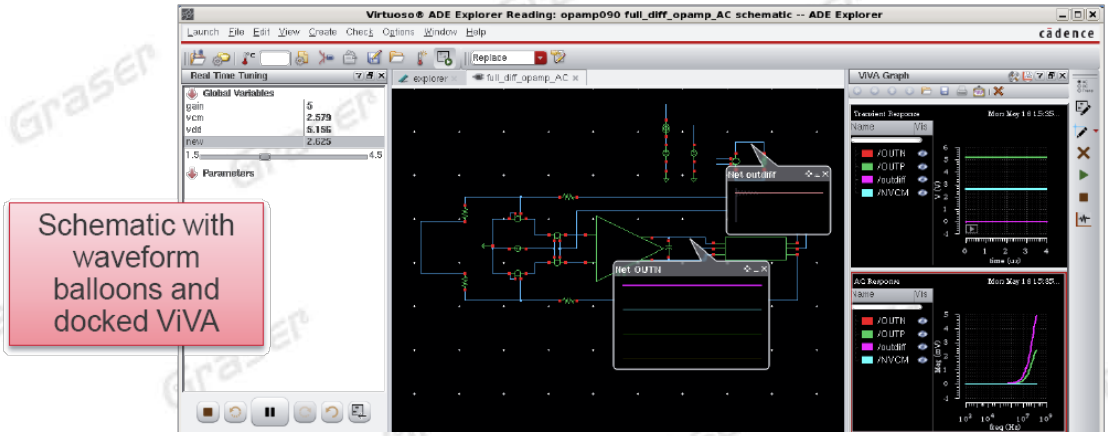



**Real-Time Tuning in Simulations**

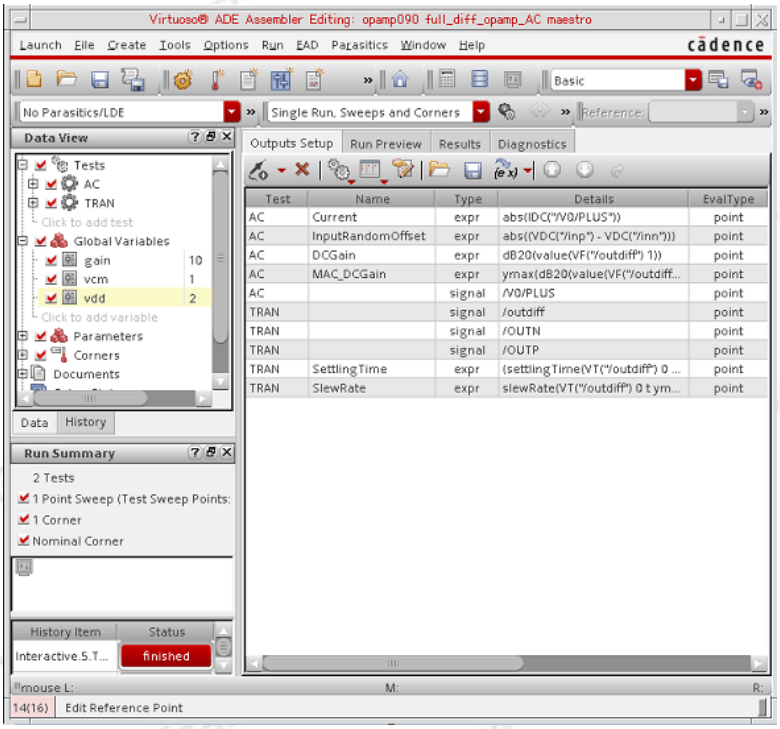


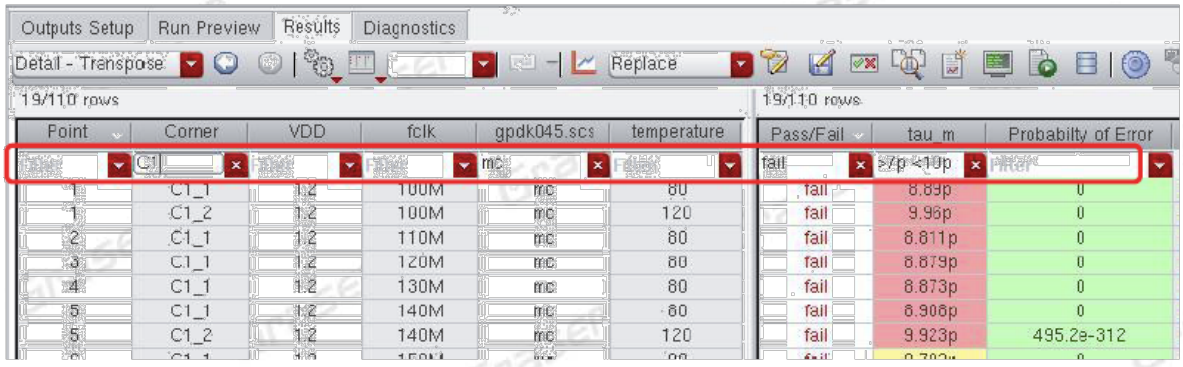

**Variety of waveform displays**

# Cadence® Virtuoso® ADE Assembler

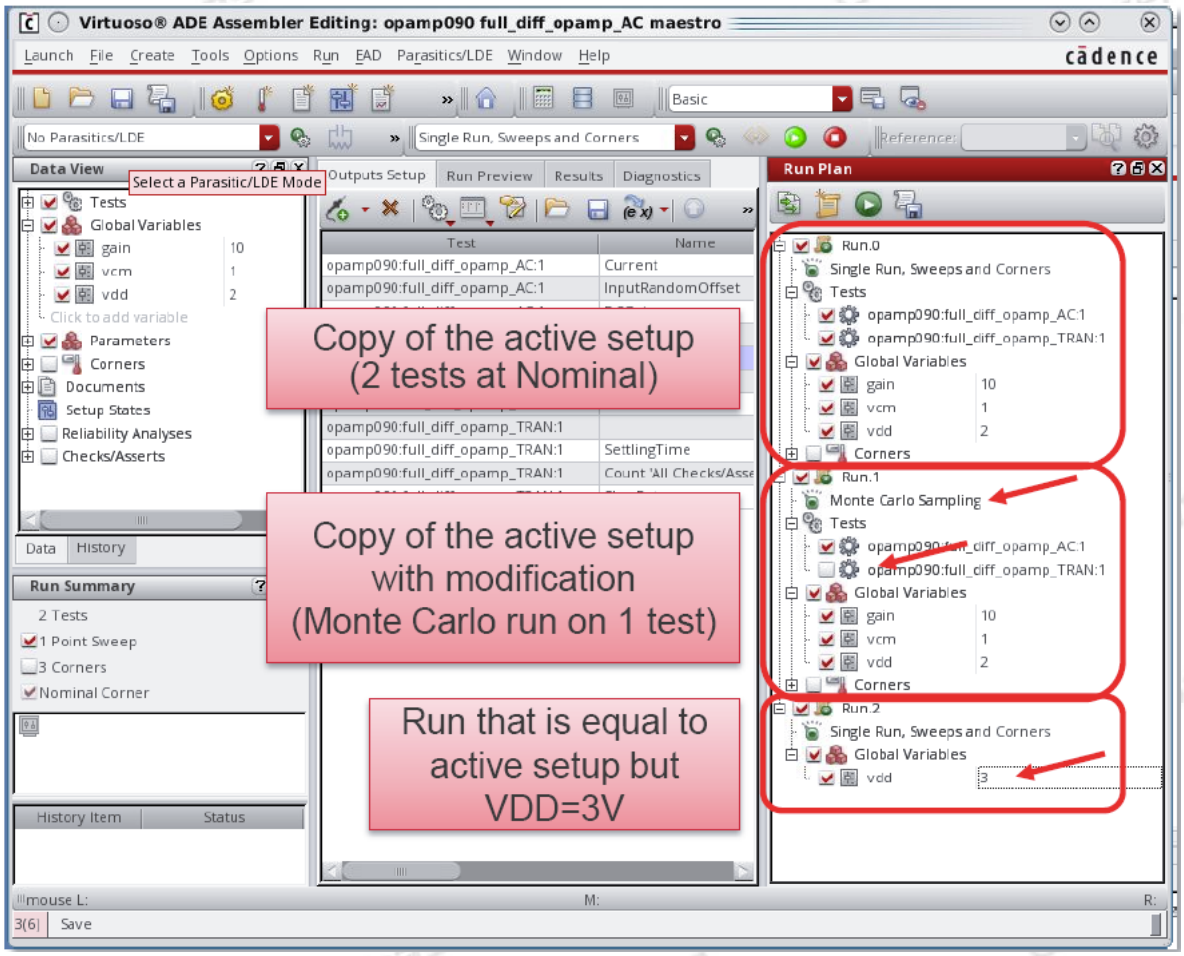
協助工程師在不同的製程–電壓–溫度(PVT) 組合條件分析其設計，並提供基於 GUI 的驗證計畫，因此設計人員能輕鬆地建立條件與相依性模擬。




Cadence® Virtuoso® ADE Assembler cockpit



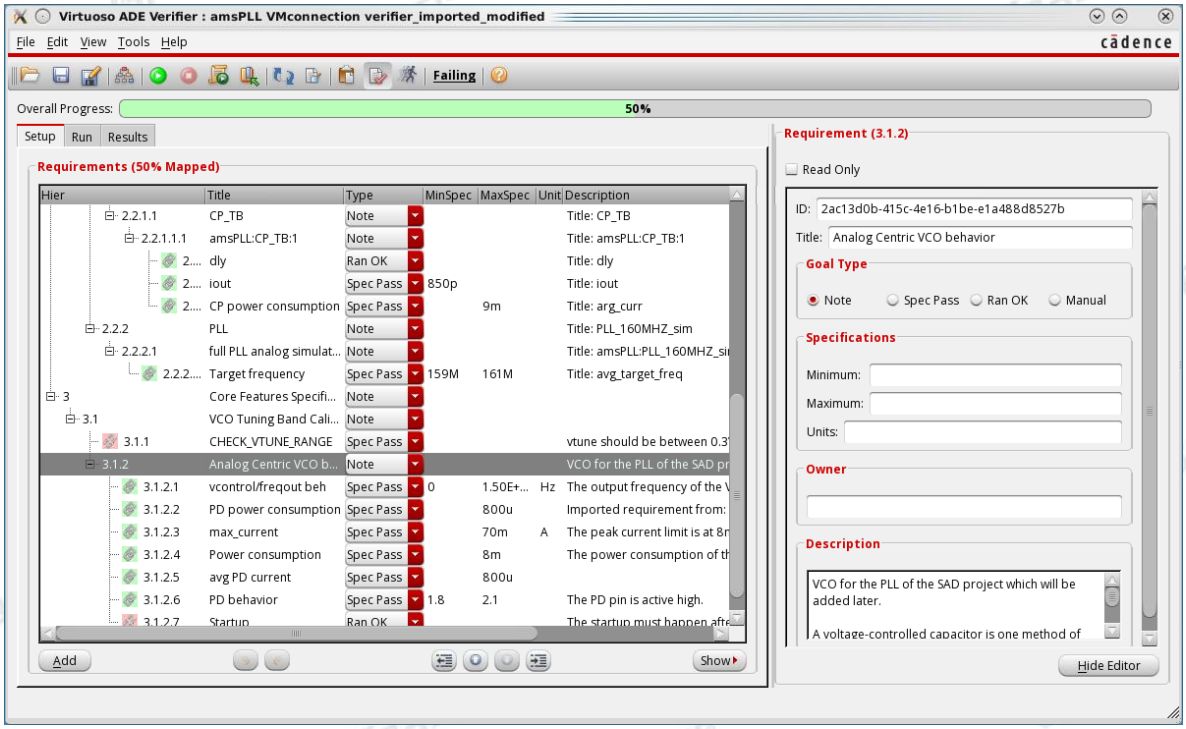

Filtering of results


Virtuoso® ADE Assembler Editing: opamp090 full_diff_opamp_AC maestro
Launch File Create Tools Options Run EAD Parasitics/LDE Window Help
cadence
Basic
No Parasitics/LDE
Single Run, Sweeps and Corners
Reference:
Data View
Select a Parasitic/LDE Mode
Outputs Setup
Run Preview
Results
Diagnostics
Run Plan
Tests
Global Variables
gain 10
vcm 1
vdd 2
Click to add variable
Parameters
Corners
Documents
Setup States
Reliability Analyses
Checks/Asserts
Test
Name
opamp090:full_diff_opamp_AC:1 Current
opamp090:full_diff_opamp_AC:1 InputRandomOffset
opamp090:full_diff_opamp_TRAN:1
opamp090:full_diff_opamp_TRAN:1 SettlingTime
opamp090:full_diff_opamp_TRAN:1 Count 'All Checks/Asse
Copy of the active setup (2 tests at Nominal)
Copy of the active setup with modification (Monte Carlo run on 1 test)
Run that is equal to active setup but VDD=3V
Run.0
Single Run, Sweeps and Corners
Tests
opamp090:full_diff_opamp_AC:1
opamp090:full_diff_opamp_TRAN:1
Global Variables
gain 10
vcm 1
vdd 2
Corners
Run.1
Monte Carlo Sampling
Tests
opamp090:full_diff_opamp_AC:1
opamp090:full_diff_opamp_TRAN:1
Global Variables
gain 10
vcm 1
vdd 2
Corners
Run.2
Single Run, Sweeps and Corners
Global Variables
vdd 3
Data History
Run Summary
2 Tests
1 Point Sweep
3 Corners
Nominal Corner
History Item Status
mouse L: M: R:
3(6) Save

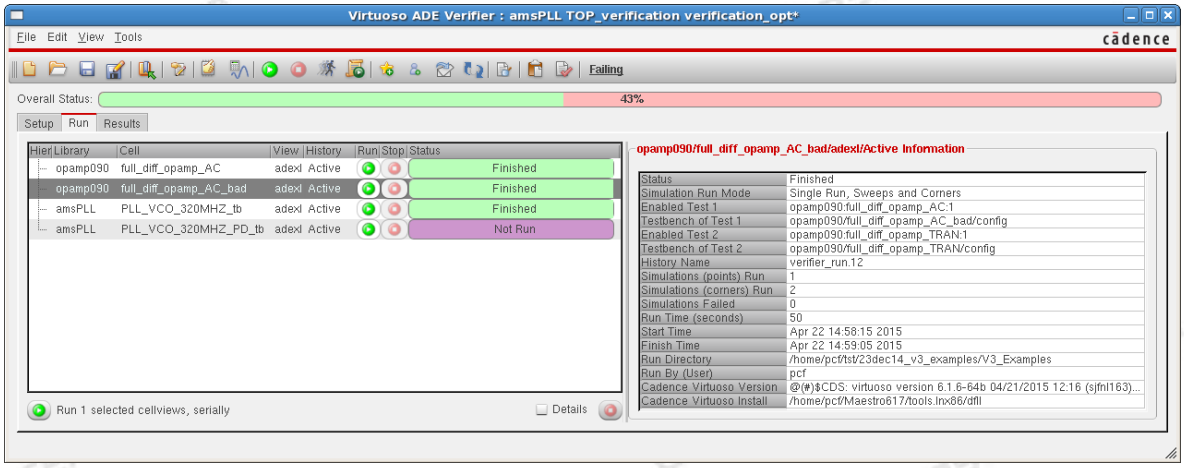
**Run Plan**

# Cadence® Virtuoso® ADE Verifier

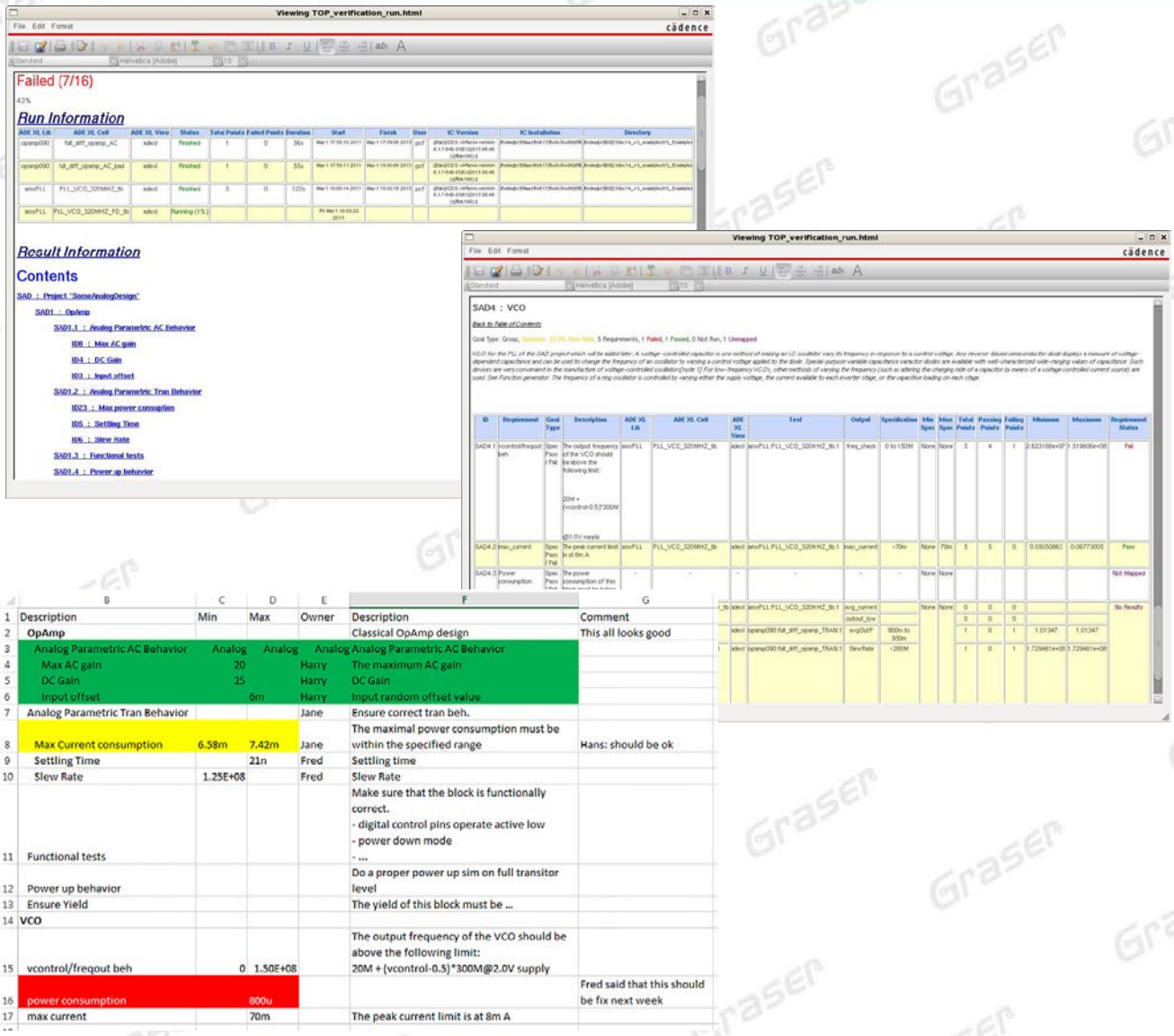
提供一個整合式驗證環境，可讓工程師/產品經理輕鬆連結到與設計有關的所有模塊去進行驗證與分析，進而掌控各模塊的執行進度以執行最佳資源分配。




Cadence® Virtuoso® ADE Verifier cockpit




Cadence® Virtuoso® ADE Verifier job monitor




| | B | C | D | E | F | G |
|---|---|---|---|---|---|---|
| 1 | Description | Min | Max | Owner | Description | Comment |
| 2 | OpAmp | | | | Classical OpAmp design | This all looks good |
| 3 | Analog Parametric AC Behavior | Analog | Analog | Analog | Analog Parametric AC Behavior | |
| 4 | Max AC gain | | 20 | Harry | The maximum AC gain | |
| 5 | DC Gain | | 25 | Harry | DC Gain | |
| 6 | Input offset | | 6m | Harry | Input random offset value | |
| 7 | Analog Parametric Tran Behavior | | | Jane | Ensure correct tran beh. | |
| 8 | Max Current consumption | 6.58m | 7.42m | Jane | The maximal power consumption must be within the specified range | Hans: should be ok |
| 9 | Settling Time | | 21n | Fred | Settling time | |
| 10 | Slew Rate | 1.25E+08 | | Fred | Slew Rate | |
| 11 | Functional tests | | | | Make sure that the block is functionally correct.<br>- digital control pins operate active low<br>- power down mode<br>- ... | |
| 12 | Power up behavior | | | | Do a proper power up sim on full transitor level | |
| 13 | Ensure Yield | | | | The yield of this block must be ... | |
| 14 | VCO | | | | | |
| 15 | vcontrol/freqout beh | 0 | 1.50E+08 | | The output frequency of the VCO should be above the following limit:<br>20M + (vcontrol-0.5)*300M@2.0V supply | |
| 16 | power consumption | | 800u | | | Fred said that this should be fix next week |
| 17 | max current | | 70m | | The peak current limit is at 8m A | |

**Specification comparison sheets and datasheets**