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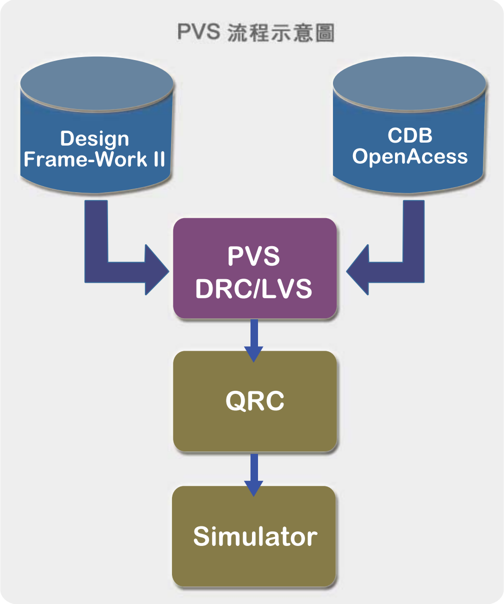
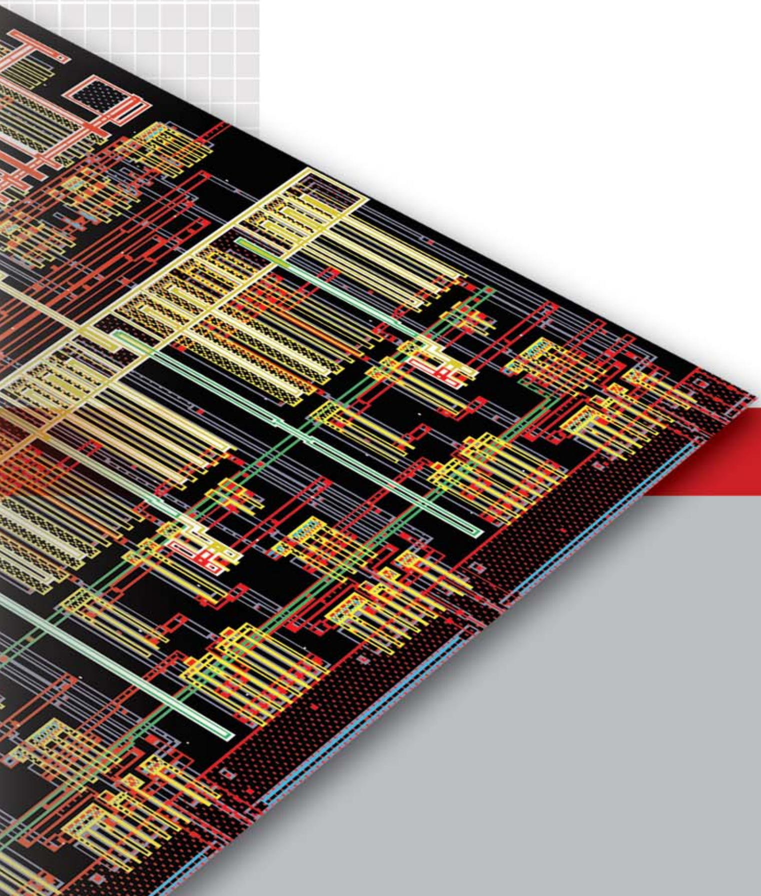
# Cadence Physical Verification System

Cadence® Physical Verification System(PVS) 是由 EDA 軟體商 Cadence 所提出之新一代晶片驗証工具，它不僅能使用於類比 / 數位 / 混合訊號之設計平台，如 Virtuoso IC Layout Platform、Encounter，且更與寄生參數萃取軟體整合，如 QRC，以萃取佈局後寄生參數，提供使用者在晶片後段驗証的完整解決方案。

隨著半導體製程微縮的發展趨勢，晶片後段驗証 (Back-end Verification) 所耗費的處理時間與複雜度不斷提昇的情況下，Cadence® Physical Verification System(PVS) 驗証工具，憑其線性化的優異性能表現 (Performance)，不僅能減少運算處理時的等待時間；另外其創新的即時偵錯 (Time-To-Error) 功能，即時偵錯已運算完成部份，讓使用者不再浪費時間等待運算結果，再者，其新創的人性化圖形除錯界面 (Graphic LVS Debug Interface ) 及互動式短路偵察系統 (Interactive Short Locator)，不僅能有效彌補偵錯經驗不足的困擾，更能有效縮短來回除錯所耗費的時間 (Turn Around Time)，以提昇工程師的效率及晶片產出。

此外，Cadence® Physical Verification System(PVS) 不僅同時支援 GDSII 與 Open-Access 的格式，亦相容於目前工業界標準的驗証語言，以降低工程師跨平台使用上的額外工作與難度。


PVS 流程示意圖



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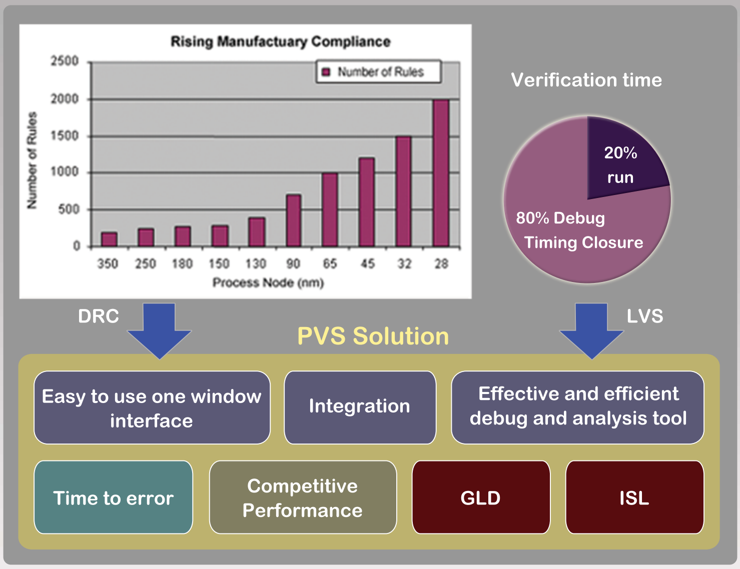


PVS後段驗証解決方案示意圖

**成功經驗**
- 超過50位以上使用客戶，包括晶圓廠及晶片設計公司
- 使用不同晶圓廠之不同製程下投產成功，包括成熟製程，如130/90/65nm及先進製程，如45/40/28nm

**競爭力的性能表現**
- 優異的單一處理器(singleCPU)運算效能
- 支援單機多核心或多機多核心
- 線性化運算處理能力

**有效率的分析及偵錯界面**
- 整合式偵錯環境
  即時偵錯(Time to Error)
- 圖形化除錯界面(Graphic LVS Debug Interface)
- 互動式短路偵查系統(Interactive ShortLoctor)

**跨平台整合**
- 整合Virtuoso customer IC layout platform與Cadence digital IC Encounter platform
- 整合Cadence QRC extraction，提升布局後寄生參數萃取之完整流程

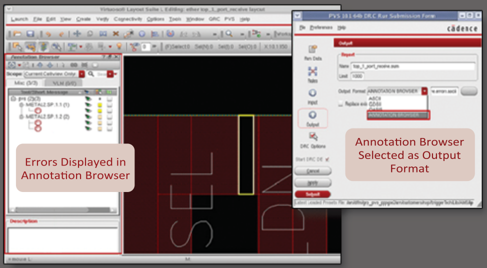
**晶圓廠級的設計服務**
- 配合晶圓廠Process Design Kits(PDK)提供晶片設計所需文件資料
- 相容於台積電驗證之iDRC/iLVS design kits

**轉換無障礙**
- 相似之使用者界面，熟悉度高易上手，操作無障礙
- 內建類似業界標準語法之DRC/LVS命令文檔，相容性高
- 支援業界標準語法之DRC/LVS命令文檔

## 功能介紹

### PVS DRC

- Easy to use one window interface
- Time to error
  -Error Browser will pop up and allow viewing of errors while job is still running.
- Standard DRC Browsing capabilities
  -By Cell/ By Rule
- Error Waivers

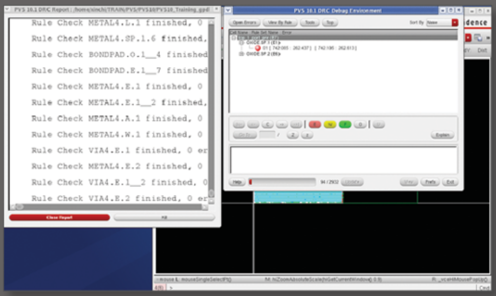


Errors Displayed in Annotation Browser

Annotation Browser Selected as Output Format

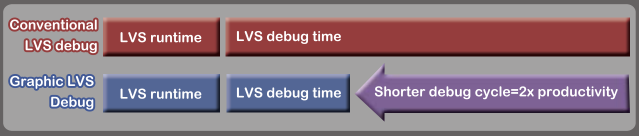
**Time To Error**

Error Browser will pop up and allow viewing of errors while job is still running.



```
PVS 10.1 DRC Report : /home/xinchi/TRAIN/PVS/PVS10/PVS10_Training.gpd
     Rule Check METAL4.L.1 finished, 0
     Rule Check METAL4.SP.1.6 finished,
     Rule Check BONDPAD.O.1__4 finished
     Rule Check BONDPAD.E.1__7 finished
     Rule Check METAL4.E.1 finished, 0
     Rule Check METAL4.E.1__2 finished,
     Rule Check METAL4.A.1 finished, 0
     Rule Check METAL4.W.1 finished, 0
     Rule Check VIA4.E.1 finished, 0 er
     Rule Check METAL4.E.2 finished, 0
     Rule Check VIA4.E.1__2 finished, 0
     Rule Check VIA4.E.2 finished, 0 er
```

### PVS LVS



Conventional LVS debug: LVS runtime | LVS debug time

Graphic LVS Debug: LVS runtime | LVS debug time | Shorter debug cycle=2x productivity

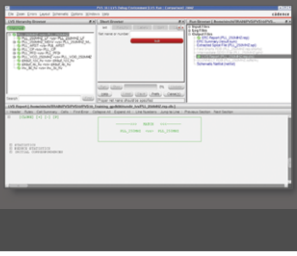
**Rapidly identifies complex LVS mismatches**

**Graphic LVS Debug accelerates identification of complex LVS mismatches in chip designs**

- Compares logical and physical design using a common schematic representation
- Guides navigation using design errors
- Can be launched with LVS debug environment, and graphical elements can be probed through the LVS debug environment
- All errors and warnings are easily navigated and show surrounding context

**Strong functionalities and flexible usability**

- Error Tags
- World view or detail view
- Filter net, devices for better understanding of error
- Drill down for more information on points of interest
- etc



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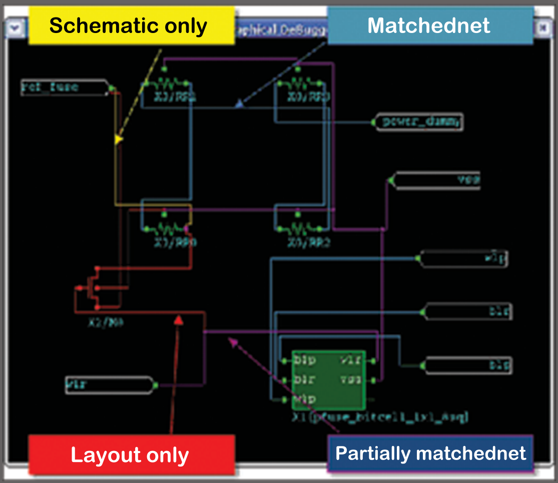
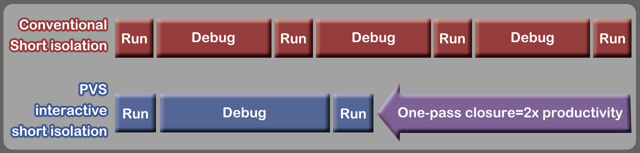
## LVS Hyper debugger --- Graphical LVS Debug

LVS debug is extremely time-consuming and experience dependent

- Limitation of current tools
  - -Static error report in batch mode, contain large data, difficult to understand
  - -Errors in text report hard to identify relationship.
  - -User cannot actively query more information on points of interest
  - -Not allow easy navigation of the original design
- Bind-key --- Cadence Composor like



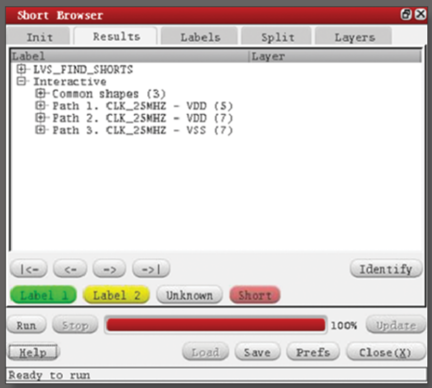
## LVS --- Interactive Short Locator


Conventional Short isolation: Run | Debug | Run | Debug | Run | Debug | Run

PVS interactive short isolation: Run | Debug | Run | One-pass closure=2x productivity

## One-pass short isolation

- Locating shorts found in old-fashion LVS comparison report requires:
  - -Additional manual work
  - -Additional LVS extraction and comparison runs
- PVS approach facilitates one-pass short isolation for cell/block/full-chip designs
  - -Run time typically <10% of extraction time and scales up to 5x with 8 CPUs
  - -Start debugging while run is in progress as soon as first results are available


Short Browser

| Label | Layer |
|---|---|
| ⊞ LVS_FIND_SHORTS | |
| ⊟ Interactive | |
| ⊞ Common shapes (3) | |
| ⊞ Path 1. CLK_25MHZ - VDD (5) | |
| ⊞ Path 2. CLK_25MHZ - VDD (7) | |
| ⊞ Path 3. CLK_25MHZ - VSS (7) | |

Ready to run

## Interactive Short Locator --- Customer Testimony

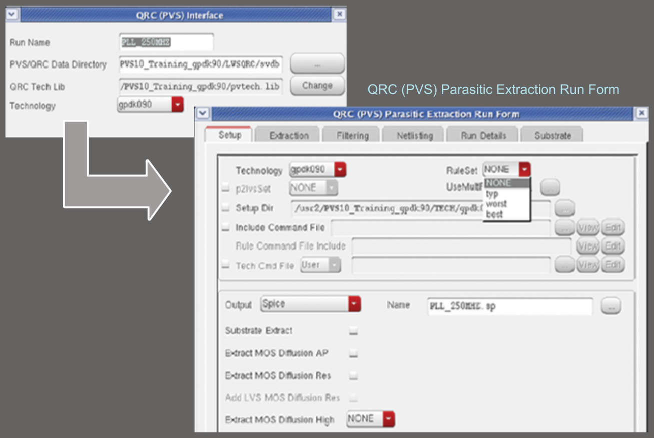
| Node | Extraction Time | TAT wi ISL | TAT wo ISL |
|---|---|---|---|
| 40nm | 1 hr 30 min (8 CPUs) | 30 min | 2 hours |
| 45nm | 1 hr 15 min (8 CPUs) | 3.3 hours | 8 hours |
| 65nm | 1 hr 20 min (8 CPUs) | 20 min<br>428 shrt | NA |

## PVS to QRC interface

Fully solution for back-end verification ---

Support Cadence QRC flow to complete post-layout simulation

- No additional licenses required to enable flow
- Provides complete QRC GUI support
- TECHLIB feature makes PVS QRC flow easy to use
- Batch / interactive use model
- Support Spice, SPEF, DSPF, extracted view, etc. flows
- Parity of flow between PVS / Assura = easy transition


QRC (PVS) Interface

QRC (PVS) Parasitic Extraction Run Form

QRC (PVS) Interface

Run Name: PLL_250MHZ

PVS/QRC Data Directory: PVS10_Training_gpdk90/LVSQRC/svdb

QRC Tech Lib: /PVS10_Training_gpdk90/pvtech.lib

Technology: gpdk090

QRC (PVS) Parasitic Extraction Run Form

Technology: gpdk090

RuleSet: NONE (NONE / typ / worst / best)

□ p2lvsSet: NONE

UseMultF

□ Setup Dir: /usr2/PVS10_Training_gpdk90/TECH/gpdk0

□ Include Command File

Rule Command File Include

□ Tech Cmd File: User

Output: Spice

Name: PLL_250MHZ.sp

Substrate Extract □

Extract MOS Diffusion AP □

Extract MOS Diffusion Res □

Add LVS MOS Diffusion Res □

Extract MOS Diffusion High: NONE