

OrCAD Capture17.2-2016 Design Difference 功能介紹

Cadence[®] 發佈 17.2-2016 新版本中, OrCAD[®] Capture 新增 Design Difference 的功能[,]此功能可以依照電路圖專案或線路圖頁 面中的零件、Net 連線關係、物件屬性與圖形位置做比對。

結果顯示的視窗提示邏輯差異和線路圖中所有的差異;邏輯差異包 括 : 零件、Net 連接、和 Net 屬性設定。所有的差異報表顯示: 電 路圖頁面差異、零件(包含邏輯差異)、Net 連接、Net 屬性設定、 走線線段、跨圖紙連接、和標題欄屬性等。

新的 Design Difference 差異比對功能,可以讓你更快掌握前後版本 設計不同的資訊。

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· Revision :	57°		Gra
Version: Cadence [®] OrCAD [®] V17	7.2 及以後的版本		
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OrCAD Capture – Design Difference

Design Difference 功能差異,可以針 OrCAD[®] Capture 修改前後的電路圖做比對,針對零件(包含零件屬性與位置)、Net 連線關係、Net 屬性設定、Net 線段、跨圖紙連接與標題欄(TitleBlock)等差異做出比對。

功能:

進入 OrCAD Capture / CIS 功能後,開啟任何一份電路圖檔,並且在專案管理視窗中,選擇 Tools
 >> Compare Designs 呼叫 UI 視窗。



2. 進入UI視窗後,先針對要比對的檔案由 Design1及 Design2 的位置選擇,選擇後可透過 Schematic 及 Page 的位置選擇: All (專案頁面全部比對);或是針對特定的 Schematic 資料夾與頁面比對, 當有選定各資料夾或頁面比對,其他未被選擇的頁面將不被比對。 另外針對專案比對後結果,選擇輸出:

HTML Type :

- lightweight HTML:較簡易的 HTML Report, Report 檔案較小。
- portable HTML:完整的 HTML Report, Report 檔案較大,但可以支援在任何電腦中直接
 開啟。

Open With :

支援 Internet Explorer (支援 IE 11 包含以後版本)與 Google Chrome (支援 V45 含以後版本) (建議選項)。



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Design Difference			×
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		Compare	Help

raser 3. 比對完成後,包含 Logical Difference:只包含零件、Net 連線關係、Net 屬性差異報表;與 All Difference:包含更多詳細資訊的報表;與一般資訊,比對的檔案與 Difference 功能選項。

Design Difference Summa	ry		×	
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Pin Net Connectivity	0	Page	7	250.
FlatNet	16	Components(Logical Differences)	2	Gran
		Components(All Differences On Matching Pages Only)	2	
		Pin Net Connectivity	0	
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		Hierarchical Port	0	
		TitleBlock	7	

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F	Page	<all></all>	<all></all>
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		Close	
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4. 在 Summary Report 中, Logical Differences 項目中點選 Show Details,即可使用設定的瀏覽器開啟相關差異結果,透過瀏覽器視窗下方差異項目,雙擊項目後,可直接顯示兩份差異的電路圖檔,差異位置與差異的內容。

透過 Filter 功能,於 Logical Differences 項目中,可查看 Components 及 FlatNets 的差異內容。

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5. 在 Summary Report 中, All Differences 項目中點選 Show Details,即可使用設定的瀏覽器開啟 相關差異結果,透過瀏覽器視窗下方差異項目,雙擊項目後,亦可直接顯示兩份差異的電路圖檔, 差異位置與差異的內容。

透過 Filter 功能,可看見 All Differences 項目中,可查看的差異內容項目較完整包含 Schematic、Page、Components、Wires、OffPages、TittleBlock、FlatNets 及 Pin 差異。透過篩 選,可查看特定差異狀況與連結位置。

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